BRNO UNIVERSITY OF TECHNOLOGY

Faculty of Electrical Engineering
and Communication

MASTER'S THESIS

Brno, 2020 Bc. Samuel Dušek

BRNO UNIVERSITY OF TECHNOLOGY
VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF MICROELECTRONICS
ÚSTAV MIKROELEKTRONIKY

CHANNEL MERGING TECHNIQUES FOR IMPROVING DYNAMIC RANGE OF ± 10 V SIGNAL CHAIN CHANNEL
TECHNIKY SLUČOVÁNÍ KANÁLŮ ZA ÚČELEM ZVÝŠENÍ DYNAMICKÉHO ROZSAHU KANÁLU S ROZSAHEM ±10 V

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

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BRNO 2020

BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

Master's Thesis

Master's study field **Microelectronics**

Department of Microelectronics

Student: Bc. Samuel Dušek ***ID:*** 174281

Year of study: 2 ***Academic year:*** 2019/20

TITLE OF THESIS:

Channel Merging Techniques for improving Dynamic Range of ± 10 V Signal Chain Channel

INSTRUCTION:

Evaluate performance (dynamic range, signal-to-noise ratio, total harmonic distortion) of channel merging technique that uses ±10 V and ±2.5 V channels and was used in Analog Devices part AD7606C. Analyze impact of temperature, offset and gain mismatch together with external RC filters to see impact of external components. Re-design AD7606C programmable gain amplifier so it is able to combine ±10 V and ±1.25 V channels in order to improve dynamic range of ±10 V channel. Investigate options to reduce signal-to-noise ratio loss in ±1.25 V channel due to low input impedance. Investigate and analyze techniques for preventing ±1.25 V channel from saturation. Evaluate obtained results.

RECOMMENDED LITERATURE:

According to recommendations of supervisor

Date of project specification: 3.2.2020 ***Deadline for submission:*** 1.6.2020

Supervisor: Ing. Vilém Kledrowetz, Ph.D.
Consultant: Eamonn Byrne

doc. Ing. Lukáš Fujcik, Ph.D.
Subject Council chairman

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ

Diplomová práce

magisterský navazující studijní obor **Mikroelektronika**

Ústav mikroelektroniky

Student: Bc. Samuel Dušek ***ID:*** 174281

Ročník: 2 ***Akademický rok:*** 2019/20

NÁZEV TÉMATU:

Techniky slučování kanálů za účelem zvýšení dynamického rozsahu kanálu s rozsahem ±10 V

POKYNY PRO VYPRACOVÁNÍ:

Zjistěte základní parametry (dynamický rozsah, poměr signálu k šumu, celkové harmonické zkreslení) techniky slučování kanálů, která byla použita v součástce AD7606C firmy Analog Devices. Vyhodnoťte vliv teploty, různého zesílení a napěťové nesymetrie s různými hodnotami součástek v externím RC filtru. Navrhněte, jak změnit programovatelný zesilovač uvnitř součástky AD7606C tak, aby bylo dosaženo vyšších hodnot dynamického rozsahu za použití kanálů s rozsahem ±10 V a ±1,25 V. Navrhněte, jak potlačit vliv ±1,25 V kanálu na zhoršení poměru signál-šum kvůli jeho nižší vstupní impedanci. Vyšetřete a analyzujte techniky prevence proti saturaci ±1,25 V kanálu. Vyhodnoťte dosažené výsledky.

DOPORUČENÁ LITERATURA:

Podle pokynů vedoucího práce

Termín zadání: 3.2.2020 ***Termín odevzdání:*** 1.6.2020

Vedoucí práce: Ing. Vilém Kledrowetz, Ph.D.
Konzultant: Eamonn Byrne

doc. Ing. Lukáš Fujcik, Ph.D.
předseda oborové rady

ABSTRACT

The aim of this master's thesis is to measure and evaluate the performance of the channel merging technique which is currently implemented on the Analog Devices part called AD7606C. Then, based on the results from measurement, propose, design, and simulate options to improve this technique in terms of dynamic range and total harmonic distortion performance. It was discovered that by increasing the gain of the lower range channel together with decreasing the cutoff frequency of the whole signal chain, the currently implemented channel merging technique might be able to achieve 118.6 dB of dynamic range which is about 3.6 dB more than was measured on the AD7606C. Also, by implementing a simple algorithm in the internal logic block together with small additional circuitry, the immunity towards the value of the external resistor, that customers use as a part of the anti-aliasing filter, was achieved.

KEYWORDS

dynamic range, signal chain, signal-to-noise ratio, channel, merging, saturation, total harmonic distortion

ABSTRAKT

Cílem této diplomové práce je změřit a vyhodnotit parametry techniky slučování kanálů, která je momentálně implementována v součástce AD7606C firmy Analog Devices. Poté, na základě výsledků z měření, navrhnout a odsimulovat několik možností, pomocí kterých by tato technika mohla dosahovat vyšších hodnot dynamického rozsahu a celkového harmonického zkreslení. V průběhů práce bylo zjištěno, že pomocí zvýšení zesílení kanálu s nižším rozsahem společně se snížením mezní frekvence celého signálového řetězce může tato technika dosahovat až 118.6 dB dynamického rozsahu, což je o 3.6 dB více, než bylo změřeno na AD7606C. Dále také bylo zjištěno, že pomocí jednoduchého algoritmu implementovaného v logickém bloku, je možné dosáhnout imunity vůči hodnotě externího rezistoru, který zákazníci používají jako součást anti-aliasingového filtru.

KLÍČOVÁ SLOVA

dynamický rozsah, signálový řetězec, poměr signálu k šumu, kanál, slučování, saturace, celkové harmonické zkreslení

SAMUEL, Dušek. *Channel merging techniques for improving dynamic range of ± 10V signal chain*. Brno, 2020, 86 p. Master's Thesis. Brno University of Technology, Faculty of Electrical Engineering and Communication, Department of Microelectronics. Advised by Ing. Vilém Kledrowetz, Ph.D.

ROZŠÍŘENÝ ABSTRAKT

ÚVOD

Předmětem této diplomové práce bylo změřit a vyhodnotit parametry techniky slučování kanálů, která byla implementována do součástky AD7606C firmy Analog Devices. AD7606C je osmi kanálová součástka, ve které každý kanál obsahuje jeden programovatelný zesilovač (PGA) a jeden analogově digitální převodník (ADC) s postupnou aproximací (SAR) a s maximální frekvencí převodu 800 kHz.

Na základě výsledků z měření bylo dalším úkolem navrhnout možnosti, jak tuto techniku vylepšit se zaměřením na dynamický rozsah (DR). V průběhu měření bylo rovněž zjištěno, že tato technika je velmi citlivá na hodnotu odporu, který zákazníci předřazují před PGA jako součást anti-aliasingového filtru. Jelikož citlivost na hodnotu předřadného odporu výrazně redukuje možnosti použití této techniky, byly rovněž navrženy možnosti, jak tuto citlivost potlačit.

Jednotlivé návrhy byly následně řádně simulovány a výsledky ze simulací srovnány s výsledky získaných během měření. V závěru této práce byly jednotlivé návrhy porovnány a byl vybrán ten nejlepší s ohledem na složitost případné implementace a dosažených parametrů.

POPIS ŘEŠENÍ

Měření momentálně implementované techniky bylo realizováno v laboratořích firmy Analog Devices. K měření byla použita vývojová deska pro testování čipů z produktové řady AD7606X, velice přesný zdroj testovacího signálu, zdroj napájecího napětí, zdroj taktovacího signálu a zdroj tepelný, který umožňoval realizovat jednotlivá měření i pro různé teploty. Data z měření pak byla zaznamenávána pomocí PC stanice.

Z takto provedeného měření bylo zjištěno, že momentálně implementovaná technika je schopna dosáhnout 115 dB dynamického rozsahu s poměrem převzorkování (OSR) nastaveným na 256, což je o 5 dB více ve srovnání se samostatně pracujícím kanálem. Rovněž bylo zjištěno, že hodnota celkového harmonického zkreslení (THD) je stabilní do hodnoty předřadného odporu 100 Ω. Po této hodnotě pak s jejím růstem THD klesá.

Pro dosažení vyšších hodnot dynamického rozsahu byly navrženy a simulovány celkem 3 řešení. První řešení počítá s možností snížení mezní frekvence PGA, čímž dojde ke snížení celkového šumu v systému, navýšení hodnoty poměru signálu k šumu (SNR) a tím i ke zvýšení DR. Druhé řešení navrhuje snížení rozsahu druhého kanálu z ±2.5 V na ±1.25 V a to snížením hodnoty vstupního odporu PGA na polovinu. Třetí řešení pak kombinuje obě již představená řešení.

Pro dosažení imunity THD vůči hodnotě předřadného odporu PGA byly navrženy tři řešení. První řešení mění zesílení PGA druhého kanálu v závislosti na hodnotě vstupního signálu, tímto dochází k prevenci před saturací tohoto kanálu. Druhé

řešení navrhuje odpojit druhý kanál pokaždé, když vstupní signál přesáhne hodnotu vstupního rozsahu druhého kanálu. Poslední představené řešení navrhuje rovněž odpojení druhého kanálu v případě, kdy vstupní signál je mimo vstupní rozsah tohoto kanálu. Avšak po odpojení je druhý kanál okamžitě připojen ke navzorkované hodnotě vstupního signálu těsně před momentem, kdy vstupní signál opouštěl rozsah druhého kanálu.

SHRNUTÍ A ZHODNOCENÍ VÝSLEDKŮ

Celkově tedy byly navrženy a simulovány tři možnosti, jak zvýšit maximálně dosažitelnou hodnotu dynamického rozsahu. Jako nejatraktivnější se ukázala možnost třetí, neboť právě s touto možností bylo dosaženo 118.6 dB dynamického rozsahu, což je o 3.6 dB více než s momentálně implementovanou technikou. Ovšem, možnost snížení mezní frekvence PGA má vliv pouze do hodnoty OSR 64. Pracuje-li ADC s vyšší hodnotou OSR než 64, snižování mezní frekvence PGA nemá pro dosažení vyšších hodnot DR žádný význam.

Pro dosažení imunity THD vůči hodnotě předřadného odporu byly rovněž navrženy a simulovány 3 možnosti. Všechny tři představené možnosti byly schopny potlačit vliv předřadného odporu na hodnotu THD. Možnost třetí, tedy připojování druhého kanálu na navzorkovanou hodnotu vstupního signálu ve chvíli kdy vstupní signál je mimo rozsah druhého kanálu, dosahovala nejlepších výsledků, neboť byla schopna potlačit i další nežádoucí jev a to pokles hodnoty THD se vzrůstající frekvencí vstupního signálu. Bohužel, možnost třetí vyžaduje přidání velkého množství dalších obvodů a tím výrazně zvyšuje složitost implementace. Z tohoto důvodu byla pro budoucí možnou implementaci vybrána možnost druhá. Ta navrhuje odpojení druhého kanálu od prvního v momentu, kdy je vstupní signál mimo rozsah druhého kanálu.

ACKNOWLEDGEMENT

I would like to thank the Analog Devices company for giving me an opportunity to be its part for one whole year as a co-op student. Namely, I would like to thank to Paraic Brannik, Pawel Czapor, Eamonn Byrne and Jesus Bonache for their guidance regarding this master's thesis and for their time, patience and knowledge they were willing to share with me during the whole year. Finally, I also would like to thank to Ing. Vilém Kledrowetz, Ph.D. for his feedback and guidance regarding formal aspects of this thesis.

Brno ....

author's signature

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Introduction

One of the challenges that engineers of the integrated circuits must face is building a signal chain that has high specification performance when the input signal is within certain limits, for instance, ±2.5 V, and is also able to maintain performance as good as possible when the input signal is outside of these specified limits.

This is highly requested by some Analog Devices customers as the signal, which they want to process, might be in the range of ±10 V, but most of the time is actually in the range of ±2.5 V.

It might be the case that the customer's signal should most of the time be in the range of ±2.5 V, but because of some unexpected event, a fault condition with voltage levels outside of the ±2.5 V range might occur as well. An example of a situation like this can be seen in figure 1.

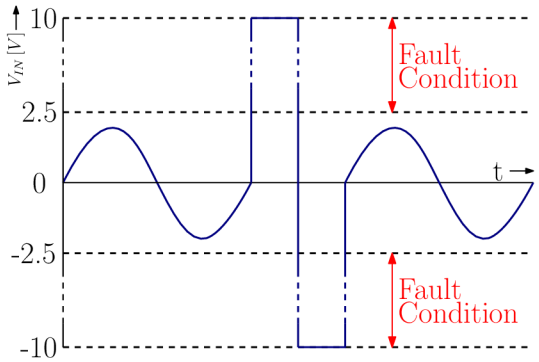

Fig. 1: Signal with fault condition

The Analog Devices company has already implemented a technique that uses two channels to build one signal chain with such a performance. This diploma thesis aims to measure and evaluate the performance of the currently implemented channel merging technique and propose, design and simulate possible improvements to this approach.

The first part of this thesis presents the currently implemented channel merging technique and its dynamic range (DR) and total harmonic distortion (THD) performance.

The second part then proposes 3 options to improve the DR performance and evaluates obtained results.

The last part deals with the undesirable phenomenon when the THD performance is decreasing due to the increasing value of the external resistor which the Analog Devices customers use as a part of the anti-aliasing filter in front of the AD7606C.

While working on this diploma thesis, internal and confidential documents from the Analog Devices company have been used. Therefore, few of the cited documents in the bibliography section can not be found anywhere in public space.

1 Currently implemented channel merging technique

At the time of writing this diploma thesis, company Analog Devices is developing part AD7606C that will be another generic of AD7606X family[1][2]. AD7606C has an option to merge two of its channels in order to improve the overall DR of $\pm 10\,\mathrm{V}$ signal chain.

As can be seen in figure 1.1 currently implemented solution uses 2 channels of the AD7606C part. Channel 1 is set to $\pm 2.5\,\mathrm{V}$ range and channel 2 is set to $\pm 10\,\mathrm{V}$ range. Internal logic block then reads the output codes of channel 2 and based on their values decides whether to use codes from channel 1 or channel 2.

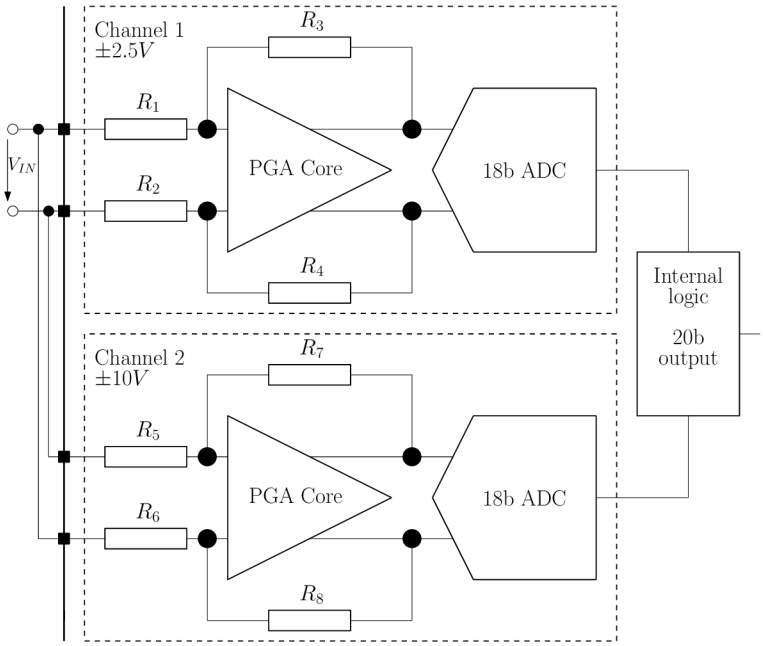

Fig. 1.1: Block diagram of the currently implemented channel merging technique in AD7606C

When the input voltage V_{IN} is within the range of $\pm 2.5\,\mathrm{V}$ channel the internal logic block outputs codes directly equal to codes from this channel. On the other hand, when the input voltage V_{IN} is outside of the $\pm 2.5\,\mathrm{V}$ range, the internal logic block outputs codes from the $\pm 10\,\mathrm{V}$ channel shifted by 2 to the left [3].

$$Code_{output} = \begin{cases} Code_{2.5} & V_{IN} \in <-2.5, 2.5> \\ Code_{10} \ll 2 & V_{IN} \in <-10; -2.5) \cup (2.5; 10> \end{cases} \tag{1.1}$$

Extra DR that can be potentially gained using this technique is given by the following equation[3].

$$DR_{EXT} = 20 \times log\left(\frac{10}{2.5}\right) = 12dB \tag{1.2}$$

As can be seen in equation 1.2, the ideal extra DR should be 12 dB. This extra DR is added to the DR of ± 10 V by itself and thus overall DR of the whole signal chain is improved.

In order to prove this theory, measurements on AD7606C silicon were performed. How these measurements were performed and what results have been obtained is described in chapter 2.

2 Measurements of the current solution

All measurements, that are being presented in following sections 2.1, 2.2 and 2.3, were performed in one of Analog Devices laboratories, where the setup, that is depicted in figure 2.1, had been built.

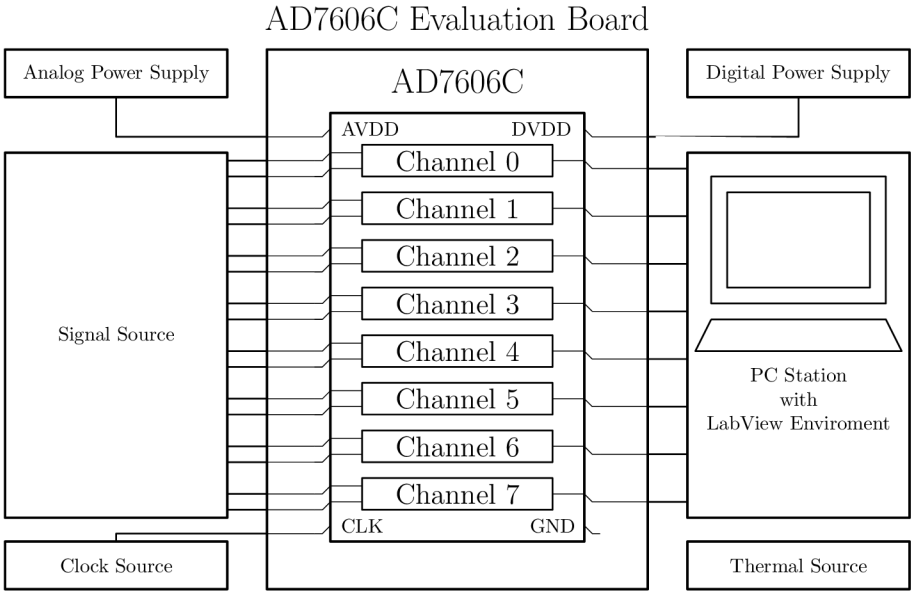

Fig. 2.1: Simplified block diagram of setup that was used for measuring the DR of the AD7606C

It is necessary to bear in mind that block diagram in figure 2.1 is simplified and for example does not show any of the complex circuitry on the evaluation board.

It is also worth noticing that thermal source was available in this setup. Thus, this allowed measurements to be made for different temperatures as can be seen in subsection 2.3.3.

2.1 Dynamic range measurements

The DR of AD7606C was measured using the setup shown in figure 2.1 and LabView environment that had been developed by Analog Devices and that is able to read and write data from and to AD7606C.

The data that has been gathered is following.

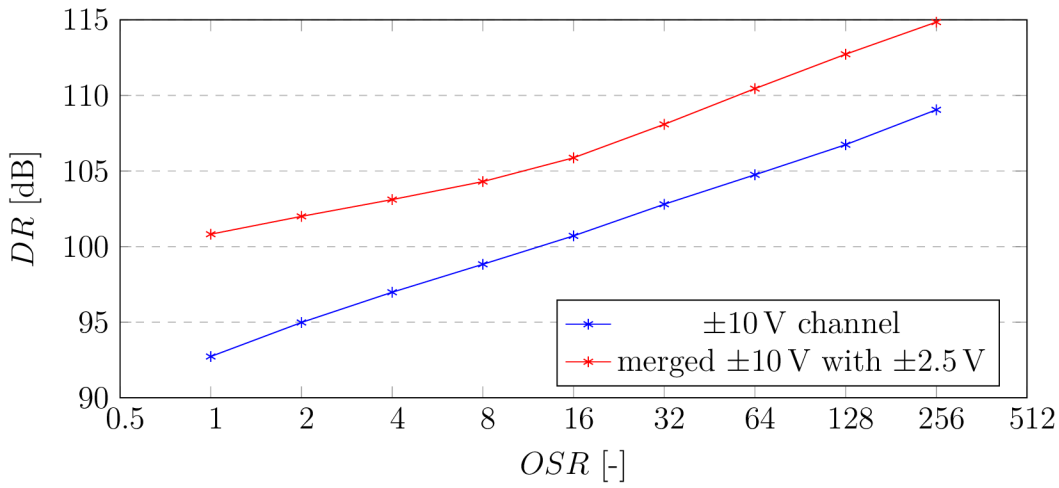

Fig. 2.2: The DR performance of the ±10 V channel and the ±10 V and ±2.5 V merged channels

As can be noticed in figure 2.2, the highest DR achievable by currently implemented channel merging technique is 115 dB with oversampling ratio (OSR) equal to 256. On the other hand, it can also be noticed that the highest DR, that can be achieved by ±10 V channel itself is 110 dB with OSR equal to 256. That is only extra 5 dB that have been gained by this technique, which is not what had been expected according to equation 1.2.

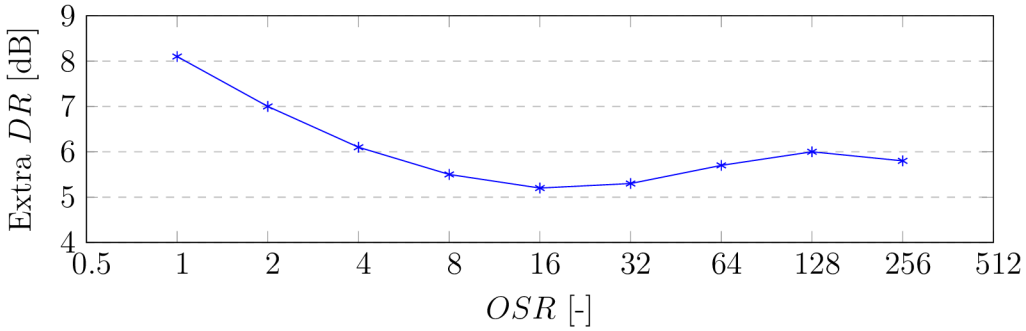

Fig. 2.3: The extra DR gained by merging the ±10 V and the ±2.5 V channels

Figure 2.3 shows the extra DR that was gained by implementing the channel merging technique described in chapter 1 versus OSR. As can be seen, the extra DR is lower than expected 12 dB. In order to understand why extra 12 dB is not achieved it is necessary to have a look at equation for final DR when merging ±10 V with ±2.5 V channel [3].

$$DR = SNR_{10} + \left(20 \times log\left(\frac{10}{2.5}\right) - (SNR_{10} - SNR_{2.5})\right) \tag{2.1}$$

It can be seen in equation 2.1 that the final DR when merging ±10 V with ±2.5 V channel also depends on the signal-to-noise ratio (SNR) of the ±2.5 V channel and if the SNR of the ±2.5 V channel is not equal to the SNR of the ±10 V channel, then the difference must be subtracted from the expected 12 dB.

2.2 Signal-to-noise ratio measurements

In order to get a better idea about why the final DR of presented channel merging technique is dependent on the SNR of both channels, measurements of the SNR of both channels, ±10 V and ±2.5 V, were performed using the setup described in figure 2.1. The gathered data is shown in figure 2.4.

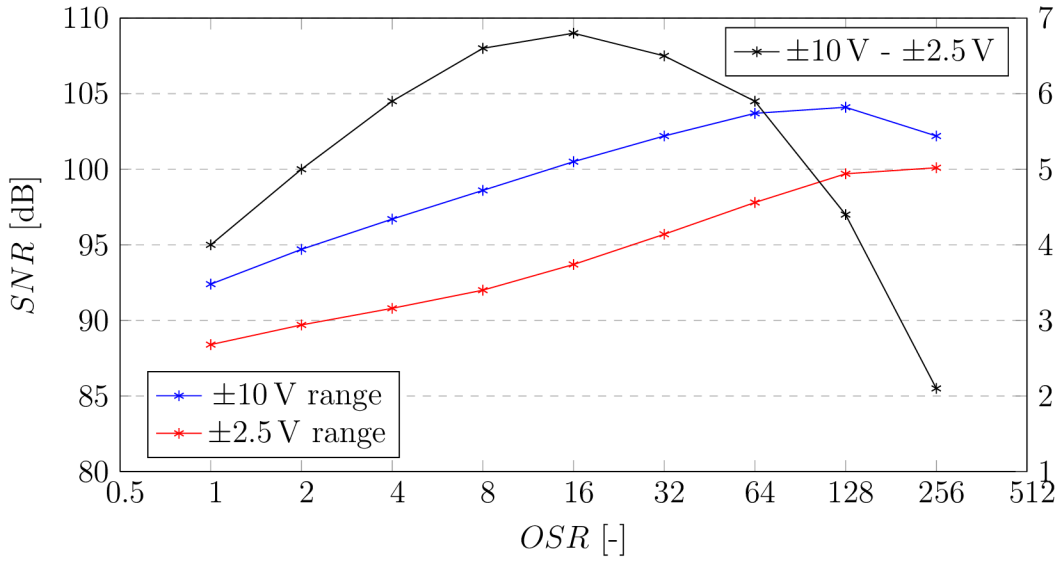

Fig. 2.4: The SNR performance of the ±10 V channel and the ±2.5 V channel and their difference

It can be noticed that the SNR of the ±10 V range is higher than the SNR of the ±2.5 V range and thus the difference is not equal to 0. The reason why the SNR of the ±2.5 V range is different might be explained by looking at equation 2.2 for the SNR of the whole signal chain including PGA and ADC as it is being shown in figure 1.1.

$$SNR = 20 \times log\left(\frac{\frac{V_{REF}}{\sqrt{2}}}{\sqrt{{n_{PGA}}^2 + {n_{ADC}}^2 + {n_Q}^2}}\right) \tag{2.2}$$

In equation 2.2 V_{REF} is ADC reference voltage, n_{PGA} is RMS noise of the whole PGA and can be derived using equation 2.3, n_{ADC} is RMS noise of the ADC and

n_Q is RMS value of the quantization noise.

$$n_{PGA} = \sqrt{\left[n_{RIN} \times G \times \sqrt{\frac{\pi}{2} \times f_{3db}}\right]^2 + \left[n_{RFB} \times \sqrt{\frac{\pi}{2} \times f_{3db}}\right]^2 + {n_{PGACORE}}^2} \quad (2.3)$$

In equation 2.3 n_{RIN} is the noise spectral density of the input resistor R_{IN}, G is set gain of the PGA, f_{3db} is the cutoff frequency of the PGA, n_{RFB} is the noise spectral density of the feedback resistor R_{FB} and $n_{PGACORE}$ is the RMS noise of the PGA core.

As V_{REF}, n_{ADC} and n_Q are the same for all ranges of the PGA, the main reason why the SNR of the $\pm 10\,\mathrm{V}$ range is different from the SNR of the $\pm 2.5\,\mathrm{V}$ range is value of n_{PGA} that is given by equation 2.3.

The main contributor to the difference between the RMS noise of the $\pm 2.5\,\mathrm{V}$ range PGA and $\pm 10\,\mathrm{V}$ range PGA is the feedback resistor R_{FB} that is $4\times$ higher in case of the $\pm 2.5\,\mathrm{V}$ range PGA. The reason for that is that the feedback resistor sets the the overall gain G of the PGA that is needed in order to convert the input signal going from $-2.5\,\mathrm{V}$ to $2.5\,\mathrm{V}$ to levels that are accepted by the ADC. This gain G can be derived using following equation [3].

$$G = \frac{R_{FB}}{R_{IN}} \quad (2.4)$$

It can be noticed in equation 2.3 that gain G multiplies the noise spectral density n_{RIN} of the input resistor R_{IN}. Thus, because of higher value of the feedback resistor R_{FB} the noise contribution of the input resistor R_{IN} is also increased. Higher value of the feedback resistor R_{FB} and thus higher gain of the $\pm 2.5\,\mathrm{V}$ range PGA are 2 main reasons why the SNR of the $\pm 2.5\,\mathrm{V}$ range is lower than the SNR of the $\pm 10\,\mathrm{V}$ range and why we do not see expected extra DR of 12 dB.

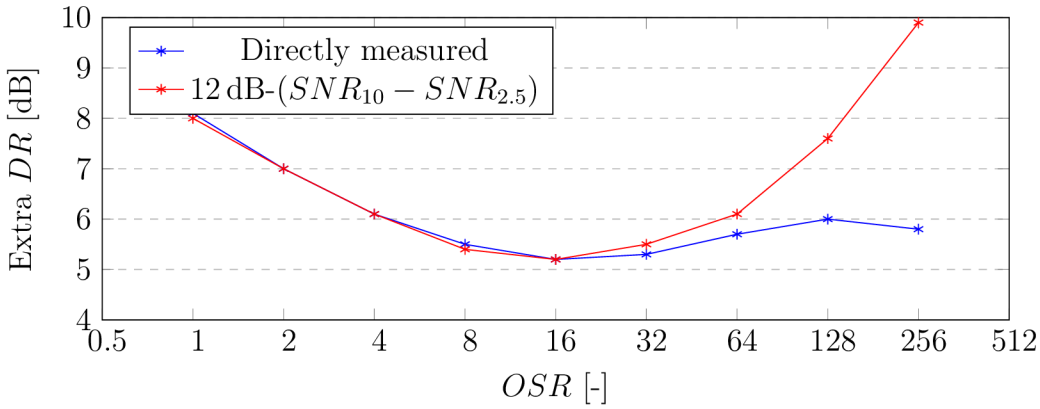

Fig. 2.5: Measured and derived extra DR gained by merging the $\pm 10\,\mathrm{V}$ and the $\pm 2.5\,\mathrm{V}$ channels

In figure 2.5 the measured extra DR is compared to the expected extra DR that was derived using the measured SNR values for both ranges $\pm 10\,\mathrm{V}$ and $\pm 2.5\,\mathrm{V}$. It can be seen that the expected values match with measured values up to OSR equal to 64. With OSR equal to 128 and 256 the difference between both values increases. This is probably due to the fact that with OSR equal to 128 and 256 the spread of codes that are being send to LabView environment is that low that the calculations of DR are not 100 % accurate.

The early conclusion from this section might be that with channel merging technique that is currently implemented on silicon it is possible to achieve 115 dB with OSR equal to 256. The ways to improve this technique, which mean increasing the DR, are evident from equations 2.1, 2.2 and 2.3. One option is to decrease range of lower range channel from $\pm 2.5\,\mathrm{V}$ to $\pm 1.25\,\mathrm{V}$. Another option is to decrease the cutoff frequency. How to put these options in to practice and what performance might be gained using these options is described in the chapter 3.

2.3 Total harmonic distortion measurements

Another way how to evaluate performance of currently implemented channel merging technique that can be seen in figure 1.1 is to connect sine wave source to the input of the signal chain and measure the (THD) of the signal in the output of the signal chain. As the output signal is being built by the internal logic block from the codes from $\pm 2.5\,\mathrm{V}$ and $\pm 10\,\mathrm{V}$ channels, there are few sources of errors that might decrease overall THD performance of the whole signal chain [3].

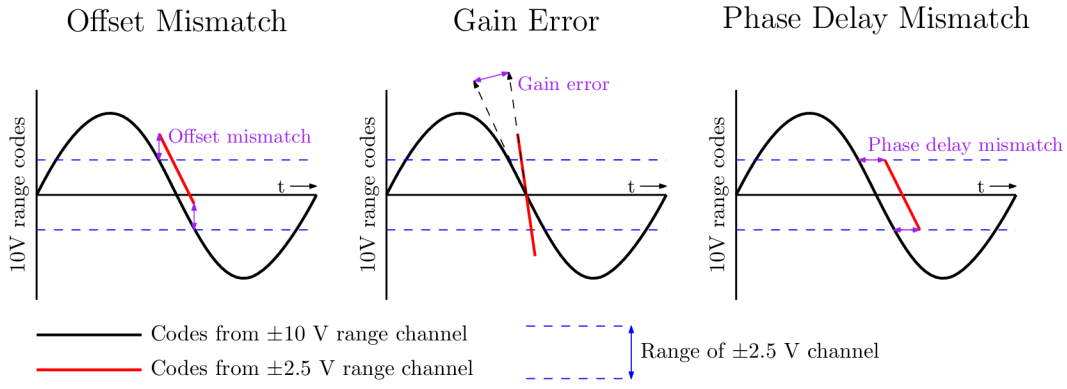

Fig. 2.6: Potential sources of distortion when using channel merging technique

The first source of error and thus potential reason of decreased THD is offset mismatch. If the $\pm 2.5\,\mathrm{V}$ channel has different offset value than the $\pm 10\,\mathrm{V}$ channel, codes from $\pm 2.5\,\mathrm{V}$ will be shifted up or down and the final signal, that is being built by the internal logic block, will be distorted as it is shown in figures 2.6 and 2.7.

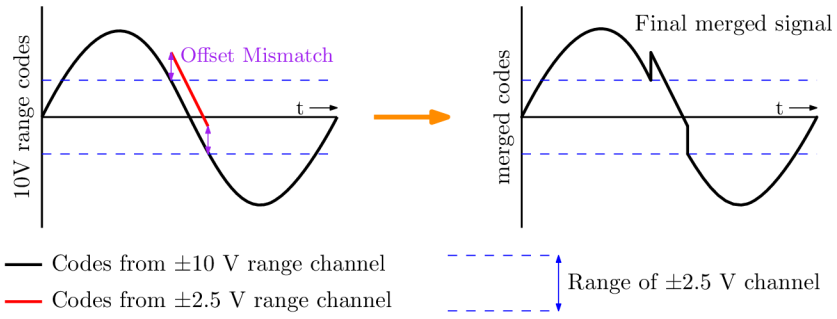

Fig. 2.7: Distortion due to offset mismatch

It is obvious from figure 2.7 that it is desirable for both channels to have the same offset value. To evaluate how sensitive this channel merging technique is to the offset mismatch between both channels several measurements were performed and can be seen in subsection 2.3.1.

The second source of error and thus potential reason of decreased THD performance is the gain error. Both channels are set to different gain that is given by equation 2.4. It is clear that due to process mismatch and variation, the input resistor R_{IN} and the feedback resistor R_{FB} might have slightly different values from part to part and even from channel to channel. Thus, if the $\pm 2.5\,\mathrm{V}$ has slightly different gain G from its ideal value, undesirable distortion might occur.

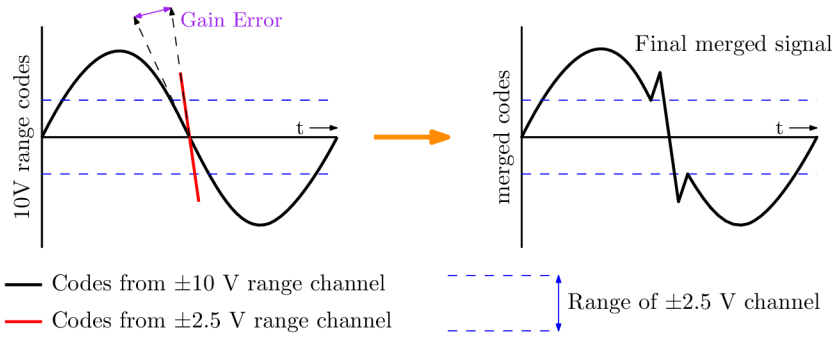

Fig. 2.8: Distortion due to gain error

As it can be seen in figure 2.8, it is desirable to have gain error as low as possible. To have better understanding how sensitive to gain error currently implemented channel merging technique is few measurements were taken and are presented in subsection 2.3.2.

Final source of error directly related to the principle of this channel merging technique is the phase delay mismatch as it is shown in figure 2.6. Both channels

shown in figure 1.1 have certain value of the cutoff frequency $f_{3\mathrm{dB}}$ that is given by following equation.

$$f_{3dB} = \frac{1}{2\pi R_{FB} C_{FB}} \tag{2.5}$$

The feedback capacitor C_{FB} is not being shown in figure 1.1 but in real schematic it is connected in parallel with the feedback resistors R_{FB}. As it was in the case of the gain error, due to the process mismatch and variation the values of the feedback resistor R_{FB} and capacitor C_{FB} might vary from part to part and even from channel to channel. This means that both channels might have different value of the cutoff frequency and thus different phase response. In other words, the input signal with certain frequency f_{IN} might be delayed by certain time when going through the $\pm 2.5\,\mathrm{V}$ channel and by different time when going through the $\pm 10\,\mathrm{V}$ channel. This effect might result in distortion as it is shown in figure 2.9.

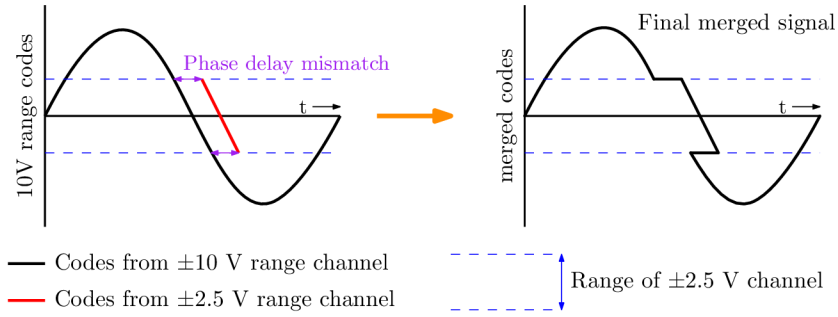

Fig. 2.9: Distortion due to phase delay mismatch

It is then clear that the cutoff frequency $f_{3\mathrm{dB}}$ of both channels should be matched as precisely as possible. However, the Analog Devices part AD7606C has no option to trim the cutoff frequency and because of that there is no option how to measure THD versus phase delay mismatch. Nevertheless, it is clear that the $f_{3\mathrm{dB}}$ mismatch has impact on the THD performance and it would be worth implementing trimming of the $f_{3\mathrm{dB}}$ frequency on each channel separately to maximize the THD performance of this channel merging technique.

2.3.1 Total harmonic distortion versus offset mismatch

Analog Devices part AD7606C has an option to trim the offset value of each channel separately. This feature was then used to measure sensitivity of currently implemented channel merging technique to the offset mismatch. By changing value

in appropriate register of AD7606C the offset value of the ±2.5 V channel was altered and then the THD was measured. By this procedure following plot has been obtained.

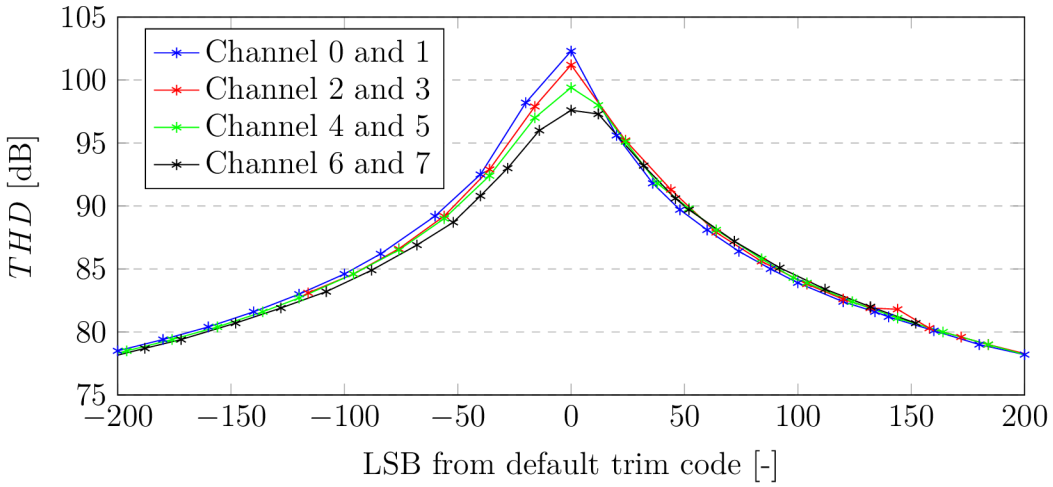

Fig. 2.10: The THD performance versus offset mismatch between the ±10 V and ±2.5 V channels

In figure 2.10 THD versus offset mismatch can be seen. To fully understand this figure it is necessary to explain what the horizontal axis x means. Every part, after being manufactured, has to be tested. Part of the testing procedure is also trimming of the offset mismatch and the gain error. After trimming procedure, the best trim codes are then stored in appropriate registers to give the part best possible performance. Thus, on the horizontal axis in figure 2.10 we can see the difference of offset values from offset value that has been set by the trimming procedure in the test.

Also, it is important to mention that AD7606C has overall 8 stand-alone channels. When channel merging is being used in order to enhance performance of the ±10 V range option, two channels are merged together and are used as one. This is the reason why there are 4 curves in figure 2.10.

Two main conclusions might be drawn from figure 2.10.

- Trimming procedure that is implemented in test of AD7606C works well as the best THD performance is achieved with default trim codes.
- As long as the offset mismatch is within ±48 LSBs from the ideal value, the minimum THD of 90 dB is achieved.

2.3.2 Total harmonic distortion versus gain error

As it was mentioned in previous subsection, AD7606C has an option to trim gain G off all channels separately. To the benefit of this work, this feature was used to alter gains of $\pm 2.5\,\mathrm{V}$ channels to see how sensitive the currently implemented channel merging technique is to the gain error.

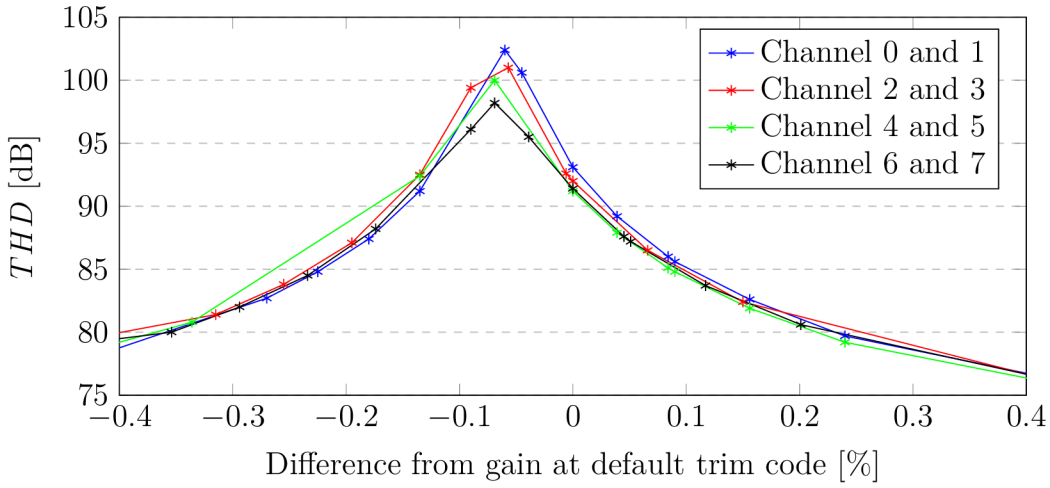

Fig. 2.11: The THD performance versus gain error between the $\pm 10\,\mathrm{V}$ and $\pm 2.5\,\mathrm{V}$ channels

To understand the plot in figure 2.11 it is appropriate to explain its horizontal axis x. This axis shows difference between gain that corresponds to trim code that has been set by trimming procedure in test and gain that was set by altering trim code during measurements. This difference is then divided by the gain value that corresponds to trim code from test and multiplied by 100 to get percentage.

Two main conclusions might be drawn from figure 2.11.

- In this case trimming procedure that is implemented in test of AD7606C did not set the most appropriate trim code in order to achieve best THD performance.
- As long as the gain of $\pm 2.5\,\mathrm{V}$ channel is within $\pm 0.08\,\%$ from the ideal value the minimum THD of $90\,\mathrm{dB}$ is achieved.

2.3.3 Total harmonic distortion versus temperature

As it was mentioned before, the setup in figure 2.1 allowed to alter temperature during the measurements. Thus, to see how the THD performance of the currently

implemented channel merging technique varies with temperature, following measurements were performed across the whole guaranteed temperature range of the AD7606C which goes from −40 °C to 125 °C.

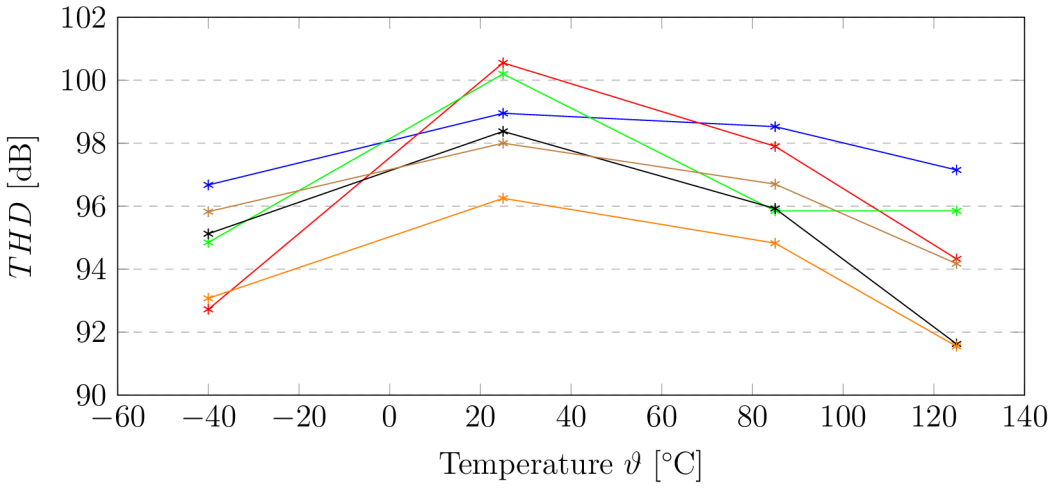

Fig. 2.12: The measured THD of the ±10 V and the ±2.5 V merged channels of 6 parts versus temperature ϑ

The plot in figure 2.12 shows the THD performance of 6 parts versus temperature ϑ. It can be seen that the THD holds very well across the whole temperature range as it is stable and higher than 90 dB.

2.3.4 Total harmonic distortion versus external resistor

Another significant source of error and thus potential cause for decreased THD performance is the external resistor R_{EXT} and the non-linear current I_{NL} going out of the lower range channel as it is shown in figure 2.13.

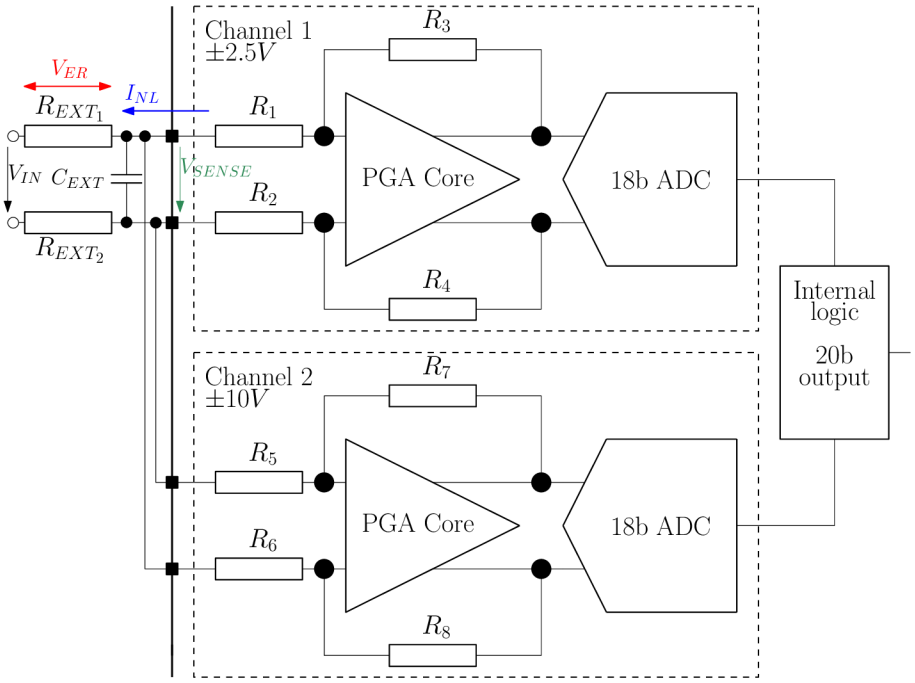

Fig. 2.13: Block diagram of the currently implemented channel merging technique in the AD7606C with the external filter

The R_{EXT} in figure 2.13 is part of the external filter that customers usually use as an antialiasing filter together with parts from the AD7606X family.

The reason why there is the I_{NL} going out of lower range channel is in details described in chapter 4, which also covers mitigation of this undesirable current.

These two facts are one of the root causes that are behind decreasing of the THD performance. The I_{NL} generates the non-linear error voltage V_{ER} that is given by equation 2.6.

$$V_{ER} = R_{EXT} I_{NL} \tag{2.6}$$

As it can be seen in figure 2.13 the actual voltage V_{SENSE} that is being sensed by the PGA is given by equation 2.7.

$$V_{SENSE} = V_{IN} + V_{ER} \tag{2.7}$$

Equation 2.7 means that input voltage V_{IN} is distorted by the V_{ER}, which is not linear, and thus the THD performance of the whole signal chain is decreased.

It can be noticed from equation 2.6 that the higher the value of the R_{EXT} is the higher the V_{ER} is. As the setup depicted in figure 2.1 allowed to connect the external filter to the whole signal chain, the THD versus the value of the R_{EXT} was measured and the data gathered is shown in figure 2.14.

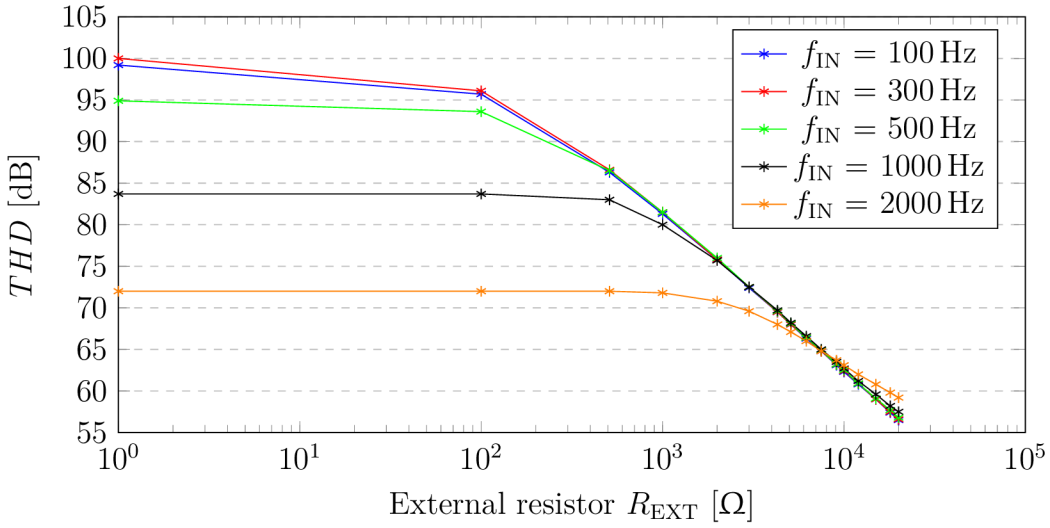

Fig. 2.14: The THD performance of the $\pm 10\,\mathrm{V}$ and the $\pm 2.5\,\mathrm{V}$ merged channels versus the R_{EXT}

It can be seen in figure 2.14 that the THD performance decreases with increasing value of the R_{EXT} as expected.

Interesting phenomenon also occurred during this measurement. It can be noticed that the THD performance not only decreases with the increasing value of the R_{EXT}, but also decreases with the increasing value of the input signal frequency f_{IN}. To have a closer look at this phenomenon, the THD versus the f_{IN} was also measured and the data gathered can be seen in figure 2.15.

Nevertheless, the conclusion that might be drawn from this measurement is that the currently implemented channel merging technique is able to achieve THD higher than 90 dB with the R_{EXT} lower than $500\,\Omega$ and with the f_{IN} lower than 500 Hz.

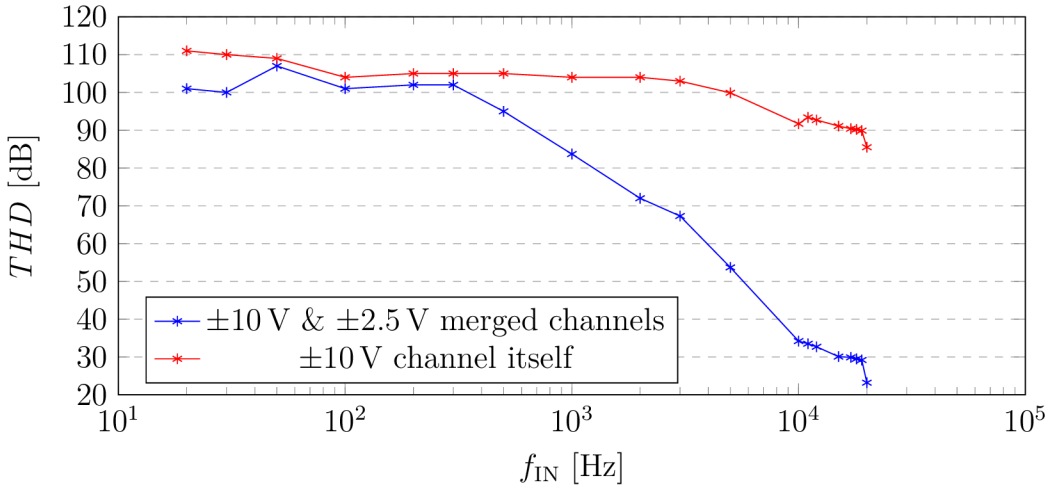

Fig. 2.15: The THD performance of the ±10 V and ±2.5 V merged channels versus the f_{IN}

The figure 2.15 shows the THD performance versus f_{IN} in case where the ±10 V channel is merged with the ±2.5 V channel and in case where the ±10 V channel works alone. It is clear that the THD performance of the ±10 V channel itself is relatively stable over the whole measured frequency range as it decreases from 110 dB to 85 dB. On the other hand, the THD performance of the ±10 V channel merged with the ±2.5 V channel decreases rapidly with the increasing value of the f_{IN}. It is believed that this issue occurs due to mismatch between cutoff frequency f_{3dB} of both channels. Nevertheless, as it was mentioned before, the AD7606C has no option to trim the f_{3dB} and thus, further analysis of this phenomenon was not possible at this stage.

2.4 Performance summary of the current solution

The currently implemented channel merging technique uses two channels of the AD7606C. One channel is set to the ±10 V range and the other one is set to the ±2.5 V range. Based on the codes from the ADC of the ±10 V channel, the internal logic block makes decision whether to use codes from the ±10 V channel or from ±2.5 V channel in order to build the final output signal as it is shown in figure 1.1. By this technique, the extra 12 dB of DR should be gained as it is given by equation 1.2.

Based on the measurements of the AD7606C first silicon few conclusions might be drawn.

- The extra DR of 12 dB is not possible to achieve as the signal chain with the PGA set to the ±10 V range has different SNR than the signal chain with the PGA set to the ±2.5 V range. This issue is described in figure 2.5 where it can be seen that in the worst case this technique is achieving 5 dB of extra DR.
- This technique is very sensitive to several errors that might decrease its THD performance. These errors are: offset mismatch, gain error and phase delay mismatch. In order to keep the THD performance higher than 90 dB these errors have to be within a limits that are summarized in table 2.1.
- This technique is also sensitive to the value of the R_{EXT} that customers use as a part of the antialiasing filter. In order to keep the THD performance higher than 90 dB the value of the R_{EXT} should not exceed 500 Ω.
- Also, sensitivity to the frequency of the input signal f_{IN} has been discovered, but as the AD7606C has no option to trim the f_{3dB}, further investigation was not possible. Nevertheless, it is clear that in order to keep the THD performance higher than 90 dB the value of the f_{IN} must not be higher than 500 Hz.

Tab. 2.1: Performance summary of the currently implemented channel merging technique

Specification				Conditions			
Parameter	Symbol	Value	Unit	Parameter	Symbol	Value	Unit
Dynamic range	DR	115	dB	Oversampling ratio	OSR	256	-
				Internal sampling frequency	f_{SI}	800	kHz
Total harmonic distortion	THD	>90	dB	External resistor	R_{EXT}	<500	Ω
				Input frequency	f_{IN}	<500	Hz
				Temperature	ϑ	−40 to 125	°C
				Gain error	-	<±0.08	%
				Offset mismatch	-	<±48	LSB

Based on the silicon results summarized in table 2.1 two main goals for the rest of this thesis were set:

- investigate options to further increase DR when merging two channels together,
- investigate options to make the channel merging technique immune to the value of the R_{EXT} or, in other words, investigate options to mitigate the I_{NL}

going out of the lower range channel when the input signal is outside of the range.

3 Improving the dynamic range performance of the current solution

The currently implemented channel merging technique in the Analog Devices part AD7606C is able to achieve performance that is summarized in table 2.1. It can be seen that the highest DR that can be achieved is 115 dB with the OSR equal to 256.

This chapter of this master's thesis proposes, designs, simulates and evaluates three options to increase the currently achieved DR of 115 dB.

3.1 Decreasing the cutoff frequency of the PGA

As it was mentioned in the conclusion of section 2.2, one way to increase the DR of the currently implemented channel merging technique is to reduce the $f_{3\text{dB}}$ of the PGA. As it can be seen in equation 2.3, decreasing the $f_{3\text{dB}}$ of the PGA will also decrease the RMS noise of the input resistor R_{IN} and the RMS noise of the feedback resistor R_{FB}. Decreasing these two values also means decreasing RMS noise n_{PGA} of the whole PGA which should increase the overall SNR as it can be seen in equation 2.2.

Increasing the SNR of the ±2.5 V channel should result in increasing the final DR of the currently implemented channel merging technique as it is shown in equation 2.1.

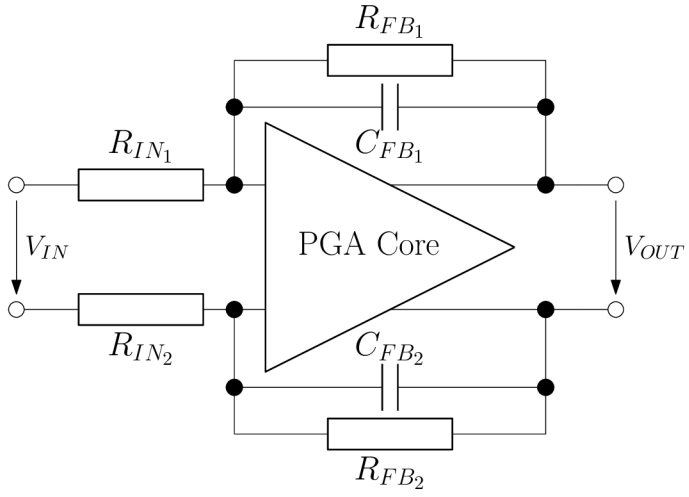

Fig. 3.1: The PGA of the AD7606C

The $f_{3\text{dB}}$ of the PGA is given by the feedback resistor $R_{FB_{1/2}}$ and the feedback capacitor $C_{FB_{1/2}}$ as it is shown in equation 2.5. In order to decrease the $f_{3\text{dB}}$ either

the $C_{FB_{1/2}}$ or the $R_{FB_{1/2}}$ must to be increased. But, with equation 2.4 in mind, it is clear that in order to keep the gain G of the PGA the same, the value of the $R_{FB_{1/2}}$ must be intact. This means, that the only way to reduce the $f_{3\text{dB}}$ of the PGA is to increase value of the $C_{FB_{1/2}}$.

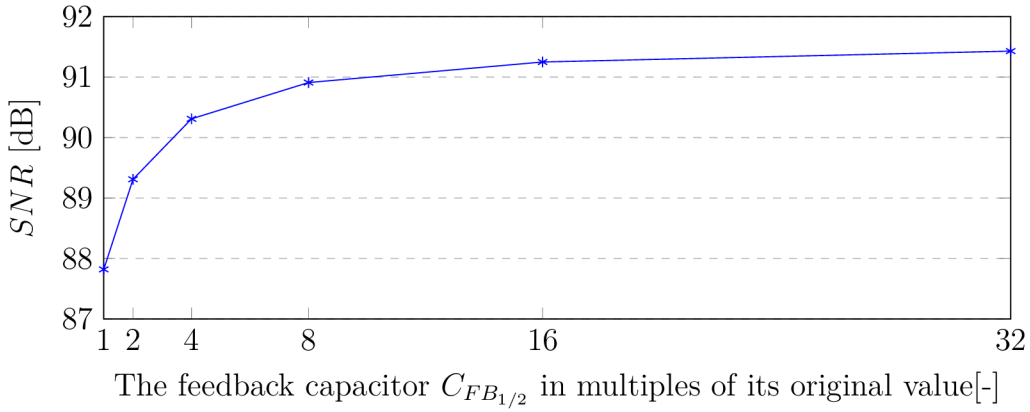

Fig. 3.2: The SNR performance of the $\pm 2.5\,\text{V}$ channel versus the $C_{FB_{1/2}}$

The figure 3.2 shows estimated SNR of the $\pm 2.5\,\text{V}$ channel versus the value of the $C_{FB_{1/2}}$ for the OSR equal to 1. The estimated SNR was derived using equations 2.2 and 2.3.

It can be seen that the highest gain in the SNR performance is obtained when increasing the value of the $C_{FB_{1/2}}$ from $1 \times C_{FB_{1/2}}$ to $2 \times C_{FB_{1/2}}$. Because of that, further analysis will be done with the $C_{FB_{1/2}}$ equal to double of its original value. This change decreases the $f_{3\text{dB}}$ of the PGA from its original value of 32.1 kHz to 16.05 kHz.

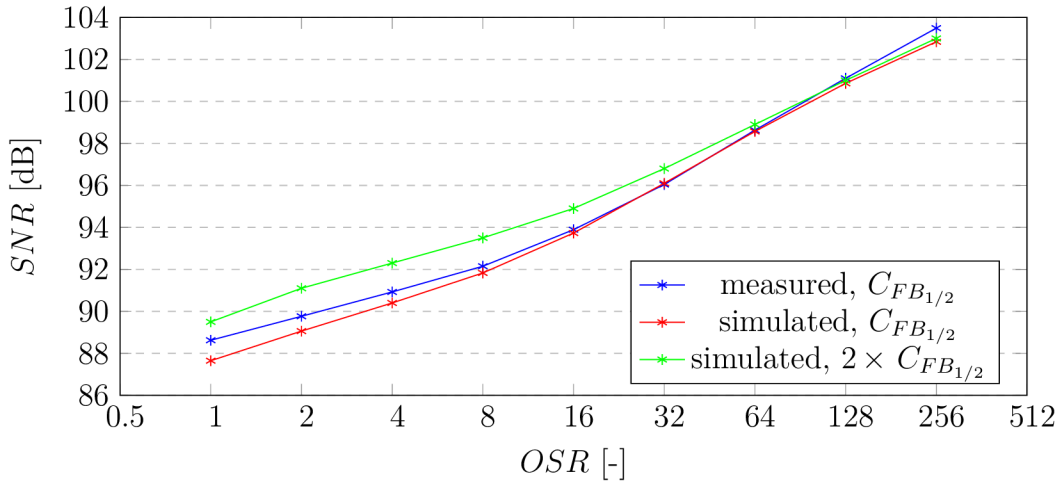

Fig. 3.3: The SNR of the $\pm 2.5\,\text{V}$ channel versus the OSR and the $C_{FB_{1/2}}$

The figure 3.3 shows the SNR versus the OSR of the $\pm 2.5\,\mathrm{V}$ channel. Two curves were obtained in simulations and one curve was obtained from measurements on silicon and serves as a reference to make sure that the simulation results are correct and reflects the reality.

It can be seen that by increasing the value of the $C_{FB_{1/2}}$ by factor of 2 and thus, reducing the $f_{3\mathrm{dB}}$ of the PGA to half, the SNR of the $\pm 2.5\,\mathrm{V}$ channel might be increased up to the OSR equal to 64. After that, the SNR values are the same no matter the value of the $C_{FB_{1/2}}$.

Also, it is worth to notice that the simulated values of the SNR match the measured values very well as the biggest difference is 1 dB in the case where the OSR equals to 1. This gives the simulated values reasonable credibility.

As it was mentioned before, by increasing the SNR of the $\pm 2.5\,\mathrm{V}$ channel, the overall DR, when merging the $\pm 10\,\mathrm{V}$ channel with the $\pm 2.5\,\mathrm{V}$ channel, should also increase as it is shown in equation 2.1. To find out the final DR of the $\pm 10\,\mathrm{V}$ and $\pm 2.5\,\mathrm{V}$ channels merged together with reduced value of the $f_{3\mathrm{dB}}$, the simulation was performed and following data was gathered.

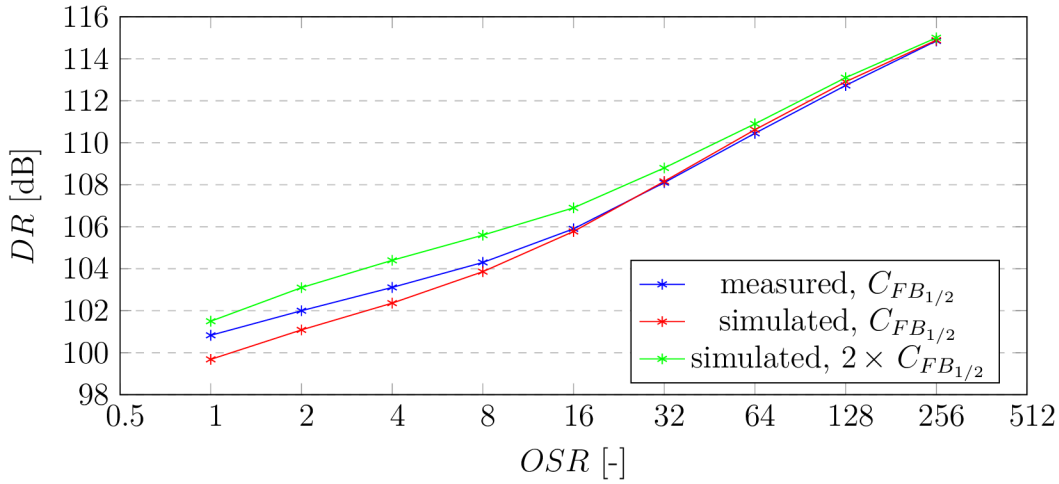

Fig. 3.4: The DR performance of the $\pm 2.5\,\mathrm{V}$ and the $\pm 10\,\mathrm{V}$ merged channels versus the OSR and the $C_{FB_{1/2}}$

As in the case of the SNR values, even here very good matching with the measured values can be observed. It is now easy to see that with reducing of the $f_{3\mathrm{dB}}$ to half, higher values of the overall DR cannot be achieved as the maximum value of 115 dB is the same no matter the value of the $C_{FB_{1/2}}$. On the other hand, it can be seen that reducing the $f_{3\mathrm{dB}}$ of the PGA increases the overall DR for lower values of the OSR.

Thus, increasing the value of the $C_{FB_{1/2}}$ might be helpful in situations where the customer does not want to use the AD7606C part with high OSR. On the other

hand, it is necessary to bear in mind that increasing the value of the $C_{FB_{1/2}}$ also reduces the $f_{3\text{dB}}$ of the PGA and thus ability of the AD7606C to process signals with higher frequencies.

3.2 Decreasing range of the lower range channel

Another way to increase the overall DR of the currently implemented channel merging technique is, according to equations 1.2 and 2.1, decreasing the range of the lower range channel from ±2.5 V to lower value. As the customers using parts from the AD7606X family are interested in the ±1.25 V range, the rest of this section will analyse this particular range.

First of all, it is necessary to realize what does lowering the range of the PGA mean as it has several impacts on the whole channel merging technique. According to equation 1.2, the extra dynamic range (DR_{EXT}) that can be gained in theory by merging ±2.5 V and ±10 V channels is 12 dB. It is clear that if the range decreases from ±2.5 V to ±1.25 V, the new DR_{EXT} that can be gained is given by equation 3.1:

$$DR_{EXT} = 20 \times log\left(\frac{10}{1.25}\right) = 18\,\text{dB}. \tag{3.1}$$

Another thing that is necessary to realize is that with lowering the range from ±2.5 V to ±1.25 V the size of the LSB is also decreasing as is shown in equation 3.2.

$$LSB_{2.5} = \frac{2.5}{2^{18-1}} = 19.1\,\mu\text{V} \rightarrow LSB_{1.25} = \frac{1.25}{2^{18-1}} = 9.53\,\mu\text{V} \tag{3.2}$$

This has direct impact on the internal logic block that can be seen in figure 1.1. As the size of the ±1.25 V range LSB is half the size of the ±2.5 V range LSB, the codes that the internal block outputs must be 21 bits long instead of 20 bits as it was in the case of the ±2.5 V range. Also, the threshold values, that decide whether to use codes from the ±10 V channel or from the ±1.25 V channel, must be adjusted to accommodate the ±1.25 V range. The last thing that must be changed regarding the internal logic block is the number of bits that codes from the ±10 V channel get shift by. As the size of the lower range channel LSB is halved, the codes from the ±10 V channel must be logically shifted by 3 bits to the left and not by 2 as it was in the case of the ±2.5 V range. The full behavioural model of the internal logic block that was used to merge ±1.25 V and ±10 V channels can be found in listing B.2.

Another important thing to realize is that lowering the range of the PGA from ±2.5 V to ±1.25 V also means increasing the gain G of the PGA. As it was shown before, the gain G is given by the equation 2.4 and depends on the values of the

R_{IN} and the R_{FB}. Thus, in order to double the gain G of the PGA the R_{IN} must be halved or the R_{FB} must be increased 2 times. To decide what option to choose, following table that compares both scenarios was created.

Tab. 3.1: Comparison of two options to increase gain G of the PGA

Parameter	$2 \times R_{FB}$	$R_{IN}/2$
Area	increases	decreases
Input resistance	R_{IN}	$R_{IN}/2$
PGA noise n_{PGA}	191 µV	146 µV
Cutoff frequency $f_{3\mathrm{dB}}$	decreases	stays the same

Apart from others, the most important thing to notice is that the PGA with halved R_{IN} has lower PGA noise n_{PGA} than the option with the doubled R_{FB}. This also means that the SNR will be higher in the case of the halved R_{IN} than in the case of the doubled R_{FB}, which should also mean better overall DR when merging ±10 V and ±1.25 V channels together. Because of that, further analysis will be done with the halved R_{IN}.

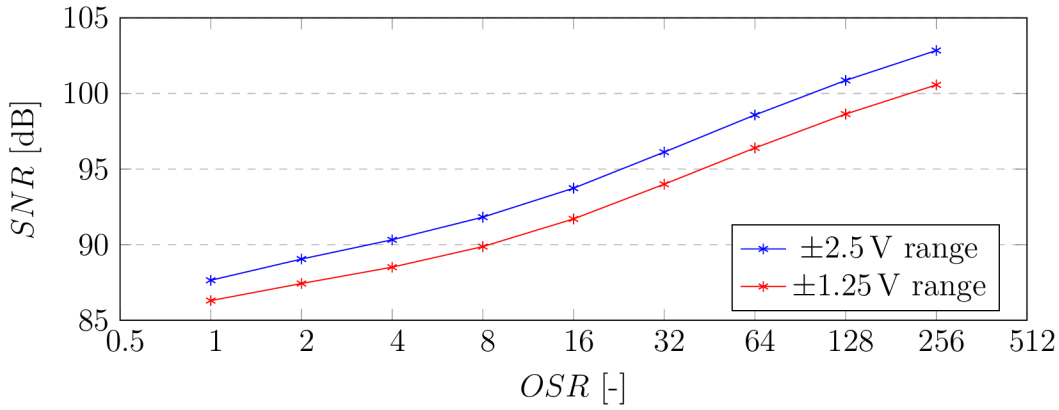

Fig. 3.5: The simulated SNR performance of the ±2.5 V and the ±1.25 V channels versus the OSR

The figure 3.5 shows the simulated SNR performance of ±2.5 V and ±1.25 V ranges versus the OSR. It can be seen that the SNR performance of the ±1.25 V range is about 1.5 dB lower than the SNR performance of the ±2.5 V range. This phenomenon makes sense once it is realized that even though the value of the R_{IN} was reduced to half and thus the noise contribution of this resistor got reduced as well, the gain G was increased and thus the overall PGA noise n_{PGA} got increased too. In case of the PGA set to ±2.5 V range the n_{PGA} was equal to 124 µV, but in case of the PGA set to ±1.25 V range the n_{PGA} was equal to 146 µV.

One way to reduce this drop in the SNR performance of the channel with range set to $\pm 1.25\,\mathrm{V}$ has already been introduced in section 3.1. By increasing the value of the feedback capacitor in the PGA the SNR performance of the channel should be increased. This option is in more detail described in section 3.3.

Judging only by the SNR performance of $\pm 1.25\,\mathrm{V}$ range it may seem that by lowering the range from $\pm 2.5\,\mathrm{V}$ to $\pm 1.25\,\mathrm{V}$ it cannot be won much. Nevertheless, it is necessary to bear in mind equation 3.1, which shows that by lowering the range extra 18 dB of DR should be gained. In order to find out the final DR performance of channel merging technique that uses $\pm 1.25\,\mathrm{V}$ and $\pm 10\,\mathrm{V}$ channels, simulation was performed and following data was gathered.

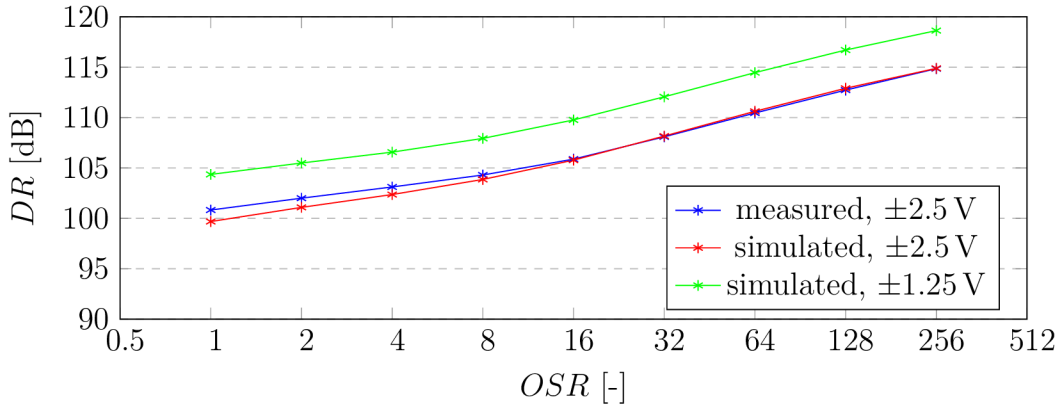

Fig. 3.6: The DR performance of $\pm 2.5\,\mathrm{V}/\pm 1.25\,\mathrm{V}$ and $\pm 10\,\mathrm{V}$ merged channels versus the OSR

It is very clear to see in figure 3.6 that even though the SNR performance of the $\pm 1.25\,\mathrm{V}$ channel was approximately 1.5 dB worse than the SNR performance of the $\pm 2.5\,\mathrm{V}$ channel, as it is shown in figure 3.5, the final DR performance of the channel merging technique that uses the $\pm 1.25\,\mathrm{V}$ channel with the $\pm 10\,\mathrm{V}$ channel has improved by approximately 4 dB over the whole OSR range.

The highest DR that this option is able to achieve is 118.6 dB with the OSR equal to 256.

It is also necessary to point out that this option is able to achieve 115 dB of DR with the OSR equal to 64. The currently implemented channel merging technique is able to achieve the same performance with OSR equal to 256. This is a huge improvement as it allows customers to run the part with much higher clock frequency in order to get the same performance. In the case where the OSR equals 256, the maximum allowed clock frequency is 3.125 kHz, but in the case where the OSR equals 64 it is 12.5 kHz.

3.3 Decreasing range of the lower range channel and decreasing the cutoff frequency of the PGA

The drop in the SNR performance of $\pm 1.25\,\mathrm{V}$ channel is caused by decreasing the value of the R_{IN} and thus by increasing the overall value of the PGA gain G as it is explained in section 3.2. In order to improve the SNR performance of $\pm 1.25\,\mathrm{V}$ channel the only thing that can be done is to reduce the $f_{3\mathrm{dB}}$ of the PGA as it is shown in equations 2.2 and 2.3.

As it was in the case of the $\pm 2.5\,\mathrm{V}$ channel, even here the $f_{3\mathrm{dB}}$ will be halved by increasing the $C_{FB_{1/2}}$ to double of its original value. Further increasing of the $C_{FB_{1/2}}$ also further increases the SNR performance as it was shown in figure 3.2, but increasing the value of the $C_{FB_{1/2}}$ by factor of 2 shows the highest step in improvement.

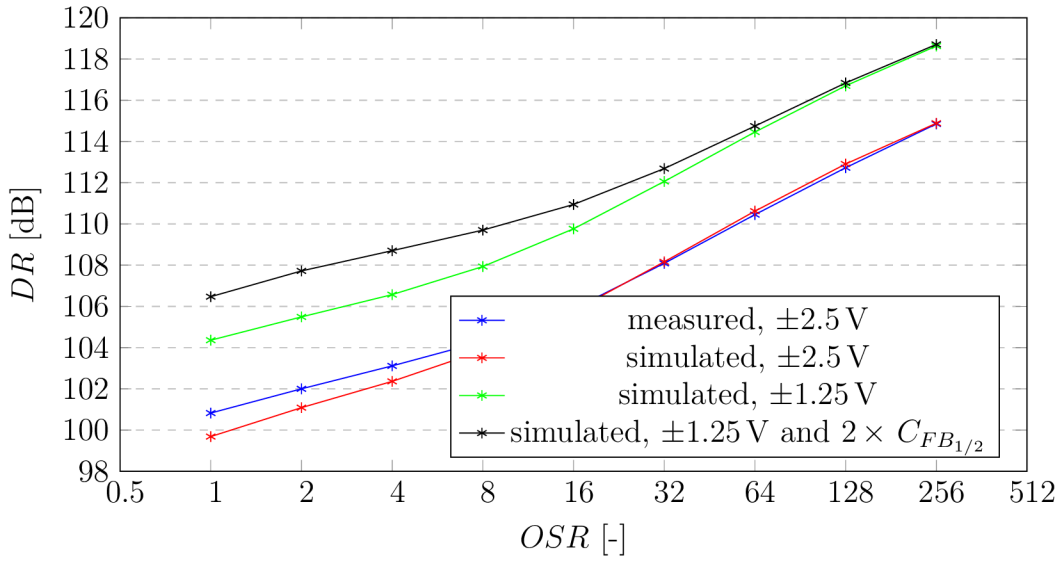

Fig. 3.7: The DR performance of $\pm 2.5\,\mathrm{V}/\pm 1.25\,\mathrm{V}$ with $2\times$ $C_{FB_{1/2}}$ and $\pm 10\,\mathrm{V}$ merged channels versus the OSR

It is necessary to point out two important things in figure 3.7. The first thing to notice is that with halved $f_{3\mathrm{dB}}$ another extra 2 dB of the DR might be gained in comparison with the option where the $f_{3\mathrm{dB}}$ has its original value. Thus, this might be a good option to reduce the drop in the SNR performance of the channel with the range set to $\pm 1.25\,\mathrm{V}$ in comparison with the channel with the range set to $\pm 2.5\,\mathrm{V}$ if the halved $f_{3\mathrm{dB}}$ is no issue for the customers. The other thing to notice is that the higher the OSR is the lower the difference in DR is until there is no difference between the option with halved $f_{3\mathrm{dB}}$ and the option with original $f_{3\mathrm{dB}}$. The same phenomenon was observed in figure 3.4 and it relates to the fact that once the OSR

is equal to values 64 and higher, the digital filter has already filtered out all noise contribution from the R_{IN} and the R_{FB} resistors and only the noise that is left is 1/f noise of the PGA core that is the same no matter the value of the $C_{FB_{1/2}}$.

3.4 Summary of proposed options

Three options to improve the currently implemented channel merging technique in terms of the DR performance were proposed, designed and simulated in this chapter.

The first option was based only on decreasing the $f_{3\mathrm{dB}}$ of the PGA by increasing the value of the $C_{FB_{1/2}}$ by factor of 2. This change results in increasing the SNR performance of the ±2.5 V channel and thus in increasing the overall DR of merged ±2.5 V and ±10 V channels.

The second option was based on reducing the range of the lower range channel from ±2.5 V to ±1.25 V. This option requires changes in the internal logic block as well as changes in the PGA itself. Even though the SNR performance of the ±1.25 V channel is about 1.5 dB worse than in case of the ±2.5 V channel, the final DR of ±1.25 V and ±10 V merged channels has improved by approximately 4 dB.

The last option was a combination of two previous ones. To improve the SNR performance of the ±1.25 V channel, the $f_{3\mathrm{dB}}$ was reduced and another improvement of 2 dB in the overall DR was observed for the lower OSR values.

Tab. 3.2: Comparison between proposed options

Option	Lower range [V]	$f_{3\mathrm{dB}}$	C_{FB}	R_{IN}	LSB [µV]	Results	DR [dB] OSR=1	DR [dB] OSR=256
Silicon	±2.5	$f_{3\mathrm{dB}}$	C_{FB}	R_{IN}	19.1	Measured	100.8	114.8
						Simulated	99.7	114.8
1	±2.5	$f_{3\mathrm{dB}}/2$	$2C_{FB}$	R_{IN}	19.1	Simulated	101.6	115.0
2	±1.25	$f_{3\mathrm{dB}}$	C_{FB}	$R_{IN}/2$	9.54	Simulated	104.4	118.6
3	±1.25	$f_{3\mathrm{dB}}/2$	$2C_{FB}$	$R_{IN}/2$	9.54	Simulated	106.5	118.6

From table 3.2 and from following figure 3.8 it can be seen that the best option to increase the overall DR of the currently implemented channel merging technique is option 3. This option uses the ±1.25 V channel and cuts the $f_{3\mathrm{dB}}$ to the half of its original value and can achieve 118.6 dB of the DR with the OSR equal to 256.

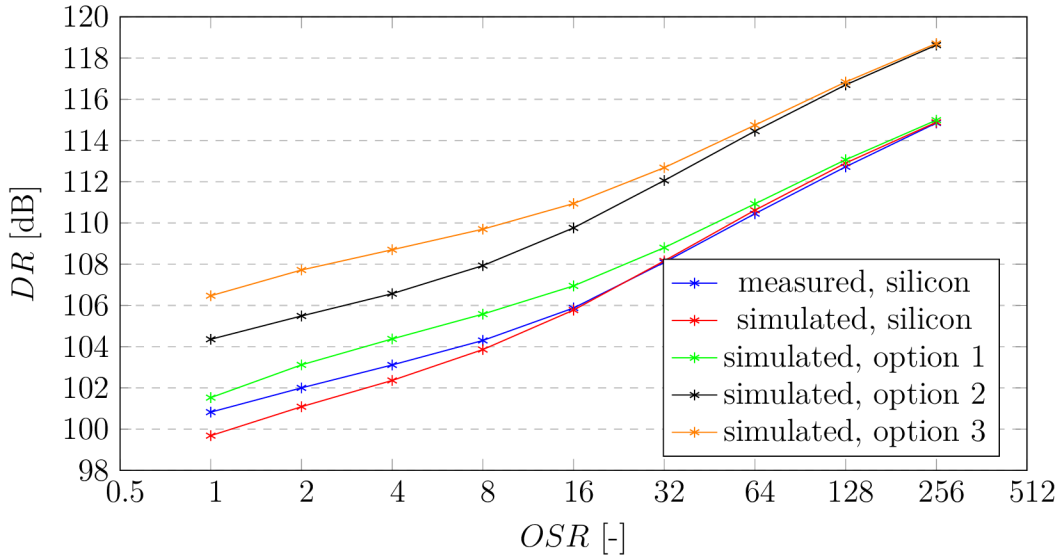

Fig. 3.8: The DR of all proposed options versus the OSR

The range of the lower range channel might be reduced even more as well as the cutoff frequency of the PGA to obtain even better DR performance than with proposed options. Nevertheless, it is necessary to bear in mind that further decreasing the cutoff frequency has its limitation as it was shown in figure 3.2 and also it decreases the ability of the signal chain to work with signals of higher frequencies. Further lowering the range of the lower range channel might also have some negative consequences as the R_{IN} of the PGA must be reduced as well.

4 Mitigation of the non-linear current of the lower range channel

As it was mentioned in subsection 2.3.4, one of the main cause of the THD performance degradation is the non-linear current I_{NL} going out of the lower range channel when the input voltage V_{IN} is out of its range. This I_{NL} then generates the non-linear error voltage V_{ER} across the R_{EXT}, as can be seen in figure 2.13. This V_{ER} then adds up to the actual V_{IN} and creates distortion as it is described by equations 2.6 and 2.7. This distortion then increases with increasing value of the R_{EXT} as it can be seen in figure 2.14 where is data which has been measured on silicon of the AD7606C with the currently implemented channel merging technique.

This phenomenon is highly undesirable as the customers want to use the R_{EXT} as part of the antialiasing filter. Thus, in this chapter of this thesis, three options to mitigate the I_{NL} are proposed, designed and simulated.

Nevertheless, to fully understand the cause of the I_{NL} it is necessary to have a closer look on what is happening when the V_{IN} is outside of the range of the lower range channel.

4.1 The non-linear current of the lower range channel

In order to find out root cause of the I_{NL} going out of the lower range channel, the transient simulation was performed and the data shown in figure 4.1 was gathered.

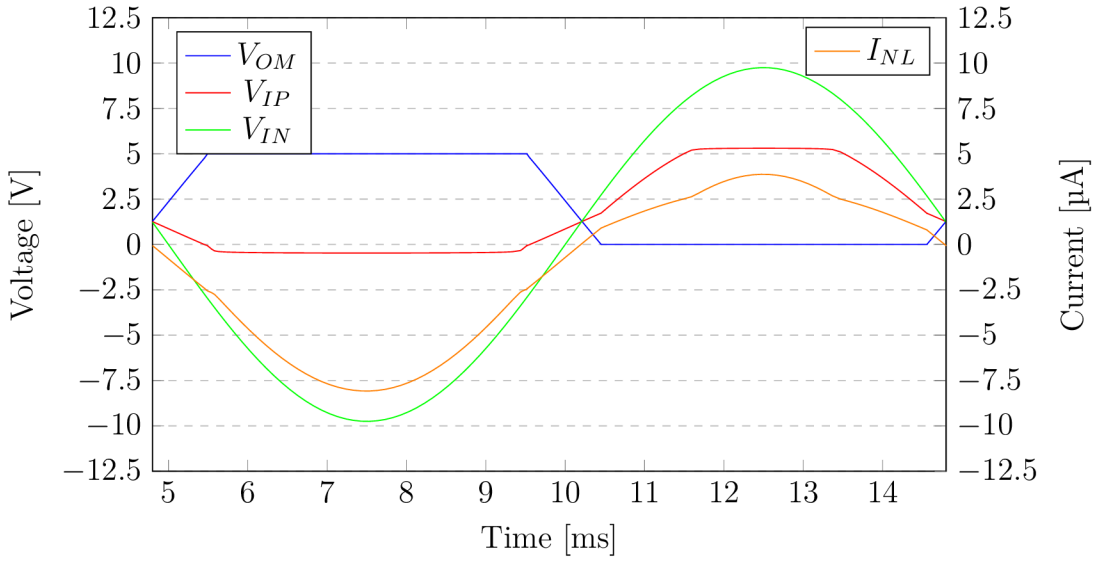

Fig. 4.1: The transient analysis of the lower range channel

In figure 4.1 one period of input signal V_{IN} can be seen together with the voltage at the input and output of the PGA core and the I_{NL} going out of the channel.

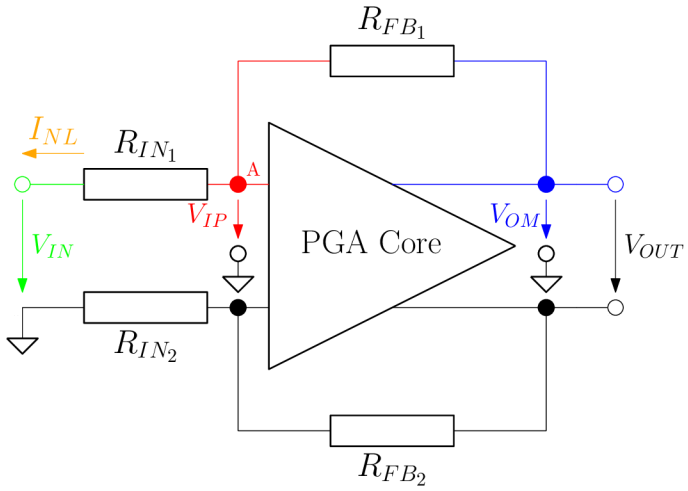

Fig. 4.2: The PGA of the AD7606C, the I_{NL} analysis

It can be seen that when the V_{IN} is within $\pm 2.5\,\mathrm{V}$ range the voltages V_{IP} and V_{OM} follow correctly. Once the V_{IN} goes out of the $\pm 2.5\,\mathrm{V}$ range, the PGA gets saturated as the output of the PGA is limited by its rails. In the same time the V_{IP} still follows the V_{IN} until it gets clamped and settles on value of one forward bias voltage bellow ground ($0\,\mathrm{V}$) or one forward bias voltage above V_{DD} ($5\,\mathrm{V}$).

It is clear to see that the I_{NL} going out of the lower range channel is given by equation 4.1:

$$I_{NL} = \frac{V_{IN} - V_{IP}}{R_{IN_1}} \tag{4.1}$$

and as the V_{IP} gets clamped and thus it is not linear, the I_{NL} is not linear as well.

The reason why the V_{IP} gets clamped is that there are many switches connected to the node A that are not being shown in the simplified figure 4.2. To understand why these switches clamp the V_{IP} it is necessary to have a look at figure 4.3.

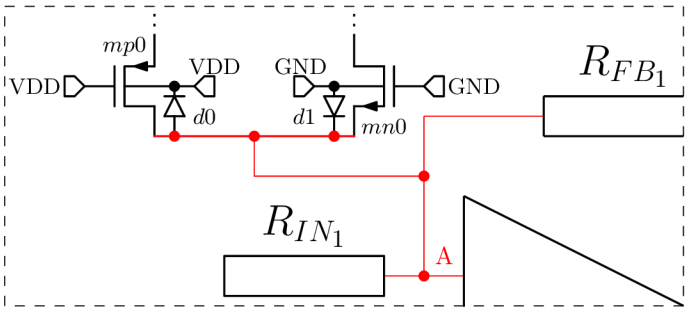

Fig. 4.3: Clamping of the V_{IP}, the I_{NL} analysis

Figure 4.3 depicts one switch of many that are connected to the node A. As it can be seen this switch consists of PMOS and NMOS transistor connected in parallel. When the switch is turned off, that means that the gate of the NMOS transistor is tied to ground and the gate of the PMOS transistor is tied to the V_{DD}, the back gate of the NMOS transistor is tied to the ground and the back gate of the PMOS transistor is tied to the V_{DD}. In this case, when the voltage in node A goes above V_{DD} or bellow ground diodes $d0$ or $d1$ start to open and create clamp. Then, because of this phenomenon, the V_{IP} remains stable until it is back bellow the V_{DD} or above the ground.

As it was described, the facts, that the PGA goes into saturation when the V_{IN} goes outside of the $\pm 2.5\,\mathrm{V}$ range and that in the same time the V_{IP} gets clamped, create the I_{NL} going out of the lower range channel that generates the V_{ER} over the R_{EXT}. This phenomenon then reduces the overall THD performance of the whole channel merging technique which is highly undesirable. Thus, in the following three sections, three options to mitigate this phenomenon are proposed, designed, simulated and evaluated.

In order to design and simulate following three options, proper test bench had to be created and compared to measured results from the currently implemented solution on silicon. The comparison between results from the measurements on silicon and simulated results can be seen in figure 4.4. It can be noticed that the simulation is more optimistic with lower input frequencies but more pessimistic with higher input frequencies. Nevertheless, the test bench, that had been created, reflects the measurements very well and thus will be used for simulations of 3 following options.

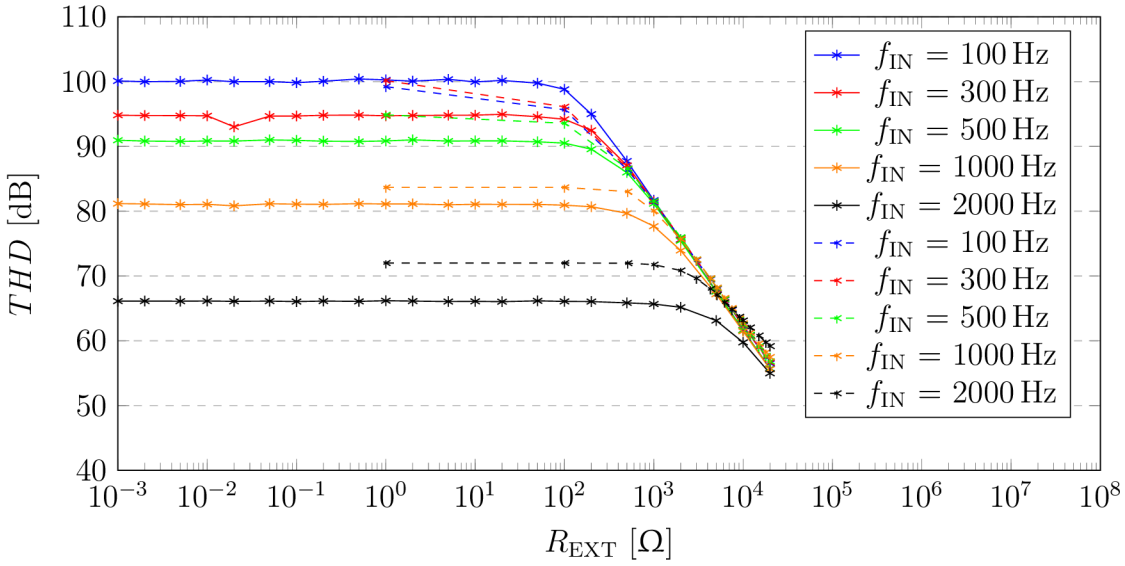

Fig. 4.4: The THD performance of the currently implemented channel merging versus the R_{EXT}, simulation (solid) vs measurement (dashed)

4.2 Changing gain of the lower range channel

The first option to mitigate the I_{NL} only requires changes in the internal logic block which can be seen in figure 1.1. This option is based on changing gain of the lower range channel with regards to the value of the V_{IN}. The internal logic block reads the codes from the $\pm 10\,\mathrm{V}$ range channel and once the codes are outside of the $\pm 2.5\,\mathrm{V}$ range, the internal logic block sets the gain of the $\pm 2.5\,\mathrm{V}$ channel to the value corresponding to the gain of the $\pm 5\,\mathrm{V}$ range or to the value corresponding to the gain of the $\pm 10\,\mathrm{V}$ range when the V_{IN} is outside of the $\pm 5\,\mathrm{V}$ range. Thanks to this technique the output voltage of the lower range channel PGA can not get saturated and the V_{IN} can not get clamped. Thus, the non-linearity of the I_{NL} is mitigated.

Changes that were required to implement this algorithm in the internal logic block can be seen in listing B.3.

To see the mitigation of the I_{NL} non-linearity, the transient simulation was performed and data gathered is shown in figure 4.5.

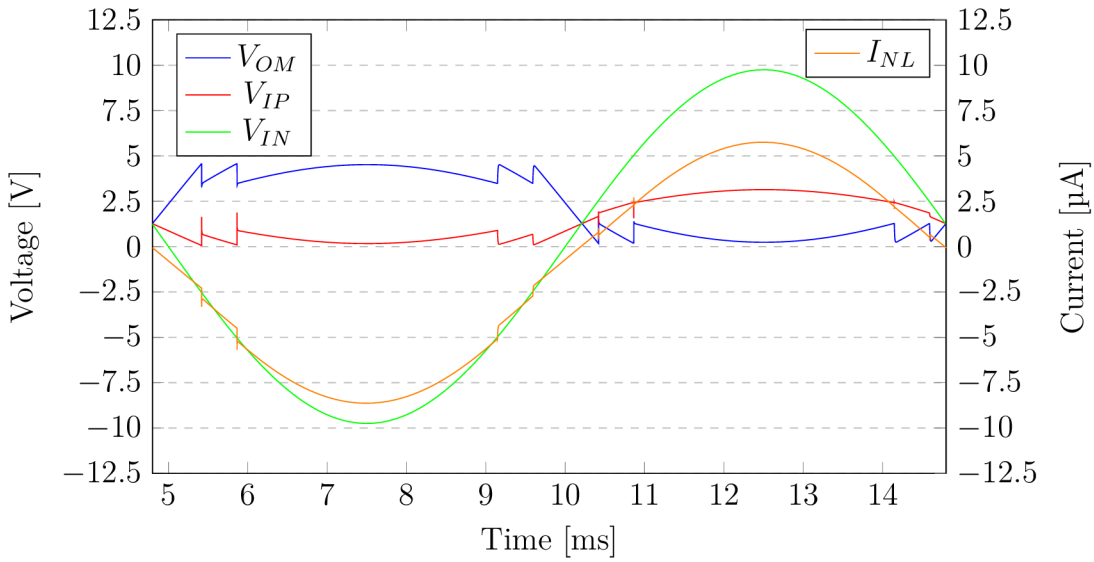

Fig. 4.5: The transient analysis of the lower range channel while changing its gain

It can be seen in figure 4.5, that the V_{OM} at the output of the PGA does not get saturated as the gain of the PGA is changing. Thanks to this, the V_{IP} does not get clamped in the same way as it does in the currently implemented solution, which makes the I_{NL} more linear.

To see if this technique works, another transient simulation was performed with different values of the R_{EXT} and the THD performance was measured. The data gathered is shown in figure 4.6.

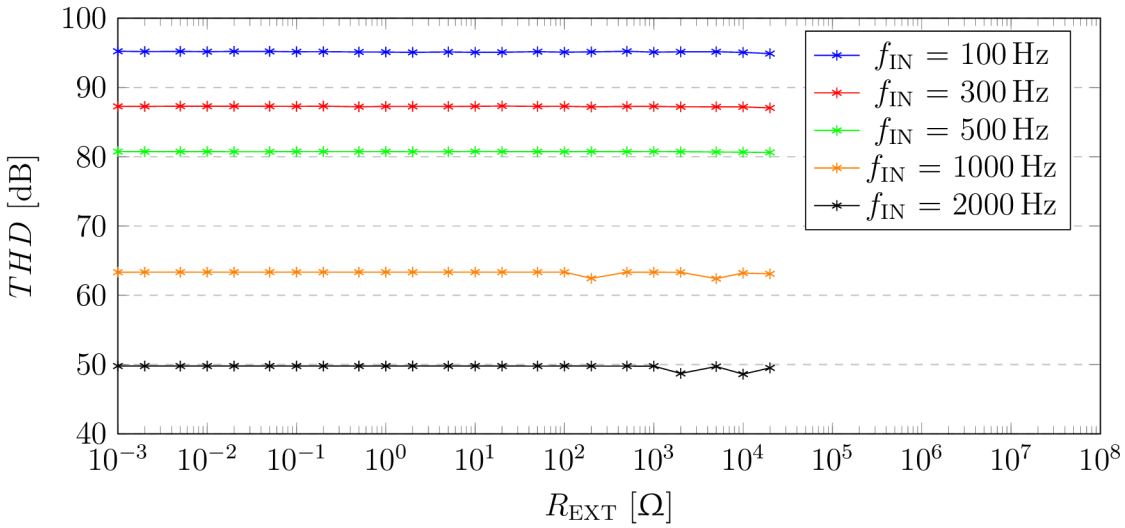

Fig. 4.6: The THD performance versus the R_{EXT} with gain switching technique

It can be seen that in figure 4.6 that the THD performance is no longer decreas-

ing with increasing value of the R_{EXT}.

The main advantage of this option is that it only requires changes in the internal digital block, thus, it is easy to implement. Nevertheless, it is necessary to realize that this option can not be used for the channel merging technique that uses $\pm 1.25\,\mathrm{V}$ and $\pm 10\,\mathrm{V}$ channels, because the $\pm 1.25\,\mathrm{V}$ range was created by halving the R_{IN} and not by adding more resistance to the R_{FB}. Thus, there is no option how to simply switch range from $\pm 1.25\,\mathrm{V}$ to $\pm 2.5\,\mathrm{V}$ or higher.

4.3 Disconnecting the lower range channel from the signal chain

Another option to mitigate the I_{NL} going out of the lower range channel is to disconnect the lower range channel from the signal chain once the V_{IN} is outside of the range. For this option it is necessary to implement two more switches to the PGA architecture, as it is shown in figure 4.7, and also add one more signal to the internal logic block, whose code can be found in listing B.4.

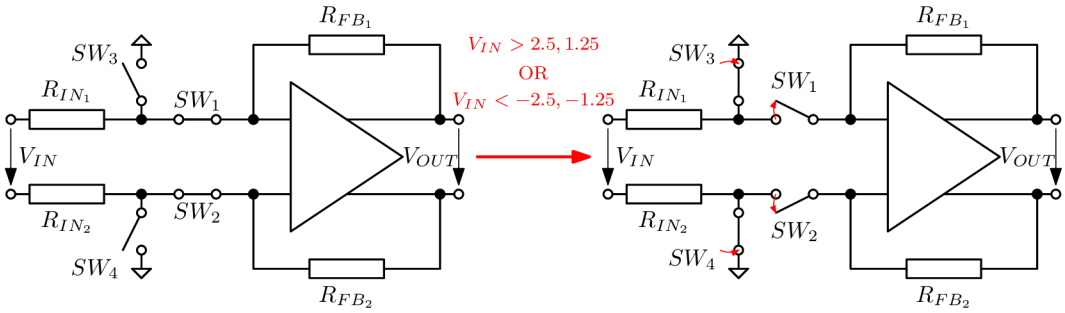

Fig. 4.7: Disconnecting the lower range channel from the signal chain

The switches SW_1 and SW_2 are already implemented in the architecture of the AD7606C PGA, but switches SW_3 and SW_4 must be added. These switches only have to connect input resistors R_{IN_1} and R_{IN_2} to the ground so simple NMOS transistor working as a switch is enough to do the work. After adding the switches the transient simulation was performed to check the behaviour of the proposed algorithm. The data gathered is shown in figure 4.8.

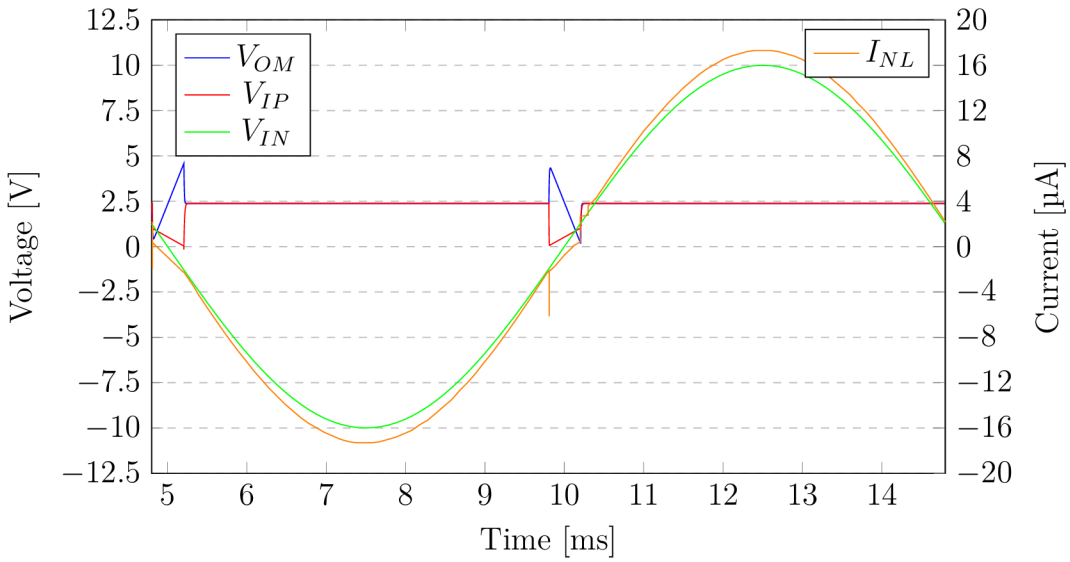

Fig. 4.8: The transient analysis of the lower range channel while disconnecting from the signal chain

It can be seen in figure 4.8 that when the V_{IN} is inside of the $\pm 1.25\,\mathrm{V}$ range, the voltage V_{OM} and V_{IP} follows input voltage V_{IN} accordingly. But once the V_{IN} is outside of the $\pm 1.25\,\mathrm{V}$ range, the $\pm 1.25\,\mathrm{V}$ channel gets disconnected and voltages V_{OM} and V_{IP} settle to value of the common mode voltage. Thanks to this, the non-linearity of the I_{NL} is noticeably mitigated.

The transient simulation was performed to see how proposed technique works with different values of the R_{EXT}. The data gathered is shown in figure 4.9.

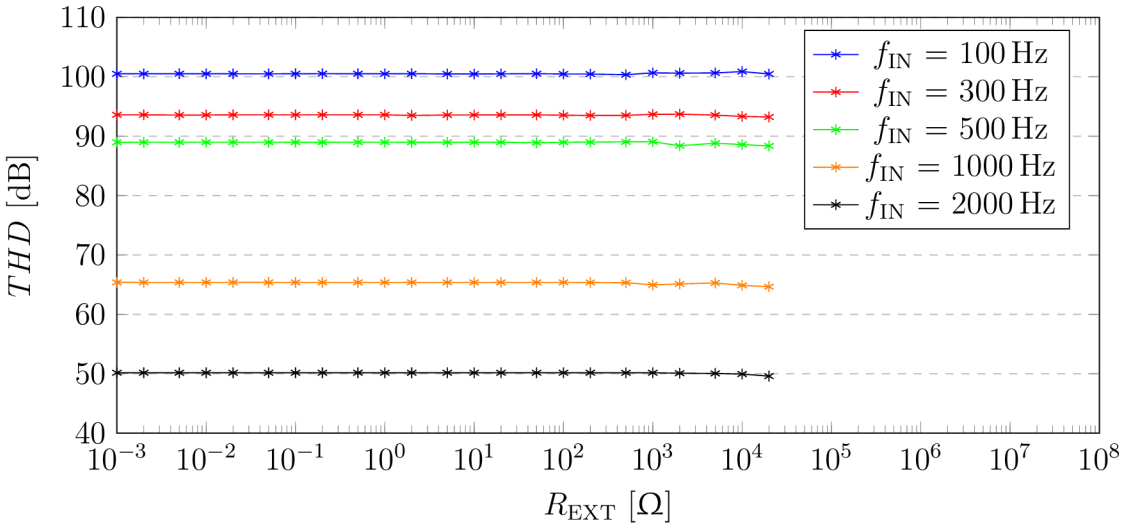

Fig. 4.9: The THD performance of the channel merging versus the R_{EXT} with disconnecting technique

It can be seen in figure 4.9 that this option also makes the channel merging technique immune to the presence of the R_{EXT} as the THD performance does not decrease with the increasing value of the R_{EXT}.

The main advantage of this option is that it can be used even when merging $\pm 1.25\,\mathrm{V}$ and $\pm 10\,\mathrm{V}$ channels. This was not possible with the previous option described in section 4.2 and thus, it makes this option more convenient.

4.4 Connecting the lower range channel to the sampled value of the virtual ground

Last option to mitigate effect of the I_{NL} is very similar to previous one with one main difference. When the V_{IN} is outside of the lower range channel range, the input of the PGA core does not get connected to the ground, but rather to the sampled value of the same node right before it gets disconnected. This means that the internal logic block has to read codes from the $\pm 10\,\mathrm{V}$ range channel and once the codes are close to the threshold value for the $\pm 1.25\,\mathrm{V}$ or $\pm 2.5\,\mathrm{V}$ range, the voltage value of the input of the PGA has to be sampled. Then, once the threshold value of the $\pm 1.25\,\mathrm{V}$ or $\pm 2.5\,\mathrm{V}$ range has been crossed, the input of the PGA is connected to the sampled voltage value.

It is clear that such a technique requires changes in the internal logic block as well as designing of sample and hold circuit that will be able to sample and then drive the input of the PGA core.

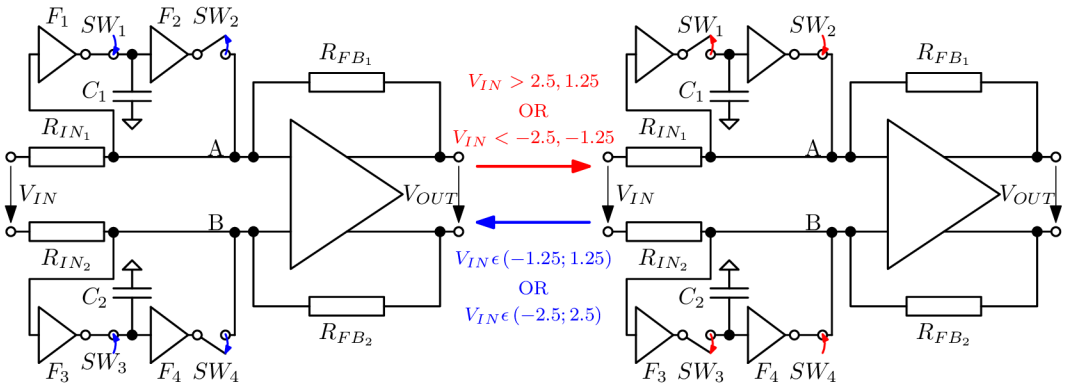

Fig. 4.10: Usage of the sample and hold circuit for mitigation of the I_{NL}

The figure 4.10 depicts usage of sample and hold circuit that consists of 2 switches SW_1 and SW_2, 2 voltage followers F_1 and F_2 and capacitor C_1. It can be seen that when the V_{IN} is in the range of the lower range channel the switch SW_1 remains closed and thus, the voltage on the capacitor C_1 directly follows voltage on the

input of the PGA core. Once the V_{IN} is outside of the lower range channel range, the switch SW_1 opens and in the same time the switch SW_2 closes. Once the switch SW_2 has been closed, the voltage follower F_2 drives the input of the PGA core with fixed value.

This technique has one big advantage in comparison with the option described in section 4.3 and it is that the node A is connected to the voltage that is very similar to the voltage that will be on this node again once the input voltage is back within the range of the lower range channel. This means that all capacitance in this node does not have to be charged and thus makes the transition over the lower range threshold smoother.

4.4.1 Sample and hold circuit

In order to implement technique described in section 4.4, sample and hold circuit must be designed. Figure 4.11 shows proposed architecture.

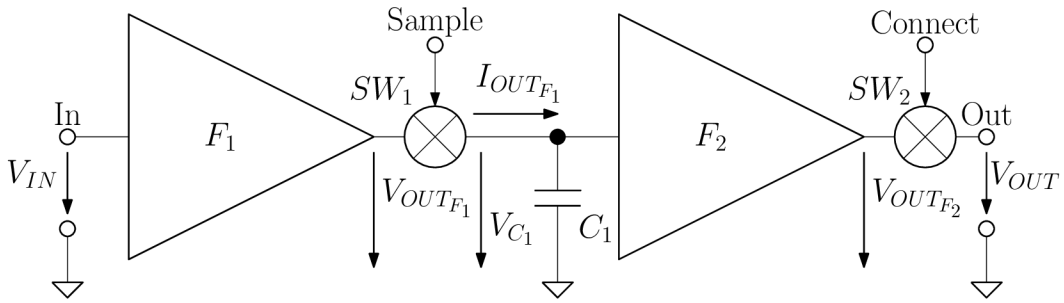

Fig. 4.11: Sample and hold circuit

As can be seen in figure 4.11, this circuit consists of two voltage followers F_1 and F_2, two switches SW_1 and SW_2 and one capacitor C_1. The idea behind this circuit is that the switch SW_1 remains open and thus the voltage V_{C_1} on the capacitor C_1 directly follows the V_{IN} while the switch SW_2 remains closed. Once it is desirable to sample the V_{IN}, the switch SW_1 closes and the switch SW_2 opens. Then the V_{OUT} is directly equal to the V_{C_1} on the capacitor C_1.

Following sections describe the design process that ends with fully designed sample and hold circuit proposed in figure 4.11.

Initial design of voltage follower

For the voltage followers F_1 and F_2 architecture depicted in figure 4.12 was chosen.

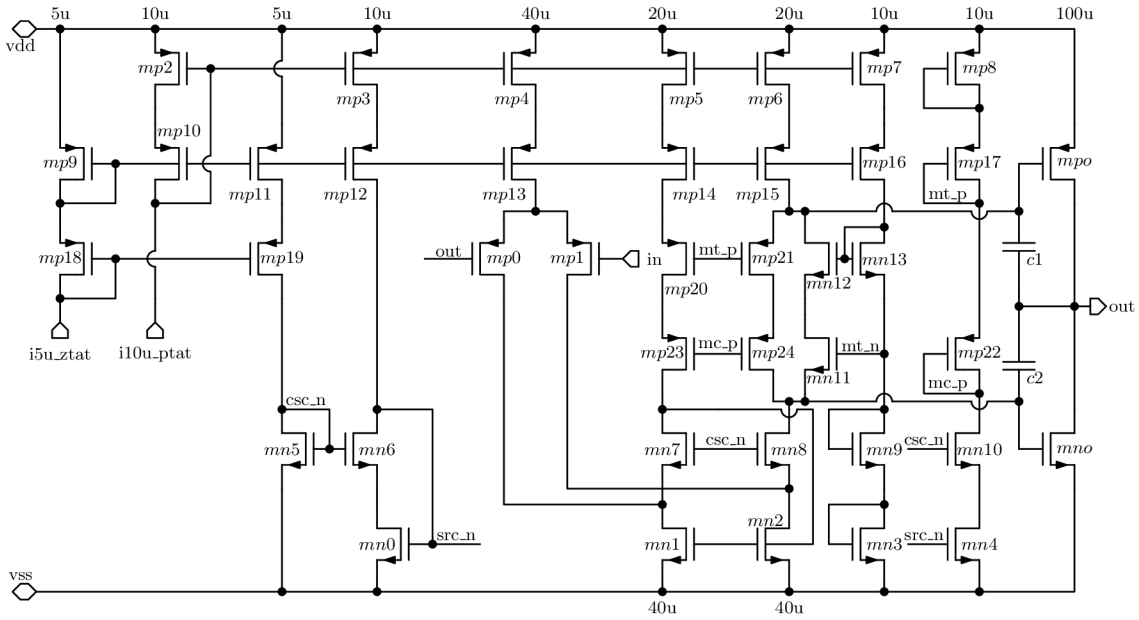

Fig. 4.12: Architecture of the voltage follower

First of all, the size of the output *mpo* PMOS transistor must be decided. This device has to be able to source 100 µA and has to have the biggest transconductance *gm* possible. These two conditions give us some clue for the W/L ratio, but in order to set this ratio, length has to be decided first. The lower the length is the higher the *gm* is, so based on this fact, the lowest length possible should be chosen. Nevertheless, devices with the lowest length possible can sometimes suffer from the leakage current I_{lkg} which is undesirable. Because of that, the I_{lkg} versus length of this device has been simulated and the data gathered is shown in figure 4.13.

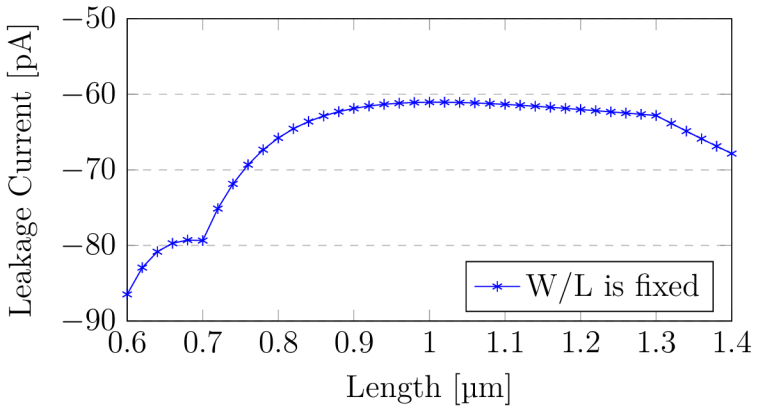

Fig. 4.13: The I_{lkg} of the 5 V PMOS transistor versus its length at 125 °C

It can be seen that the I_{lkg} of the 5 V PMOS transistor is in pA. Such a low value is not a problem for this case. Because of that, the initial length of this device

is 0.5 µm.

As it was said, the output *mpo* PMOS transistor has to have high *gm* in order to have the lowest noise possible. Because of that, the width of this transistor will be set so that its V_{GS} is going to be the same as its V_{TH} when the transistor is being biased with 100 µA.

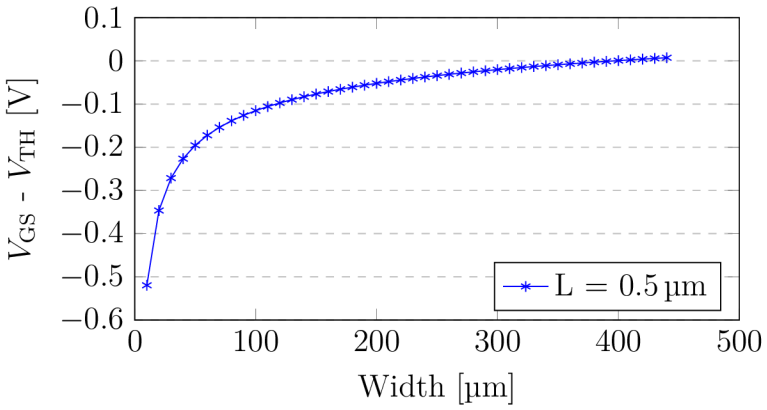

Fig. 4.14: V_{GS} - V_{TH} of the 5 V PMOS transistor vs. its width when being biased with 100 µA

It can be seen that with width of 400 µm the *mpo* transistor should work in weak inversion when being biased with 100 µA.

Dimensions of the *mpo* directly sets dimensions of the *mp8* as these two transistors must have the same current densities. Because of that the width of *mp8* is set to 40 µm.

The same design process can be applied to the output *mno* NMOS transistor. To decide the length of this transistor, the I_{lkg} versus its length has been simulated and the data gathered is shown in figure 4.15.

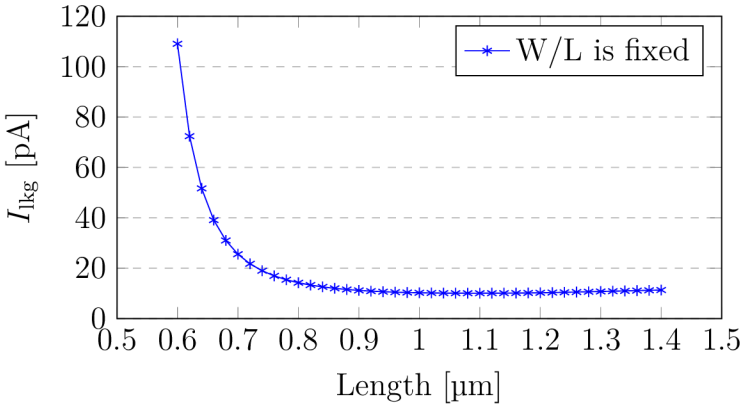

Fig. 4.15: The I_{lkg} of the 5 V NMOS transistor vs. its length at 125 °C

It can be seen again that the I_{lkg} is in units of pA which is not an issue for this particular case. Because of that the length of the output *mno* NMOS transistor is set to 0.6 µm.

As well as *mpo*, the *mno* should work in weak inversion in order to have high *gm*. To find the appropriate value of the width of this transistor, the simulation showing V_{GS} - V_{TH} versus the width has been performed and the results are shown in figure 4.16.

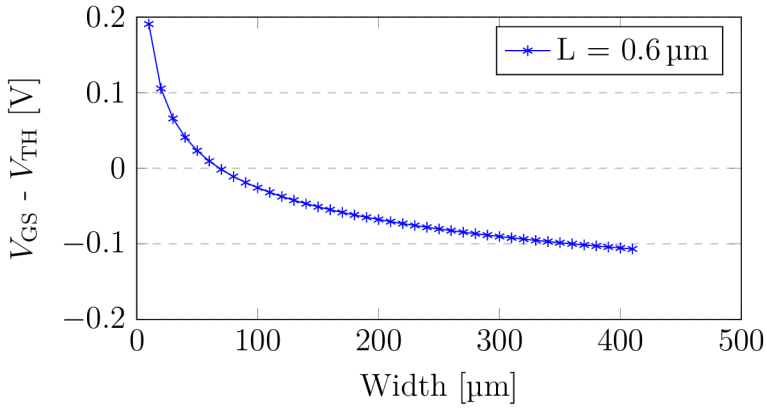

Fig. 4.16: The V_{GS} - V_{TH} of the 5 V NMOS transistor vs. its width when being biased with 100 µA

It can be seen that in order to work in weak inversion when being biased with 100 µA, the output *mno* NMOS transistor should have width of 80 µm.

As *mn3* must have the same current density as *mno*, the width of this transistor is set to 8 µm.

The input pair transistors (*mp0* and *mp1*) should also work in weak inversion in order to have high *gm* and thus low noise. As this condition is the same as the condition for the output *mpo* PMOS transistor the length of *mp0* and *mp1* is set to 0.5 µm. It is also known that current of 20 µA is flowing through each of these transistors. Thus, simulation showing V_{GS} - V_{TH} versus width of these transistors has been performed and the results are shown in figure 4.17.

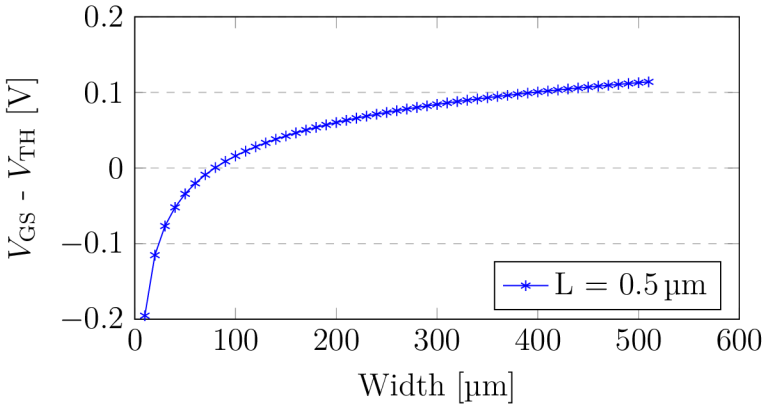

Fig. 4.17: The V_{GS} - V_{TH} of the 5 V PMOS transistor vs. its width when being biased with 20 µA

In order to push the input pair transistors *mp0* and *mp1* a bit more into the weak inversion and thus gain more *gm*, the width of 200 µm is chosen.

Next transistors to be designed are *mp2*, *mp3*, *mp4*, *mp5*, *mp6*, and *mp7*. These transistors create current mirror whose task is to distribute current of 10 µA proportional to absolute temperature (PTAT) to the rest of the circuit. The higher the output impedance r_o of the MOS transistor is the lower the current mismatch is. Thus, to find out optimal ratio of r_o and length of the PMOS transistor, the simulation was performed and the results are shown in figure 4.18.

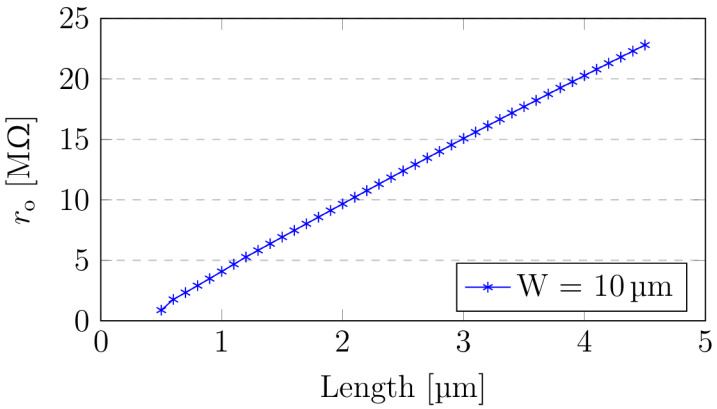

Fig. 4.18: The r_o of the PMOS transistor vs. its length when being biased with 10 µA

As it can be seen the r_o of the PMOS transistor with fixed width is proportionally increasing with its length. As this design is not area restricted the length of 2 µm is chosen. With this length relatively high r_o of 10 MΩ is achieved while the area of the PMOS current mirror is not unreasonable high.

It is desirable for the current mirror to work in the strong inversion. In order to work in the strong inversion, the V_{GS} - V_{TH} of the MOS transistor should be around 100 mV in this process. This fact gives us a clue to choose the initial width of transistors in the PMOS current mirror. To choose the most appropriate width, the simulation has been performed and the data gathered is shown in figure 4.19.

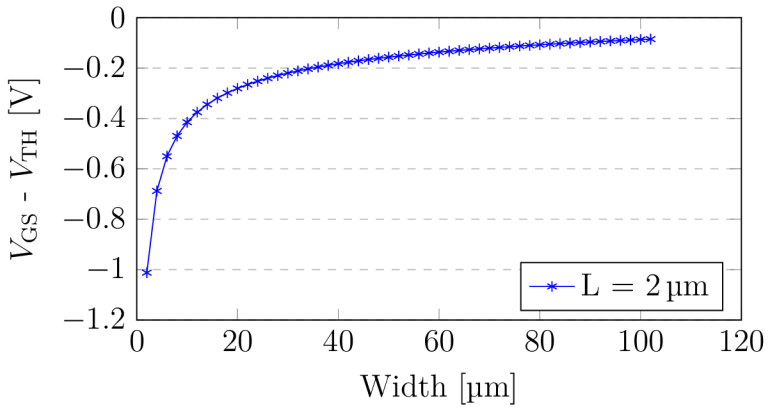

Fig. 4.19: The V_{GS} - V_{TH} of the PMOS transistor vs. its width when being biased with 10 µA

To keep the area of the PMOS current mirror reasonable, the width of 30 µm is chosen for transistors with 10 µA. For transistors in the PMOS current mirror with higher currents than 10 µA, the width of 30 µm is appropriately multiplied by the ratio of these currents.

Transistors *mp9* and *mp11* create another current mirror that mirrors current of 5 µA with zero dependency on absolute temperature ZTAT. Thus, the initial dimensions of these transistors might be the same as in previous case, only the width has to be set to 15 µm instead of 30 µm because the current sourced is 5 µA and not 10 µA.

Transistors *mp9*, *mp11*, *mp12*, *mp13*, *mp14*, *mp15* and *mp16* are working as cascodes. The only task of these transistors is to keep voltage on their sources the same regardless the voltage on their drains. This basically means that these transistors are increasing the overall r_o of the PMOS current mirror. To keep these transistors as small as possible the minimal length of 0.5 µm is chosen.

To be able to work as cascodes, these transistors must work in saturation region. Because of that, the width of these transistors is set so that the V_{GS} - V_{TH} is 0 V. This condition ensures that the V_{DSAT} of these transistors is as low as possible and thus the ability to reach the saturation region is maximized.

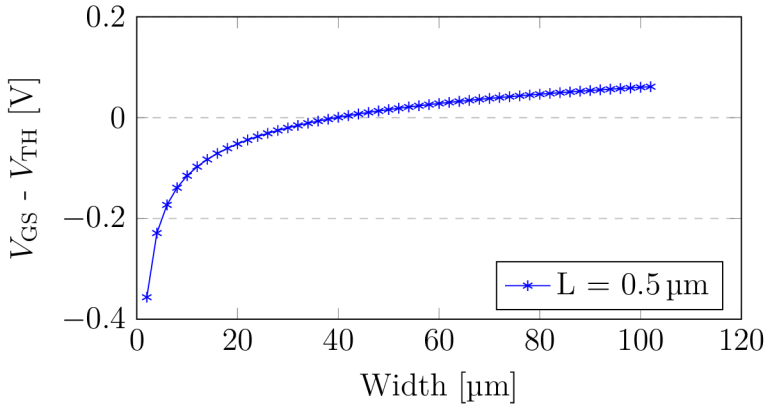

Fig. 4.20: The V_{GS} - V_{TH} of the PMOS transistor vs. its width when being biased with 10 µA

As can be seen in figure 4.20 the width of 40 µm should ensure that the V_{DSAT} = V_{GS} - V_{TH} = 0 V. Also, in this case applies the rule that the width of transistors with higher current than 10 µA has to be multiplied by the ratio of these currents.

It can be noticed that the transistors *mp18* and *mp19* are also working as cascodes for the transistors *mp9* and *mp11*. Thus, the dimensions of these transistors can be derived with the same logic as it was in the previous case. The only difference is that the current of only 5 µA is flowing through these transistors so width of 20 µm is chosen instead of 40 µm.

Transistors *mn0*, *mn1*, *mn2* and *mn4* create the NMOS current mirror. As it was mentioned previously, the higher the r_o of the MOS transistor is the lower the current mismatch error is. Thus, to find out the appropriate length of these devices the simulation showing the r_o of the NMOS transistor versus its length when being biased with 10 µA has been performed and the results are shown in figure 4.21.

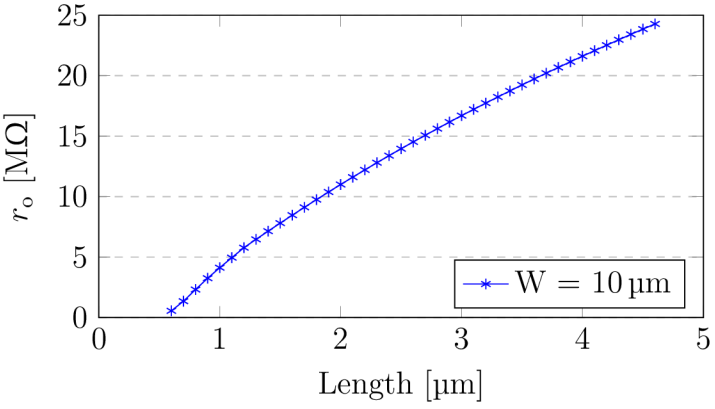

Fig. 4.21: The r_o of the NMOS transistor vs. its length when being biased with 10 µA

Based on the results from figure 4.21, the length of 2 µm is chosen to achieve the r_o of 10 MΩ and to keep the area of the NMOS current mirror reasonable.

As it was in the case of the PMOS current mirror, it is also desirable for the NMOS current mirror to work in the strong inversion region.

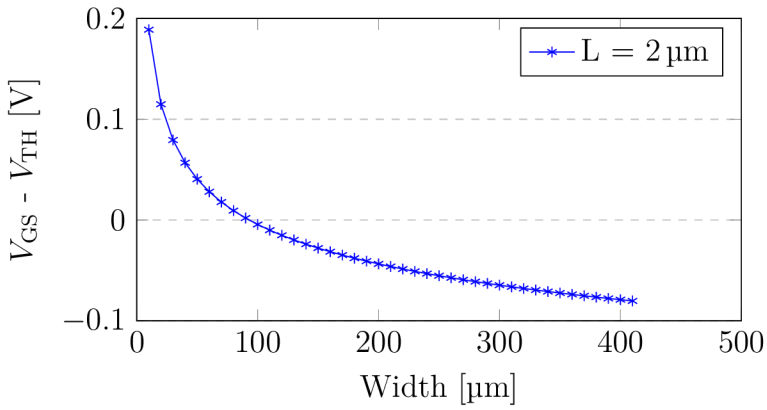

Fig. 4.22: The V_{GS} - V_{TH} of the NMOS transistor vs. its width when being biased with 10 µA

It can be seen in figure 4.22 that with width of 20 µm the V_{GS} - V_{TH} of the transistors in the NMOS current mirror should be around 100 mV. This value should ensure that these transistors will work in the strong inversion.

The width of *mn1* and *mn2* must be set to 80 µm as the current flowing through them is 40 µA.

Transistors *mn6*, *mn7*, *mn8* and *mn10* are working as cascodes. Their main task is to ensure that the voltage on their sources remains the same regardless the voltage on their drains. To keep these devices as small as possible the minimum length of 0.6 µm is chosen. To maximize the ability to work in the saturation region with the lowest V_{DS} possible, the difference V_{GS} - V_{TH} is chosen so that it is equal to 0 V.

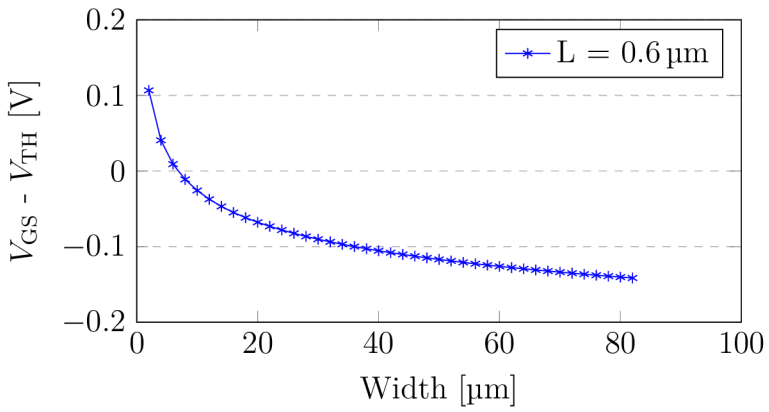

Fig. 4.23: The V_{GS} - V_{TH} of the NMOS transistor vs. its width when being biased with 10 µA

It can be seen in figure 4.23 that with width of 7 µm the difference V_{GS} - V_{TH} = 0 V should be achieved.

The width of *mn7* and *mn8* must scale appropriately from 7 µm to 14 µm as the current flowing through them is 20 µA.

Transistor *mn5* generates one V_{GS} above ground to bias the NMOS current mirror cascodes. Based on the sizing of the transistors in the NMOS current mirror the dimensions for *mn5* are chosen. Thus, the length of 2 µm and width of 10 µm is chosen for the transistor *mn5* as the current of 5 µA is half of the current flowing through the transistor *mn0*.

Transistors *mn9* and *mn11* create the floating current source or the floating current mirror. Currents flowing through each of these transistors are the same. Thus, the dimension will also be the same. As these two transistors work as current source and as dimensions for the NMOS current mirror, which also works as the current source, have been set previously, the same initial dimensions are used for *mn9* and *mn11*. It is length of 2 µm and width of 20 µm.

Transistors *mn12* and *mn13* are working as floating cascodes for transistors *mn9* and *mn11*. As dimensions for the NMOS transistors working as cascodes have already been derived previously, the initial dimensions for *mn12* and *mn13* are going to be the same. It is the minimum length of 0.6 µm and width of 7 µm.

Transistors *mp17*, *mp20* and *mp21* are also working as floating current source or floating current mirror. As dimensions for the PMOS transistor working as the current mirror have already been derived the same dimensions will be used in case of these 3 transistors. It is the length of 2 µm and width of 30 µm for *mp17* and *mp21*, and width of 60 µm for *mp20* as the current flowing through this transistor is two times higher than current flowing through *mp17* and *mp21*.

Transistors *mp22*, *mp23* and *mp24* work as cascodes for transistors *mp17*, *mp20* and *mp21*. Dimensions for the PMOS transistors working as cascodes have already been derived previously. Because of that, the same dimensions will be used for these 3 transistors. It is the minimum length of 0.5 µm and width of 40 µm for *mp22* and *mp24* and 80 µm for *mp23*.

The initial dimensions of all transistors are summarized in table 4.1.

Tab. 4.1: Initial dimensions of all transistors in the proposed voltage follower

Transistor	Width [µm]	Length [µm]	Transistor	Width [µm]	Length [µm]
mp0	200	0.5	mn0	20	2
mp1	200	0.5	mn1	80	2
mp2	30	2	mn2	80	2
mp3	30	2	mn3	8	0.6
mp4	120	2	mn4	20	2
mp5	60	2	mn5	15	2
mp6	60	2	mn6	7	0.6
mp7	30	2	mn7	14	0.6
mp8	40	0.5	mn8	14	0.6
mp9	15	2	mn9	20	2
mp10	40	0.5	mn10	7	0.6
mp11	15	2	mn11	20	2
mp12	40	0.5	mn12	7	0.6
mp13	160	0.5	mn13	7	0.6
mp14	80	0.5	mno	80	0.6
mp15	80	0.5	—	—	—
mp16	40	0.5	—	—	—
mp17	30	2	—	—	—
mp18	20	0.4	—	—	—
mp19	20	0.5	—	—	—
mp20	60	2	—	—	—
mp21	30	2	—	—	—
mp22	40	0.5	—	—	—
mp23	80	0.5	—	—	—
mp24	40	0.5	—	—	—
mpo	400	0.5	—	—	—

It is necessary to bear in mind that dimensions in table 4.1 are only initial. To get final dimensions of all transistors in the proposed voltage follower more

simulations are necessary to perform. The optimization process is described in following subsection 4.4.1.

Optimization of the voltage follower

The first condition that must be met is that all transistors must work in the saturation region across all corners. Thus, the proposed voltage follower will be simulated across following corners:

- VDD: 4.75 V, 5 V and 5.25 V,
- temperature: −40 °C to 125 °C,
- biasing current accuracy: 85 %, 100 % and 115 %,
- input voltage: 0.02 V and 1.25 V,
- process variation models: fnfpfrfc, fnfpsrsc, fnspnrnc, nominal, snfpnrnc, snspfrfc, snspsrsc.

The overall number of corners given by the combinations of conditions summarized above is 126.

To check whether particular transistor is working in saturation or not, the condition given by equation 4.2 must apply.

$$V_{DS} - V_{DSAT} \geq 60mV \tag{4.2}$$

Also, to ensure that none of the transistors is working deep into weak inversion, the condition given by equation 4.3 must be met.

$$V_{GS} - V_{TH} \geq -200mV \tag{4.3}$$

Dimensions of all transistors will be edited to ensure that the conditions given by equations 4.2 and 4.3 are being met across all corners.

After simulation of the voltage follower across all corners mentioned in the list above, dimensions of several transistors were changed in order to meet the conditions given by equations 4.2 and 4.3. The transistors that have been changed are summarized in table 4.2.

Tab. 4.2: Dimensions changes in the voltage follower after the optimization

Transistor	from width [µm]	to width [µm]	from length [µm]	to length [µm]
mp9	15	3	2	2
mp11	15	3	2	2
mn5	15	2	2	2

To understand the reason why the width of *mp9* and *mp11* had to be increased, it is necessary to have a look at following equation 4.4.

$$V_{GS_{mp9}} = V_{GS_{mp11}} = V_{GS_{mp10}} + V_{DS_{mp2}} \tag{4.4}$$

It can be noticed in equation 4.4 that the V_{GS} of transistors *mp9* and *mp11* directly sets the V_{DS} of transistor *mp2*. It was observed in some corners of the simulation that the V_{DS} of *mp2* was too low and the transistors *mp2* up to *mp7* were no longer in the saturation region and thus were not working as current sources. To increase the V_{DS} of the transistors *mp2* up to *mp7* the V_{GS} of *mp9* and *mp11* had to be increased. This was done by decreasing the width of *mp9* and *mp11* from 15 µm to 3 µm.

The very same issue was observed on the NMOS side.

$$V_{GS_{mn5}} = V_{GS_{mn6}} + V_{DS_{mn0}} \tag{4.5}$$

As can be seen in equation 4.5, the V_{GS} of *mn5* directly sets the V_{DS} of transistor *mn0*. It was observed in some corners of the simulation that the transistor *mn0* was not working in the saturation region as its V_{DS} was too low. To increase the V_{DS} of transistor *mn0* the width of the transistor *mn5* was decreased from 15 µm to 2 µm. Such a change increased the V_{GS} of *mn5* and thus the V_{DS} of *mn0*.

After optimization, all transistors in the voltage follower meet the conditions given by equations 4.2 and 4.3 except 2 of them.

The transistor *mn0* does not meet the condition given by equation 4.2 in 50 % of the corners mentioned in the list above. This issue was expected as one of the corner sets the V_{IN} of the proposed voltage follower to 0.02 V. If the voltage follower works correctly, the input voltage gets directly to the output of the voltage follower and thus equation 4.6 applies.

$$V_{DS_{mno}} = V_{IN} = V_{OUT} = 20\,\mathrm{mV} \tag{4.6}$$

It is clear that the condition given by equation 4.2 cannot be met with the V_{DS} of transistor *mno* equal to 0.02 V.

The second transistor that does not meet the condition given by equation 4.2 is *mp15*. The condition is not being met in 22 % of all corners and the minimum value which this transistor meets is −18 mV. Even though the issue had been seen no change was introduced. It is necessary to realize that this transistor is working as a cascode and its only task is to make sure that the voltage on its source remains the same regardless the voltage on its drain. The transistor *mp15* is able to maintain this function even in these 22 % where the condition given by equation 4.2 is not being met.

Design of the switch SW_1 and capacitor C_1

The next step would be check stability of the voltage follower, but in order to do that, capacitor C_1 and switch SW_1 must be designed first so that the load of the voltage follower F_1 is known.

In order to mitigate the leakage current from switch SW_1 and crosstalk from the node *in* to the node *out*, architecture depicted in figure 4.24 is going to be designed and used.

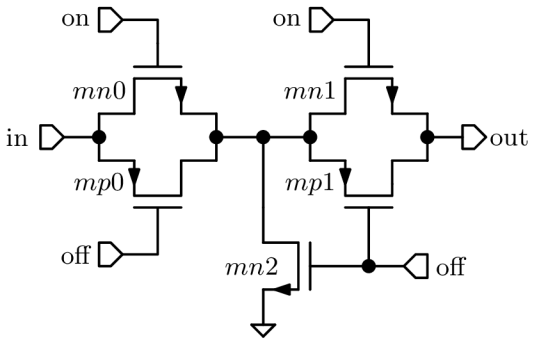

Fig. 4.24: Architecture of the switch in the sample and hold circuit

The transistors *mn0* and *mp0* create so called t-gate switch as well as the transistors *mn1* and *mp1*. The transistor *mn2* is simple NMOS switch and its purpose is to connect the middle node of the whole switch SW_1 to the ground when the switch SW_1 is in open state in order to mitigate the crosstalk from node *in* to node *out*.

The leakage current going out of the switch SW_1 is the biggest contributor to the error in this case as it charges the capacitor C_1 no matter the fact that the switch SW_1 is open. Because of that, the dimensions of the devices inside of the switch SW_1 are going to be designed in a way that will mitigate this undesirable current as much as possible. Nevertheless, it is necessary to realize first that the sample and hold circuit will be sampling voltage around 20 mV or 1 V as it was found out in simulations. This means that the voltage at node *out* will be somewhere around these values and thus, the V_{GS} voltage of transistor *mp1* is going to be highly positive which means that this transistor will be completely turned off and no current will be able to flow between its drain and source. Due to this fact, the lowest length possible is going to be chosen for the transistors *mp0* and *mp1* and that is 0.5 µm. On the other hand, the NMOS transistors *mn0* and *mn1* can have the V_{GS} voltage of -20 mV which still does not mean that no current can flow between their drain and source. Thus, based on figure 4.15, length of 0.8 µm is going to be chosen for these devices in order to mitigate the leakage current from drain to source.

The widths of transistors *mn0*, *mp0*, *mn1* and *mp1* are going to be set so that one t-gate switch has around 250 Ω of on resistance r_{on} when being closed and also

so that the charge injection of both devices is being mitigated by each other. In order to find out the appropriate width of these transistors, the simulation has been performed and the results are shown in figure 4.25.

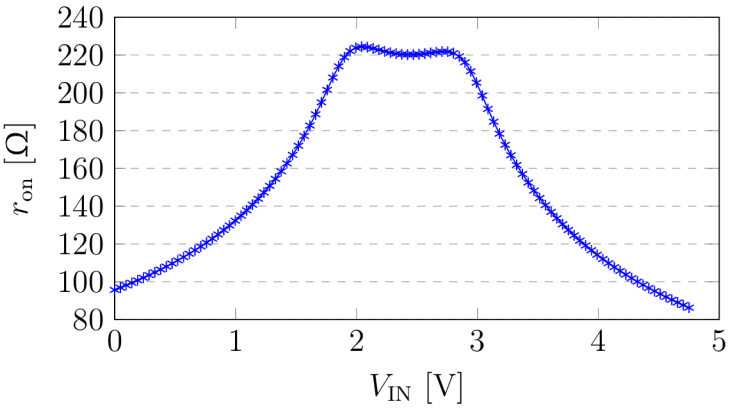

Fig. 4.25: The r_{on} of the t-gate switches *mn0* + *mp0* and *mn1* + *mp1* vs. V_{IN}

In figure 4.25 can be seen the r_{on} of one t-gate switch that was achieved in the worst case corner. This means that the switch SW_1 has the worst case r_{on} of 450 Ω.

The final dimensions of all devices in the switch SW_1 are summarized in table 4.3.

Tab. 4.3: The final dimensions of devices in the switch SW_1

transistor	width [µm]	length [µm]
mn0,1	40	0.8
mp0,1	100	0.5
mn2	1	1

Another value to decide is the value of the sampling capacitor C_1 in figure 4.11. It is necessary to realize that the higher the value of the capacitor C_1 is, the lower impact the leakage current of switch SW_1 has. On the other hand, capacitors in general are very demanding with regards to area on the die. Because of that, the value of 10 pF is set for the capacitor C_1. This value was chosen as a good compromise between the capacitor area on the chip and the ability to mitigate the effect of the leakage current going out of the switch SW_1.

Capacitor C_1 together with on resistance r_{on} of switch SW_1 introduces time constant that is given by following equation 4.7.

$$\tau = r_{on_{SW_1}} C_1 = 450 \times 10 \times 10^{-12} = 4.5\,\text{ns} \tag{4.7}$$

The fastest signal that can go through the AD7606C PGA is given by its f_{3dB} that is, in worst case, equal to 50 kHz. Based on that information, it can be assumed that all signals up to 50 kHz must be settled within 100 µs. For these signals to be settled with 18 bits precision, the time constant of the low pass filter that is given by SW_1 and capacitor C_1, must be lower than [4]:

$$\tau = \frac{100\,\mu s}{12.48} = 8\,\mu s > 4.5\,ns. \tag{4.8}$$

As it can be see in equation 4.8 the time constant of the proposed switch SW_1 and capacitor C_1 is much lower than it should be. This means that signals up to 50 kHz should be able to go through the low pass filter made of switch SW_1 and capacitor C_1 without any distortion.

Design of the switch SW_2

The last circuit in figure 4.11 that needs to be designed is switch SW_2. The purpose of this switch is to provide connection from the output of the voltage follower F_2 and the input of the lower range channel PGA. It is clear that the voltage V_{OUT} in figure 4.11 should be as close as possible to the voltage $V_{OUT_{F_2}}$. Thus, the r_{on} of switch SW_2 should be as low as possible. Because of that, for the switch SW_2 one half of the switch SW_1 will be used. This means that in worst case scenario the switch SW_2 should have the r_{on} of 225 Ω as it can be see in figure 4.25.

Stability of the voltage followers F_1 and F_2

As loads for both voltage followers are known in this part of this thesis it is possible to analyse stability. It can be seen in figure 4.12 that for compensation of the feedback loop, capacitors C_1 and C_2 are being used. To decide value of these capacitors, multiple simulations, showing the phase and gain response of the open feedback loop, are going to be run across all corners that were mentioned in the list above. The goal is to get minimum of 50° of the phase margin in the worst case scenario.

It was found out that with the capacitors C_1 and C_2 equal to 1.38 pF the minimum phase margin in worst case scenario is 50°.

All results obtained during the frequency simulation can be observed in figure C.4.

4.4.2 Changes in the internal logic block

As two new signals are necessary to drive the previously designed sample and hold circuit, few changes were also made to the internal logic block. The behavioural model of this block can be seen in listing B.5.

4.4.3 Implementation of the proposed sample and hold circuit

As the sample and hold circuit has been designed, the same simulations, as in sections 4.3 and 4.2, are going to be run to find out the potential performance of this proposed option. The results obtained are shown in figure 4.26.

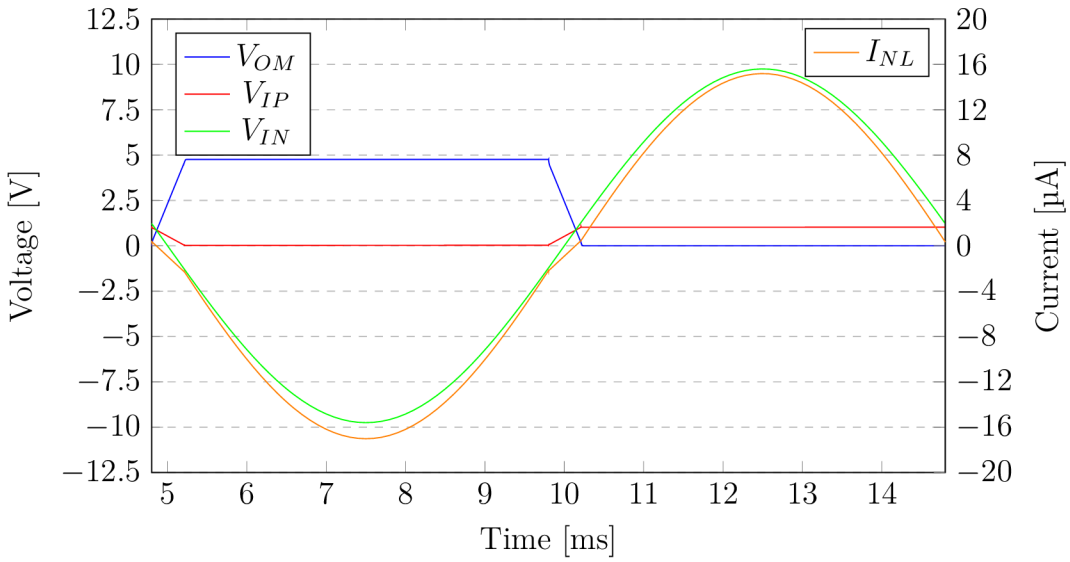

Fig. 4.26: The transient analysis of the lower range channel while using the sample and hold circuit

As can be seen in figure 4.26, once the V_{IN} is outside of the lower range channel range, that is in this case $\pm 1.25\,\mathrm{V}$, the voltage V_{IP} in the core of the PGA gets sampled and then holds on this sampled value until the V_{IN} is back in the range. Thanks to this process, the non-linearity of the I_{NL} current is mitigated to minimum. To see the final THD performance of this mitigation technique, the transient simulation with different values of the R_{EXT} has been performed and the results obtained are shown in figure 4.27.

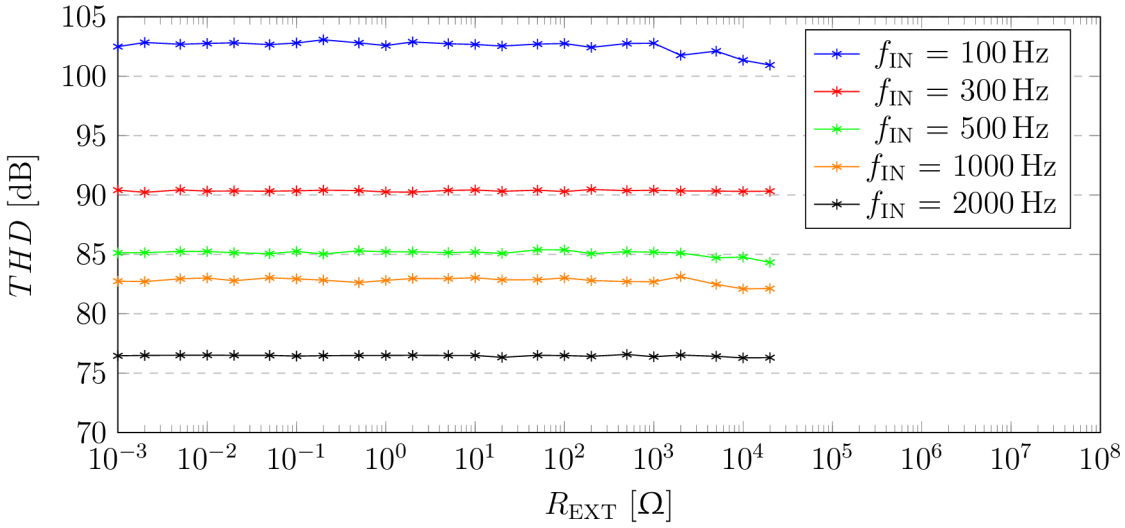

Fig. 4.27: The THD performance of the channel merging versus the R_{EXT} with the sample and hold circuit

It can be seen in figure 4.27 that connecting the input of the PGA core to the sampled value of the virtual ground makes the merging of ±10 V and ±1.25 V channels immune to the value of the R_{EXT}. It can also be noticed that with this technique higher THD values are achieved for higher input frequencies in comparison with the previously proposed techniques as it can be seen in figures 4.9 and 4.6, where the THD is equal to 50 dB for the input frequency equal to 2000 Hz. This makes this technique more attractive in terms of performance than the other techniques.

4.5 Summary of proposed options

Three options to mitigate the I_{NL}, which is undesirable phenomenon when merging 2 channels with different ranges, were proposed, designed and simulated. As can be seen in figures 4.6, 4.9 and 4.27, all 3 options were able to mitigate the effect of the I_{NL} to absolute minimum.

The first technique uses switching of gain G of the lower range channel based on the value of the V_{IN}. This technique only requires changes in the internal logic block in comparison with the currently implemented solution on silicon so it is very convenient in terms of implementation. On the other hand, this technique can not be used for merging the ±10 V channel and the ±1.25 V channel as there is no way how to simply switch from the ±1.25 V range to the ±10 V range. This fact makes this technique unattractive for solutions where the high DR performance is desirable.

The second technique only connects the inputs of the PGA core to the ground when the V_{IN} is outside of the lower range channel range. This technique requires changes in the internal logic block as well as implementation of 2 switches in the analog circuitry. This makes it a bit more complicated for implementation than the first option. The big advantage in comparison with option 1 is that it can be used for merging the $\pm 10\,\mathrm{V}$ and $\pm 1.25\,\mathrm{V}$ channels. This makes this technique highly attractive for solutions where the high DR performance is key requirement.

The third and last technique connects the inputs of the PGA core to the sampled value of the virtual ground. It requires the sample and hold circuit as well as changes in the internal logic block. This makes this technique highly unattractive in terms of implementation. On the other hand, with this technique the highest THD performance has been achieved for higher input frequencies as can be seen in table 4.4.

Tab. 4.4: The THD performance summary of proposed options to mitigate the I_{NL}

f_{IN} [Hz]	THD [dB]		
	option 1	option 2	option 3
100	95.2	100.5	102.5
300	87.3	93.6	90.4
500	80.7	89.0	85.1
1000	63.3	65.4	82.7
2000	49.8	50.2	76.5

It is not clear from the summary what option would be the best to choose as it is highly dependent on key requirement. If the key requirement is minimum changes to the silicon, then option 1 or option 2 would be appropriate. Nevertheless, if the key requirement is high DR and high THD performance, then the option 3 should be the one to choose.

Conclusion

The thesis aimed to evaluate channel merging technique currently implemented on the Analog Devices part AD7606C and then propose, design and simulate options to increase the dynamic range performance of this channel merging technique and finally propose and analyze options to mitigate the non-linear current going out of the lower range channel when it gets saturated.

In section 2.1 it was discovered that the currently implemented channel merging technique can achieve 115 dB of dynamic range with the oversampling ratio equal to 256. Also, later in section 2.3 different sources of error and their impact on the THD performance have been presented. It was discovered that the THD performance decreases rapidly with increasing value of the external resistor R_{EXT} as can be seen in figure 2.14. This phenomenon makes this technique unattractive for customers as they want to use the external resistor as a part of the anti-aliasing filter. Thus, chapter 4 is trying to propose options to mitigate this phenomenon.

In chapter 3 three options to improve the currently implemented channel merging technique were proposed, designed and simulated. As can be seen in the summary in section 3.4, the best dynamic range performance of 118.6 dB has been achieved with the oversampling ratio equal to 256 with option 3. This option combines decreasing the original cutoff frequency $f_{3\mathrm{dB}}$ to half together with decreasing the range of the lower range channel from $\pm 2.5\,\mathrm{V}$ to $\pm 1.25\,\mathrm{V}$.

As it was mentioned, the non-linear current going out of the lower range channel is causing the THD performance degradation in the AD7606C. Thus, in chapter 4, three options to mitigate this issue were proposed, designed and simulated. It was discovered that all three options can make the presented channel merging technique immune to the value of the external resistor R_{EXT} as the non-linearity of the current was mitigated to a minimum. Nevertheless, option 1 turned out to be inappropriate as it cannot be used with the $\pm 1.25\,\mathrm{V}$ range. On the other hand, option 2, which is disconnecting the lower range channel from the signal chain, requires minimal changes to the current silicon and can work with the $\pm 1.25\,\mathrm{V}$ range. This makes option 2 highly attractive. However, the best THD performance has been achieved with option 3, but as it requires a lot of additional circuitry to the existing die, it is probably not going to be used in the AD7606C next generic.

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List of symbols, physical constants and abbreviations

MOS	Metal-oxide-semiconductor
PMOS	P-type metal-oxide-semiconductor
NMOS	N-type metal-oxide-semiconductor
PTAT	Proportional to absolute temperature
ZTAT	Variable independent of temperature
PGA	Programmable Gain Amplifier
ADC	Analog to Digital Converter
RMS	Root Mean Square
LSB	Least Significant Bit

DR	dynamic range
DR_{EXT}	extra dynamic range
SNR	signal-to-noise ratio
G	gain
PM	phase margin
GM	gain margin
UGF	unity gain frequency
THD	total harmonic distortion
$n_{\mathbf{RMS}}$	RMS noise
OSR	oversampling ratio
$r_{\mathbf{o}}$	output impedance
$r_{\mathbf{on}}$	on resistance
$I_{\mathbf{DD}}$	current consumption
$R_{\mathbf{IN}}$	input resistor
$R_{\mathbf{FB}}$	feedback resistor
$R_{\mathbf{EXT}}$	external resistor
$C_{\mathbf{FB}}$	feedback capacitor
$V_{\mathbf{DD}}$	power supply voltage
$V_{\mathbf{GS}}$	gate-to-source voltage of MOS transistor
$V_{\mathbf{TH}}$	threshold voltage of MOS transistor
$V_{\mathbf{DS}}$	drain-to-source voltage of MOS transistor
$V_{\mathbf{DSAT}}$	minimum V_{DS} required to maintain MOS transistor in saturation
$V_{\mathbf{IN}}$	input voltage

$V_{\mathbf{ER}}$	error voltage
$V_{\mathbf{OF}}$	offset voltage
$V_{\mathbf{OFdrift}}$	offset voltage temperature drift
$f_{\mathbf{IN}}$	frequency of input signal
$f_{\mathbf{S}}$	sampling frequency
$f_{\mathbf{SI}}$	internal sampling frequency
$f_{\mathbf{3dB}}$	cutoff frequency
$V_{\mathbf{REF}}$	reference voltage
ϑ	temperature [°C]
$I_{\mathbf{NL}}$	non-linear current
gm	transconductance
$I_{\mathbf{lkg}}$	leakage current of MOS transistor

List of appendices

A Sample and hold circuit schematics

A.1 Sample and hold circuit top-level view

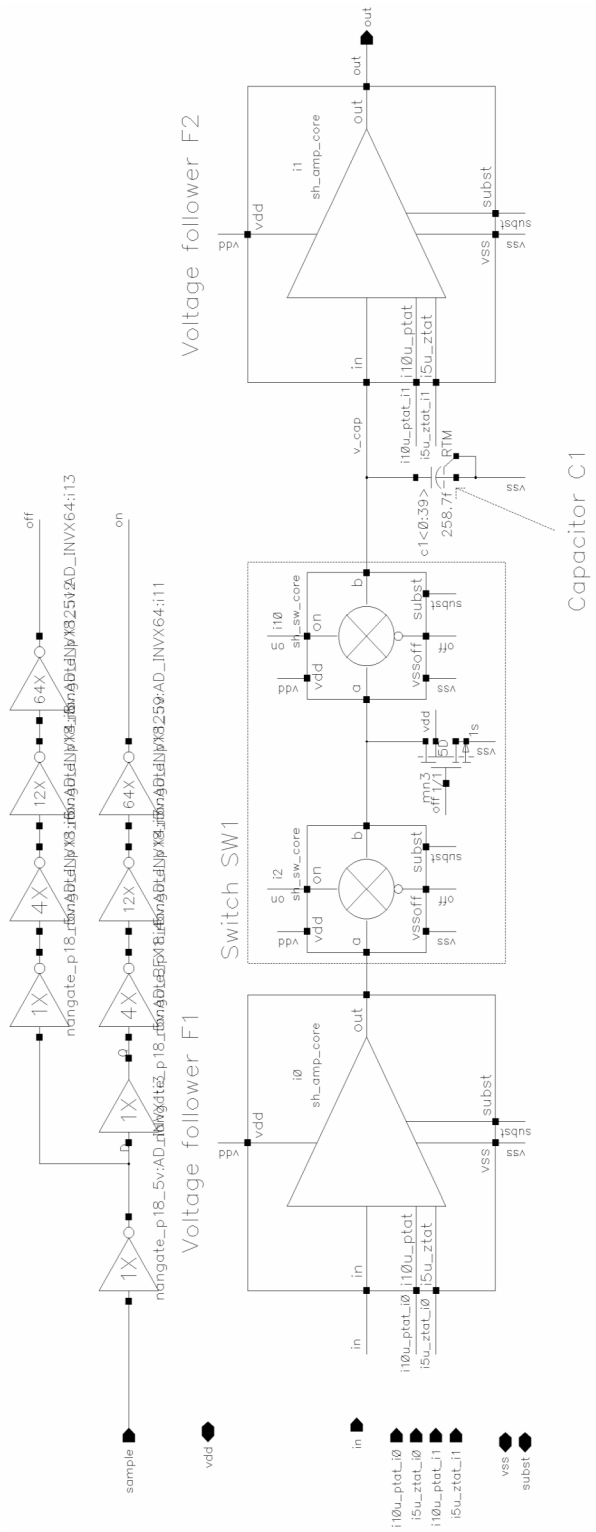

Fig. A.1: Top-level view of sample and hold circuit

A.2 Voltage follower

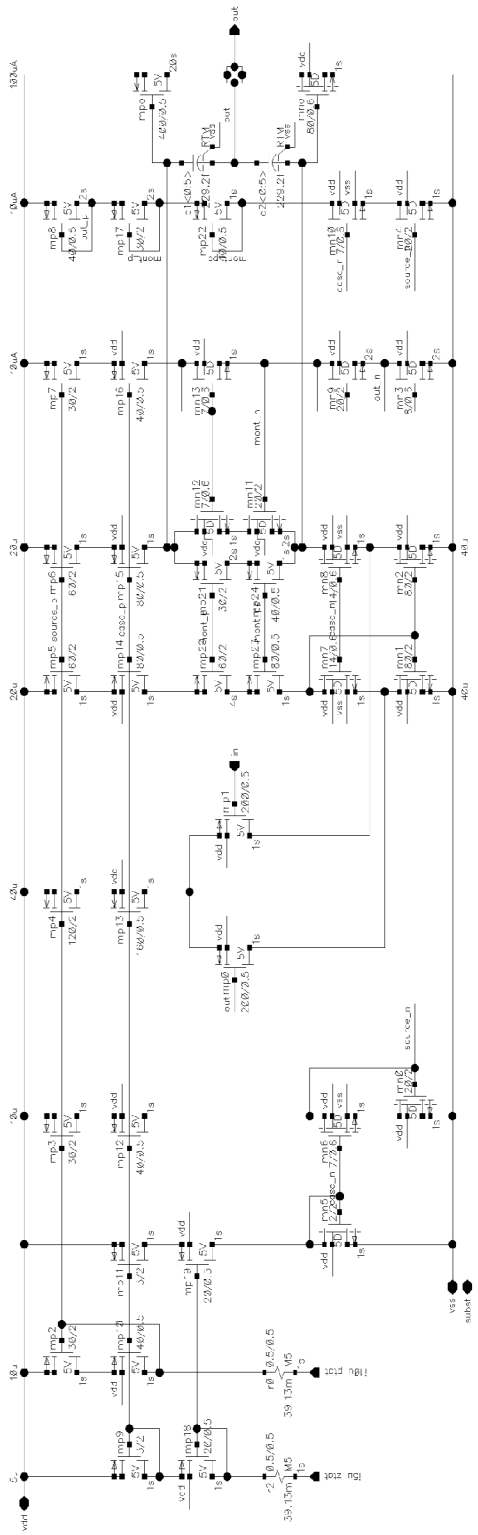

Fig. A.2: Voltage follower schematic

A.3 Switch

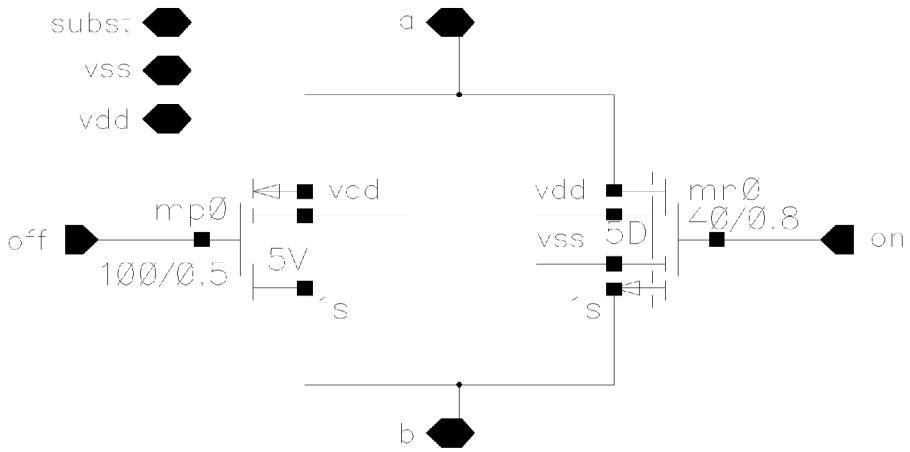

Fig. A.3: Schematic of switch in the sample and hold circuit

B Behavioural models of the internal logic block

Listing B.1: Behavioural model of the internal logic block merging the ±10 V and the ±2.5 V channels.

```
MODEL dyn_logic_2p5_to_10v_no_midgains_rs {
 UMInLogicArray in_10v(size=18), in_2p5v(size=18);
 UMOutLogicArray out;
 UMOutLogic range_2p5v, range_5v, range_10v;
 UMOutLogic use_2p5_range;
 UMParmInt margin(def=50);
 UMParmInt num_conv_settle(def=4);
 int count; };
INITIALIZE {
 in_10v.signedInteger();
 in_2p5v.signedInteger();
 count = 0; }
SIMULATE {
  if ( in_10v > -32768 && in_10v < 32768 ) {
    count += 1;
    range_2p5v = 1;
    range_5v = 0;
    range_10v = 0; }
  else if ((in_10v < -32768) || (in_10v > 32768) ) {
    count = 0;
    range_2p5v = 0;
    range_5v = 0;
    range_10v = 1; }
  if (count > num_conv_settle) {
    out = in_2p5v;
    use_2p5_range = 1; }
   else {
    out = in_10v<<2;
    use_2p5_range = 0; }}
```

Listing B.2: Behavioral model of the internal logic block merging the ±10 V and the ±1.25 V channels.

```
MODEL dyn_logic_1p25_to_10v_no_midgains_rs {
 UMInLogicArray in_10v(size=18), in_1p25v(size=18);
 UMOutLogicArray out;
 UMOutLogic range_1p25v, range_5v, range_10v;
 UMOutLogic use_1p25_range;
 UMParmInt margin(def=50);
 UMParmInt num_conv_settle(def=4);
 int count;};
INITIALIZE {
 in_10v.signedInteger();
 in_1p25v.signedInteger();
 count = 0;}
SIMULATE {
  if ( in_10v > -16384 && in_10v < 16384 ) {
    count += 1;
    range_1p25v = 1;
    range_5v = 0;
    range_10v = 0;}
  else if ((in_10v < -16384) || (in_10v > 16384) ) {
    count = 0;
    range_1p25v = 0;
    range_5v = 0;
    range_10v = 1;}
  if (count > num_conv_settle) {
    out = in_1p25v;
    use_1p25_range = 1;}
   else {
    out = in_10v<<3;
    use_1p25_range = 0;}}
```

Listing B.3: Behavioral model of the internal logic block merging the ±10 V and the ±2.5 V channels with gain switching algorithm.

```
MODEL dyn_logic_2p5_to_10v_midgains_rs {
 UMInLogicArray in_10v(size=18), in_2p5v(size=18);
 UMOutLogicArray out;
 UMOutLogicArray gain_sel;
 UMOutLogic range_2p5v, range_5v, range_10v;
 UMOutLogic use_2p5_range;
 UMParmInt margin(def=50);
 UMParmInt num_conv_settle(def=4);
 int count;
 int gain_sel_selected; };
INITIALIZE {
 in_10v.signedInteger();
 in_2p5v.signedInteger();
 count = 0; }
SIMULATE {
  if ( in_10v > -32768 && in_10v < 32768 ) {
    count += 1;
    range_2p5v = 1;
    range_5v = 0;
    range_10v = 0;
    gain_sel = 0; }
  else if ((in_10v < -32768 && in_10v > -65536) ||
       (in_10v > 32768 && in_10v < 65536) ) {
    count = 0;
    range_2p5v = 0;
    range_5v = 1;
    range_10v = 0;
    gain_sel = 1;}
  else {
    count = 0;
    range_2p5v = 0;
    range_5v = 0;
    range_10v = 1;
    gain_sel = 3; }
  if (count > num_conv_settle) {
    out = in_2p5v;
    use_2p5_range = 1; }
   else {
    out = in_10v<<2;
    use_2p5_range = 0; }}
```

Listing B.4: Behavioral model of the internal logic block merging the ±10 V and the ±1.25 V channels with disconnecting algorithm.

```
MODEL dyn_logic_1p25_to_10v_no_midgains_rs {
 UMInLogicArray in_10v(size=18), in_1p25v(size=18);
 UMOutLogicArray out;
 UMOutLogic range_1p25v, range_5v, range_10v;
 UMOutLogic use_1p25_range;
 UMParmInt margin(def=50);
 UMParmInt num_conv_settle(def=4);
 int count;};
INITIALIZE {
 in_10v.signedInteger();
 in_1p25v.signedInteger();
 count = 0; }
SIMULATE {
  if ( in_10v > -16384 && in_10v < 16384 ) {
    count += 1;
    range_1p25v = 1;
    range_5v = 0;
    range_10v = 0;}
  else if ((in_10v < -16384) || (in_10v > 16384) ) {
    count = 0;
    range_1p25v = 0;
    range_5v = 0;
    range_10v = 1; }
  if (count > num_conv_settle) {
    out = in_1p25v;
    use_1p25_range = 1; }
   else {
    out = in_10v<<3;
    use_1p25_range = 0; }}
```

Listing B.5: Behavioral model of the internal logic block merging the ±10 V and the ±1.25 V channels handling sampling and connecting of virtual ground.

```
MODEL dyn_logic_1p25_to_10v_no_midgains_rs_sh {
 UMInLogicArray in_10v(size=18), in_1p25v(size=18);
 UMOutLogicArray out;
 UMOutLogic range_1p25v, range_5v, range_10v;
 UMOutLogic use_1p25_range;
 UMOutLogic sample;
 UMOutLogic connect_vr_gnd;
 UMParmInt margin(def=50);
 UMParmInt num_conv_settle(def=4);
 int count; };
INITIALIZE {
 in_10v.signedInteger();
 in_1p25v.signedInteger();
 count = 0;}
SIMULATE {
  if ( in_10v > -16384 && in_10v < 16384 ) {
    count += 1;
    range_1p25v = 1;
    range_5v = 0;
    range_10v = 0;
    sample = 1;
    connect_vr_gnd = 0; }
  else if ((in_10v < -16384) || (in_10v > 16384) ) {
    count = 0;
    range_1p25v = 0;
    range_5v = 0;
    range_10v = 1;
    connect_vr_gnd = 1;
    sample = 0; }
  if (count > num_conv_settle) {
    out = in_1p25v;
    use_1p25_range = 1;}
   else {
    out = in_10v<<3;
    use_1p25_range = 0;}}
```

C The simulation results of the voltage follower

C.1 The performance summary

Tab. C.1: Basic parameters of the voltage follower

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply	V_{DD}	4.75	5.00	5.25	V
Temperature range	ϑ	−55		135	°C
Current consumption	I_{DD}	400	250	120	µA
Input range	V_{IN}	0		4	V
DC Gain	G	40[1]	102	110	dB
Phase margin	PM	49	66	78	°
Gain margin	GM	14	19	23	dB
Unity gain frequency	UGF	1.97[1]	16.88	26.61	MHz
RMS noise	n_{RMS}	51	78	132	µV
Offset at 25 °C	V_{OF}	−38	37	100	µV
Offset temperature drift	V_{OFdrift}	−0.70		0.74	µV °C^{-1}

[1] Value is for the $V_{\mathrm{IN}} = 20\,\mathrm{mV}$. This means that the output NMOS transistor is out of saturation region and thus the overall gain G decreases. This behaviour is expected.

C.2 Temperature sweep

Tab. C.2: Corners for temperature sweep

Parameter	Symbol	Units	Values
Power supply	V_{DD}	[V]	4.75, 5 and 5.25
Input voltage	V_{IN}	[V]	0.02 and 1.25
Bias current accuracy		[%]	85, 100 and 115
Models			fnfpfrfc, fnfpsrsc, fnspnrnc, nominal, snfpnrnc, snspfrfc, snspsrsc

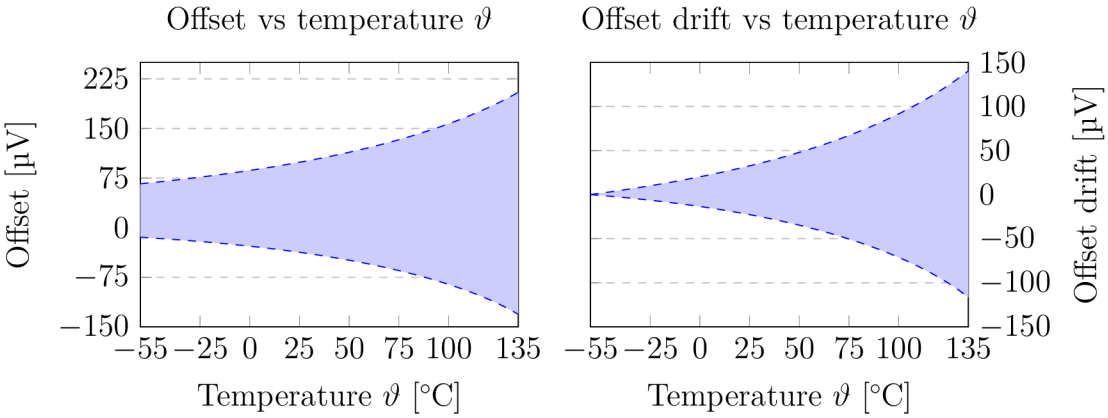

Fig. C.1: Offset and offset drift of the voltage follower versus temperature ϑ

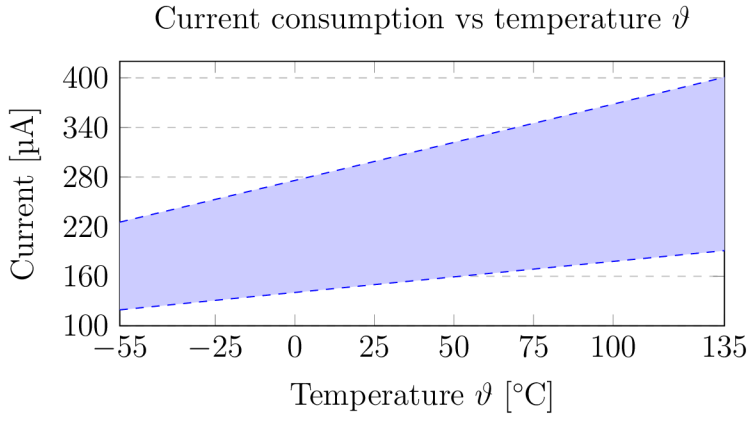

Fig. C.2: Current consumption of the voltage follower versus temperature ϑ

C.3 Input voltage sweep

Tab. C.3: Corners for input voltage sweep

Parameter	Symbol	Units	Values
Power supply	V_{DD}	[V]	4.75, 5 and 5.25
Bias current accuracy		[%]	85, 100 and 115
Temperature	ϑ	[°C]	−55, 27 and 135
Models			fnfpfrfc, fnfpsrsc, fnspnrnc, nominal, snfpnrnc, snspfrfc, snspsrsc

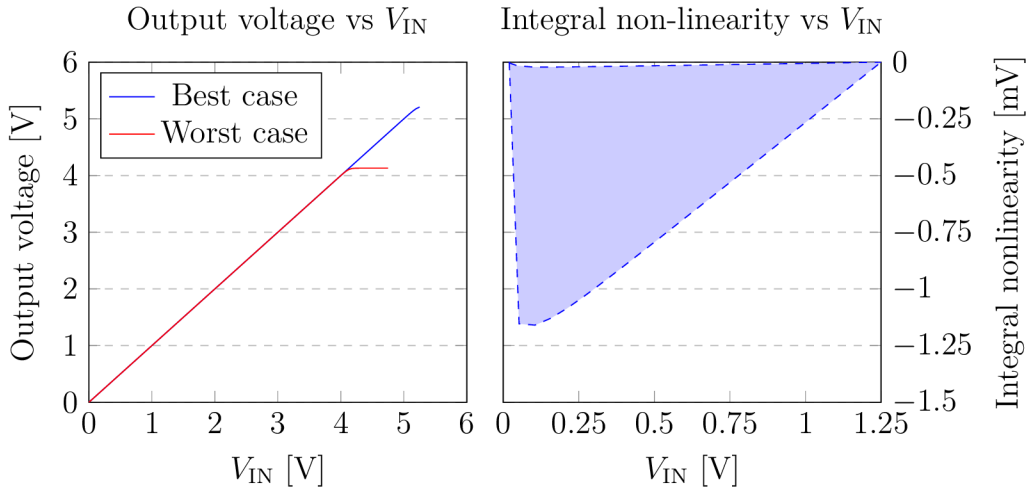

Fig. C.3: Integral non-linearity and the output voltage of the voltage follower versus the V_{IN}

C.4 Frequency sweep

Tab. C.4: Corners for frequency sweep

Parameter	Symbol	Units	Values
Power supply	V_{DD}	[V]	4.75, 5 and 5.25
Input voltage	V_{IN}	[V]	0.02 and 1.25
Bias current accuracy		[%]	85, 100 and 115
Temperature	ϑ	[°C]	−55, 27 and 135
Output capacitor	C	[pF]	10
Models			fnfpfrfc, fnfpsrsc, fnspnrnc, nominal, snfpnrnc, snspfrfc, snspsrsc

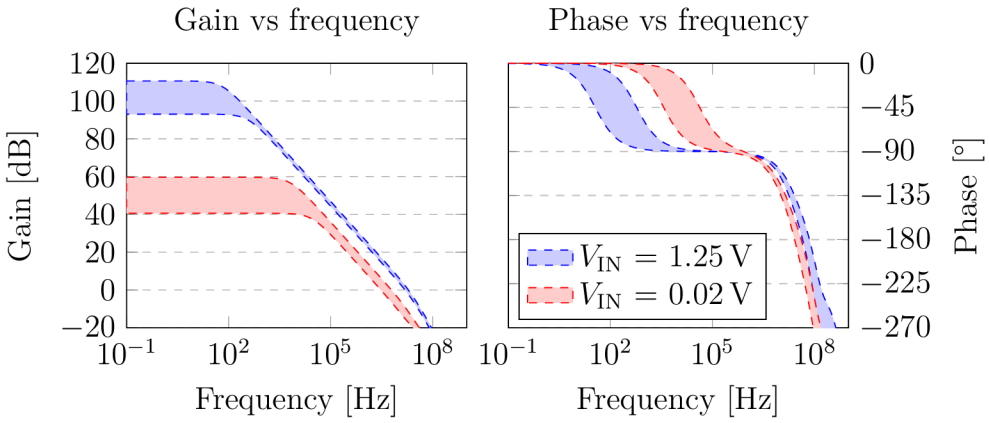

Fig. C.4: Gain and phase response of the voltage follower

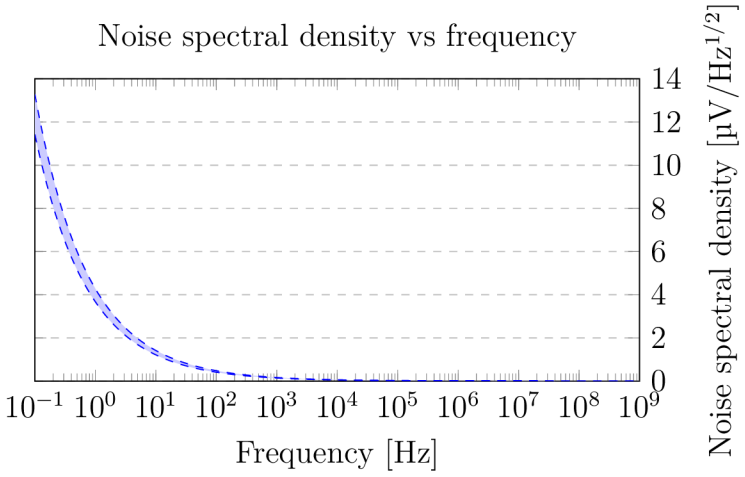

Fig. C.5: Noise performance of the voltage follower

D Simulation results of switch

D.1 Input voltage sweep

Tab. D.1: Corners for the V_{IN} sweep

Parameter	Symbol	Units	Values
Power supply	V_{DD}	[V]	4.75, 5 and 5.25
Temperature	ϑ	[°C]	−55, 27 and 135
Models			fnfpfrfc, fnfpsrsc, fnspnrnc, nominal, snfpnrnc, snspfrfc, snspsrsc

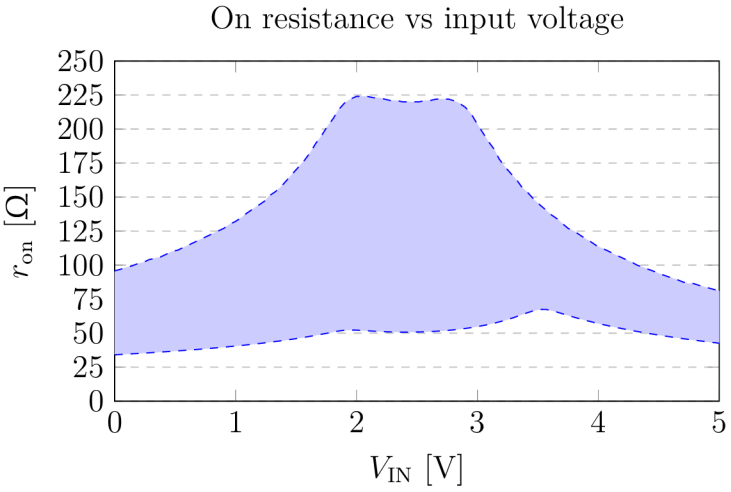

Fig. D.1: On resistance r_{on} of switch versus the V_{IN}