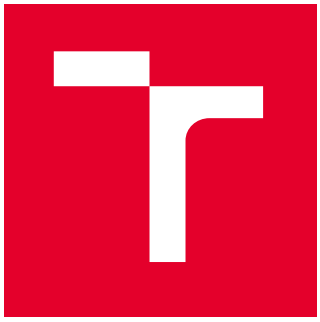

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FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY
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DEPARTMENT OF RADIO ELECTRONICS

ÚSTAV RADIOELEKTRONIKY

LHC ABORT GAP MONITOR ACQUISITION SYSTEM

AKVIZIČNÍ SYSTÉM PRO LHC ABORT GAP MONITOR

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

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BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

Master's Thesis

Master's study program **Electronics and Communication Technologies**

Department of Radio Electronics

Student: Bc. Petr Pacner ***ID:*** 195406

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TITLE OF THESIS:

LHC Abort Gap Monitor acquisition system

INSTRUCTION:

In the introduction part get acquainted with the LHC beam dump system, a system which extracts beam particles from the LHC accelerator beamlines. Describe the technical implementation of the LHC beam-dump system, put emphasis on description of the beam bunch pattern, and in particular of the abort gap in the bunch pattern. Describe current measurement method quantifying amount of the particles in the abort gap and analyse the issues associated with the use of specialised analogue integrators in the implemented method. Design a concept of a new system applying a direct signal analogue to digital conversion and processing the entire measurement in the digital domain. For the new design deploy off-shelf components used in the CERN SY-BI group.

Create a digital acquisition system based on the proposed design. Implement it using modern HDL techniques and demonstrate theoretical functionality of the system using HDL verification tools. Install the acquisition system in the LHC and measure data from a real system.

Thesis supervisor is Ing. David Bělohrad, PhD (CERN).

RECOMMENDED LITERATURE:

[1] FUKÁTKO, Tomáš. Detekce a měření různých druhů záření. Praha: BEN - technická literatura, 2007. Senzory neelektrických veličin. ISBN 978-80-7300-193-3.

[2] LINDH Lennart, KLEVIN Tommy. Advanced HW/SW Embedded System for Designers, 2018: FPGA - System On Chip. Independently published, 2018. ISBN: 978-1731115812

[3] IHNÁT Kryštof: FPGA-based Pulse Classification. Brno 2019/2020, 87 p. Master Thesis. Brno University of Technology, Faculty of Electrical Engineering and Communication, Department of Radio Electronics. Advised by Ing. Michal Kubíček, Ph.D.

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Supervisor: Ing. Michal Kubíček, Ph.D.

prof. Dr. Ing. Zbyněk Raida
Chair of study program board

ABSTRACT

The Beam Dump System of the LHC Large Hadron Collider is one of its critical systems. It is responsible for changing the trajectory of the beam towards the beam dump. For its functionality it uses an Abort Gap - a space with no particles within a beam structure. This gap is formed during the injection of the particles into the LHC. The injection is never ideal hence Abort Gap always contains some particles. Energy accumulated in the Abort Gap can cause various damages and so the amount has to be continuously estimated. This is the purpose of an Abort Gap Monitor.

The currently deployed Abort Gap Monitor uses analog integrators to measure the particle population. This makes the instrument difficult to calibrate due to its hardware inaccuracies. To improve the system measurement versatility and reproducibility an effort is made to create an acquisition system with digital integration. This work aims to design, verify and implement the digital acquisition system. The digital acquisition system serves as one of the major parts of the new CERN SY-BI group Abort Gap Monitor.

This document is split into four sections. The first briefly describes the structure of the Beam Dump System and the importance of the Abort Gap. The second section explains the principle of Abort Gap measurements and the data evaluation methodology. The third section describes the current system design and its issues. Then it focuses on the new Abort Gap Monitor topology followed by acquisition system development. The last section presents the simulations and measurements obtained with the new Abort Gap Monitor Acquisition System and discusses further development steps.

KEYWORDS

FPGA, LHC, MCP-PMT, VME64x, Abort Gap, Abort Gap Monitor, Beam Dump System, Non-invasive beam measurement

ABSTRAKT

Beam Dump Systém velkého hadronového urychlovače LHC je jedním z jeho kritických systémů. Ten se stará o odvedení urychlovaného svazku z prostoru urychlovače do míst, kde je absorbován. Pro jeho funkci využívá takzvaný Abort Gap - prázdné místo ve svazku bez částic. Toto místo vznikne při injektování částic do LHC. Injekce není nikdy dokonalá, tudíž Abort Gap vždy nějaké částice obsahuje. Určitá výše energie může způsobit škody na zařízení. Proto je toto množství nutné kontinuálně měřit. K tomuto účelu slouží Abort Gap Monitor.

Současná nainstalovaná verze Abort Gap Monitor využívá k měření analogové integrátory. Ty komplikují kalibrační proces z důvodu jejich výrobních nepřesnosti. Aby se tak zvýšila univerzálnost a reprodukovatelnost měření je snaha vytvořit akviziční systém, který využije digitální integraci. Tato práce si klade za cíl vytvořit, verifikovat a implementovat digitální akviziční systém. Akviziční systém je jeden z hlavních částí nového CERN SY-BI Abort Gap Monitor.

Tento dokument je rozdělen na čtyři částí. První z nich stručně popisuje strukturu Beam Dump Systém a význam Abort Gap. V druhé části je popsán princip měření Abort Gap a metodologie vyhodnocování dat z Abort Gap Monitor. Následuje třetí část popisující současný systéme a jeho známé nedostatky. Pak se zabývá novou topologii Abort Gap Monitor a vývojem jeho akvizičního systému. Poslední oddíl tohoto dokumentu prezentuje simulace a měření získané pomocí nové realizace Abort Gap Monitor akvizičního systému a diskutuje návrhy pro další vývoj.

KLÍČOVÁ SLOVA

FPGA, LHC, MCP-PMT, AGM, VME64x, abort gap, abort gap monitor, beam dump system, neinvazivní měření svazku

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DECLARATION

I declare that I have written the semestral project titled "LHC Abort Gap Monitor Acquisition System" independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the project and listed in the comprehensive bibliography at the end of the project.

As the author I furthermore declare that, with respect to the creation of this semestral project, I have not infringed any copyright or violated anyone's personal and/or ownership rights. In this context, I am fully aware of the consequences of breaking Regulation § 11 of the Copyright Act No. 121/2000 Coll. of the Czech Republic, as amended, and of any breach of rights related to intellectual property or introduced within amendments to relevant Acts such as the Intellectual Property Act or the Criminal Code, Act No. 40/2009 Coll., Section 2, Head VI, Part 4.

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I would like to thank my both supervisors Ing. David Bělohrad, Ph.D. from CERN and Ing. Michal Kubíček, Ph.D. from BUT for their professional support, patience and for giving me very valuable ideas to bring my work to a higher level.

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Contents

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1 Introduction

The Nominal Energy which can be stored in the *Large Hadron Collider* (LHC), at CERN is 350 MJ, distributed in 2808 bunches. This amount of energy is stored in beams with an average transverse size smaller than 1 mm [1]. Such high energy density is dangerous for the accelerator. One bunch hitting a conductive surface is enough to melt metallic surfaces, and destroy surrounding equipment. To safely remove the entire beam from the beamline, the collider incorporates the *Beam Dump System* (BDS). This system is crucial for machine protection, as it has to be operational at all times and be able to intervene promptly when needed.
The BDS uses kicker magnets to deflect the beam towards the beam dump. A certain amount of time is required for the magnet to reach the nominal magnetic field. An empty space of 3 μs, the *Abort Gap* (AG), is reserved for this purpose [2].
If particles are present in this gap during the kicker ramp up, they will be deflected towards the accelerator vacuum chamber. Damage to the machine may occur once a certain population threshold is reached. Therefore continuous monitoring of the AG population is required. This is the purpose of the *Abort Gap Monitor* (AGM) [3]. The AGM uses the *Synchrotron Radiation* (SR) spontaneously emitted by the beam to quantify the fraction of particles present in the AG.
One version of AGM is currently installed in the LHC. This AGM system uses an analog electronics chain, which has certain limitations, including temperature dependence and timing-related issues ⟦↪4.⟧. This thesis aims to mitigate these issues by creating a new AGM *Data Acquisition System* (DAQ) to process the received data in the digital domain. The thesis documents the design verifies its functionality, and performs basic measurements using control scripts and existing updated AGM, build from CERN SY-BI off-the-shelf components ⟦↪5.⟧. The design demonstration takes place in a laboratory environment using artificial signals connected to the DAQ.
The structure of this thesis is divided into four parts. The first part briefly describes and explains the BDS and AG; the second part focuses on the current AGM and introduces a new DAQ solution; the third part presents the related work, which has been done including the development steps; the final part presents real test results and the conclusion, including a discussion of future development.

2 LHC Beam Dump System

The energy, of ≈ 350 MJ, that the beam can reach after acceleration in the LHC, is enough to cause magnets to lose their superconductivity (so-called magnet quench). To remove the beam safely from the accelerator, the LHC is therefore equipped with a BDS, which, when activated, directs the beam towards the energy-absorbing graphite blocks [4].
The system is complex and robust, consisting of dilution kicker magnets and two absorber blocks. It is installed at *Intersection Region 6* (IR6), Fig. 2.1 [1].

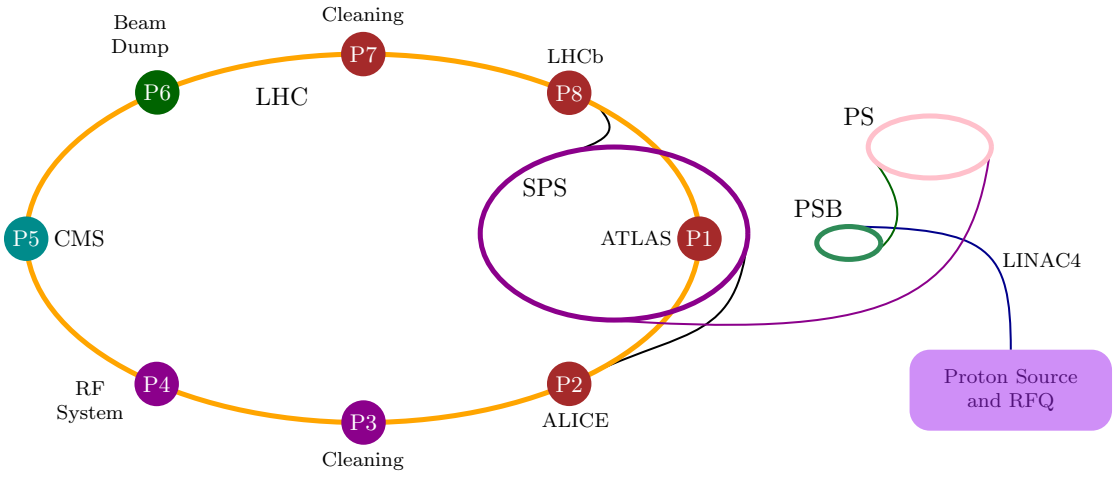

Fig. 2.1: LHC filing accelerator chain and LHC experiments

The simplified topology of the BDS is shown in Fig. 2.2. The black arrows passing through the whole structure in opposite directions represent the trajectories of the circulating beams. The devices of the Beam Dump System are located between magnets Q5 and Q4 on the both sides of IR6. Between these quadrupoles, there are positioned 15 *Horizontally deflecting extraction kicker magnets* (MKD). These are turned on only in case of beam dump. They deflect the beam and

send it towards the 15 *Lambertson septum magnets* (MSD), where it is vertically deflected [5]. Just before the absorbers, the beam is further deflected by a set of *Orthogonally deflecting dilution kicker magnets* (MKB). These spread the beam energy over a larger volume. The beam is finally absorbed by the graphite blocks *Dump Core* (TDE) [1].

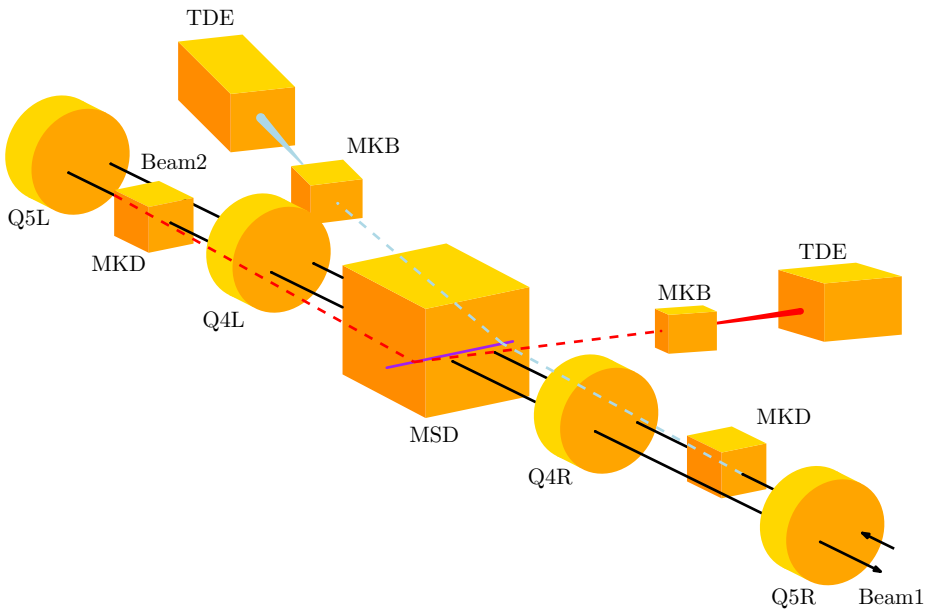

Fig. 2.2: LHC Beam Dump System topology

2.1 LHC Injection and Filling Pattern

The particles in the beam are not uniformly distributed. They are grouped into so-called bunches. Up to 2808 bunches can be injected into the LHC ring. These bunches are separated by 25 ns [6]. In each beam, there must be a gap of 3 μs for the MKD in the BDS [[↩2.]].

The gap is created during the LHC fill. The fill starts in LINAC 4 Fig. 2.1. The particles are accelerated to 160 MeV [7] and continue in the *Proton Synchrotron Booster* (PSB), where they are accelerated further in four parallel rings independently. Then the beam continues to the *Proton Synchrotron* (PS) and the *Super*

Proton Synchrotron (SPS), where it is split and merged. This creates a structure of bunches with defined gaps. This is called a "filling pattern" and it varies according to the machine particle type, protons or heavy ions. However, the BDS Abort Gap is always present in its structure [8]. Finally the beam is injected to the LHC. There it undergoes collisions with the second beam [9].

2.2 Particles in Abort Gap and Beam Dump

The extraction of the beam from the vacuum chamber is performed by the Kicker magnets, which are triggered synchronously with AG. This scenario is shown

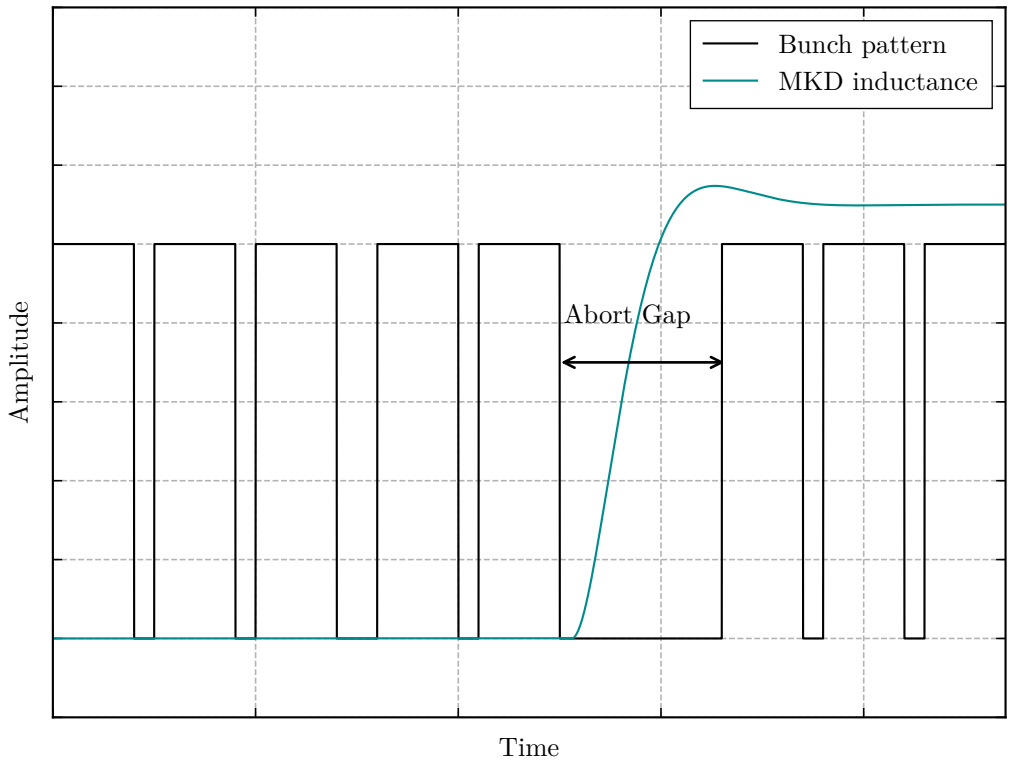

Fig. 2.3: Abort gap in the filling pattern

in Fig. 2.3, emphasizing the part of the filling pattern with AG. The black trace represents bunch envelopes. The 3 μs delay, an AG, is marked by an arrow, and the cyan rising curve depicts the magnetic field inductance. The particles are confined in the beam bunches by the *Radiofrequency* (RF) system. Due to the system imperfections, particles may populate the space outside of the bunches [10]. This populates the AG as well. If the Beam Dump is triggered, it does not deflect the particles in the AG in the required angle to reach the absorber blocks. This causes particles to hit the surrounding structures. This scenario is depicted in Fig. 2.4. The particles populating the AG do not get enough angular displacement to be diverted towards the beam dump (Red trace). If density of the particle population inside the AG exceeds certain levels, it can result in magnet quench [11]. These limits are called population thresholds and vary depending on the beam energy. To detect and estimate the number of particles in the AG, an instrument called AGM is used.

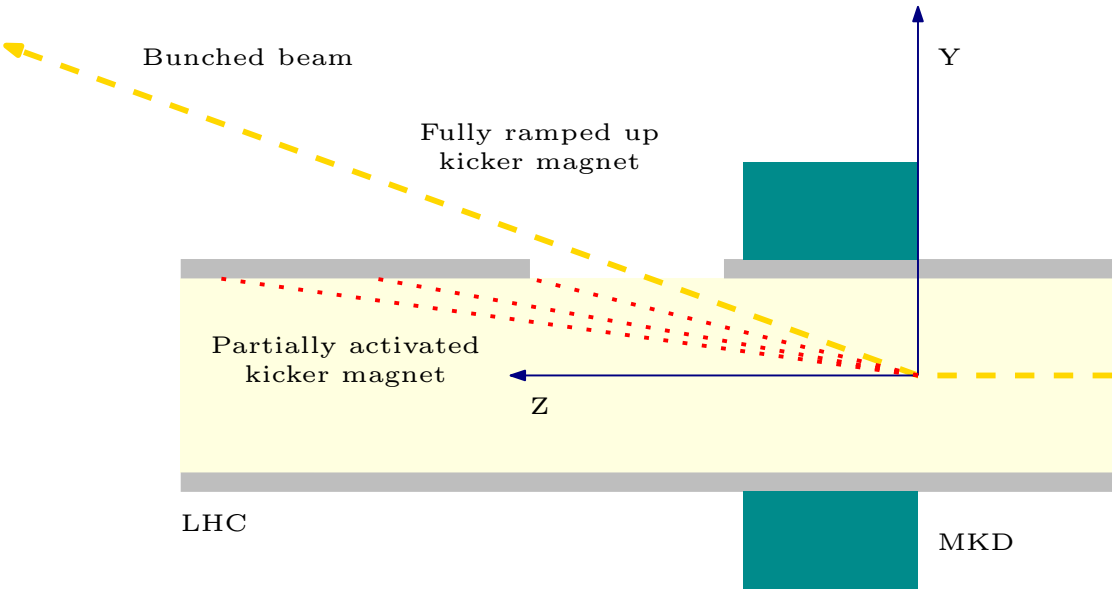

Fig. 2.4: Deflected particles populating the Abort Gap

3 Abort Gap Monitoring

The particle population in the Abort Gap must be measured in the non-invasive manner. In a circular collider, SR can be exploited [12]. When a particle is deflected, SR is emitted along the instantaneous velocity vector [13]. Since the intensity of the radiation is proportional to the beam intensity, it carries the information about the particle population in the beam. Based on this, the AGM exploits the SR emitted by the particles in the AG, to obtain its population. To convert the SR to a population estimate, an electrical signal detector is deployed.

3.1 Detector

Conversion of the SR to electric current is performed by the *Photomultiplier Tube* (PMT). It consists of electron multiplier dynodes, photocathode, and anode. All of the components are confined in the vacuum glass tube. The photons passing through the vacuum tube hit the photocathode generating electrons interacting with electron multiplier dynodes generating the secondary electron emission. The number of electrons is exponentially rising and all of them gather at the output anode [14]. The electrons reaching the anode generate current pulse which is being measured and further processed.
For higher gains, a *Micro Channel Plate Photomultiplier Tube* (MCP-PMT) is used. Its dynode structure is replaced by a microchannel plate having a lot of channels made of continuous dynode structure. The signal is multiplied in each channel in parallel (multiple channels are depicted in Fig. 3.1 with three dots and the Δ symbol represents their short length).
The MCP-PMT current gain can achieve $\approx$ 60 dB. In addition, the microchannel plate is also very thin, so the response of the sensor can be around 180 ps. Its sensitivity relies on the light spectrum impinging the detection area and this varies for each particular MCP-PMT.

3.2 Measurement Method

The aperture for measuring the SR is located at IR4, Fig. 2.1. It is shown in Fig. 3.1. The information about the beam is extracted in the form of SR from

the straight section dipoles. For beams with low energy of 450 GeV the output SR is in infrared spectrum. Because the used detector is sensitive to visible light, the spectrum has to be shifted towards the visible spectrum by an undulator [15]. The extracted signal is guided to the MCP-PMT via an optical line. Currently

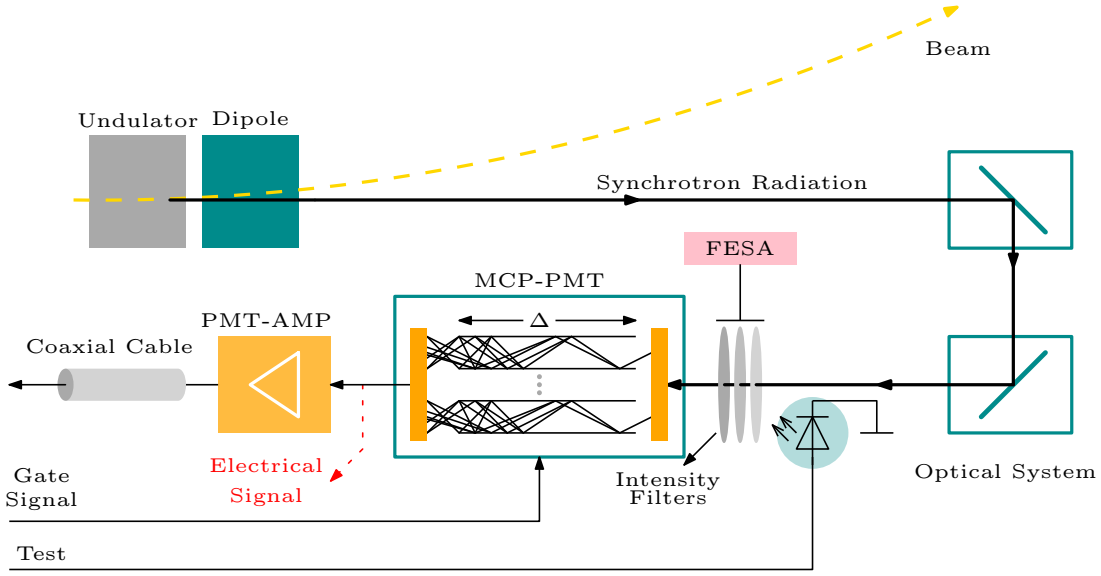

Fig. 3.1: Abort Gap Monitor measurement system

used MCP-PMT is HAMAMATSU R5916U-50 with a rise time $\approx$ 180 ps. According to the MCP-PMT datasheet the sensor has the highest sensitivity around the wavelength of 450 nm. Therefore the SR spectrum coming from the LHC has to be in a range of visible light. It corresponds to blue light [16]. The light intensity is proportional to the number of particles inside the abort gap but it differs with particles energy. This implies, that the light intensity can vary. Therefore an optical density filter has been deployed to attenuate the SR. The filter is selectable by an expert application (*Front-end Software Architecture* (FESA)).
The MCP-PMT generates a preamplified electrical signal ⟦↩3.1.⟧. The signal is further amplified by *Photomultiplier Pre-amplifier* (PMT-AMP), so that it can be transferred through a 100m long cable to the technical gallery.

3.3 Signal Characteristics

The bandwidth of the converted electrical signal is defined by the PMT-AMP. The currently used PMT-AMP is HAMAMATSU C5594 with a gain of 34 dB. According to the datasheet, the bandwidth is approximately 50 kHz-1.5 GHz [17]. The final amplitude is in the range ± 0.5 V. The input signal to the digital acquisition system of the AGM is not required to be broadband because the particle population of the AG does not change so rapidly. The instrument generates one sample per 100 ns. This gives the bandwidth of 10 MHz [18].

3.4 Analog to Digital Conversion

As the intensity of the synchrotron radiation, is proportional to the amount of particles, the particle population is calculated from the transfer function applied to the acquired MCP-PMT signal. To find the transfer function calibration has to be performed. For this can be used the mathematical framework described in [19]. The input effective optical power on the MCP-PMT can be expressed by Eq. 3.1. W_{pmt} is a function of energy and particle population, W_{SL} corresponds to the power of arriving SR on the photocathode, A_{flt} stands for attenuation of the optical neutral density filters and p specifies the number of particles in the abort gap.

$$W_{pmt}(E,p) = \frac{W_{SL}(E)}{A_{flt}(E)} \cdot p \tag{3.1}$$

The photomultiplier is source current, which can be described by Eq. 3.2. It can be seen, that the output does not depend just on the optical input power but also on the polarization voltage of MCP-PMT.
In the following equation, the V stands for the voltage applied to the PMT electrodes and $G_{pmt}(V)$ is the preamplification gain as a function of polarization voltage.

$$I_{pmt}(V,E,p) = \frac{G_{pmt}(V)}{W_{pmt}(E,p)} \cdot p \tag{3.2}$$

The MCP-PMT HAMAMATSU R5916U-50's current gain characteristic is shown in Fig. 3.2, taken from the datasheet [16]. The simplest and reliable approximation of the current gain characteristics is made by fitting the plot with an exponential

curve. Second order polynomial was used to fit the curve.

$$G_{pmt}(V) = G_{pmt0} \cdot 10^{a \cdot V^2 + b \cdot V} \tag{3.3}$$

If a particle is accelerated to the energy of 450 GeV it is considered a low energy particle. This energy can not damage the collider. Therefore it is used for calibra-

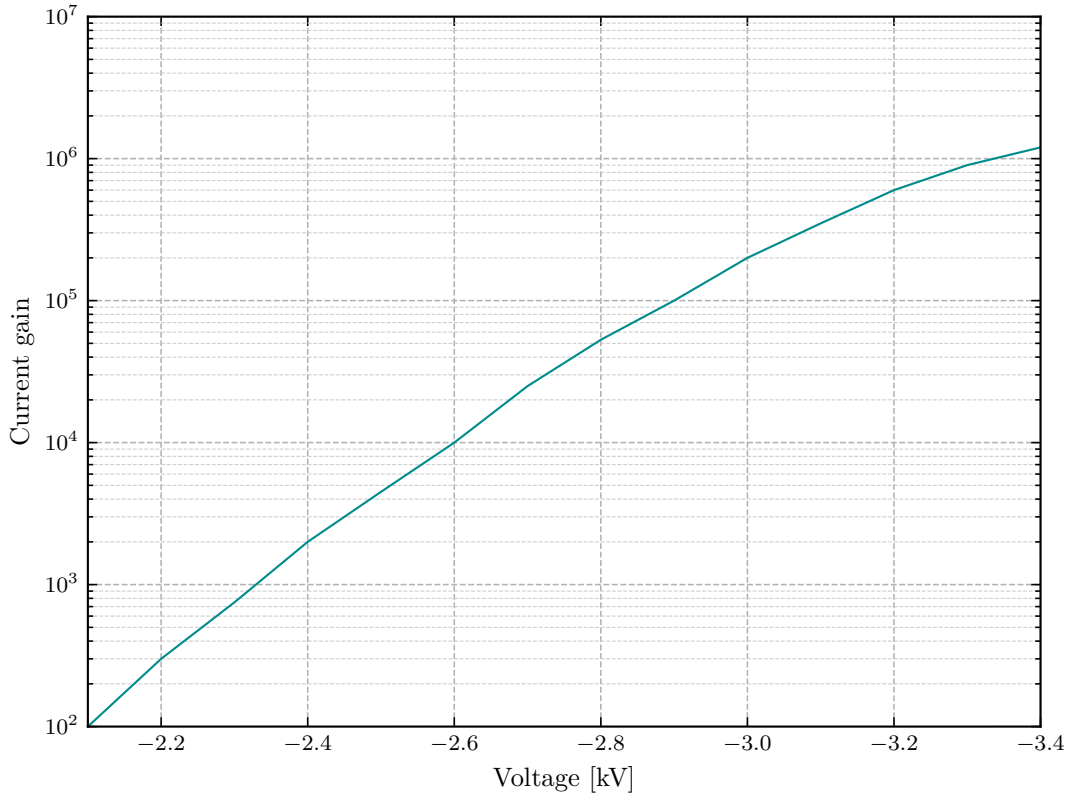

Fig. 3.2: Current gain vs polarization voltage for R5916U-50 [16]

tion. This yields to that all measured values are relative to 450 GeV. The result term $\overline{W}_{SL}$ is then called normalized effective emission.

$$\overline{W}_{SL}(E) = \frac{W_{SL}(E)}{W_{SL}(450\ GeV)} \tag{3.4}$$

During the process of calibration, the beam energy is known and so the $\overline{W}_{SL}$ is the relative value of synchrotron light received from the machine. The gain of the MCP-PMT does not change with the impinging light spectrum, but it varies with the applied high voltage to the electrodes.
The k factor is introduced in Eq. 3.5. By normalizing the k factor to 450 GeV the energy level cancels out in Eq. 3.8.

$$k = \frac{1}{G_{pmt0} \cdot W_{SL}(450\ GeV)} \tag{3.5}$$

Finally Eq. 3.1 can be modified accordingly. The W_{pmt} is expressed using Eq. 3.4 and the gain equation is rewritten using the factor k as follows.

$$W_{SL}(E) = \overline{W}_{SL}(E) \cdot W_{SL}(450\ GeV) \tag{3.6}$$

$$G_{pmt}(V) = \frac{10^{a \cdot V^2 + b \cdot V}}{k \cdot W_{SL}(450\ GeV)} \tag{3.7}$$

The preamplification gain G_{pmt} and W_{pmt} in Eq. 3.1 is substituted by Eq. 3.6 and Eq. 3.7. This yields to desired particle population equation.

$$p_{meas} = k \cdot \frac{A_{flt}(E)}{\overline{W}_{SL}(E)} \cdot \frac{1}{10^{a \cdot V^2 + b \cdot V}} \cdot I_{meas} \tag{3.8}$$

3.5 Finding the Missing Factors

The method of data interpretation is closely tied to the process of calibration. As a first, the approximation of the photomultiplier gain function has to be determined. This is done by sweeping the polarization voltage and measuring the current output, while a constant light is impinging the detection area of the MCP-PMT. A simple LED light can be used to generate the optical stimulus. Once the data is collected, they are transformed to the logarithmic scale and fitted with the second-order polynomial function. The least-square method is used to find the coefficients a, b, c by minimizing the square area defined as a difference between real value L_i and value predicted by a fitting voltage function:

$$\begin{aligned} L_i &= log_{10}(I_{meas\_i}) \\ S &= \sum_i [L_i - (a \cdot V_i^2 + b \cdot V_i + c)]^2 \end{aligned} \tag{3.9}$$

To calculate factor k it is necessary to measure the MCP-PMT current from a known particle population. This is achieved by gating the MCP-PMT over a bunch with known intensity, and by measuring the output signal current I_{meas}. The measurement procedure is performed at 450 GeV, which corresponds to $\overline{W}_{SL\_i} = 1$ referring to 3.4.

$$\overline{W}_{SL\_i} = k \cdot \frac{I_{meas\_i}}{p_{known\_i} \cdot 10^{a \cdot V_i^2 + b \cdot V_i}} \tag{3.10}$$

Using this input condition the Eq. 3.10 can be rewritten to Eq. 3.11, where p_{known_i} is the number of measured particles using the fast beam current transformer [20] and i corresponds to a particular sample i in the gated injection to FLAT-TOP transition as the particle's energy increases (up to 7 TeV) during the acceleration process. The energy growth is linear as the particles are accelerated. therefore the k factor is the same for all the following indices i. The energy of 450 GeV corresponds to the $i = 0$, so the k could be calculated just from the first value in the vectors V, I_{meas} and p_{known} as expressed in the equation Eq. 3.11.

$$k = \frac{p_{known\_0} \cdot 10^{a \cdot V_0^2 + b \cdot V_0}}{I_{meas\_0}} \tag{3.11}$$

Because in the previous procedure the filters $[\![\hookleftarrow 3.2.]\!]$ were omitted, their impact needs to be also taken into account. In case of particles with higher energies the ADC output could get saturated, so a function needs to be determined defining the attenuation of the filters as a function of energy.

$$A_{flt\_i} = \frac{p_{known\_i} \cdot \overline{W}_{SL\_i} \cdot 10^{a \cdot V_i^2 + b \cdot V_i}}{k \cdot I_{meas\_i}} \tag{3.12}$$

The $A_{filt}(E)$ is given by the ratio of expected to measured values. This implies that the p_{known}, $\overline{W}_{SL}$, V and I_{meas} have to be already known. Under normal operation circumstances, the filter function can be approximated from the values measured at the injection (450 GeV) and FLAT-TOP (7 TeV). The values between the measured points are interpolated.

4 Existing Abort Gap Monitor

This chapter focuses on the current system. It describes system functionality, main components, working principle and introduces briefly the LHC synchronization signals. Finally, the system hierarchy is introduced and its limitations derived from the current system design are discussed.

4.1 Synchronization Signals

The synchronization of the instruments in LHC is derived from the RF system clock. The clock synchronizes the RF generators driving the cavities, which accelerate the particles and form them in buckets Fig. 4.1. The set of 10 RF buckets,

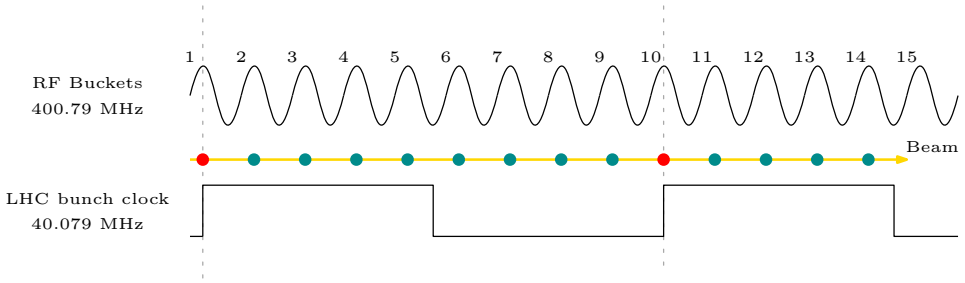

Fig. 4.1: LHC bunch clock scheme

where the first bucket is filled with particles, is referred to as a bunch. As the RF clock is 400.79 MHz the derived bunch clock is 40.079 MHz, Fig. 4.1. The rising edge of the bunch clock indicates the starting position of the particles in one bunch.

The bunches are distributed in the LHC orbit as shown in Fig. 4.2. For each beam the filling pattern might be different [[↩2.1.]]. When a collision occurs, it is necessary to keep track of the colliding bunches. Thus, the second synchronization clocking signal, the turn clock, is deployed. The turn mark determines the first slot in the orbit [21]. The LHC timing is distributed through *Timing, Trigger and Control* (TTC) to several thousand devices at CERN [22].

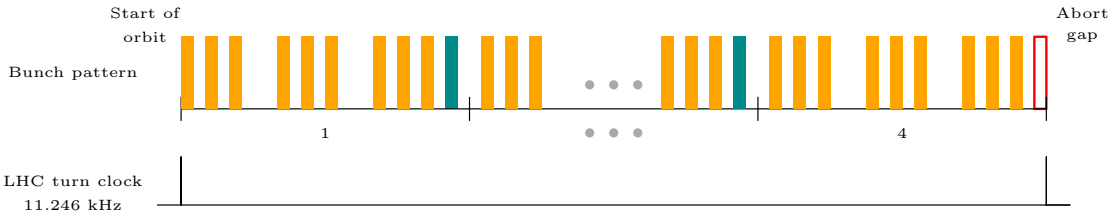

Fig. 4.2: LHC orbit turn clock scheme

4.2 Design Topology and Data Processing

Chapter [[↩3.2.]] describes the electro-optical assembly used to provide the electrical signals from the AGM. The conversion of the optical signal to the electric is done by a MCP-PMT. The MCP-PMT requires gating to enable its operation, and provides wide-bandwidth analog signal. The signal amplitude is proportional to the incoming light [14]. The electro-optical assembly is installed near the beam-

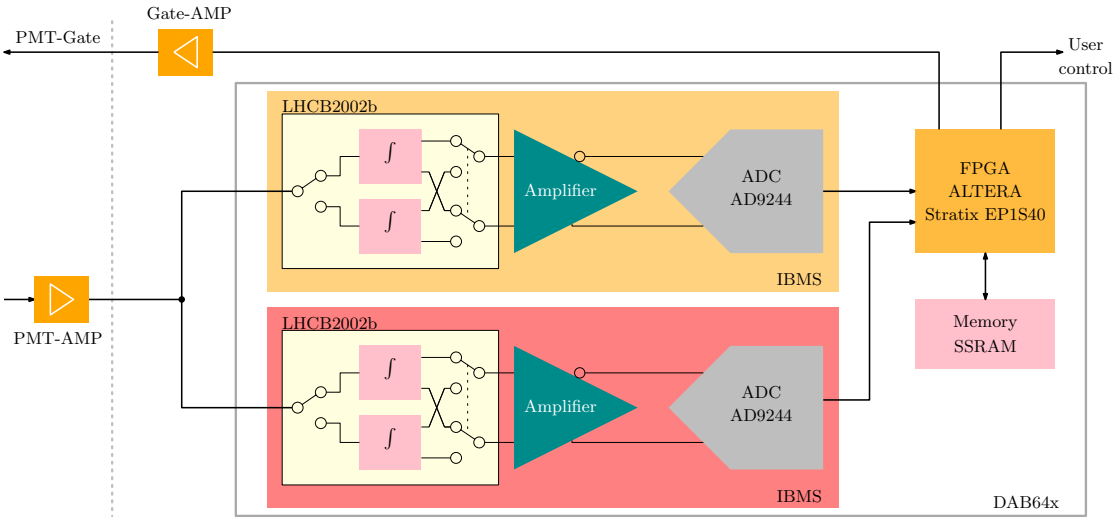

Fig. 4.3: Block diagram of the existing system

line. The gate enable signal and raw data signal need to be carried 100 meters away to a technical gallery. The area is radiation safe, so it is suitable for processing electronics. As the distance to the control unit is very long the signals get attenuated. This needs to be taken into account when choosing the amplifier gains. The trigger voltage range for MCP-PMT gate is from 10 V to 20 V [16]. The signal

amplitude provided by the FPGA is 1.8V. A gate driver is needed to amplify the gate signal to the required 10 V. The raw signal comes to the *VME64x Digital*

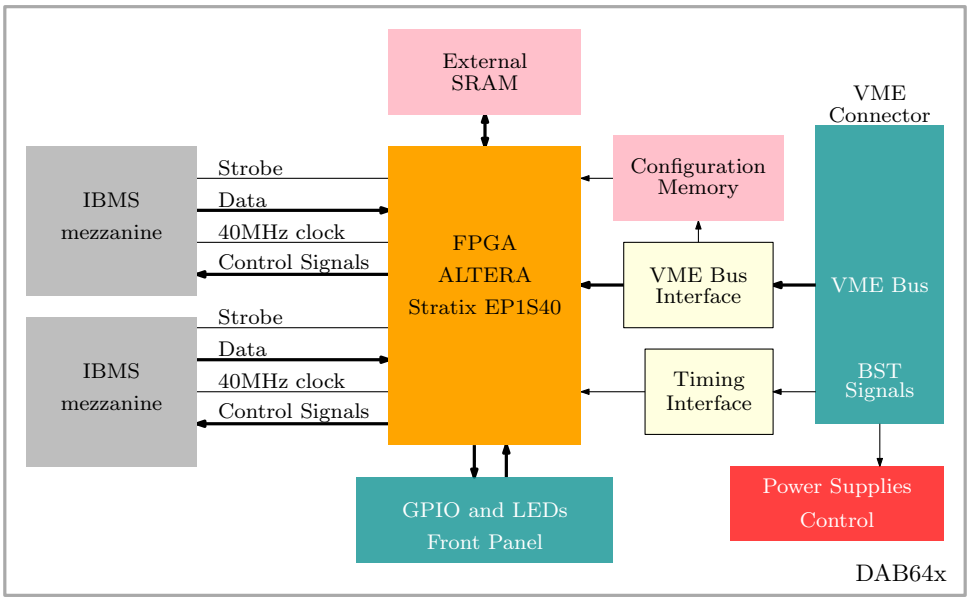

Fig. 4.4: Block diagram of DAB64x

Acquisition Board (DAB64x) depicted in Fig. 4.4. This carrier is commonly used in many applications across the LHC. The DAB64x carrier deploys FPGA Altera Stratix EP1S40. It is equipped with the external SRAM chips (512k x 32bit), industrial VME64x communication bus interface and two *Individual Bunch Measurement System* (IBMS) mezzanines, which sample, integrate, and digitize input signal [23].

4.2.1 Individual Bunch Measurement System

The IBMS deploys *application specific integrated circuit* (ASIC) lhcb2002b developed by the Laboratoire de Physique Corpusculaire, Clermont-Ferrand for the LHCb preshower detector. The ASIC implements 8 integrating channels. Fig. 4.5 shows simplified implementation of one channel, as only one is used on IBMS.
A signal applied to the lhcb2002b channel is first converted from the common mode to the differential mode (MC/MD block). Then it goes in parallel into two analog channel integrators followed by the track and hold blocks. In the final stage

the integrators connect to to a multiplexer.
The reason for this duplex topology is to relax the ASIC timing constraints. The lhcb2002b is running with a 40 MHz reference clock. It switches the two internal integrators according to the 20 MHz clock enable signal. This gives the integrators 25 ns to recover every cycle. One can integrate the incoming signal while the other one outputs the data and resets. During the the switching of the integrators non of them is integrating. This known as a dead time, which individual for each channel. The mean value of the dead time is 4ns [24]. The integrated voltage is sampled in the track and hold circuits before it is multiplexed to the output. The integrated

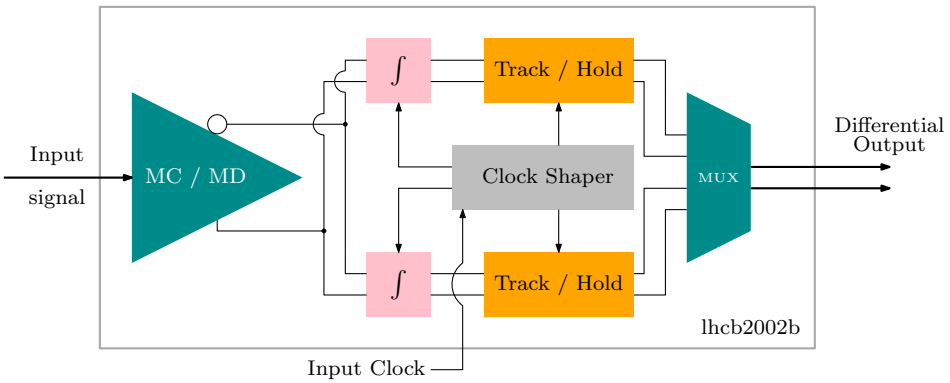

Fig. 4.5: Block diagram of lhcb2002b ASIC

signal from the lhcb2002b is buffered on the IBMS. Follows digital conversion using AD9244, 40 MSPS 14-bit analog to digital converter with the reference voltage of 2 V [25].

4.3 Instrument Functionality and Performance

The AGM system indicates whether the particle population is within certain limits. It exports flags defined by thresholds for particular particle population states. The engineering specification declares the following states: stop cleaning, start cleaning, dump, damage [19]. The thresholds for each state have been specified as percentage of the quench energy limits of Q4 and Q5. The threshold limits used in 2018 are shown in Fig. 4.6.

The existing AGM samples signal from electro-optical assembly in the AG using IBMS. The samples arrive from IBMS as 40 MHz stream of numeric samples. Each sample represents an integral of input analog signal. The integration time is 25 ns, including the dead-time. Every four bunches are summed in FPGA creating 100 ns bins. The acquisition system collects 64 bins, 30 of them covering the AG are exported. These parameters are set according to the technical specification of LHC which requires an instrument to be able detect an electric charge density of 60 protons/ps at 7 TeV and 50% accuracy [3]. The data are further logged and published at 1 Hz rate as the average of 10 last readings.

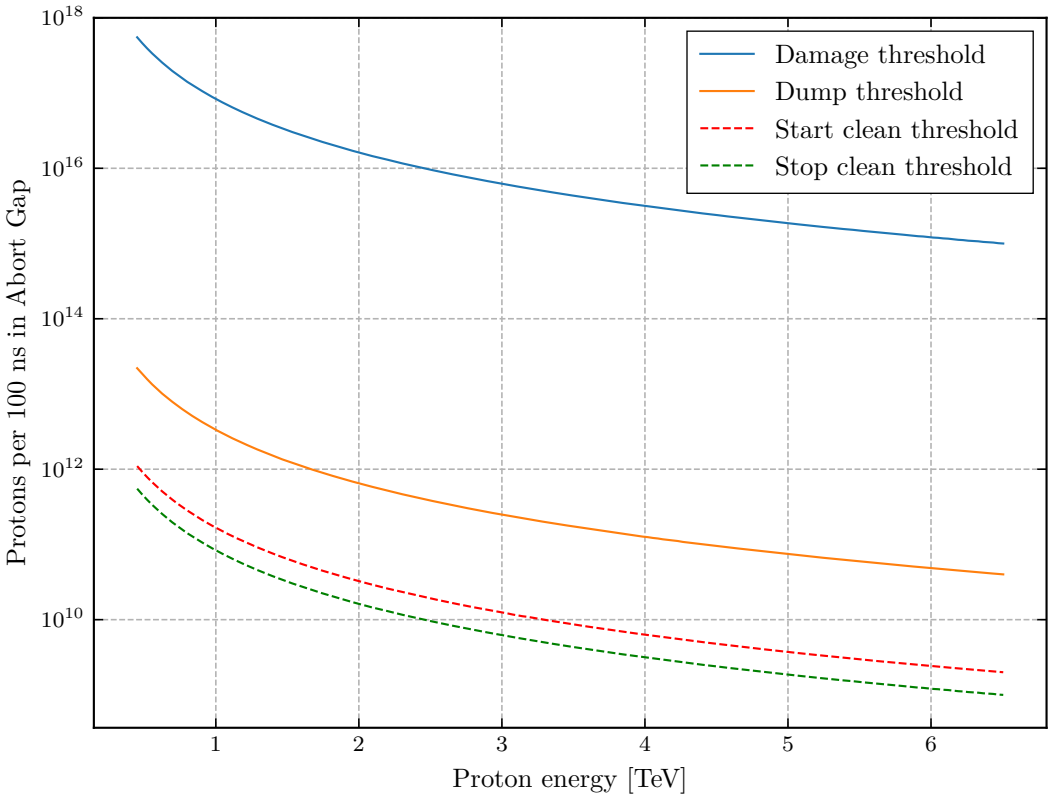

Fig. 4.6: Abort gap thresholds referring to proton energy

The system also defines errors and alarms which are raised in case of events that could lead to the damage of the instrument. The error states are described in the technical documentation for AGM [19].

4.3.1 Device Control and Data Processing

The digitized signal from IBMS is handled by the FPGA of DAB64x. The integrated samples from IBMS arrive with the 40 MHz clock to the FPGA and the acquisition system sums each four received samples. The FPGA has to handle the triggering signal for MCP-PMT gate as well. The gate delay (related to turn

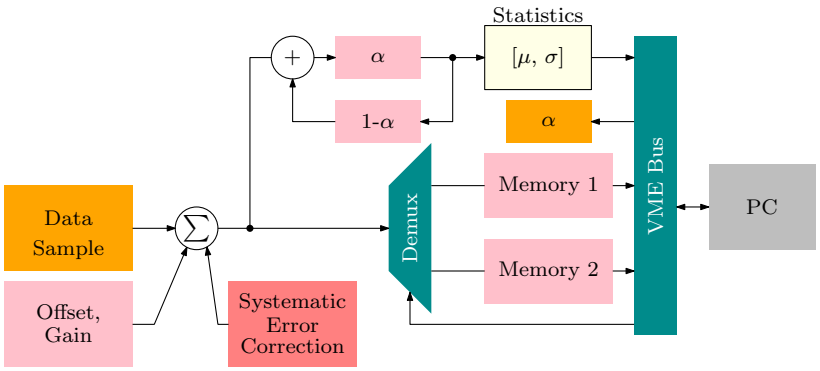

Fig. 4.7: Block scheme of the processing chain

mark) and length is user selectable. The gate delay defines the position of 64 bins long acquisition window. Only 30 bins are exported ⟦↔4.3.⟧. The time resolution of all the settings is 25 ns. Such a degree of freedom is necessary in order to compensate delays on the transmission lines.

When the data arrives in the FPGA, they are equalized by deploying the correction factors obtained from the hardware calibration process. The values might be affected by a systematic error that is balanced with the coefficients taken from the so-called pedestal memory [26].

The corrected samples are saved into cumulative memory. The design shown in Fig. 4.3 implements two multiplexed memories hence when the data is read from one of the memories by upstream software, the incoming data can be still accumulated in the other one. This resolves the reading dead time and ensures

that no data are lost. The design also implements two buffers to store statistical data: mean value and signal deviation. These statistical values are calculated from the filtered data by exponential smoothing filter. The smoothing coefficient is user selectable.

4.4 Issues and Limitations

The current system has drawbacks which make the calibration of the acquisition difficult. Therefore attempts were made to analyze the issues of the current platform. Because of the lack of detailed documentation, the analysis could not be correctly performed, so the long-term experience with the current AGM serves as the analysis result.

The AGM measures both LHC beams. Each beam is measured by DAB64x equipped by two IBMS [[↩4.2.1.]]. Four IBMS equipped with totally 8 slightly different integrators are used to provide the integrated data. The integrators differ by their output offsets, dead times, and gains. The calibration process finds these factors for each integrator. The calibration procedure needs to be re-run whenever the IBMS is replaced. Observed output drifts of acquired integrated values also indicate temperature dependence. An automated script was designed to calibrate the integrators factors and thus minimize the errors of the measurements [26].

The last concern with the current system is the obsolescence of used components. The lhcb2002b is not produced anymore. The deployed memories and the FPGA Intel Stratix are obsoleted.

5 New Abort Gap Monitor

The motivation to create a new Abort Gap Monitor is initiated by the problems associated with the analog integrators in lhcb2002b. These cause measurements errors and make the AGM difficult to calibrate [[↩4.4.]]. The AGM topology was modified and new components were added [[↪5.1.3.]]. The system was installed in the LHC and waits for the implementation of the new acquisition system, that will provide the required AGM functionality. The new DAQ will considerably reduce problem of dead-time and variation of offset and gain. In addition the versatility of the system improves.

Following sections focus on development and theoretical verification of the new DAQ and its laboratory test. A brief introduction to the AGM topology and description of its hardware is included. The simulation and laboratory test results are presented in the summary.

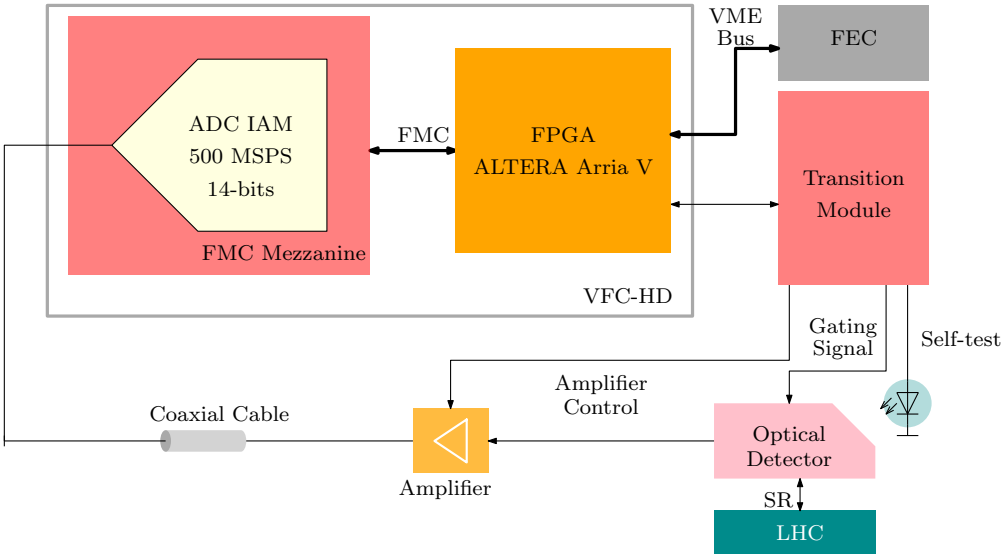

Fig. 5.1: The new AGM system topology

5.1 Existing Hardware and Topology

The new AGM is based on an improved control platform. This requires changing the AGM topology adding two new components: amplifier and *Rear Transition Module* (RTM) as shown in Fig. 5.1.
The Transition Module creates a bridge between the DAQ and the individual parts of the AGM and the optical system is unchanged [[↩3.2.]]. The data format obtained from the new DAQ is compatible with the original system. The DAQ sums and filters the data according to user settings and distributes the results via VME bus [27] to *Front-end Controller* (FEC) connected to the CERN technical network.

5.1.1 VFC-HD - Control Platform

The link between the FEC and the AGM is the control platform. It receives commands from the upstream control software to set the data acquisition delay, filtering, amplifier configuration, turns on the built-in LED, requests data, and generates the gate signal. Current AGM deploys the DAB64x as a control platform.

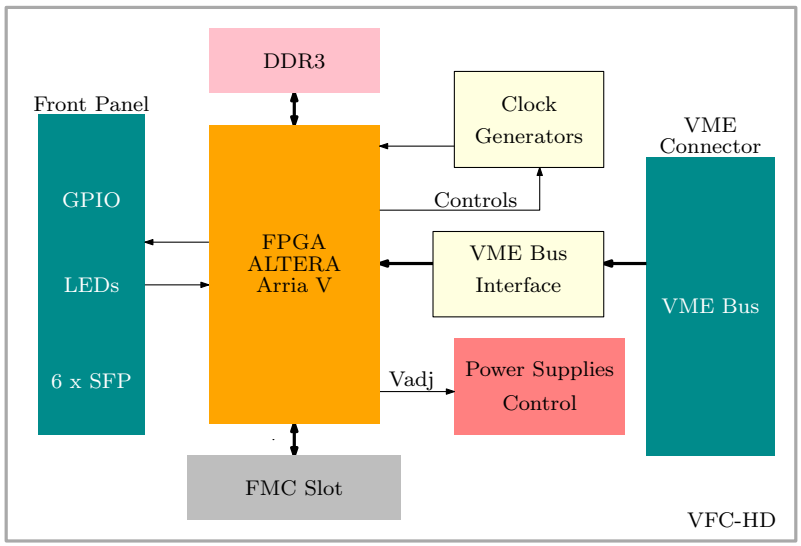

Fig. 5.2: VFC-HD block diagram

The new system replaces DAB64x by VFC-HD, which is used in many CERN SY-BI projects. It is a new standard of CERN BI group, easily accessible and long-term maintained. The VFC-HD is equipped with FPGA Intel Arria V GX, one FMC slot to deploy additional hardware modules, four 6.25 GBit SFPs and two system SFPs providing *Beam Synchronous Timing* (BST)/White Rabbit & Ethernet, 2 x 1GB DDR3 memory, clocking circuits, GPIOs and LEDs [28].
As far as the development of the digital design is concerned, it already has a basic functional design template in place. This includes the system and application part. The system part handles VFC-HD settings, such as adjustable voltage of FMC slot, activation of external PLLs, interrupt vector handling and more. The application part implements the application code.

5.1.2 ADC Modules

Signal integration is done digitally in the new system. The 14-bit 100 MSPS ADC FMC (FmcAdc100M14b4cha - depicted left in Fig. 5.3) module designed by SY-CO CERN was specified in the project requirements. However, during the development it turned out that the module is not compatible with the VFC-HD: DC/DC onboard converters suffer from temperature dependency and some of the digital interconnects use different voltage link levels. As a result, the project

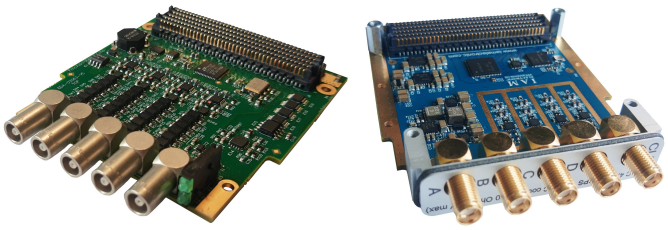

Fig. 5.3: ADC modules for Abort Gap Monitor

specification was modified and the FMC 500 'MSPS 14-bit converter from IAM Electronic with JESD204B data interface was chosen (Fig. 5.3 right). It was deployed in two other projects in CERN BI group already and thus it has now a functional and tested digital module for streaming data.

5.1.3 Additional Components

The topology of the new Abort Gap Monitor was modified with respect to the selected control platform VFC-HD. The VME form factor of the VFC-HD does not allow the usage of bulky connectors. Therefore RTM was designed to provide

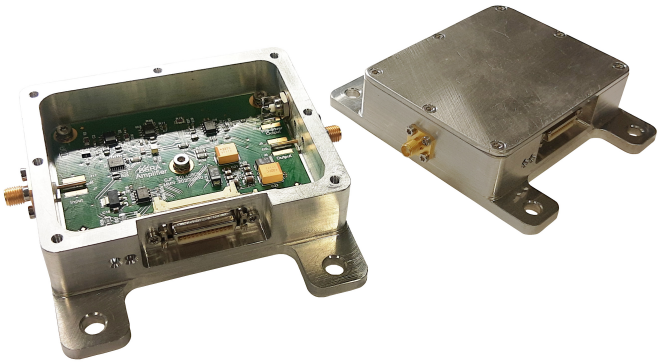

Fig. 5.4: New amplifier

the link between the control part of the DAQ and the rest of the AGM hardware, in particular, the amplifier and the gate driver. The amplifier is placed in the AGM topology between the optical detector and the ADC module Fig. 5.1. It replaces the existing AC coupled HAMAMATSU C5594 by a DC coupled amplifier. The new

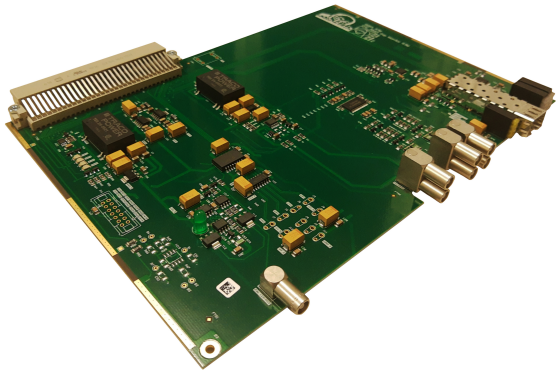

Fig. 5.5: Rear Transition Module

amplifier implements a configurable analog input low pass filter with three different

settings and the gain by 10 dB. The second platform that has been added to the topology is the Transition Module. The second platform is the RTM generating the signals to control the amplifier and implements the gate driver. The gate driver provides a compatible 15 V signal to drive the gate of MCP-PMT. Another functionality of the RTM is to provide a current source to drive the calibration LED.

5.2 New Digital Acquisition System

5.2.1 Conceptual Design

The goal of the new acquisition system is to completely digitize the AGM signal processing. The proposed system performs digital integration of the incoming ADC samples, filters the signal according to the specified settings and stores the results in memory. The results are stored in the same format as the original system. The system outputs 64 filtered bins of cumulative samples over 100 ns. The output can be read out through the software running on FEC, which recalculates the raw data to number of particles using predetermined constants. The constants are obtained by calibration.

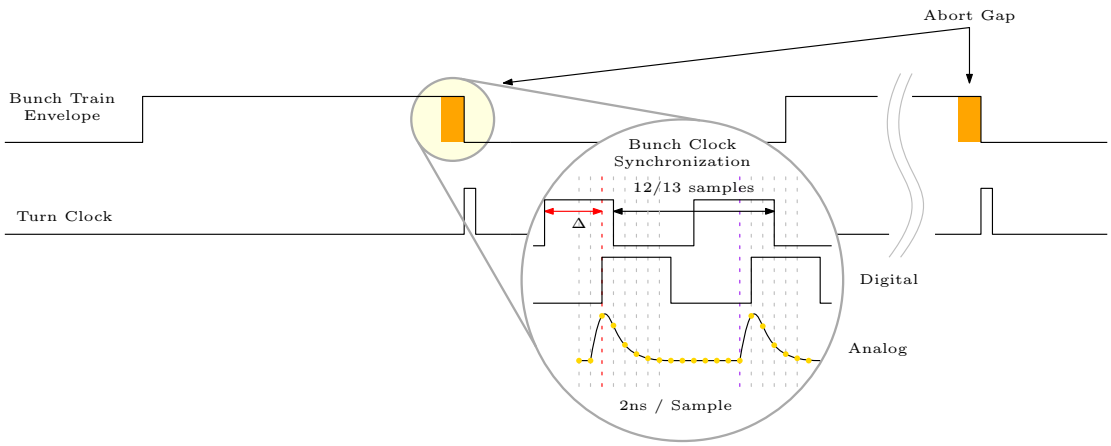

Fig. 5.6: Bunch clock time shift

The DAQ must provide adjustable delays for transmission lines delay compensation and measurement synchronization control. As the MCP-PMT can be used with

only 1% duty cycle the minimum delay between two measurements has to be ≈ 300 μs taken into account acquisition gate window 3 μs. The acquisition period is configured by turn clock delay, which instructs the DAQ to trigger the acquisition every Nth turn. To start the data measurement cycle the MCP-PMT gate has to be activated. The active gate region is defined by its acquisition start and bunch clock delay, related to turn start.
The digitally synchronized bunch clock can get out of phase relative to the gated analog bunches. This scenario is depicted in Fig. 5.6. The delay is caused by in-equal lengths of the transmission lines between the bunch clock source and various locations in the LHC. This phenomena also changes dynamically when accelerating the beam.
An additional requirement to implement is the calibration pulse LED generator and MCP-PMT gate generator. The new acquisition system design requirements are summarized in the following list:

- Adjustable delay on bunch and turn clock with bunch clock resolution
- Fine delay of the bunch clock with the resolution of 2 ns
- Exponential smoothing filter
- One bin representing a sum of 4 bunch integrals (100 ns)
- 64 measured bins to cover the interval of 6.4 μs acquisition
- Provide calibration delays and pulse width to control MCP-PMT gate and calibration LED

The DAQ is split into the ADC data management, synchronization, and the system control part.

5.2.1.1 System Controls and Read Out

The DAQ settings will be configured from the FEC. This will set the parameters of the delays, set the filtering factor, LED / gate delay and pulse width, and configure amplifier. It will also request and read out the data. This will be performed via the VME bus. The connection between VME bus and digital design is carried out

by the Wishbone interface [29] and a system part in the VFC-HD digital design development template. This maps Wishbone registers to the VME.
The structure of the Wishbone interface is created from single Wishbone interfaces for each digital block requiring the VME control. These interfaces are connected to one main Wishbone interface in the VFC-HD system part connected through a Wishbone crossbar.

5.2.1.2 Data Management and Synchronization

Raw ADC sample blocks of 256 bits enter the system synchronously with a 125 MHz link clock. These blocks contain data for four channels in 64-bit frames and each frame carries four 16-bit samples. As the ADC is 14-bit, the values are left shifted in the 16-bit words, so the lowest two bits remain empty.
To synchronize this data stream with the LHC bunch clock and turn clock, a tagging method needs to be deployed. The empty bits in words can be exploited to store them. For the stream synchronization purpose, a component from CERN SY-BI BST Provider in combination with BST Sync is used. The BST Provider is a digital block that is the source of the bunch clock and turn clock. It can extract timing from the BST optical line or an external source. It features also the LHC timing emulation. Its settings are possible to activate via Wishbone interface as depicted in Fig. 5.7. The initial time domain of the BST Provider is 160 MHz. To

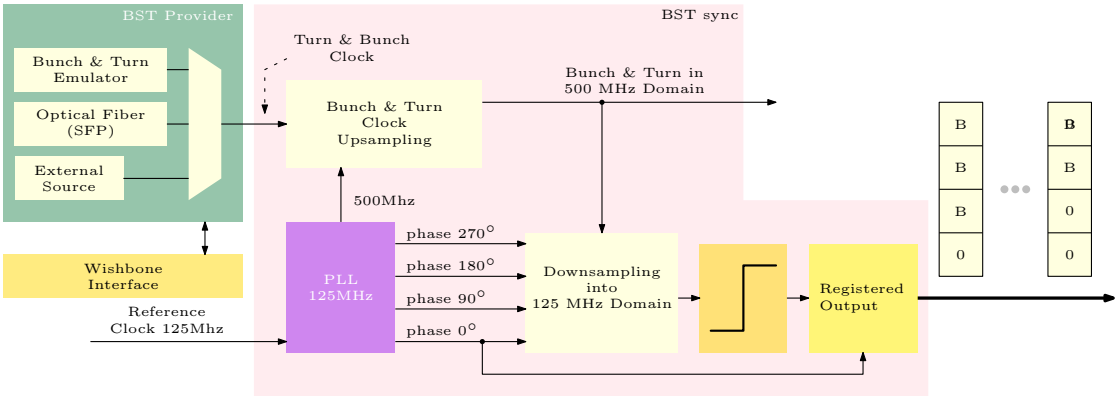

Fig. 5.7: BST synchronizer Simplified diagram

convert it to 500 MHz domain and 125 MHz domain, you need to use BST Sync. It resamples the 160 MHz signal to 500 MHz. This is sent to the output of the

BST sync and to the downsampling block. The downsampling block resamples the 500 MHz signal with 125 MHz clock signal for four different phase shifts (0°, 90°, 180°, 270°). These are synchronized with an edge detector and gated with 0° phase shift 125 MHz clock. This determines the phase shift of the bunch and turn clock in the vector of 4 values. The time intervals between the values match the intervals of the samples in the ADC frames. The tag to the ADC stream is inserted at the sample position in a frame, where the phase vector changes. The tagged stream carries now the information about LHC timing and further processing can performed.

Fig. 5.8 depicts the data management used to calculate the 64 output bins. The data is supplied by an ADC block stream containing data for all the channels. They continue to the preprocessor, block mediating the tagging. It receives the BST stream of tags, shown in orange, and inserts them in the data stream. The vector example shown in Fig. 5.8 of two zeros and two phase flags will be interpreted as a vector of zeros with logic one at the first bit indexed from zero. This holds also for the turn clock, if it is present. The turn clock and bunch clock signals are synchronous, so whenever turn clock arrives the bunch clock is present. The next focus is on the integration procedure. The number of samples reflects

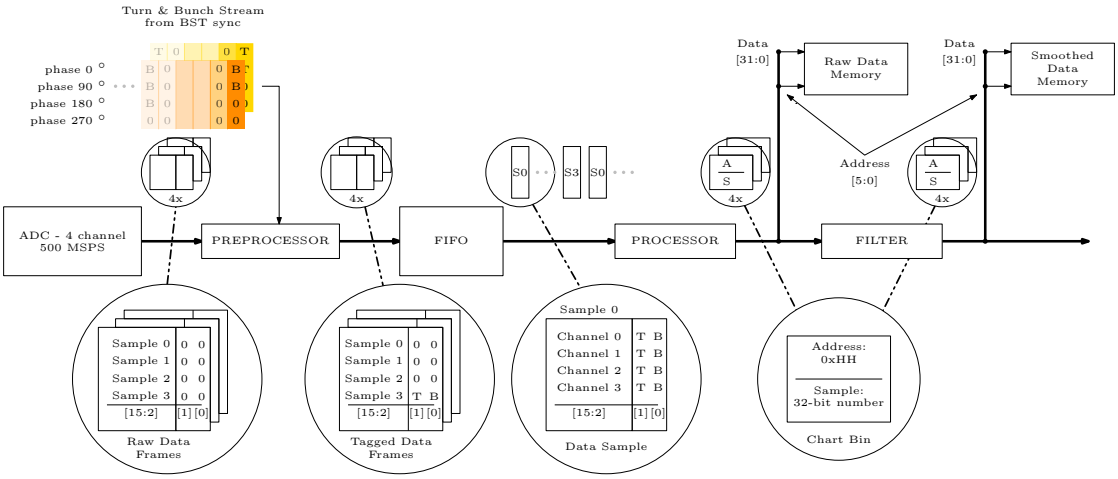

Fig. 5.8: Data flow within the AGM

the number of bunches which need to summed, and is fixed. As the samples are stored in the ADC frames and the tags determine, which sample corresponds to

which bunch in the beam (by utilizing the BST phase vector information), the frames need to be split. This is done by a FIFO with a capacity of six hundred blocks of 256-bit word size. The readout from the FIFO is performed with a lower rate and each word is being split into 64-bit values by multiplexing. The multiplexing reassembles new frames containing the samples measured at the same time for each channel shown in Fig. 5.8. These new frames go to processor, which sums up a number of samples specified by the digital block configuration. This is according to the specification 100 ns (four bunches) intervals and it corresponds to the 50 ADC samples to be summed. The expected result bit width is 22-bits if the summation is performed with 16-bit values. As the 32-bit is a initial size for Wishbone for data collection, the results are aligned to 32-bit values. These results are stored to memory for debugging purposes. Therefore, the processor output values also include the address specifying the position in it.
The last processing block is the filter. It applies exponential smoothing to the incoming signal. Eq. 5.1 describes the weight distribution for the current and previous sample according to the set alpha factor.

$$Y(z) = \alpha X + (1 - \alpha) Y z^{-1} \tag{5.1}$$

This behaves as a low-pass filter and hence smooths the summed bins. As the filtered values are then saved to the memory for the processor, the address is passed on unchanged.

5.2.1.3 System Overview

Based on the requirements and data processing a new design concept was created. This is depicted in Fig. 5.9. It consists of a processing chain (green blocks) running in a 125 MHz domain, structured according to ⟦↩5.2.1.2.⟧. This domain is created by the ADC frame clock. Blocks for MCP-PMT pulse generation and LED circuit are in the 160 MHz domain and Wishbone interface at 125 MHz clock from different a source than ADC frame clock. As the system uses three different clock domains, the data acquisition, generation of the MCP-PMT and data collection has to be synchronized. For reading out system results, the FEC, accessing the design over VME bus, has to send a request first specifying the memory. The DAQ stores data into the memory and replies with the interrupt signal. The data stays

in the memory until a new request is sent and the memory is rewritten. The reading will be performed by the FEC every second, so the interrupt will not be used to trigger the readout.
For the synchronization of the processing chain, gate and LED pulse generator, a dedicated domain synchronizer block is introduced. This block is picking every $N - 1$ turn clock, and sends a synchronization pulse to the FIFO and both LED and Gate generator. This triggers the blocks on the next turn clock rising edge.
The last parts of the conceptual design are the additional raw memory, amplifier configuration outputs, and testing interface. The raw memory is needed to return information about the incoming signal, so that the correct delays can be found during the calibration process. The additional outputs control the amplifier settings and the testing interface is created to connect the signal analyzer or additional processing blocks.

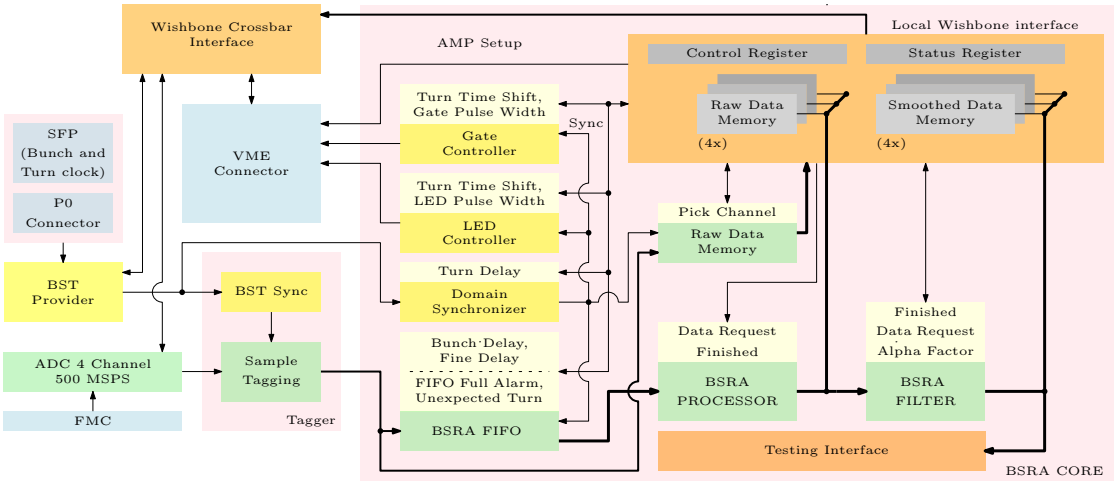

Fig. 5.9: New digital design overview

5.2.2 System Development

As a starting point for the acquisition system development served the VFC-HD template. The template includes a basic design with a Wishbone interface mapped onto the VME bus, so that it can communicate with a FEC.
The template has two parts - system and application. The system part is the management of the board. It has hardcoded VME register addresses for configuration.

So it can be plugged into VME and controlled by the FEC without additional development. The second part of the template is for the application. It is connected to the system and on-board connectors such as FMC or VME P1. Since the new AGM is based on the 500 MSPS ADC used in other projects, a project with an implemented ADC digital block has been used. This reduced the difficulties of re-implementing the ADC.

5.2.2.1 Processing Chain Implementation

The processing chain is designed as a connection of three blocks. It reads tagged data from the input, processes them according to the requirements, and stores them in the output memory. It consists of FIFO, Processor and Filter. All these blocks process data for all four ADC channels.
The starting block is the FIFO. This expects tagged data according to the concept. Its purpose is to find the start of acquisition and store a defined amount of ADC data blocks. These are sent sample by sample to the processor. The FIFO has three more features. It resolves the shift between real bunches and the distributed bunch clock. It stores the particular number of ADC blocks and adds an extra flag defining the start of summation.
The block is implemented as an Intel IP core FIFO, *Finite State Machine* (FSM), output multiplexer, and delay lines. The input and output width of the IP core is 256-bits controlled by an FSM with three states. The FSM cycle starts waiting for a synchronization pulse. When it arrives it waits for the next turn tag in the stream and then it switches to the next state. There it counts the number of bunches passed. If the bunch delay is not set it starts storing ADC blocks directly. The number of stored data is parametric. This can be set before design compilation. The current configuration is 400 bunches. This value has been selected as an optimal value to create 64 bins (256 bunches) in the processor block. When the data is stored the state machine returns to the state, where it waits for the next synchronization pulse.
Another purpose of the FIFO is the insertion of an extra tag to the stream to mark the first value to be summed. The tag is placed on the second LSB in the ADC samples. This implies, that the turn tag marks the summation start. When a bunch delay is configured the turn tag is not present in the output stream.

Therefore it has to be added. As the bunch and turn tag are synchronous the FIFO copies the bunch tag to the turn tag position.
At the output of the IP core the data is read out as 256-bit blocks. The blocks are split along the ADC samples in frames for all the channels. Each concurrent 64-bit sample block is connected to the input of the multiplexer. Once the first data are stored in FIFO the 2-bit counter switches the multiplexer inputs and the data from FIFO are sent out. The compensation for the bunch clock out of phase with gated signal is also placed at the FIFO output. It is implemented as two 16-bit shift registers for bunch and turn tags. By setting the fine delay input it takes the delayed tags and place it to the output samples. The 16-bit shift register is sufficient as the maximum phase shift can reach value of 13 samples.
The FIFO also equippes two alarm signals. First the FIFO full alarm indicating the overflow of the FIFO IP core and unexpected turn signalizes violation of the turn synchronization – the turn clock arrived during data storage.
The next block in the processing is the processor. It contains four parallel 32-bit Intel IP core adders, the sign extension circuit, FSM with two states and address counter. The processor waits for a synchronization tag in the stream. It triggers the summation when it arrives and it sums up periodically every sample until Nth bunch tag. New data are distributed at the output every $\approx$ 400ns. When the 64 bins are calculated the block sets the signal valid high for one clock cycle used as an IRQ.
The processor is connected to an additional block memory, where it stores the results. It controls the write enable signal based on the external requests. The block receives a request for data. It waits until the current processing cycle is finished and waits for the new synchronization tag. When it arrives, it enables the memory enable and all the data is stored to the memory. After calculating 64 bins. It raises the IRQ and the data can be fetched. The block also includes an error flag when the cycle of 64 bins could not be finished. To identify this scenario it takes the FIFO empty signal from FIFO block. If the signal is valid, and the calculation of 64 bins has not been finished yet, the processor raises an error.
The processing chain is terminated by a filter. It consists of 64 multiplexed filters using the Eq. 5.1. Each of them filters one of the bins. Fig. 5.10 depicts the multiplexing of the values based on the address. For the filter implementation, the Altera Multiply Adder IP core with the two pairs of 32-bit inputs and one

65-bit output was used. The first pair calculates the first term in Eq. 5.1. The second pair corresponds to the second term. It is connected to $(1 - \alpha)$ factor and a multiplexer. The multiplexer inputs are connected to a 64x32-bits array holding the previous results. These are then picked by the address value arriving with data.

The data storage function is implemented in the same manner as for the processor. An external request is received and the filter waits for the next value with zero address. After that, it activates the write enable signal and all the next 64 samples are stored. Then it raises the IRQ to indicate the end of the cycle.

The filter experienced a timing error, because the original design calculated the results in one cycle. As the block receives data with the $\approx$ 2.5 MHz rate, an additional parametric delay was added. Then the input paths were set as clock multi-cycle which relaxed the timing.

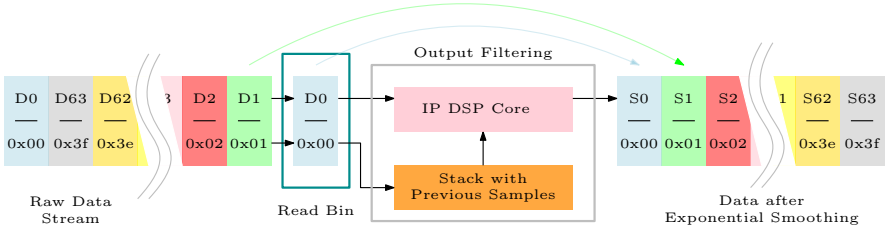

Fig. 5.10: Output data filtering block

5.2.2.2 Stream Data Selection

The processing chain works with different formats of data. It receives data chucks from the ADC, it stores them in the FIFO and then it processes them. Fig. 5.11 shows how the data is picked from the stream in case of one bunch summation.

The ADC data arrives as tagged blocks. If the FIFO detects a bunch tag in the block the data is stored. Then it stores each block until it finds the next bunch tag. The last block with the tag must be stored too, because the FIFO does not keep track of the bunch tag positions, therefore tag can be on one of four samples in the block frame. The tagged samples in the ADC block are depicted in Fig. 5.11 with orange color. When the data arrives at the processor it starts the bunch

summation from the sample containing the bunch tag and keeps summing until the next tag. The next tag is not included in the sum.

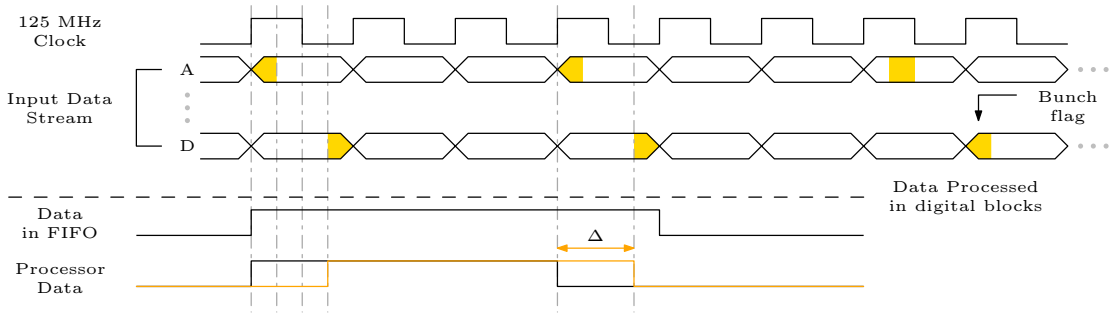

Fig. 5.11: Stream data selection

5.2.2.3 Data Interpretation

The values interpretation and sizes vary within the processing chain, which is shown in Fig. 5.12. The data arrives in 16-bit samples with 14-bit left-aligned values. The two lowest bits are filled in the processor with the BST tags. This data is then passed through the FIFO into the processor. There the value is extended to 32-bits. In Fig. 5.12 the bit size of the value size after summation

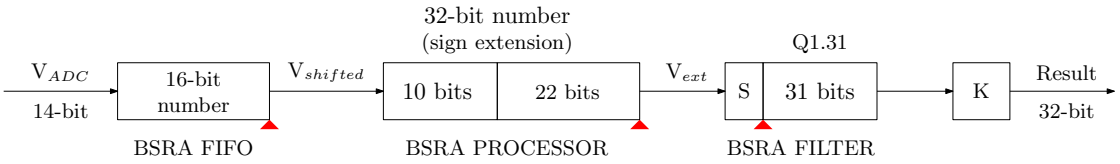

Fig. 5.12: Data conversions within processing chain

increases up to 22 bits is shown. For the current configuration, where 100 ns segments are integrated, the value size never exceeds 32-bits and never overflows. The data is received by the filter. There they are interpreted as fixed point values Q1.31. The input values are thus divided by the constant $K = 2^{31}$. To recover the correct magnitude of the output they have to be multiplied by the constant K.

5.2.2.4 System Configuration

The DAQ waveforms for the current configuration are shown in Fig. 5.13. All signals are in the 160 MHz domain. Every acquisition cycle starts with waiting for 3rd turn clock. When it arrives, the domain synchronizer generates one pulse. All synchronized blocks (LED and Gate generator and FIFO) are notified, that the acquisition starts at the next turn clock. When the turn clock is received, the blocks are enabled. The FIFO counts the delay in bunches and then it starts the acquisition. In parallel the gate signal is generated. The generator delay is realized by delaying the turn clock as depicted in Fig. 5.13. This triggers the block able to generate certain pulse width. The generator block deploys SY-BI group blocks. For finding the settings of bunch delay (FIFO) and gate delay (Gate generator) the calibration needs to be performed.

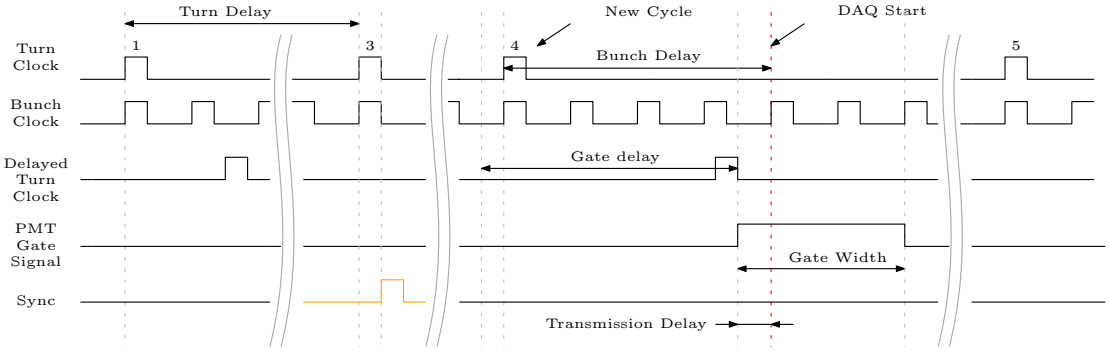

Fig. 5.13: The System waveforms in 160 MHz domain

5.2.2.5 Verification Concept

Verification of the design will be performed in SystemVerilog with either SVA or randomized testbenches. This will be decided in the context of complexity of the component. The basic testing method will send data to the inputs of the *Device Under Test* (DUT) and compare its outputs with outputs from the DUT model. The Verification is split in two parts. The first creates tests for processing chain and the second part embeds the complete design in the CERN SY-BI testbench environment to test the overall functionality of the design and plot the results.
The test methodology of the processing chain is based on sending transactions to

the testbench and receiving notifications and errors from the process. These transactions are packed data equipped with set of methods and variables. As different blocks in the processing chain have different input / output data formats, these methods can imitate them. For example, one method can create tagged columns in the same format as the output of the FIFO. This simplifies the driver functions, where the functions to interpret the data are not necessary. The transaction consists of randomized ADC 16-bits values with the two lowest bits always empty, four 32-bits number packed with address representing the adder and filter outputs and 4-bit vectors for turn and bunch tags. The methods then modify and combine these variables to determine their return values. To be able to use the transaction test approach a unified testbench environment was created. It consists of Packet Generator, Clock Generator, Checker, Driver and Monitor Functions.

The Packet Generator is an object providing the stream of transactions. The

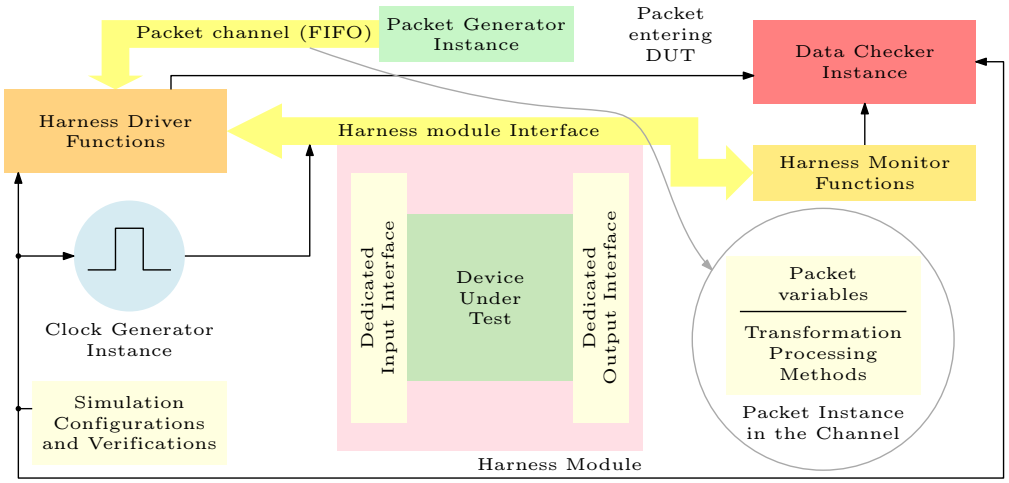

Fig. 5.14: General testbench topology

interconnection of the generator and the testbench is provided by the queue. This acts as FIFO. The generator fills the queue with randomized transactions at the start of the verification process. These are then read out by the DUT with its own speed. The generator has two modes - Randomized or static value generation. In the randomized mode, it randomizes all the transaction variables and generates the bunch and turn tags. This is performed as a loop of 5625 cycles shifting a 4-bit vector to the right. The 4-bit vector starts with value 1 at the MSB. It is shifted

every second cycle. When the vector is zero, it waits for another two cycles before it resets again. In case of the static number generation mode, all the variables in each transaction are prefilled with static value. The next testbench instance is the Harness Module. This connects the DUT with the testbench. It merges the DUT inputs and outputs including extra signal for synchronization into one interface.
To verify the outputs of the DUT the Checker instance is created. It measures the inputs / outputs and calculates the expected results. These are stored in the internal queue and compared with the measured inputs. The object equips a task "body", which triggers the continuous process of comparison. It is implemented as two queues with the measured and expected data read out in the infinite loop. It uses the transaction method "compare" for content verification. Therefore the data is formatted as a transaction instance before they are loaded into the queue.
The clock signal generator usually resides inside the Harness Module. However, it was placed in the main testbench module to simplify the control of the instance. Therefore it is connected to the interface of the Harness Module. The clock generator features a randomized start delay, reset and can create a derived clock from a parent object.
The last testbench instances shown in Fig. 5.14 are the Driver and Monitor functions. The Driver reads transactions from the generator queue, formats the data depending on the connected DUT and sends them to the checker and to the Harness Module. The Monitor serves as feedback. It measures the output of the DUT and calls the appropriate checker function to store the data in the checker internal queue. When the input and output data is stored in the checker, the expected values are calculated from the DUT model and compared.
The whole testbench works as follows. The packet generator outputs predefined number of data and stores them in the queue. They are read out by the driver function. This is connected to the Harness Module through its dedicated interface and to the checker. The data propagates from the driver to the DUT and checker and then the outputs return through the Harness Module to the monitor function. There the function registers the data and calls the method of checker to store the data in the form of the transaction. The checker "body" runs in the background. When the measured data is received, the expected values are already calculated from driver data. It compares them and if the data is correct the process continues with the next cycle. In case of failure, an error is raised.

5.2.3 Laboratory Test

Fig. 5.15 depicts the laboratory setup diagram and Fig. 5.16 depicts the real laboratory setup. The DAQ is installed on the VFC-HD in the laboratory rack. This

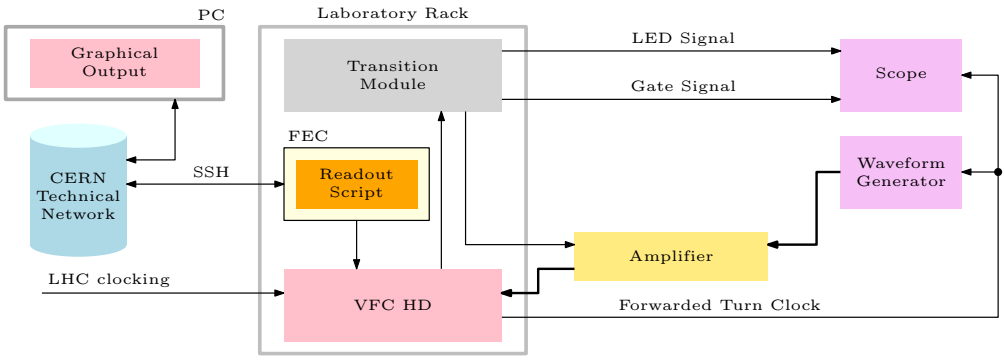

Fig. 5.15: Testing setup diagram

is connected via VME bus to the FEC with access to the CERN technical network. There it can be controlled via SSH. To show the plots on the user PC, the FEC graphical interface has to be forwarded via SSH. The functionality was

Fig. 5.16: Laboratory setup

tested using an oscilloscope and a waveform generator. Both laboratory devices were synchronized with the turn clock.

To test the design of the acquisition system a Python script was created. This script configures, requests, and reads data from the instrument. These are then plotted in the graphs. The device must be first registered in the CERN driver database to be able to load the instrument memory map to specific storage on the FEC. This memory map is generated by the CERN automation scripts. When the script is launched, it identifies the set of parameters passed as arguments. Then it activates the power on a FMC connector and it programs the ADC over SPI. The ADC is set to continuous mode. The script creates a separate thread to run a window with plots and sends a request for new data to be fetched. It waits for one second and reads the raw and filtered bin memories including the memory with raw samples. These values are stored into the queue, new requests are sent and the cycle repeats. In parallel to that, the data is taken from the queue, interpreted according to the ⟦↩5.15.⟧ and plotted using pyqtgraph. The test was

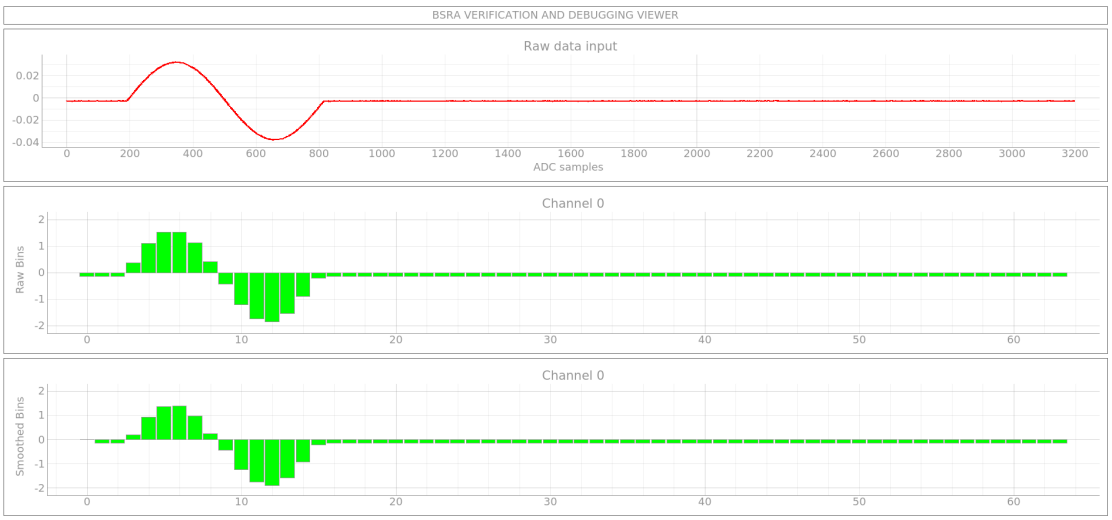

Fig. 5.17: Acquisition system debugging script output

performed by generating one sinusoidal period of 1.2 μs burst with an amplitude of $\pm$ 30 mV. The signal was passed through the amplifier with 0 dB gain. This is depicted in Fig. 5.17. The integrated amplitude is $\approx$ 1.5V (the values are shifted because of internal ADC offset). This is the expected value, because the processor integrates 50 samples per bin (corresponding to 100 ns segments). The graph with the filter output shows the same pattern as the summation. Its filtering ability

was tested manually. The alpha factor was set to 0.0008, which slowed down the output responce to the input signal changes.

5.3 Summary

The new AGM acquisition system has been successfully developed and tested. The analog integration, used in the current AGM, has been replaced by the digital integration. The system returns 64 bins of 100 ns filtered integrated segments as required. The processing chain was tested by a randomized testbench. Each of the digital blocks of the processing chain was tested separately. The chosen methodology allowed to combine the theoretical models and verify the partial functionality of the processing chain. To verify the theoretical functionality of the complete

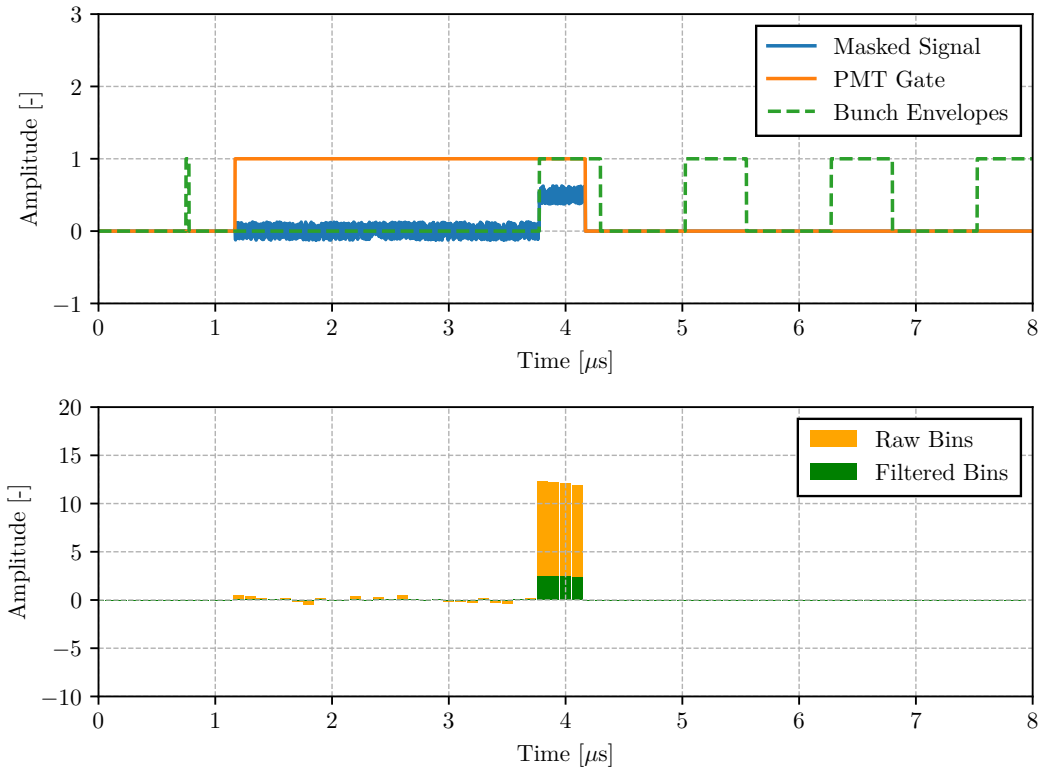

Fig. 5.18: Wrong synchronization of the AG

design of AGM the simulation of wrong and correct gate synchronization was performed as depicted in Fig. 5.18 and Fig. 5.19.
To test the complete design with all the synchronization blocks and Wishbone, the CERN BI testbench environment was used. It embeds the BST, ADC instances, Wishbone interface and it emulates all the necessary clock domains present on the VFC-HD platform. The environment had to be modified to simulate the AGM

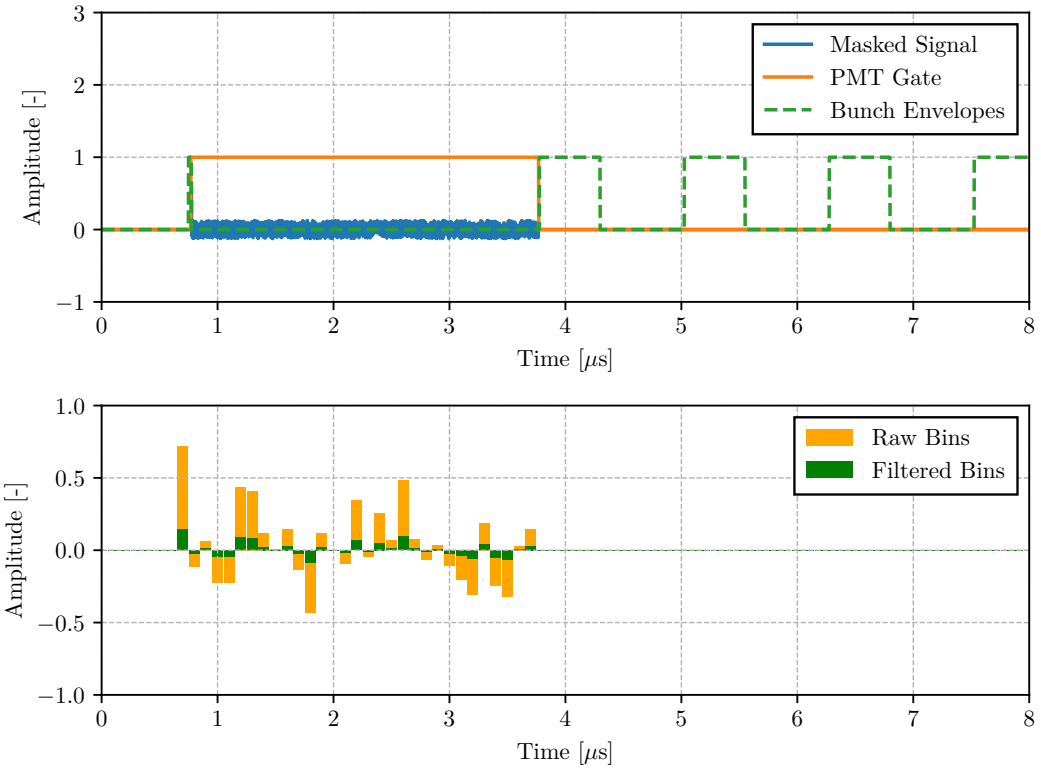

Fig. 5.19: Correct synchronization of AG

features. Therefore an extra generator and artificial bunch pattern were created in the 160 MHz domain. This is connected to the ADC, where the signal is gated with 500 MSPS and the 14-bit amplitude is selected according to the testbench configuration. The value is left-aligned and packed in the four sample vectors. These vectors are sent to the processing chain. As in the real system is the ADC signal masked by the MCP-PMT signal, the signal is also masked in the testbench,

before it arrives at the ADC instance.
The particles in AG were simulated as white noise with the magnitude of 3 dB added to the generated ADC samples. The first Fig. 5.18 shows the wrong synchronization of the AG. The gate signal of 3 μs overlaps with the bunch envelopes in the beam. This can be seen in the resulting graph of 64 bins. The last bins have higher values than the integrated noise. The correct synchronization with AG is shown in Fig. 5.19. The gate signal selects exactly the area of the AG. the upper

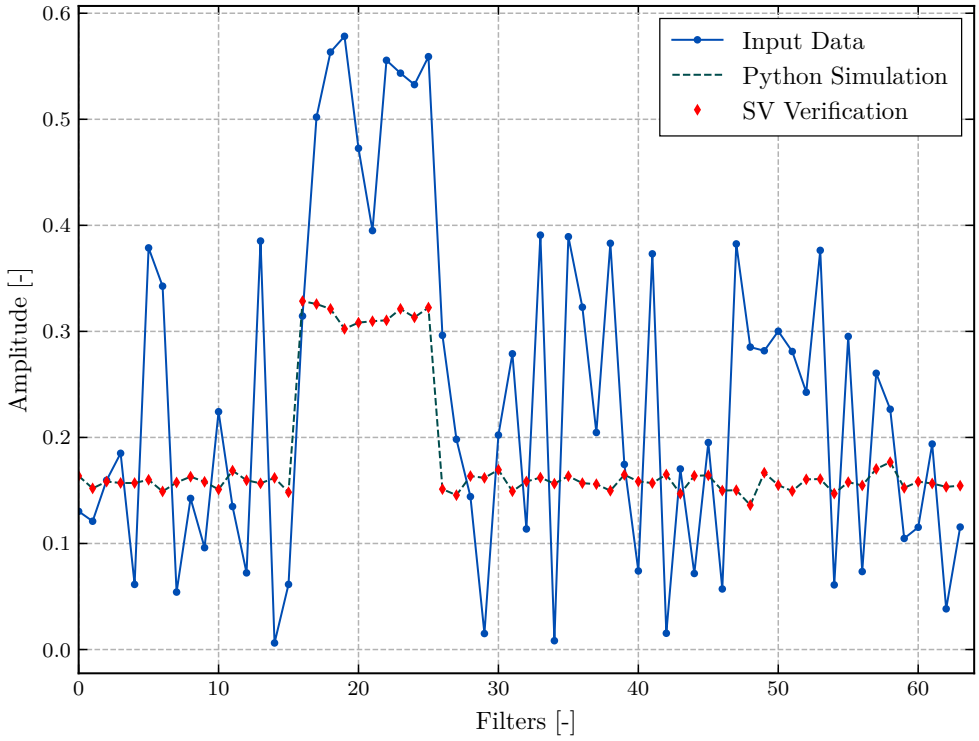

Fig. 5.20: Comparison of the filter data output in SV and Python

graph again shows the masking signal with the incoming data and the bottom graph shows the integrated and filtered data.
To verify the filtering capability of the exponential filter, a Python model of 64 smoothing filters was created and compared with the System Verilog simulation.

The same set of input values were given to the both models and their outputs were plotted in the chart shown in Fig. 5.20. The driving signal was a square signal burst with 1 μs width and 1.6 μs with the period of 6.4 μs. The amplitude was set to 0.2 and the generated noise 0.4 with an offset of 0.2. This offset represents populated AG. To filter the noise the $\alpha = 0.008$ was set. The x-axis

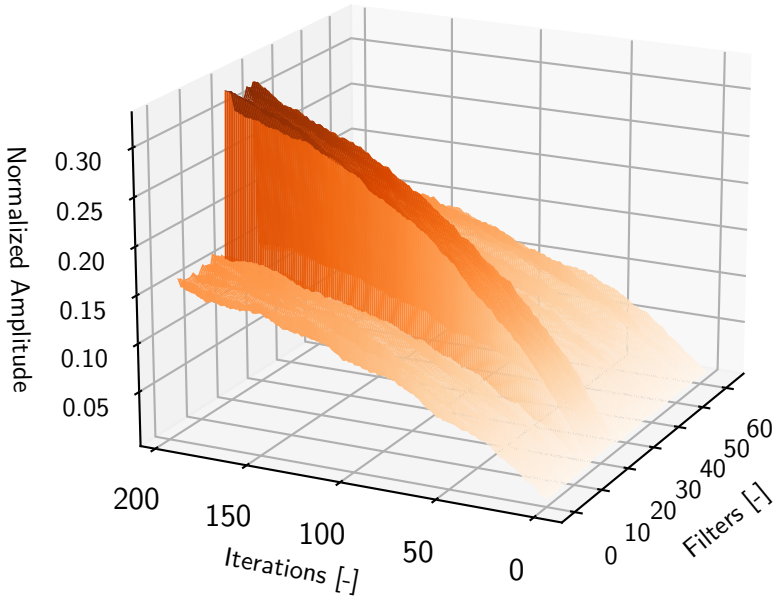

Fig. 5.21: Filter simulation for 200 iterations

represents the bin number and the y-axis unitless amplitude. It was calculated that the error between the curves from Python and the SV simulation is less than 0.001%. Fig. 5.20 shows just one realization of the signal. As the DAQ has 64 filters the behaviour of all of the filters was plotted in Fig. 5.21. This depicts 200 iterations of filtering. Fig. 5.21 shows the slow ramp up of the filtered signal with

attenuated noise. The simulation was launched with the same set of parameters as for the Fig. 5.20. To perform this simulation a burst pattern generator had to be embedded in the generator instance in the testbench environment ⟦↩5.2.2.5.⟧.

6 Conclusion

The goals and objectives set out in the beginnig of this thesis were achieved. The basic structure of the Beam Dump System was described with the focus on the Abort Gap in the beam bunch pattern. The particles populating the Abort Gap have an impact on the machine safety, which is the motivation to measure the particles in this gap with an Abort Gap Monitor. Therefore the current method of measurement including the mathematical framework was described. After that, the thesis focused on the design and implementation of currently deployed Abort Gap Monitor. It explained the measurement principle of two multiplexed analog integrators lhcb2002b and analyzed the limitation of the analog integrators. This was the reason for their removal and the creation of a new system with digital integration. This digital integration had to be built into the acquisition system using a new generation of Abort Gap Monitor hardware.
This new acquisition system was the goal of this thesis. First the concept of the system was developed. Then the digital blocks were designed and the processing part was tested using the randomized HDL testbenches. To test the complex functionality, the complete design was inserted to the CERN SY-BI testbench to emulate the VFC-HD. This verified the theoretical design functionality.
The system was installed into the LHC successfully in collaboration with colleagues at CERN. However, testing of the acquisition system was not possible due to technical difficulties during the LHC run. Therefore, the verification of the real functionality of the acquisition system was performed in the laboratory environment with an oscilloscope and an artificial signal from a waveform generator. For this tests a control script had to be created.

6.1 Further Developments Steps

The proposed acquisition system has successfully passed the first stage of development. The basic required features of the system have been implemented. This did not include sensitivity testing of the system or noise susceptibility. This will be the next step of the development to compare the current outputs of the new acquisition system with the one currently deployed. These properties have to be

tested first before the system will be fully deployed in the LHC. A further improvement of the whole system will be the addition of histograms informing about the statistical properties of the measured data.

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List of symbols, physical constants and abbreviations

AG	Abort Gap
AGM	Abort Gap Monitor
ASIC	application specific integrated circuit
BST	Beam Synchronous Timing
DAB64x	VME64x Digital Acquisition Board
DAQ	Data Acquisition System
DUT	Device Under Test
BDS	Beam Dump System
FEC	Front-end Controller
FESA	Front-end Software Architecture
FSM	Finite State Machine
IBMS	Individual Bunch Measurement System
IR6	Intersection Region 6
LHC	Large Hadron Collider
MCP-PMT	Micro Channel Plate Photomultiplier Tube
MKB	Orthogonally deflecting dilution kicker magnets
MKD	Horizontally deflecting extraction kicker magnets
MSD	Lambertson septum magnets
RF	Radiofrequency
RTM	Rear Transition Module
PMT	Photomultiplier Tube
PMT-AMP	Photomultiplier Pre-amplifier
PS	Proton Synchrotron
PSB	Proton Synchrotron Booster
SPS	Super Proton Synchrotron
SR	Synchrotron Radiation
TDE	Dump Core
TTC	Timing, Trigger and Control
VFC-HD	VME High Density FMC Carrier