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ELECTRONICALLY CONFIGURABLE TRANSFER STRUCTURES

ELEKTRONICKY KONFIGUROVATELNÉ PŘENOSOVÉ STRUKTURY

DOCTORAL THESIS
DIZERTAČNÍ PRÁCE

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ABSTRACT

The thesis is focused on the development and research in the field of electronically configurable transfer structures. The main goal is to design these structures using modern electronically adjustable active elements. The work presents a number of reconnection–less reconfigurable filtering structures, which were created with help of various design methods. Emphasis is also placed on the ability to control some of the typical filter parameters using controllable active elements. Furthermore, the work contains several topological circuit designs of active elements or building blocks with specifically implemented electronic controllability, so that these elements/blocks can be further used for the design of reconnection–less reconfigurable filters. The correctness of the design of individual proposed circuits is supported by PSpice and Cadence simulations with transistor–level models. Selected solutions are further implemented using available active elements and subjected to experimental measurements.

KEYWORDS

active element, analogue filter, current amplifier, current conveyor, current follower, electronic control, fractional–order filter, frequency filter, operational transconductance amplifier, reconnection–less reconfigurable filter, reconnection–less reconfiguration, variable gain amplifier

ABSTRAKT

Práce se zaměřuje na vývoj a výzkum v oblasti elektronicky rekonfigurovatelných přenosových struktur. Primárním cílem je návrh těchto struktur za užití moderních elektronicky řiditelných aktivních prvků. V práci je prezentováno množství elektronicky rekonfigurovatelných filtračních struktur, jež byly vytvořeny za užití různých návrhových metod. Důraz je dále kladen na možnost řídit některý z typických parametrů filtru pomocí řiditelných aktivních prvků. Práce dále obsahuje několik obvodových návrhů aktivních prvků či stavebních bloků s vhodně řešenou elektronickou řiditelností, tak, aby tyto prvky/bloky mohly být dále použity pro návrh elektronicky rekonfigurovatelných filtrů. Správnost návrhu jednotlivých zapojení je podpořena PSpice a Cadence simulacemi s modely na tranzistorové úrovni. Vybraná zapojení jsou dále realizována za pomocí dostupných aktivních prvků a podrobena experimentálnímu měření.

KLÍČOVÁ SLOVA

aktivní prvek, analogový filtr, elektronická řiditelnost, elektronicky rekonfigurovatelný filtr, filtr fraktálního řádu, kmitočtový filtr, proudový konvejor, proudový sledovač, proudový zesilovač, řiditelný filtr, řiditelný napěťový zesilovač, operační transkonduktanční zesilovač

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DECLARATION

I declare that I have written my doctoral thesis on the theme of "Electronically configurable transfer structures" independently under the supervision of a doctoral thesis supervisor and using the technical literature and other information sources which are all quoted in the thesis and detailed in the list of literature at the end of the thesis.

As the author of the doctoral thesis, I furthermore declare that, as regards the creation of this doctoral thesis, I have not infringed any copyright. In particular, I have not unlawfully encroached on anyone's personal and/or ownership rights and I am fully aware of the consequences in the case of breaking Regulation S 11 and the following of the Copyright Act No 121/2000 Sb., and of the rights related to intellectual property right and changes in some Acts (Intellectual Property Act) and formulated in later regulations, inclusive of the possible consequences resulting from the provisions of Criminal Act No 40/2009 Sb., Section 2, Head VI, Part 4.

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List of Used Abbreviations

ACA	Adjustable Current Amplifier
AP	All Pass
BOTA	Balanced Operational Transconductance Amplifier
BP	Band Pass
BS	Band Stop
CA	Current Amplifier
CC–CFA	Current–Controlled Current Feedback Amplifier
CCCDTA	Current–Controlled Current Differencing Transconductance Amplifier
CCCFTA	Current–Controlled Current Follower Transconductance Amplifiers
CCCII	Current Controlled Conveyors of the second generation
CCDDCC	Current–Controlled Differential Difference Current Conveyor
CCII	Current Conveyor of the second generation
CCII+/-	Current Conveyor of the second generation with positive and negative output
CF	Current Follower
CFE	Continued Fraction Expansion
CG–CCDDCC	Controlled–Gain Current–Controlled Differential Difference Current Conveyor
CM	Current Mode
DO–CA	Dual–Output Current Amplifier
DT	Direct Transfer, Diamond Transistor
DVB	Differential Voltage Buffer
ECCII	Electronically Controllable Current Conveyor of the second generation
F–D	Fully–Differential
FD–CF	Fully–Differential Current Follower
FLF	Follow–the–Leader Feedback
FO	Fractional–Order
FOE	Fractional–Order Element
GCCII	Generalized Current Conveyor of the second generation
HP	High Pass
HPZ	High Pass with Zero
IC	Integrated Circuit
IDT	Inverse Direct Transfer
IFLF	Inverse Follow–the–Leader Feedback
IOGC–CA	Independent Output Gain Controlled Current Amplifier
I–V	Current to Voltage
LP	Low Pass
LPZ	Low Pass with Zero
M–C	Mason–Coates
MIMO	Multiple–Input Multiple–Output
MISO	Multiple–Input Single–Output
MLT	Multiplication unit
MO–CF	Multiple–Output Current Follower
MOTA	Multi–Output Transconductance Amplifier
MUNV	Method of Unknown Nodal Voltages
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
SFGs	Signal–Flow Graphs
SIMO	Single–Input Multiple–Output
SISO	Single–Input Single–Output

SITO	Single–Input Triple–Output
SNAP	Symbolic Network Analysis Program
UCC	Universal Current Conveyor
VCCS	Voltage–Controlled Current Source
VCG–CCII	Voltage and Current Gain Current Conveyor of the second generation
VDCC	Voltage Differencing Current Conveyor
VDDB	Voltage Differencing Differential Buffer
VDTA	Voltage Differencing Transconductance Amplifier
VGA	Variable Gain Amplifier
V–I	Voltage to Current
VM	Voltage Mode
ZC–CG–VDCC	Z–Copy–Controlled–Gain Voltage Differencing Current Conveyor

List of Used Symbols

α	fractional–order
A	voltage gain
a	coefficients of the fractional–order approximation
β	fractional–order
B	current gain
b	coefficients of the denominator
BW	bandwidth
C	capacitor, capacitance
C_α	pseudo–capacitance (fractional–order)
δ	fractional–order
Δ	determinant
$D(\boldsymbol{s})$	denominator of the transfer function
f_0	pole frequency
f_C	center frequency
f_{max}	upper frequency of the operational bandwidth
f_{min}	lower frequency of the operational bandwidth
f_S	stop–band frequency
γ	fractional–order
G	conductance
g_m	transconductance
I	current
$\boldsymbol{I}$	current (complex variable)
I_{bias}	control current
I_{SET}	control current
k	coefficients
$K(\boldsymbol{s})$	transfer
K_P	transfer in pass band
K_S	transfer in stop band
L	inductance
L_α	pseudo–inductance (fractional–order)
m	positive integer
n	(integer) order/ transfer of CF input
$N(\boldsymbol{s})$	numerator of the transfer function
ω_0	angular frequency
Q	quality factor
q_i	i^{th} parameter
R	resistor, resistance
R_{in}	intrinsic (input) resistance
R_X	intrinsic (input) resistance
S	relative sensitivity
$\boldsymbol{s}$	Laplacian operator (complex variable)
τ	time constant
V	voltage
$\boldsymbol{V}$	voltage (complex variable)
V_{SET}	control voltage
Y	admittance
Z	impedance

Contents

Introduction

Nowadays, we usually encounter signals in their digital form and similarly we come across the digital signal processing. Despite this fact, the analog frequency filters are an essential part of the electronic circuitry, which find their utilization in many areas of industry such as telecommunication, radio electronics, measurement and control technology, electroacoustics etc. as the digitized signals still need to be worked with and processed in their analogue form as well. Furthermore, the digital filters, in comparison to the analog ones, have some disadvantages such as processed signals must be firstly converted into digital form which results in the loss of part of the information, quantization noise and limitation of usable bandwidth. Moreover, the process of the digital signal conversion takes a considerable amount of time (no real-time operations) and requires high clock frequency. For this reason, analogue filters are subject to increasing demands on the easily and immediately (fast reaction) adjustable properties due to the continuous development which results in the design of new filter structures with improved features.

As one of these properties, we can mention the ability of the electronic reconnection–less reconfiguration of their transfer function (transfer response) achieved by the utilization of the modern active elements, which provide the electronic tunability of some of their parameters, voltage or current transfer (gain), transconductance, intrinsic resistance, for instance. The resulting type of transfer function of given filtering structure is then determined by appropriate setting of these electronically (continuously in many cases) settable parameters instead of the manual switching between inputs/outputs of the filter, or physical topological modification of the internal structure, which is not appropriate or even possible in situations like the on–chip implementation of given filtering structure. Electronically adjustable active elements can also be used to obtain an advantageous electronic tunability of the pole frequency, quality factor, or frequency limits of pass–band and stop–band regions and gains/attenuations in these areas bringing an additional degree of freedom within designed applications. Newly proposed active elements can be intentionally designed in the way, they can offer interesting and useful abilities of the electronic tunability for the future applications.

1 State–of–the–Art

The development of the electronic industry and the signal processing area creates the ever–increasing demands on features of all types of circuits including the frequency filters as the signal filtering is the fundamental operation of electrical circuits. This leads to the design of new filtering structures with enhanced properties such as an electronic tunability of a desired parameter (pole frequency, quality factor, order, level of pass–band/stop–band area, etc.), wider operational bandwidth range, or a presence of several available transfer functions allowing their switchless selection (single input and single output of topology).

A feature of frequency filters being more versatile (providing several various types of the transfer function from single filtering circuit topology) is a common trend of the last few decades. Based on this fact, we can divide filters into single purpose filters [1–5], when the structure is specifically designed to provide one particular function, multifunctional filters [6–11] offering two and more functions and so–called universal filters [12–27] which provide all standard transfer functions (if we are talking about the 2^{nd}–order filters, it means functions of all pass (AP), band pass (BP), band stop (BS), high pass (HP), and low pass (LP)) and we can use whichever currently demanded function. Despite a useful ability of multifunctional and universal filters to provide various transfer functions, a typical feature of these structures consists in availability of transfer functions between different nodes of the structure. This leads to the circuit topology having multiple inputs and/or outputs. The mentioned multifunction/universal filters, depending on the organization of their inputs/outputs, can be divided into Single–Input Multiple–Output (SIMO) filters [6], [7], [9], [11–18], [29], [30] (as the name suggests, these structures consist of one input terminal and two or more output terminals), Multiple–Input Single–Output (MISO) filters [10], [19–28], [31], [32] (with two or more input terminals and one output terminal) and Multiple–Input Multiple–Output (MIMO) filters [8], [33–35] (having two or more input terminals and two or more output terminals). Subsequently, the manual reconnection (port interchange) between the inputs/outputs of such filter or their suitable combination is required in order to change the type of the transfer function. The manual reconnection is not suitable or even possible in some cases, on–chip implementation of given structure, for example. The resulting output response can be also depending on a combination of the excitation voltages or currents used simultaneously (in specific nodes of topology for example). As a result, it suggests the usage of copies of the input voltage/current, their inverted form or even their increased (amplified) or decreased value in some cases. The fact, we need several input signal copies, or their amplified/attenuated value applied to different circuit nodes, can become an increasing technical difficulty. From the point of view of on–chip implementation, the interchange between the inputs/outputs of the filter can be achieved by complementing the filtering structure with controllable switches, for instance. Nonetheless, this brings some subsequent problems such as requirements for an additional space on chip and power consumption for the control logic as well as issues with linearity and parasitic effects. The design of the control

logic itself is required as it is usually not included in the filter design. The switching itself can bring additional issues such as possible interference caused by the switching process to other parts of complex system (application), requirements on the additional digital control (software development), etc. It is also possible to come across the so–called Single–Input Single–Output (SISO) filters [36], but in this case, a manual modification of the internal topology (placement and character of passive elements in topology or the circuit interconnection) is necessary in order to provide a different transfer function which is again not possible in case of on–chip implementation.

A possible solution of above–mentioned issues is offered by a design of so–called reconnection–less (switchless) reconfigurable filters [37–50]. These concepts can be understood as a two–port structure (having one input and one output terminal), where the resulting transfer function is based on the setting of electronically controllable parameters (usually controlled by DC current or DC voltage, which can be externally applied to the chip or discrete solution) of used active elements. The output response is then changed continuously and solely by the electronic form of driving without a necessity of any switching between the inputs and/or outputs of the filter, or any modification of the internal topology of the filtering structure. This approach can be beneficial in case of on–chip implementation when we do not have the possibility to modify the structure or swap between the nodes of the filter. The reconnection–less reconfigurable filters are common for RF bands around gigahertz (microwave systems most usually) [37–41], where the switchless change of transfer function is typically achieved by the electromagnetic coupling of elements. It is not so easy in low–frequency circuitry [42–50] where adjustable electromagnetic coupling existing for RF bands of > MHz is not easily possible (due to physical values and sizes of inductances/coils, etc.). Therefore, we have to utilize adjustable features of active elements.

The previously proposed (low frequency) solutions of reconnection–less reconfigurable filters are discussed in further text. The paper [42] presents a reconnection–less reconfigurable filter using a Z–Copy Controlled Gain Voltage Differencing Current Conveyor (ZC–CG–VDCC). It is possible to change between AP and LP function. The paper provides not only simulations but also the experimental measurements. The solution in [43] offers functions of AP, BP, BS, HP, LP and special functions of low pass and high pass with transfer zero (LPZ, HPZ). The structure is based on Operational Transconductance Amplifiers (OTAs) and the simulated results are supported by experiments. The research in [44] offers a design of a reconnection–less reconfigurable filter based on OTAs and an Electronically Controllable Current Conveyor of the second generation (ECCII) providing functions of AP, LP, LPZ and inverting direct transfer (IDT). The research is verified by PSpice simulations. Paper [45] introduces an OTA–based reconnection–less reconfigurable filter with functions of AP, HP and LP. The results are provided for PSpice simulations. The filter in [46] is utilizing OTAs and provides AP, BP, BS, HP, HPZ and LPZ supported by PSpice simulations. The AP/BS filter based on Current conveyors of the second generation (CCII) is described in [47]. The

experimental results are provided. The design in [48] is based on Voltage–Differencing Current Conveyor (VDCC) and Dual–Output Current Amplifier (DO–CA) and features BS, HP, LP, HPZ and LPZ functions. The results are provided for simulations and experimental measurements as well. A circuit solution based on Controlled–Gain Current–Controlled Differential Difference Current Conveyors (CG–CCDDCCs) providing all above–mentioned transfer functions can be found in [49]. Finally, the solution described in [50] offers functions of HP and LP of the 1st–order together with AP and BS of the 2nd–order. The design is supported by PSpice simulations, and it is using Differential Voltage Buffers (DVBs), Variable Gain Amplifiers (VGAs) and OTA as its building blocks. All described solutions are working in the voltage mode (VM) except the filter in [48] which is operating in the current mode (CM). A brief comparison of these filters has been made in Tab. I.

TABLE I. COMPARISION OF PREVIOUSLY PROPOSED RECONNECTION–LESS RECONFIGURABLE FILTERS

Reference number	Operation mode	Number of active/passive elements	Available functions (count)	Simulations/ Measurements	Independent adjustment of f_0	All capacitors grounded	Technology	Supply voltage	Note
[42]	VM	1/1	AP, DT, LP (3)	Yes/Yes	Yes	Yes	TSMC 0.18 μm	±1V	[1]
[43]	VM	4/2	AP, BP, BS, HP, HPZ, LPZ (6)	No/Yes	N/A	No	Comerc. available	±5V	-
[44]	VM	3/2	AP, LP, LPZ (3)	Yes/No	Yes	Yes	Comerc. available	±5V	[1]
[45]	VM	2/2 2/2 2/2 2/3	AP, DT, HP, HPZ, LP (5) AP, DT, HP, HPZ, LP (5) AP, DT, HP, HPZ, LP (5) AP, LP (2)	Yes/No	N/A N/A N/A N/A	No No Yes Yes	Comerc. available	±5V	[1], [2]
[46]	VM	4/2 4/2 4/3	AP, BP, BS, HP, HPZ, LPZ (6) AP, BP, BS (3) AP, BP, BS, HP, HPZ, LPZ (6)	Yes/No	Yes Yes Yes	No No No	Comerc. available	±5V	-
[47]	VM	2/3	AP, BS (2)	Yes/Yes	Yes	No	Comerc. available	±5V	-
[48]	CM	2/3	BS, HP, HPZ, LP, LPZ (5)	Yes/Yes	Yes	Yes	Comerc. available	±5V	-
[49]	VM	4/4	AP, BP, BS, HP, LP (5)	Yes/No	Yes	Yes	I3T 0.35 μm	±1.65V	-
[50]	VM	6/3	AP, BP, IDT, HP, LP (5)	Yes/No	N/A	Yes	Comerc. available	±5V	[3]

Notes: [1]filter of the 1st order, [2]there are six solution in total (four of them are further analyzed), [3]HP a LP functions are of the 1st order

Some researchers made their designs [51–53] (design of fractional–order filters in this case) having partial character of reconnection–less filters. Their reconfiguration of the transfer function is solved by the array of electronic switches controlled digitally (as discussed above).

These filters offer the electronic reconfigurable reconnection of the transfer without a necessity of any manual change or modification. Nonetheless, the solutions offer only the change between functions in a strictly binary manner (the switches are either on or off and require control logic (decoder) or/and software in comparison to a continuous control, where suitable active elements are employed as in case of filters in [42–50]. A possible continuous electronic control of active elements, used for the design (as in [42–50]), can offer a feature of fine–tuning compensating undesired gain shift, for example. The gain level adjustment of stop–band/pass–band area of available functions can create a beneficial property in case of the signal processing [50]. The design of the reconnection–less reconfigurable filters can be performed by two conventional ways/methods. The first one supposes to design a filter with the ability of the reconnection–less reconfiguration from the beginning of the design procedure [42–53]. The other approach is based on the suitable modification of an existing structure which does not dispose of such ability. This will be described in further text.

In recent years, the domain of the fractional–order (FO) circuit design received an increased attention of many scientists due to its possible utilization in various standard and multidisciplinary areas including medicine [54], [55], modeling and measurement of various signals, tissues and materials [56–58], agriculture [59] and car industry [60], for example. These widespread areas give many new potential applications a chance for a further development of given area. In comparison to the integer–order systems, FO systems provide an increased degree of freedom, due to the presence of the non–integer–order (α) offering the ability to follow the required resulting features more accurately. It extends possibilities of various applications. The research concerning the electrical engineering, synthesis of fractional–order circuits and their utilization for modelling of systems with fractional–order characteristics, in particular, covers synthesis of FO frequency filters [51–53], [61–70], FO oscillators [71–75] and other circuits exhibiting FO characteristics [76–87].

The most typical approach to the design of circuits with FO characteristics is the employment of so–called Fractional–Order Elements (FOEs). The FOE can be understood as a passive non–integer element with the slope of the magnitude of $\pm 20 \times \alpha$ dB/decade, where parameter α (order) is a real number in range $0 < \alpha < 1$. Similarly, the phase shift of such element is equal to $\pm 90 \times \alpha$ degrees. The FOE either has the character of a FO capacitor (element with its character being between a standard capacitor and standard resistor), or a FO inductor (its character is between a standard inductor and standard resistor)). The impedance of FO capacitor is given as $Z_C = 1/(\boldsymbol{s}^{\alpha} C_{\alpha})$, where $\boldsymbol{s}^{\alpha}$ represents the Laplacian operator with FO characteristics and C_{α} is a pseudo–capacitance having its unit of Farad/sec$^{1-\alpha}$ [88]. The impedance of a FO inductor is described by $Z_L = \boldsymbol{s}^{\alpha} L_{\alpha}$, where $\boldsymbol{s}^{\alpha}$ is again the FO Laplacian operator and L_{α} is a pseudo–inductance with units of sec$^{1-\alpha}$/Farad [78]. There are three general ways how to obtain the FOE. The first technique is based on the physical fabrication of these elements [89–94] on various basis (electro–chemical [89–91], silicon based [92], [93] organic materials [94], for instance). The main disadvantages of this approach are complex and

expensive process of fabrication, commercial unavailability of these elements and the absence of the electronic adjustment of the resulting order (and pseudo-value). Because of the complex fabrication of the above–mentioned solutions of FOEs, these elements are usually substituted by specifically designed RC ladder networks with suitably selected values of passive elements resulting in the specific order and pseudo-capacity/inductance [65–70], [88], [95], [96]. RC structures (as the second possible approach to the design of FOEs) offer a possibility of a simple design since they only need commercially available passive elements (common capacitors and resistors). There are several topologies of the RC ladder structures such as Foster I, Foster II, Cauer I, and Cauer II [88], [95], for instance. The values of individual parts of the RC structure are calculated based on a suitable fractional–order approximation, the approximation introduced by Valsa [95], or the Oustaloup approximation [96], for instance. The drawback of this approach consists in the impossibility of electronic adjustment of the order similarly to the previous approach. The values of individual parts of the RC structure need to be changed for each value of the order and pseudo–capacitance/inductance (general immittance). The last approach involves the use of a topology with electronically adjustable active elements. The active topology approximates the function of a FO impedance (so–called FO emulators) [76–79] or behaves as a FO two-port (FO integrator/differentiator) [80–87]. The disadvantage of this approach consists in high complexity of the resulting structure and necessity of active elements (and power supply). The advantage, on the other hand, is a possibility of the electronic tunability (reconfiguration) of the order, character (inductance/capacitance or integrator/differentiator) and pseudo-value which can be easily set depending on the desired value of α and L_α/C_α. These active solutions of FO two-port and immittances may also offer the electronic adjustment of other parameter(s) (frequency band where the FO approximation is valid, gain adjustment, etc.). The FO integrators/differentiators can be further divided into solutions using passive FOE [81–83], or not using FOE [84–87] for their function. FO integrators/differentiators based on a FOE do not allow the electronic control of the order (they still might offer the electronic control of other parameters such as gain). The FO integrators/differentiators, which do not used FOEs, usually perform the electronic adjustment of order and other parameters as well.

When discussing the FO filters, the slope of the transition between the pass–band and stop–band area is characterized by the relation $20\cdot(n+\alpha)$ dB/decade, where n stands for integer order and α provides the fractional–order parameter. FO filters can be understood as a special case of reconnection–less reconfigurable filters as their order (and possibly a type of function) can be controlled electronically in some cases as shown in [51–53], for example. It is possible to come across two basic approaches to the design of fractional–order filters. The first one supposes the placement of FOEs into the filtering structure. Typically, we are talking about filters with a working capacitor(s) being replaced by the FOE (approximated by RC structure [65–70], for example). The second approach is based on the approximation of the Laplacian operator of the fractional–order $\boldsymbol{s}^\alpha$ by the integer–order function of the higher order, which results in the design of a special filtering structure with specific values of passive and active

elements [51–53], [61–64]. The resulting filter structure is then the 3rd and higher than 3rd–order topology, depending on the order of selected FO approximation (giving the bandwidth where the approximation is valid). A suitable 2nd–order approximation is typically used [61], [62], but it is also possible to use higher order functions [62], [97] that provide a wideband improvement of validity and the accuracy of the approximation. However, it also increases the complexity of the circuit solution. The advantage of this method expects that the resulting fractional–order filter can provide a possibility of the electronic control of the order (in case of usage of electronically controllable active elements). The higher complexity of the circuit structure and the higher number of active elements in the circuit seems to be significant disadvantage in comparison to passive FOE–based filters. The most typical frequency response of proposed fractional–order filters is the LP function [51–53], [61–67], [69], [70]. Some structures [51], [52], [61], [64] offer the FO HP function. Furthermore, fractional–order filters of BP [51], [52], [62], [68], [69] and BS [51], [52] type of response are also reported. We can find FO filters providing transfer functions having the Butterworth characteristic in most cases, but it is also possible to find fractional–order functions exhibiting Chebyshev characteristics [53], [65].

Let us also mention the field of fully–differential structures [98–104]. The design of these structures can be approached directly with regards to the direct design of fully–differential circuits, or by the transformation of non–differential structures into fully–differential ones. In case of a direct design, an experienced designer is able to design the differential structures intuitively. The transformation of a non–differential structure, a non–differential filter in particular, into a fully–differential one is based on the mirroring of passive components around the horizontal axis of the circuit, depending on the chosen transformation method. It can be followed by the mirroring of the active elements if the fully–differential version of the active element is not available. The transformation method has two ways of possible application, i.e., transformation of vertical and transformation of horizontal structures [104]. Transformation of horizontal structures mirrors the passive elements in the horizontal branches of the circuit when the values of the passive components in the vertical branches remain unchanged and the values of the components in the horizontal branches are modified in dependence on type of the passive element (the values of capacitors are doubled, and the values of resistors are halved). The transformation of the vertical structures is also based on the mirroring of the passive elements in the horizontal branches of the circuit, but the values of the components in the vertical branches are modified. The fully–differential active circuits offer better power supply rejection ratio, lower harmonic distortion, greater dynamic range of the processed signals and better attenuation of undesirable common–mode signals, in some cases [105].

Active elements with several independently adjustable parameters (multi–parameter control) can provide an additional degree of freedom. It increases the variability of applications where these special active elements are used. Many active elements suitable

for the signal processing are described in [106]. An electronic control of several parameters of different type within various applications (pole frequency, quality factor, the level of gain in pass–band/stop–band region in case of frequency filters, oscillation condition, frequency of oscillations, amplitude of oscillations in oscillators, etc.) belongs to desirable features in the modern analog circuit design. In case of the multi–parameter tunability of active elements [42], [49], [107–119], the current gain B, voltage gain A, transconductance g_m and intrinsic resistance R_X (or R_{in}) belong to the most typical controllable parameters/features of these devices. The idea of electronically adjustable intrinsic resistance R_X has been introduced in [107]. Despite the fact this resistance is technically a parasitic feature, the possibility to control this impedance can be considered as a beneficial advantage in some types of circuits offering an additional degree of freedom. Many papers [42], [49], [107–112] focus on the proposal of different types of current conveyors of the second generation (CCIIs) providing multi–parameter control (several independently adjustable parameters are available in single device). We can mention Current Controlled Conveyors of the second generation (CCCIIs) [107], [108], Generalized Current Conveyor of the second generation (GCCII) [109], Voltage Differencing Current Conveyor (VDCC) [110], Voltage and Current Gain Current Conveyor of the second generation (VCG–CCII) [111] and more advanced current conveyors such as Current–Controlled Differential Difference Current Conveyor (CCDDCC) [112], Controlled–Gain Current–Controlled Differential Difference Current Conveyor (CGCCDDCC) [49] and Z–Copy Controlled–Gain Voltage Differencing Current Conveyor (ZC–CG–VDCC) [42]. Furthermore, there are papers introducing a design of Current Amplifiers (CAs) [113–115], different types of Operational Transconductance Amplifiers (OTAs), namely Current–Controlled Current Differencing Transconductance Amplifier (CCCDTA) [116] and Current–Controlled Current Follower Transconductance Amplifiers (CCCFTAs) [117], [118]. Lastly, an active element in [119] is a Current–Controlled Current Feedback Amplifier (CC–CFA). Proposed active elements in [107], [108], [112–115], [119] and [49] provide the electronic control of the current gain B together with the intrinsic resistance R_X. The element in [49] offers an interesting ability to control the current gain of each output separately (the element has two outputs). The transconductance g_m and the intrinsic resistance R_X are the independently controllable parameters in case of [110], [116–118]. The research in [111] comes up with the electronic control of the voltage gain A and the intrinsic resistance R_X. The designs in [42] and [109] introduce the control of three independent parameters, the intrinsic resistance R_X, transconductance g_m and current gain B in case of the element proposed in [42] and the intrinsic resistance R_X, current gain B and voltage gain A (transfer from Y to X terminal of a CCII) for the element in [109]. The designs [42], [49], [107–113], [115–119] offer the simulation results while [42], [110], [114], [115] are supported by the experimental measurements (measurements of so-called behavioral models using specifically interconnected commercially available parts and active elements).

2 Thesis Goals

The dissertation is primarily focused on the design of filtering structures providing the reconnection–less (switchless) electronic reconfiguration of their transfer functions using electronically tunable active elements. The goals of the dissertation can be divided into three main parts.

The first part targets on the synthesis and analysis of new circuit solutions of reconnection–less electronically reconfigurable filtering structures based on modern active elements such as current conveyors, current followers, operational transconductance amplifiers, current amplifiers, etc. For the feature of electronic reconfigurability, the modern advanced active elements (providing the electronic controllability of some of their parameters, such as transconductance, amplification, and input resistance) are used. The emphasis is placed on the versatility of the proposed solutions. Except the reconfiguration, the filters provide the possibility of electronic adjustability of selected parameters, such as the pole frequency, quality factor and others by specific beneficial use of controllable features of active elements, if possible, for the obtainment of high degree of freedom in reconfigurability and adjustability of performance. The design of reconnection–less reconfigurable filters, presented in this thesis, employs various methods of synthesis. Method of Unknown Nodal Voltages (MUNV) based on the square admittance matrix is the first used approach. Other applied procedure is Signal Flow Graph (SFG) method of synthesis resulting from Mason–Coates graphs. The next used method of synthesis considers filtering structures of high–orders based on the cascade combination of the second and first order filter sections with feedbacks, where the individual blocks in the cascade are defined by the normalized values of the transfer function coefficients. Reconnection–less reconfigurable filtering structures can be also generated by a modification of the previously presented filters without the ability of the electronic reconfiguration. The suitable supplement(s) of controllable active element(s) brings reconfigurable features in existing topology in some cases. The last used approach uses the transformation of reconnection–less filtering topology working in the voltage mode into a counterpart circuit topology operating in the current mode. The SNAP software verifies proposed structures at the initial stage of the design. PSpice simulations, using available models of active elements, subsequently support detailed study of topologies, as well as simulations in the Cadence IC6 (spectre) environment using devices designed in CMOS process. Selected circuits are also practically implemented using available active elements and subjected to experimental measurements. Experimental results are compared with theoretical expectations and simulation results.

The second goal of the thesis consists of the design of fractional–order filtering structures (and corresponding FO circuits), as they can be considered a special case of reconnection–less reconfigurable filters, in order to see and compare features of these circuits with standard integer–order designs. The fractional–order filters, introduced in the thesis, utilize the

replacement of one or more working capacitors by appropriately designed FOEs employing approximation by RC structures. These designs are also supported by PSpice or cadence simulations and experimental measurements.

The last part of the thesis focuses on the research and development in the field of modern advanced active elements and building blocks that provide the independent multi-parameter electronic controllability. These intentions lead to additional degrees of freedom used for extended possibilities in adjustability and controllability of specific parameter(s) of future application, in reconnection–less reconfigurable filters especially.

3 Description of Used Active Elements

This chapter describes the active elements used for the design of own newly presented reconnection–less electronically reconfigurable filters (chapter 5) and the design of the active element and building blocks in chapter 6. The topologies in chapter 5 and 6 utilize active elements of Operational Transconductance Amplifier (OTA) [106], Variable Gain Amplifier (VGA) [106], Voltage Differencing Transconductance Amplifier (VDTA) [120], Adjustable Current Amplifier (ACA) [121], Current Follower (CF) [99] (Multiple Output Current Follower (MO–CF) [121] in particular), Controlled–Gain Current–Controlled Differential Difference Current Conveyor (CG–CCDDCC) [49] and newly proposed Independent Output Gain Controlled Current Amplifier (IOGC–CA) which is illustrated in section 6.1. The filter presented in subsection 5.2.1 uses active elements implemented in CMOS 0.18 μm TSMC technology. The research described in subsection 5.3.2 is based on commercially available integrated circuits, while designs in subsections 5.4.1, 5.5.1, 5.5.2 and 6.1.1 use commercially available integrated circuits together with a Universal Current conveyor (UCC) [122], [123]. The remaining solutions in subsections 5.1.1, 5.1.2, 5.2.2, 5.3.1, 6.2.1 and 6.2.2 are designed by building cells implemented in ON Semiconductor CMOS 0.35 μm I3T process [124]. Mentioned building cells are fabricated in form of an integrated circuit (IC) encapsulated in DIL40 and introduced in [125]. The chip [125] contains different types of building cells namely: a Current–Controlled Current Conveyor of the second generation (CCCII) with four outputs, Current Amplifier, Voltage multiplication units (multipliers) (MLTs) with a current output terminal (unit utilizing CMOS technology and unit based on a bipolar core) and a Voltage Differencing Differential Buffer (VDDB). These cells allow construction of various advanced active elements. The voltages of all input and output terminals of the individual active elements presented in this chapter are taken in relation to the ground (analog ground = 0 V). The current arrows in the schemes (principles) of active elements (in chapter 3) and circuits (in chapter 4, 5 and 6) do not necessary correspond with the actual orientation of the current. The actual current orientation (the outputs of specific active elements) is given by the triangle arrows. Similarly, the actual current orientation of output responses of individual proposed circuits is defined by the transfer function of specific circuit.

3.1 Universal Current Conveyor (UCC)

First of all, it is appropriate to introduce the Universal Current Conveyor (UCC) [122], which was created in cooperation of the Brno University of Technology and the ON Semiconductor Design Center. It was used in case of practical implementation of some presented active elements by the appropriate connection of its individual terminals. The chip is designated UCC–N1B_0520 and it is implemented by CMOS 0.35 μm I3T technology. In addition, the chip also contains second–generation current conveyor with positive and negative output (CCII+/-) [106]. The schematic symbols of these elements are shown in Fig. 3.1.

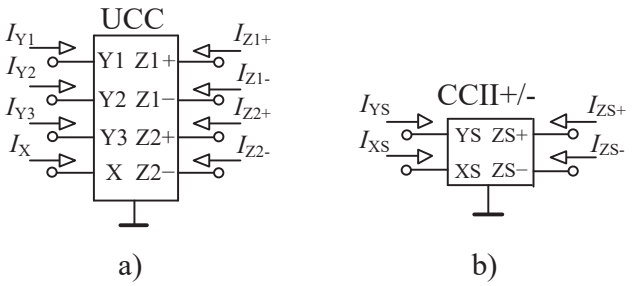


Fig. 3.1: Schematic symbols of: a) Universal Current Conveyor (UCC), b) second generation Current Conveyor with positive and negative output (CCII +/-)

The universal current conveyor consists of three high–impedance voltage input terminals Y1, Y2 and Y3, where Y2 has the opposite polarity in relation to Y1 and Y3. Terminal X is a low–impedance current input, and Z terminals are high–impedance current outputs. The current from terminal X is mirrored to Z terminals with the same or opposite polarity. The universal current conveyor can be described by the following definition matrix of inter–terminal relations:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ V_X \\ I_{Z1+} \\ I_{Z1-} \\ I_{Z2+} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_{Z1+} \\ V_{Z1-} \\ V_{Z2+} \\ V_{Z2-} \end{bmatrix}. \tag{3.1}$$

The CCII +/- element is characterized by the simplified matrix:

$$\begin{bmatrix} I_{YS} \\ V_{XS} \\ I_{ZS+} \\ I_{ZS-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_{YS} \\ I_{XS} \\ V_{ZS+} \\ V_{ZS-} \end{bmatrix}. \tag{3.2}$$

3.2 Operational Transconductance Amplifier (OTA)

The idealized OTA [106] element can be described as a voltage controlled current source (VCCS). The transfer of the input differential voltage to output current is depending on the value of the transconductance g_m. The schematic symbol of the OTA element is illustrated in Fig. 3.2.

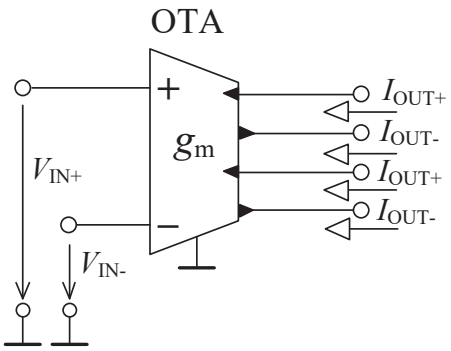


Fig. 3.2: Schematic symbol of the OTA element

Depending on the number of outputs of the OTA element, we can distinguish between OTA (with single output), Balanced–Output Transconductance Amplifier (BOTA) [126] (with two mutually opposite outputs) and Multiple–Output Transconductance Amplifier (MOTA) [98] (with three and more outputs of both current orientations). The ideal transfer relation between inputs and outputs is defined as:

$$I_{OUT\pm} = \pm g_m (V_{IN+} - V_{IN-}) . \tag{3.3}$$

A possible implementation of the OTA (MOTA in particular) by the UCC is shown in Fig. 3.3 (terminals Y1 and Y2 are used as inputs, terminal Y3 is grounded, and the X terminal is grounded through resistor R for UCC operating as OTA). The transconductance of this implementation is then set by the value of resistor R, where $g_m = 1/R$.

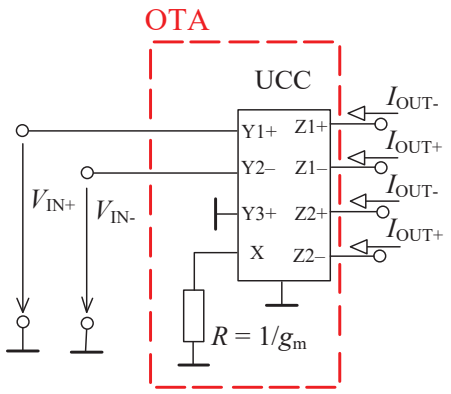


Fig. 3.3: Implementation of the OTA element by the UCC

Other solution of OTA is using a CMOS model of the OTA taken from [42]. The transconductance of this model is controlled by the DC current I_{SET_gm}.

The OTA elements were also implemented by the CMOS multiplication unit from the chip described in [125]. The MLT operates as an OTA when differential pair of Y terminals serve as voltage inputs and selected X terminal (from second differential pair) is used to control the

transconductance while the remaining X terminal is grounded, or vice versa (I_{OUT} = (V_{X1} - V_{X2}).(V_{Y1} - V_{Y2})·k, where k is a constant given by technological parameters, designed aspect ratios of specific transistors). As the input and control terminals can be swapped, this implementation of OTA can easily provide the output current of both orientations. The transconductance of this solution is controlled via DC voltage V_{SET_gm}.

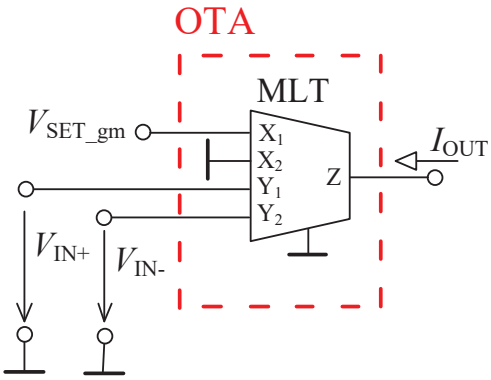


Fig. 3.4: Implementation of the OTA element by a multiplication unit from [125]

The last used solution (shown in Fig. 3.5) of the OTA element (BOTA in particular) is based on commercially available ICs LT1228 [127] and EL4083 [128]. The LT1228 device operates as an OTA element with single output. The transconductance is controlled by DC current I_{SET_gm}. The design (where this solution was used) requires transconductance amplifiers with two outputs. Therefore, the EL4083 provides copies of the current from LT1228 whereas current transfer of EL4083 is set to 1.

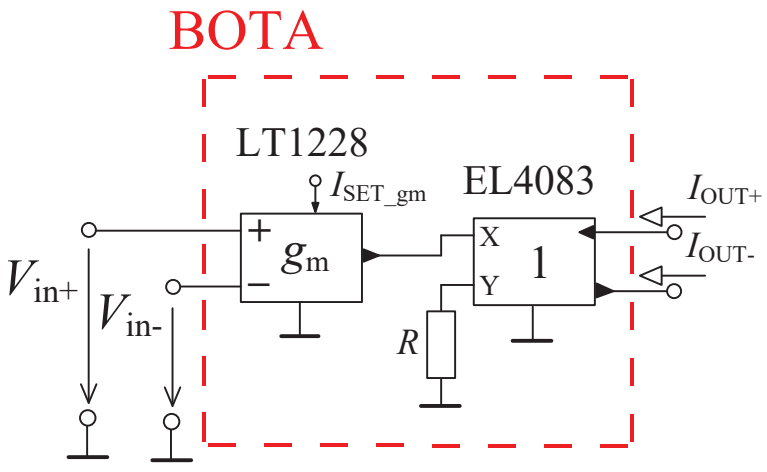


Fig. 3.5: Implementation of the OTA element by LT1228 and EL4083 ICs

3.3 Current Follower (CF)

The CF [99] element copies the input current to its outputs. It allows to obtain multiple copies of current with the same or opposite polarity (orientation) as the copies of current cannot be simply and directly taken from high-impedance circuit nodes in comparison to voltage. The CF with multiple outputs is usually referred to as MO–CF [121]. The schematic symbol of the MO–CF with four outputs is depicted in Fig. 3.6.

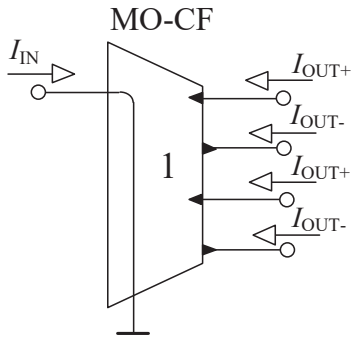


Fig. 3.6: Schematic symbol of the Multiple–Output Current Follower (MO–CF)

The ideal behavior of the CF element is described by relation:

$$I_{OUT\pm} = \pm I_{IN}\,. \tag{3.4}$$

The MO–CF can be implemented by the UCC as shown in Fig. 3.7. All Y terminals are grounded, and the X terminal is used as a current input. This solution of the MO–CF has been also used as a part of structure of the IOGC–CA element in some cases.

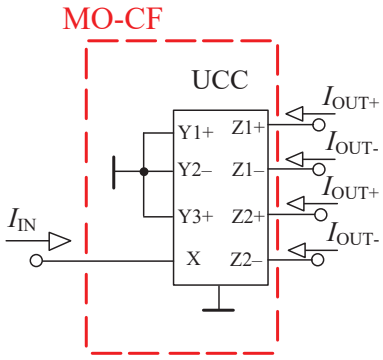


Fig. 3.7: Implementation of the MO–CF by the UCC

A CMOS model of the MOCF from [120] is another used solution.

The CCCII cell from [125] was used (implemented in the similar way as the UCC in Fig. 3.7) in proposals discussed in chapter 6 and the CF part of the structure of the IOGC–CA element in subsection 5.2.2.

A special case of a CF device has been used in the design of the fully differential version of the circuit presented in section 6.1. This special case is called a Fully–Differential Current Follower (FD–CF) [129]. The FD–CF element has a differential pair of current inputs and four or more current outputs offering copy of difference of input currents in specific polarity. The relations between the inputs and outputs of this element are given as:

$$I_{IN\_DIF} = I_{IN+} - I_{IN-}, \tag{3.5}$$

$$I_{OUT\_DIF} = I_{OUT+} - I_{OUT-}, \tag{3.6}$$

$$I_{OUT\_DIF} = 0.5 \cdot I_{IN\_DIF}, \tag{3.7}$$

where I_{IN_DIF} is the input differential current and I_{OUT_DIF} stands for the output differential current.

This element was created by the same CMOS simulation model as the MO–CF element with simple difference that the negative input is not grounded but used as the negative input (both inputs are forming differential pair) of the follower. In addition, the gain of the structure is set to 0.5 (differential gain). Figure 3.8 shows the schematic symbol of the FD–CF.

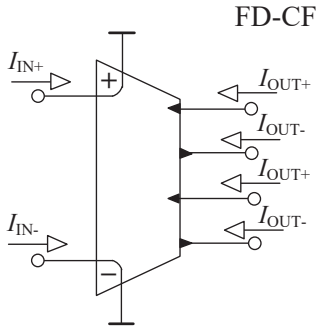


Fig. 3.8: Schematic symbol of the Fully–Differential Current Follower (FD–CF)

3.4 Adjustable Current Amplifier (ACA)

The ACA [121] element has one current input and one or more current outputs. The input current is copied to the outputs, but in comparison to the CF, the output current can be attenuated or amplified depending on the value of the current gain *B*. Figure 3.9 shows the schematic symbol of the ACA in its non–differential and differential form.

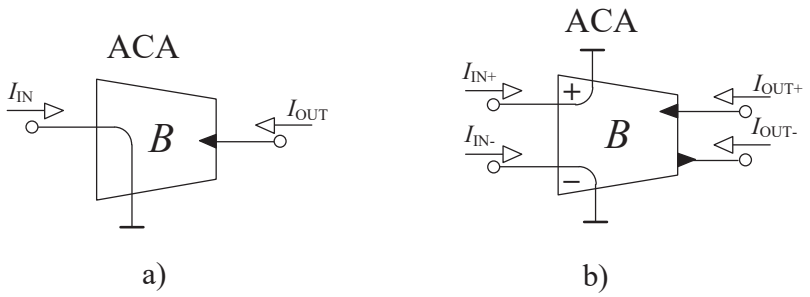


Fig. 3.9: Adjustable Current Amplifier (ACA): a) schematic symbol of the non–differential version, b) schematic symbol of the differential version

The non–differential ACA has single current input and single output, and its simple definition is given by the relation $I_{OUT} = B \cdot I_{IN}$. The differential version of the element has a differential pair of current inputs (following the same relation as in (3.5)) and at least two current outputs (relation (3.6)). The behavior of the differential ACA element is defined as:

$$I_{OUT\_DIF} = B(I_{IN+} - I_{IN-}) . \tag{3.8}$$

One of the used implementation of ACAs is done by EL2082 device [130] (also used in the internal structure of IOGC–CA element in some cases). This particular implementation is illustrated in Fig. 3.10. The current gain B of this solution is controlled through DC control voltage ($V_{SET\_B} \approx B$).

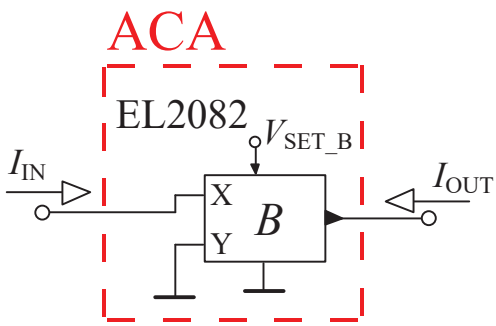


Fig. 3.10: Implementation of the ACA by the EL2082 IC

The CMOS model of the ACA element, as another solution, is presented in [121]. The current gain B of mentioned model is controlled by the DC current.

The last used solution of the ACA employs the MLT from [125] and one resistor as shown in Fig 3.11. The current gain B depends on the product of the value of resistor R and transconductance ($g_m \cdot R$) between the voltage input and current output of the MLT. Thus, the current gain can be controlled by DC control voltage V_{SET_B}.

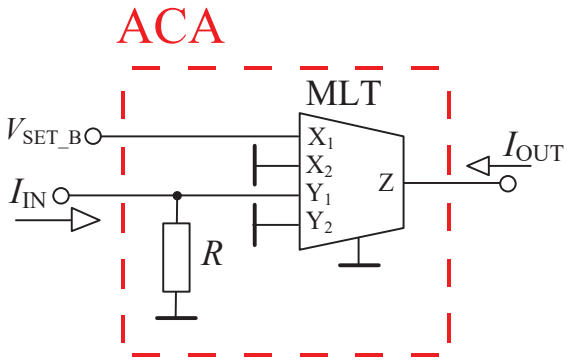


Fig. 3.11: Implementation of the ACA by the MLT and one resistor

3.5 Variable Gain Amplifier (VGA)

VGA operates as a voltage mode amplifier with variable voltage gain A. The schematic symbol of this element is provided in Fig. 3.12.

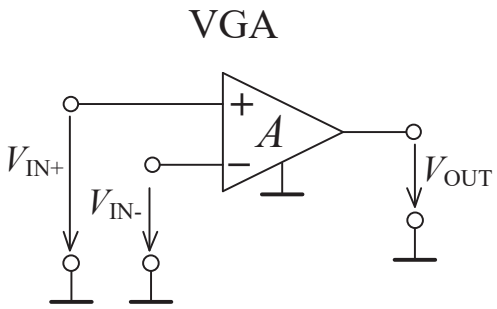


Fig. 3.12: Schematic symbol of the Variable Gain Amplifier (VGA)

The element has two voltage inputs and one voltage output. The relation between the terminals has form:

$$V_{OUT} = A(V_{IN+} - V_{IN-}). \tag{3.9}$$

The VGA can be also implemented by commercially available ICs VCA810 [131] and VCA822 [132] as presented in Fig. 3.13. Voltage gain A of this solution is controlled by DC control voltage V_{SET_A}. The dependence of gain on driving voltage has exponential character for VCA810 and linear form for VCA822.

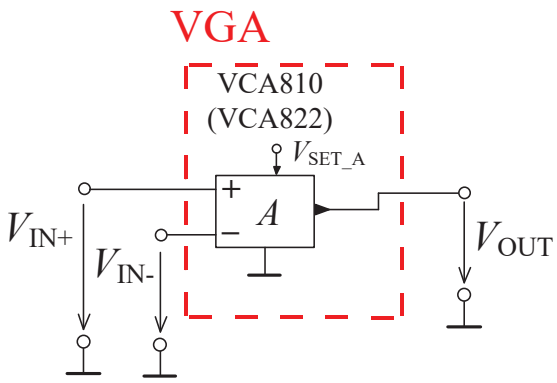


Fig. 3.13: Implementation of the VGA by the VCA810 or VCA822 device

Another possible solution employs the MLT and grounded resistor as depicted in Fig. 3.14. The resistor R at the output of the MLT is used to convert the output current to voltage. The resulting voltage gain A is defined by the product of the value of the resistor R and the transconductance of the MLT which can be adjusted electronically ($A = g_m \cdot R \cong V_{SET\_A} \cdot k \cdot R$, where k is specific transconductance constant of the MLT).

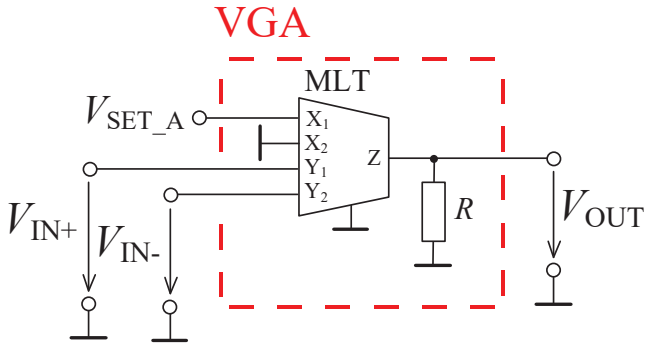


Fig. 3.14: Implementation of the VGA by the MLT and one resistor

The VGA element can be created by the CG–CCDDCC and one resistor using the same idea as in Fig. 3.14.

The design in subsection 5.1.2 utilizes the same interconnection as in Fig. 3.14. However, the proper function of the filter in subsection 5.1.2 requires the impedance separation of the node where the resistor R is connected to from rest of circuitry. This is solved by the additional VDDB as demonstrated in Fig. 3.15.

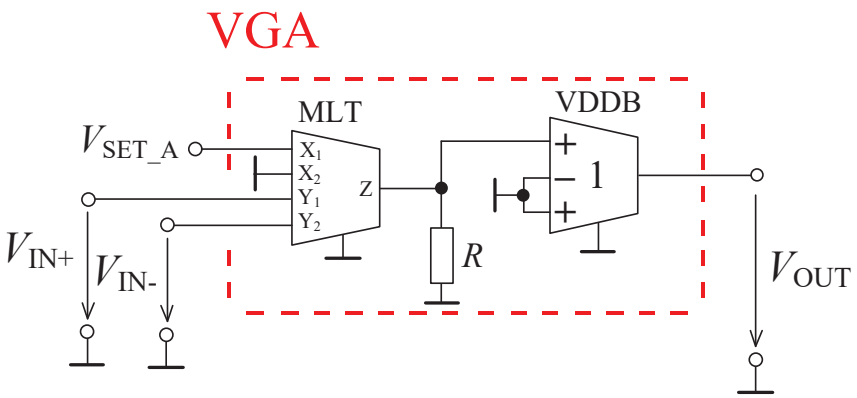


Fig. 3.15: Implementation of the VGA by the MLT, VDDB and one resistor

3.6 Voltage Differencing Transconductance Amplifier (VDTA)

VDTA element belongs to special advanced (offering multi-parameter adjustability) complex active elements. Its inner structure is created by composition of several (two in this case) elementary active elements (sub-blocks, cells). In case of the VDTA, two BOTAs are interconnected effectively. The schematic symbol of this element and its internal sub-block structure are depicted in Fig. 3.16 a), b), respectively.

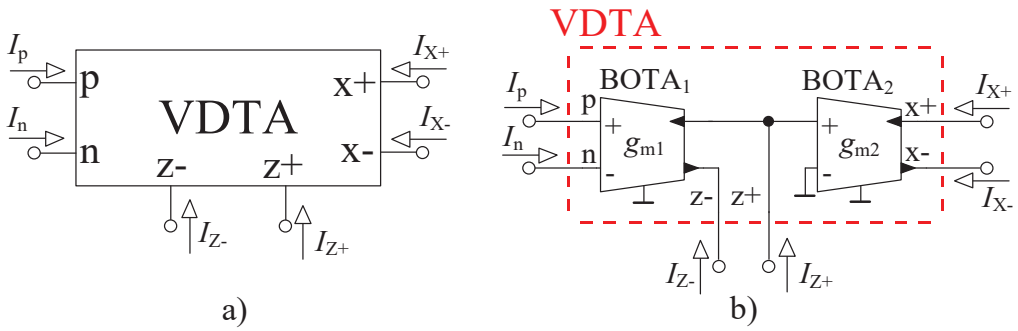


Fig. 3.16: Voltage Differencing Transconductance Amplifier (VDTA): a) schematic symbol, b) its inner structure created by two BOTA elements

The ideal behavior of the VDTA element is given by the following matrix of relations:

$$\begin{bmatrix} I_p \\ I_n \\ I_{Z+} \\ I_{Z-} \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{m1} & -g_{m1} & 0 & 0 \\ -g_{m1} & g_{m1} & 0 & 0 \\ 0 & 0 & g_{m2} & 0 \\ 0 & 0 & -g_{m2} & 0 \end{bmatrix} \cdot \begin{bmatrix} V_p \\ V_n \\ V_{Z+} \\ V_{Z-} \end{bmatrix}. \tag{3.10}$$

Due to the presence of two OTAs, the VDTA offers two controllable parameters (two transconductances). The particular implementation of OTAs of the inner structure of VDTA has been discussed in chapter 3.2. The structure of the VDTA has been partially modified for the filter in subsection 5.4.1. This modification consists of the first OTA (input part of VDTA) in a cascade being implemented by a multiple output element (MOTA). This modification offers one additional negative Z output (Z– in this case). Furthermore, the negative input of the second OTA is not grounded (as in standard case) but used as a negative input (labeled as v in given chapter).

3.7 Voltage Differencing Current Conveyor (VDCC)

The next used complex advanced active element is a Voltage Differencing Current Conveyor (VDCC) [106]. The VDCC is created by the single OTA sub-block and single CCII sub-block. Figure 3.17 shows the schematic symbol and simplified inner concept of this element.

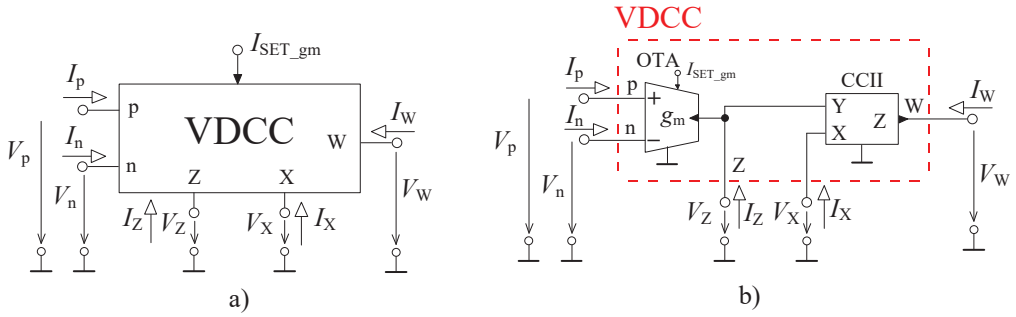


Fig. 3.17: Voltage Differencing Current Conveyor (VDCC): a) schematic symbol, b) its inner structure created by one OTA and one CCII

This element has four high impedance terminals (p, n, Z, W) and one low impedance input terminal (X). The VDCC was used in the design of the filter presented in subsection 5.2.2. The VDCC can be expressed by the following matrix:

$$\begin{bmatrix} I_p \\ I_n \\ I_Z \\ V_X \\ I_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_p \\ V_n \\ V_Z \\ I_X \end{bmatrix}. \tag{3.11}$$

3.8 Controlled–Gain Current–Controlled Differential Difference Current Conveyor (CG–CCDDCC)

So–called Controlled–Gain Current–Controlled Differential Difference Current Conveyor (CG–CCDDCC) [49] is name for the last advanced active element applied in this thesis (Fig. 3.18). This device originates from a Current–Controlled Differential Difference Current Conveyor (CCDDCC) [112].

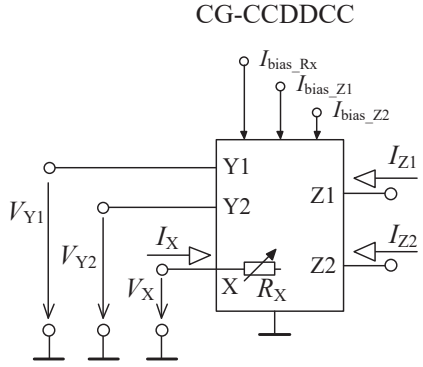


Fig. 3.18: Schematic symbol of the Controlled–Gain Current–Controlled Differential Difference Current Conveyor (CG–CCDDCC)

The CG–CCDDCC has one low–impedance current input, two high–impedance voltage inputs and two high–impedance current outputs. The CG–CCDDCC offers the electronic control of its intrinsic input resistance R_X and electronic control of current gain B of the both current outputs independently by DC bias currents. The principle of CG–CCDDCC can be described by the following relations:

$$V_{Y1} - V_{Y2} = V_X - R_X I_X, \tag{3.12}$$

$$I_{Z1} = B_a I_X, \tag{3.13}$$

$$I_{Z2} = -B_b I_X, \tag{3.14}$$

where B_a and B_b represent independent current gain of each output.

The internal sub-block structure of this element employs six OTA elements interconnected as depicted in Fig. 3.19. The detailed design of CG–CCDDCC and its transistor level model can be found in [49].

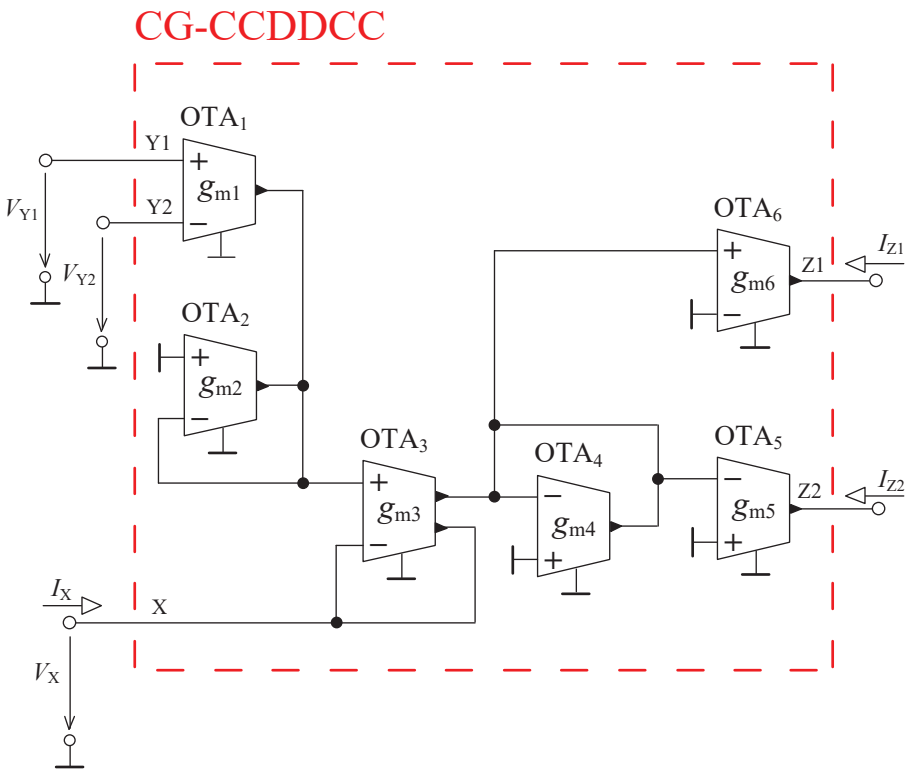


Fig. 3.19: Inner structure design of the CG–CCDDCC consisting of six OTAs

4 Methodology

This chapter focuses on the principle of the reconnection–less reconfiguration and the description of suitable methods applied for the design of reconnection–less (switchless) reconfigurable filters presented in the following chapter.

4.1 Reconnection–less reconfiguration

The proposal (of reconnection–less reconfigurable filters) usually starts with the establishment of the demands and subsequent formulation of the resulting transfer function of the synthesized filter. The reconnection–less reconfigurable structures are designed having one input and one output (SISO structures). Switching or mechanical (connector, probe, etc.) interchange between individual nodes (inputs, outputs) or further topological modifications of the structure are not allowed. Therefore, all reconnection–less reconfigurable filters are designed as SISO type (purpose) or originating from structures with single input and multiple outputs (SIMO), multiple inputs and single output (MISO), or both multiple inputs and outputs (MIMO) which have capability to be turned into a SISO type structure (as discussed later in section 4.3). As mentioned earlier, the reconnection–less reconfiguration is achieved through the setting of electronically tunable parameters which are used to change the transfer function (output response). These suitable adjustable parameters are intentionally integrated in the transfer function and serve for the cancelation of selected terms (coefficients) of the transfer function (when specific value of the parameter leads into cancellation of the coefficient). As an example, we have the following equation:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{s}^2 C_1 C_2 B_3 - \boldsymbol{s} C_2 g_{m1} B_2 + g_{m1} g_{m2} B_1}{\boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m1} + g_{m1} g_{m2}}. \tag{4.1}$$

This equation represents the current–mode transfer function of the filter from subsection 5.4.1. In this case, the $\boldsymbol{s}^2$ term can be intentionally influenced by current gain B_3, term $\boldsymbol{s}^1$ by B_2 and term $\boldsymbol{s}^0$ by B_1. Note that the parameters for the reconfiguration are only part of the numerator and they are not required (suitable to be present) in the denominator (physical realization and stability aspects). Each term of the numerator can be canceled if adjustable current gain (in case of (4.1)) is set to zero, while the denominator of the transfer function remains unchanged. It is also possible for the term being canceled in different manner than setting the control parameter to zero (e.g., -1, 0.5, 2, etc.) depending on the form of the transfer function (composition of individual terms of the numerator). The denominator should be independent on parameters serving for the reconfiguration since the setting these parameters to zero would change the general character (order) of the filter or it may result even into stability issues. The cancelation of a responsibly selected term in the denominator can be used in specific cases in order to obtain a transfer function of a different (decreased) order (reconfiguration of the magnitude response in slope) as shown for filters in subsections

5.1.1 and 5.1.2 (obtainment of transfer functions of the 1st–order from general structure of the 2nd–order).

As discussed, the reconnection–less reconfiguration is usually achieved by the cancelation of the terms (coefficients) of the numerator. For another example, let us have the equation:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{s}^2 C_1 C_2 A - \boldsymbol{s} C_2 g_{m1} + g_{m3} g_{m4}}{\boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m2} + g_{m3} g_{m4}}. \tag{4.2}$$

The transfer function belongs to the filter presented in subsection 5.1.2. The setting of the term $\boldsymbol{s}^1$ is done by transconductance g_{m1} as the corresponding term in the denominator is actually using a different parameter (g_{m2}). However, the cancelation of the $\boldsymbol{s}^0$ term cannot be done since it is identical with the term of the denominator and setting g_{m3} or g_{m4} to zero would change the general character of the filter. Thus, the $\boldsymbol{s}^0$ term cannot be canceled. It would be available by an additional parameter contained in the $\boldsymbol{s}^0$ term of the numerator (g_{m5}, for example) but not in this case. As a result, the reconfiguration is typically done by the parameters contained in forward transfer branches of the multiple-loop topology not in the main path of integrators of the filter or the feedback paths as these transfers determine the form of the denominator.

The last part worth mentioning is that the parameters used for the reconnection–less reconfiguration do not necessarily have to be either on or off (set to zero or unity gain in case of voltage/current gain, for instance). A proper implementation of the specific active elements offers the analogue adjustment of discussed features (continuous control). It provides a useful advantage of fine–tuning compensation of undesired gain shift (attenuation) of the resulting output response, for instance. Another advantage relates with level adjustment of stop–band/pass–band area of available transfer functions offering the obtainment of special responses such as HPZ and LPZ.

Consequently, there are various types of the reconnection-less reconfiguration: 1) reconfiguration of the numerator resulting in the change of the output response (most common type of the reconfiguration), 2) reconfiguration of the denominator resulting in the change of the slope of the response (change of the order), 3) reconfiguration of the denominator resulting in the change of the general function of the circuit (change between circuit operating as a filter and oscillator by cancelation of the linear term of the denominator, for instance). Furthermore, special cases of the reconnection-less reconfiguration can be considered: 4) reconfiguration resulting in the change of the approximation of the filter (Butterworth, Cauer, Chebyshev, etc.), 5) reconfiguration resulting in the change of the fractional order of the output response (either by the FOE or by change of the values of the topology parameters based on a suitable FO approximation). If the denominator is being changed, it is necessary to consider possible stability issues.

4.2 Method of unknown nodal voltages (MUNV)

MUNV [105] is a well–known approach for the symbolic analysis and synthesis of the linear analogue circuitry. It is based on a system of linear equations (I. Kirchhoff's law) $\mathbf{Y}\cdot\mathbf{V} = \mathbf{I}$, where $\mathbf{Y}$ is a square admittance matrix, $\mathbf{V}$ stands for a column vector of unknown nodal voltages, and $\mathbf{I}$ is designated for a column vector of excitation current sources. If we consider that the designed circuit has three independent nodes and one excitation source, in order to obtain a SISO type filter, it leads to a 3x3 $\mathbf{Y}$ matrix. The matrixes of higher dimensions are theoretically possible. However, the hand calculation (sub-determinants and algebraic complements for Laplace expansion based on selected column or row) has many practical difficulties, for higher number of nodes than 3 especially. Hand-calculations of MUNV-based theoretical filtering concepts of the proposed filters were used for the synthesis. More complex systems that use more than 3 nodes require suitable mathematical tools (Matlab, Mathcad).

The general MUNV matrix of a circuit with three independent nodes and one excitation source has the following form:

$$\begin{pmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}. \tag{4.3}$$

Considering the first node of the circuit as the voltage input and the third node as the voltage output, the transfer function is $K(\mathbf{s}) = V_{OUT}/V_{IN} = V_3/V_1 = \Delta_{1,3}/\Delta_{1,1}$. The determinants $\Delta_{1,1}$ and $\Delta_{1,3}$ are defined by the following form:

$$\Delta_{1,1} = Y_{22}Y_{33} - Y_{32}Y_{23} = b_2\mathbf{s}^2 + b_1\mathbf{s} + b_0, \tag{4.4}$$

$$\Delta_{1,3} = Y_{21}Y_{32} - Y_{31}Y_{22} = a_2\mathbf{s}^2 + a_1\mathbf{s} + a_0. \tag{4.5}$$

Fulfilment of this definition in the 2nd–order (and the 3x3 matrix) supposes one of the working capacitors connected between two nodes (must be floating). Both grounded capacitors (presented in 2nd-order reconfigurable filter) result into the structure consisting of several additional nodes leading to a matrix of higher rank. A possible result of the MUNV–based design (selected example) is given by the following matrix:

$$\begin{pmatrix} \mathbf{s}C_1 & 0 & -\mathbf{s}C_1 \\ -g_{m2}A & \mathbf{s}C_2 & g_{m2} \\ -\mathbf{s}C_1 + g_{m3} & -g_{m1} & \mathbf{s}C_1 + g_{m1} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}. \tag{4.6}$$

This exemplary matrix corresponds with the matrix of the filter introduced in subsection 5.1.1 which is depicted in Fig. 4.1. Note that the resulting structure has four independent nodes (due to the presence of voltage gain A). Node 4 has been added later after the initial MUNV design for an advantageous option of the additional reconfiguration. This modification will adjust the operation of OTA2 as follows $(V_3 - A \cdot V_1) \cdot g_{m2}$, where V_1 and V_3 stand for the nodal voltages of nodes 1 and 3 (you can notice this specific operation has been already included in (4.6) in first column, second row cell).The resulting structure can be easily created from the matrix in regard to the position of individual parameters in rows and columns denoting the relation between the nodes of the topology. For instance, parameter g_{m1} in the second column and the third row tells us that the filter topology will have the OTA_1 (g_{m1}) connected by input terminal (negative) from node 2 to node 3 with a minus sign as evident from Fig. 4.1 (dark green circle).

$$\Delta_{1,1} = Y_{22}Y_{33} - Y_{32}Y_{23} = b_2 s^2 + b_1 s + b_0 = s^2 C_1 C_2 + sC_2 g_{m1} + g_{m1} g_{m2} =$$
$$= (sC_2)(sC_1 + g_{m1}) - (-g_{m1} g_{m2})$$

$$\Delta_{1,3} = Y_{21}Y_{32} - Y_{31}Y_{22} = a_2 s^2 + a_1 s + a_0 = s^2 C_1 C_2 - sC_2 g_{m3} + g_{m1} g_{m2} =$$
$$= (-g_{m2})(-g_{m1}) - [(-sC_1 + g_{m3})(sC_2)]$$

$$\begin{pmatrix} sC_1 & 0 & -sC_1 \\ -g_{m2}A & sC_2 & g_{m2} \\ -sC_1 + g_{m3} & -g_{m1} & sC_1 + g_{m1} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}$$

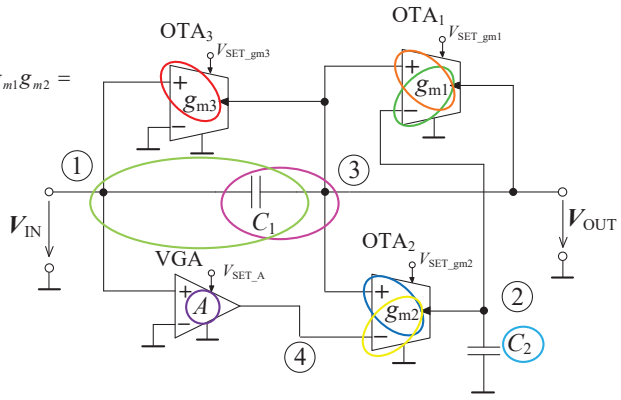


Fig. 4.1: Example of the resulting circuit created by MUNV

4.3 Modification of existing structures

Most of the filtering structures, which offer multiple transfer functions, are of SIMO, MISO or MIMO type when, for a desired function, a specific input/output or a suitable combination of multiple inputs/outputs is used. Nevertheless, reconnection–less reconfigurable features can be obtained and generated as a modification of these structures. This new feature of topology results from addition of adjustable (advanced) active elements to specific position of topology in previously proposed SIMO, MISO or MIMO filters when the final structure has one input and one output. A possible approach is presented in [133]. Based on the topology, this modification can be divided into input distribution depicted in Fig. 4.2 (distribution of the input signal into different nodes of the structure) for MISO structures and output summation shown in Fig. 4.3 (summation of the signal responses from different nodes of the structure) for SIMO structures.

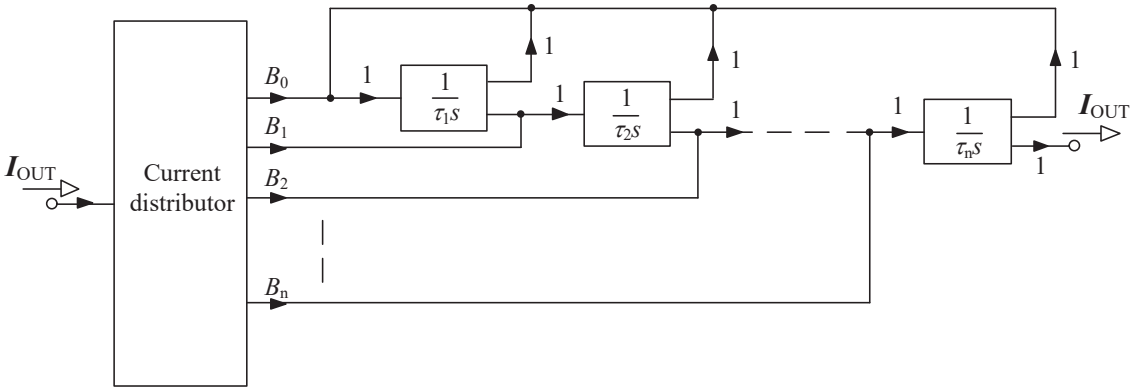


Fig. 4.2: Demonstration of the input distribution in case of a block diagram of a general CM FLF topology

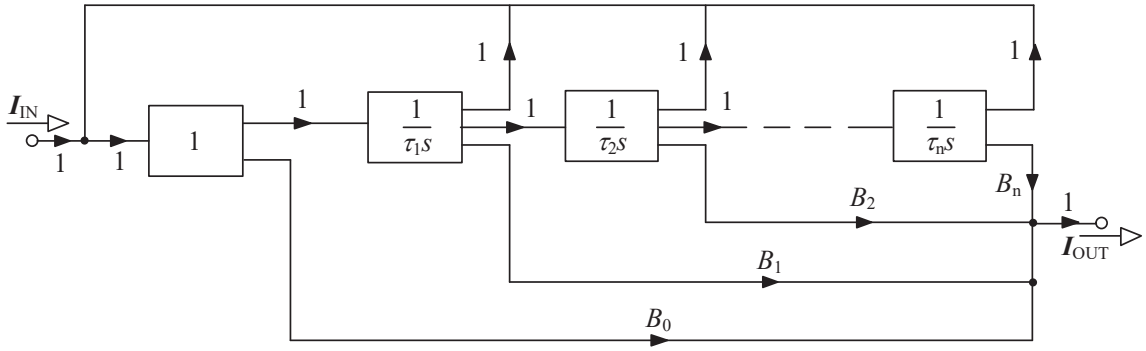


Fig. 4.3: Demonstration of the output summation in case of a block diagram of a general CM FLF topology

From the operational mode of the filter point of view, it is evident that the output summation is more favorable for the current mode (currents can be easily summed together in a node without a necessity of an additional active element(s)). On the other hand, the input distribution requires to create copies of the input current by a CF(s). The input distribution has significant advantages in case of the voltage mode where the input voltage can be taken from one node (by voltage follower/buffer(s) when low-impedance terminal is not available) in comparison to the summation of voltages that requires at least additional active element for this operation. Nonetheless, both approaches are available for CM and VM alike.

4.4 VM to CM transformation

Other possible technique of the reconnection–less reconfigurable filter design targets the transformation of these filters from their VM form into the CM form (alternative) [134]. Circuits working in the current mode can, in comparison to their VM counterparts, offer possible advantages such as lower power consumption, better signal–to–noise ratio and wider bandwidth operational range, in particular cases [105]. The general idea of the VM to CM transformation involves swapping the input and output of the circuit. All active elements within the structure have to be mirrored in inputs and outputs direction. This can be easily

done when OTA elements are used (they work in mixed mode – current output/voltage input). The elements operating in VM only (high impedance voltage input/low impedance voltage output) have to be replaced by their CM counterpart (VGA replaced by ACA, for example) and vice versa. Some voltage polarity change (or current orientation) might be necessary for the newly created circuit alternative (having corresponding transfer function as its counterpart working in the other mode) and to be stable.

Specific example of the VM to CM transformation is given by Fig. 4.1 and Fig. 4.4. Figure 4.4 represents the CM reconnection–less reconfigurable filter described in subsection 5.3.2 created by the transformation of the VM reconnection–less reconfigurable filter shown in Fig. 4.1 which has been introduced in subsection 5.5.1. The number of used OTA elements remains the same. If both inputs of the OTA were used (in the VM filter), the OTA in the CM topology has now two outputs (of the opposite polarity) thus, OTA_1 and OTA_2 turn into $BOTA_1$ and $BOTA_2$, OTA_3 turns into OTA. The designation of the transconductances (in subsection 5.3.2) has been renumbered for easier presentation of given filter. The VGA element has been replaced by the ACA. One additional ACA has been added to the CM topology in subsection 5.3.2 for the sake of an additional feature of reconfiguration option of the CM filter.

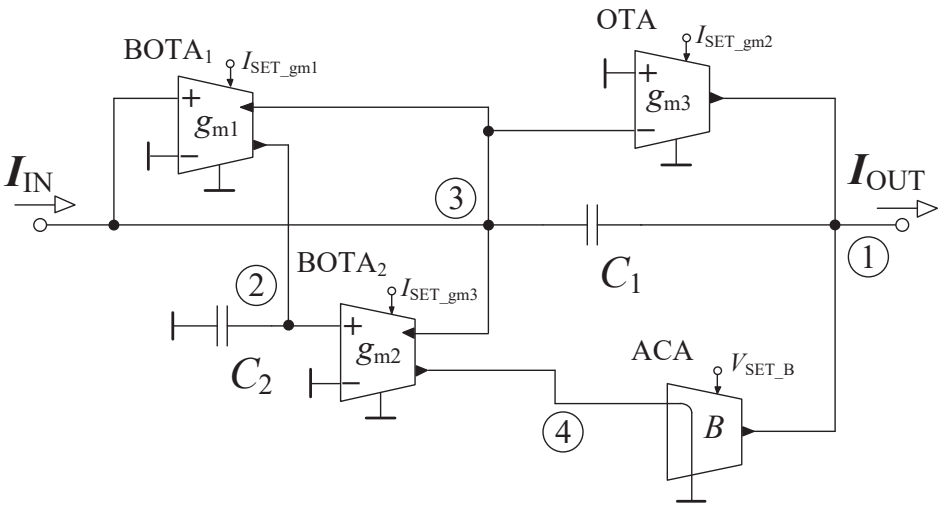


Fig. 4.4: CM reconnection–less reconfigurable filter created by the VM to CM transformation of the filter from Fig. 4.1

4.5 Signal flow graph (SFG) method

Signal flow graph (SFG) method provides an easy way for the analysis and synthesis of linear circuits. It allows clear insight into to the topological principle of operation of the system. This approach has been firstly introduced by S. J. Mason (so–called Mason's graphs [135]) for the purpose of the solution of linear algebraic sets. A few years later, Coates' graphs [136] were introduced. Nowadays, so–called mixed Mason–Coates (M–C) graphs

[137] are also used. The MC graphs combine some features of both mentioned approaches. These graphs represent a set of nodes and directed branches between them graphically and illustratively. The nodes symbolize variables, and the branches define the relationship between the nodes. The transfer function is then calculated using the Mason's gain formula given by equation:

$$K = \frac{1}{\Delta}\sum_{i} P_i \Delta_i \,, \tag{4.7}$$

where P_i represents the gain of i^{th} forward path and Δ is a determinant of the graph which is expressed as:

$$\Delta = P - \sum_{l} P_1^{(l)} \Delta_1^{(l)} + \sum_{m} P_2^{(m)} \Delta_2^{(m)} - \sum_{n} P_3^{(n)} \Delta_3^{(n)} + \cdots, \tag{4.8}$$

where P stands for self–loop products, $P_1^{(l)}$ means individual loop gains, $P_2^{(m)}$ represent products of two non–touching loops, $P_3^{(n)}$ give products of three non–touching loops, $\Delta_1^{(l)}$, $\Delta_2^{(m)}$ and $\Delta_3^{(n)}$ are loop gain terms which do not touch the l^{th}, m^{th} and n^{th} forward paths and so on.

An example of a SFG for Leap-frog topology [138] can be seen in Fig. 4.5 (after the elimination of the self–loops for easier calculation since all determinants are now equal to 1). This graph represents the design of the filter presented in subsection 5.5.2.

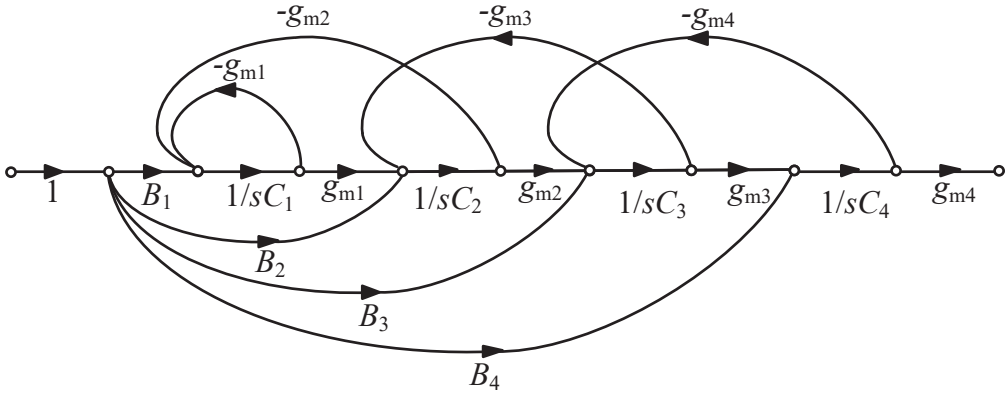


Fig. 4.5: Simplified signal–flow graph of the filter proposed in subsection 5.5.2

The denominator of the transfer function of the graph from Fig. 4.5 is calculated as:

$$D(\boldsymbol{s}) = 1 - \left(L_1 + L_2 + L_3 + L_4\right) + L_1L_4 + L_2L_4 + L_1L_3 =$$
$$= 1 - \left(-\frac{g_{m1}}{\boldsymbol{s}C_1} - \frac{g_{m1}g_{m2}}{\boldsymbol{s}C_1\boldsymbol{s}C_2} - \frac{g_{m2}g_{m3}}{\boldsymbol{s}C_2\boldsymbol{s}C_3} - \frac{g_{m3}g_{m4}}{\boldsymbol{s}C_3\boldsymbol{s}C_4} \right) +$$
$$+ \left[-\frac{g_{m1}}{\boldsymbol{s}C_1} \cdot \left(-\frac{g_{m3}g_{m4}}{\boldsymbol{s}C_3\boldsymbol{s}C_4} \right) \right] + \left[-\frac{g_{m1}g_{m2}}{\boldsymbol{s}C_1\boldsymbol{s}C_2} \cdot \left(-\frac{g_{m3}g_{m4}}{\boldsymbol{s}C_3\boldsymbol{s}C_4} \right) \right] + \tag{4.9}$$
$$+ \left[-\frac{g_{m1}}{\boldsymbol{s}C_1} \cdot \left(-\frac{g_{m2}g_{m3}}{\boldsymbol{s}C_2\boldsymbol{s}C_3} \right) \right] = \boldsymbol{s}^4C_1C_2C_3C_4 + \boldsymbol{s}^3C_2C_3C_4g_{m1} + \boldsymbol{s}^2C_3C_4g_{m1}g_{m2} +$$
$$+ \boldsymbol{s}^2C_1C_4g_{m2}g_{m3} + \boldsymbol{s}^2C_1C_2g_{m3}g_{m4} + \boldsymbol{s}C_2g_{m1}g_{m3}g_{m4} + \boldsymbol{s}C_4g_{m1}g_{m2}g_{m3} +$$
$$+ g_{m1}g_{m2}g_{m3}g_{m4}$$

The numerator of the transfer function is given as:

$$N(\boldsymbol{s}) = \boldsymbol{s}^3C_1C_2C_3g_{m4}B_4 + \boldsymbol{s}^2C_1C_2g_{m3}g_{m4}B_3 + \boldsymbol{s}^2C_2C_3g_{m1}g_{m4}B_4 +$$
$$+ \boldsymbol{s}C_3g_{m1}g_{m2}g_{m4}B_4 + \boldsymbol{s}C_2g_{m1}g_{m3}g_{m4}B_3 + \boldsymbol{s}C_1g_{m2}g_{m3}g_{m4}B_4 + \tag{4.10}$$
$$+ \boldsymbol{s}C_1g_{m2}g_{m3}g_{m4}B_2 + g_{m1}g_{m2}g_{m3}g_{m4}B_4 + g_{m1}g_{m2}g_{m3}g_{m4}B_2 +$$
$$+ g_{m1}g_{m2}g_{m3}g_{m4}B_1 + g_{m1}g_{m2}g_{m3}g_{m4}B_3$$

The final circuit structure (Fig. 4.6) can be easily generated from the created M–C graph.

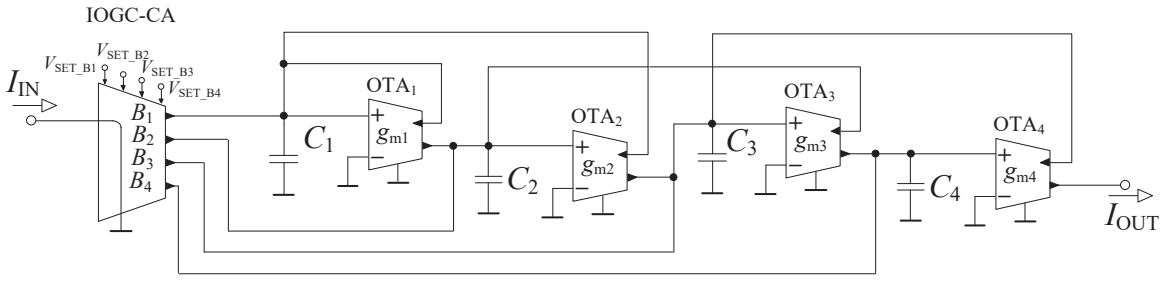


Fig. 4.6: The circuit structure created based on the graph in Fig. 4.5

4.6 Higher order filter design

The last method, discussed in this work, solves filters of high orders (3 and more) [139]. Despite a possibility to design these filters directly (by a direct design of higher order topology and obtainment of coefficients), a cascade combination (of individual filters or basic building blocks) [140] is being commonly used for the design of filters of higher orders. In case of cascade synthesis, filters of the 1st and 2nd order are typically combined when the value of the pole frequency and quality factor of these partial filters can be transformed as the pole frequency and quality factor of the resulting structure and vice versa [140]. Advantageous features of each block of cascade having specific characteristics of the

impedances (CM filters having low input impedances and high output impedances and vice versa for the VM filters) offer good performance for interconnection with application. In order to obtain a desired value of the pole frequency, quality factor, etc., and the resulting filtering response having the desired approximation (Butterworth characteristics, for instance), the individual coefficients of the transfer function have to be calculated in dependence on these parameters. These specific values of coefficients of transfer function yield from tables of normalized values in many books ([140], for instance) or can be gained by a sophisticated designs tools (Filter Solution [141], NAF [142], etc.). The parameters of the tolerance field such as the pole frequency, transfer in pass-band K_P, the stop-band frequency f_S and transfer in stop-band K_S (LP tolerance filed shown in Fig. 4.7) together with the desired approximation are inputs of these SW tools. The example of coefficients (evaluated by the design SW tool and used for the calculation of the filter in subsection 5.5.1) are given as follows:

$$\begin{aligned} b_3 &= 1, \\ b_2 &= 5.995 \cdot 10^5, \\ b_1 &= 1.797 \cdot 10^{11}, \\ b_0 &= 2.694 \cdot 10^{16}. \end{aligned} \tag{4.11}$$

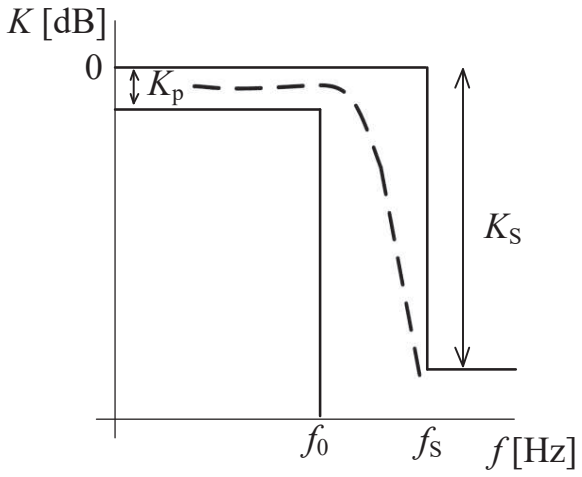


Fig. 4.7: Tolerance field in case of LP transfer function

5 Design of Reconnection–less Reconfigurable Filtering Structures

My research results for the topic of reconnection–less reconfigurable filtering structures are described in this chapter. All proposals are verified using the SNAP [143], (SNAP version 3.0) as the first step. The further simulations of the proposed structures are performed in OrCAD program in version 16.6 (subsections 5.2.1, 5.3.2, 5.4.1, 5.5.1 and 5.5.2) and Cadence IC6 (virtuoso editors and spectre simulator) software (subsections 5.1.1, 5.1.2, 5.2.2 and 5.3.1). Furthermore, the designs in subsections 5.5.1 and 5.5.2 are complemented with experimental measurements. Concepts and principles of all active elements (for purposes of simulations as well as experimental testing) used in the design have been described in chapter 3. The measurements are performed using a vector network analyzer Agilent 4395A and voltage–to–current, current–to–voltage converters based on OPA860 [144] and OPA861 [145] (commercially available ICs). All proposed filters in this thesis work in the current mode with exception of filters in section 5.1 which work in the voltage mode. The filter in 5.4.1 operates in both CM and VM. The following concept of the representation of results has been used (unless stated otherwise): when comparing the theoretical expectations and simulations results, the theory is represented by black dashed traces while colored traces represent the simulation results (that applies for chapter 6 as well). Furthermore, when comparing simulations and experimental results, the simulations are represented by black dashed traces and the experimental results by colored traces. Figure 5.1 illustrates the block diagram of the measurement setup (for measurement of current–mode filters). The measurement setup for VM filters has the identical arrangement but without converters. Implemented V–I and I–V converters use simple principle of a suitable connection of a CCII. The V–I converter (Fig. 5.2 a)) has the input voltage connected to the voltage input node of the CCII and this voltage is converted to the output current through the resistor connected to the current input node. The function of the I–V converter (Fig. 5. 2 b)) is analogical. The current from the output of the proposed filter is connected to the current input of the CCII (working as a current follower) and mirrored to the current output terminal of the CCII. The output current is then transferred to voltage through the resistor. A voltage buffer (available in the package of OPA860 together with the CCII) connected to the output of the converter provides the impedance separation (due to 50 Ω input impedance of analyzer). All simulation and experimental results presented in the thesis are influenced by real properties and parasitic characteristics of used active elements. It causes deviation from theoretical expectations and limitations of the operational bandwidth where proposed circuits work properly.

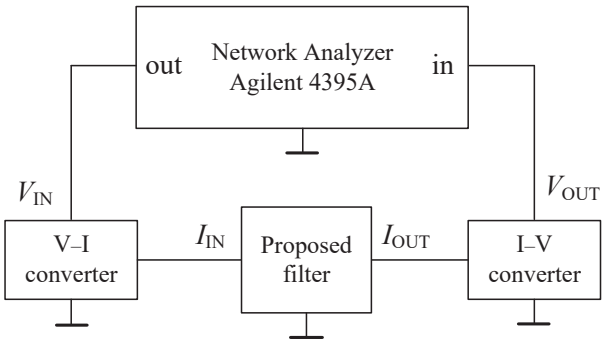


Fig. 5.1: Block diagram of the measurement setup (in case of CM filters)

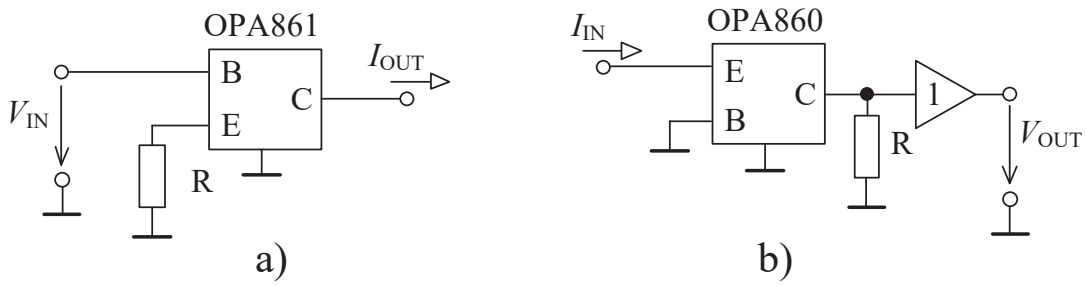


Fig. 5.2: Basic principles of the used converters: a) principle of the V–I converter, b) principle of the I–V converter

Section 5.1 describes the design of reconnection–less reconfigurable filters using MUNV. The first filter consists of three OTAs and one VGA. The filter is also complemented with an RC structure to work as 1+α FO filter in further studies. The second filter uses two VDTAs and one VGA for its function. The following section deals with the design of reconnection–less reconfigurable filters based on modifications of previously published MISO type filtering structures. Subsection 5.2.1 presents a modification of a filter based on two VDTAs and subsection 5.2.2 described a modification of a filter with one VDCC. Reconnection–less reconfigurable filters using CG–CCDDCCs (subsection 5.3.1), OTAs and ACAs (subsection 5.3.2), created by voltage mode to current mode (adjoint) transformation (and modification), of previously published reconnection–less reconfigurable filters, are introduced in section 5.3. Section 5.4 introduces a reconnection–less reconfigurable filter designed by signal flow graph method implementing one VDTA, one CF, three VGAs, three ACAs, one grounded capacitor and one virtually grounded capacitor [146]. The filter operates in both modes (current mode and voltage mode). The final section of this chapter presents reconnection–less reconfigurable filters of high orders (3rd and 4th order). The numerical design for these filters has been performed by the NAF tool [142] designed to calculate individual coefficients of the transfer function in dependence on the desired order of the filter, selected parameters and used approximation. Both designs contain OTAs, and a current amplifier introduced in subsection 6.1.1. The filter in subsection 5.5.1 is based on a 3rd–order topology and provides functions of the 1st, 2nd and 3rd order while subsection 5.5.2 illustrates

a 4th–order structure offering functions of LP of 1st, 2nd, 3rd and 4th order and also reconfigurable slope of fractional–order transfer characteristics (after a suitable modification). This solution is also supported by the stability analysis [147]. The stability analysis itself was carried out using a Matlab script assimilating the mathematical procedure introduced in [148]. Furthermore, the chosen filters are complemented with the sensitivity analysis [105] of selected transfer functions.

The differences between the theoretical expectations, simulation results and the experimental results are mainly given by the parasitic/real characteristics of used simulation models and fabricated chips used in case of experimental implementation, respectively. The effect of real part of input and output impedances (that they are not high or low enough in comparison to the ideal impedances which are infinite or zero based on specific input/output) impacts the stop–band area of available transfer functions. These values influence the maximal attenuation levels in stop–band area (the magnitude trace does not follow the expected slope of attenuation but rather stay at specific value of attenuation – parasitic zero created). The (magnitude and phase) characteristics at lower frequencies are mainly affected by the real characteristics of the output (current) impedances of the active elements. Similarly, the differences at higher frequencies are mainly caused by the influence of the real characteristics of the input (current) impedances and bandwidth limitation of the chips (up to tens of MHz). The measured results are also affected by the features of used V–I/ I–V converters (theoretically compensated by the calibration) and by the features (signal to noise ratio) of used vector network analyzer (around -80 dB). These fact apply for all presented results (chapter 5 and 6). These issues can be mostly eliminated by more suitable implementation of suitable active elements with substantially higher/lower values (closer to the ideal features) of terminal resistances (significant issue in modern miniaturized low–voltage and low–power CMOS processes without cascading especially). Furthermore, the effect of parasitic capacitances (in case of undesired pole frequency shift of proposed filters) should be negligible in comparison to the chosen values of the working capacitors (chosen high enough (usually around 1 nF)). In addition, any possible significant frequency shift (caused by parasitic capacitances) can be easily compensated by the adjustment of the values of transconductances (if OTAs do allow the electronic adjustment of transconductances).

5.1 Structures designed by MUNV

The designed structures are based on 3x3 admittance matrix using OTAs and VGAs as building blocks. One of the working capacitor of both presented filters is floating (both filters are of the 2nd–order thus, they require two capacitors) as a result of used matrix dimensions.

5.1.1 Structure with three OTAs and one VGA

The proposed filter offers the 2nd–order functions (HP, BS, AP) and also HP transfer function of the 1st–order as well as direct transfer between the input and output of the filter.

The pass–band/stop–band region at lower frequencies can be easily adjusted (therefore, the filter also offers HPZ function). Furthermore, the filter has capability of the electronic adjustment of its pole frequency. Moreover, the proposed structure is later complemented with the FOE in order to confirm the suitability of the structure for the fractional–order filter design. The proposed filter is published in [149] (Elektronika ir Elektrotechnika (ISSN 1392–1215), 2019).

Design proposal

We start the design by the expectation of the resulting transfer function which is then used for the circuit synthesis. The desired transfer function is described as:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{s}^2 C_1 C_2 - \boldsymbol{s} C_2 g_{m3} + g_{m1} g_{m2} A}{\boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m1} + g_{m1} g_{m2}}. \tag{5.1}$$

In this case, we consider that the designed circuit has three independent nodes and one excitation source. The MUNV matrix of such circuit has the following form:

$$\begin{pmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}. \tag{5.2}$$

For the simplicity of the proposal and easier calculation, we will omit voltage gain A in (5.1) for now (the circuit would have four independent nodes). Considering the proposed structure with capacitor C_1 between nodes 1 and 3 and capacitor C_2 connected to node 2, the relation (5.2) turns into:

$$\begin{pmatrix} \boldsymbol{s} C_1 & 0 & -\boldsymbol{s} C_1 \\ 0 & \boldsymbol{s} C_2 & 0 \\ -\boldsymbol{s} C_1 & 0 & \boldsymbol{s} C_1 \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}. \tag{5.3}$$

In order to obtain the same transfer functions as in (5.1) and supposing $K(\mathbf{s}) = V_{OUT}/V_{IN} = V_3/V_1 = \Delta_{1,3}/\Delta_{1,1}$, determinants $\Delta_{1,1}$ and $\Delta_{1,3}$ have to be in form of (back operation expressing partial components of final products of sub-determinant calculation – these partial components indicate coordinates/positions of g_ms in **Y** matrix and, therefore, also nodal connection of OTAs in the circuit topology):

$$\begin{aligned} \Delta_{1,1} &= Y_{22} Y_{33} - Y_{32} Y_{23} = b_2 \boldsymbol{s}^2 + b_1 \boldsymbol{s} + b_0 = \boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m1} + g_{m1} g_{m2} = \\ &= \boldsymbol{s} C_2 \left(\boldsymbol{s} C_1 + g_{m1} \right) - \left(-g_{m1} g_{m2} \right) \end{aligned}, \tag{5.4}$$

$$\Delta_{1,3} = Y_{21}Y_{32} - Y_{31}Y_{22} = a_2\boldsymbol{s}^2 + a_1\boldsymbol{s} + a_0 = \boldsymbol{s}^2C_1C_2 - \boldsymbol{s}C_2g_{m3} + g_{m1}g_{m2} = \\ = \left(-g_{m2}\right)\left(-g_{m1}\right) - \left[\left(-\boldsymbol{s}C_1 + g_{m3}\right)\boldsymbol{s}C_2\right] \quad . \tag{5.5}$$

Supplementing (5.4) and (5.5) in form of sum of products (from operation of determinant calculation) into (5.3), the final matrix takes form of:

$$\begin{pmatrix} \boldsymbol{s}C_1 & 0 & -\boldsymbol{s}C_1 \\ -g_{m2} & \boldsymbol{s}C_2 & g_{m2} \\ -\boldsymbol{s}C_1 + g_{m3} & -g_{m1} & \boldsymbol{s}C_1 + g_{m1} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}. \tag{5.6}$$

The matrix (5.6) can be then directly transferred into a circuit scheme shown in Fig. 5.3.

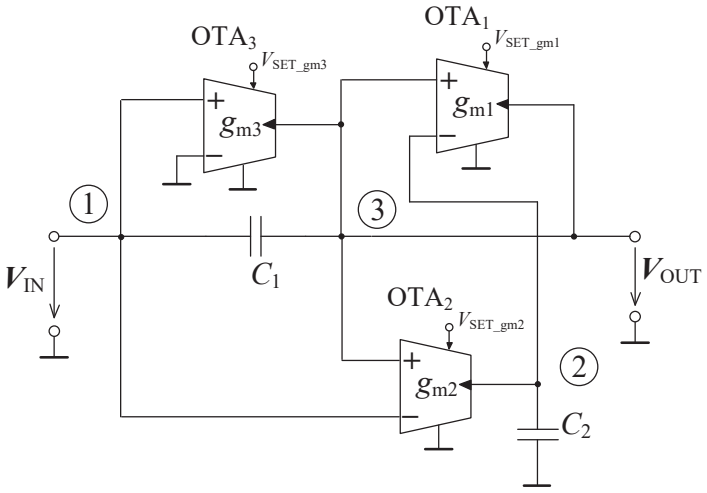


Fig. 5.3: Proposed reconnection–less reconfigurable filter before the addition of the VGA

The $\boldsymbol{s}^0$ term of the numerator has to be adjustable to be able to obtain some transfer functions. Thus, either g_{m1} or g_{m2} in the numerator (see (5.1)) has to be multiplied by voltage gain A. In order to influence the coefficient of the $\boldsymbol{s}^0$ term in the numerator of the transfer function, voltage gain A has to multiply Y_{21} as suggested by (5.6) (other possible term from (5.6) (i.e., Y_{32}) would add A in the $\boldsymbol{s}^0$ term of the denominator as well). Inclusion of the amplifier A into the designed circuit creates the fourth independent node. There is no other passive circuit component connected to node 4. It solves only direct connection between the output of the VGA and input of the OTA_2. Thus, the system does not require extension to full 4x4 matrix and gain A can be written directly in product with g_{m2} for simplicity. The resulting matrix takes form of:

$$\begin{pmatrix} \boldsymbol{s}C_1 & 0 & -\boldsymbol{s}C_1 \\ -g_{m2}A & \boldsymbol{s}C_2 & g_{m2} \\ -\boldsymbol{s}C_1 + g_{m3} & -g_{m1} & \boldsymbol{s}C_1 + g_{m1} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}. \tag{5.7}$$

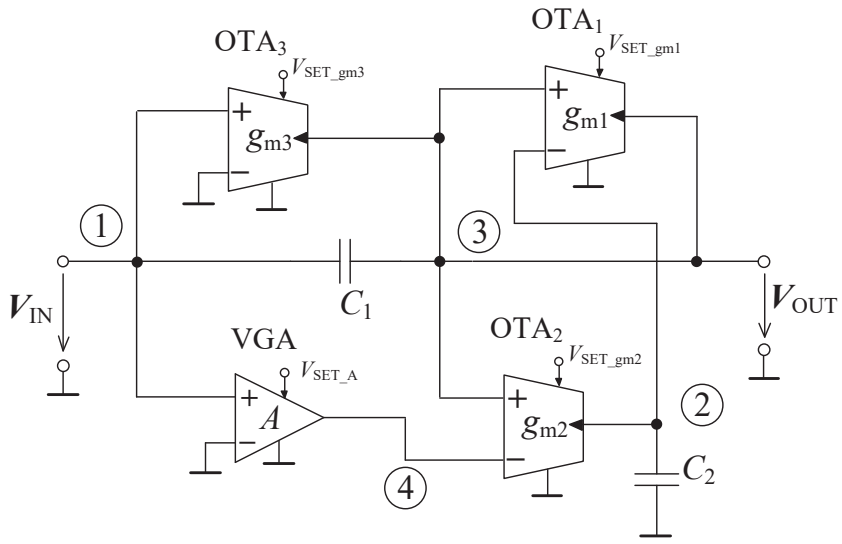


Fig. 5.4: Proposed reconnection–less reconfigurable filter using three OTAs and one VGA

The proposed filter (Fig. 5.4) consists of three OTAs, one VGA and two capacitors and its transfer function is identical to (5.1). The OTAs are implemented by multiplication units as depicted in Fig. 3.4, the VGA is also created by a multiplication unit and one resistor (Fig. 3.14). The expected power consumption is 31. 2 mW. The transfer function of the 1st–order HP is equal to $K(\boldsymbol{s}) = \boldsymbol{s}C_1/(\boldsymbol{s}C_1 + g_{m1})$. A special function HPZ can be obtained for the same setting as in case of BS, except that voltage gain A is less than 1. The specific setting of driving voltages of the adjustable parameters of the used active elements (in dependence on desired output response) is listed in Tab. II.

TABLE II. SETTING OF CONTROL VOLTAGES FOR SPECIFIC OUTPUT RESPONSE

	V_{SET_gm1} [V]	V_{SET_gm2} [V]	V_{SET_gm3} [V]	V_{SET_A} [-]
AP	0.5	0.5	0.5	0.5
BS	0.5	0.5	0	0.5
HP	0.5	0.5	0	0
1st–order HP	0.5	0	0	0.5
Direct transfer	0	0.5	0	0
HPZ	0.5	0.5	0	< 0.5

The relations for the pole frequency and quality factor of the proposed filter are derived from (5.1) as follows:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}\,, \tag{5.8}$$

$$Q = \sqrt{\frac{C_1 g_{m2}}{C_2 g_{m1}}} \,. \tag{5.9}$$

From (5.8 and 5.9), it is evident that f_0 can be electronically tuned, independently from Q, by changing g_{m1} and g_{m2} transconductances with following condition $g_{m1} = g_{m2}$.

Design verification

Simulations using Cadence IC6 (spectre) software have been carried out to verify the design correctness. In the initial state, the values of all parameters were set accordingly: the values of transconductances are $g_{m1} = g_{m2} = g_{m3} = 1$ mS, capacitors $C_1 = 1$ nF and $C_2 = 2$ nF, voltage gain A is equal to 1. This specific setting results in theoretical $f_0 = 112.5$ kHz and $Q = 0.707$ (Butterworth approximation).

The transfer functions of BS, HP, HP of the 1st–order and direct transfer (DT) are shown in Fig. 5.5. The simulation results are presented by colored lines and the theoretical expectations by black dashed lines. The obtained results indicate a good agreement with the theoretical expectations. The specific setting of independent filter parameters, according to the desired transfer function, can be found in Tab. II. Figure 5.6 depicts the characteristics of the all–pass filter (group delay (blue line), phase (red line) and magnitude/gain (green line)).

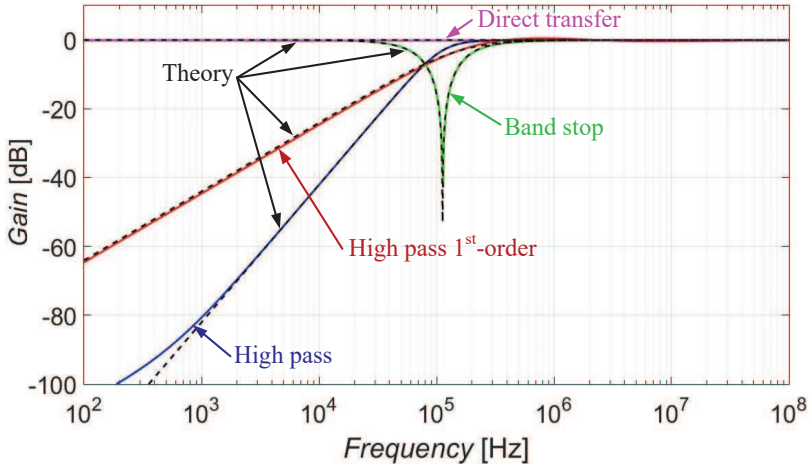


Fig. 5.5: Output responses of BS, HP, HP of the 1st–order and DT – simulations (colored lines), theoretical expectations (black dashed lines)

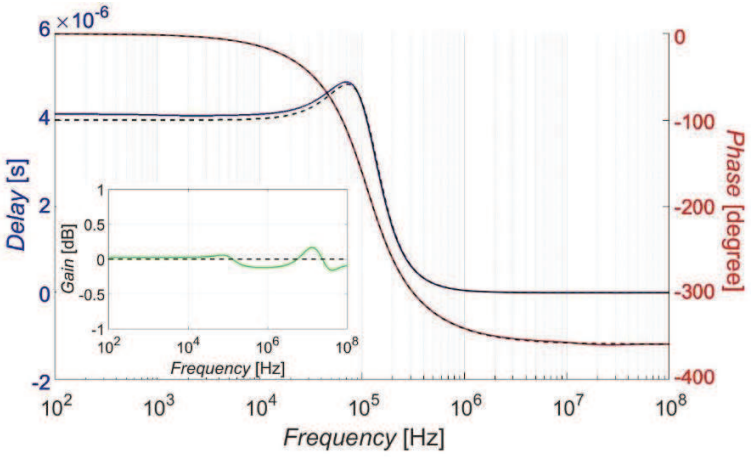


Fig. 5.6: AP filter – group delay (blue line), phase (red line) and gain (green line), theory (black dashed lines)

The illustration of the electronic tuning of f_0 of the proposed filter in case of the BS function is shown in Fig. 5.7. As mentioned before, the frequency f_0 is adjusted by the values of transconductances g_{m1} and g_{m2} which are set by the DC voltages V_{SET_gm1} and V_{SET_gm2}. For illustrative purposes, the values of these voltages have been set to 0.25 V, 0.5 V and 1 V which correspond with the values of the transconductances equal to 0.5 mS, 1 mS and 2 mS resulting in the theoretical pole frequencies of 56.3 kHz, 112.5 kHz and 225.1 kHz. The actual values of f_0 obtained from simulations are stated directly in Fig. 5.7 and compared with the theoretical values in Tab. III.

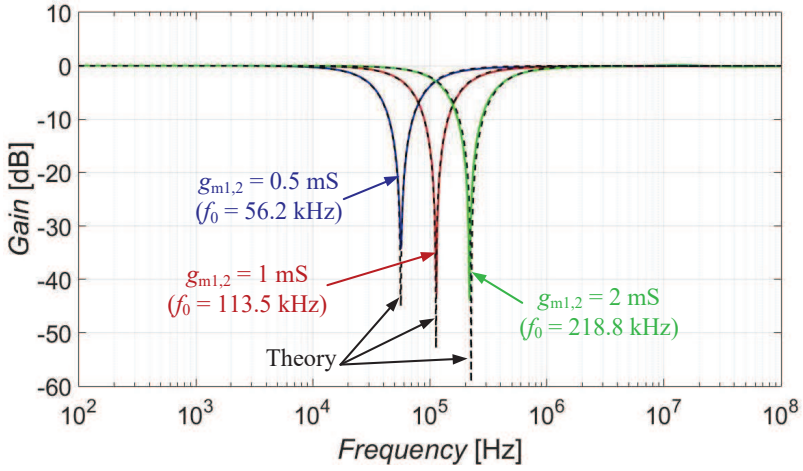


Fig. 5.7: Example of the electronic adjustment of f_0 for $g_{m1} = g_{m2}$ = 0.5 mS, 1 mS and 2 mS

TABLE III. ADJUSTMENT OF THE POLE FREQUENCY

g_{m1}, g_{m2} [mS]	0.5	1	2
Theoretical f_0 [kHz]	56.3	112.5	225.1
Simulated f_0 [kHz]	56.2	113.5	218.8

The special function HPZ (high pass with transfer zero) and its comparison to the theory is presented in Fig. 5.8. The HPZ has the same setting as the BS function except voltage gain A that is lower than 1. It provides the adjustment of the pass–band/stop–band region at lower frequencies. The demonstrational value of the voltage gain A has been subsequently set to 0.2, 0.05, 0.01 and 0.002 (corresponding with the values of control voltage V_{SET_A} equal to 0.1 V, 0.025 V, 0.005 V and 0.001 V).

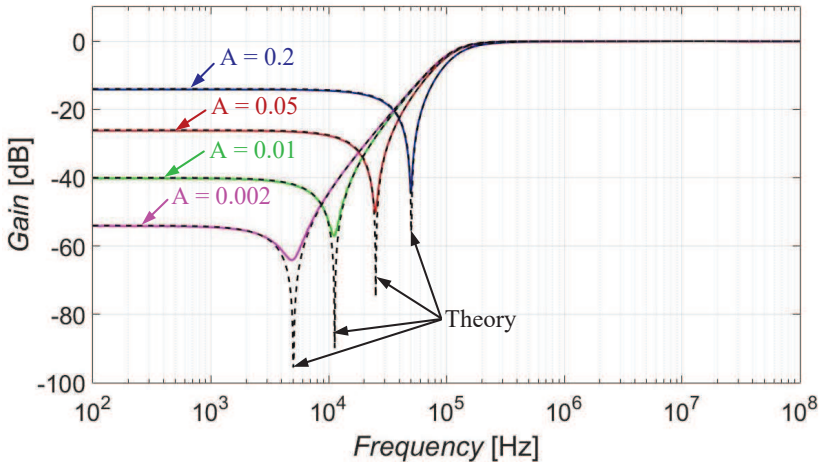


Fig. 5.8: Demonstration of behavior of HPZ – simulations (colored lines) vs. theory (black dashed lines)

Sensitivity analysis

The further analysis of the proposed filtering structure includes a sensitivity analysis. The fabrication mismatch (certain inaccuracy of individual outputs of each active element and the tolerance of used passive parts) can significantly influence the resulting transfer characteristics. Based on this fact, the filter involves 6 parameters (C_1, C_2, g_{m1}, g_{m2}, g_{m3}, and A). Parameters g_{m1}, g_{m2}, and g_{m3} are transconductances of individual outputs of OTA elements and parameter A stands for the voltage gain of the VGA.

The corresponding denominator considering these parameters takes a form of:

$$D_{real}(\boldsymbol{s}) = \boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m1} + g_{m1} g_{m2}\,. \tag{5.10}$$

The real numerator of the filter is given by the following equation:

$$N_{real}(\boldsymbol{s}) = \boldsymbol{s}^2 C_1 C_2 - \boldsymbol{s} C_2 g_{m3} + g_{m1} g_{m2} A\,. \tag{5.11}$$

The relative sensitivity (module) of the filter on variation of each individual parameter can be described as [105]:

$$S_{qi}^{|\boldsymbol{K}(j\omega)|} = \mathrm{Re}\{S_{qi}^{|\boldsymbol{K}(j\omega)|}\}, \tag{5.12}$$

where $\boldsymbol{K} = \boldsymbol{K}(j\omega)$ is a transfer of the filter $\boldsymbol{K} = \boldsymbol{I}_{OUT}/\boldsymbol{I}_{IN}$ and q_i represents i^{th} parameter of the filter. Maple tool was used to perform the mathematical expression of the sensitivities.

Figures 5.9 and 5.10 show the results of the sensitivity analysis across whole frequency range from 100 Hz to 100 MHz for AP and HP responses. Figure 5.9 shows the results for the AP function and Fig. 5.10 presents the results for the HP function (sensitivities for parameters g_{m3} and A are not shown because these parameters are not presented in the symbolical transfer form for the HP function). All sensitivities are relatively low (they are around one, which is the typical value). The highest sensitivity is around the pole frequency of the filter (112.5 kHz), which is well known fact [105].

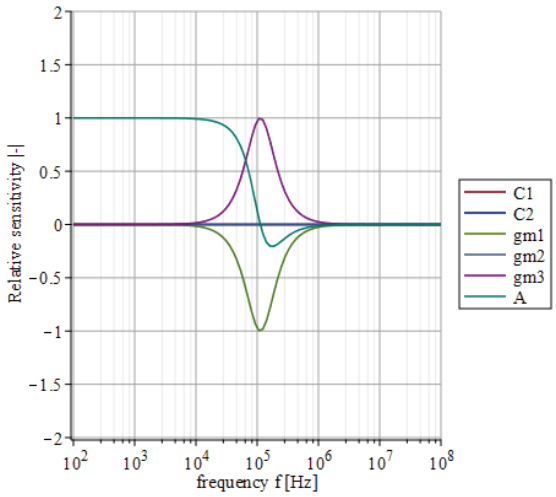


Fig. 5.9: Relative sensitivity of the AP function for individual parameters in dependence on the frequency

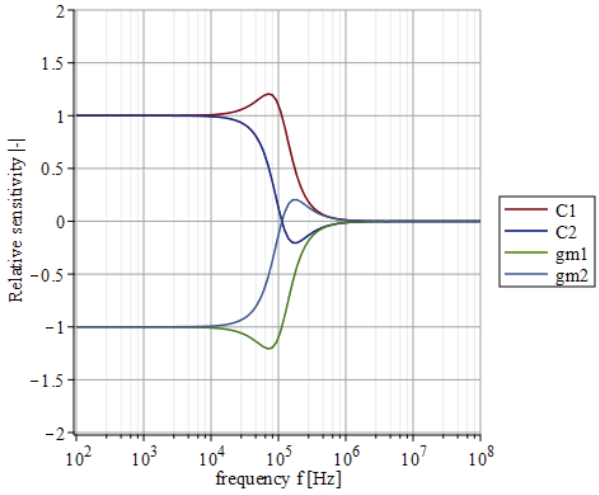


Fig. 5.10: Relative sensitivity of the HP function for individual parameters in dependence on the frequency

Fractional–order characteristics

The proposed filtering structure has been supplemented by the FOE in order to test fractional–order behavior. A fractional–order capacitor $C_\alpha = C\omega_0^{1-\alpha}$ [88], implemented by the 5th–order RC topology of the Cauer I type (depicted in Fig. 5.11), has been applied to the proposed structure as a replacement of capacitor C_2.

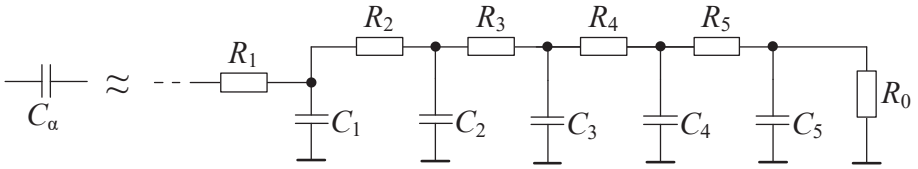


Fig. 5.11: 5th–order RC structure of the Cauer I type used in order to approximate C_2

The denominator of the fractional–order function, based on the general fractional–order transfer functions with Butterworth characteristics [63], is described as:

$$D(\boldsymbol{s}) = \boldsymbol{s}^{1+\alpha} + \boldsymbol{s}^{\alpha}\frac{g_{m1}}{C_1} + \frac{g_{m1}g_{m2}}{C_1 C_{2\alpha}}. \tag{5.13}$$

The Oustaloup approximation [96] has been used in order to calculate the values of the individual components of the RC approximating structure for the tested values of parameter α. These calculations were carried out using a created Matlab script. All these values are summarized in Tab. IV (for the HP transfer function). The value of capacitor C_1 = 10 nF and the pole frequency was chosen f_0 = 10 kHz. The values of transconductances g_{m1} and g_{m2} have to be recalculated depending on the actual value of capacitor C_2 which relates on the selected value of parameter α. The values of g_{m1} and g_{m2} are calculated comparing the particular term of (5.13) and general fractional order transfer functions [51] (general fractional-order HP function in this case (5.14)). The resulting values of g_{m1} and g_{m2} are also included in the table.

$$K_{1+\alpha}^{HP}(\boldsymbol{s}) = \frac{k_1 \boldsymbol{s}^{1+\alpha}}{k_3 \boldsymbol{s}^{1+\alpha} + k_2 \boldsymbol{s} + 1} \tag{5.14}$$

Coefficients k shape the transition between the pass–band and stop–band area so the transition keeps the Butterworth characteristics (k_1 = 1, $k_2 = 1.008\alpha^2 + 0.2867\alpha + 0.2366$ and $k_3 = 0.2171\alpha + 0.7914$).

TABLE IV. VALUES OF COMPONENTS OF THE RC STRUCTURE FOR HP FUNCTION IN DEPENDENCE ON VALUE OF ALPHA

α [–]	**0.3**	**0.5**	**0.7**
$C_{2\alpha}$ [µF/sec$^{1-\alpha}$]	22.8	2.5	0.28
R_0 [Ω]	1831.0	6439.5	178867.6
R_1 [Ω]	399.8	159.2	63.4
R_2 [Ω]	471.4	462.9	454.4
R_3 [Ω]	687.3	1025.2	1525.9
R_4 [Ω]	1143.6	2464.5	5239.1
R_5 [Ω]	1802.9	5364.3	14827.6
C_1 [nF]	1.5	2.2	3.85
C_2 [nF]	5.2	4.2	3.52
C_3 [nF]	18.4	10.2	5.7
C_4 [nF]	69.4	27.0	10.7
C_5 [nF]	336.0	97.8	32.2
g_{m1} [µS]	259.7	397.1	585.1
g_{m2} [µS]	1302.0	894.8	636.5

Figure 5.12 illustrates the behavior of the fractional–order HP function for three chosen values of parameter α (α = 0.3, 0.5 and 0.7). The values of the resulting orders (n), obtained from simulations, are stated in Fig. 5.12. Real behavior indicates that the used approximation does not follow the correct slope of the transition between pass–band and stop–band region under frequency of 100 Hz because the approximation, used for design of FO capacitor C_{2a}, is not valid anymore.

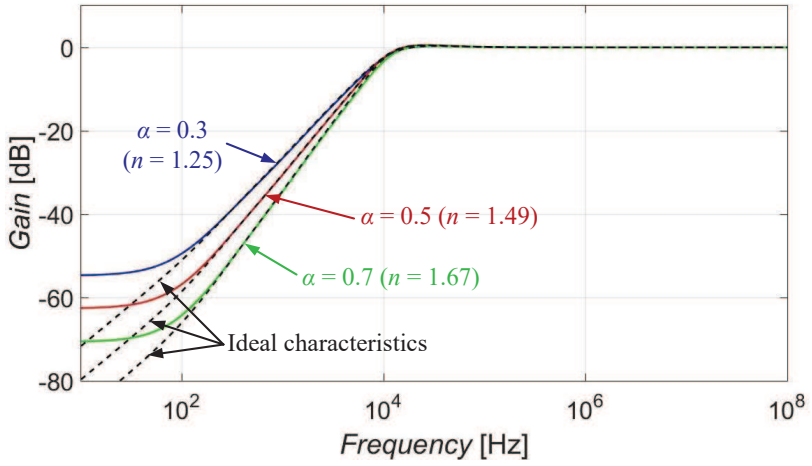


Fig. 5.12: Demonstration of fractional–order HP function for α = 0.3, 0.5 and 0.7 – simulations (colored lines), ideal characteristics (black dashed lines)

5.1.2 Structure with two VDTAs and one VGA

The proposed structure offers (2nd–order) transfer functions of AP, BS, LP, LPZ and HP function of the 1st–order and DT in dependence on setting of transconductances g_m and voltage gain A all electronically controlled. The filter also offers the electronic adjustment of its pole frequency and quality factor. The additional useful feature consists in the

adjustment of the center frequency of the BS function while maintaining its bandwidth constant. Moreover, the pass–band/stop–band region at higher frequencies can be easily adjusted by the voltage gain *A*. This research is presented in [150] (conference Radioelektronika (ISBN: 978-1-5386-9321-6), 2019).

Design proposal

The desired form of the circuit transfer function, which is then used for the circuit synthesis, has the symbolical expression:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{s}^2 C_1 C_2 A - \boldsymbol{s} C_2 g_{m1} + g_{m3} g_{m4}}{\boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m2} + g_{m3} g_{m4}}, \tag{5.15}$$

where g_{m1} to g_{m4} are transconductance of the OTA elements which are then creating $VDTA_1$ and $VDTA_2$ in Fig. 5.13. Voltage gain A in (5.15) will be omitted in this stage of solution in order to perform easier hand calculation. The VGA element is added in resulting structure after the circuit synthesis to the proper connection causing desired feature. We expect the circuit having two capacitors (capacitor C_1 between nodes 1 and 3 and capacitor C_2 is connected to node 2). Based on this fact, the relation (5.2) turns into:

$$\begin{pmatrix} \boldsymbol{s}C_1 & 0 & -\boldsymbol{s}C_1 \\ 0 & \boldsymbol{s}C_2 & 0 \\ -\boldsymbol{s}C_1 & 0 & \boldsymbol{s}C_1 \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}. \tag{5.16}$$

When supposing $K(\mathbf{s}) = V_{OUT}/V_{IN} = V_3/V_1 = \Delta_{1,3}/\Delta_{1,1}$, determinants $\Delta_{1,1}$ and $\Delta_{1,3}$ (with regard to (5.15)) are found in form of:

$$\begin{aligned} &\Delta_{1,1} = Y_{22}Y_{33} - Y_{32}Y_{23} = b_2\boldsymbol{s}^2 + b_1\boldsymbol{s} + b_0 = \boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m2} + g_{m3} g_{m4} = \\ &= \boldsymbol{s} C_2 \left(\boldsymbol{s} C_1 + g_{m2}\right) - \left(g_{m4}\left(-g_{m3}\right)\right) \end{aligned}, \tag{5.17}$$

$$\begin{aligned} &\Delta_{1,3} = Y_{21}Y_{32} - Y_{31}Y_{22} = a_2\boldsymbol{s}^2 + a_1\boldsymbol{s} + a_0 = \boldsymbol{s}^2 C_1 C_2 - \boldsymbol{s} C_2 g_{m1} + g_{m3} g_{m4} = \\ &= \left(g_{m3} g_{m4}\right) - \left[\left(-\boldsymbol{s} C_1 + g_{m1}\right)\boldsymbol{s} C_2\right] \end{aligned}. \tag{5.18}$$

Combining (5.16), (5.17) and (5.18), the resulting matrix is as follows:

$$\begin{pmatrix} \boldsymbol{s}C_1 & 0 & -\boldsymbol{s}C_1 \\ g_{m3} & \boldsymbol{s}C_2 & -g_{m3} \\ -\boldsymbol{s}C_1 + g_{m1} & g_{m4} & \boldsymbol{s}C_1 + g_{m2} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}. \tag{5.19}$$

The circuit structure in Fig. 5.13 has been created from (5.19).

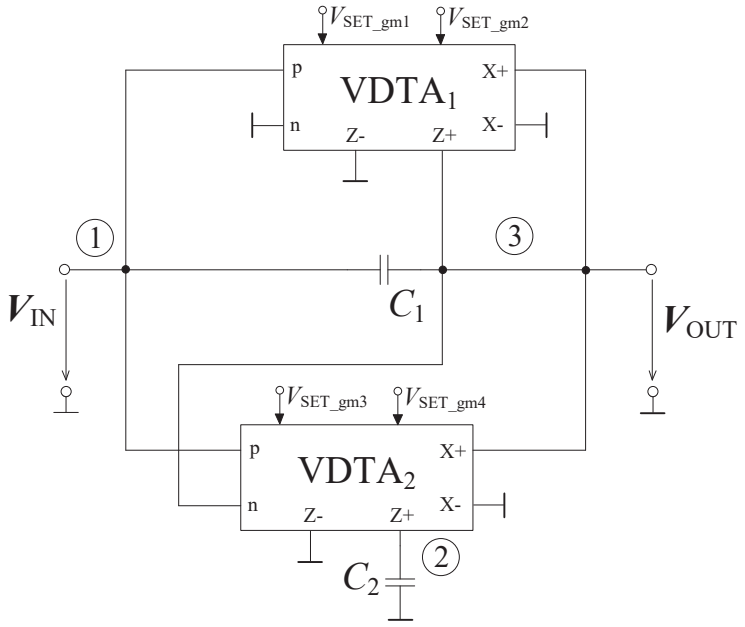


Fig. 5.13: Proposed solution of a reconnection–less reconfigurable filter before addition of the VGA element

The resulting structure provides AP, BS, DT a 1st–order HP functions. Thus, the VGA element is added between the input node (node 1) and C_1. This modification extends features of the circuit for additional LP and LPZ functions. Such modification results in the circuit topology having four independent nodes. Voltage gain A has to multiply Y_{31} in order to only apply in s^2 term in the numerator of the transfer function. This modification also brings the ability to electronic adjustment of the pass–band/stop–band area at higher frequencies. The resulting matrix is given as:

$$\begin{pmatrix} sC_1 & 0 & -sC_1 \\ g_{m3} & sC_2 & -g_{m3} \\ -sC_1A+g_{m1} & g_{m4} & sC_1+g_{m2} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} = \begin{pmatrix} I_1 \\ 0 \\ 0 \end{pmatrix}. \tag{5.20}$$

The resulting circuit structure (depicted in Fig. 5.14) is obtained from the matrix in (5.20). The filter is formed by two VDTAs, one VGA and two capacitors and its transfer function is identical to (5.15) as required by the synthesis. The OTAs in the inner structure of VDTAs (Fig. 3.16) are based on multiplication units as depicted in Fig. 3.4. Figure 3.15 presents the used solution of the VGA element. The power consumption, based on above mentioned implementation, has been calculated as 48.1 mW. The 1st–order HP function is described as $K(s) = sC_1/(sC_1+g_{m2})$. The LPZ function has the same setting as the BS function. However, A has to be less than 1 ($V_{SET\_A} < 0.5$ V) for the correct operation.

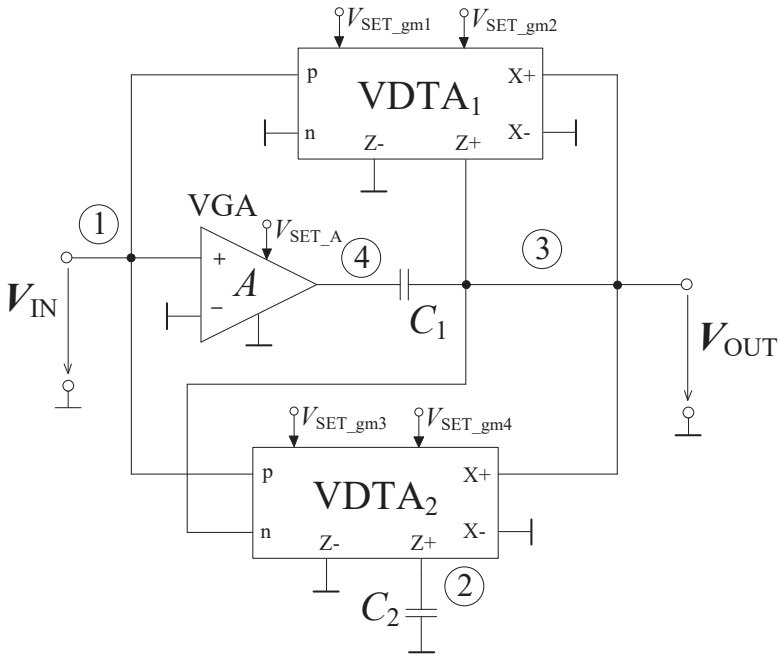


Fig. 5.14: Proposed solution of a reconnection–less reconfigurable filter based on two VDTA and one VGA elements

The resulting transfer function of the filter depends on the setting summarized in Tab. V.

TABLE V. OBTAINABLE OUTPUT RESPONSES IN DEPENDENCE ON THE SETTING OF CONTROL VOLTAGES

	V_{SET_gm1} [V]	V_{SET_gm2} [V]	V_{SET_gm3} [V]	V_{SET_gm4} [V]	V_{SET_A} [V]
AP	0.5	0.5	0.5	0.5	0.5
BS	0	0.5	0.5	0.5	0.5
LP	0	0.5	0.5	0.5	0
LPZ	0	0.5	0.5	0.5	< 0.5
1st–order HP	0	0.5	0	0	0.5
DT	0	0	0	0	0.5

The pole frequency f_0 and quality factor Q of the proposed filter follow relations:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m3}g_{m4}}{C_1C_2}}, \tag{5.21}$$

$$Q = \frac{1}{g_{m2}}\sqrt{\frac{C_1g_{m3}g_{m4}}{C_2}}. \tag{5.22}$$

The pole frequency f_0 can be adjusted electronically and independently on Q by adjusting values of transconductances g_{m2}, g_{m3} and g_{m4}. Both equations (5.21) and (5.22) indicate that

constant Q requires equality of $g_{m2} = g_{m3} = g_{m4}$ during the tuning process of f_0. The quality factor Q can be tuned electronically and independently of f_0 by adjusting values of g_{m2}. It is also possible to adjust the center frequency of the BS function while maintaining its bandwidth constant (quality factor varies) by adjusting values of transconductances g_{m3} and g_{m4} simultaneously.

Design verification

The simulations of the proposed filter were carried out using Cadence IC6 (spectre simulator) software. The numerical design of the initial state of the filter has been set as follows: the values of transconductances $g_{m1} = g_{m3} = g_{m4} = 1$ mS and values of capacitors C_1 and C_2 are 1.6 nF which results in $f_0 = 99.5$ kHz. The value of g_{m2} is equal to 1.33 mS and together with above mentioned values provides $Q = 0.75$. In case of the AP filter, the value of g_{m2} must be the same as the value of other transconductances (1 mS) for flat magnitude response (having unity gain).

Figure 5.15 illustrates the output responses of BS, LP, DT and 1st–order HP function. The figure compares the simulation results (colored solid lines) with the theoretical expectations (black dashed lines). The differences between the theory and simulation results at higher frequencies are (beside standard parasitic characteristics) caused by the specific used implementation of the VGA element. The node between the OTA and VDDB elements where resistor R is connected (see Fig. 3.15) is the main reason of deviations from ideal characteristics as the node is supposed to be a low–impedance node. The value of the resistor R together with parasitic capacitance in this node (terminal stray capacity + PCB capacity) create this parasitic influence. This issue can be mostly eliminated by more suitable implementation of the VGA element having a single voltage input voltage output element with the electronically controllable gain (VCA810 device [131], for example).

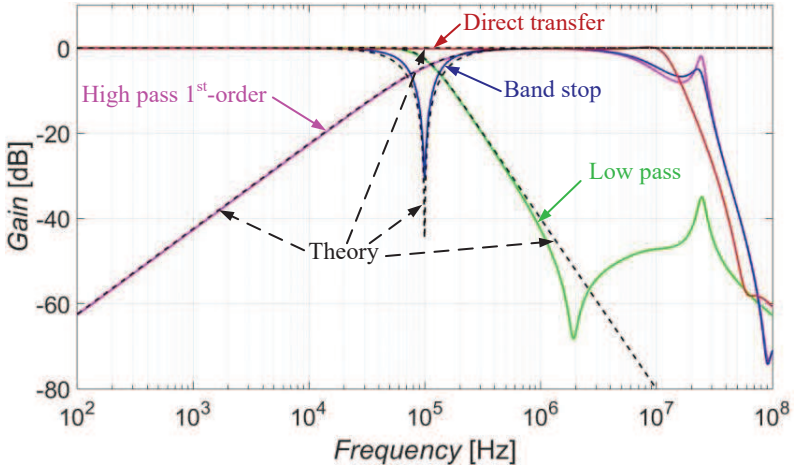


Fig. 5.15: Output responses of BS, LP, 1st–order HP and DT – simulation results (colored lines), theoretical expectations (black dashed lines)

Figure 5.16 illustrates the electronic adjustability of the pole frequency f_0 for four different values of f_0. The LP function has been used for the demonstration of tunability. The values of transconductances $g_{m3} = g_{m4}$ were set to 0.56 mS, 0.75 mS, 1 mS and 1.33 mS (g_{m2} = 0.75 mS, 1 mS, 1.33 mS and 1.77 mS). We expect theoretical f_0 equal to 56.0 kHz, 74.6 kHz, 99.5 kHz and 132.6 kHz. The value obtained from simulations are given in the graph (Fig. 5.16) and compared to the theoretical values in Tab. VI.

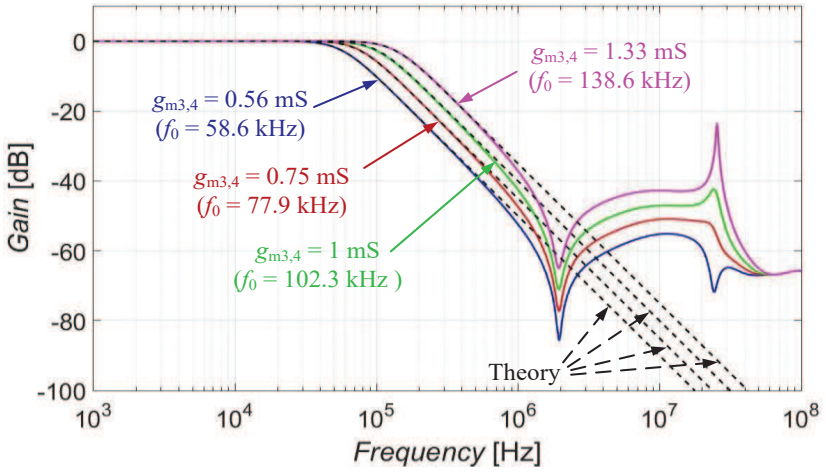


Fig. 5.16: Electronic adjustment of f_0 in case of LP function – simulations (colored lines), theory (black dashed lines)

TABLE VI. ADJUSTMENT OF THE POLE FREQUENCY

g_{m3}, g_{m4} [mS]	0.56	0.75	1	1.33
Theoretical f_0 [kHz]	56.0	74.6	99.5	132.6
Simulated f_0 [kHz]	58.6	77.9	102.3	138.6

The demonstration of the ability of the electronic adjustment of the Q (in case of the BS function) is shown in Fig. 5.17. This feature was tested for three values of g_{m2} (1.33 mS, 0.67 mS and 0.33 mS) providing theoretical quality factors of 0.75, 1.5 and 3 ($g_{m1} = g_{m3} = g_{m4}$ = 1 mS). The values obtained from simulations are provided in the graph and compared with the theoretical values of quality factors in Tab. VII.

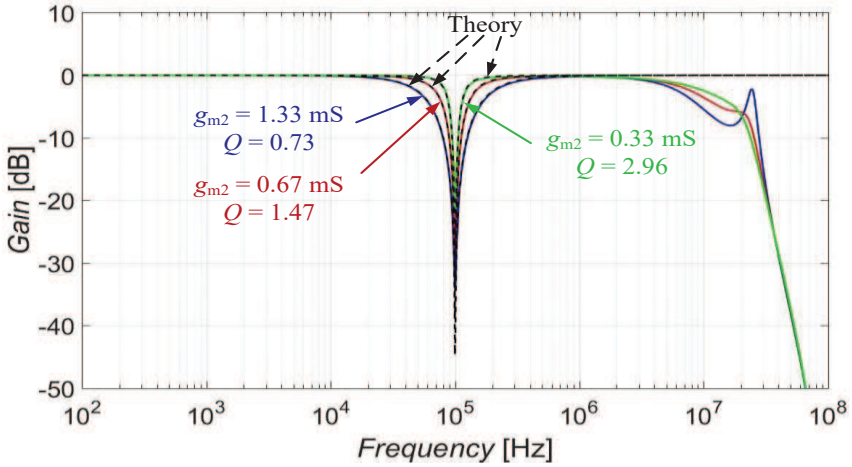


Fig. 5.17: Demonstration of the electronic adjustment of Q in case of BS function – simulations (colored lines), theory (black dashed lines)

TABLE VII. ADJUSTMENT OF THE QUALITY FACTOR

g_{m2} [mS]	1.33	0.67	0.33
Theoretical Q [-]	0.75	1.5	3
Simulated Q [-]	0.73	1.47	2.96

The ability of the electronic adjustment of f_0 of BS function with constant bandwidth is depicted in Fig. 5.18. The ideal bandwidth of the BS function for the initial values (f_0 = 99.5 kHz and Q = 0.75) yields $BW = f_0/Q$ = 132.7 kHz. The expected bandwidth, depending on the values obtained for simulations, is 137.3 kHz. The values of transconductances g_{m3} and g_{m4} (g_{m2} = 1.33 mS) were set the same as in case of the electronic adjustment of the f_0. For the tested f_0, the value of obtained bandwidth varies from 137.2 kHz to 138.3 kHz.

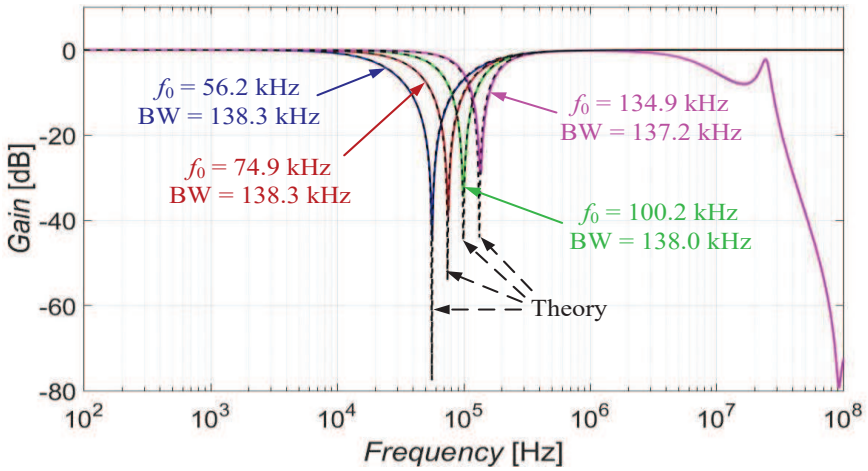


Fig. 5.18: Example of the ability to electronically tune f_0 of BS function with constant bandwidth – simulations (colored lines), theory (black dashed lines)

5.2 Structures based on a modification of existing filters

The proposal in this chapter is based on a modification of existing filtering structures which do not offer the ability of the reconnection–less modification of the transfer in their already known topology. The useful modification is achieved through the supplement of these topologies by additional active elements and further minor modifications than used in known concept. These elements (at suitable positions) in the structure ensure the ability of the reconnection–less reconfiguration. The filter in subsection 5.2.1 originates from a MISO structure using two VDTAs. Single VDCC–based filter was the fundamental prototype for the design of the filter described in subsection 5.2.2.

5.2.1 Structure with two VDTAs, three ACAs and one MO–CF

The proposed filter follows the concept of the previously published universal filter presented in [120]. The modified reconnection–less reconfigurable filter can provide all standard transfer functions (LP, BP, HP, BS, AP) as well as HPZ and LPZ from the same circuit topology by the specific readjustment of current gains of used ACAs in the topology. Transconductances of VDTA elements are implemented in order to provide the electronic tunability of the pole frequency and quality factor independently of each other. The pass–band/stop–band area (attenuation level) across whole frequency band can be easily adjusted. The discussed design is published in [151] (International Conference Radioelektronika (ISBN: 978-1-5386-2485-2), 2018).

The used structure from [120] employs two VDTAs and offers all standard transfer functions. The filter topology of used prototype has a character of MISO type (three inputs in particular). There, a manual mechanical reconnection of particular input (or a suitable combination of two or more inputs) is necessary in order to obtain desired transfer function (see Fig. 5.19).

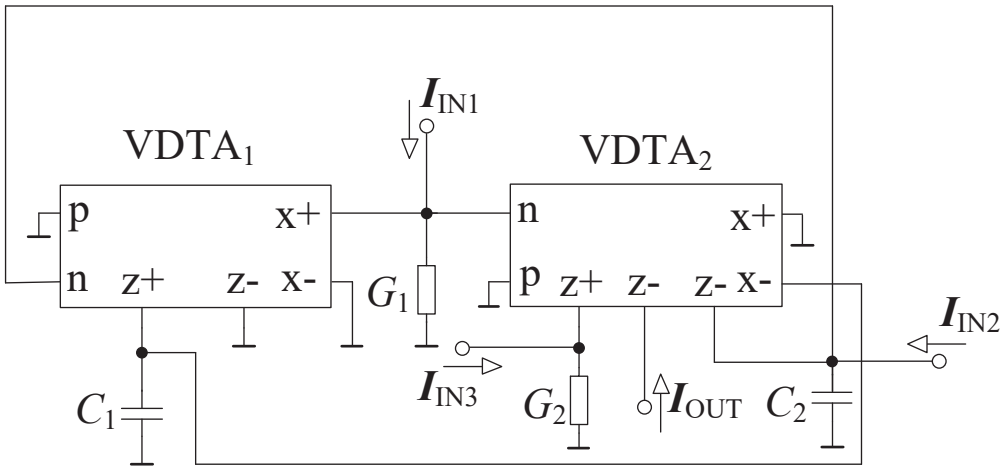


Fig. 5.19: MISO current–mode filter from [120] used for the modification

The filter consists of two VDTAs, two resistors (labeled as conductance G_1 and G_2) and two grounded capacitors. The transfer function of the filter from Fig. 5.19 is given by:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{I}_{OUT}}{\boldsymbol{I}_{IN}} = \frac{\boldsymbol{s}^2 C_1 C_2 G_2 g_{m3} \boldsymbol{I}_{IN1} - \boldsymbol{s} C_2 g_{m2} g_{m3} g_{m4} \boldsymbol{I}_{IN3} + G_2 g_{m1} g_{m2} g_{m3} \boldsymbol{I}_{IN2}}{\boldsymbol{s}^2 C_1 C_2 G_1 G_2 + \boldsymbol{s} C_2 g_{m2} g_{m3} g_{m4} + G_2 g_{m1} g_{m2} g_{m3}}, \tag{5.23}$$

where $\boldsymbol{I}_{\mathrm{IN1}}$ (current excitation in this node) represents the signal input allowing the presence of the quadratic term of numerator in the transfer response, $\boldsymbol{I}_{\mathrm{IN3}}$ corresponds with the signal input associated with the linear term of numerator and $\boldsymbol{I}_{\mathrm{IN2}}$ represents the signal input for the $\boldsymbol{s}^0$ term. Based on this fact, the individual transfer functions are available as stated in Tab. VIII.

TABLE VIII. OBTAINABLE OUTPUT TRANSFER FUNCTIONS BASED ON THE SETTING OF EXCITATION CURRENTS

	$\boldsymbol{I}_{\mathrm{IN1}}$	$\boldsymbol{I}_{\mathrm{IN2}}$	$\boldsymbol{I}_{\mathrm{IN3}}$
LP		●	
HP	●		
BP			●
BS	●	●	
AP	●	●	●

The pole frequency and quality factor are expressed as (considering $G_1 = g_{\mathrm{m3}}$):

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}, \tag{5.24}$$

$$Q = \frac{G_2}{g_{m4}} \sqrt{\frac{C_1 g_{m1}}{C_2 g_{m2}}}. \tag{5.25}$$

Design proposal

The filtering structure from original MISO concept in Fig. 5.19 is complemented with a suitable arrangement of three ACAs. They have responsibility of the electronic change of the filter transfer response. The additional auxiliary MO–CF serves for the redistribution of the input current (copy of input current in both orientations/polarities) to specific branches supplying input nodes. Such modification results in the reconnection–less reconfigurable filter presented in Fig. 5.20. The structure is created by two VDTAs, three ACAs, one MO–CF, two resistors and two grounded capacitors. All used active elements are created by CMOS models created by TSMC 0.18 μm technology (MO–CF created by a model from [120], OTAs (used

in the inner topology of VDTAs) by a model from [42] and ACAs by a model from [121]). The power consumption of the filter from Fig. 5.20 is 13 mW.

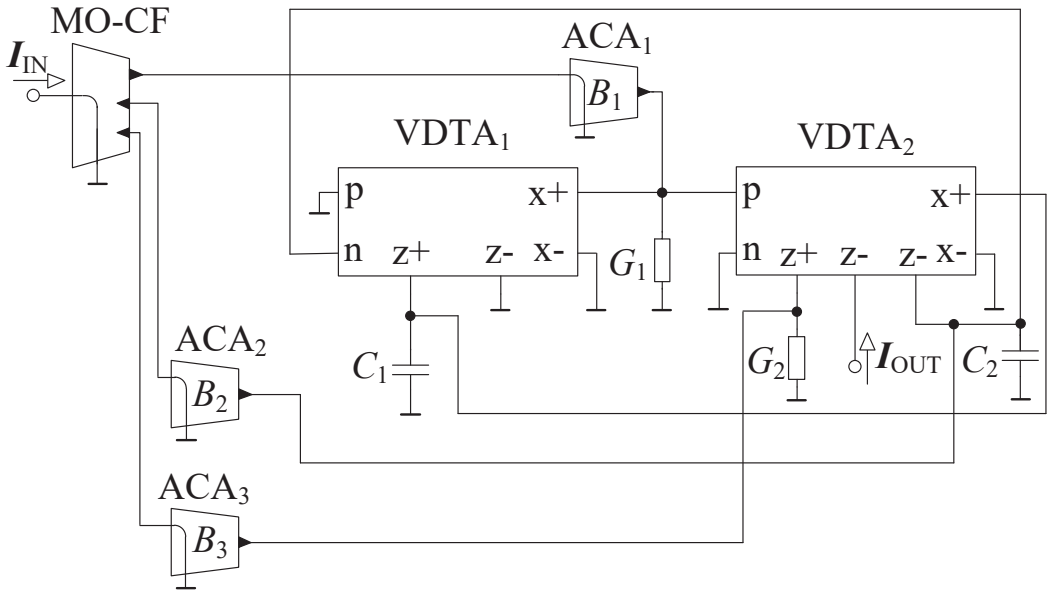


Fig. 5.20: Proposed reconnection–less reconfigurable universal filter based on a modification of the structure from [120]

The transfer of the proposed filter is given as:

$$K(s) = \frac{I_{OUT}}{I_{IN}} = \frac{s^2 C_1 C_2 G_2 g_{m3} B_1 - s C_2 g_{m2} g_{m3} g_{m4} B_3 + G_2 g_{m1} g_{m2} g_{m3} B_2}{s^2 C_1 C_2 G_1 G_2 + s C_2 g_{m2} g_{m3} g_{m4} + G_2 g_{m1} g_{m2} g_{m3}}. \quad (5.26)$$

The equation (5.26) offers an evident feature allowing the electronic reconfiguration of transfer response by setting of individual current gains B_1 to B_3. The proposed filter can provide transfer functions specified in Tab. IX depending on actual setting of current gains.

TABLE IX. OBTAINABLE OUTPUT TRANSFER FUNCTIONS BASED ON THE SETTING OF CURRENT GAINS

	B_1	B_2	B_3
LP	0	1	0
HP	1	0	0
BP	0	0	1
BS	1	1	0
AP	1	1	1
HPZ	1	< 1	0
LPZ	< 1	1	0

If we consider $G_1 = g_{m3}$, the pole frequency f_0 and quality factor Q of the proposed filter are the same as relations in (5.24) and (5.25).

Relations (5.24) and (5.25) documents the feature of the independent electronic adjustment of f_0 and Q by a simultaneous change of transconductance g_{m1} and g_{m2} when a simple condition $g_{m1} = g_{m2}$ is applied. The quality factor can be tuned electronically without any impact on f_0 by adjustment of transconductance g_{m4}. Similarly, f_0 could be also tuned by the change of values of capacitances C_1, C_2 and Q could be adjusted by conductance G_2, but the direct ability of the electronic adjustment is more advantageous.

Design verification

The proposal has been verified by PSpice simulations using transistor–level models of applied active elements. The proposed filter has been designed to operate at pole frequency equal to 100 kHz and quality factor equal to 0.707 (Butterworth approximation). Based on these expectations, the values of transconductances and values of passive elements have been selected and calculated as follows: $g_{m1} = g_{m2} = g_{m3} = 1$ mS, conductances $G_1 = G_2 = 1$ mS. Capacitances C_1 and C_2 (1.6 nF) were calculated from (5.24) in order to obtain the desired f_0. Transconductance g_{m4} was set to 1.414 mS and results in $Q = 0.707$.

Figure 5.21 shows output responses LP (blue line), BP (red line), HP (green line) and BS (magenta line) in case of simulations and compares them with the theoretical expectations (black dashed lines).

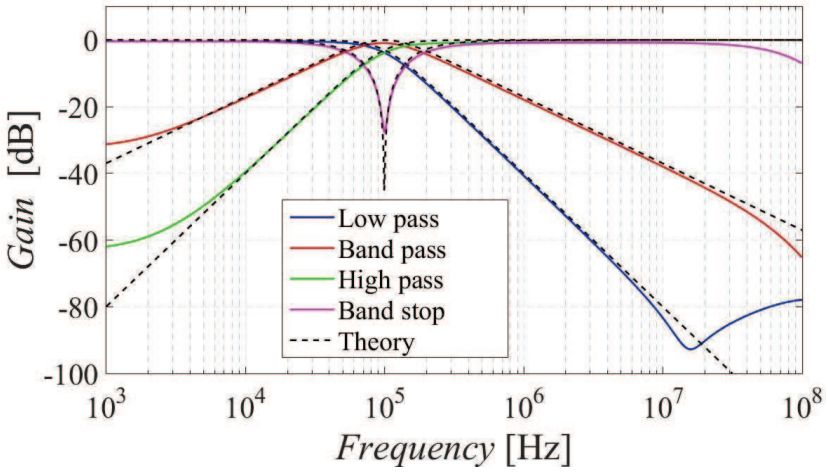


Fig. 5.21: Output responses LP, BP, HP and BS: theory (black dashed lines) and simulations (colored lines)

Characteristics of group delay, phase and gain of the AP filter are illustrated in Fig. 5.22. Phase (blue line), group delay (red line), gain (green line) are compared with the theory (black dashed lines).

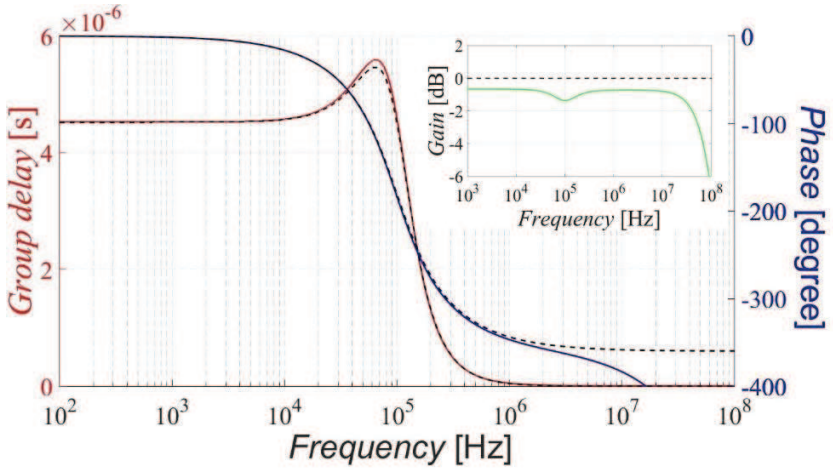


Fig. 5.22: Output responses of AP filter: phase (blue line), group delay (red line), gain (green line), theory (black dashed lines)

The ability of the electronic adjustment of f_0 is demonstrated in Fig. 5.23 for LP function and for three different settings of $g_{m1} = g_{m2} = g_m$ (0.5 mS, 1 mS and 2 mS). The gained values of tuned f_0 reach approximately 50 kHz, 100 kHz and 200 kHz. Values obtained from simulations are stated in the graph legend (values in parenthesis). Also, the theoretical and simulated values of f_0 are compared in Tab. X.

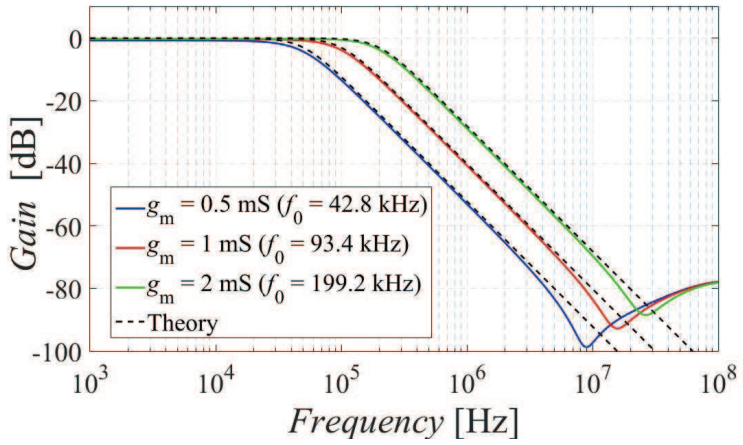


Fig. 5.23: Illustration of the electronic adjustment of the pole frequency of LP for f_0 = 50 kHz, 100 kHz and 200 kHz

TABLE X. ADJUSTMENT OF THE POLE FREQUENCY

g_{m1}, g_{m2} [mS]	0.5	1	2
Theoretical f_0 [kHz]	49.7	99.5	198.9
Simulated f_0 [kHz]	42.8	93.4	199.2

As mentioned before, the electronic adjustability of the quality factor of the filter (independently on the pole frequency) brings an interesting feature except electronic

tunability of f_0. Figure 5.24 illustrates this ability using BP function as an example. The values of g_{m4} were set to 1.414 mS, 0.707 mS and 0.354 mS which results in Q equal to 0.71, 1.41 and 2.83. Values obtained from simulations are stated in the graph legend (values in parenthesis) and they are compared with the theoretical values of the quality factor in Tab. XI.

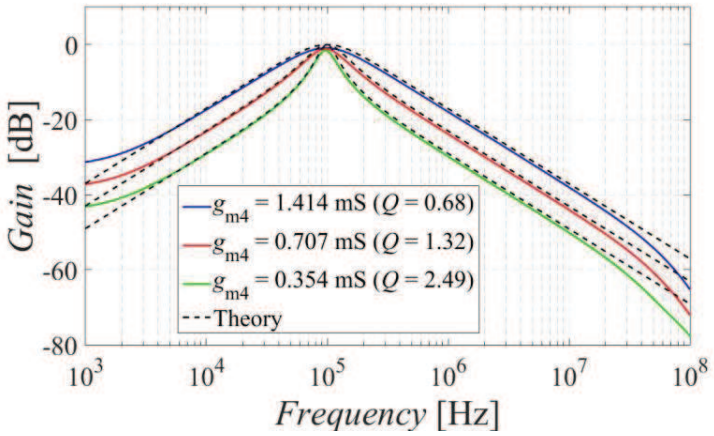


Fig. 5.24: Illustration of the electronic adjustment of the quality factor of BP for Q = 0.71, 1.41 and 2.83

TABLE XI. ADJUSTMENT OF THE QUALITY FACTOR

g_{m4} [mS]	1.414	0.707	0.354
Theoretical Q [-]	0.71	1.41	2.83
Simulated Q [-]	0.68	1.32	2.49

The proposed structure also offers the ability to create low–pass and high–pass response with intended zero in transfer function. The behavior of the LPZ and HPZ function (for default values of transconductances) can be observed in Fig. 5.25.

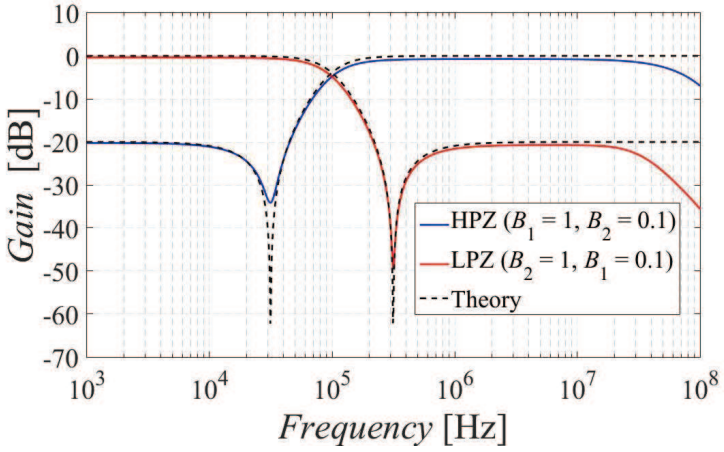


Fig. 5.25: Illustration of the HPZ and LPZ functions

5.2.2 Structure with one VDCC and one IOGC–CA

The proposal is showing a simple way how obtain the reconnection–less reconfigurable ability for a standard MISO filter structure by the addition of the IOGC–CA element presented in subsection 6.1.1. The designed filter offers all standard 2nd–order transfer functions and also functions of DT and HPZ from the same topology without any further modification of the structure or switching between nodes. In comparison with the structure before the modification (i.e., original structure in [24]), the proposed filter provides the electronic tunability of its pole frequency and quality factor. The filter is presented in [152] (International Conference Radioelektronika (ISBN: 978-1-7281-6468-7), 2020).

The structure, used for the purposes of the design of the reconnection–less reconfigurable filter based on the modification of an existing circuit, is a MISO filter presented in [24]. The core of the filter is created by one VDCC as depicted in Fig. 5.26.

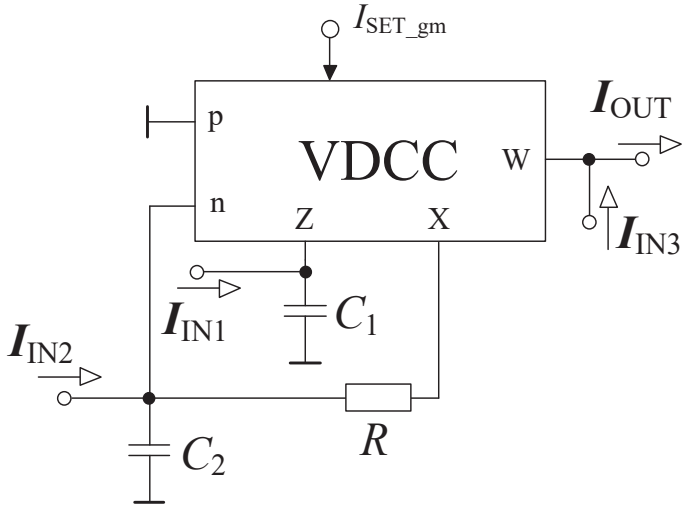


Fig. 5.26: MISO current–mode filter presented in [24] used for the conversion into its reconnection–less reconfigurable form

The structure in Fig. 5.26 employs single VDCC, two capacitors and one resistor. The filter offers LP, BP, HP, BS and AP transfer functions and has three inputs when a manual reconnection of particular input, their suitable combination, or the necessity of the amplified value of the input current is required in order to obtain all available transfer functions. The transfer function of the filter is expressed as:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{I}_{OUT}}{\boldsymbol{I}_{IN}} = \frac{\boldsymbol{I}_{IN1}\boldsymbol{s}C_2G - \boldsymbol{I}_{IN2}(\boldsymbol{s}C_1G + g_mG) + \boldsymbol{I}_{IN3}(\boldsymbol{s}^2C_1C_2 + \boldsymbol{s}C_1G + g_mG)}{\boldsymbol{s}^2C_1C_2 + \boldsymbol{s}C_1G + g_mG}, \tag{5.27}$$

where G stands for the conductance of resistor R.

The available output responses are obtained as follows:

- BP function for $\boldsymbol{I}_{IN1}$ being used, $\boldsymbol{I}_{IN2} = \boldsymbol{I}_{IN3} = 0$,
- LP function for $\boldsymbol{I}_{IN1}$ and $\boldsymbol{I}_{IN2}$ being used, $\boldsymbol{I}_{IN3} = 0$,
- HP function for $\boldsymbol{I}_{IN2}$ and I_{IN3} being used, $\boldsymbol{I}_{IN1} = 0$,
- BS function for $\boldsymbol{I}_{IN3}$ and inversion of $\boldsymbol{I}_{IN1}$ being used, $\boldsymbol{I}_{IN2} = 0$,
- AP function for $\boldsymbol{I}_{IN3}$ and inversion of double value of $\boldsymbol{I}_{IN1}$ being used, $\boldsymbol{I}_{IN2} = 0$.

The relations for the angular frequency ω_0 and quality factor Q are derived as:

$$\omega_0 = \sqrt{\frac{g_m G}{C_1 C_2}}, \tag{5.28}$$

$$Q = \sqrt{\frac{C_2 g_m}{C_1 G}}. \tag{5.29}$$

Design proposal

In order to create a reconnection–less reconfigurable filter from the topology in Fig. 5.26, given structure has been complemented by an IOGC–CA. This modification has been done in order to distribute the input current to each node and to provide its amplified/attenuated value (if necessary), changing the filtering structure into a single–input single–output filter. Each original input current ($\boldsymbol{I}_{IN1}$, $\boldsymbol{I}_{IN2}$ and $\boldsymbol{I}_{IN3}$) can be now distributed by transfer branches having electronically adjustable gains B_1, B_2 and B_3. Consequently, this modification transforms any MISO filter into a reconnection–less reconfigurable SISO filter. The internal block concept of the IOGC–CA, used in this case, is created with help of a CCCII with four outputs and multipliers (both available in the chip package [125]) as presented later in Fig 6.8. The current conveyor part of the IOGC–CA offers the copies of the input current. The multipliers together with resistive loads provide the electronically adjustable transfers of these individual outputs. The current gain of an individual output of the IOGC–CA is given as follows: the current from the output of the current conveyor is transferred into voltage by the resistor R. Then, this voltage is applied to the voltage input of a multiplier and transferred back to current based on the electronically controllable transconductance g_m. Thus, the resulting output current (current gain of specific output) depends on the product between the value of resistor R which is fixed (1 kΩ) and transconductance g_m which is adjusted by the DC voltage. Therefore, the control voltage (labeled as V_{SET_B}) is driving the transconductance and results in the adjustment of the current gain as well. This solution has been made due to the lack of a suitable current amplifier (and simulation model) implemented in the used CMOS process in our case.

Some orientations/polarities of the outputs of the active elements within the filter in Fig. 5.26 have been altered. The inversion of the input current is required only for one specific function (formerly, the inversion was required in case of two functions: BS and AP). As a result, LP and BS functions are now inverting. Nonetheless, this is not an issue. The multiplier provides both polarities/orientations of the output current in comparison to standard commercially available devices. The last modification, forming the resulting topology, involves the removal of the resistor R in the filtering structure (Fig. 5.26) since the used current conveyor has an electronically adjustable intrinsic resistance of its X input (R_X). It decreases the number of passive elements within the filter topology, and it also enables the electronic adjustability of the pole frequency f_0 and quality factor Q (g_m is controlled by V_{SET_gm}, R_X is controlled by I_{SET_RX}). The pole frequency and quality factor (in case of the original filter from Fig. 5.26) were tuned by the change of the transconductance g_m and the change of the value of the resistor R. The resulting structure of the proposed reconnection–less reconfigurable filter is shown in Fig. 5.27. The circuit involves one VDCC, one IOGC–CA and two grounded capacitors. The inner topology of the VDCC (Fig. 3.17) was created by OTA solution presented in Fig. 3.4 and CCII made by the CCCII cell [125]. The inner topology of the IOGC–CA has been made by CCCII, multiplication units and resistors as shown in Fig. 6.8. The expected power consumption (of the filter in Fig. 5.27) is 64.8 mW.

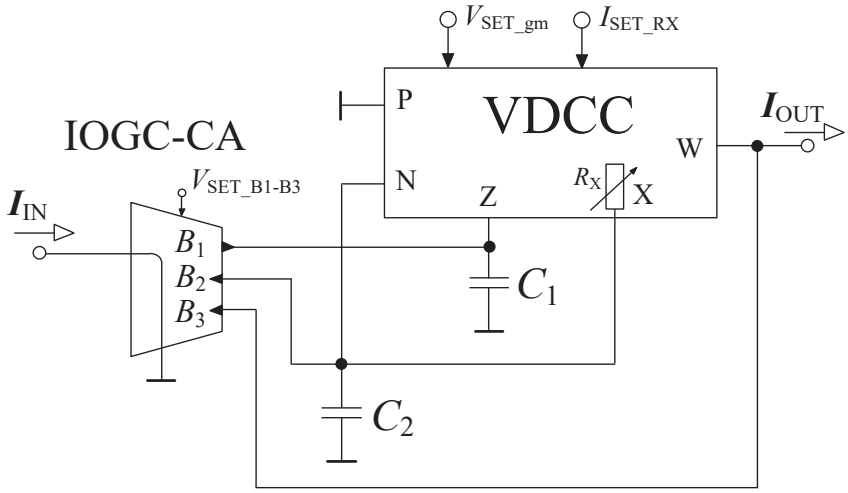


Fig. 5.27: Proposed reconnection–less reconfigurable filter created from the MISO filter from [24]

The transfer function of the filter in Fig. 5.27 is expressed as:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{I}_{OUT}}{\boldsymbol{I}_{IN}} = \frac{-B_1\boldsymbol{s}C_2G_X - B_2(\boldsymbol{s}C_1G_X + g_mG_X) + B_3(\boldsymbol{s}^2C_1C_2 + \boldsymbol{s}C_1G_X + g_mG_X)}{\boldsymbol{s}^2C_1C_2 + \boldsymbol{s}C_1G_X + g_mG_X}, \tag{5.30}$$

where G_X is equal to $1/R_X$. The angular frequency ω_0 and quality factor Q turned into:

$$\omega_0 = \sqrt{\frac{g_m G_X}{C_1 C_2}}, \tag{5.31}$$

$$Q = \sqrt{\frac{C_2 g_m}{C_1 G_X}}. \tag{5.32}$$

The available output responses use the setting (except already mentioned functions, it is also possible to obtain DT and HPZ (with a condition $B_1 + B_2 = 1$)) as stated in Tab. XII.

TABLE XII. OBTAINABLE OUTPUT TRANSFER FUNCTIONS BASED ON THE SETTING OF CURRENT GAINS

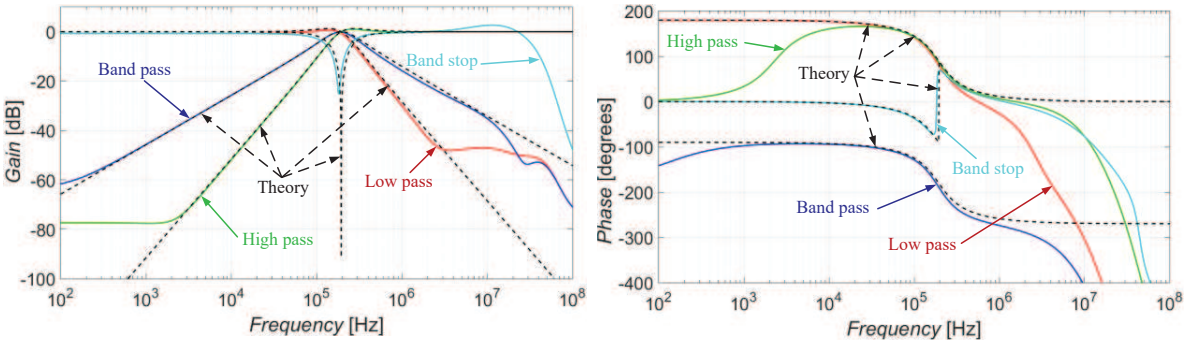
	B_1	B_2	B_3
LP	-1	1	0
HP	0	1	1
BP	1	0	0
BS	1	0	1
AP	2	0	1
HPZ	> 0	> 0	1
DT	0	0	1

The current gain $B = 1$ is obtained for $V_{SET\_B} = 0.5$ V, $B = 0$ is for $V_{SET\_B} = 0$ V and $B = 2$ for $V_{SET\_B} = 1$ V [125].

Design verification

The design has been verified my simulations in Cadence IC6 (spectre simulator) with help of simulation models of developed active elements. The numerical design has following specification: capacitors $C_1 = C_2 = 820$ pF, the value of transconductance g_m is set to 1 mS and the value of intrinsic resistance R_X is equal to 1 kΩ. Based on these values, the theoretical f_0 and Q are determined to be $f_0 = 194.1$ kHz and $Q = 1$ (no specific requirements were set, used values are solely for the demonstration of the circuit function). The setting of current gains B depends on selected output transfer function (the setting is given above).

The transfer characteristics of all standard 2nd–order transfer functions are presented in Fig 5.28 and Fig 5.29. Magnitude and phase characteristics of available functions: BP (blue lines), LP (red lines), HP (green lines) and BS (teal lines) obtained from simulations are compared with the theoretical expectations (black dashed lines) in Fig. 5.28 a), b), respectively. Figure 5.29 shows the magnitude (green line), phase (red line) and group delay (blue line) of AP filter compared with the theoretical traces (black dashed lines).



a) b)

Fig. 5.28: Comparison of simulated and theoretical functions of BP, LP, HP and BS: a) magnitude characteristics, b) phase characteristics

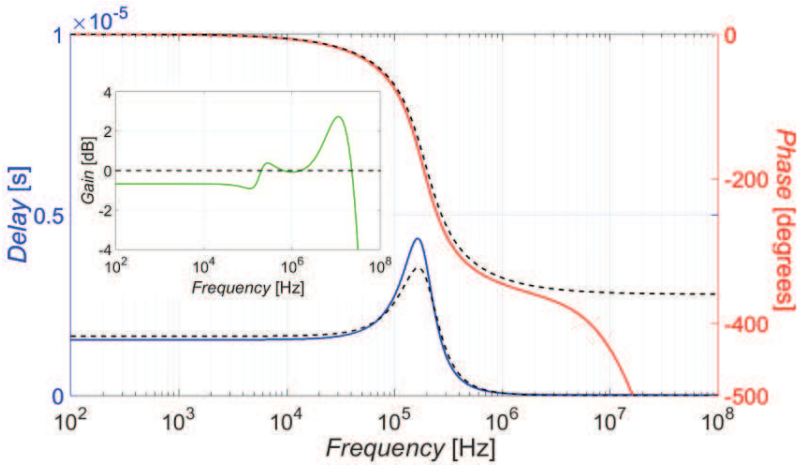


Fig. 5.29: Comparison of simulated and theoretical characteristics (magnitude, phase and group delay) of the AP filter

Figure 5.30 shows how the output response can be changed in accordance with the setting of current gains B_1 to B_3. We can start from HP function ($B_1 = 0$, $B_2 = 1$, $B_3 = 1$) over HPZ function ($B_1 = 0.01$, $B_2 = 0.99$, $B_3 = 1$ and $B_1 = 0.1$, $B_2 = 0.9$, $B_3 = 1$) to BS function ($B_1 = 1$, $B_2 = 0$, $B_3 = 1$). All these functions are a configured by electronically controllable parameters without any manual modification of the filtering structure.

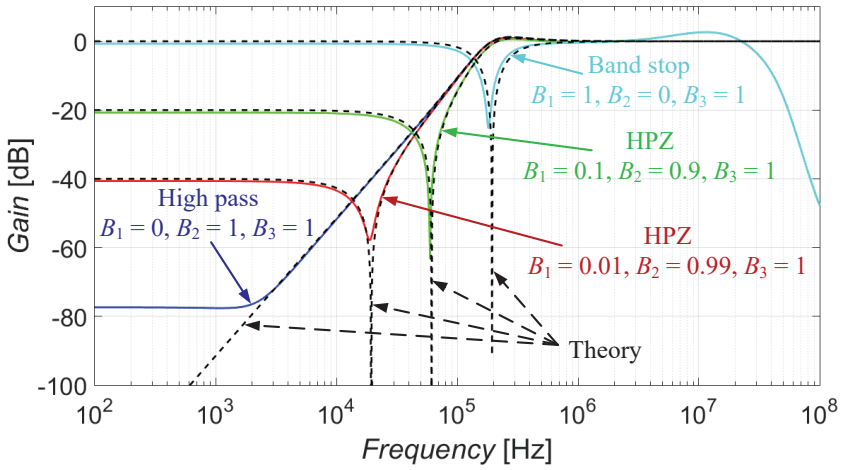


Fig. 5.30: Demonstration of the possibility to adjust the pass–band/stop–band area at lower frequencies by the change of current gains B_1 and B_2

The modification of given MISO filter, except for the feature of the reconnection–less reconfiguration, brings two additional available transfer functions (DT and HPZ) and the ability of the electronic adjustment of the pole frequency and quality factor.

Sensitivity analysis

The sensitivity analysis of the filter considers 8 parameters (C_1, C_2, g_m, n, G_X, B_1, B_2, and B_3). Parameter g_m is the transconductance of the OTA element within the VDCC, n stands for the transfer of the output of the CCII within the VDCC, G_X is the conductance inversely proportional to the intrinsic resistance R_X and parameters B_1, B_2, and B_3 are current gains of individual ACA elements.

The denominator considering these parameters has the following form:

$$D_{real}(\boldsymbol{s}) = \boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_1 G_X + g_m G_X \,. \tag{5.33}$$

The real numerator is given as:

$$\begin{aligned} N_{real}(\boldsymbol{s}) &= -B_1 \boldsymbol{s} C_2 G_X n - B_2(\boldsymbol{s} C_1 G_X n + g_m G_X n) + \\ &+ B_3(\boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_1 G_X + g_m G_X) \end{aligned} \,. \tag{5.34}$$

The sensitivities for the BP function (sensitivities for parameters B_2, and B_3 are not included as they are not present in the symbolical transfer of this function) are depicted in Fig. 5.31. The results for the LP function (B_3 is not included) is shown in Fig. 5.32 (B_3 is not included). All sensitivities are up to 1 except for the area around the pole frequency where the sensitivity is typically highest.

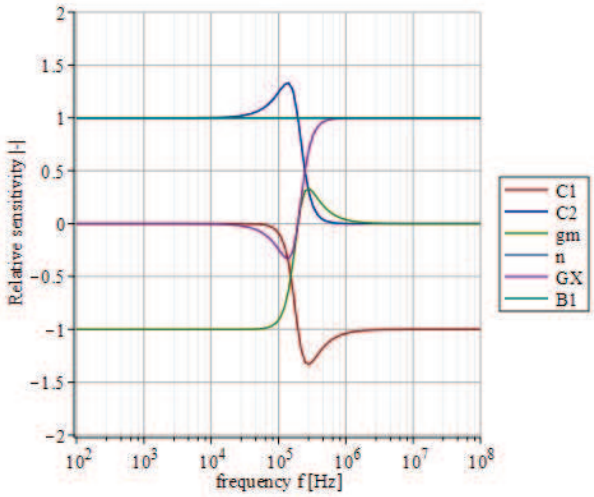


Fig. 5.31: Relative sensitivity of the BP function for individual parameters in dependence on the frequency

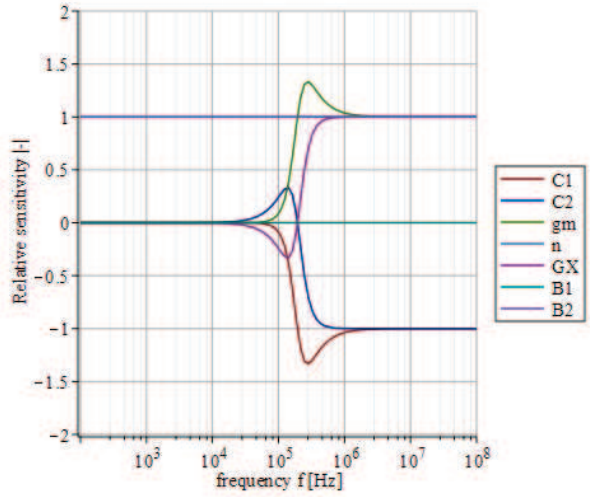


Fig. 5.32: Relative sensitivity of the LP function for individual parameters in dependence on the frequency

5.3 Structures created by VM to CM transformation

The proposals described in this chapter are created by the VM to CM transformation of existing reconnection–less reconfigurable filtering structures. The solution in subsection 5.3.1 employs CG–CCDDCC and VGA elements. The other design, introduced in subsection 5.3.2, uses OTA and ACA elements for its function.

5.3.1 Structure with four CG–CCDDCCs and one VGA

The filter is based on the transformation of the reconnection–less reconfigurable filter from [49]. The topology offers transfer functions of AP, BP, BS, HP, LP and 1st–order HP. In addition, the filter also provides functions of HPZ and LPZ. These advanced active elements (CG–CCDDCCs) have a special multiparameter adjustability. Therefore, we do not require simple active elements at specific places of the topology for reconfiguration of output

responses as well as adjustment of the value of the pole frequency and quality factor. As in previous cases, the proposed concept offers a possibility of the adjustment of pass–band and stop–band area within whole frequency band (B_{12} for high frequency band, A for middle frequency band and B_{22} for low frequency band). Furthermore, the design is subsequently complemented by a fractional–order passive element for the fractional–order behavior of transfer response (magnitude slope variation, etc.). The presented circuit architecture is published in [153] (International Conference on Electronics Circuits and Systems (ICECS) (ISBN: 978-1-7281-0996-1), 2019).

Design proposal

The designed reconnection–less reconfigurable filter is depicted in Fig. 5.33. The structure consists of four CG–CCDDCCs (based on suitable interconnection of OTA elements as suggested in Fig. 3.19, CMOS model from [49] has been used), one VGA (solved by another CG–CCDDCC with a resistor connected to its output), two resistors and two grounded capacitors. The power consumption is 24.2 mW.

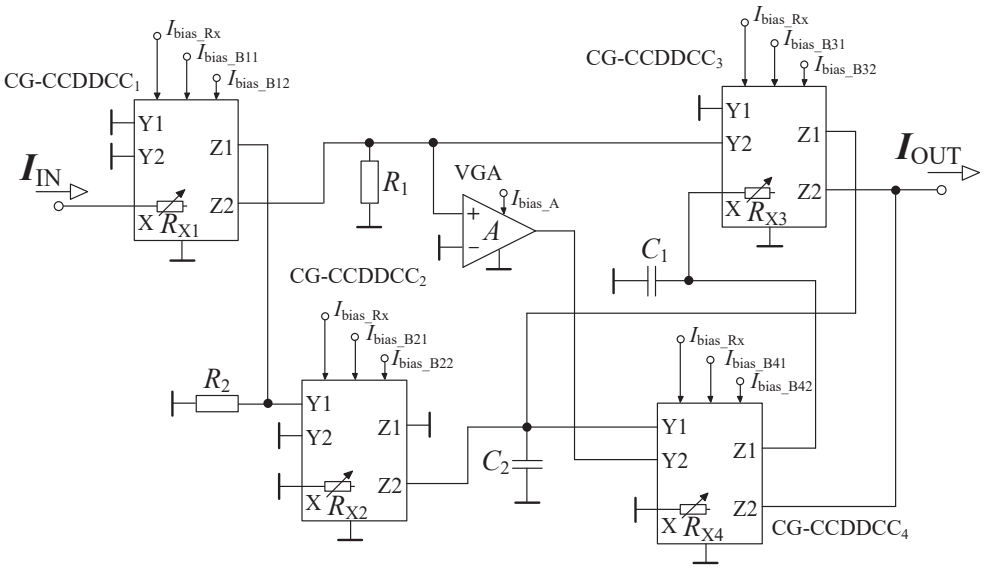


Fig. 5.33: Proposed reconnection–less reconfigurable filter with four CG–CCDDCCs and one VGA element

The transfer function of this filter is expressed as:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{s}^2 C_1 C_2 G_{X3} R_1 B_{12} - \boldsymbol{s} C_2 G_{X3} G_{X4} R_1 B_{12} A + G_{X2} G_{X3} G_{X4} R_2 B_{22}}{\boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 G_{X3} + G_{X3} G_{X4}}. \tag{5.35}$$

As already discussed, this design has been created by the VM to CM transformation of the structure from [49]. The proposed filter, in comparison to the structure from [49], contains one additional VGA element influencing the $\boldsymbol{s}^1$ term of the numerator of the transfer function.

Parameters G_{Xi} in (5.35) are equal to $1/R_{Xi}$. The first indexing number of parameter (I_{bias_Bxx}) refers to the CG–CCDDCC number in the structure, the second number is used for the designation of the particular output 1 for Z_1 and 2 for Z_2 (e.g., B_{31} refers to current gain of the Z_1 output of the third CG–CCDDCC). The transfer function (5.35) is shown in a simplified form (transfers of outputs Z_1 of the first (B_{11}), third (B_{31}) and fourth (B_{41}) CG–CCDDCC are equal to one, transfer of output Z_2 of the fourth CG–CCDDCC (B_{42}) is set to zero) due to better clarity. The BP transfer function has a special term ($\boldsymbol{s}C_1G_{X3}G_{X4}R_1B_{12}B_{42}$, transfer B_{32} is zero) than the $\boldsymbol{s}$ term given in the numerator of (5.35) since in (5.35) HP term of the numerator cannot be separated from BP term (BP term can be separated from HP term by setting $A = 0$, but not vice versa). Therefore, the resulting BP transfer function is obtained for different setting ($B_{42} = 1$) than other available functions. First order HP function takes form of $\boldsymbol{s}C_1G_{X3}R_1/(\boldsymbol{s}C_1+G_{X3})$. The complete setting of current gains/bias currents (transfer B_{31} is always set to 1) depending on the particular function is summarized in Tab. XIII. HPZ and LPZ have the same setting as BS function (as usual) with the exception: gain $B_{12} < 1$ in case of LPZ and gain $B_{22} < 1$ in case of HPZ. In this case of active device (Fig. 3.18), current gain $B = 1$ is obtained for $I_{bias\_B} = 100$ μA, $B = 0$ is for $I_{bias\_B} = 0$ A and $B < 1$ for $I_{bias\_B} < 100$ μA.

TABLE XIII. SETTING OF BIAS CURRENTS FOR INDIVIDAL AVAILABLE FUNCTION

	I_{bias_B12} [μA]	I_{bias_B22} [μA]	I_{bias_B32} [μA]	I_{bias_B41} [μA]	I_{bias_B42} [μA]	I_{bias_A} [μA]
LP	0	100	100	100	0	100
BP	100	0	0	100	100	0
HP	100	0	100	100	0	0
BS	100	100	100	100	0	0
AP	100	100	100	100	0	100
1st–order HP	100	100	100	0	0	100
HPZ	100	< 100	100	100	0	0
LPZ	< 100	100	100	100	0	0

The relations for the quality factor Q and angular frequency ω_0 of the filter are given by:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{G_{X3}G_{X4}}{C_1C_2}}, \tag{5.36}$$

$$Q = \sqrt{\frac{C_1G_{X4}}{C_2G_{X3}}}. \tag{5.37}$$

Thus, the electronic tuning of f_0 independently on Q can be achieved by the change of input resistances R_{X3} and R_{X4} as long as a simple condition $R_{X3} = R_{X4}$ is preserved.

Design verification

The simulations were carried out using Cadence IC6 (spectre simulator) software. The initial values of passive parts and filter parameters, chosen for the simulations, are as follows: $R_1 = R_2 = R_{X1} = R_{X2} = R_{X3} = R_{X4} = 1$ kΩ, $C_1 = C_2 = 1$ nF. These selected values result in the nominal pole frequency $f_0 = 159.2$ kHz and quality factor Q is equal to 1. Current gains B and voltage gain A are set in accordance with Tab. XIII depending on the specified transfer function.

Figure 5.34 illustrates obtained responses of BP, BS, HP and LP transfer functions compared to the ideal characteristics (black dashed lines). The simulation results and theoretical characteristics are in good correspondence with each other. Figure 5.35 shows the features (phase response (red line), gain (green line) and group delay (blue line)) of the all–pass function.

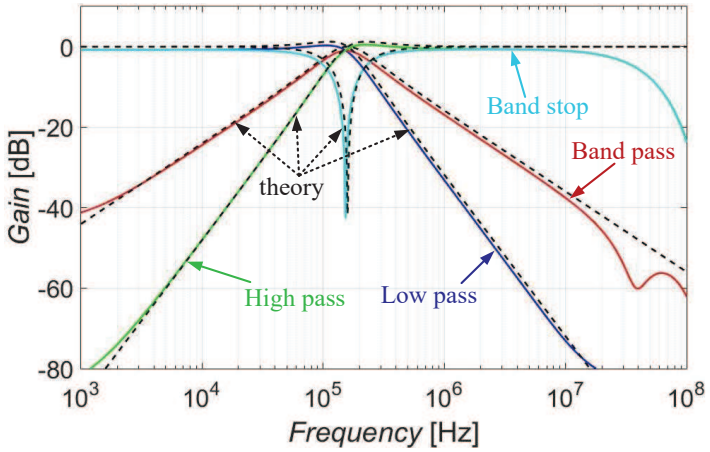


Fig. 5.34: Obtainable responses LP, HP, BP and BS – simulation (colored lines) and theoretical (black dashed lines) results

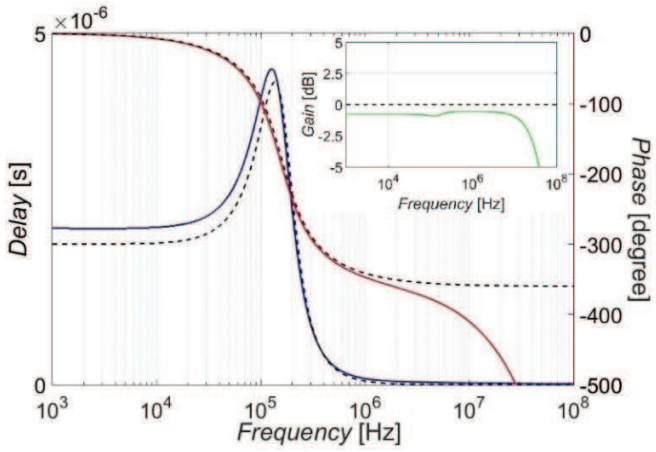


Fig. 5.35: Characteristics of AP function – gain (green line), group delay (blue line) and phase response (red line), theoretical characteristics (black dashed lines)

The electronic f_0 adjustability of the proposed filter is presented in Fig. 5.36. The BS function has been used for the demonstration. The bias currents (adjusting input resistances R_{X3} and R_{X4}) were set to 10 µA, 25 µA and 50 µA. It corresponds with values of $R_{X3} = R_{X4}$ equal to 1.71 kΩ, 1 kΩ and 843.8 Ω resulting in theoretical f_0 values 92.9 kHz, 159.2 kHz and 188.6 kHz. Table XIV provides a comparison of the theoretical and simulated values of f_0 for selected values of bias currents.

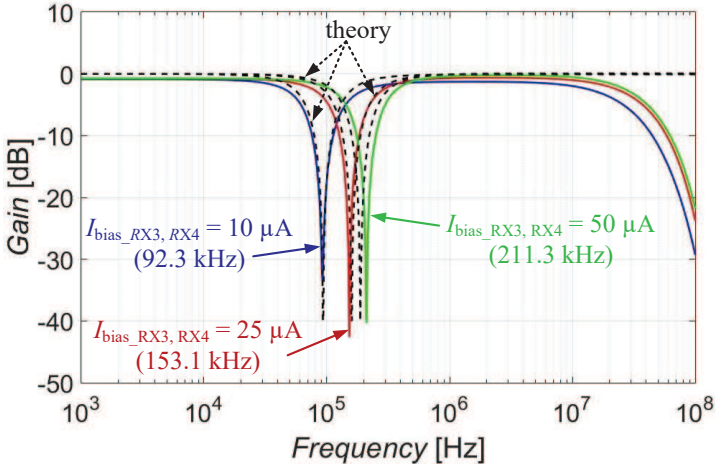


Fig. 5.36: Demonstration of the f_0 adjustment for I_{bias_RX3}, I_{bias_RX4} = 10 µA, 25 µA and 50 µA

TABLE XIV. ADJUSTMENT OF THE POLE FREQUENCY

$I_{bias\ RX3}$, $I_{bias\ RX4}$ [µA]	10	25	50
Theoretical f_0 [kHz]	92.9	159.2	188.6
Simulated f_0 [kHz]	92.3	153.1	211.3

The behavior of special functions HPZ and LPZ is demonstrated in Fig. 5.37. The HPZ and LPZ are modifications of the BS function. Thus, the setting of current gains/bias currents is similar to BS with following partial differences: $I_{bias\_Z2\ (1)}$ is set to 50 µA, 10 µA and 1 µA (B_{12} = 0.65, 0.195 and 0.025) in case of LPZ. The same values of bias currents/current gains are used for HPZ for $I_{bias\_Z2\ (2)}$ (B_{22}) instead of $I_{bias\_Z2\ (1)}$ (B_{12}).

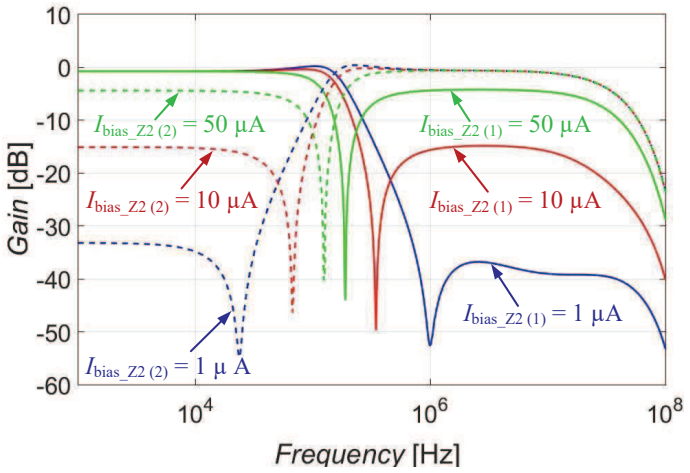


Fig. 5.37: Responses of LPZ (solid lines) and HPZ (dashed lines) for $I_{bias\_Z2\ (1)}$ (for LPZ) and $I_{bias\_Z2\ (2)}$ (for HPZ) equal to 50 µA, 10 µA and 1 µA

Fractional–order characteristics

Capacitor C_2 in the proposed structure has been replaced by a fractional–order capacitor $C_{2\alpha} = C_2\omega_0^{1-\alpha}$ (C_2 = 10 nF) obtained by the RC topology of Foster I [88] type shown in Fig. 5.38. The individual values of passive elements of the circuitry in Fig. 5.38 (based on specific value of parameter α) were calculated using Oustaloup approximation [96] and are summarized in Tab. XV (for FO LP transfer function). The values of all parameters of the current filter setting in Tab. XV together with the value of C_1 equal to 10 nF result in f_0 = 10 kHz (for given number of stages of the used RC structure, the operational bandwidth, where the approximation is valid, is approximately two decades).

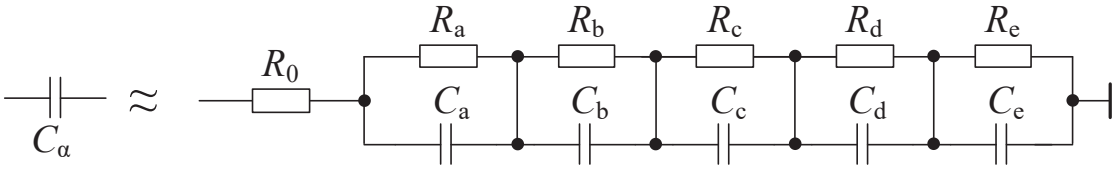


Fig. 5.38: 5th–order Foster I type RC structure used to approximate $C_{2\alpha}$

TABLE XV. VALUES OF RESISTORS AND CAPACITORS WITHIN THE RC STRUCTURE AND VALUES OF RX3 AND RX4 DEPENDING ON THE VALUE OF ALPHA

α [–]	**0.3**	**0.5**	**0.7**
$C_{2\alpha}$ [µF/sec$^{1-\alpha}$]	22.8	2.5	0.28
R_0 [Ω]	399.8	159.1	63.4
R_a [Ω]	284.3	164.2	77.5
R_b [Ω]	466.2	459.7	320.2
R_c [Ω]	821.4	1179.8	1196.8
R_d [Ω]	1457.6	3091.0	4674.7
R_e [Ω]	2942.6	10859.3	33656.6

α [–]	**0.3**	**0.5**	**0.7**
C_a [nF]	2.1	3.9	9.8
C_b [nF]	7.1	8.7	15.0
C_c [nF]	25.5	21.4	25.3
C_d [nF]	90.8	51.5	40.9
C_e [nF]	283.9	92.5	35.9
R_{X3} [Ω]	3851.6	2518.5	1709.1
R_{X4} [Ω]	768.0	1117.6	1571.0

The denominator of the resulting transfer function, calculated with help of general transfer functions of fractional order having Butterworth characteristics [63], takes form of:

$$D(s) = s^{1+\alpha} + s^{\alpha}\frac{G_{X3}}{C_1} + \frac{G_{X3}G_{X4}}{C_1 C_{2\alpha}}. \tag{5.38}$$

The values of input resistance R_{X3} and R_{X4} have to be adjusted depending on the value of α influencing the resulting value of the RC structure in order to correct value of the operational f_0. The values of R_{X3} and R_{X4} (included in Tab. XV) are calculated by the comparison of the specific term of (5.38) and transfer functions from [51].

The fractional–order responses of LP function (chosen to demonstrate the change of the order) for selected values of α (0.3, 0.5, 0.7) are shown in Fig. 5.39. The obtained values of the complete resulting order of the filter (n) are stated in the graph in Fig. 5.39.

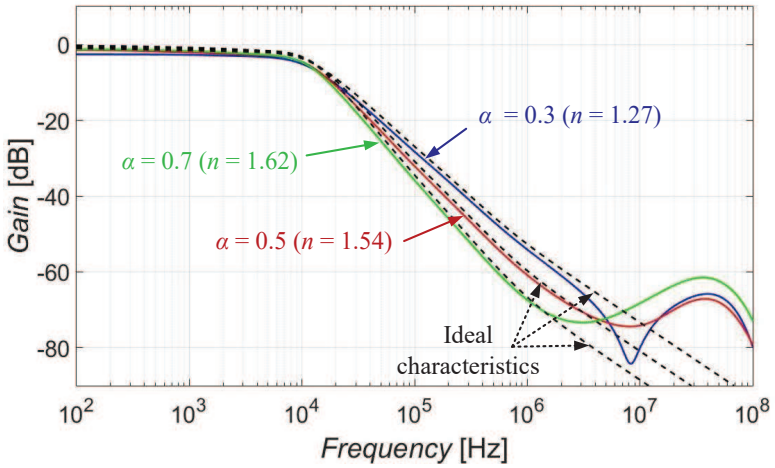


Fig. 5.39: LP function for orders 1.3, 1.5 and 1.7 – simulation results (colored lines) and ideal characteristics (black dashed lines)

Figure 5.40 illustrates available fractional–order functions LP, HP, BP (the function is asymmetrical, side to the left from f_0 follows the steepness of the integer order (2^{nd} order) while side to the right from f_0 is given by the by the currently used fractional order) and BS when $\alpha = 0.7$.

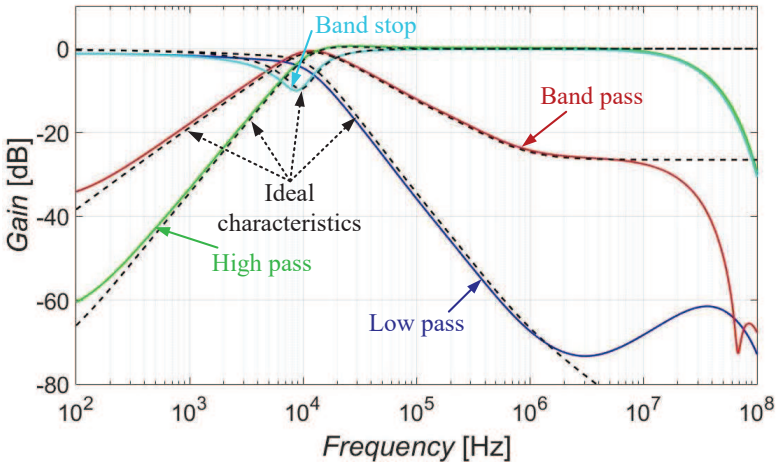


Fig. 5.40: Fractional–order LP, HP, BP and BS functions for $\alpha = 0.7$

5.3.2 Structure with two BOTAs, one OTA and two ACAs

The presented filter topology results from the transformation of the reconnection–less reconfigurable filter introduced in subsection 5.1.1. This proposal performs all standard 2nd–order functions together with additional HPZ, LPZ, DT and high–pass function of the 1st–order in dependence on current setting of electronically adjustable active elements (no topological modification or switching between inputs/outputs of the structure is required). The filter also offers the electronic tunability of its pole frequency and quality factor. In addition, the pass–band and stop–band areas of obtainable functions can be easily adjusted. The discussed research is available in [154] (International Conference Mixed Design of Integrated Circuits and Systems (MIXDES) (ISBN: 978-83-63578-15-2), 2019).

Design proposal

The proposed reconnection–less reconfigurable filter (shown in Fig. 5.41) consists of three OTA elements (two BOTA and one OTA), two ACA elements and two capacitors (C_1 is grounded and C_2 is virtually grounded through the low–impedance input of the ACA_1). The OTA element has been implemented by LT1228 device [127]. Since two OTAs in the circuit structure require inverting and non–inverting output (BOTAs) this element has been created by a combination of one LT1228 device (providing the transformation of voltage to current through its transconductance) and one current–mode multiplier implemented by EL4083 device [128] as presented in Fig. 3.5. The gain of EL4083 is fixed to 1. A lack of commercial availability of BOTAs leads to this arrangement. EL2082 device [130] has been used for the implementation of the ACA element (Fig. 3.10). This solution (based on given implementation) yields the power consumption of 610 mW. The transfer function of the proposed filter follows the equation:

$$K(s) = \frac{s^2 C_1 C_2 B_1 - s C_1 g_{m2} + g_{m1} g_{m3} B_2}{s^2 C_1 C_2 + s C_1 g_{m1} + g_{m1} g_{m3}}. \tag{5.39}$$

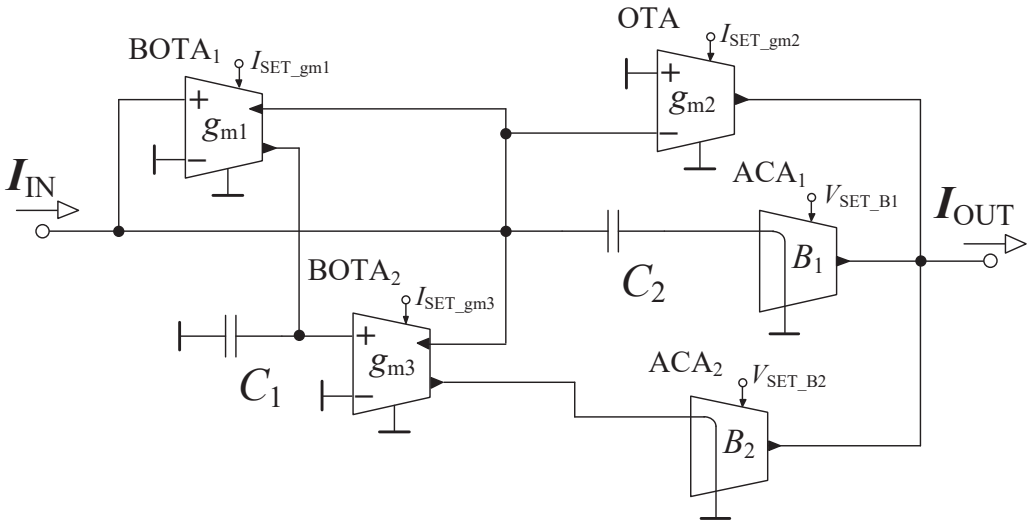


Fig. 5.41: Proposed reconnection–less reconfigurable filter based on OTA and ACA elements

The resulting output response depends on the setting of current gains (B_1, B_2) and transconductances (g_{m1} to g_{m3}). The specific setting for individual available transfer functions is summarized in Tab. XVI (the driving voltage 1 V corresponds with the value of B = 1, 100 μA corresponds with the value of g_m = 1 mS). The transfer function of the high–pass function of the 1st–order is given as $sC_2B_1/(sC_2+g_{m1})$.

The pole frequency f_0 and quality factor Q of the proposed filter are given by equations (5.40) and (5.41). The pole frequency f_0 can be tuned electronically without the impact on the quality factor by adjusting transconductances g_{m1} and g_{m3} when following a simple condition $g_{m1} = g_{m3}$. The quality factor Q can be adjusted electronically without the disturbance of f_0 by adjusting transconductances g_{m1} and g_{m3} in accordance with the condition $g_{m1} \cdot v = g_{m3}/v$, or $g_{m3} \cdot v = g_{m1}/v$ (where v is a real unsigned number and ratio must be preserved constant when f_0 tuned).

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{g_{m1} g_{m3}}{C_1 C_2}} \tag{5.40}$$

$$Q = \sqrt{\frac{C_2 g_{m3}}{C_1 g_{m1}}} \tag{5.41}$$

TABLE XVI. SETTING OF CONTROL CURRENTS/VOLTAGES IN DEPENDENCE ON INDIVIDUAL TRANSFER FUNCTION

	V_{SET_B1} [V]	V_{SET_B2} [V]	I_{SET_gm1} [μA]	I_{SET_gm2} [μA]	I_{SET_gm3} [μA]
AP	1	1	100	100	100
BS	1	1	100	0	100
HP	1	0	100	0	100
LP	0	1	100	0	100
BP	0	0	100	100	100
HPZ	1	< 1	100	0	100
LPZ	< 1	1	100	0	100
1st–order HP	1	0	100	0	0
DT	1	0	0	0	0

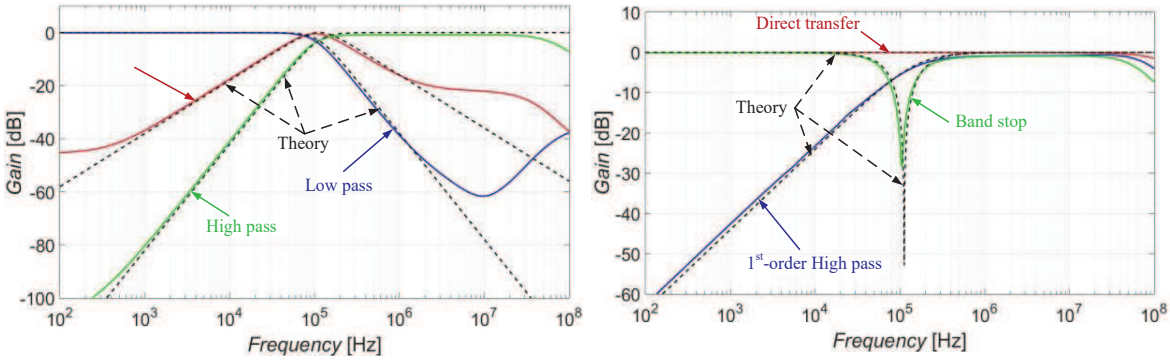
Design verification

The simulations results were carried out by PSpice simulation using active elements implemented by commercially available devices LT1228 [127], EL4083 [128] and EL2028 [130]. The numerical design of the filter has been set to the following nominal specification: transconductances $g_{m1} = g_{m2} = g_{m3} = 1$ mS, the values of capacitors $C_1 = 2$ nF and $C_2 = 1$ nF which results in $f_0 = 112.5$ kHz and $Q = 0.707$ (Butterworth approximation).

The available functions are shown in Fig. 5.42. Fig 5.42 a) depicts the output responses of LP, HP and BP function while Fig 5.42 b) illustrates the output responses of 1st–order HP, DT and BS function. The simulation results (solid colored lines) are compared with theoretical expectations (black dashed lines).

Figure 5.43 shows characteristics (magnitude, phase and group delay) of the all–pass transfer function. The magnitude is denoted by green solid line, phase by red solid line, group delay by blue solid line and the theory by black dashed lines.

The electronic adjustment of the pole frequency f_0 is demonstrated in Fig. 5.44 in case of the BS function. The electronic adjustment of f_0 was tested for three different settings of control currents $I_{SET\_gm1} = I_{SET\_gm3}$. The currents have values 50 μA, 100 μA and 200 μA which results in transconductances g_{m1} and g_{m3} equal to 0.5 mS, 1 mS and 2 mS providing theoretical pole frequencies 56.3 kHz, 112.5 kHz, 225.1 kHz. The values of f_0 (simulations) are stated in the graph and compared in Tab. XVII.



a) b)

Fig. 5.42: Output responses of: a) LP, HP and BP functions b) 1st–order HP, DT and BS functions

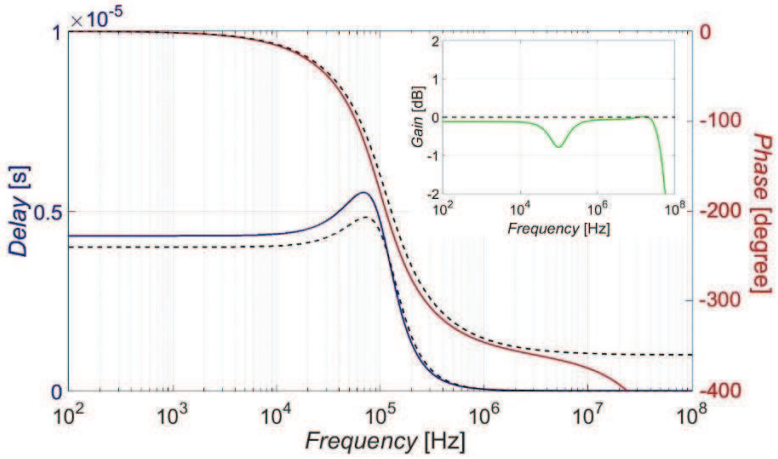


Fig. 5.43: Characteristics of AP output response – gain (green solid line), phase (red solid line), group delay (blue solid line) and theoretical expectations (black dashed lines)

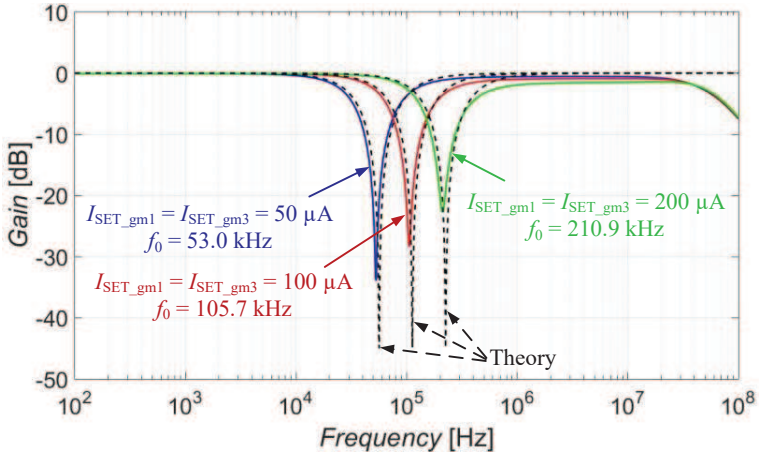


Fig. 5.44: Electronic adjustment of f_0 in case of BS function for three different setting of control currents I_{SET_gm1}, I_{SET_gm3}

TABLE XVII. ADJUSTMENT OF THE POLE FREQUENCY

I_{SET_gm1}, I_{SET_gm3} [µA]	50	100	200
Theoretical f_0 [kHz]	56.3	112.5	225.1
Simulated f_0 [kHz]	53.0	105.7	210.9

The demonstration of the electronic adjustment of the quality factor of the filter is presented in Fig. 5.45 (at BP response as example). The driving currents have been set to $I_{SET\_gm1} = I_{SET\_gm3} = 100$ µA, $I_{SET\_gm1} = 50$ µA, $I_{SET\_gm3} = 200$ µA and $I_{SET\_gm1} = 25$ µA, $I_{SET\_gm3} = 400$ µA that yield theoretical quality factors of 0.707, 1.41 and 2.83. The simulated values of Q (also stated in the graph) are provided in Tab. XVIII. Since the term of $\boldsymbol{s}$ variable in the numerator of the transfer function (5.39) is not equal to the $\boldsymbol{s}$ term of the denominator, the value of transconductance g_{m2} have the same value (simultaneous adjustment if necessary) as transconductance g_{m1} in order to keep the pass band gain at the same level (0 dB).

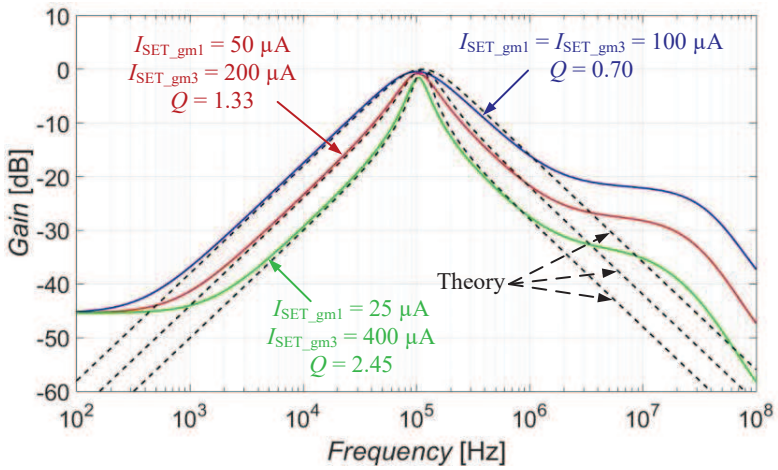


Fig. 5.45: Electronic adjustment of Q in case of BP function for three different setting of control currents I_{SET_gm1}, I_{SET_gm3}

TABLE XVIII. ADJUSTMENT OF THE QUALITY FACTOR

I_{SET_gm1} [µA]	100	50	25
I_{SET_gm3} [µA]	**100**	**200**	**400**
Theoretical Q [-]	0.707	1.41	2.83
Simulated Q [-]	0.70	1.33	2.45

Figure 5.46 illustrates the behavior of the special functions HPZ and LPZ. Figure 5.46 also demonstrates how the stop–band area of the available transfer functions at lower and higher frequencies can be easily adjusted. The pass–band area can be adjusted in the same way if necessary. The characteristics of HPZ are denoted by solid lines while the characteristics of LPZ by dashed lines. In order to obtain HPZ function, control voltage V_{SET_B2} has been set to values of 0.2 V, 0.05 V and 0.01 V (V_{SET_B1} is fixed to 1 V).

Analogical way of adjustment can be used for LPZ: V_{SET_B1} = 0.2 V, 0.05 V and 0.01 V and V_{SET_B2} fixed to 1 V.

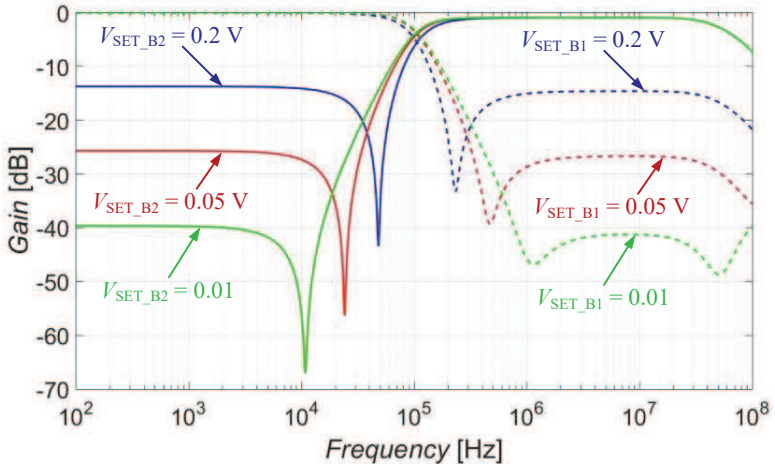


Fig. 5.46: Behavior of HPZ and LPZ functions for V_{SET_B1} (V_{SET_B2}) = 0.2 V, 0.05 V and 0.01 V

Sensitivity analysis

The results for the filter are further supplemented by a sensitivity analysis. We have to consider 9 parameters (C_1, C_2, g_{m11}, g_{m12}, g_{m2}, g_{m31}, g_{m32}, B_1 and B_2) Parameters g_{m11}, g_{m12}, g_{m2}, g_{m31}, and g_{m32} are transconductances of individual outputs of OTAs and parameters B_1 and B_2, are current gains of individual ACA elements.

The real denominator and numerator of given filter are expressed as:

$$D_{real}(s) = s^2 C_1 C_2 + sC_1 g_{m11} + g_{m12} g_{m31}, \tag{5.42}$$

$$N_{real}(s) = s^2 C_1 C_2 B_1 - sC_1 g_{m2} + g_{m12} g_{m32} B_2. \tag{5.43}$$

Functions of AP and BP have been selected for the presentation of the sensitivity of individual parameters. Figure 5.47 (AP) includes all parameters and Fig. 5.48 (BP) includes the sensitivities of C_1, C_2, g_{m11}, g_{m12}, g_{m2}, and g_{m31}. All sensitivities are up to 1.

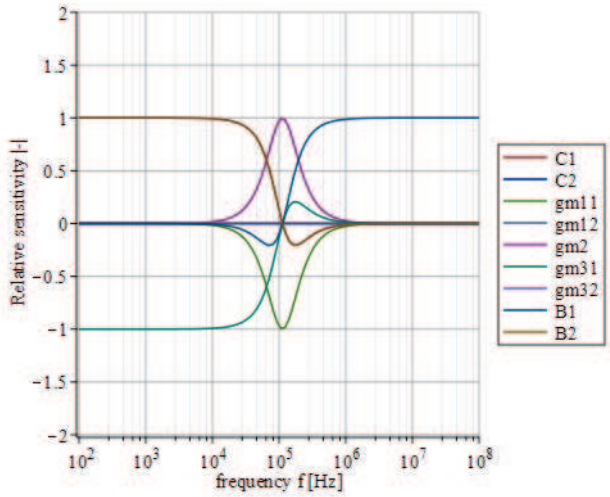


Fig. 5.47: Relative sensitivity of the AP function for individual parameters in dependence on the frequency

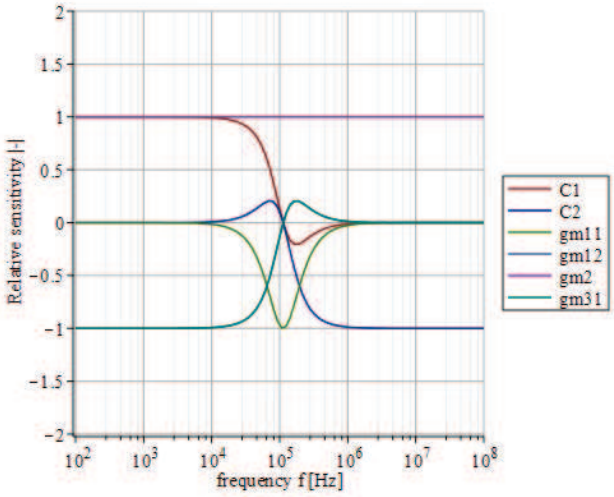


Fig. 5.48: Relative sensitivity of the BP function for individual parameters in dependence on the frequency

5.4 Structures created by SFGs method

This chapter contains a proposal designed by the signal flow graph method. This method has been beneficially used for the synthesis of the current–mode and voltage–mode structures and it may offer the best solution for the systematic design of filters allowing the widest reconfigurability and tunability at all. The filter can also work in mixed mode (voltage to current transfer functions).

5.4.1 Structure with three VGAs, three ACAs, two OTAs and one CF

The filter works in the current mode, voltage mode, and mixed mode (voltage to current) and offers sixteen transfer functions in total (7 in the CM, 7 in the VM, and 2 in case of voltage to current transfer). The designed structure has implemented the tunability of the pole frequency and quality factor and the adjustment of the stop–band/pass–band area

of available functions. The filter is presented in [155] (Elektronika ir Elektrotechnika (ISSN: 1392-1215), 2020).

Design proposal

The filter core utilizes single VDTA element in specific topological position. A current follower, variable gain amplifiers and adjustable current amplifiers are then added to the structure for the obtainment of further degrees of freedom in form of reconfigurability and tunability. The CF has been added for the HP response being taken from a high–impedance node. Otherwise, this response would be available as a current through C_1 (in case of the CM). The capacitor creates parasitic transfers in attenuated stop–bands without precise grounding [146]. VGAs and ACAs then provide the reconnection–less reconfiguration of the resulting output transfer. The VGAs were implemented by commercially available devices (linearly adjustable amplifiers) VCA822 [132] (Fig. 3.13) and ACAs are created by EL2082 devices [130] (Fig. 3.10) which are also commercially available. The inner structure of the VDTA (Fig. 3.16) was created by OTAs implemented by the UCC (Fig. 3.3). The CF element is also created by the UCC (Fig. 3.7). The power consumption of this solution (based on used implementation) has been estimated to 1.5 W.

The proposed filter is presented in Fig 5.49. The input voltage is distributed into different nodes of the filter since the voltage can be easily taken from one node and it does not require any additional active element to distribute the input voltage in comparison to the voltage summation. On the other hand, the currents of individual responses are summed up in one node for the CM as the current summation can be made without a necessity of an extra active element in comparison to the current distribution. The first OTA of the VDTA structure has been implemented by a multiple output element, so it gives one additional Z output (Z- in this case). The negative input of the second OTA is used as an input (labeled as v in Fig. 5.49). The capacitor C_1 and negative voltage inputs of the first and second OTA in the VDTA structure are virtually grounded through the outputs of VGA elements taking into consideration the fact that the voltage output has zero impedance in the ideal case.

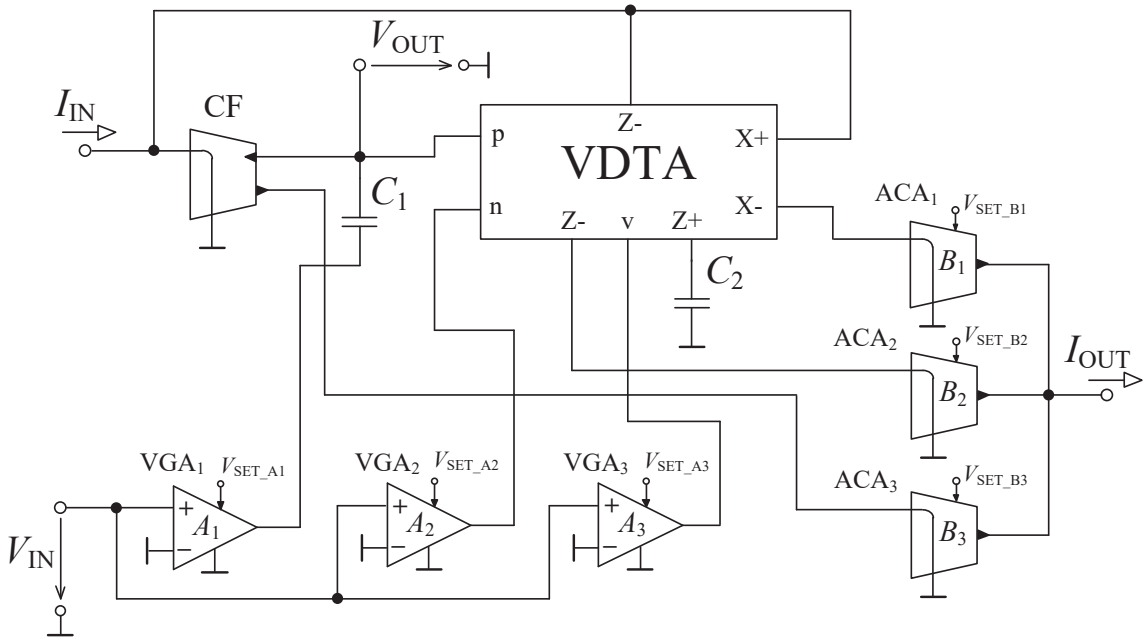


Fig. 5.49: Proposed dual–mode multifunctional reconnection–less reconfigurable filter

The denominator of the resulting transfer function has identical form for both the CM and VM:

$$D(\boldsymbol{s}) = \boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m1} + g_{m1} g_{m2}\,. \tag{5.44}$$

The numerator in case of the VM is:

$$N_{VM}(\boldsymbol{s}) = -\boldsymbol{s}^2 C_1 C_2 A_1 + \boldsymbol{s}(C_2 g_{m2} A_3 - C_2 g_{m1} A_2) - g_{m1} g_{m2} A_2\,, \tag{5.45}$$

and the numerator for the CM is:

$$N_{CM}(\boldsymbol{s}) = \boldsymbol{s}^2 C_1 C_2 B_3 - \boldsymbol{s} C_2 g_{m1} B_2 + g_{m1} g_{m2} B_1\,. \tag{5.46}$$

The resulting output response depends on the setting of voltage gains A for the VM, and current gains B for the CM, all controlled electronically by DC voltages. The filter provides all standard transfer functions (AP, BS, HP, BP, and LP) and functions HPZ and LPZ, all of them in both modes. The setting of control voltages in dependence on the resulting output response is stated in Tab. XIX. This filter also offers functions BP and HP (both polarities – inverting/noninverting) in the mixed mode (transadmittance) form (voltage to current transformation). The control voltages relate to voltage and current gains as follows: $A = 0$ for -1 V, $A = 1$ for 0 V, and $A = 2$ for 1 V when referring to the VGA and $B = 0$ for 0 V and $B = 1$ for 1 V in case of the ACA.

TABLE XIX. THE SETTING OF THE CONTROL VOLTAGES IN RELATION TO PARTICULAR OUTPUT RESPONSE

VM	**HP**	**BP**	**LP**	**BS**	**AP**	**HPZ**	**LPZ**
V_{SET_A1} **[V]**	0	-1	-1	0	0	0	< 0
V_{SET_A2} **[V]**	-1	-1	0	0	0	$A_2 = A_3$	0
V_{SET_A3} **[V]**	-1	0	0	0	1	< 0	0

CM	**HP**	**BP**	**LP**	**BS**	**AP**	**HPZ**	**LPZ**
V_{SET_B1} **[V]**	0	0	1	1	1	1	< 1
V_{SET_B2} **[V]**	0	1	0	0	1	0	0
V_{SET_B3} **[V]**	1	0	0	1	1	< 1	1

The pole frequency and quality factor of the filter in both cases are expressed as:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}\,, \tag{5.47}$$

$$Q = \sqrt{\frac{C_1 g_{m2}}{C_2 g_{m1}}}\,. \tag{5.48}$$

Therefore, f_0 can be adjusted without affecting Q by the change of g_{m1} and g_{m2} if a simple condition $g_{m1} = g_{m2}$ is fulfilled. Similarly, Q can be tuned without affecting f_0 by changing the ratio between g_{m1} and g_{m2} as long as the result of the multiplication of g_{m1} and g_{m2} remains the same.

Design verification

The verification of the design has been made with the help of PSpice simulations involving available simulation models of the UCC (substituting CF and OTA elements) and commercially available devices VCA822 and EL2082. The values of transconductances and capacitances were chosen to be $g_{m1} = g_{m2} = 1$ mS and $C_1 = C_2 = 1$ nF. Therefore, the theoretical values of the pole frequency and quality factor are equal to $f_0 = 159.2$ kHz and $Q = 1$.

The current mode transfer functions of BS, HP, BP, and LP obtained from the simulations are compared with the theoretical expectations in Fig. 5.50. Similarly, the same transfer functions for the voltage mode are presented in Fig. 5.51.

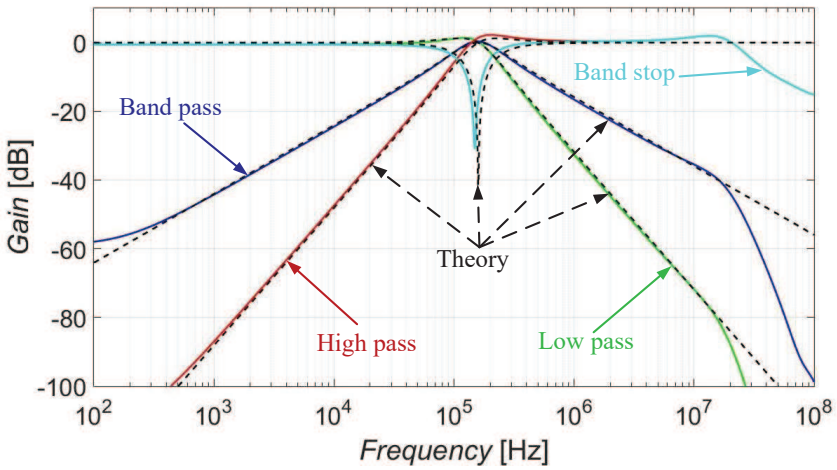


Fig. 5.50: Transfer functions of BS, HP, BP, and LP in case of the CM: simulation results (colored solid characteristics) and theory (black dashed characteristics)

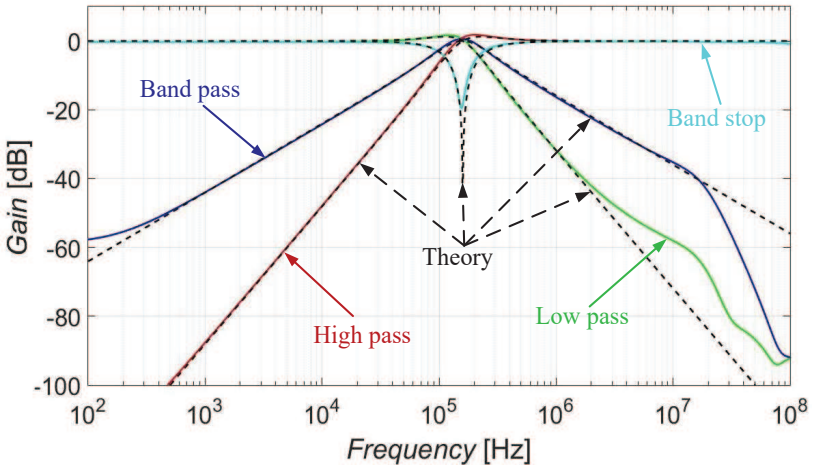


Fig. 5.51: Transfer functions of BS, HP, BP and LP in case of the VM: simulation results (colored solid characteristics) and theory (black dashed characteristics)

The band–stop function of the voltage mode has been selected for the presentation of the adjustability of f_0. This ability is demonstrated for five different settings of values of transconductances $g_{m1} = g_{m2}$. The chosen values are 560 µS, 750 µS, 1 mS, 1.33 mS, and 1.77 mS resulting in the theoretical f_0 of 89.1 kHz, 119.4 kHz, 159.2 kHz, 211.7 kHz, and 281.7 kHz. The obtained simulation results are depicted in Fig. 5.52.

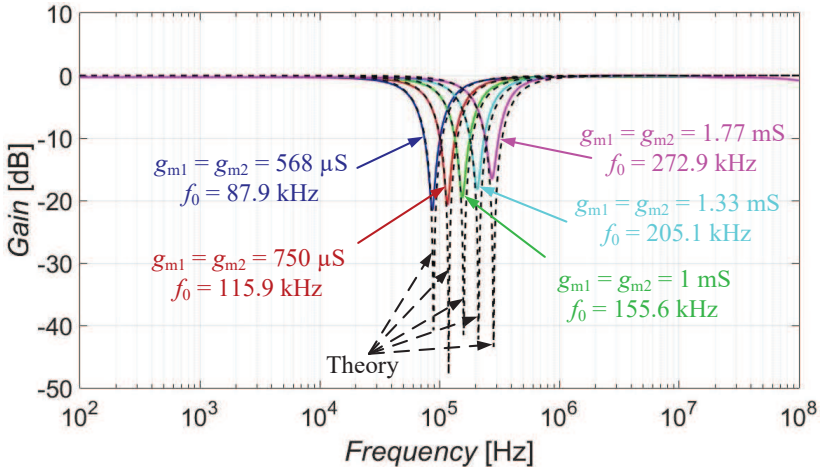


Fig. 5.52: Adjustability of f_0 demonstrated for five different settings of transconductances g_{m1} and g_{m2}

The values of f_0 (acquired from the simulation) are compared with the theoretical values in Tab. XX. It would be possible to provide the electronic adjustment of f_0 and Q by a different type of implementation of the OTA element. Unfortunately, the commercially available OTAs usually offer only one output. The extension of number of these outputs requires a parallel interconnection of several active elements (additional complexity).

TABLE XX. ADJUSTMENT OF THE POLE FREQUENCY

g_{m1}, g_{m2}	**560 µS**	**750 µS**	**1 mS**	**1.33 mS**	**1.77mS**
Theoretical f_0 [kHz]	89.1	119.4	159.2	211.7	281.7
Simulated f_0 [kHz]	87.9	115.9	155.6	205.1	272.9

The stop–band area (as much as the pass–band area) of available functions can be easily adjusted if required. It is demonstrated in Fig. 5.53 on the CM band–pass function. The stop–band area at lower frequencies can be controlled by the adjustment of the current gain B_1, while the stop–band area at higher frequencies can be adjusted by B_3. Similarly, the stop–band/pass–band areas of the VM functions can be adjusted by changing the value of A_2 for lower frequency band and A_1 for higher frequency band. This feature also allows special functions of HPZ, LPZ. The setting for the Fig. 5.53 uses values V_{SET_B1} (or V_{SET_B3}) = 0.1 V, 0.03 V, and 0.01 V. The colored solid lines show the adjustment of the higher frequency band of BP (controlled by B_3), and the colored dashed lines stand for the adjustment of the lower frequency band of BP (controlled by B_1).

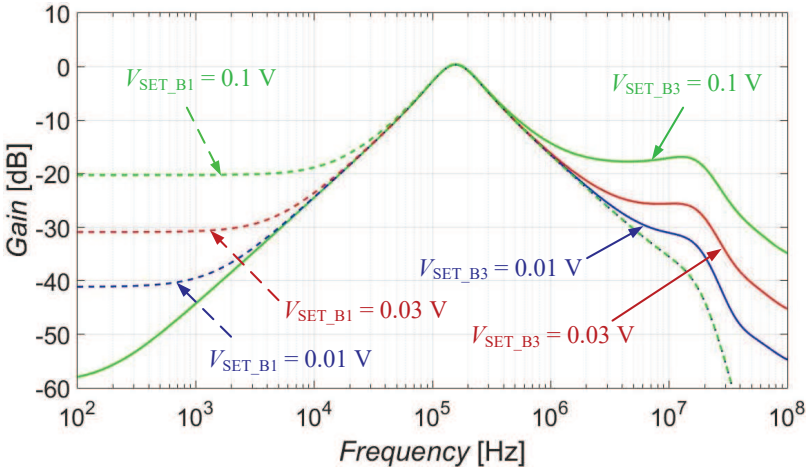


Fig. 5.53: Demonstration of the adjustability of the stop–band areas of the CM band–pass function for various settings

Sensitivity analysis

The sensitivity analysis of the circuit structure involves 12 parameters (C_1, C_2, g_{m11}, g_{m12}, g_{m13}, g_{m21}, g_{m22}, n_1, n_2, B_1, B_2, and B_3) when working in the CM and 9 parameters (C_1, C_2, g_{m11}, g_{m12}, g_{m21}, n_1, A_1, A_2, and A_3) in the VM. Parameters g_{m11}, g_{m12}, g_{m13}, g_{m21}, and g_{m22} are transconductances of individual outputs of OTA elements within the VDTA, n_1 and n_2 are transfers of individual outputs of the CF, parameters B_1, B_2, and B_3 are current gains of individual ACA elements, and, finally, A_1, A_2, and A_3 stand for the voltage gains of VGAs.

The corresponding denominator (common for both current and voltage modes) considering these parameters takes a form of:

$$D_{real}(\boldsymbol{s}) = \boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m11} n_1 + g_{m12} g_{m21} n_1 . \tag{5.49}$$

The real numerators of the filter working in the CM and VM are given by the following equations:

$$N_{real\_CM}(\boldsymbol{s}) = \boldsymbol{s}^2 C_1 C_2 n_2 B_3 + \boldsymbol{s} C_2 g_{m13} n_1 B_2 + g_{m12} g_{m22} n_1 B_1 , \tag{5.50}$$

$$N_{real\_VM}(\boldsymbol{s}) = \boldsymbol{s}^2 C_1 C_2 A_1 + \boldsymbol{s}(C_2 g_{m11} n_1 A_2 - C_2 g_{m21} n_1 A_3) + g_{m12} g_{m21} n_1 A_2 . \tag{5.51}$$

Figure 5.54 shows the results for the HP function in case when the proposed filter operates in the current mode (sensitivities for parameters g_{m12}, g_{m22}, B_1, and B_2 are zero because these parameters are not presented in the ideal symbolical transfer form for the HP function), and Fig. 5.55 presents the results for the LP function in case of the VM (sensitivity of A_1 is zero). All sensitivities are relatively low (around the typical value of 1, with the highest sensitivity around the pole frequency of the filter (159.2 kHz)).

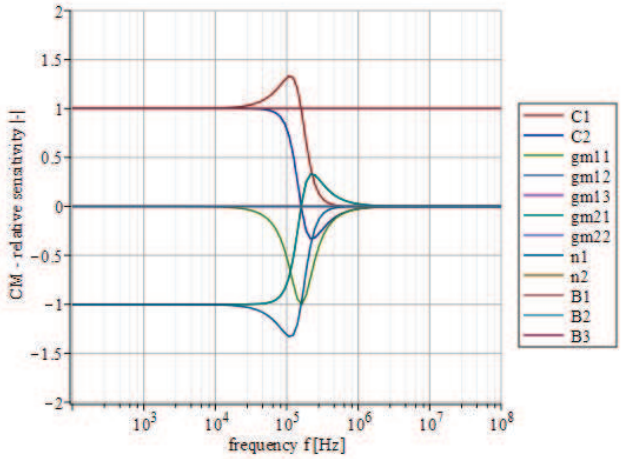


Fig. 5.54: Relative sensitivity of the HP function of the CM for individual parameters in dependence on the frequency

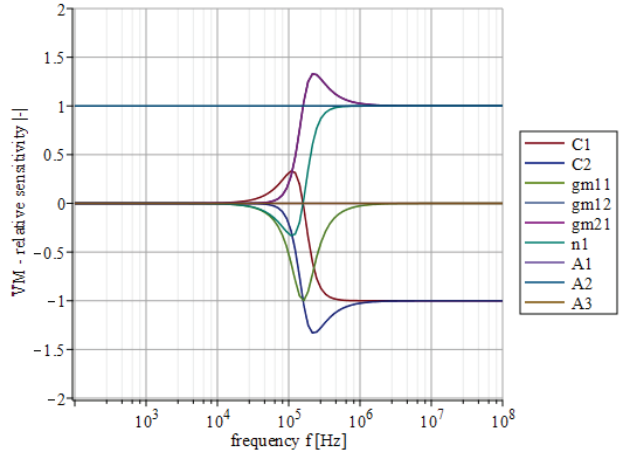


Fig. 5.55: Relative sensitivity of the LP function of the VM for individual parameters in dependence on the frequency

5.5 Structures of reconnection–less reconfigurable filters of higher orders

The designs described in this section target on structures of orders higher than 2nd (the 3rd–order in subsection 5.5.1 and the 4thorder in subsection 5.5.2). Individual values of parameters of solved structures are calculated by the NAF software [142] in order to obtain the desired pole frequency and approximation characteristics of resulting transfer functions.

5.5.1 Structure based on the third–order IFLF topology

The introduced filter is a 3rd–order filter based on Inverse Follow–the–Leader feedback (IFLF) [133] topology offering 13 transfer functions (LP function of the 3rd, 2nd and 1st order, HP function of the 3rd and 2nd order, BP function of the 2nd order, asymmetrical BP 20/40 dB (low frequency slope/high-frequency slope) per decade and 40/20 dB per decade, two BS functions, AP function of the 2nd and 1st order and inverting direct transfer (IDT)). All

transfers are reconfigurable electronically. Furthermore, the topology offers the electronic adjustment of its pole frequency. The proposed design has been published in [156] (International Symposium on Circuits and Systems (ISCAS) (ISBN:978-1-7281-3320-1), 2020).

Design proposal

The core of the presented topology is formed by OTA elements. The OTAs were created by the UCC chip as shown in Fig. 3.3. Since each chip contains single UCC together with single CCII±, the single output OTA elements in the filter structure were implemented using the CCII± from the chip. This implementation does not offer the electronic control of the transconductance. Nonetheless, commercially available devices with the electronic control of their transconductance usually have only one output. However, OTA_3 in the proposed structure requires four outputs. The input current distribution is solved by the current amplifier with individual gain control of each output (IOGC–CA) comprising the UCC and EL2082 devices [130] as depicted in Fig. 6.3 a). The IOGC–CA uses simplified concept without adjustable intrinsic resistance since this feature is not necessary in this case. The power consumption of 584.8 mW is expected.

The proposed filter, depicted in Fig. 5.56, employs three OTA elements (two with single output and one with four outputs), one IOGC–CA element and three capacitors (all grounded). The transfer function is given as $K(\boldsymbol{s}) = \boldsymbol{I}_{OUT}/\boldsymbol{I}_{IN} = N(\boldsymbol{s})/D(\boldsymbol{s})$ where:

$$N(\boldsymbol{s}) = \boldsymbol{s}^3 B_3 C_1 C_2 C_3 + \boldsymbol{s}^2 (B_3 C_1 C_2 g_{m3} - B_2 C_1 C_2 g_{m3}) + \\ + \boldsymbol{s}(B_3 C_1 g_{m2} g_{m3} - B_1 C_1 g_{m2} g_{m3}) + B_3 g_{m1} g_{m2} g_{m3} - B_0 g_{m1} g_{m2} g_{m3}, \tag{5.52}$$

$$D(\boldsymbol{s}) = \boldsymbol{s}^3 C_1 C_2 C_3 + \boldsymbol{s}^2 C_1 C_2 g_{m3} + \boldsymbol{s} C_1 g_{m2} g_{m3} + g_{m1} g_{m2} g_{m3}. \tag{5.53}$$

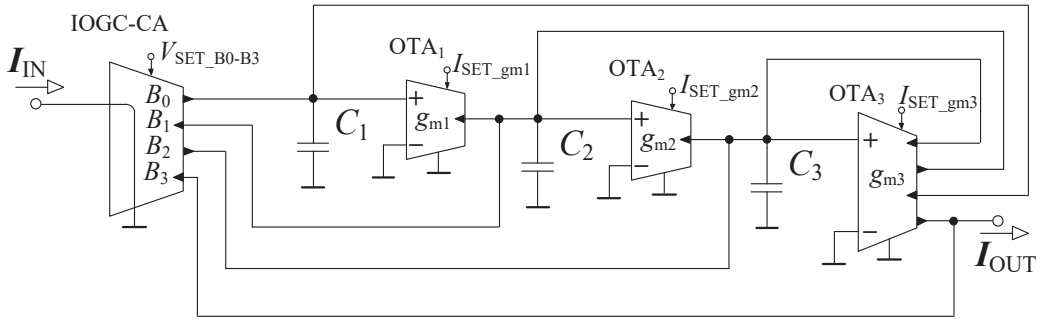


Fig. 5.56: Proposed 3rd–order reconnection–less electronically reconfigurable filter

The resulting output response depends on current setting of current gains B_0 to B_3 (adjustable by DC control voltages V_{SET_B0} to V_{SET_B3}). A list of available transfer functions

based on the setting of V_{SET_B0} to V_{SET_B3} is given in Tab XXI. Standard approximations cause non-unity pass-band gain of some transfer functions for high–order design (especially BP having gain at center frequency). Note that magnitude responses are modified in this way for pass-band gain being equal to 0 dB (in inverting/noninverting form). It is easily available due to electronic adjustment of the filtering structure. The value of the control voltages is directly proportional to the resulting value of the current gain.

TABLE XXI. AVAILABLE TRANSFER FUNCTIONS IN ACCORDANCE WITH THE CONTROL VOLTAGES CONFIGURATIONS

function	V_{SET_B0} [V]	V_{SET_B1} [V]	V_{SET_B2} [V]	V_{SET_B3} [V]
LP (3rd–order)	1	0	0	0
BP (20/40 dB/dec)	0	0.75	0	0
LP (2nd–order)	1	0.25	0	0
BP (40/20 dB/dec)	0	0	0.75	0
BP (2nd–order)	0	0.5	0.5	0
LP (1st–order)	1	0.5	0.5	0
IDT	0	0	0	1
BS (2nd–order)	0	0.8	0	1
HP (2nd–order)	1	1	0	1
BS (2nd–order)	0	0	0.8	1
AP (2nd–order)	0	1	1	1
HP (3rd–order)	1	1	1	1
AP (1st–order)	2	1	1	1

Design verification

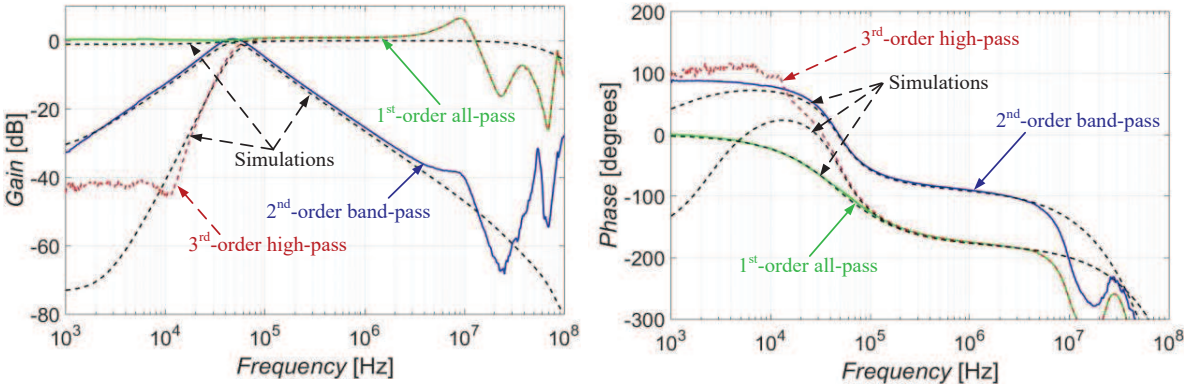
The simulation results were carried out in PSpice software. Furthermore, the filter has been implemented in form of a printed circuit board (PCB) in order to perform experimental measurements. The first step of the numerical design starts with NAF software for the calculation of individual coefficients of the transfer function in dependence on the desired order of the filter and used approximation. The following parameters of tolerance field (for Butterworth approximation and LP prototype) were used: the pole frequency $f_0 = 47$ kHz, transfer in pass–band $K_P = -3$ dB, the stop–band frequency $f_s = 470$ kHz, transfer in stop–band $K_S = -60$ dB.

The calculated coefficients of the denominator for this configuration yield:

$$\begin{aligned} b_3 &= 1, \\ b_2 &= 5.995 \cdot 10^5, \\ b_1 &= 1.797 \cdot 10^{11}, \\ b_0 &= 2.694 \cdot 10^{16}. \end{aligned} \tag{5.54}$$

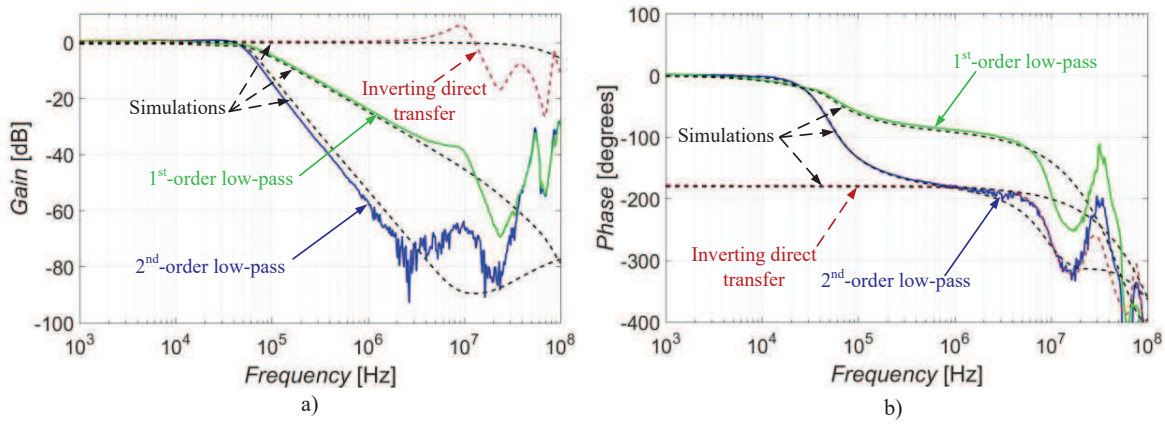
Applying the coefficients from (5.54) into (5.53), while selected values of capacitors are $C_1 = C_2 = C_3 = 1$ nF, the calculation results in values of transconductances $g_{m3} = b_2C_3 = 150$ µS, $g_{m2} = (b_1C_2C_3)/g_{m3} = 300$ µS and $g_{m1} = (b_0C_1C_2C_3)/(g_{m2}g_{m3}) = 600$ µS.

The simulated and measured results of selected responses are compared in Fig. 5.57 and Fig. 5.58. Fig. 5.57 shows output responses of the 3rd–order HP, 2nd–order BP and 1st–order AP while Fig. 5.58 displays transfer functions of inverting direct transfer, 2nd–order LP and 1st–order LP.



a) b)

Fig. 5.57: Transfer functions 3rd–order HP, 2nd–order BP and 1st–order AP: a) magnitude characteristics, b) phase characteristics



a) b)

Fig. 5.58: Transfer functions IDT, 2nd–order LP and 1st–order LP: a) magnitude characteristics, b) phase characteristics

The pole frequency of the filter can be easily tuned by values of the transconductances g_{m1}, g_{m2} and g_{m3} (as long as the ratio between them is preserved constant (ratio 1:2:4)). This tunability is demonstrated at the 3rd–order LP function in Fig. 5.59 for three different settings ($g_{m1} = 75$ µS, $g_{m2} = 150$ µS, $g_{m3} = 300$ µS; $g_{m1} = 150$ µS, $g_{m2} = 300$ µS, $g_{m3} = 600$ µS; and $g_{m1} = 300$ µS, $g_{m2} = 600$ µS, $g_{m3} = 1200$ µS) resulting in the theoretical pole frequency of 23.8 kHz, 47.4 kHz and 94.6 kHz. Obtained simulated and measured frequencies are compared in Tab. XXII.

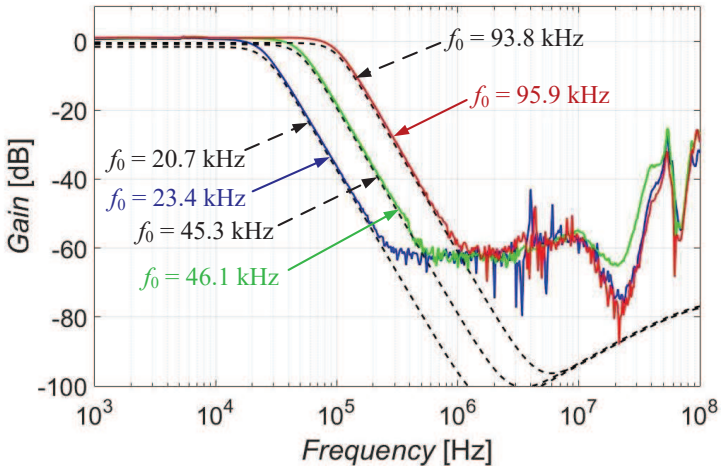


Fig. 5.59: Possibility of f_0 tuning in case of the 3rd–order LP function for three different configurations of the transconductances

TABLE XXII. SUMMARY OF THEORETICAL, SIMULATED AND MEASURED POLE FREQUENCIES

Theoretical f_0 [kHz]	**23.8**	**47.4**	**94.6**
Simulated f_0 [kHz]	20.7	45.3	93.8
Measured f_0 [kHz]	23.4	46.1	95.9

5.5.2 Structure based on the fourth–order leap–frog topology

The solution, introduced in this subsection, uses a 4th–order leap–frog topology [138] as its basic prototype. The filter operates in the CM and provides LP functions of the first, second, third and fourth order. The topology employs OTA elements. The additional current amplifier with adjustable gain of each output independently (IOGC–CA) offers the reconnection–less reconfiguration of the resulting filtering response of this structure. The FO characteristics and behavior are obtained by the stepwise replacement of integer–order capacitors (in the structure) by their FO counterparts (RC ladder networks/approximants). Such modification generates FO LP transfer functions of various orders as: LP 3 + α, LP 2 + α, LP 1 + α, LP 2 + α + β, LP 1 + α + β, LP 1 + α + β + γ, LP α + β + γ and LP α + β + γ + δ. The possibility of the electronic tuning of the order of FO device is also discussed and presented. Paper [157] (Journal of Advanced Research (ISSN: 2090-1232), 2020) introduces this research.

Design proposal

The proposed structure was firstly designed in its integer–order form. Its FO counterpart is described later. The initial topology of this circuit results from the SFG synthesis of a 4th–order leap–frog topology. The filter is working in the current mode. The input current is applied to different circuit nodes via electronically controllable current gains in order to ensure the reconnection–less reconfiguration of the transfer function. The proposed

(simplified) signal–flow graph of the filtering structure is depicted in Fig. 5.60 (after the elimination of the self loops for easier calculation since all determinants are now equal to 1).

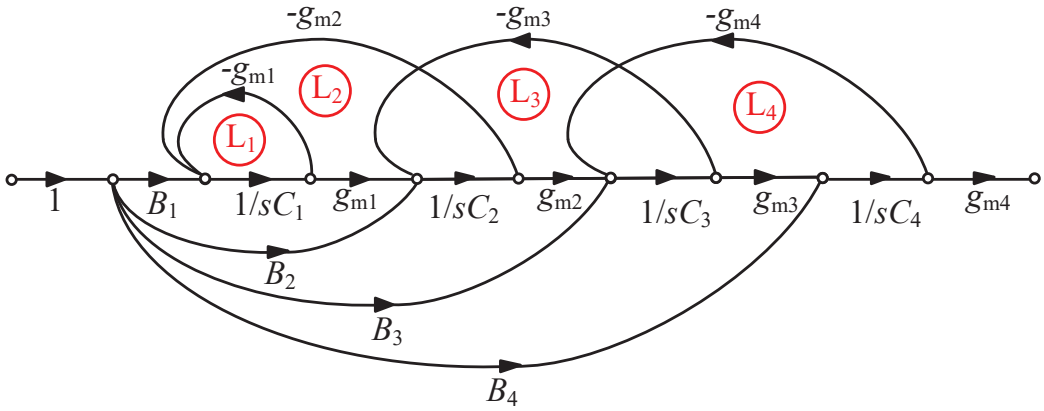


Fig. 5.60: Simplified signal–flow graph of the proposed 4th–order leap–frog topology suitable for the design of a reconnection–less reconfigurable low–pass integer–order and fractional–order filter

The denominator of the proposed filter, which corresponds with the graph in Fig. 5.60, is calculated as:

$$D(\boldsymbol{s}) = 1 - (L_1 + L_2 + L_3 + L_4) + L_1L_4 + L_2L_4 + L_1L_3\,, \tag{5.55}$$

then:

$$\begin{aligned} D(\boldsymbol{s}) &= 1 - \left(-\frac{g_{m1}}{\boldsymbol{s}C_1} - \frac{g_{m1}g_{m2}}{\boldsymbol{s}C1\boldsymbol{s}C2} - \frac{g_{m2}g_{m3}}{\boldsymbol{s}C_2\boldsymbol{s}C_3} - \frac{g_{m3}g_{m4}}{\boldsymbol{s}C_3\boldsymbol{s}C_4} \right) + \\ &+ \left[-\frac{g_{m1}}{\boldsymbol{s}C_1} \cdot \left(-\frac{g_{m3}g_{m4}}{\boldsymbol{s}C_3\boldsymbol{s}C_4} \right) \right] + \left[-\frac{g_{m1}g_{m2}}{\boldsymbol{s}C_1\boldsymbol{s}C_2} \cdot \left(-\frac{g_{m3}g_{m4}}{\boldsymbol{s}C_3\boldsymbol{s}C_4} \right) \right] + \\ &+ \left[-\frac{g_{m1}}{\boldsymbol{s}C_1} \cdot \left(-\frac{g_{m2}g_{m3}}{\boldsymbol{s}C_2\boldsymbol{s}C_3} \right) \right] = \boldsymbol{s}^4C_1C_2C_3C_4 + \boldsymbol{s}^3C_2C_3C_4g_{m1} + \boldsymbol{s}^2C_3C_4g_{m1}g_{m2} + \\ &+ \boldsymbol{s}^2C_1C_4g_{m2}g_{m3} + \boldsymbol{s}^2C_1C_2g_{m3}g_{m4} + \boldsymbol{s}C_2g_{m1}g_{m3}g_{m4} + \boldsymbol{s}C_4g_{m1}g_{m2}g_{m3} + \\ &+ g_{m1}g_{m2}g_{m3}g_{m4} \end{aligned} \tag{5.56}$$

The numerator of the transfer function is given as:

$$N(\boldsymbol{s}) = \boldsymbol{s}^3 C_1 C_2 C_3 g_{m4} B_4 + \boldsymbol{s}^2 C_1 C_2 g_{m3} g_{m4} B_3 + \boldsymbol{s}^2 C_2 C_3 g_{m1} g_{m4} B_4 + \\ + \boldsymbol{s} C_3 g_{m1} g_{m2} g_{m4} B_4 + \boldsymbol{s} C_2 g_{m1} g_{m3} g_{m4} B_3 + \boldsymbol{s} C_1 g_{m2} g_{m3} g_{m4} B_4 + \\ + \boldsymbol{s} C_1 g_{m2} g_{m3} g_{m4} B_2 + g_{m1} g_{m2} g_{m3} g_{m4} B_4 + g_{m1} g_{m2} g_{m3} g_{m4} B_2 + \\ + g_{m1} g_{m2} g_{m3} g_{m4} B_1 + g_{m1} g_{m2} g_{m3} g_{m4} B_3 \quad . \tag{5.57}$$

The resulting output response of the filter is controlled by the current gains B_1 to B_4 and depends on their adjustment. The 4th–order LP function requires current gain B_1 set to 1 and remaining gains equal to zero, for example. Based on this fact, the numerator turns into $g_{m1}g_{m2}g_{m3}g_{m4}B_1$, other terms of the numerator are canceled. In case of the 1st–order function, current gain B_4 is set to 1 and other gains are zero thus, the numerator takes form of $\boldsymbol{s}^3 C_1 C_2 C_3 g_{m4} B_4 + \boldsymbol{s}^2 C_2 C_3 g_{m1} g_{m4} B_4 + \boldsymbol{s}(C_3 g_{m1} g_{m2} g_{m4} B_4 + C_1 g_{m2} g_{m3} g_{m4} B_4) + g_{m1} g_{m2} g_{m3} g_{m4} B_4$. Similar situation occurs for the 2nd and 3rd–order function, where the current gain B_2 or B_3 is set and the remaining gains are zero, the numerator will change accordingly. As evident, the current gains B are either set to 1 or 0 in order to obtain a specific transfer function. It is also possible (depending on particular implementation of adjustable current amplifiers) to set specific value of gain (the pass band of the transfer function will not have the unity gain). This feature can be beneficial in case of the fine adjustment of the pass–band area of available LP functions (inaccuracy of filter parameters in real case or if the function does not have its pass band at 0 dB, for example). The stop–band area can be also intentionally influenced by partial addition of another term ($0 < B < 1$) to the resulting transfer function. The resulting functions, based on the setting of current gains B in ideal case, are stated in Tab. XXIII.

TABLE XXIII. CURRENT GAIN CONFIGURATION IN REGARD TO THE RESULTING INTEGER–ORDER TRANSFER FUNCTION

function	B_1 [–]	B_2 [–]	B_3 [–]	B_4 [–]
4th–order LP	1	0	0	0
3rd–order LP	0	1	0	0
2nd–order LP	0	0	1	0
1st–order LP	0	0	0	1

The graph in Fig. 5.60 can be turned into a circuit scheme (see Fig. 5.61) considering active elements (OTAs and IOGC–CA) suitable for the required function fulfillment.

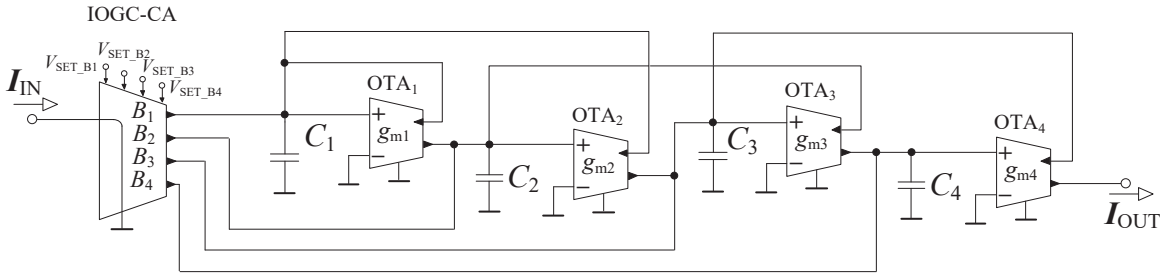


Fig. 5.61: Proposed reconnection–less reconfigurable filtering structure based on a 4th–order leap–frog topology used for the design of a reconnection–less reconfigurable low–pass integer–order and fractional–order filter

The proposed topology consists of four OTA elements (implemented as in Fig. 3.3) and one IOGC–CA. The IOGC–CA itself disposes by two non–inverting and two inverting outputs. The outputs of the IOGC–CA must have the same polarity (current orientation) for non–inverting transfer responses of the filter. The modified implementation of IOGC-CA employs UCC [121] and EL2082 devices [130] (just like in Fig. 6.3 a)), but additionally there are two supporting OPA860 devices [144] connected in series with EL2082 outputs (paths from Z+ outputs of the UCC, i.e., B_1 and B_3). OPA860 devices invert polarity of these outputs so transfer functions of the filter have the same polarity in all cases. The power consumption of this filter is 867.2 mW.

Design verification of the proposed integer–order filter

The verification of the proposed filter is supported by PSpice simulations together with experimental measurements. The numerical design (calculation of individual coefficients of the transfer function in regard to the filter order and used approximation) has been made with by the NAF software. Used coefficients, stated in (5.58), are obtained for the following specification of LP tolerance field: Butterworth approximation, the operational angular frequency ω_0 = 300,000 rad/s (f_0 = 47 kHz), transfer in pass–band K_P = -3 dB, the stop–band frequency f_s = 470 kHz, transfer in stop–band K_S = -80 dB.

$$\begin{aligned} b_4 &= 1 \\ b_3 &= 7.8440 \cdot 10^5 \\ b_2 &= 3.0764 \cdot 10^{11} \\ b_1 &= 7.0680 \cdot 10^{16} \\ b_0 &= 8.1193 \cdot 10^{21} \end{aligned} \tag{5.58}$$

These coefficients have been applied onto the denominator (expressed in (5.56)) of the transfer function. The transconductances g_{m1} to g_{m4} can be calculated as:

$$g_{m1} = b_3 C_1, \tag{5.59}$$

$$g_{m2} = \frac{b_2 C_1 C_2 C_3 C_4 - C_1 C_2 g_{m3} g_{m4}}{C_1 C_4 g_{m3} + C_3 C_4 g_{m1}}, \tag{5.60}$$

$$g_{m3} = -\frac{C_1 C_3 C_4 b_1 g_{m1}}{C_1^2 C_4 b_1 - C_1 C_4 b_2 g_{m1} - g_{m1}^{\ 2} g_{m4}}, \tag{5.61}$$

$$g_{m4} = \frac{C_1 C_4 b_0 (C_1 b_1 - b_2 g_{m1})}{C_1^2 b_1^2 - C_1 b_1 b_2 g_{m1} + b_0 g_{m1}^{\ 2}}. \tag{5.62}$$

Selected values of capacitors (C_1 = C_2 = C_3 = C_4 = 1 nF) result in values of the transconductances (in accordance with coefficients in (5.58)) as: g_{m1} = 784.4 µS, g_{m2} = 277.3 µS, g_{m3} = 190.3 µS and g_{m4} = 196.1 µS.

The list of available transfer functions for the filter from Fig. 5.61 is given in Tab. XXIV. The setting is now stated for control voltages in comparison to Tab. XXIII, where V_{SET_B} = 1 V corresponds to current gain B equal to 1, V_{SET_B} = 0 V is B = 0.

TABLE XXIV. CONTROL VOLTAGE CONFIGURATION IN REGARD TO THE RESULTING INTEGER–ORDER TRANSFER FUNCTION

function	V_{SET_B1} [V]	V_{SET_B2} [V]	V_{SET_B3} [V]	V_{SET_B4} [V]
4th–order LP	1	0	0	0
3rd–order LP	0	1	0	0
2nd–order LP	0	0	1	0
1st–order LP	0	0	0	1

The theoretical (indicated by black dashed lines) and simulation (represented by colored lines) results of the proposed integer–order filter are compared in Fig. 5.62. Magnitude characteristics of the first, second, third and fourth LP function are depicted in Fig. 5.62 a) while their phase characteristics are given in Fig. 5.62 b). Obtained simulation (black dashed lines) and experimental (colored lines) results of the same circuit are shown in Fig. 5.63. The transfer functions are based on the setting of current gains B_1 to B_4 as listed in Tab. XXIII or Tab. XXIV and presented results confirm the intended reconnection–less reconfiguration of the transfer function.

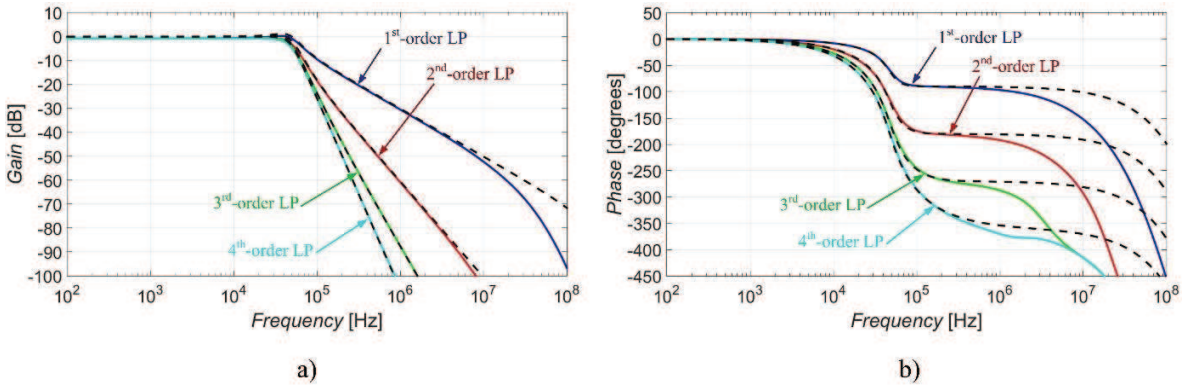


Fig. 5.62: Theoretical and simulation results of the proposed integer–order filter: a) magnitude characteristics, b) phase characteristics

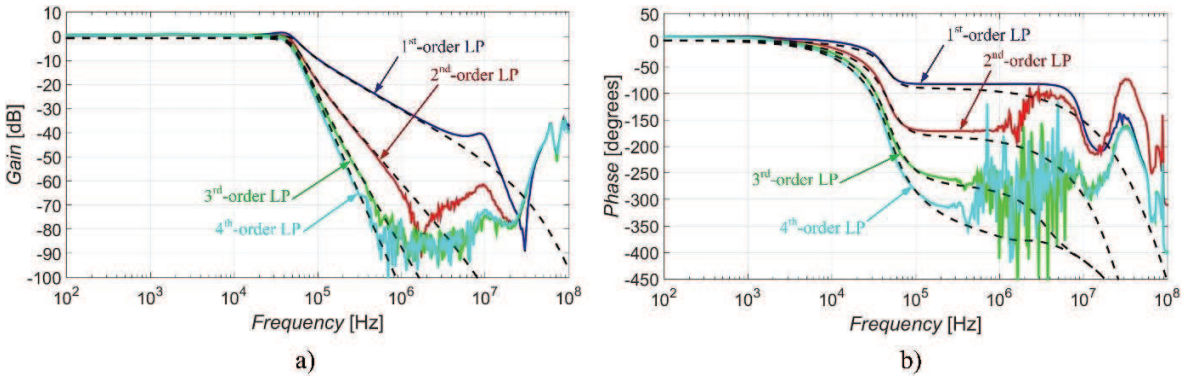


Fig. 5.63: Simulation and experimental results of the proposed integer–order filter: a) magnitude characteristics, b) phase characteristics

Design modification into a fractional–order filter

The filtering structure in Fig. 5.61 can be considered as two second–order filtering sections connected in a cascade which are then considered as integer–order (2^{nd}–order) or fractional–order (either $1 + \alpha$ or $\alpha + \beta$) depending on a specific function. This fact respects that FO filters can be stable only when the overall order of the filter is less than 2 as stated in [61]. The integer–order capacitors in the filtering structure are progressively replaced by their FO counterparts implemented by RC ladder networks (passive approximants). This progressive replacement creates transfer functions of LP $3 + \alpha$, LP $2 + \alpha$, LP $1 + \alpha$, LP $2 + \alpha + \beta$, LP $1 + \alpha + \beta$, LP $\alpha + \beta$, LP $1 + \alpha + \beta + \gamma$, LP $\alpha + \beta + \gamma$ and LP $\alpha + \beta + \gamma + \delta$. The presence of several FO orders provides an additional degree of freedom since the electronic reconnection-less reconfigurability performs more possible combinations (better chance for the fulfilment of requirements on the specific slope of the transition between the pass–band and stop–band area or specific phase shift than in integer-order case). The FOE elements are approximated by the 5^{th}–order RC structures of the Foster I type [88] (Fig. 5.38). Four printed circuit boards have been constructed for FOE used to replace integer–order capacitors in the proposed filter. Each board includes five RC structures of orders 0.3, 0.4, 0.5, 0.6 and 0.7.

The values of the components of these RC approximants are calculated using the Oustaloup approximation (in a Matlab script) [96]. All these values (calculated for the central frequency of FOEs f_C = 50 kHz) are stated in Tab. XXV. However, electronically reconfigurable order value is not still available when passive RC approximants of FO elements are used. Nevertheless, used RC structures could be replaced by an electronically adjustable emulator of FO element introduced in [77] or some other FO emulators [76], [78], [79] in order to ensure the electronic adjustment of the order. This fact will be shown later.

TABLE XXV. SPECIFICATION OF THE PART VALUES OF THE RC STRUCTURES

α [–]	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**
R_0 [Ω]	149.4	57.0	50.6	29.5	17.2
R_1 [Ω]	118.7	96.3	71.6	49.3	31.1
R_2 [Ω]	241.3	246.1	229.5	197.8	155.9
R_3 [Ω]	465.5	590.6	685.1	734.7	720.4
R_4 [Ω]	902.6	1431.1	2077.6	2793.9	3444.0
R_5 [Ω]	1960.1	4140.7	8208.3	15643.7	29039.1
C_1 [nF]	0.55	0.75	1.1	1.8	3.2
C_2 [nF]	2.3	2.6	3.1	4.0	5.6
C_3 [nF]	10.6	9.3	8.9	9.3	10.5
C_4 [nF]	47.5	33.4	25.6	21.2	19.2
C_5 [nF]	190.4	100.4	56.4	33.0	19.8

Since the values (Table XXV) for the RC structure are nonstandard in fabrication series, they are generated by a parallel combination of E24 resistors (with tolerance of 1%) and a parallel combination of E12 capacitors (with tolerance of 5–20%).

The denominator of one section of the filter (divided to two parts as discussed above) is expressed by (5.63) where only one integer–order capacitor is replaced by a FO capacitor. The equation (5.64) is valid for both capacitors replaced by their FO counterparts. These denominators have forms:

$$D(s) \cong s^{1+\alpha} + s^{\alpha}\frac{g_{m1}}{C_1} + \frac{g_{m1}g_{m2}}{C_1 C_{2\alpha}}, \tag{5.63}$$

$$D(s) \cong s^{\alpha+\beta} + s^{\beta}\frac{g_{m1}}{C_{1\alpha}} + \frac{g_{m1}g_{m2}}{C_{1\alpha}C_{2\beta}}. \tag{5.64}$$

Design verification of the proposed fractional–order filter

Figures 5.64–5.69 show the results (magnitude and phase characteristics) of the proposed filter when capacitor C_4 is replaced by one of the implemented RC FOE approximants. The denominator of the filter (after this modification) is expressed as:

$$D(\boldsymbol{s}) = \boldsymbol{s}^{3+\alpha}C_1C_2C_3C_{4\alpha} + \boldsymbol{s}^{2+\alpha}C_2C_3C_{4\alpha}g_{m1} + \boldsymbol{s}^{1+\alpha}C_3C_{4\alpha}g_{m1}g_{m2} + \\ + \boldsymbol{s}^{1+\alpha}C_1C_{4\alpha}g_{m2}g_{m3} + \boldsymbol{s}^{2}C_1C_2g_{m3}g_{m4} + \boldsymbol{s}^{1}C_2g_{m1}g_{m3}g_{m4} + \\ + \boldsymbol{s}^{\alpha}C_{4\alpha}g_{m1}g_{m2}g_{m3} + g_{m1}g_{m2}g_{m3}g_{m4} \quad . \tag{5.65}$$

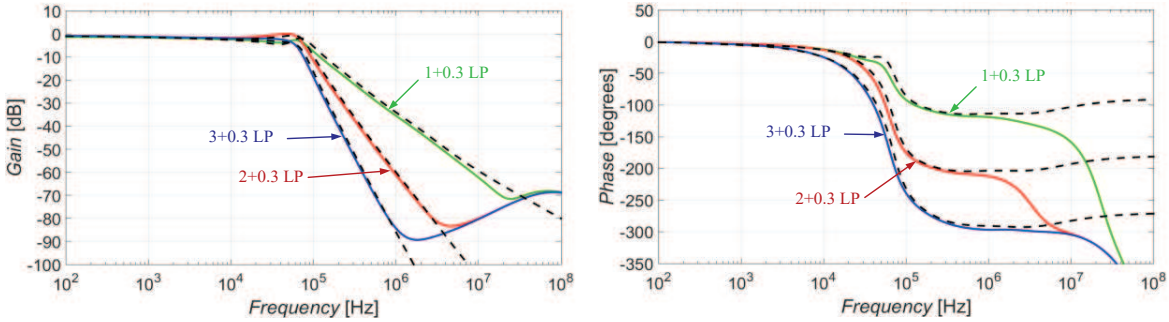
Such modification offers FO low–pass transfer functions of $3 + \alpha$, $2 + \alpha$ and $1 + \alpha$ in correlation with the setting of current gains. The first section of the filter in Fig. 5.61 (involving OTA_1, OTA_2 and capacitors C_1 and C_2) is expressed as a standard 2nd–order filter with its f_0 = 50 kHz according to the relation:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad . \tag{5.66}$$

The design at f_0 = 50 kHz and selected values of capacitors $C_1 = C_2$ = 4.7 nF yield the values of transconductances g_{m1} and g_{m2} calculated as $g_{m1} = g_{m2}$ = 1.477 mS. The second section is using C_3 = 4.7 nF and the values of transconductances g_{m3} and g_{m4} (stated in Tab. XXVI) are calculated in relation to the value of the FO capacitor which is depending on FO parameter α. Figures present the comparison of the theoretical and simulated results and then simulation and experimental results of functions of $3 + \alpha$, $2 + \alpha$ and $1 + \alpha$ when α is equal to 0.3 in case of Figs. 5.64 and 5.65, it is α = 0.5 for Figs. 5.66 and 5.67 and α = 0.7 for Figs. 5.68 and 5.69. The resulting orders are usually slightly lower than the expected values (about 0.1 less than expected). Several reasons are responsible for these differences from the theory. The rounding of calculated values takes part on these errors. A substantial mismatch results also from the parallel combination of resistors/capacitors that do not exactly match the desired values due to the fabrication tolerance of used passive elements. Note that this inaccuracy will be added to each other as more integer–order capacitors are replaced by the implemented RC structures. Other possible solution is the implementation of the RC structure with more stages resulting in improved accuracy.

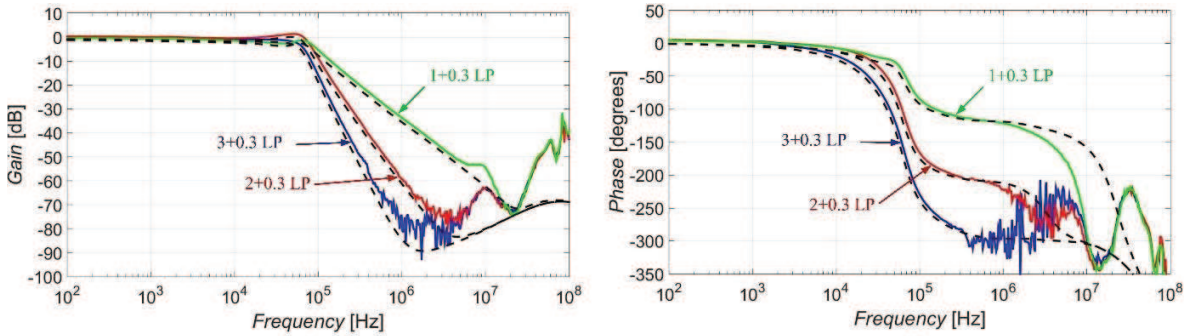
TABLE XXVI. VALUES OF TRANSCONDUCTANCES GM3 GM4 IN RELATION TO THE VALUES OF ALPHA

α [–]	0.3	0.4	0.5	0.6	0.7
g_{m3} [mS]	0.61	0.76	0.93	1.14	1.38
g_{m4} [mS]	3.06	2.53	2.10	1.76	1.50



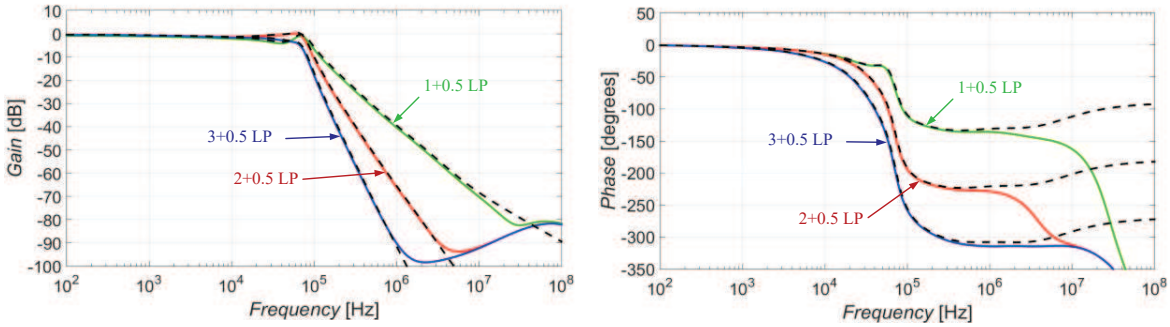
a) b)

Fig. 5.64: Theoretical and simulation results of 3 + α, 2 + α and 1 + α orders for α = 0.3: a) magnitude characteristics, b) phase characteristics



a) b)

Fig. 5.65: Simulation and experimental results of 3 + α, 2 + α and 1 + α orders for α = 0.3: a) magnitude characteristics, b) phase characteristics



a) b)

Fig. 5.66: Theoretical and simulation results of 3 + α, 2 + α and 1 + α orders for α = 0.5: a) magnitude characteristics, b) phase characteristics

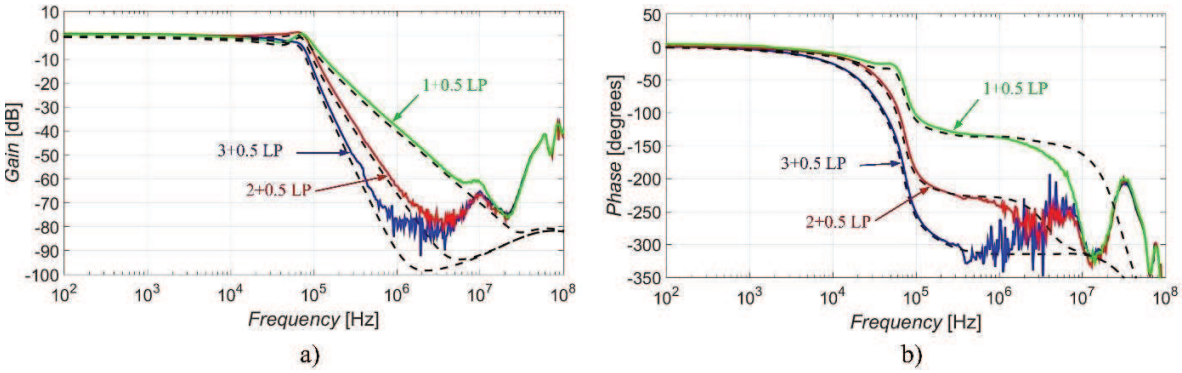


Fig. 5.67: Simulation and experimental results of 3 + α, 2 + α and 1 + α orders for α = 0.5: a) magnitude characteristics, b) phase characteristics

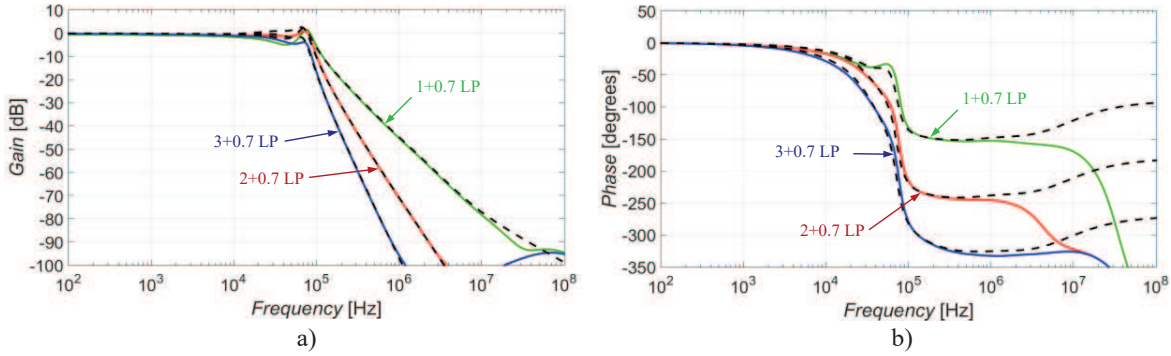


Fig. 5.68: Theoretical and simulation results of 3 + α, 2 + α and 1 + α orders for α = 0.7: a) magnitude characteristics, b) phase characteristics

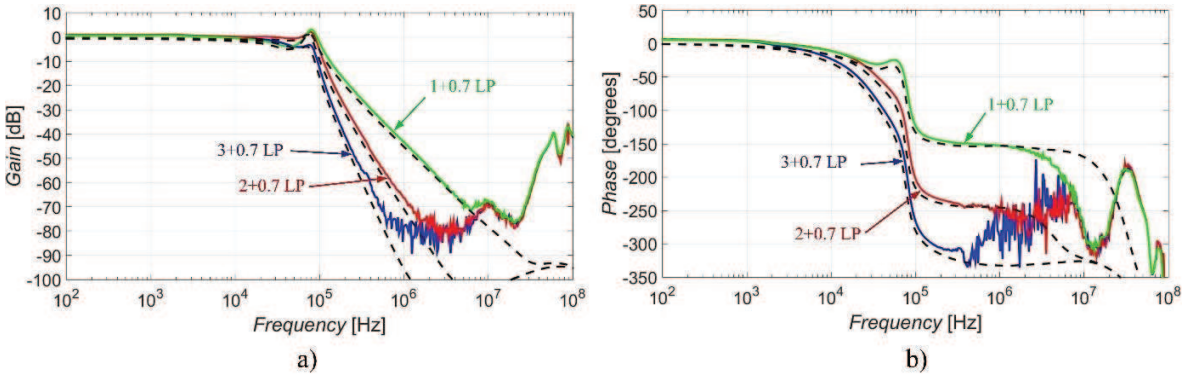


Fig. 5.69: Simulation and experimental results of 3 + α, 2 + α and 1 + α orders for α = 0.7: a) magnitude characteristics, b) phase characteristics

The proposed filter creates FO low–pass functions of 2 + α + β, 1 + α + β and α + β by replacing two capacitors (C_3 and C_4) in the topology by FO capacitors. The denominator for this case is given as:

$$D(s) = s^{2+\alpha+\beta}C_1C_2C_{3\alpha}C_{4\beta} + s^{1+\alpha+\beta}C_2C_{3\alpha}C_{4\beta}g_{m1} + \\ + s^{\alpha+\beta}C_{3\alpha}C_{4\beta}g_{m1}g_{m2} + s^{1+\beta}C_1C_{4\beta}g_{m2}g_{m3} + s^2C_1C_2g_{m3}g_{m4} + \\ + s^1C_2g_{m1}g_{m3}g_{m4} + s^\beta C_{4\beta}g_{m1}g_{m2}g_{m3} + g_{m1}g_{m2}g_{m3}g_{m4} \quad (5.67)$$

The first section of the filter is identical to the previous case (C_1 = C_2 = 4.7 nF, $g_{m1} = g_{m2}$ = 1.477 mS). The second section is now involving two FO capacitors. Used values of g_{m3} and g_{m4} are summarized in Tab. XXVII. The value of g_{m3} is depending on parameter α but its change is insignificant (going from 1.45 mS to 1.46 mS when α changes from 0.3 to 0.7). Therefore, the transconductance g_{m3} has been set to 1.46 mS for all used α. The transconductance g_{m4} depends on the value of β. Figure 5.70 introduces the results of $2 + \alpha + \beta$ function for four different combinations of α and β values. The following setting has been used: $\alpha = 0.3$, $\beta = 0.4$, $\alpha = 0.5$, $\beta = 0.4$, $\alpha = 0.5$, $\beta = 0.6$ and $\alpha = 0.5$, $\beta = 0.7$ resulting in orders 2.7, 2.9, 3.1 and 3.3. The characteristics of $1 + \alpha + \beta$ functions are provided in Fig. 5.71. The α and β value combination for this case is $\alpha = 0.4$, $\beta = 0.3$, $\alpha = 0.6$, $\beta = 0.3$, $\alpha = 0.4$, $\beta = 0.7$ and $\alpha = 0.7$, $\beta = 0.6$ (orders 1.7, 1.9, 2.1 and 2.3).

TABLE XXVII. VALUES OF TRANSCONDUCTANCES GM3 GM4 IN RELATION TO THE VALUES OF ALPHA AND BETA

α [–]	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**
g_{m3} [mS]	1.46				
β [–]	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**
g_{m4} [mS]	3.47	2.57	2.03	1.67	1.41

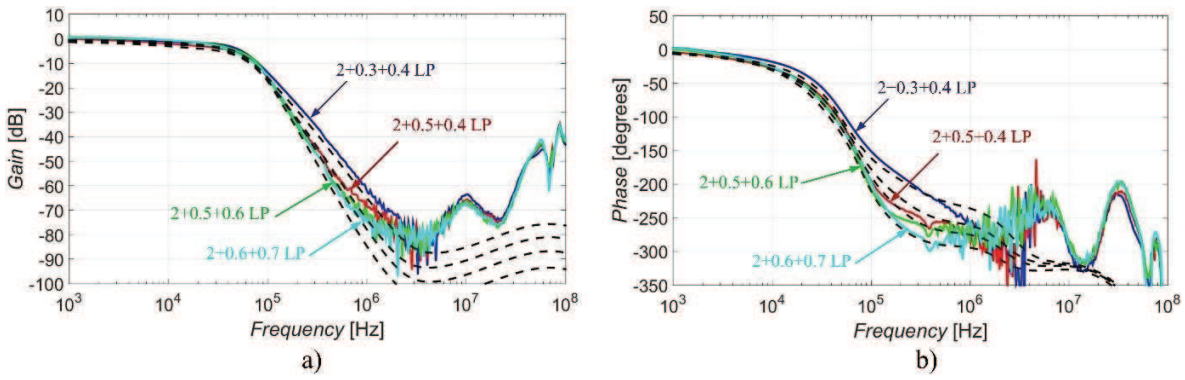


Fig. 5.70: Simulation and experimental results of $2 + \alpha + \beta$, functions for various combinations: a) magnitude characteristics, b) phase characteristics

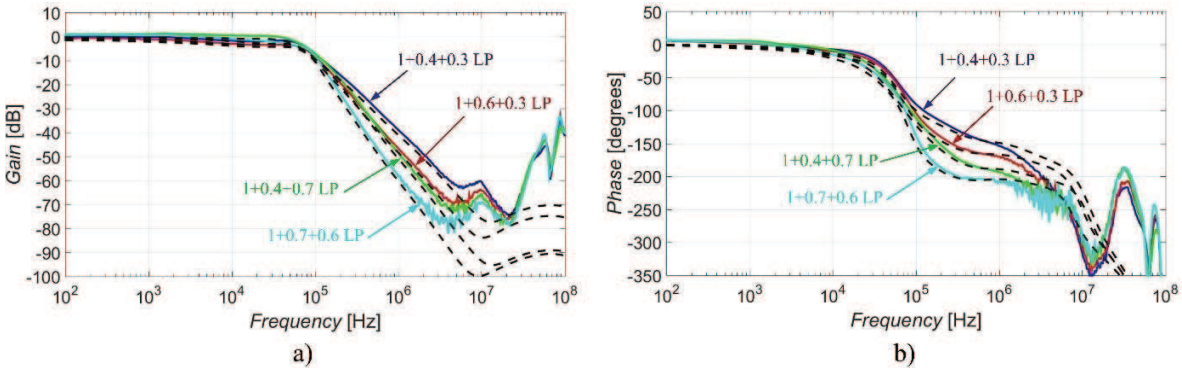


Fig. 5.71: Simulation and experimental results of 1 + α + β, functions for various combinations: a) magnitude characteristics, b) phase characteristics

Fractional–order low–pass functions of 1 + α + β + γ and α + β + γ are available if three capacitors (C_2, C_3, C_4) are replaced by the designed RC approximants of FOE. The denominator takes form of:

$$D(s) = s^{1+\alpha+\beta+\gamma}C_1C_{2\alpha}C_{3\beta}C_{4\gamma} + s^{\alpha+\beta+\gamma}C_{2\alpha}C_{3\beta}C_{4\gamma}g_{m1} + \\ + s^{\beta+\gamma}C_{3\beta}C_{4\gamma}g_{m1}g_{m2} + s^{1+\gamma}C_1C_{4\gamma}g_{m2}g_{m3} + s^{1+\alpha}C_1C_{2\alpha}g_{m3}g_{m4} + \\ s^{\alpha}C_{2\alpha}g_{m1}g_{m3}g_{m4} + s^{\gamma}C_{4\gamma}g_{m1}g_{m2}g_{m3} + g_{m1}g_{m2}g_{m3}g_{m4} \quad (5.68)$$

The first section of the filter is solved as a 1 + α filter (the same way as the second section in case of 3 + α, 2 + α and 1 + α functions). The values of transconductances g_{m1} and g_{m2} are identical with values of g_{m3} and g_{m4} in Tab. XXVI. The second section is identical to the previous case (g_{m3} and g_{m4} are set according to Tab. XXVII). The results of the 1 + α + β + γ transfer functions are shown in Fig. 5.72 for combinations α = 0.3, b = 0.3, γ = 0.3, α = 0.5, β = 0.4, γ = 0.4, α = 0.5, β = 0.6, γ = 0.6 and α = 0.7, β = 0.7, γ = 0.7 (resulting overall orders of the filter 1.9, 2.3, 2.7 and 3.1). Figure 5.73 introduces results of α + β + γ function for α = 0.5, β = 0.3, γ = 0.3, α = 0.3, β = 0.5, γ = 0.7 and α = 0.6, β = 0.6, γ = 0.7.

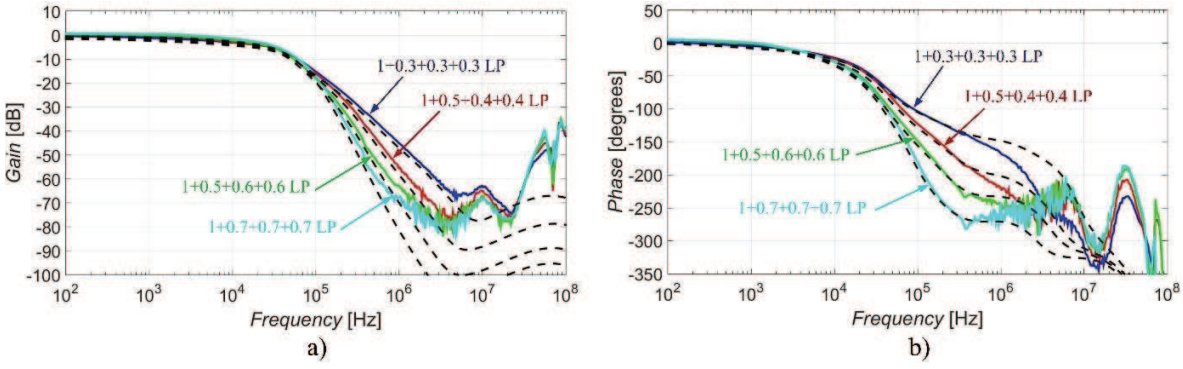


Fig. 5.72: Simulation and experimental results of 1 + α + β + γ, functions for various combinations: a) magnitude characteristics, b) phase characteristics

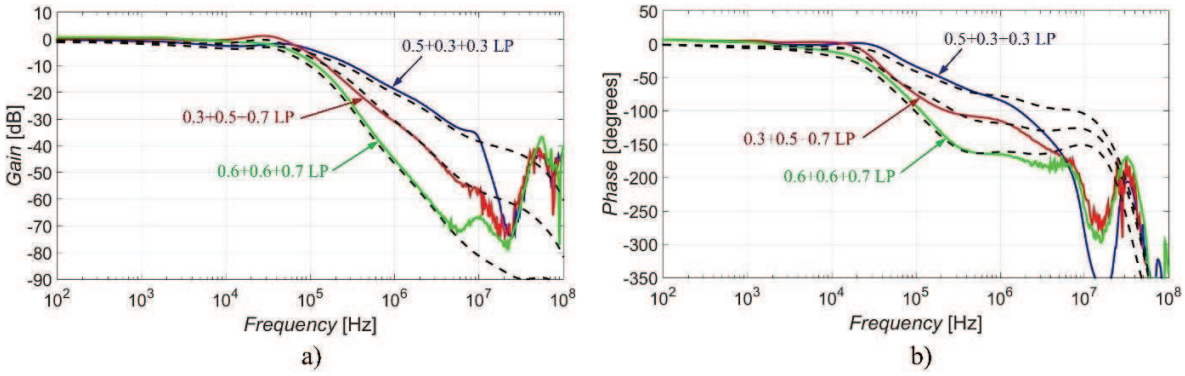


Fig. 5.73: Simulation and experimental results of $\alpha + \beta + \gamma$, functions for various combinations: a) magnitude characteristics, b) phase characteristics

The last configuration (all four FO capacitors) employs both sections of the filter set in accordance with Tab. XXVII depending on the values of FO orders. The denominator is:

$$D(s) = s^{\alpha+\beta+\gamma+\delta}C_{1\alpha}C_{2\beta}C_{3\gamma}C_{4\delta} + s^{\beta+\gamma+\delta}C_{2\beta}C_{3\gamma}C_{4\delta}g_{m1} + \\ + s^{\gamma+\delta}C_{3\gamma}C_{4\delta}g_{m1}g_{m2} + s^{\alpha+\delta}C_{1\alpha}C_{4\delta}g_{m2}g_{m3} + s^{\alpha+\beta}C_{1\alpha}C_{2\beta}g_{m3}g_{m4} + \\ s^{\beta}C_{2\beta}g_{m1}g_{m3}g_{m4} + s^{\delta}C_{4\delta}g_{m1}g_{m2}g_{m3} + g_{m1}g_{m2}g_{m3}g_{m4} \tag{5.69}$$

Characteristics of $\alpha + \beta + \gamma + \delta$ function (for $\alpha = 0.3$, $\beta = 0.3$, $\gamma = 0.5$, $\delta = 0.3$, $\alpha = 0.3$, $\beta = 0.6$, $\gamma = 0.5$, $\delta = 0.4$, $\alpha = 0.7$, $\beta = 0.5$, $\gamma = 0.6$, $\delta = 0.4$, $\alpha = 0.7$, $\beta = 0.7$, $\gamma = 0.6$, $\delta = 0.6$) are available in Fig. 5.74.

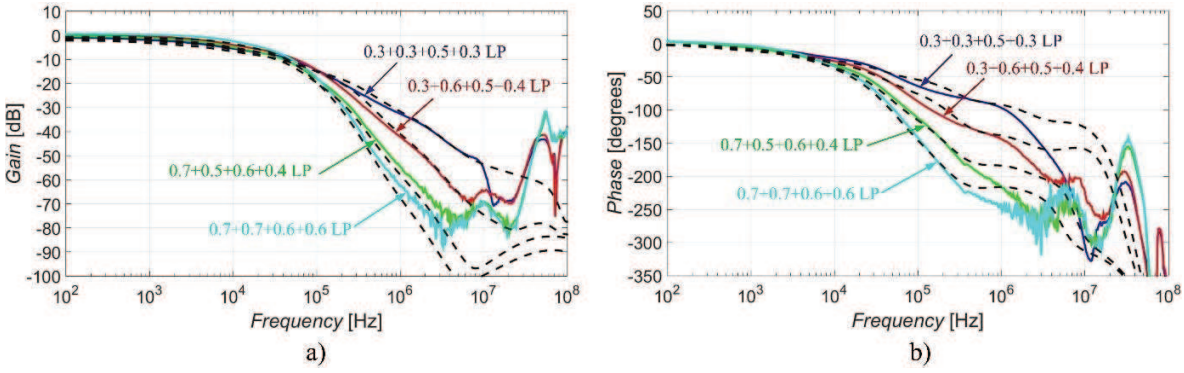


Fig. 5.74: Simulation and experimental results of $\alpha + \beta + \gamma + \delta$, functions for various combinations: a) magnitude characteristics, b) phase characteristics

Pole frequency adjustment

The beneficial feature of the designed filter includes the adjustment of the pole frequency which can be adjusted by the change of transconductances g_{m1} to g_{m4} when ratio between transconductances given by the FO approximation remains unchanged (approximate ratio 1:0.35:0.24:0.25). This feature has been tested for three different pole frequencies (25 kHz,

50 kHz and 100 kHz) in case of $\alpha + \beta + \gamma$ function where $\alpha = \beta = \gamma = 0.5$ (Fig. 5.75). The values of transconductances are specified in Tab. XXVIII. The possibility of the pole frequency adjustment works as expected. The limitation of the tunability range of f_0 depends on the bandwidth of validity of used FO approximation (approximately two decades for used 5th–order RC approximant (5 kHz to 500 kHz)). This range can be extended by increasing the order (i.e., number of sections of topology) of used RC approximants (increased circuit complexity is the cost for this improvement).

TABLE XXVIII. VALUES OF TRANSCONDUCTANCES USED FOR THE POLE FREQUENCY ADJUSTMENT

Theoretical f_0 [kHz]	**25**	**50**	**100**
g_{m1} [mS]	0.47	0.93	1.87
g_{m2} [mS]	1.05	2.10	4.21
g_{m3} [mS]	0.73	1.46	2.91
g_{m4} [mS]	1.01	2.03	4.06

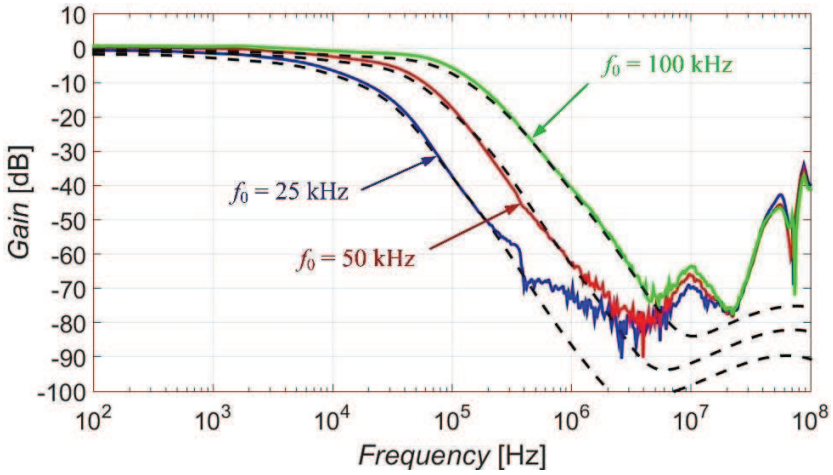


Fig. 5.75: Demonstration of the f_0 adjustability for three different settings for $\alpha + \beta + \gamma$ function where $\alpha = \beta = \gamma = 0.5$

Stability analysis of FO solutions

The analysis of the stability of analog circuits, and frequency filters especially, is an important part of the design. A general approach to stability analysis of fractional–order circuits requires the transformation of the s–plane into a general plane that includes the fractional orders so–called W–plane, as was introduced in [147]. W–plane is defined as $s^{1/m}$, where m is a positive integer value [147]. The unstable and stable regions of the s–plane are transformed into $|\theta_W| < \pi/2m$ and into $\pi/2m < |\theta_W| < \pi/m$ as suggested in Fig. 5.76. The region where $|\theta_W| > \pi/m$ is non–physical. Thus, the system will be stable if all roots in the W–plane take positions in the region $|\theta_W| > \pi/2m$ and unstable if at least one root is in the region $|\theta_W| < \pi/2m$. In order to investigate and prove the stability of the proposed fractional–order filter, positions of poles projected into the W–plane of various situations were carried out

using a Matlab script based on the mathematical procedure introduced in [148]. Figures 5.77–5.79 depict W–planes for the 3+α filter, where Fig. 5.77 shows a situation for α = 0.3, Fig. 5.78 for α = 0.5 and Fig.5.79 for α = 0.7. W–planes in case of the 2+α+β filter are presented in Fig. 5.80, Fig. 5.81 and Fig. 5.82, respectively for situations $\alpha = \beta =$ 0.3, $\alpha = \beta =$ 0.5 and $\alpha = \beta =$ 0.7. The last three pictures (Fig. 5.83, Fig. 5.84 and Fig. 5.85) offer the W–planes of the 1+α+β+γ filter for combinations of different fractional–orders (the first combination is α = 0.3, β = 0.5, γ = 0.7, the second one is α = 0.5, β = 0.7, γ = 0.3 and the third one is α = 0.7, β = 0.5, γ = 0.3). It is evident that the filter is stable for all tested cases.

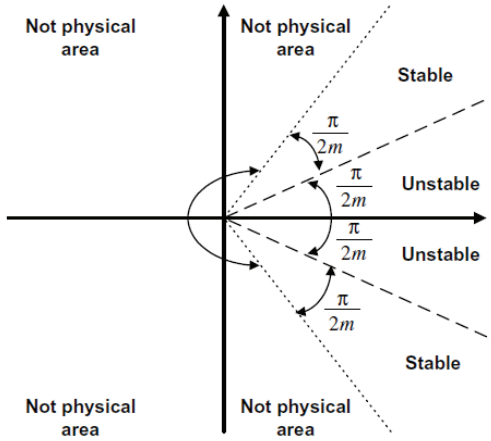


Fig. 5.76: W–plane regions (adopted from [145])

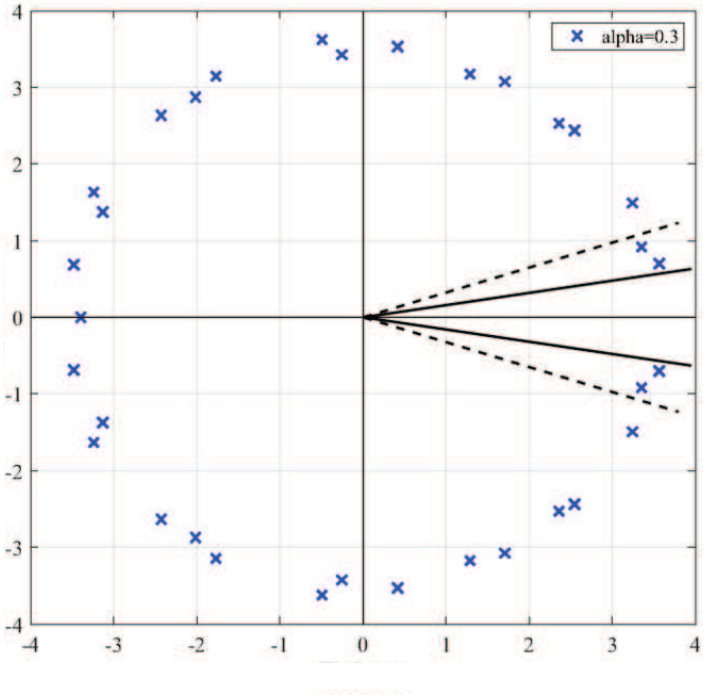


Fig. 5.77: Roots in the W–plane for 3+α filter where α = 0.3

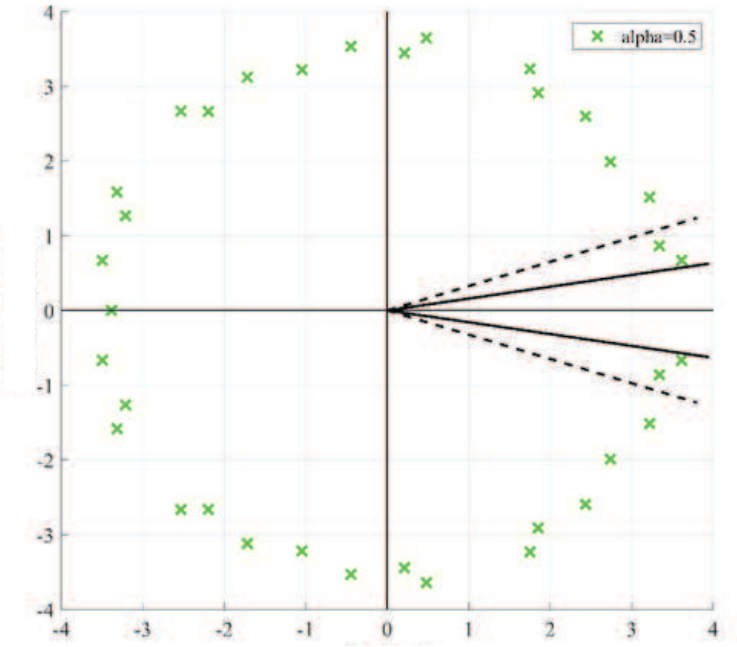


Fig. 5.78: Roots in the W–plane for 3+α filter where α = 0.5

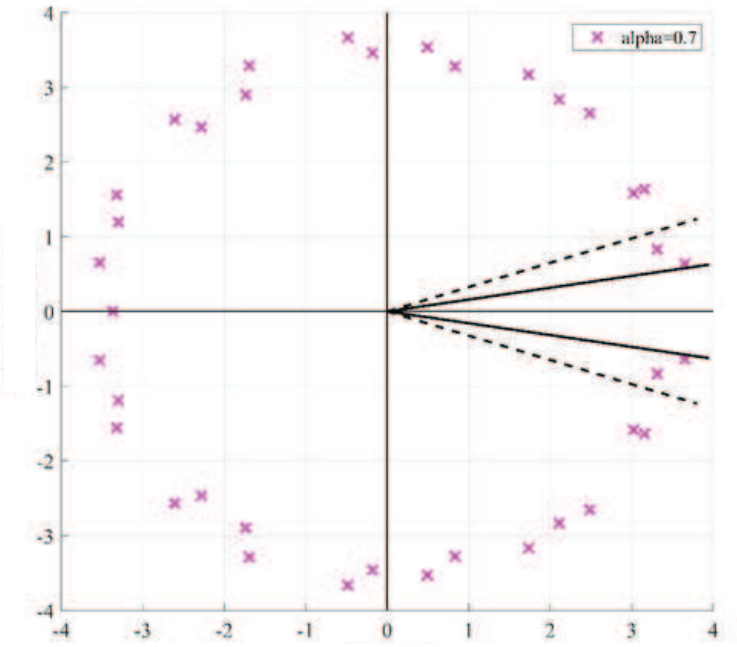


Fig. 5.79: Roots in the W–plane for 3+α filter where α = 0.7

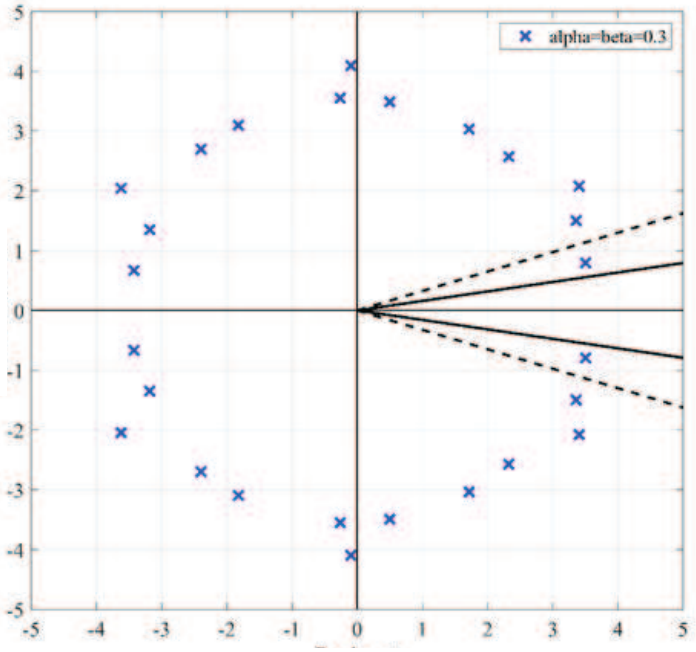


Fig. 5.80: Roots in the W–plane for 2+α+β filter where $\alpha = \beta = 0.3$

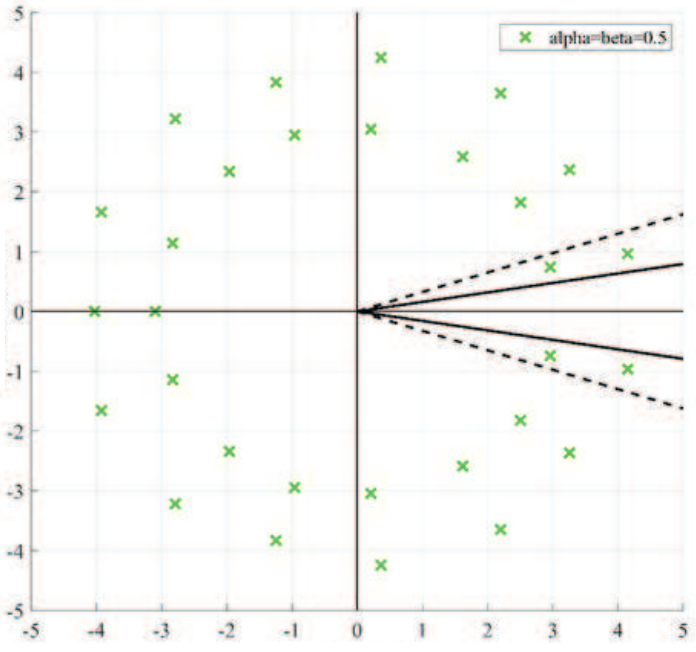


Fig. 5.81: Roots in the W–plane for 2+α+β filter where $\alpha = \beta = 0.5$

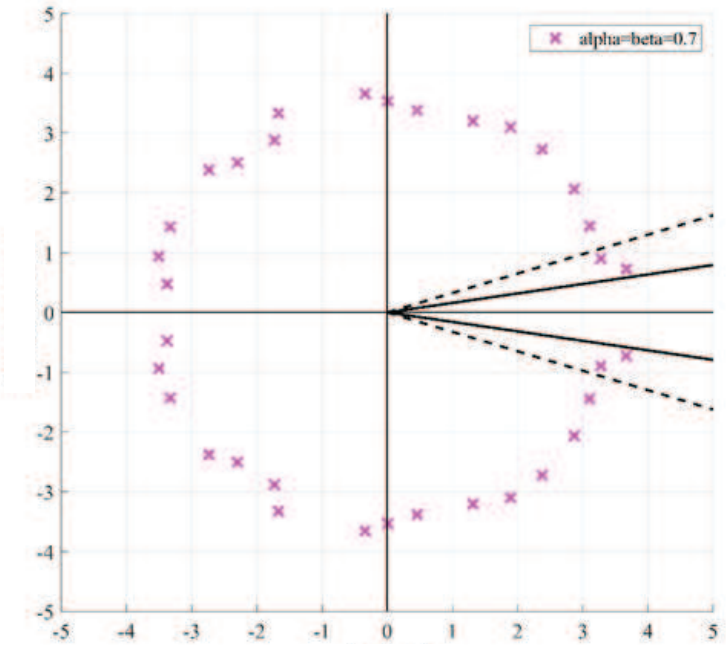


Fig. 5.82: Roots in the W–plane for 2+α+β filter where $\alpha = \beta = 0.7$

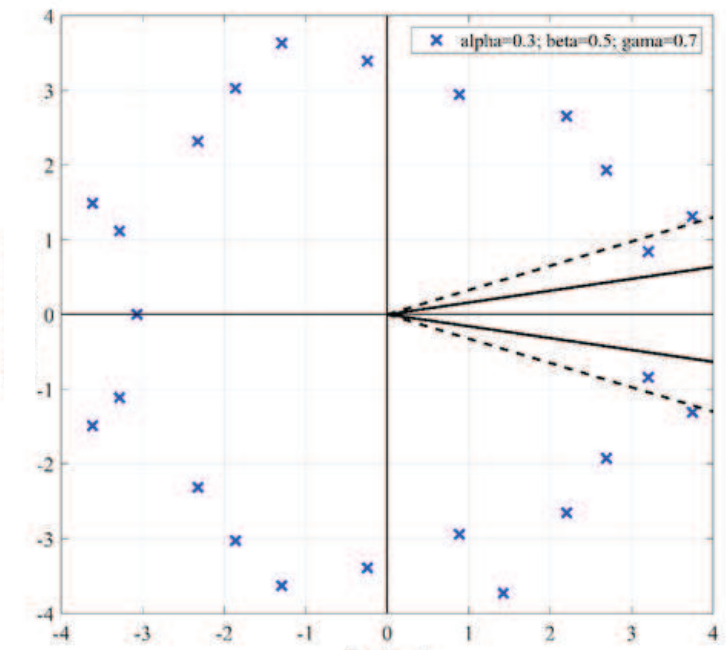


Fig. 5.83: Roots in the W–plane for 1+α+β+γ filter where $\alpha = 0.3$, $\beta = 0.5$, $\gamma = 0.7$

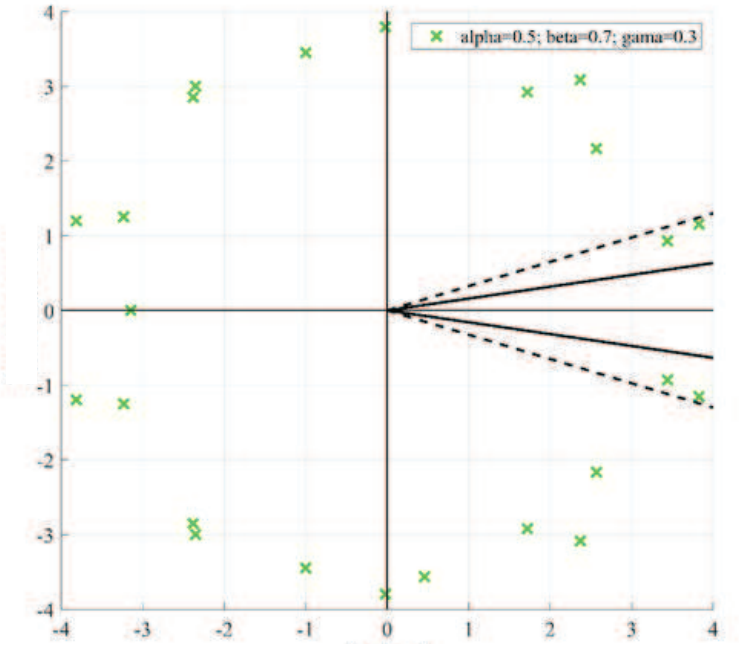


Fig. 5.84: Roots in the W–plane for $1+\alpha+\beta+\gamma$ filter where $\alpha = 0.5$, $\beta = 0.7$, $\gamma = 0.3$

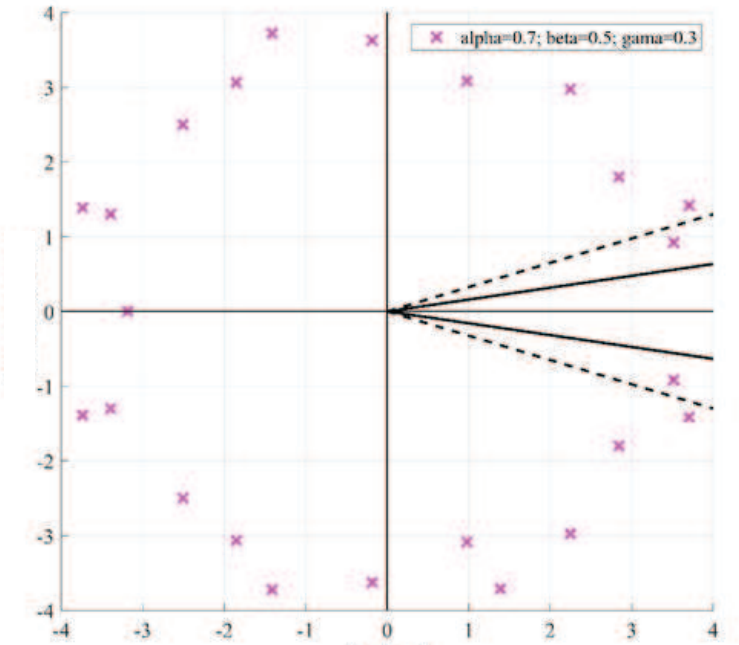


Fig. 5.85: Roots in the W–plane for $1+\alpha+\beta+\gamma$ filter where $\alpha = 0.7$, $\beta = 0.5$, $\gamma = 0.3$

Electronic adjustment of the order of the fractional-order filter

The proposed filter was implemented with RC approximants to substitute the function of fractional–order capacitors in previous parts. However, the electronically adjustable solution of FOE exists in literature. Unfortunately, their high complexity of the constructed structure limits usability, unless it is designed in complete form of on–chip implementation [85]. Then the complexity of such resulting circuitry is not so significant for the realization. In our case, the electronic adjustment of the order has been achieved by the replacement of a building block of given filter (CM integrator created by the OTA and RC ladder FOE approximant) by an electronically adjustable integrator of a fractional–order introduced in chapter 6.2 (complete design procedure is described there as one from possible ways of the design). The mentioned current–mode integrator is shown in Fig. 5.86. The topology in Fig. 5.86 is described by the equation:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{s}^2 C_1 C_2 B_1 + \boldsymbol{s} C_2 g_{m1} B_2 + g_{m1} g_{m2} B_3}{\boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m1} + g_{m1} g_{m2}} \cong \frac{1}{\tau_\alpha s^\alpha}. \tag{5.70}$$

The values of transconductances and current gains of the Follow–the–Leader–Feedback (FLF) [133] topology in Fig. 5.86, are obtained in correspondence with the desired fractional orders (0.3, 0.5 and 0.7) and calculated for the center frequency of the operational bandwidth of the integrator being 100 kHz and C_1 = 470 pF, C_2 = 4.7 nF. They are stated in Tab. XXIX.

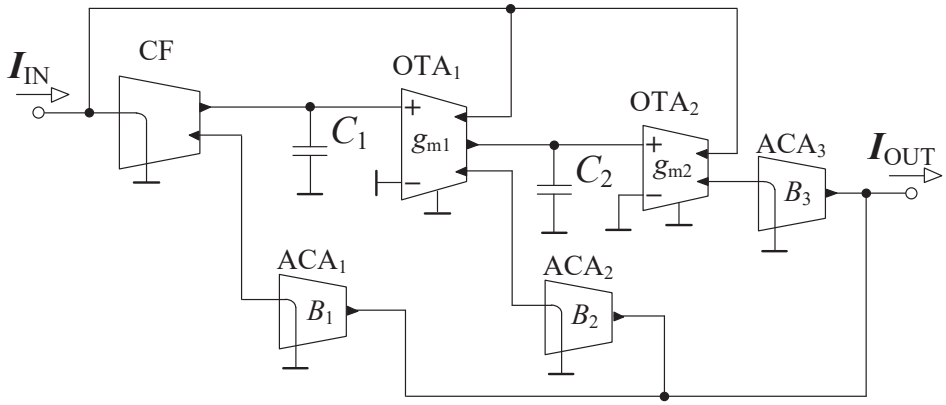
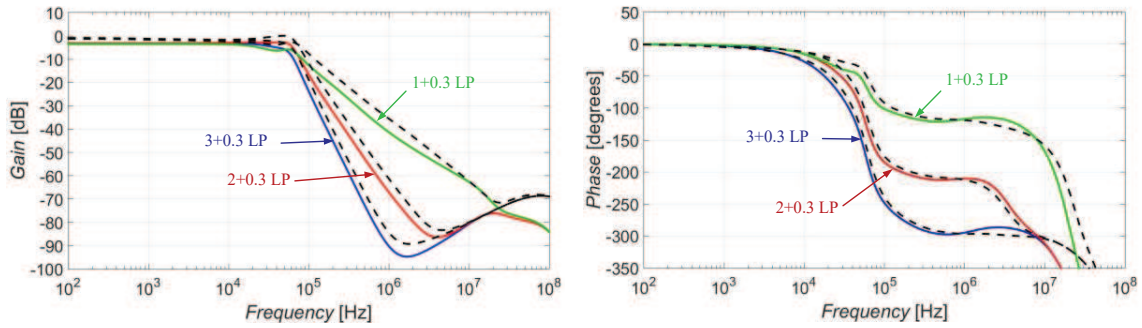


Fig. 5.86: Current–mode integrator based on FLF topology used for the approximation of a fractional–order integrator

TABLE XXIX. VALUES OF TRANSCONDUCTANCES AND CURRENT GAINS OF THE STRUCTURE FROM FIG. 5.86 FOR CHOSEN VALUES OF ALPHA

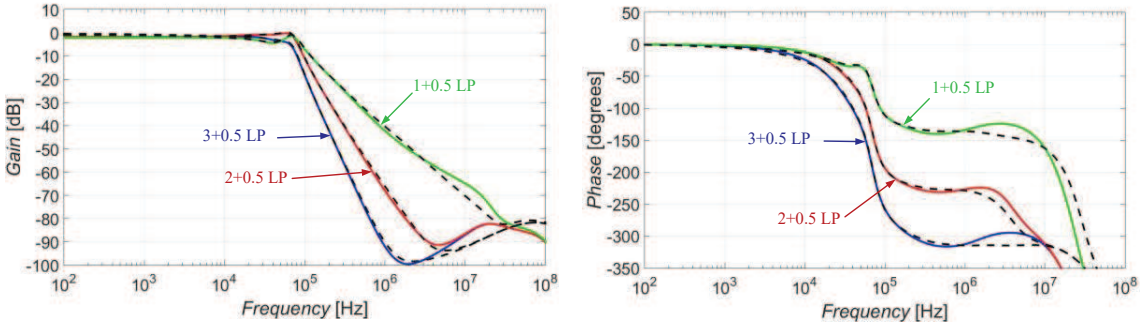
α [–]	**0.3**	**0.5**	**0.7**
g_{m1} [µS]	772.3	590.6	451.7
g_{m1} [µS]	449.4	295.3	164.1
B_1 [–]	0.4	0.2	0.09
B_2 [–]	1	1	1
B_3 [–]	2.5	5	11.8

The function of the designed fractional–order integrator (the integrator itself is analyzed in subchapter 6.2) has been tested in case of simulations for selected filtering transfer functions $3 + \alpha$, $2 + \alpha$ and $1 + \alpha$ (OTA_4 and C_4 (OTA-C integrator) in Fig. 5.61 were replaced by the integrator from Fig. 5.86) for α being equal to 0.3, 0.5 and 0.7. The achieved results are compared with results of the corresponding solutions with the RC passive approximants (subsection "Design verification of the proposed fractional–order filter" for orders of $3+\alpha$, $2+\alpha$ and $1+\alpha$ (Figs. 5.64, 5.66 and 5.68)). The values of parameters of the filter (transconductances and current gains of the filter itself (Fig. 5.61) not the circuit from Fig. 5.86) are the same as in given subsection. Figures 5.87–5.89 compare the simulation results of the filter when using the RC structure (black dashed lines) with the simulation results of the filter when using the FO integrator allowing the electronic order adjustment (colored lines). The results yield a good agreement of both approaches. It documents accuracy and sufficient validity of the employment of the electronic adjustment of the fractional order despite drawbacks of significantly increased complexity of resulting solution. There is a slight shift (systematic) in the frequency for the results with the FO integrator. Nonetheless, this undesired behavior can be easily compensated (readjustment only) as demonstrated earlier.



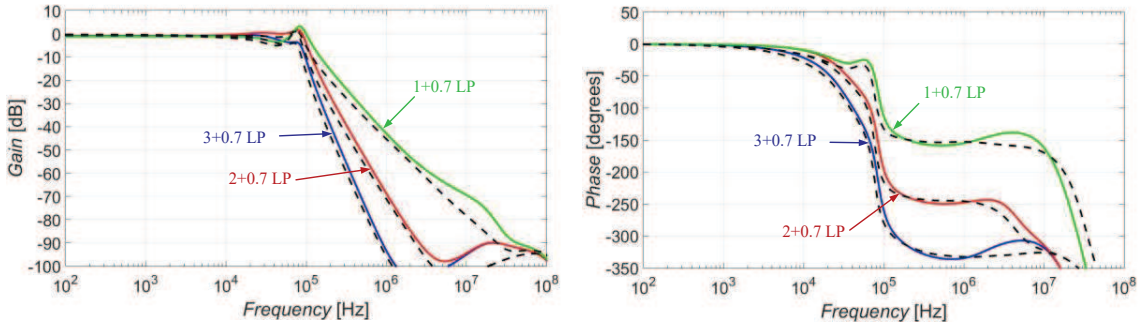
a) b)

Fig. 5.87: Simulation results of $3 + \alpha$, $2 + \alpha$ and $1 + \alpha$ orders for the solution with the RC structure and FO integrator when $\alpha = 0.3$: a) magnitude characteristics, b) phase characteristics



a) b)

Fig. 5.88: Simulation results of $3 + \alpha$, $2 + \alpha$ and $1 + \alpha$ orders for the solution with the RC structure and FO integrator when $\alpha = 0.5$: a) magnitude characteristics, b) phase characteristics



a) b)

Fig. 5.89: Simulation results of 3 + α, 2 + α and 1 + α orders for the solution with the RC structure and FO integrator when α = 0.7: a) magnitude characteristics, b) phase characteristics

The proposed structure of a FO reconnection–less reconfigurable filter offers LP functions of $3+\alpha$, $2+\alpha$, $1+\alpha$, $2+\alpha+\beta$, $1+\alpha+\beta$, $\alpha+\beta$, $1+\alpha+\beta+\gamma$, $\alpha+\beta+\gamma$ and $\alpha+\beta+\gamma+\delta$ and 4 additional functions of integer–order as well. It depends on the setting of control gains B_1 to B_4 and replacement of standard integer–order capacitors by their FO counterparts creating an additional degree of freedom when it results in adjustable values of the filter order. All FO filters were constructed by a cascade combination of a $1 + \alpha$ filter with an integer–order structure so far. The presented solution works with whole topology (4^{th}–order as maximum in this case) and the resulting order of the filter results from the selection of the setting of current gains B_1 to B_4 (and the parameters of the FO integrator(s) in case of the electronic adjustment of the fractional order).

5.6 Comparison of the proposed solutions of reconnection–less reconfigurable filters

The first subchapter (subchapter 5.1) contains structures designed by MUNV. The advantage of these structures covers easy design and usually low number of used active elements. The disadvantage, on the other hand, is the presence of a floating capacitor unless the circuit has more nodes which increases the mathematical complexity significantly. The following subchapter (subchapter 5.2) presents structures which have been created by a modification of existing MISO filtering structures by adding electronically controllable active elements in order to obtain the feature of the reconnection–less reconfiguration. A design of the IOGC–CA element (introduced in subchapter 6.1) has been specifically made for the purposes of the reconnection–less reconfiguration in the previously proposed MISO type filters. It documents and confirms an easy approach how to design reconnection–less reconfigurable filters from already existing filters without this feature. The next subchapter (subchapter 5.3) presents filters using the synthesis based on transformation of VM circuits into their CM form. As already mentioned, the CM operation has some advantages in comparison to the VM circuits in particular cases. Subchapter 5.4 introduces a proposal based on the SFG synthesis. The SFG method can be well used for the proposal of filters

working in multiple modes. The disadvantage of this approach may be found in the design of non-standard topologies (differential structures, for instance) when the expression of the transfer function is complicated (when many loops are present, typically for high order of the filter, for instance). The last subchapter of this part of the work targets at the proposal of reconnection–less reconfigurable filters of high orders (higher than 2nd). The synthesis and design of reconnection–less reconfigurable filters of high orders can generate functions of various orders, but a significant increase of number of active elements and a difficult adjustment of the pole frequency and quality factor (ratios of parameters preserved as constant) which depend on the coefficients of the transfer function are the costs for these features. There is a significant trade–off between complexity and performance. A complex comparison of proposed filters can be made from Tab. XXX.

TABLE XXX. COMPARISION OF OWN RECONNECTION–LESS RECONFIGURABLE FILTERS PROPOSED IN THIS THESIS

Chapter number	Operation mode	Type of control	Number of active/passive elements	Available functions (count)	Simulations/ Measurements	Independent adjustment of f_0	Independent adjustment of Q	All capacitors grounded	Power consumption [mW]
5.1.1	VM	g_m, A	4/2	AP, BP, DT, HP, HP(1st), HPZ (6)	Yes/No	[1]Yes	[1]Yes	No	31
5.1.2	VM	g_m, A	3/2	AP, BS, DT, HP(1st), LP, LPZ (6)	Yes/No	Yes	Yes	No	48
5.2.1	CM	g_m, B	6/4	AP, BP, BS, HP, HPZ, LP, LPZ (7)	Yes/No	Yes	Yes	Yes	13
5.2.2	CM	g_m, R_X, B	2/2	AP, BP, BS, DT, HP, HPZ, LP (7)	Yes/No	[1]Yes	[1]Yes	Yes	65
5.3.1	CM	R_X, B	5/4	AP, BP, BS, HP, HP(1st), HPZ, LP, LPZ (8)	Yes/No	[1]Yes	[1]Yes	Yes	24
5.3.2	CM	g_m, B	5/2	AP, BP, BS, DT, HP, HP(1st), HPZ, LP, LPZ (9)	Yes/No	[1]Yes	[1]Yes	No	610
5.4.1	CM VM	g_m, A, B	8/2	AP, BP, BS, HP, HPZ, LP, LPZ (16)[2]	Yes/No	[1]Yes	[1]Yes	[3]Yes	1500
5.5.1	CM	g_m, B	4/3	AP(1st), AP(2nd), BP(2nd), BP(20/40 dB/dec), BP (40/20 dB/dec), BS(2nd), BS(2nd), IDT, HP(2nd), HP(3rd), LP(1st), LP(2nd), LP(3rd) (13)	Yes/Yes	[1]Yes	-	Yes	585
5.5.2	CM	g_m, B	5/4	LP(1st), LP(2nd), LP(3rd), LP(4th) (4)	Yes/Yes	[1]Yes	-	Yes	867

Notes: [1]independent adjustment is possible under a certain condition, [2]stated functions are available from the CM (7) and VM (7) plus two additional functions of BP and HP in case of voltage to current transfer, [3]one of the working capacitors is grounded virtually through the voltage output (impedance close to zero) of the VGA element

Note that some characteristics are difficult to compare. For instance, filters of higher orders (subsections 5.5.1 and 5.5.2) are technically able to provide more functions (not only different types but also different orders), but they usually require more active and passive elements. Another aspect is whether used active elements are simple (OTA, CF, VGA, etc.) or complex (VDTA, VDCC, CG–CCDDCC, etc.). The filters with complex active elements can be constructed by less active elements in total (in case of the scheme) however, the overall number of active elements or the complexity of the CMOS structure will be higher as complex active elements are made by multiple simple elements (e.g., each VDTA is made by two OTAs). With this in mind, comparing the proposed filters based on the number of used active and passive elements, the most advantageous filter is the one from subsection 5.2.2 with two active and two passive elements (when not distinguishing between simple and complex active elements). If preferring simple active elements, the most advantageous filter is the one from subsection 5.1.1 with four simple active elements and two passive elements. The filter from subsection 5.4.1 is the most advantageous when considering the number of available transfer functions with 16 functions in total followed by the filter from subsection 5.5.1 with 13 functions. Filters in subsections 5.1.1, 5.1.2 and 5.3.2 are less suitable from the point of view of the implementation of these topologies as they do contain floating capacitors. The advantage of topologies in subsections 5.1.2 and 5.2.1 is that they do offer completely independent adjustment of their f_0 and Q (other filters offer this feature under certain conditions). The disadvantage of high order filters is that the adjustment of f_0 and especially Q is problematic. The last compared aspect is the power consumption of the proposed topology. It is evident that, the filters based on CMOS structures have way lower power consumption (tens of milli watts) in comparison to the topologies based on the usage of commercially available ICs (hundreds of milli watts) nonetheless, if the filters with commercially available ICs are designed using the CMOS technology, the power consumption would be comparable. On the other hand, the usage of commercially available ICs might be necessary if not having access to a suitable active element in given technology. In conclusion, it is safe to say each filter has its advantage and disadvantage and the selection of the most suitable filter is depending on our current preferences.

6 Design of controllable active elements and building blocks

A part of the research in the field of reconnection–less reconfigurable filters was targeted on important development of active elements and basic building blocks with an interesting and suitable controllability which can be beneficial in the design of reconnection–less reconfigurable filters and/or fractional order–filters where standard devices may not be sufficient for the expected requirements of synthesis. The design introduced in chapter 6.1 is supported by PSpice simulations (OrCAD 16.6) while concepts in chapters 6.2 and 6.3 are verified by simulations in cadence IC6 (spectre simulator) together with experimental measurements. The measurements were performed the same way as described in chapter 5 i.e., using a network analyzer Agilent 4395A and simple V–I, I–V converters created by OPA860 and OPA861. Chapter 6.1 presents a modification of a current follower/amplifier with electronically controllable current input resistance. This modification targets on its utilization for the design of reconnection–less reconfigurable filters (the number of outputs addition and the independent control of the gain of each output). Chapters 6.2 and 6.3 illustrate a design of fractional–order building blocks (two solutions of FO integrators).

6.1 Modification of Current Follower/Amplifier with Adjustable Intrinsic Resistance

This chapter deals with the modification of a previously published circuitry solution of a current follower/amplifier with electronically adjustable intrinsic resistance (real part of Z_X) originally presented in [115]. The modification consists of two main points. The first modification increases the number of available outputs for its improved performance in the design of frequency filters (CM especially), where multiple feedbacks are often needed (to suppress undesired terms in transfer functions). The second improvement gives an additional separated adjustment of the current gain of each output independently. Such advanced active element can be easily placed in almost any MISO (CM) type of filtering topology useful for features of the reconnection–less reconfiguration (unavailable without such modification). Improved concepts of this active device are also suitable for the utilization in differential topologies (working with differential signals). The research described in this chapter is presented in [158] (International Conference on Telecommunications and Signal Processing (TSP) (ISBN: 978-1-5386-4695-3), 2018).

The described proposal is based on a current follower/amplifier [115]. The particular solution of the current follower ($I_{OUT} = I_{IN}$) depicted in Fig. 6.1 a) consists of a VGA which was implemented by the VCA810 device [131] (Fig. 3.13), CCII implemented by the OPA860 [141] (also called diamond transistor (DT)) and a single resistor. An advanced solution of the same circuitry supposes a replacement of CCII (or DT) by an ECCII. ECCII can be practically implemented by EL2082 device [130] (Fig. 3.10), for instance. This modification results in a current amplifier ($I_{OUT} = BI_{IN}$) while its electronically adjustable

intrinsic resistance remains preserved as shown in Fig. 6.1 b). The electronically adjustable intrinsic resistance of these circuits is set by the DC voltage V_{SET_Rin} (the dependence given by specific implementation) and the current gain (in the case of the circuit shown in Fig. 6.1 b)) is controlled by the DC voltage V_{SET_B}.

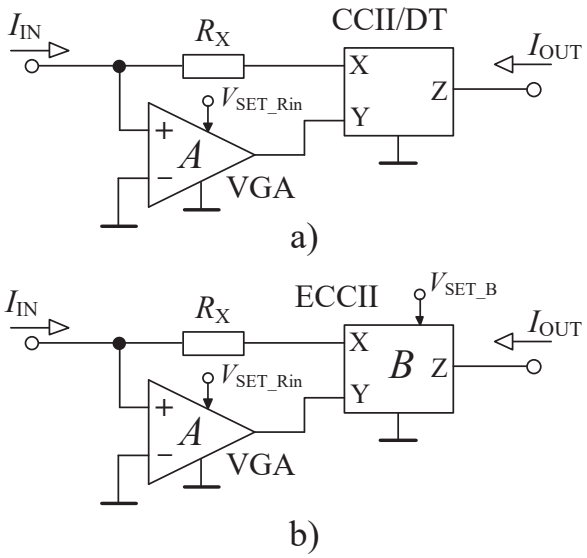


Fig. 6.1: Solution of active element with adjustable intrinsic resistance [115]: a) current follower, b) current amplifier

The ideal relation for R_{in} of both circuits in Fig. 6.1 can be expressed as:

$$R_{in} = \frac{R_X}{1 - A}. \tag{6.1}$$

The minimum value of R_{in} is equal to R_X when $A \rightarrow 0$, maximum value theoretically converges to infinity (for $A \rightarrow 1$). It is also possible to obtain negative values of resistance for $A > 1$ but possible instability must be taken into account.

Design proposal

The first modification (Fig. 6.2) of the current follower/amplifier from [115] involves additional current outputs. This advantage can be easily achieved by the replacement of the CCII/DT element in the structure by the UCC. UCC consists of four outputs (two positive and two negative). The power consumption of the circuit in Fig. 6.2 a) is given as 192.4 mW. Reference [115] includes a solution with multiple outputs, but the input current divides into identical parts of identical individual branches and thus, the current transfer will not have unity value and further amplification must be ensured. The gain is compensated by ECCIIs, depending on the number of outputs. However, gain of EL2082s used in the implementation can only be set up to value 3 without a significant error of linearity of gain vs driving voltage

dependence. That limits the number of outputs up to three (for unity gain transfer of each output). In such case, it provides possible adjustment only in one direction of gain from 3 to 0 (attenuation of the resulting output signals if the gain is less than 3).

The UCC in Fig. 6.2 a) can be replaced by an ACA with multiple outputs. This arrangement solves the requirement for current amplification adjustability. Figure 6.2 b) introduces the new differential–mode version of the modified circuit. This modification consists of two independent branches to set the R_{in} for each input (VGA, CCII/DT, and resistor) and fully-differential current follower (FD–CF). The resulting circuitry provides four single–ended outputs (creating two pairs of differential outputs). The FD–CF can be replaced by a differential current amplifier to provide adjustable amplification. Also, CCIIs/DTs in Fig. 6.2. b) can be replaced by ECCIIs for independent gain control of each input. The modified circuits from Fig. 6.2 follow the same relations as the original circuit in [115]. The transfer function of the differential version can be expressed as $I_{OUTi\pm} = \pm(I_{IN+}\text{-}I_{IN-})$ for MO-CF, $I_{OUTj\pm} = \pm B(I_{IN+}\text{-}I_{IN-})$ in case of version with an adjustable amplification where i and $j = \{1, 2\}$.

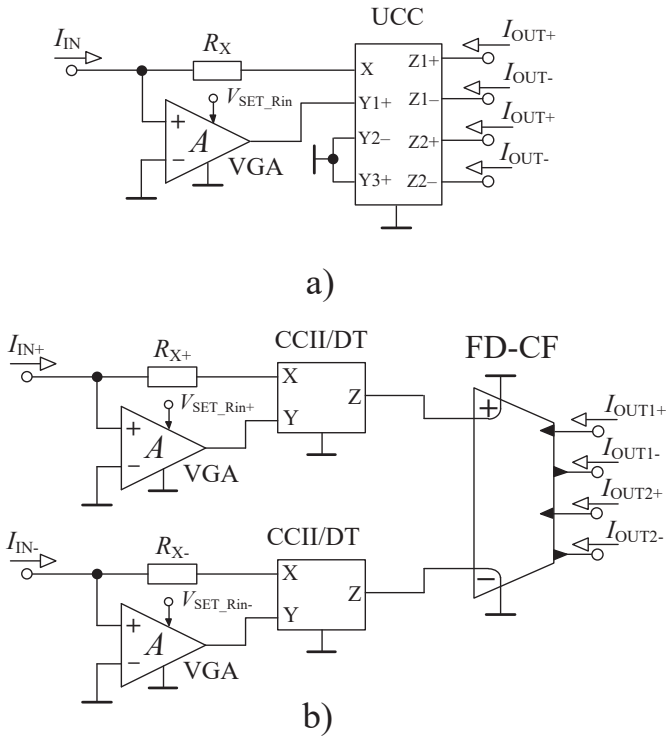


Fig. 6.2: New modified active element based on current follower with adjustable intrinsic resistance from [115]: a) single–ended version, b) differential version

The further modification comprises an addition of ECCIIs for each output of solutions in Fig. 6.2. Therefore, the independent gain control of each output current can be achieved. Figure 6.3 a) shows the non–differential version of this modification containing VGA, UCC, single resistor and four ECCIIs. The power consumption of the solution in Fig. 6.3 a) is

592.4 mW. The transfer function of the circuit (for each of individual output) follows relation $I_{OUT\pm} = \pm B_i(I_{IN})$, where $i = \{1, 2, 3, 4\}$. The resulting active element has been designed specifically to be added to a structure of MISO type filters for modification bringing the reconnection–less reconfiguration. The differential version of active element in Fig. 6.3 b) consists of two VGAs, two CCIIs/DTs, two resistors, one FD–CF and two ACAs providing two differential (independent adjustment of gains) outputs. The transfer function of this solution is given by relation $I_{OUT\pm} = \pm B_j(I_{IN+}\text{-}I_{IN-})$, where $j = \{1, 2\}$.

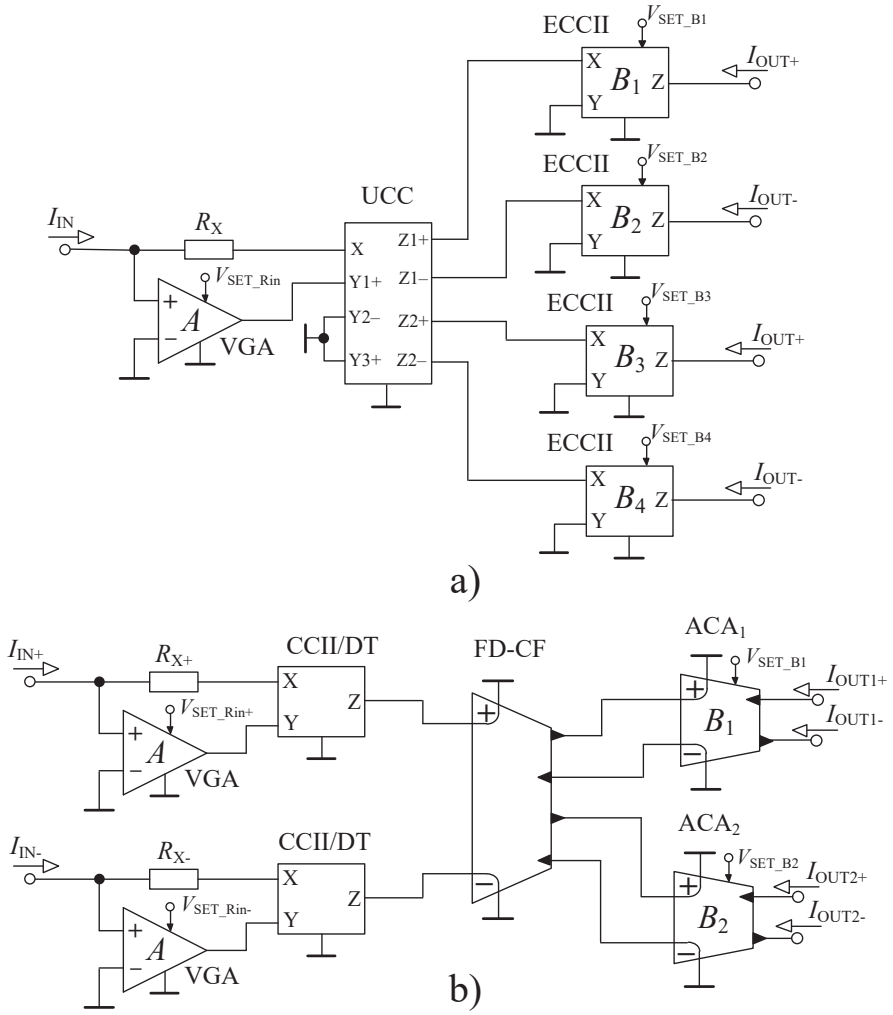


Fig. 6.3: Further modification of active element from Fig. 6.2 offering individual gain control of outputs: a) single–ended version, b) differential version

Design verification

Figure 6.4 depicts characteristics of R_{in} of circuits from Fig. 6.2 (R_{in+} (the positive branch) of the differential version from Fig. 6.2 b)) for several settings of gain A (V_{SET_Rin}, respectively). The voltage V_{SET_Rin}, controlling the gain of VGA element ($A = 10\text{^}(2*(V_{SET}\text{-}$

1))), was set to -0.65, -0.8, -0.89 and -0.951 which corresponds with gains A = 0.2, 0.4, 0.6 and 0.8. The value of external resistor R_X was selected as 1 kΩ. The theoretical values of R_{in} achieve 1250 Ω, 1667 Ω, 2500 Ω and 5000 Ω for selected examples. The simulated values of R_{in} are listed in the graph and compared in Tab. XXXI. The setting of control voltages was identical for both the non–differential and differential version. The features of the negative branch of the differential circuit are almost identical. The values of input impedance (resistive part) of the differential version (Fig. 6.2 b)) seem to be closer to the theoretical expectations than for the non–differential version (Fig. 6.2 a)). The differential version also provides wider bandwidth. The bandwidth reaches approximately 2 MHz for the differential version and 1 MHz for the non–differential version when A = 0.8, for example (as it can be seen in Fig. 6.4). The usable bandwidth increases with lower values of R_{in}.

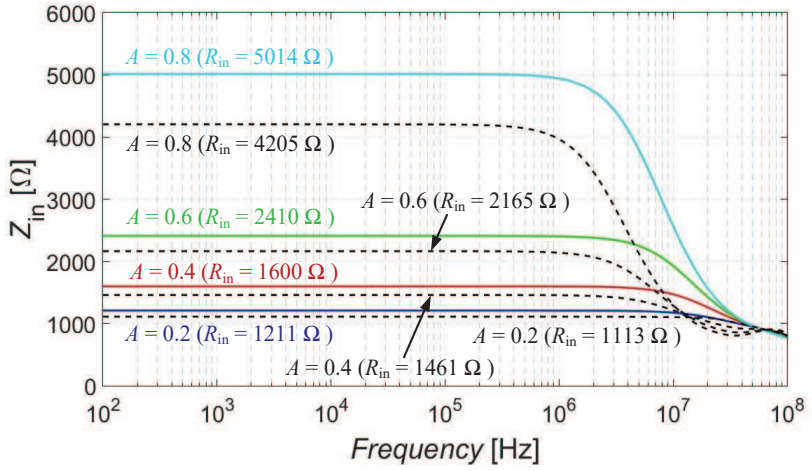


Fig. 6.4: Dependence of input impedance (resistive part) of the circuit from Fig. 6.2 a) (black dashed lines) and circuit from Fig. 6.2 b) (solid colored lines)

TABLE XXXI. COMPARISON OF THEORETICAL RIN WITH SIMULATED RIN OF THE NON-DIFFERENTIAL AND DIFFERENTIAL CIRCUIT FROM FIG. 6.2

A [–]	0,2	0,4	0,6	0,8
Theoretical R_{in} [Ω]	1250	1667	2500	5000
Simulated non–diff. R_{in} [Ω]	1113	1461	2165	4205
Simulated diff. R_{in} [Ω]	1211	1600	2410	5014

Figure 6.5 compares the dependence of the real part of input impedance of circuits from Fig. 6.2 on the selected value of gain A. Gain A was set in range from 0.1 to 0.9. The differential version is better in accuracy of R_{in} setting. The dependency follows the theoretical expectations up to A approximately 0.85. The values > 0.85 cause significantly higher input resistance than expected (caused by the inaccuracy of the actual gain which is higher than expected and sooner converges to 1). Based on the PSpice analysis, elements from Fig. 6.3 have almost identical (theoretically identical) behavior (AC and DC characteristics) of their adjustable intrinsic resistance with the elements from Fig. 6.2.

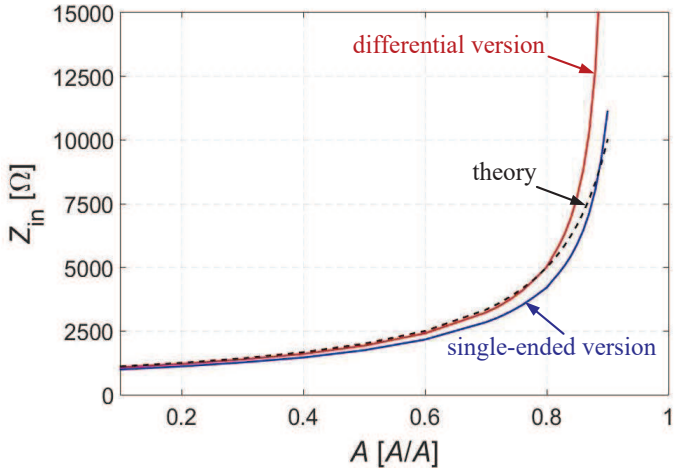


Fig. 6.5: Comparison of the dependence of intrinsic impedance (resistive part) of the circuit from Fig. 6.2 a) (blue line), circuit from Fig. 6.2 b) (red line) and theory (black dashed line)

Application example

The current followers with adjustable intrinsic input resistance R_{in} (from Fig. 6.2) have been utilized in a current–mode (CM) frequency filter taken from prototype [34] (where R_{in} can be used for the adjustment of the pole frequency) in order to verify the proper function of proposed active devices when implemented in a specific circuit topology. Similarly, the proposed active element from Fig. 6.3 a) could be simply connected to the input of the filter from chapter 5.2.1 for solution of the reconnection–less reconfiguration of its transfer instead of the MO–CF and ACA_1 to ACA_3 elements. The filter structure from [34] has been simplified and adapted for this particular case. The simplification of the original structure comprises removal of the current follower in the input part of the structure. Now, the filter does not provide the high–pass transfer function anymore. This modification turns the filter from universal (all standard transfer functions) into multifunctional (band–pass and low–pass function in this particular case). It has been done to simplify the resulting filter which is used simply for demonstrational purposes. Since the current follower at the end of the filter topology offers only four outputs but six outputs in total are required for further processing. Therefore, two additional second generation current conveyors with positive and negative output (CCII±) have been added (provide additional required outputs). Resulting filtering F–D structure can be seen in Fig. 6.6. This circuit consists of two current followers with adjustable intrinsic resistance, two CCII±s and four capacitors.

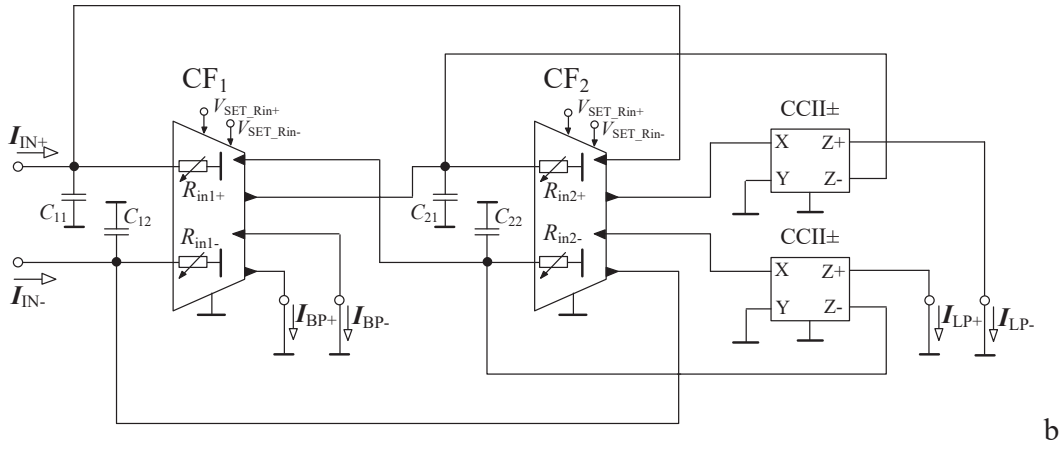


Fig. 6.6: Application of a multifunctional CM filter employing differential CFs with adjustable intrinsic resistance from Fig. 6.2 b)

The transfer function of circuit in Fig. 6.6 is given by:

$$K(\boldsymbol{s}) = \frac{N(\boldsymbol{s})}{\boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 G_{IN1} + G_{IN1} G_{IN2}}, \tag{6.2}$$

where $N(\boldsymbol{s}) = \pm \boldsymbol{s} C_2 G_{\text{in1}}$ in case of BP outputs and $\pm G_{\text{in1}} G_{\text{in2}}$ for LP outputs. The pole frequency and quality factor of the filter can be derived in forms:

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{G_{in1} G_{in2}}{C_1 C_2}}, \tag{6.3}$$

$$Q = \sqrt{\frac{C_1 G_{in2}}{G_{in1} C_2}}. \tag{6.4}$$

The values of capacitors used in simulations are 1 nF. Gain A was set to values 0.2, 0.4, 0.6 and 0.8 ($R_{\text{in1}} = R_{\text{in2}}$, in both positive and negative branch) which results into theoretical values of f_0 (depending on simulated values of R_{in}) of 131.5 kHz, 99.5 kHz, 66.0 kHz, 31.7 kHz for the differential version of the filter and 143.0 kHz, 109.0 kHz, 73.5 kHz, 37.9 kHz in case of the non–differential filter structure. These simulated results of the non–differential filter were included for comparison. The setting of the non–differential and differential filter was identical. Figure 6.7 compares obtained values of f_0 for selected gains A. These results are also compared with the theory in Tab. XXXII for the non–differentiated version of the filter and in Tab. XXXIII for the differential version. The values valid for the differential filter tend to better correspond to expected values than the non–differential solution.

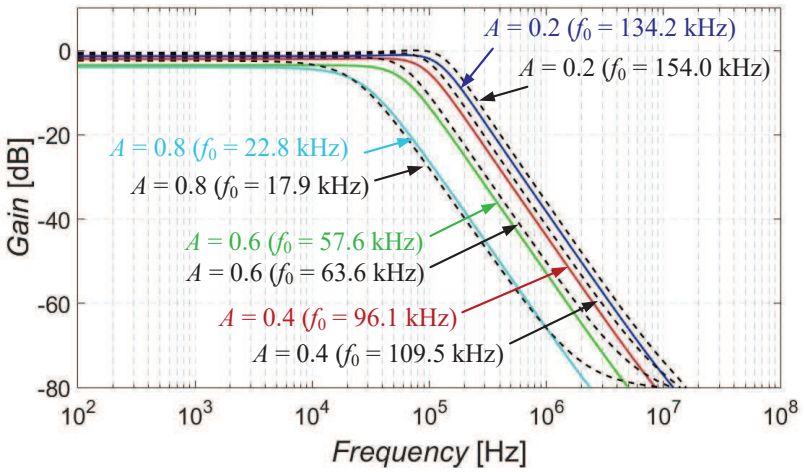


Fig. 6.7: Comparison of simulation results of differential filter from Fig. 6.6 (colored solid lines) and its non–differential counterpart (black dashed lines)

TABLE XXXII. COMPARISON OF THEORETICAL AND SIMULATED F0 FOR THE NON–DIFFERENTIAL FILTER

A [–]	**0,2**	**0,4**	**0,6**	**0,8**
Simulated non–diff. R_{in} [Ω]	1113	1461	2165	4205
Theoretical (non–differential) f_0 [kHz]	143,0	109,0	73,5	37,9
Simulated (non–differential) f_0 [kHz]	154,0	109,5	63,6	17,9

TABLE XXXIII. COMPARISON OF THEORETICAL AND SIMULATED F0 FOR THE DIFFERENTIAL FILTER

A [–]	**0,2**	**0,4**	**0,6**	**0,8**
Simulated diff. R_{in} [Ω]	1211	1600	2410	5014
Theoretical (differential) f_0 [kHz]	131,5	99,5	66,0	31,7
Simulated (differential) f_0 [kHz]	134,2	96,1	57,6	22,8

The concept of a current amplifier with independently controlled outputs (Fig. 6.3 a)) under abbreviation IOGC–CA has been also used for the design of structures in subsection 5.2.2 and both filters in section 5.5. Both filters in section 5.5 use the implementation shown in Fig. 6.3 (solution in subsection 5.5.2 additionally uses two OPA860 (based inverting follower) in first and third branch for the polarity change of given outputs). The solution of IOGG-CA used in subsection 5.2.2 is created by the CCCII and MLTs from the chip, fabricated in I3T25 0.35 μm CMOS process introduced in [125], and grounded external resistors (see Fig. 6.8).

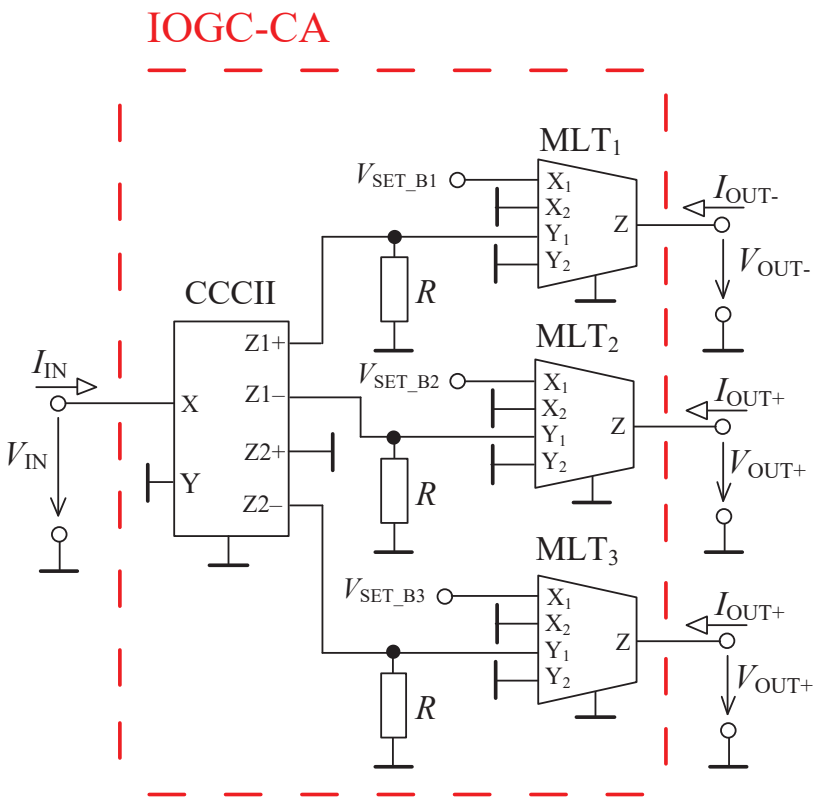


Fig. 6.8: Specific implementation of the inter structure of IOGC–CA used in chapter 5.2.2

6.2 Fractional–order integrator based on a FLF topology

This contribution presents a design of a current–mode fractional–order electronically adjustable integrator which can be used as a building block for a design of fractional–order circuits (including filters, resonators, oscillators, etc.). The design is based on a 2nd–order Follow–the–Leader–Feedback topology which is suitably approximated to operate as an integrator of a fractional order. The proposed topology offers the electronic adjustment of its order and also the electronic adjustment of the central frequency of the frequency band. This integrator has been partially used in the design of the FO filter introduced in subsection 5.5.2. The topic of this section was published in [159] (International Conference on Electronics Circuits and Systems (ICECS) (ISBN: 978-1-7281-6044-3), 2020).

Design proposal

The 2nd–order FLF topology, used for the approximation of the CM FO integrator, is depicted in Fig. 6.9. It contains two OTAs, one CF, three ACAs (6 active elements in total) and two grounded capacitors. The OTA element has been created by the MLT (Fig. 3.4). Since the multiplication unit has only one output, the CCCII [125] (in form of a current follower) has been connected to this output in order to provide copies (both

directions/polarities) of the output current. The ACA has been created by the MLT and one resistor at the input (Fig. 3.11). The CCCII was used to perform a function of the CF. The number of active elements can be decreased to five as current gain B_2 is always equal to 1 (given by used approximation of FO behavior [61]) with a proper polarity of this branch in mind.

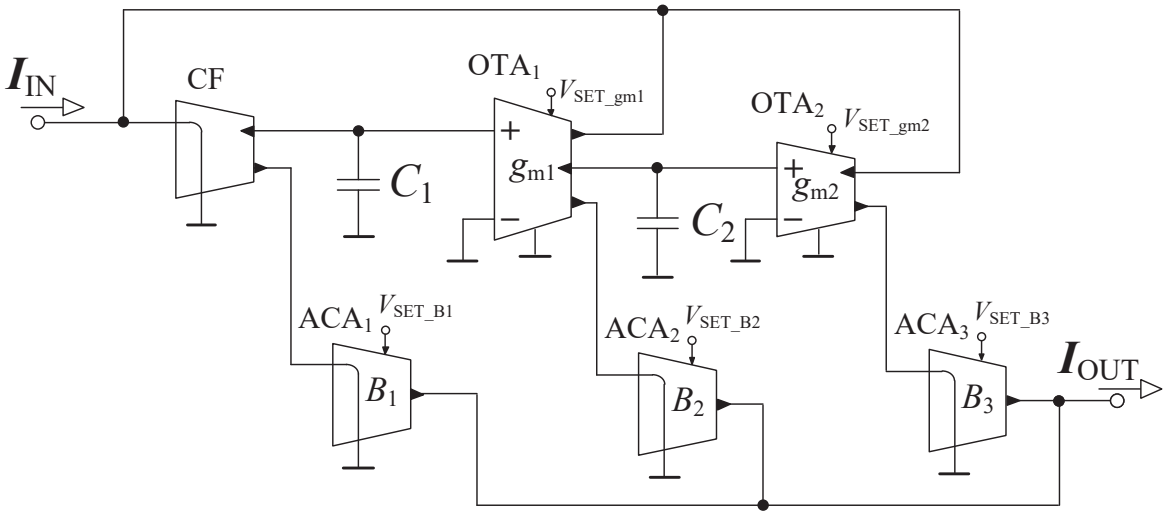


Fig. 6.9: 2nd–order FLF topology used for the approximation of a CM FO integrator

The transfer function of the structure in Fig. 6.9 is given by:

$$K(\boldsymbol{s}) = \frac{\boldsymbol{s}^2 C_1 C_2 B_1 + \boldsymbol{s} C_2 g_{m1} B_2 + g_{m1} g_{m2} B_3}{\boldsymbol{s}^2 C_1 C_2 + \boldsymbol{s} C_2 g_{m1} + g_{m1} g_{m2}}. \tag{6.5}$$

The second–order approximation of $\boldsymbol{s}^{\alpha}$ is expressed as:

$$\boldsymbol{s}^{\alpha} \cong \frac{a_0 \boldsymbol{s}^2 + a_1 \boldsymbol{s} + a_2}{a_2 \boldsymbol{s}^2 + a_1 \boldsymbol{s} + a_0}. \tag{6.6}$$

The values of a_0, a_1, a_2 (when using a second–order approximation provided in [61]) are given as $a_0 = \alpha^2 + 3\alpha + 2$, $a_1 = 8 - 2\alpha^2$, $a_2 = \alpha^2 - 3\alpha + 2$ (obtained by Continued Fraction Expansion (CFE) method [61]). Thus, the general transfer function, which approximates the 2nd–order FLF topology in order to behave as a FO integrator, is given as:

$$K(\boldsymbol{s}) = \frac{(\frac{\alpha^2 - 3\alpha + 2}{\alpha^2 + 3\alpha + 2})\boldsymbol{s}^2 + \frac{1}{\tau}(\frac{8 - 2\alpha^2}{\alpha^2 + 3\alpha + 2})\boldsymbol{s} + \frac{1}{\tau^2}}{\boldsymbol{s}^2 + \frac{1}{\tau}(\frac{8 - 2\alpha^2}{\alpha^2 + 3\alpha + 2})\boldsymbol{s} + \frac{1}{\tau^2}(\frac{\alpha^2 - 3\alpha + 2}{\alpha^2 + 3\alpha + 2})} . \tag{6.7}$$

The values of each variable in (6.5), for selected value of α and chosen operational frequency, can be determined when comparing (6.5) with (6.7).

Design verification

In order to support the proposed design, simulations in Cadence IC6 (spectre) and experimental measurements were carried out. The OTA element has been created by the MLT. Since the multiplication unit has only one output, the CCCII (in form of a current follower) has been connected to this output in order to provide copies of the output current. The ACA has been created by the MLT and one resistor. The CCCII was used to perform a function of the CF. The experimental measurements are done with the UCC substituting the OTA and CF elements and EL2082 device to implement ACA element. The expected power consumption of the CMOS–based implementation is approximately 89.4 mW. The central operational frequency f_C of the bandwidth where the approximation is valid has been chosen to be 50 kHz. The values of capacitors are selected as follows C_1 = 1 nF and C_2 = 10 nF. The values of transconductances g_{m1} and g_{m2} and current gains B_1, B_2, B_3 have been calculated based on the selected operational frequency and chosen approximation.

The electronic adjustment of FO of the proposed integrator is demonstrated in Fig. 6.10 for the simulation results represented by black dashed lines and the experimental results denoted by colored lines. The results are provided for α equal to 0.1 to 0.7 with step of 0.1. Specific values of transconductances and current gains in dependence on α are provided in Tab. XXXIV. As evident from the table, higher values of α require values of current gains which are more difficult for the physical realization using discussed active elements (either too low (B_1) or too high (B_3)). Therefore, the proposed circuit is more suitable for lower values of α ($\alpha < 0.7$ depending on the implementation). The approximation of fractional–order behavior is valid for approximately two decades (Fig. 6.10). The usable bandwidth is also limited by the frequency restrictions of used active elements as observable at frequencies above 3 MHz. The experimental traces (in case of the magnitude) are slightly (about 3 dB) higher than the simulation results. Nonetheless, both results confirm operationability of the intended function and design correctness.

TABLE XXXIV. VALUES OF INDIVIDUAL PARAMETERS OF THE INTEGRATOR IN DEPENDENCE ON VALUES OF ALPHA

α [–]	**0.1**	**0.2**	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**
g_{m1} [µS]	1090	942	822	718	628	550	480
g_{m2} [µS]	673	571	478	393	314	242	175
B_1 [–]	0.74	0.55	0.40	0.29	0.2	0.14	0.085
B_2 [–]	1						
B_3 [–]	1.35	1.83	2.51	3.5	5	7.43	11.77

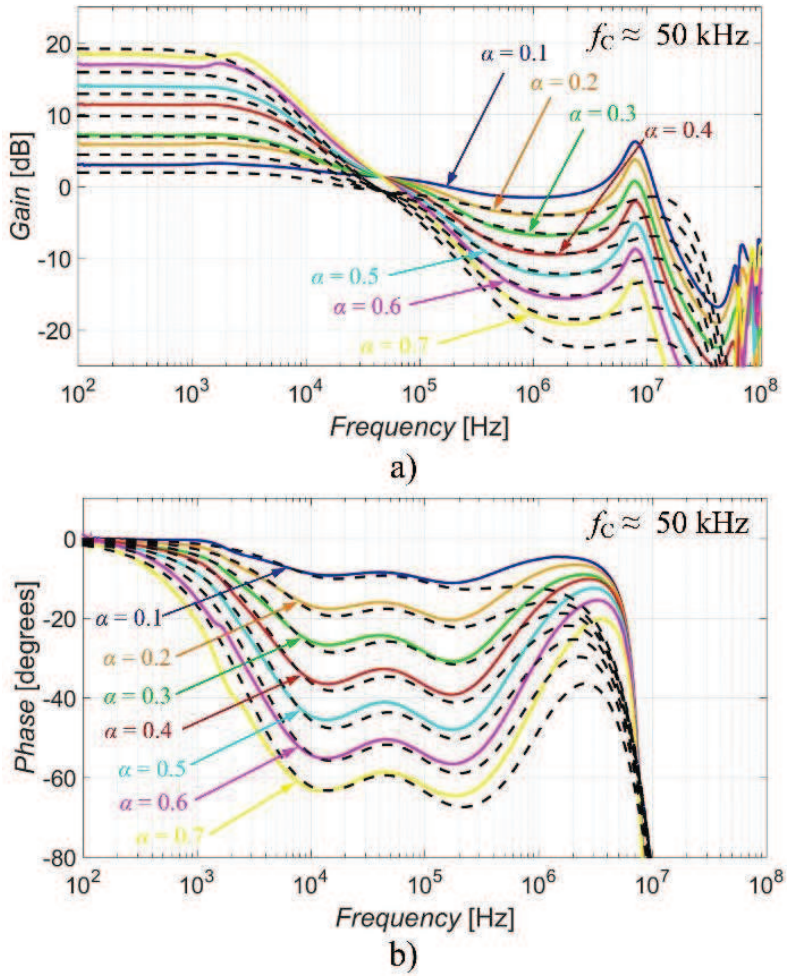


Fig. 6.10: Electronic adjustment of the order of the proposed FO integrator (experimental measurement (colored lines), simulations (black dashed lines)): a) magnitude characteristics, b) phase characteristics

This solution allows a simple adjustment of the central frequency of the operational bandwidth where the approximation is valid. This adjustment is achieved through the change of transconductances (g_{m1} and g_{m2}) as long as the ratio between them is preserved constant. That shifts the bandwidth to desired frequencies. Figure 6.11 demonstrates the frequency shift of the operational bandwidth for three different settings of transconductances (provided in the

Tab. XXXV) where the theoretical (center) frequency f_C is approximately equal to 25 kHz, 50 kHz, and 100 kHz. The demonstration example is valid for α = 0.5, thus the setting of current gains is the same as for α = 0.5 in Tab. XXXIV for all three cases in Fig. 6.11. Lower upper DC gain of the 25kHz characteristic is most likely caused by limited linear behavior based on the values of transconductances and/or by the DC offset (for used gain) being too high.

TABLE XXXV. VALUES OF TRANSCONDUCTANCES (FOR ALPHA = 0.5) IN DEPENDENCE ON THE ADJUSTMENT OF THE FREQUENCY BAND

Theoretical frequency f_C [kHz]	**25**	**50**	**100**
g_{m1} [µS]	314	628	1256
g_{m2} [µS]	157	314	628

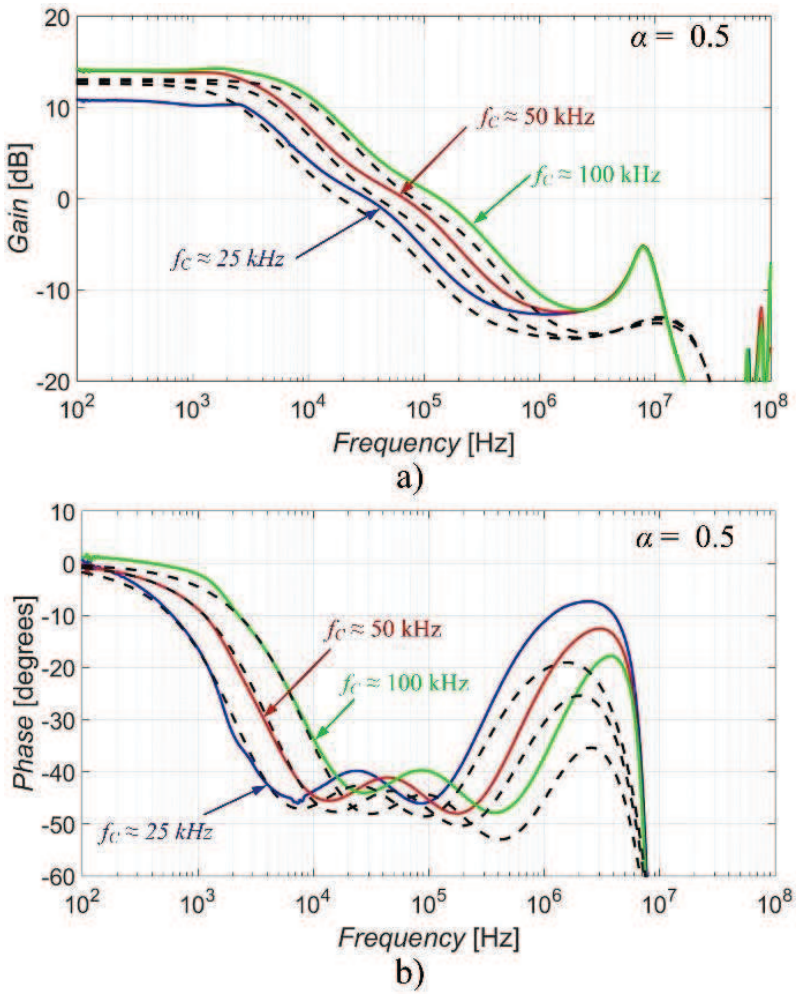


Fig. 6.11: Electronic adjustment of the frequency band of the proposed FO integrator (experimental measurement (colored lines), simulations (black dashed lines)): a) magnitude characteristics, b) phase characteristics

Usable bandwidth expansion

The analogous 4th–order FLF topology (Fig. 6.12) has been designed in order to provide wider operational bandwidth where the FO approximation is valid. The topology consists of one CF, four OTAs, five ACAs and four grounded capacitors. Since the value of current gain B_3 is always 1, the ACA_3 can be omitted (9 active elements used in total). The 4th–order approximation of FO integrator provided in [97] has been used. When the center frequency is approximately equal to 50 kHz and $\alpha = 0.5$, $C_1 = 100$ pF, $C_2 = C_3 = 1$ nF, $C_4 = 10$ nF, the values of remaining parameters were calculated accordingly: $g_{m1} = 293$ μS, $g_{m2} = 471$ μS, $g_{m3} = 898$ μS, $g_{m4} = 87$ μS, $B_1 = 0.11$ $B_2 = 0.43$ $B_3 = 1$, $B_4 = 2.33$ $B_5 = 9$. The values of transconductances and current gains were obtained similarly as in case of the topology from Fig. 6.9 (the comparison of the transfer function of the proposed structure and the relation of the 4th–order FO approximation). The transfer function of the structure in Fig. 6.12 is given as $K(\boldsymbol{s}) = N(\boldsymbol{s})/D(\boldsymbol{s})$, where:

$$N(\boldsymbol{s}) = \boldsymbol{s}^4 C_1 C_2 C_3 C_4 B_1 + \boldsymbol{s}^3 C_2 C_3 C_4 g_{m1} B_2 + \boldsymbol{s}^2 C_3 C_4 g_{m1} g_{m2} B_3 + \\ + \boldsymbol{s} C_4 g_{m1} g_{m2} g_{m3} B_4 + g_{m1} g_{m2} g_{m3} g_{m4} B_5 \quad , \tag{6.8}$$

$$D(\boldsymbol{s}) = \boldsymbol{s}^4 C_1 C_2 C_3 C_4 + \boldsymbol{s}^3 C_2 C_3 C_4 g_{m1} + \boldsymbol{s}^2 C_3 C_4 g_{m1} g_{m2} + \\ + \boldsymbol{s} C_4 g_{m1} g_{m2} g_{m3} + g_{m1} g_{m2} g_{m3} g_{m4} \quad . \tag{6.9}$$

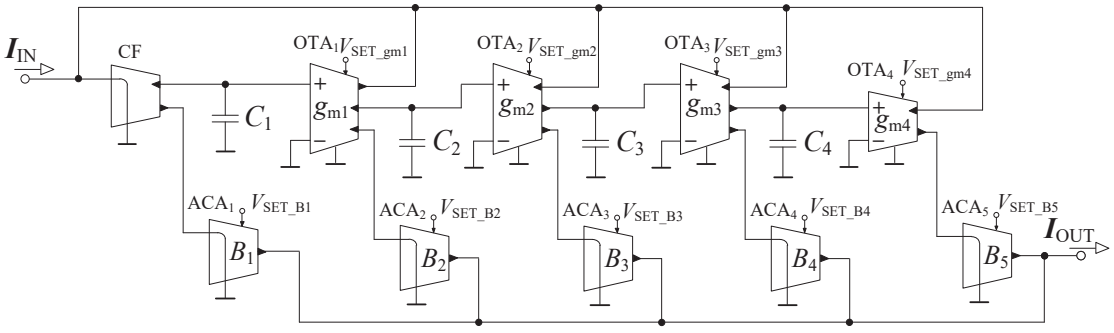


Fig. 6.12: 4th–order FLF topology used for the approximation of a CM FO integrator

The comparison of the simulation results (colored lines) and theoretical expectations (black dashed lines) of the integrator from Fig. 6.9 (blue lines) and the integrator from Fig. 6.12 (red lines) is presented in Fig. 6.13. The integrator from Fig. 6.12 provides wider bandwidth of the approximation validity (about three decades) in comparison to the integrator from Fig. 6.9 (about two decades). The usable bandwidth depends on the order of the used approximation. Considering 5° phase error for the case when $\alpha = 0.5$ (Fig. 6.13), the bandwidth is given as approximately $f_C/10$ and $f_C \cdot 10$ for $n = 2$ (order of used approximation) and $f_C/25$ and $f_C \cdot 10$ for $n = 4$.

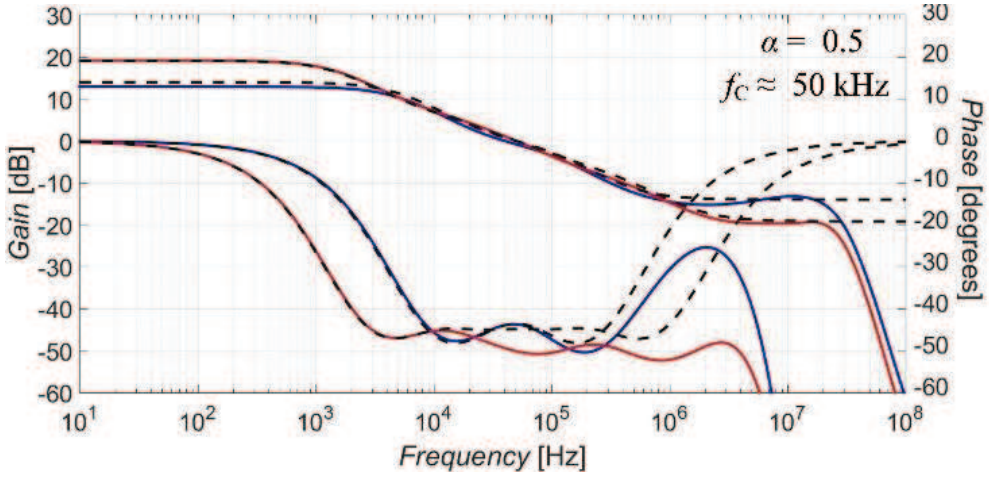


Fig. 6.13: Comparison of the simulation (colored lines) and theoretical (black dashed lines) results of the integrator from Fig. 6.9 (blue lines) and the integrator from Fig. 6.12 (red lines)

This design requires five active elements and two passive elements in case of the 2nd–order topology (with usable operational bandwidth of about 2 decades (considering 5° phase error)) and nine active and four passive elements in case of the 4th–order topology (with usable operational bandwidth of about 3 decades) which is fewer active elements needed in comparison to other previously proposed integrators based on the approximation of the FO Laplacian operator [84–87] while providing same bandwidth range. The proposed circuit topology is identical for the operation of FO differentiator when parameters are calculated accordingly.

6.3 Fractional–order integrator with simple controllability

This section presents a design of a fractional–order integrator. The CM solution provides a simplified electronic adjustment of the order and gain adjustment in comparison to previously introduced integrator/differentiator designs. Despite this solution is based on the utilization of RC approximants (nonadjustable in time constant and order), electronic adjustability of the order is possible in this case. Moreover, the control of the proposed integrator does not require specific and accurate values of the control voltages/currents in comparison to the topologies based on the approximation of the FO Laplacian operator (discussed above). The proposed integrator can be used to build various FO circuits as demonstrated by the utilization of the integrator into a structure of a frequency filter in order to provide FO characteristics. This research is contained in [160].

Design proposal

The design of the proposed integrator is based on the utilization of a chip introduced in [125]. The proposed CM FO integrator is depicted in Fig. 6.14. The structure involves one CF and several OTAs. The CF element has been created by the CCCII cell of the chip [125]. The MLTs have been used for OTAs construction (Fig. 3.4). The number of OTAs depends

on number of orders we want to obtain (required range and variety of the desired orders, respectively). We consider the orders 0.1, 0.3, 0.5, 0.7, and 0.9 (five orders) which then require five branches of the proposed integrator and thus five OTAs in this case. Such variety of possible orders is sufficient for general needs and the proposal verification. The power consumption of such topology is 55.8 mW. Additional orders can be obtained by simple increase of branches. The five orders require one additional output for the CF element. It can be easily solved on–chip. Each branch also contains an RC FOE approximant of specific RC values corresponding with the particular order. The resulting order of the integrator depends on the control of the OTAs. Each order is available by a selection a specific OTA, g_{ms} of other OTAs are set to zero. Thus, the control of the resulting order is simple (either being switched on or off). In such case, it would be easier to use simple electronically controllable switches rather than comparably complex CMOS structure of the OTAs, however, using the OTAs offers a possibility of additional electronic adjustment of the integrator parameters (possibility of the gain adjustment in this particular case). Also, a possibility to invert the polarity of the output response is available thanks to the used multiplication unit, as it can work in all four quadrants. The specific setting of the integrator is presented in Tab. XXXVI in correspondence with the desired orders. The default used value of the transconductance, when the OTA is set, was chosen to be 0.5 mS.

TABLE XXXVI. SETTING OF THE CONTROL OF THE CM FO INTEGRATOR DEPENDING ON THE DESIRED ORDER

α [–]	**0.1**	**0.3**	**0.5**	**0.7**	**0.9**
g_{m1} **[mS]**	0.5	0	0	0	0
g_{m2} **[mS]**	0	0.5	0	0	0
g_{m3} **[mS]**	0	0	0.5	0	0
g_{m4} **[mS]**	0	0	0	0.5	0
g_{m5} **[mS]**	0	0	0	0	0.5

The transfer function of the integrator in Fig. 6.14 is expressed as:

$$\frac{\boldsymbol{I}_{OUT}}{\boldsymbol{I}_{IN}} = \frac{g_{mi}}{\boldsymbol{s}^{\alpha} C_{\alpha i}}, \tag{6.10}$$

where g_{mi} and $C_{\alpha i}$ denote the specific transconductance and FO pseudo capacitance depends on currently selected OTA (g_{mi}), thus $i = \{1, 2, 3, 4, 5\}$.

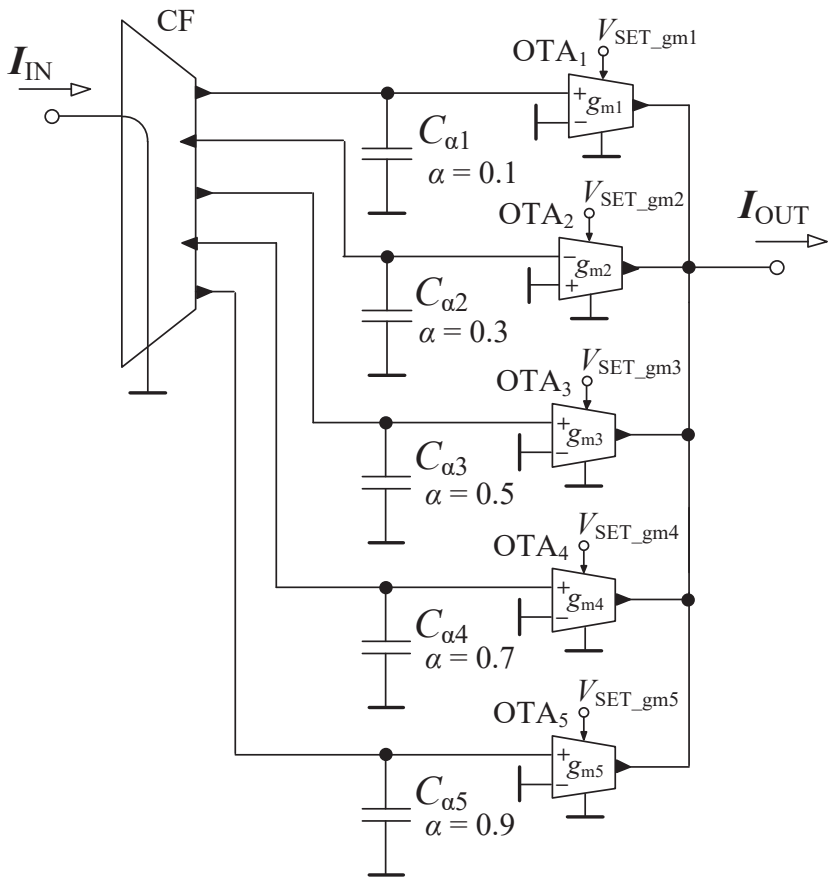


Fig. 6.14: Proposed current–mode fractional–order integrator

The integrator has theoretically lossless character. Figure 6.15 shows a possible modification of the proposed CM integrator from Fig. 6.14. This modification consists of one additional CF (CF_2) and one ACA added into the structure. It results into advantageous selection between the lossless and lossy integrator. Unfortunately, it extends complexity (two more active elements in the structure). Nonetheless, the presence of the CF with multiple outputs (more than two used in Fig. 6.15) at the output of the integrator is desirable in the design of CM circuits. The CF at the output also provides an impedance separation. The transfer function of the modified reconnection-less reconfigurable (it fulfils definition of such circuit) integrator (Fig. 6.15) is given by:

$$\frac{\boldsymbol{I}_{OUT}}{\boldsymbol{I}_{IN}} = \frac{g_{mi}}{\boldsymbol{s}^{\alpha} C_{\alpha i} + g_{mi} B}. \tag{6.11}$$

The integrator behaves as lossless for $B = 0$, when the integrator follows the equation (6.10), or lossy for $B = 1$.

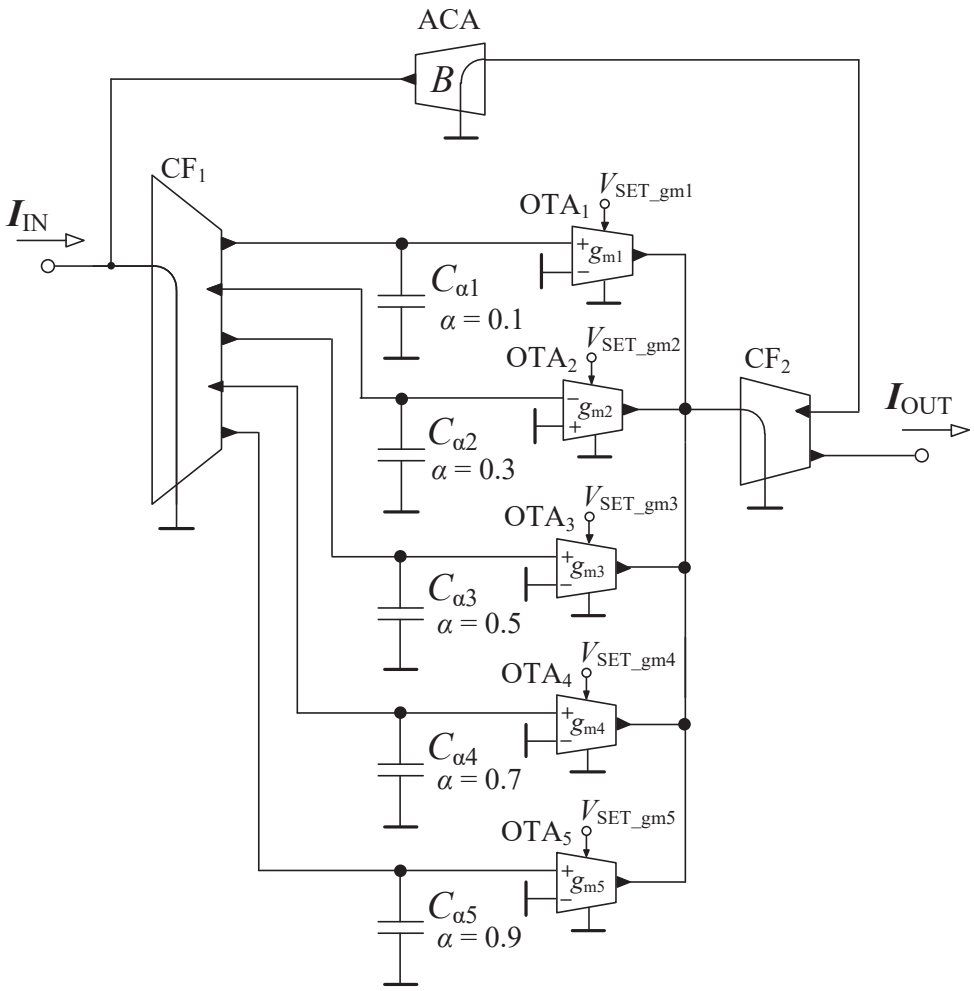


Fig. 6.15: Modified structure of the CM integrator allowing to electronically change between lossy and lossless behavior

Design verification

The simulation results were carried out in Cadence IC6 (spectre) software. The experimental measurements were performed with our fabricated chip (0.35 μm, I3T25 CMOS process) [125]. The RC approximants of FOE of required orders have been implemented (parameters in Tab. XXXVII). A 5th–order Foster I type RC topology (Fig. 5.32) has been used. The values of the individual RC parts of the approximants of FOEs were calculated using the Oustaloup approximation in Matlab software for central frequency f_C of 10 kHz. The particular values are summarized in Tab. XXXVII.

TABLE XXXVII. VALUES OF THE INDIVIDUAL PARTS WITHIN THE RC STRUCTURE IN CORRELATION WITH THE DESIRED ORDER

α [–]	**0.1**	**0.3**	**0.5**	**0.7**	**0.9**
R_0 [Ω]	1476.8	587.9	234.1	93.2	37.1
R_1 [Ω]	285.6	365.1	241.5	113.9	27.5
R_2 [Ω]	354.2	685.6	676.1	470.7	166.8
R_3 [Ω]	428.1	1208.0	1735.2	1759.5	909.1
R_4 [Ω]	517.7	2143.6	4546.3	6872.6	5374.7
R_5 [Ω]	647.1	4327.5	15972.0	49481.2	141161.4
C_1 [nF]	1.54	1.44	2.62	6.69	33.3
C_2 [nF]	7.81	4.85	5.91	10.2	34.6
C_3 [nF]	40.8	17.4	14.5	17.2	40.1
C_4 [nF]	212.7	61.8	35.0	27.8	42.8
C_5 [nF]	1073.6	193.0	62.9	24.4	10.3

The values of transconductances of individual OTA elements in the integrator structure are either set to zero or 0.5 mS. The value 0.5 mS corresponds with the value V_{SET_gm} of 0.26 V in simulations and 0.39 V in case of the experimental measurements due to expected differences between the simulated and measured transconductance constant (1.3 and 2 mA/V^2) in dependence on the control voltage. Then the transconductance was defined as $g_m \cong 2 \cdot V_{SET\_gm}$ [mS] in the simulations and $g_m \cong 1.3 \cdot V_{SET\_gm}$ [mS] for the implemented chip (standardly expected deviations fitting process corners, voltage, and temperature variations) [125].

Figure 6.16 shows a comparison of the theoretical expectations (black dashed lines) and simulation results (colored lines) of the magnitude and phase characteristics of the proposed integrator for orders (0.1, 0.3, 0.5, 0.7 and 0.9).

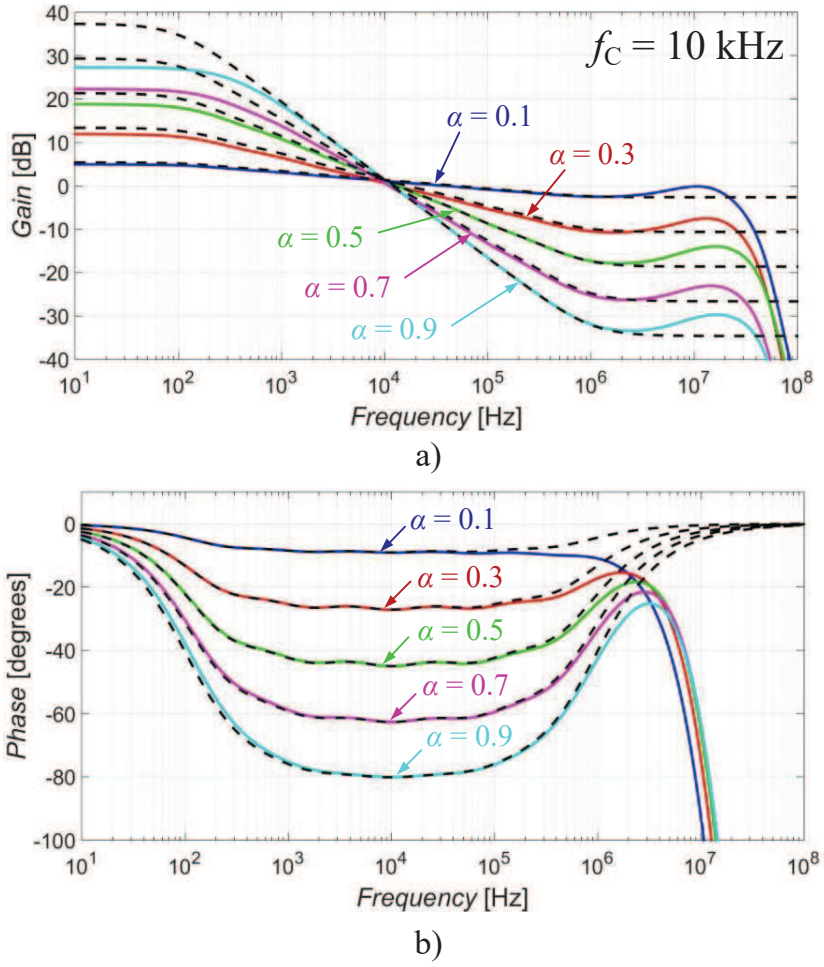


Fig. 6.16: Magnitude (a)) and phase (b)) characteristics of the proposed integrator for used orders (0.1, 0.3, 0.5, 0.7 and 0.9): theoretical expectations (black dashed lines), simulation results (colored lines)

A relative error of the phase characteristics across the operational bandwidth was carried out (Fig. 6.17) in order to evaluate the performance of the proposed integrator (the accuracy of the resulting order of the integrator and its operational bandwidth). The error is expressed in percentage as a deviation of the value of the phase obtained from the simulations and compared to the theoretical value of phase shift for given nominal (ideal) order (i.e. -9˚, -27˚, -45˚, -63˚ and -81˚ (constant across all frequencies) for orders 0.1, 0,3, 0,5, 0.7 and 0.9). The useful operational bandwidth (f_{min}, f_{max}) of given order, established for a frequency band with a relative error under 10% of phase deviation (i.e., 0.9˚, 2,7˚, 4,5˚, 6,3˚ and 8,1˚ depending on the order), is summarized in Tab. XXXVIII. The operational bandwidth (where the FO approximation is valid for the 5th–order RC structure of approximant) is above 2 decades in all cases. An RC structure of approximant of higher order (larger number of segments) can be easily designed when a wider operational bandwidth is required.

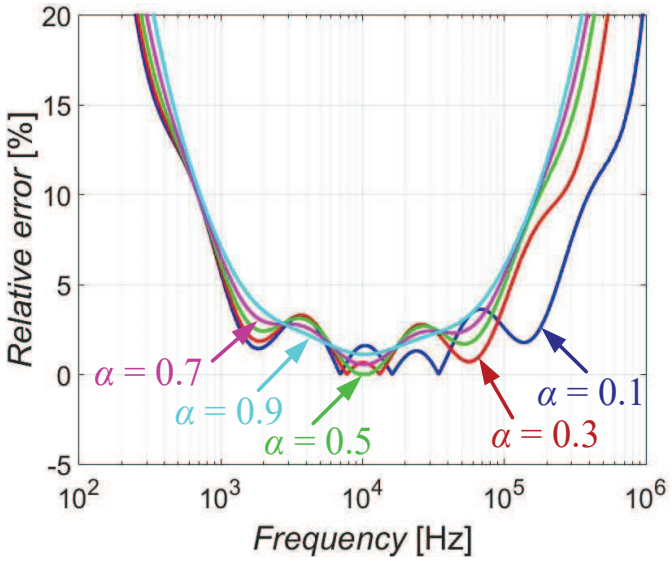


Fig. 6.17: Relative error of the phase characteristics obtained from simulation compared to the theoretical phase shift of given order

TABLE XXXVIII. COMPARISON OF OPERATIONAL BANDWIDTHS FOR USED ORDERS WHERE THE RELATIVE ERROR IS UNDER 10% IN CASE OF SIMULATION RESULTS

α [–]	f_{min} [Hz]	f_{max} [kHz]	Bandwidth
0.1	684	394	> 2 decades
0.3	684	254	> 2 decades
0.5	684	176	> 2 decades
0.7	692	170	> 2 decades
0.9	716	166	> 2 decades

As mentioned earlier, the presence of OTAs in the individual branches of the proposed circuits offers a possibility of the electronic control of the gain adjustment by changing the values of the transconductances. This ability has been tested for five different settings of the transconductance when the order of the integrator is set to 0.5. The values of the transconductance are selected as 0.7 mS, 0.6 mS, 0.5 mS, 0.4 mS and 0.3 mS (corresponding with the control voltages of 0.36 V, 0.31 V, 0.26 V, 0.21 V and 0.15 V). The comparison of simulation results and the theoretical expectations are depicted in Fig. 6.18. The results show that the gain of the integrator can be adjusted electronically while the order stays unchanged as observed in phase characteristics (practically identical).

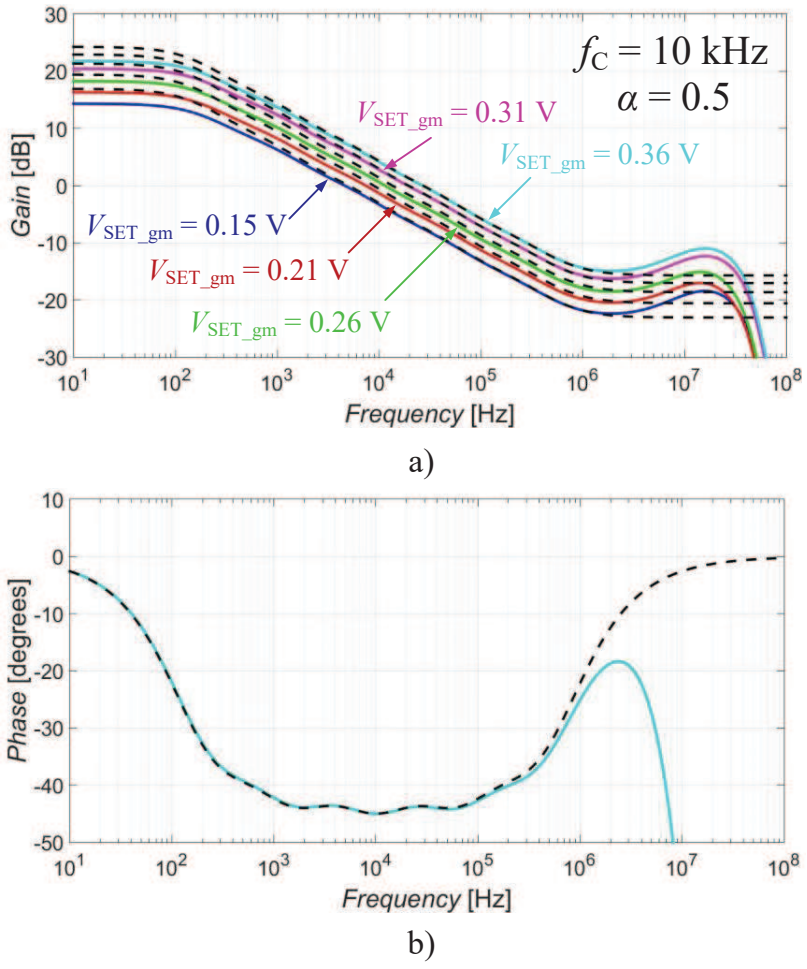


Fig. 6.18: Demonstration of the electronic control of the gain adjustment of the proposed integrator for order 0.5: theoretical expectations (black dashed lines), simulation results (colored lines)

Figure 6.19 compares the simulation results (black dashed lines) and experimental measurements (colored lines) of the magnitude and phase characteristics for used orders. The experimental results further support the design. The integrator for order 0.9 already did not work properly in experiments due to the mutual interaction of the impedance of the RC structure and real/parasitic characteristics of the output impedances of used active elements. Therefore, the experimental results of order 0.9 are not included as they do not provide any useful contribution. This issue could be solved by the recalculation of the RC FOE approximant with different values of pseudo capacitors (C_α) resulting in more favorable values of resistors of RC segments.

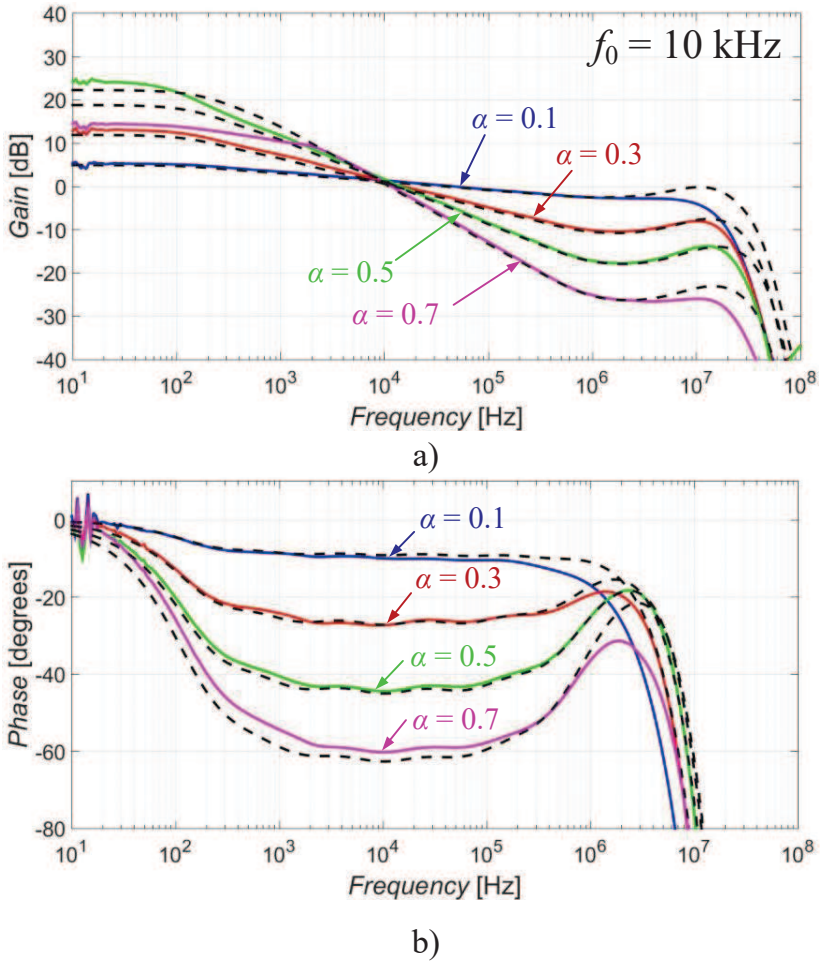


Fig. 6.19: Magnitude (a)) and phase (b)) characteristics of the proposed integrator for used orders (0.1, 0.3, 0.5, 0.7 and 0.9): simulation results (black dashed lines), experimental measurements (colored lines)

A relative error of the phase characteristics obtained from the experimental measurements compared to the theoretical value of phase shift for given order (-9˚, -27˚, -45˚ and -63˚ for orders 0.1, 0.3, 0.5, and 0.7) is depicted in Fig. 6.20. The error is not presented in Fig. 6.20 and in Tab. XXXIX for order 0.9, where the information about usable bandwidth is given. Comparing the bandwidths obtained from the simulations and experimental measurements, the implemented integrator exhibits narrower bandwidths as the effect of real/parasitic impedances (typically more significant in case of the measurement).

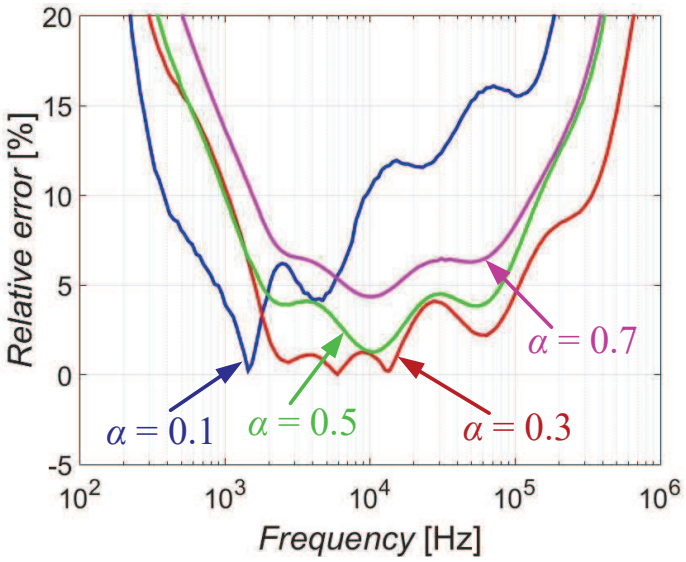


Fig. 6.20: Relative error of the phase characteristics obtained from the experimental measurements compared to the theoretical phase shift of given order

TABLE XXXIX. COMPARISON OF OPERATIONAL BANDWIDTHS FOR USED ORDERS WHERE THE RELATIVE ERROR IS UNDER 10% IN CASE OF EXPERIMENTAL MEASUREMENTS

α [–]	f_{min} [Hz]	f_{max} [kHz]	Bandwidth
0.1	369	9.5	< 2 decades
0.3	1070	330	> 2 decades
0.5	1000	144	> 2 decades
0.7	1530	128	< 2 decades

The demonstration of the electronic control of the gain adjustment (when α is set to 0.5) is shown in Fig. 6.21. The control voltages for selected values of transconductances (0.7 mS, 0.6 mS, 0.5 mS, 0.4 mS and 0.3 mS), in case of the experimental measurements, are 0.54 V, 0.46 V, 0.39 V, 0.31 V and 0.23 V.

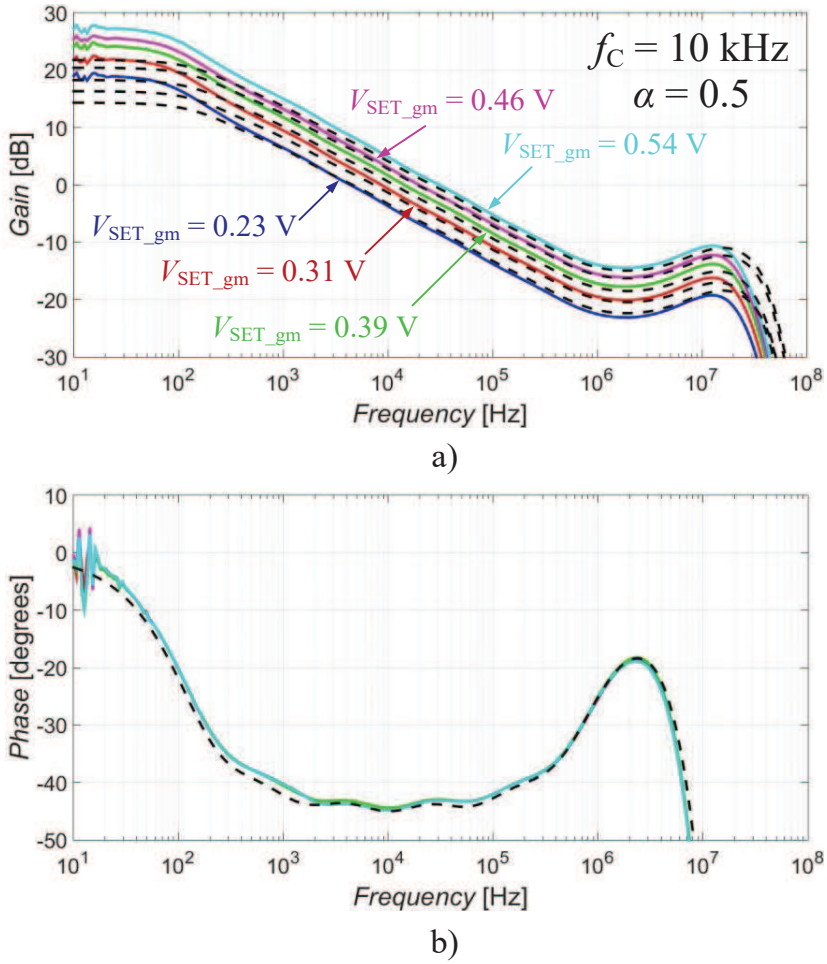


Fig. 6.21: Demonstration of the electronic control of the gain adjustment of the proposed integrator for order 0.5: simulation results (black dashed lines), experimental measurements (colored lines)

Application example

The integrator (Fig. 6.14) has been implemented into a structure of a frequency filter (designed for this purpose) in order to provide fractional–order transfer characteristics. A prototype structure is a simple current–mode second–order low–pass filter based on FLF topology (shown in Fig. 6.22). It consists of one CF, two OTAs and two grounded capacitors. The transfer function for this topology is given as:

$$K(s) = \frac{I_{OUT}}{I_{IN}} = \frac{g_{m1}g_{m2}}{s^2C_1C_2 + sC_2g_{m1} + g_{m1}g_{m2}}. \tag{6.12}$$

The OTA_2 and C_2 were replaced by the proposed CM FO integrator as shown in Fig 6.23. Thus, the modified topology behaves as a $1+\alpha$ low–pass filter. Then the transfer function from (6.12) turns into:

$$K(s) = \frac{I_{OUT}}{I_{IN}} = \frac{g_{m1}g_{m2}}{s^{1+\alpha}C_1C_{2\alpha} + s^{\alpha}C_{2\alpha}g_{m1} + g_{m1}g_{m2}}. \tag{6.13}$$

As the proposed integrator offers only one output, the additional required outputs were obtained by adding a CCCII operating as a CF at the output of the integrator.

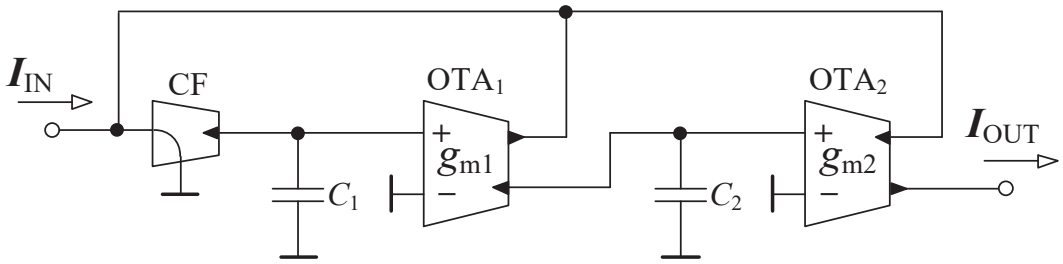


Fig. 6.22: Topology of a CM second–order low–pass FLF filter (prototype) used for demonstrational purposes

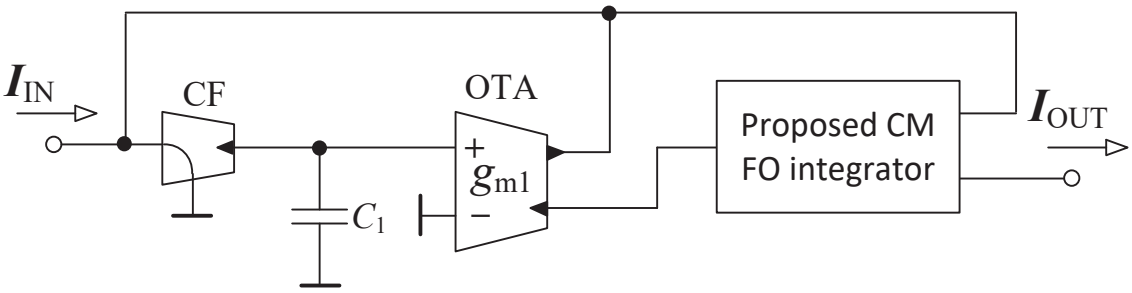


Fig. 6.23: Modified filter from Fig. 6.22 with the proposed CM FO integrator behaving as a 1+α low–pass filter

For the filter having Butterworth characteristics (for FO form), coefficients k are derived from general FO low–pass function as:

$$K_{1+\alpha}^{LP}(s) = \frac{k_1}{s^{\alpha}(s+k_2)+k_3}, \tag{6.14}$$

where $k_1 = 1$, $k_2 = 1.008\alpha^2+0.2867\alpha+0.2366$ and $k_3 = 0.2171\alpha + 0.7914$.

The operation has been tested by cadence simulations and compared to the theoretical expectations. The value of C_1 has been set to 10 nF. The values of transconductances g_{m1} of the filter and g_{m2} (substituted by the transconductance of the integrator) have to be calculated by comparing (6.13) and (6.14) in respect to coefficients k depending on the value of α and chosen pole frequency f_0 equal to 5 kHz. The values of transconductances, valid for several values of α, are stated in Tab. XL. The transfer characteristics (magnitude and phase) of the filter are presented in Fig. 6.24 (for orders 0.1, 0,3, 0,5, 0,7 and 0.9), where black dashed lines stand for the theoretical results and colored lines represent the simulation results.

TABLE XL. VALUES OF TRANSCONDUCTANCES IN RELATION TO SELECTED VALUE OF ALPHA

α [–]	**0.1**	**0.3**	**0.5**	**0.7**	**0.9**
g_{m1} **[mS]**	0.09	0.13	0.2	0.29	0.41
g_{m2} **[mS]**	0.63	0.44	0.3	0.22	0.16

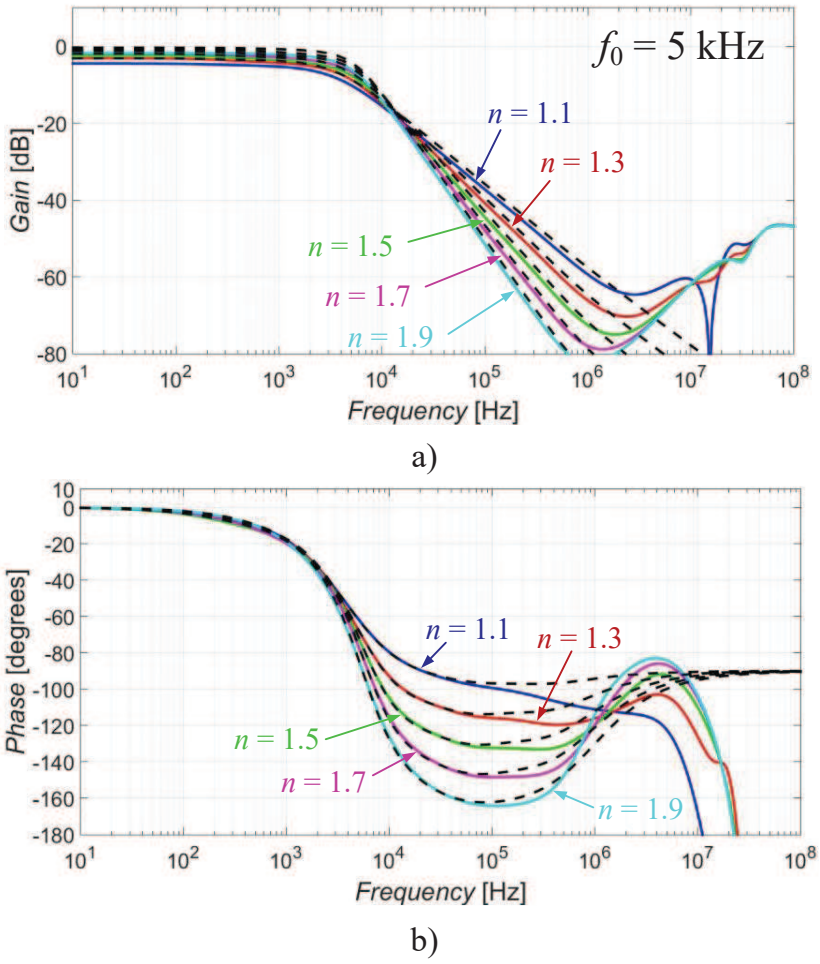
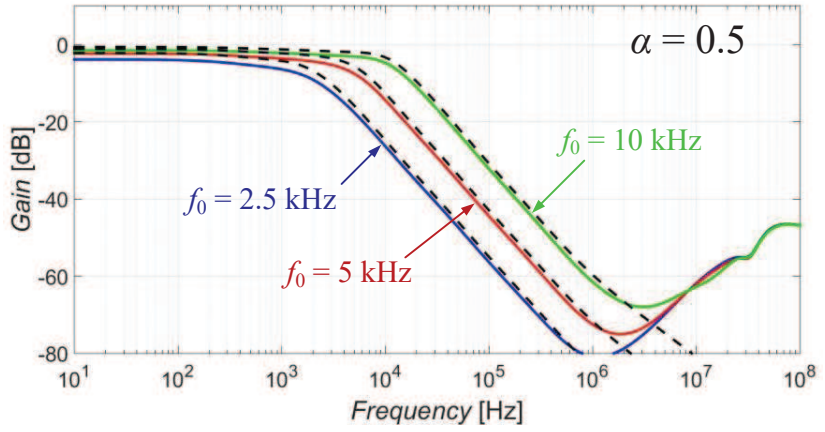


Fig. 6.24: Magnitude (a)) and phase (b)) characteristics of the 1+α filter for used orders (0.1, 0.3, 0.5, 0.7 and 0.9): theoretical expectations (black dashed lines), simulation results (colored lines)

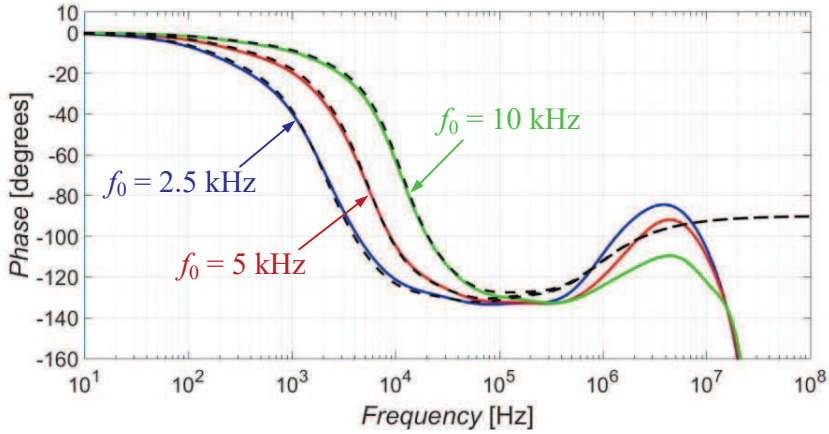
The ability of the electronic adjustment of the gain (time constant) adjustment of the proposed integrator can be useful for tuning of the pole frequency of the filter. The pole frequency depends on transconductance g_{mi} of the integrator (substituting g_{m2} of the filter) together with transconductance g_{m1} of the filter. This feature was tested for three settings (specified in Tab. XLI). The results are shown in Fig 5.25 for theoretical expectations (black dashed lines) and simulations (colored lines) when the order of the filter was set to 1.5 ($\alpha = 0.5$). The order of the output responses remains unaffected when the pole frequency is tuned.

TABLE XLI. VALUES OF TRANSCONDUCTANCES FOR TESTED POLE FREQUENCIES

Theoretical f_0 [kHz]	**2.5**	**5**	**10**
g_{m1} [mS]	0.1	0.2	0.4
g_{m2} [mS]	0.15	0.3	0.6



a)



b)

Fig. 6.25: Illustration of the electronic adjustment of the pole frequency of the filter when the order is 1.5

Note that the designs (FO integrators/differentiators) based on the RC approximant [81–83] typically are not able to perform the electronic adjustment of the resulting fractional order. The RC components have to be replaced in order to provide a different fractional order which is the most significant disadvantage of this approach. On the other hand, the circuits [84–87], based on the approximation of fractional Laplace operator, standardly utilize the electronic adjustment of the order (and other parameters in specific cases). The disadvantage of topologies based on this approach consists in the usually very complex resulting topology and control/adjustment. Quite extensive sets of specific and very precise values of the control voltages/currents are required for the accurate approximation (single parameter control or ratios between several parameters are impossible). In addition, specific values of the

control voltages/currents are difficult to obtain in some cases (e.g., very low/high values of control voltages in hundredths and thousandths of volts for α closing zero or one). The driving values of units of milli–volts or units of micro–amperes may lead to a significant inaccuracy of the FO approximation due to inaccuracy of active elements and their real behavior.

7 Conclusion

The main focus of the thesis was to propose new solutions of reconnection-less reconfigurable filters. Two other thesis goals targeted on the design of fractional–order circuits (mainly due to my involvement in the project dealing with fractional–order circuits) and the research and development in the field of modern active elements and building blocks. The proposed circuits are supported by PSpice simulations (OrCAD 16.6) or the simulations in Cadence IC6 (spectre simulator, I3T25 0.35 μm 3.3 V ON Semiconductor CMOS process) utilizing available simulation models of used active elements and developed structures and cells. Some of these solutions are complemented with an additional analysis (sensitivity analysis, stability analysis, relative error calculation). Selected solutions were also subjects of experimental tests with available fabricated ICs for further verification and support of applicability. The first chapter provides the background of the areas solved in this thesis. The second chapter outlines the main goals of the thesis. Chapter 3 gives the description of basic and standard active elements used in the design of the proposed circuits and advanced variants of active elements. The following chapter consists of the description of the general idea of the reconnection–less (switchless) reconfiguration and offers methodological steps for the design of reconnection–less reconfigurable filters by several methods of synthesis used in this thesis. Chapter 5 creates the main part of this work. This part deals with proposed solutions of reconnection–less reconfigurable filters. The proposed advanced active elements and building blocks with enhanced controllability, suitable (and used) for the synthesis and design of reconnection–less reconfigurable filters (as their important parts), are presented in chapter 6.

The main chapter contains solutions of the reconnection-less reconfigurable filters. Besides the ability of the reconnection–less reconfiguration, the proposed filters usually offer the feature of the electronic adjustment of the pole frequency and the quality factor, possibility to adjust the pass–band/stop–band area and also provide responses with fractional–order characteristics as tested in some cases. The chapter is divided into five subchapters based on the approach used for the design. The chapter offers nine solutions in total (two structures in each subchapter except for the SFG design). The filter from subsection 5.1.1 offers HP, BS, and AP functions of the 2^{nd}–order and HP transfer function of the 1^{st}–order and direct transfer. The filter was also modified in order to provide fractional order characteristics. The second topology (subsection 5.1.2) exhibits transfer functions of AP, BS, LP, LPZ (2^{nd}–order) and HP function of the 1^{st}–order and DT. All standard 2^{nd}–order transfer functions plus HPZ and LPZ are offered in case of the first filter of section 5.2. The second filter (of section 5.2) provides all standard 2^{nd}–order transfer functions and also functions of DT and HPZ. A further modification of this filter consists in the replacement of the implementation of one active element of the original structure by the addition of the electronic adjustment of the pole frequency and quality factor of the filter. AP, BP, BS, HP, LP, and 1st–order HP functions are available in case of the filter presented in subsection 5.3.1. Moreover,

the filter also provides functions of HPZ and LPZ. The employment of CG–CCDDCCs, (allowing control of each output separately) which makes the reconnection–less reconfiguration possible even with a decreased number of active elements within the structure, gives certain advantage. The filter was also tested as a FO solution. The CM proposal in subsection 5.3.2 offers all standard 2^{nd}–order functions together with HPZ, LPZ, DT and high–pass function of the 1^{st}–order. The solution described in subsection 5.4.1 works in the current mode, voltage mode, and mixed mode (transformation of voltage to current) and generates sixteen reconfigurable transfer functions in total. The proposal from subsection 5.5.1 generates 13 transfer functions of different types and orders. The last presented filter has been specifically designed to be the LP filter of various orders (including fractional orders). This structure has enhanced/extended degree of freedom considering it can offer up to 4 independently adjustable fractional orders. More detailed comparison of proposed filters has been made in section 5.6 (see Tab. XXX and accompanying text).

Newly proposed active elements and analogue building blocks were introduced in chapter 6. Proposed circuits were specifically designed to be suitable for the design of reconnection–less reconfigurable structures. The first design consists of several solutions of a current follower/amplifier with adjustable intrinsic resistance. Fully–differential solutions are also introduced for special cases of the fully–differential circuit synthesis. The adjustment of the intrinsic resistance provides an additional degree of freedom for future applications. A specific solution under designation IOGC-CA has been used for the design of reconfigurable filters in subsections 5.2.2, 5.5.1 and 5.5.2. The first introduced building block (section 6.2) serves as a reconfigurable FO integrator with the electronic control of the order and operational bandwidth (its central frequency). This integrator can be used for the design of FO circuits offering a full electronic control of the order and the bandwidth where the FO approximation is valid. These concepts are useful in comparison to designs using RC approximants that are not electronically adjustable and each modification of the order or operational frequency requires the replacement of values of RC ladder sections. The structure can easily work as a FO differentiator too. The example of the operational bandwidth extension by using high order topology is also documented. The last proposed circuit (also a reconfigurable FO integrator) implements a different order adjustment than the previous solution. This design is based on several RC approximants, but the electronic control of the order is available. Therefore, it offers a simple electronic control of the order without the requirement of specific and accurate values of the control voltages/currents.

The research described in this work has been published in proceedings of international conferences listed in the database WoS and Scopus and international journals registered in Journal Citation Report (with an impact factor). In the frame of my Ph.D. study at the Department of Radio Electronics, I'm an author and coauthor of 49 publications. 17 of these papers were published in international journals and 32 in proceedings of international conferences. I'm the main author of 9 journal publications and 12 conference publications.

The content of this thesis is covered by 12 publications (4 journal publications and 8 conference publications). The publication in Journal of Advanced Research with five year impact factor 9.479 (AIS Q1) represents the largest success of my research.

References

[1] TRAN H. D; WANG H. Y; NGUYEN Q. M; CHIANG N. H; LIN W. C; LEE T. F. High-Q biquadratic notch filter synthesis using nodal admittance matrix expansion. International Journal of Electronics and Communications (AEÜ), 2015, Vol. 69, pp. 981–987. DOI: 10.1016/j.aeue.2015.03.001

[2] SAISING E.; PROMMEE P. Fully Tunable All-Pass Filter Using OTA and its Application. In Proc. 39th International Conference on Telecommunications and Signal Processing (TSP), 2016, Vienna, Austria, pp. 287–290. DOI: 10.1109/TSP.2016.7760880

[3] SINGH A. K.; KUMAR P.; SENANI R. Fully-differential current-mode higher order filters using all grounded passive elements. International Journal of Electronics and Communications (AEÜ), 2018, Vol. 97, pp. 102–109. DOI: 10.1016/j.aeue.2018.10.009

[4] BRANDSTETTER P.; KLEIN L. Third Order Low-Pass Filter Using Synthetic Immittance Elements with Current Conveyors. Theoretical and Applied Electrical Engineering, 2012, Vol. 10, No. 2, pp. 89–94. DOI: 10.15598/aeee.v10i2.617

[5] KUMNGERN M.; KLANGTHAN K. 0.5-V Fourth-Order Low-Pass Filter. In Proc. 2nd International Conference on Automation, Cognitive Science, Optics, Micro Electro-Mechanical System, and Information Technology (ICACOMIT), 2017, Jakarta, Indonesia, pp. 119–122. DOI: 10.1109/ICACOMIT.2017.8253398

[6] MINAEI S.; YUCE E. High-Order Current-Mode Low-Pass, High-Pass and Band-Pass Filter Responses Employing CCCIIs. In Proc. 6th International Conference on Information, Communications & Signal Processing, 2007, Singapore, Singapore, pp. 1–4. DOI: 10.1109/ICICS.2007.4449676

[7] SINGH S. V.; SHANKAR C. Fully integrated multifunction trans-impedance mode biquad filter. Journal of Engineering Science and Technology, 2018, Vol. 13, No. 1, pp. 280–294.

[8] MAUNDY B. J.; ELWAKIL A. S.; OZOGUZ S.; YILDIZ H. A. Minimal two-transistor multifunction filter design. International Journal of Circuit Theory and Applications, 2017, Vol. 45, pp. 1449–1466. DOI: 10.1002/cta.2319

[9] ZHANG P.; DENG Z. A. multifunction filter configuration based on CFA. In Proc. International Conference on Information Technology and Management Innovation (ICITMI 2015), 2015, Shenzhen, China, pp. 685–689. DOI: 10.2991/icitmi-15.2015.114

[10] RANJAN A.; PAUL S. K. Nth Order Voltage Mode Active-C Filter Employing Current Controlled Current Conveyor. Circuits and Systems, 2011, Vol. 2, No. 2, pp. 85–90. DOI: 10.4236/cs.2011.22013

[11] SOLIMAN A. M. Current mode filters using two output inverting CCII. International Journal of Circuit Theory and Applications, 2008, Vol. 36, pp. 875–881. DOI: 10.1002/cta.463

[12] CHUNHUA W.; LING Z.; TAO L. A. New OTA-C current-mode biquad filter with single input and multiple outputs. International Journal of Electronics and Communications (AEÜ), 2008, Vol. 62, No. 3. pp. 232–234. DOI: 10.1016/j.aeue.2007.03.017

[13] CHAMNANPHAI V.; SA-NGIAMVIBOOL W. Electronically Tunable SIMO Mixed-mode Universal Filter using VDTAs. PRZEGLĄD ELEKTROTECHNICZNY, 2017, Vol. 93 No. 3, pp. 207–211. DOI: 10.15199/48.2017.03.48

[14] SHANKAR C.; SINGH S. V. High input impedance trans-admittance mode biquad universal filter employing DVCCTAs and grounded passive elements. Indian Journal of Pure & Applied Physics 2019, Vol. 57, No. 1, pp. 52–62.

[15] LI Y.; WANG C.; ZHU B.; HU Z. Universal Current-Mode Filters Based on OTA and MO-CCCA. IETE Journal of Research, 2018, Vol. 64, No. 6, pp. 897–906. DOI: 10.1080/03772063.2017.1381575

[16] BIOLEK D.; BIOLKOVA V.; KOLKA Z.; BAJER J. Single-Input Multi-Output Resistorless Current-Mode Biquad. In Proc. ECCTD09 - European Conference on Circuit Theory and Design 2009, 2009, Antalya, Turkey: IEEE, pp. 225–228. DOI: 10.1109/ECCTD.2009.5274928

[17] TORTEANCHAI U.; KUMNGERN M. Single-Input Four-Output Voltage-Mode Universal Biquadratic Filter Employing Four OTAs and Two Grounded Capacitors, In Proc. 4th Int. Conference on Intelligent Syst., Modelling and Sim, 2013, Bangkok, Thailand, pp. 646–649. DOI: 10.1109/ISMS.2013.137

[18] RANA U.; SUYAL S.; ARORA T. S. Single Input Multiple Output Multifunction Filter Employing Current Differencing Buffered Amplifier. In Proc. 2016 International Conference on Computational Techniques in Information and Communication Technologies (ICCTICT), 2016, New Delhi, India, pp. 1–5. DOI: 10.1109/ICCTICT.2016.7514647

[19] KUMNGERN M. Multiple-input single-output current-mode universal filter using translinear current conveyors. Journal of Electrical and Electronics Engineering Research. 2011, Vol. 3, No. 9, pp. 162–170. DOI: 10.5897/JEEER.9000024

[20] JAIKLA W.; SIRIPONGDEE S.; SUWANJAN P. MISO current-mode biquad filter with independent control of pole frequency and quality factor. Radioengineering, 2012, Vol. 21, No. 3, pp. 886–891.

[21] TOMAR R.; SINGH S.; CHAUHAN D. Current Processing Current Tunable Universal Biquad Filter Employing Two CCTAs and Two Grounded Capacitors. Circuits and Systems, 2013, Vol. 4, No. 6, pp. 443–450. DOI: 10.4236/cs.2013.46058

[22] Yesil A.; Ozenli D.; Arslan E.; Kacar F. Electronically tunable MOSFET-only current-mode biquad filter. International Journal of Electronics and Communications (AEÜ), 2017, Vol. 81, pp. 227–235. DOI: 10.1016/j.aeue.2017.07.019

[23] CHUNHUA W.; HAIGUANG L.; YAN Z. Universal current-mode filter with multiple inputs and one output using MOCCII and MO-CCCA. International Journal of Electronics and Communications (AEÜ), 2009, Vol. 63, pp. 448–453. DOI: 10.1016/j.aeue.2008.03.004

[24] UTTAPHUT P. Simple Three-Input Single-Output Current-Mode Universal Filter Using Single VDCC. International Journal of Electrical and Computer Engineering (IJECE), 2018, Vol. 8, No. 6, pp. 4932–4940. DOI: 10.11591/ijece.v8i6.pp4932-4940

[25] PSYCHALINOS C.; KASIMIS C.; KHATEB F. Multiple-input single-output universal biquad filter using single output operational transconductance amplifiers. International Journal of Electronics and Communications (AEÜ), 2018, vol. 93, pp. 360–367. DOI: 10.1016/j.aeue.2018.06.037

[26] MONGKOLWAI P.; PUKKALANUN T.; TANGSRIRAT W. Three-Input Single-Output Current-Mode Biquadratic Filter with High-Output Impedance Using a Single Current Follower Transconductance Amplifier. IAENG International Journal of Computer Science, 2017, vol. 44, no. 3, pp. 383–387.

[27] HORNG J. W.; WU C. M.; HERENCSAR N. Three-Input-One-Output Current-Mode Universal Biquadratic Filter Using One Differential Difference Current Conveyor. Indian Journal of Pure and Applied Physics, 2014, Vol. 52, pp. 556–562. DOI: 10.1142/S021812661340001X

[28] TANGSRIRAT W.; DUMAWIPATA T.; SURAKAMPONTORN W. Multiple-input single-output current-mode multifunction filter using current differencing transconductance amplifiers. International Journal of Electronics and Communications (AEÜ), 2007, Vol. 61, Iss. 4, pp. 209–214. DOI: 10.1016/j.aeue.2006.04.004

[29] ETTAGHZOUTI T.; HASSEN N.; BESBES K. SIMO type mixed mode biquadratic filter using second generation current conveyor circuits. In Proc. 7th International Conference on Sciences of Electronics, Technologies of Information and Telecommunications (SETIT), 2016, Hammamet, Tunisia, pp. 539–543. DOI: 10.1109/SETIT.2016.7939928.

[30] CHANNUMSIN O.; TANGSRIRAT W. Dual-mode multifunction filter using VDGAs. In Proc. 15th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2018, Chiang Rai, Thailand, pp. 481–484. DOI: 10.1109/ECTICon.2018.8619955

[31] CINI U.; AKTAN M. Dual-mode OTA based biquadratic filter suitable for current-mode applications. International Journal of Electronics and Communications (AEÜ), 2017, Vol. 80, pp. 43–47. DOI: 10.1016/j.aeue.2017.06.024

[32] MAHESHWARI S.; SINGH S. V.; CHAUHAN D. S. Electronically tunable low-voltage mixed-mode universal biquad filter. IET Circuits, Devices & Systems, 2011, Vol. 5, No. 3, pp. 149–158. DOI: 10.1049/iet-cds.2010.0061

[33] LEE C. Independently tunable mixed-mode universal biquad filter with versatile input/output functions. International Journal of Electronics and Communications (AEÜ), 2016, Vol. 70, pp. 1006–1019. DOI: 10.1016/j.aeue.2016.04.006

[34] LANGHAMMER L.; JERABEK J. Fully Differential Universal Current-Mode Frequency Filters Based on Signal-Flow Graphs Method. International Journal of Advances in Telecommunications, Electrotechnics, Signals and Systems, 2014, Vol. 3, No. 1, pp. 1–12.

[35] KAÇAR F.; KUNTMAN A.; KUNTMAN H. Mixed-mode biquad filter employing single active element. In Proc. IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS), 2013, Cusco, Peru, pp. 1–4. DOI: 10.1109/LASCAS.2013.6518982

[36] KESKIN A. Ü.; HANCIOGLU E. Current mode multifunction filter using two CDBAs. International Journal of Electronics and Communications (AEÜ), 2005, Vol. 59, No. 8, pp. 495–498. DOI: 10.1016/j.aeue.2005.01.003

[37] LEE T.; LEE B.; NAM S.; KIM Y.; LEE J. Frequency-Tunable Tri-Function Filter. IEEE Transactions on Microwave Theory and Techniques, 2017, Vol. 65, No. 11, pp. 4584–4592. DOI: 10.1109/TMTT.2017.2716931

[38] ADOUM B. A.; WEN W. P. Investigation of band-stop to all pass reconfigurable filter. In Proc. 4th International Conference on Intelligent and Advanced Systems (ICIAS), 2012, Kuala Lumpur, Malaysia, pp. 190–193. DOI: 10.1109/ICIAS.2012.6306185

[39] NAGLICH E. J.; LEE J.; PEROULIS D.; CHAPPEL W. J. Switchless tunable bandstop-to-all-pass reconfigurable filter. IEEE Transaction on Microwave Theory and Techniques, 2012, Vol. 60, No. 5, pp. 1258–1265. DOI: 10.1109/TMTT.2012.2188723

[40] FAN M.; SONG K.; ZHU Y.; FAN Y. Compact Bandpass-to-Bandstop Reconfigurable Filter With Wide Tuning Range. IEEE Microwave and Wireless Components Letters, 2019, Vol. 29, No. 3, pp. 198–200. DOI: 10.1109/LMWC.2019.2892846

[41] LABABIDI R.; SHAMI M. A.; ROY M. L.; JEUNE D. L.; KHODER K.; PÉRENNEC A. Tunable Channelized Bandstop Passive Filter Using Reconfigurable Phase Shifter. IET Microwaves Antennasand Propagation, Institution of Engineering and Technology, 2019, Vol. 13, No. 5, pp.591–596. DOI: 10.1049/iet-map.2018.5430

[42] SOTNER R.; HERENCSAR N.; JERABEK J.; PROKOP R.; KARTCI A.; DOSTAL T.; VRBA, K. Z-Copy Controlled-Gain Voltage Differencing Current Conveyor: Advanced Possibilities in Direct Electronic Control of First-Order Filter. Elektronika Ir Elektrotechnika, 2014, Vol. 20, No. 6, pp. 77–83. DOI: 10.5755/j01.eee.20.6.7272

[43] SOTNER R.; PETRZELA J.; JERABEK J.; DOSTAL T. Reconnection-less OTA-based Biquad Filter with Electronically Reconfigurable Transfers. Elektronika Ir Elektrotechnika, 2015, Vol. 21, No. 3, pp. 33–37. DOI: 10.5755/j01.eee.21.3.10205

[44] SOTNER R.; JERABEK J.; HERENCSAR N.; PROKOP R.; VRBA K.; DOSTAL T. Resistor-less First-Order Filter Design with Electronical Reconfiguration of its Transfer Function. In Proc. 24th International Conference Radioelektronika, 2014, Bratislava, Slovakia, pp. 63–66. DOI: 10.1109/Radioelek.2014.6828417

[45] PETRZELA J.; SOTNER R. Systematic design procedure towards reconfigurable first-order filters. In Proc. 24th International Conference radioelektronika, 2014, Bratislava, Slovakia, pp. 1–4. DOI: 10.1109/Radioelek.2014.6828462

[46] SOTNER R.; PETRZELA J.; JERABEK J.; VRBA K.; DOSTAL T. Solutions of Reconnection-less OTA-based Biquads with Electronical Transfer Response Reconfiguration. In Proc. 25th International Conference Radioelektronika, 2015, Pardubice Czech Republic, pp. 40–45. DOI: 10.1109/RADIOELEK.2015.7128991

[47] SOTNER R.; JERABEK J.; SEVCIK B.; DOSTAL T.; VRBA K. Novel solution of notch/all-pass filter with special electronic adjusting of attenuation in the stop band. Elektronika ir Elektrotechnika, 2011, Vol. 17, No. 7, pp. 37–42. DOI: 10.5755/j01.eee.113.7.609

[48] JERABEK J.; SOTNER R.; POLAK J.; VRBA K.; DOSTAL T. Reconnection-less electronically reconfigurable filter with adjustable gain using voltage differencing current conveyor. Elektronika ir Elektrotechnika, 2016, Vol. 22, No. 6, pp. 39–45. DOI: 10.5755/j01.eie.22.6.17221

[49] SOTNER R.; LANGHAMMER L.; DOMANSKY O.; PETRZELA J.; JERABEK J.; DOSTAL T. New Reconfigurable Universal SISO Biquad Filter Implemented by Advanced CMOS Active Elements. In Proc. 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2018, Prague, Czech Republic: IEEE, pp. 257–260. DOI: 10.1109/SMACD.2018.8434560

[50] SOTNER R.; JERABEK J.; PETRZELA J.; LANGHAMMER L.; DOMANSKY O.; JAIKLA W.; DOSTAL T. Reconnection-less Reconfigurable Filter and its Application into Adaptive Circuit. In Proc. 41st International Conference on Telecommunications and Signal Processing (TSP), 2018, Athens, Greece: IEEE, pp. 192–197. DOI: 10.1109/TSP.2018.8441388

[51] TSIRIMOKOU G.; SOTNER R.; JERABEK J.; KOTON J.; PSYCHALINOS C. Programmable analog array of fractional-order filters with CFOAs. In Proc 40th international conference on telecommunications and signal processing (TSP), 2017, Barcelona, Spain. pp. 706–9. DOI: 10.1109/TSP.2017.8076079

[52] BERTSIAS P.; KHATEB F.; KUBANEK D.; KHANDAY F. A. PSYCHALINOS C. Capacitorless digitally programmable fractional-order filters. International Journal of Electronics and Communications (AEÜ) 2017, Vol. 78, pp. 228–237. DOI: 10.1016/j.aeue.2017.04.030

[53] TSIRIMOKOU G.; PSYCHALINOS C.; ELWAKIL A. S. Digitally Programmed Fractional-Order Chebyshev Filters Realizations Using Current-Mirrors. In Proc. IEEE International Symposium on Circuits and Systems (ISCAS), 2015, Lisbon, Portugal, pp. 2337–2340. DOI: 10.1109/ISCAS.2015.7169152

[54] ELWAKIL A. S. Fractional-order circuits and systems: An emerging interdisciplinary research area. IEEE Circuits and Systems Magazine, 2010, Vol. 10, pp. 40–50. DOI: 10.1109/MCAS.2010.938637

[55] DAS S.; MAHARATNA K. Fractional dynamical model for the generation of ECG like signals from filtered coupled Van-der Pol oscillators. Computer Methods and Programs in Biomedicine, 2013, Vol. 112, No. 3, pp. 490–507. DOI: 10.1016/j.cmpb.2013.08.012

[56] SANTIS D. V.; MARTYNYUK V.; LAMPASI A. Fractional-order circuit models of the human body impedance for compliance tests against contact currents. International Journal of Electronics and Communications (AEÜ), 2017, Vol. 78, pp. 238–244. DOI: 10.1016/j.aeue.2017.04.035

[57] FREEBORN T.; MAUNDY B.; ELWAKIL A. S. Extracting the parameters of the doubledispersion Cole bioimpedance model from magnitude response measurements. Medical & Biological Engineering & Computing, 2014, Vol. 52, No. 9, pp. 749–58. DOI: 10.1007/s11517-014-1175-5

[58] ABUAISHA T.; KERTZSCHER J. Fractional-order modelling and parameter identification of electrical coils. Fractional Calculus and Applied Analysis, 2019, Vol. 22, No. 1, pp. 193–216. DOI: 10.1515/fca-2019-0013

[59] FREEBORN T. J.; ELWAKIL A. S.; MAUNDY B., Variability of Cole-model bioimpedance parameters using magnitude-only measurements of apples from a two-electrode configuration. International Journal of Food Properties, 2017, Vol. 20, No.1, pp. 507–519. DOI: 10.1080/10942912.2017.1300810

[60] FLORES C., MUÑOZ J., MONJE C. A., MILANÉS V., LU X. Iso-damping fractional-order control for robust automated car-following. Journal of Advanced Research, 2020, Vol. 25, pp. 181–189. DOI: 10.1016/j.jare.2020.05.013

[61] FREEBORN T. J.; MAUNDY B.; ELWAKIL A. S. Field programmable analogue array implementation of fractional step filters. IET Circuits Devices, 2010, Vol. 4, No. 6, pp. 514–524. DOI: 10.1049/iet-cds.2010.0141

[62] MAUNDY B.; ELWAKIL A. S.; FREEBORN T. J. On the practical realization of higher-order filters with fractional stepping. Signal Processing, 2011, Vol. 91, No. 3, pp. 484–491. DOI: 10.1016/j.sigpro.2010.06.018

[63] KUBANEK D.; FREEBORN T. (1+α) Fractional-order transfer functions to approximate low-pass magnitude responses with arbitrary quality factor. International Journal of Electronics and Communications (AEÜ), 2017, Vol. 78, pp. 1–10. DOI: 10.1016/j.aeue.2017.04.031

[64] VERMA R.; PANDEY N.; PANDEY R. CFOA based low pass and high pass fractional step filter realizations. International Journal of Electronics and Communications (AEÜ), 2019, Vol. 99, pp. 161–176. DOI: 10.1016/j.aeue.2018.11.032

[65] FREEBORN T. J.; MAUNDY B.; ELWAKIL A. S. Approximated Fractional Order Chebyshev Lowpass Filters. Mathematical Problems in Engineering, 2015, Vol. 2015, pp. 1–7. DOI: 10.1155/2015/832468

[66] SAID L. A.; ISMAIL S. M.; RADWAN A. G.; MADIAN A. H.; ABU EL-YAZEED M. F.; SOLIMAN A. M. On the optimization of fractional order low-pass filters. Circuits, Systems, and Signal Processing, 2016, Vol. 35, No. 6, pp. 2017–2039. DOI: 10.1007/s00034-016-0258-y

[67] MISHRA S. K.; GUPTA M.; UPADHYAY D. K. Active realization of fractional order Butterworth lowpass filter using DVCC. Journal of King Saud University - Engineering Sciences, 2020, Vol. 32, No. 2, pp. 158–65. DOI: 10.1016/j.jksues.2018.11.005

[68] VERMA R.; PANDEY N.; PANDEY R. Electronically tunable fractional order filter. Arabian Journal for Science and Engineering, 2017, Vol. 42, pp. 3409–22.

[69] FREEBORN T. J.; MAUNDY B.; ELWAKIL A. S. Fractional-step Tow-Thomas biquad filters. Nonlinear Theory and Its Applications IEICE, 2012, Vol. 3, No. 3, pp. 357–374. DOI: 10.1587/nolta.3.357

[70] HASSANEIN A. M.; SOLTAN A.; SAID L. A.; MADIAN A. H.; RADWAN A. G. Analysis and design of fractional-order low-pass filter with three elements of independent orders. In: Proc. 2019 novel intelligent and leading emerging sciences conference (NILES), 2019, Giza, Egypt. pp. 218–21. DOI: 10.1109/NILES.2019.8909312

[71] FOUDA M. E.; SOLTAN A.; RADWAN A. G.; SOLIMAN A. M. Fractional order multi-phase oscillators design and analysis suitable for higher order PSK applications. Analog Integrated Circuits and Signal Processing, 2016 Vol. 87, No. 2, pp. 301–312. DOI: 10.1007/s10470-016-0716-2

[72] SAID L. A.; ELWY O.; MADIAN A. H.; RADWAN A. G.; SOLIMAN A. M. Stability analysis of fractional-order Colpitts oscillators. Analog Integrated Circuits and Signal Processing, 2019, Vol. 101, pp. 267–279. DOI: 10.1007/s10470-019-01501-2

[73] SAID L. A.; RADWAN A. G.; MADIAN A. H.; SOLIMAN A. M. Two-port two impedances fractional order oscillators. Microelectronics Journal, 2016, Vol. 55, pp. 40–52. DOI: 10.1016/j.mejo.2016.06.003

[74] ELWAKIL A. S.; AGAMBAYEV A.; ALLAGUI A.; SALAMA K. N. Experimental demonstration of fractional-order oscillators of orders 2.6 and 2.7. Chaos, Solitons and Fractals, 2017, Vol. 96, pp. 160–164. DOI: 10.1016/j.chaos.2017.01.017

[75] TSIRIMOKOU G.; PSYCHALINOS C.; ELWAKIL A. S.; MAUNDY B. J. Analysis and Experimental Verification of a Fractional-Order Hartley Oscillator. In Proc. 2017 European Conference on Circuit Theory and Design (ECCTD), 2017, Catania, Italy, pp. 1–4. DOI: 10.1109/ECCTD.2017.8093312

[76] KAPOULEA S.; PSYCHALINOS C.; ELWAKIL A. S.; RADWAN A. G. One-terminal electronically controlled fractional-order capacitor and inductor emulator. International Journal of Electronics and Communications (AEÜ), 2019, Vol. 103, pp. 32–45. DOI: 10.1016/j.aeue.2019.03.002

[77] DVORAK J.; KUBANEK D.; HERENCSAR N.; KARTCI A.; BERTSIAS P. Electronically adjustable emulator of the fractional-order capacitor. Elektronika Ir Elektrotechnika, 2019, Vol. 25, No. 6, pp. 28–34. DOI: 10.5755/j01.eie.25.6.24823

[78] KUBANEK D.; KOTON J.; DVORAK J.; HERENCSAR N.; SOTNER R. Optimized Design of OTA-Based Gyrator Realizing Fractional-Order Inductance Simulator: A Comprehensive Analysis. Applied Sciences, 2021, Vol. 11, No. 1, pp. 1–19. DOI: 10.3390/app11010291

[79] ADHIKARY A.; CHOUDHARY S.; SEN S. Optimal Design for Realizing a Grounded Fractional Order Inductor Using GIC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, Vol. 65, No. 8, pp. 2411–2421. DOI: 10.1109/TCSI.2017.2787464

[80] JIN L.; LI X.; WU M. Realization of Fractional Order Integrator by Rational Function in the Form of Continued Product. In Proc. IEEE International Conference on Mechatronics and Automation (ICMA), 2015, Beijing, China, pp. 1630–1635. DOI: 10.1109/ICMA.2015.7237729

[81] GOYAL D.; VARSHNEY P. Analog Realization of Electronically Tunable Fractional-Order Differ-Integrators. Arabian Journal for Science and Engineering, 2019, Vol. 44, pp. 1933–1948. DOI: 10.1007/s13369-018-3209-z

[82] SOTNER R.; JERABEK J.; LANGHAMMER L.; KOTON J.; POLAK J.; ANDRIUKAITIS D.; VALINEVICIUS A. Design of Building Blocks for Fractional-Order Applications with Single and Compact Active Device. In Proc. 43rd International Conference on Telecommunications and Signal Processing (TSP), 2020, Milan, Italy, pp. 573–577. DOI: 10.1109/TSP49548.2020.9163400

[83] SOTNER R.; DOMANSKY O.; JERABEK J.; HERENCSAR N.; PETRZELA J.; ANDRIUKAITIS D. Integer-and Fractional-Order Integral and Derivative Two-Port Summations: Practical Design Considerations. Applied Sciences, 2020, Vol. 10, No. 1, pp. 1–25. DOI: 10.3390/app10010054

[84] DAR M. R.; KANT N. A.; KHANDAY F. A. Realization of fractional-order double-scroll chaotic system using operational transconductance amplifier (OTA). Journal of Circuits, Systems and Computers, 2018, Vol. 27, No. 1, pp. 1–15. DOI: 10.1142/S0218126618500068

[85] TSIRIMOKOU G.; PSYCHALINOS C.; FREEBORN T. J.; ELWAKIL A. S. Emulation of current excited fractional-order capacitors and inductors using OTA topologies. Microelectronics Journal, 2016, Vol. 55, pp. 70–81. DOI: 10.1016/j.mejo.2016.06.008

[86] TSIRIMOKOU G.; PSYCHALINOS C.; ELWAKIL A. S. Emulation of a constant phase element using operational transconductance amplifiers. Analog integrated Circuits and Signal Processing, 2015, Vol. 85, No. 3, pp. 413–423. 10.1007/s10470-015-0626-8

[87] BERTSIAS P.; PSYCHALINOS C.; ELWAKIL A. S.; SAFARI L.; MINAEI S. Design and application examples of CMOS fractional-order differentiators and integrators. Microelectronics Journal, 2019, Vol. 83, pp. 155–167. DOI: 10.1016/j.mejo.2018.11.013

[88] TSIRIMOKOU, G. A systematic procedure for deriving RC networks of fractional-order elements emulators using MATLAB. International Journal of Electronics and Communications (AEÜ), 2017, Vol. 78, pp. 7–14. DOI: 10.1016/j.aeue.2017.05.003

[89] KRISHNA M. S.; DAS S.; BISWAS K.; GOSWAMI B. Fabrication of a Fractional Order Capacitor with Desired Specifications: A Study on Process Identification and Characterization. IEEE Transactions on Electron Devices, 2011, Vol. 58, pp. 4067–4073. DOI: 10.1109/TED.2011.2166763

[90] ALEXANDER C. L.; TRIBOLLET B.; ORAZEM M. E. Contribution of Surface Distributions to Constant-Phase-Element (CPE) Behavior:1. Influence of Roughness. Electrochimica Acta, 2015, Vol. 173, pp. 416–424. DOI: 10.1016/j.electacta.2015.05.010

[91] BISWAS K.; SEN S.; DUTTA P. K. Realization of a constant phase element and its performance study in a differentiator circuit. IEEE Trans Circ Syst—II: Express Briefs, 2006, Vol. 53, No. 9, pp. 802–6. DOI: 10.1109/TCSII.2006.879102

[92] HABA T. C.; ABLART G.; CAMPS T.; OLIVIE F. Influence of the electrical parameters on the input impedance of a fractal structure realised on silicon. Chaos Solitons Fractals, 2005, Vol. 24, No. 2, pp. 479–90. DOI: 10.1016/j.chaos.2003.12.095

[93] USHAKOV P.; SHADRIN A.; KUBANEK D.; Koton J. Passive Fractional-Order Components Based on Resistive-Capacitive Circuits with Distributed Parameters. In Proc. 39th International Conference on Telecommunications and Signal Processing (TSP), 2016, Vienna, Austria, pp. 638–642. DOI: 10.1109/TSP.2016.7760960

[94] AMAND S.; MUSIANI M.; ORAZEM M. E.; PÉBÈRE N.; TRIBOLLET B.; VIVIER V. Constant-phase-element behavior caused by inhomogeneous water uptake in anti-corrosion coatings. Electrochimica Acta, 2013, Vol. 87, pp. 693–700. DOI: 10.1016/j.electacta.2012.09.061

[95] VALSA J.; VLACH J. RC models of a constant phase element. International Journal of Circuit Theory and Applications, Vol. 41, 2013, pp. 59–67. DOI: 10.1002/cta.785

[96] SUGI M.; HIRANO Y.; MIURA Y. F.; SAITO K. Simulation of fractal immitance by analog circuits: an approach to the optimized circuits. IEICE Trans. Fundam. Electron. Commun. Comput. Sci., 1999, Vol. E82, No. 8, pp. 1627–1634.

[97] TSIRIMOKOU G.; KARTCI A.; KOTON J.; HERENCSAR N.; PSYCHALINOS C. Comparative Study of Discrete Component Realizations of Fractional-Order Capacitor and Inductor Active Emulators. Journal of Circuits, Systems, and Computers, 2018, Vol. 27, No. 11, pp. 1–26. DOI: 10.1142/S0218126618501700

[98] JERABEK J.; VRBA K. Design of Fully Differential Filters with Basic Active Elements Working in the Current Mode. Elektrorevue, 2010, Vol. 2010, No. 87, pp. 1–5.

[99] KOTON J.; HERENCSAR N.; VRBA K.; JERABEK J. Digitally Adjustable Current Amplifier and its Application in Fully Differential Current-Mode Band-Pass Filter Design. Elektrorevue, 2010, Vol. 2010, No. 90, pp. 1–6.

[100] JERABEK J.; KOTON J.; SOTNER R.; VRBA K. Comparison of Fully-Differential and Single-Ended Current-Mode Band-Pass Filters with Current Active Elements. In Proc. 7th International Conference on Electrical and Electronics Engineering – ELECO, 2011, Bursa, Turkey: EMO, pp. 100–104.

[101] KACAR F.; KUNTMAN H.; OZCAN S. New High Performance CMOS Fully Differential Current Conveyor. Electroscope Applied Electronics, 2008, Vol. 2008, No. III, pp. 1–4.

[102] ALTUN M.; KUNTMAN H. Design of a fully differential current mode operational amplifier with improved input–output impedances and its filter applications. International Journal of Electronics and Communications (AEÜ), 2008, Vol. 62, pp. 239–244. DOI: 10.1016/j.aeue.2007.03.020

[103] MAHMOUD S. A.; AWAD I. A. Fully Differential CMOS Current Feedback Operational Amplifier. Analog Integrated Circuits and Signal Processing, 2005, Vol. 43, No. 1, pp 61–69. DOI: 10.1007/s10470-005-6571-1

[104] KUBANEK D. Teoretický návrh ADSL Splitterů. Studijní zpráva pro STROM telecom, (Theoretical Design of ADSL Splitters. Report for STROM telecom) Department of Telecommunications, FEKT, Brno University of Technology, Brno, 2003. 119 pages.

[105] CHEN W. K. The Circuits and Filters Handbook, Third Edition. CRC Press: New York, 2009.

[106] BIOLEK D.; SENANI R.; BIOLKOVA V.; KOLKA Z. Active Elements for Analog Signal Processing: Classification, Review, and New Proposals. Radioengineering, 2008, Vol. 17, No. 4, pp. 15–32.

[107] FABRE A.; SAAID O.; WIEST F.; BOUCHERON C. High frequency applications based on a new current controlled conveyor. IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,1996, Vol. 43, No. 2, pp. 82–91. DOI: 10.1109/81.486430

[108] SOLIMAN E. A.; MAHMOUD S. A. New CMOS Fully Differential Current Conveyor and its Application in Realizing Sixth Order Complex Filter. IEEE International Symposium on Circuits and Systems, 2009, Taipei, Taiwan, pp. 57–60. DOI: 10.1109/ISCAS.2009.5117684

[109] JERABEK J.; SOTNER R.; KARTCI A.; HERENCSAR N.; DOSTAL T.; VRBA K, Two Behavioral Models of the Electronically Controlled Generalized Current Conveyor of the Second Generation. In Proc. 38th International Conference on Telecommunications and Signal Processing (TSP). 2015, Prague, Czech Republic, pp. 349–353. DOI: 10.1109/TSP.2015.7296282

[110] SOTNER R.; JERABEK J.; PROKOP R.; KLEDROWETZ J.; POLAK J.; FUJCIK L.; DOSTAL T. Practically Implemented electronically controlled CMOS voltage differencing current conveyor. In Proc. IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), 2016, Abu Dhabi, United Arab Emirates, pp. 667–670. DOI: 10.1109/MWSCAS.2016.7870105

[111] MARCELLIS A.; FERRI G.; GUERRINI N. C.; SCOTTI G.; STORNELLI V.; TRIFILETTI A. The VGC-CCII: a novel building block and its application to capacitance multiplication. Analog Integrated Circuits and Signal Processing, 2009, Vol. 58, No. 1, pp. 55–59. DOI: 10.1007/s10470-008-9213-6

[112] PROMMEE P.; SOMDUNYAKANOK M, CMOS-based current-controlled DDCC and its applications to capacitance multiplier and universal filter. International Journal of Electronics and Communications (AEÜ), 2011, Vol. 65, pp. 1–8. DOI: 10.1016/j.aeue.2009.12.002

[113] SOTNER R.; JERABEK J.; HERENCSAR N.; DOSTAL T.; VRBA K. Additional approach to the conception of current follower and amplifier with controllable feature. In Proc. 34th International Conference on Telecommunications and Signal Processing (TSP), 2011, Budapest, Hungary, pp. 279–83. DOI: 10.1109/TSP.2011.6043726

[114] SOTNER R.; KARTCI A.; JERABEK J.; HERENCSAR N.; DOSTAL T; VRBA K. An additional approach to model current followers and amplifiers with electronically controllable parameters from commercially available ICs. Measurement Science Review, 2012, Vol. 12, No. 6, pp. 255–265. DOI: 10.2478/v10048-012-0035-4

[115] SOTNER R.; HERENCSAR N.; JERABEK J.; LANGHAMMER L.; POLAK J. On practical construction of electronically controllable compact current amplifier based on commercially available elements and its application. International Journal of Electronics and Communications (AEÜ), 2017, Vol. 81, No. 11/2017, pp. 56–66. DOI: 10.1016/j.aeue.2017.07.002

[116] JAIKLA W.; LAHIRI A. Resistor-less current-mode four-phase quadrature oscillator using CCCDTAs and grounded capacitors, International Journal of Electronics and Communications (AEÜ), 2012, Vol. 66, pp. 214–218. DOI: 10.1016/j.aeue.2011.07.001

[117] KUMNGERN M. Electronically tunable current-mode universal biquadratic filter using a single CCCFTA. In Proc. IEEE International Symposium on Circuits and Systems (ISCAS), 2012, Seoul, Korea, pp. 1175–1178. DOI: 10.1109/ISCAS.2012.6271443

[118] SRISAKULTIEW S.; SIRIPRUCHYANUN M.; JAIKLA W. Single-resistance-controlled current-mode quadrature sinusoidal oscillator using single CCCFTA with grounded elements. In Proc. 36th International Conference on Telecommunications and Signal Processing (TSP), 2013, Rome, Italy, pp. 436–439. DOI: 10.1109/TSP.2013.6613969

[119] SIRIPRUCHYANUN M., CHANAPROMMA C., SILAPAN P., JAIKLA W., BiCMOS Current-Controlled Current Feedback Amplifier (CC-CFA) and Its Applications. WSEAS TRANSACTIONS on ELECTRONICS, 2008, Vol. 5, No. 6, pp. 203–219.

[120] JERABEK J.; SOTNER R.; VRBA K. Electronically Adjustable Triple-Input Single-Output Filter with Voltage Differencing Transconductance Amplifier. Revue Roumaine des Sciences Techniques – Serie Électrotechnique et Énergétique, 2014, Vol. 59, No. 2, pp. 163–172.

[121] JERABEK J.; KOTON J.; SOTNER R.; VRBA K. Adjustable band-pass filter with current active elements: two fully-differential and single-ended solutions. Analog Integrated Circuits and Signal Processing, 2013, Vol. 74, No. 1, pp. 129–139. DOI: 10.1007/s10470-012-9942-4

[122] UCC-N1B – Universal Current Conveyor (UCC) and Second-Generation Current Conveyor (CCII+/-) (datasheet). Czech Republic: Brno University of Technology; 2010 accessible on http://www.utko.feec.vutbr.cz/~koton/soubory/UCC_N1B_Rev0.pdf

[123] SPONAR R.; VRBA K. Measurements and behavioral modelling of modern conveyors. International Journal of Computer Science and Network Security, 2006, Vol. 3A, No. 6, pp. 57–63.

[124] ON Semiconductor. I3T Process Technology, available online on: http://www.europracticeic.com/technologies_AMIS_tech.php

[125] SOTNER R.; JERABEK J.; POLAK J.; PROKOP R.; KLEDROWETZ V. Integrated Building Cells for a Simple Modular Design of Electronic Circuits with Reduced External Complexity: Performance, Active Element Assembly, and an Application Example. Electronics, 2019, Vol. 8, No. 5, pp. 1–26. DOI: 10.3390/electronics8050568

[126] JERABEK J.; SOTNER R.; VRBA K. Tunable universal filter with current follower and transconductance amplifiers and study of parasitic influences. Journal of Electrical Engineering, 2011, Vol. 62, No. 6, pp. 317–326. DOI: 10.2478/v10187-011-0051-x

[127] Linear Technology, LT1228 Current Feedback Amplifier with DC Gain Control (datasheet), available online on: http://cds.linear.com/docs/en/datasheet/1228fd.pdf

[128] Intersil (Elantec), EL4083 CN Current-mode multiplier (datasheet), 1996, available online on: http://jp.intersil.com/content/dam/Intersil/documents/el40/el4083.pdf

[129] JERABEK J.; VRBA K. Comparison of the Fully-Differential and Single-Ended Solutions of the Frequency Filter with Current Followers and Adjustable Current Amplifier. In Proc. ICN 2012: The Eleventh International Conference on Networks, 2012, Reunion, France, pp. 50–54.

[130] Intersil (Elantec), EL2082 CN Current-mode multiplier (datasheet), 1996, available online on: http://www.intersil.com/data/fn/fn7152.pdf

[131] Texas Instruments, VCA810 Wideband voltage controlled amplifier (datasheet), 2000, available online on: www.ti.com/lit/ds/symlink/vca810.pdf

[132] Texas Instruments, VCA822 Wideband variable gain amplifier (datasheet), 2015, available online on: http://www.ti.com/lit/ds/symlink/vca822.pdf

[133] DOSTAL, T. High-Order Filters with Multi-Loop Structure in Current Mode. Radioengineering, 2003, Vol. 12, No. 3, pp. 6–11.

[134] TOUMAZOU C.; LIDGEY F. J.; HAIGH D. G. Analogue IC design: the current-mode approach, London: Peter Peregrinus Ltd., 1990, pp. 649.

[135] MASON S. J. Feedback Theory: Some Properties of Signal Flow Graphs. In Proc. IRE, 1953, Vol 41, No. 9, pp. 1144–1156. DOI: 10.1109/JRPROC.1953.274449

[136] COATES C. L. Flow graph solutions of linear algebraic equations, In Proc. IRE, 1959, Vol. 6, No. 2, pp. 170–187. DOI: 10.1109/TCT.1959.1086537

[137] NISE, N. S. Signal-Flow Graphs, The Control Handbook, IEEE Press, 1996, 1566 pages.

[138] AYTEN U. E.; SAGBAS M.; SEDEF H. Current mode leapfrog ladder filters using a new active block, International Journal of Electronics and Communications (AEÜ), 2010, Vol. 64, Iss. 6, pp. 503 – 511. DOI: 10.1016/j.aeue.2009.03.012

[139] DELIYANNIS T.; SUN Y.; FIDLER J. K. Continuous-time active filter design. US: CRC Press; 1998, 462 pages.

[140] HAJEK, K.; SEDLACEK, J. Kmitočtové filtry (Frequency filters), BEN – technická literatura, Praha 2002, 1. edition, 536 pages.

[141] KAHLER J. Complete Filter Design with Discrete Elements Made Easy, Microwaves & RF, 2019, available online on: https://www.awr.com/articles

[142] HAJEK K.; SEDLACEK J. NAFID program as powerful tool in filter education area. In Proc. Conference CIBLIS'97, 1997, Leicester, United Kingdom, pp. PK-4 1–10.

[143] BIOLEK D.; KOLKA Z.; SVIEZENY B. Teaching of electrical circuits using symbolic and semisymbolic programs. In Proc. 11th Conference EAEEIE, 2000, Ulm, Germany, pp. 26–30.

[144] Texas Instruments, OPA860 Wide-bandwidth, operational transconductance amplifier (OTA) and buffer (datasheet), 2008, available online on: http://www.ti.com/lit/ds/symlink/opa860.pdf

[145] Texas Instruments - OPA861 - Wide Bandwidth Operational Transconductance Amplifier (datasheet). available online on: http://www.ti.com/lit/ds/symlink/opa861.pdf

[146] SOTNER R.; SLEZAK J.; DOSTAL T. Influence of Mirroring of Current Output Responses through Grounded Passive Elements, In Proc. 20th International Conference radioelektronika, 2010, Brno, Czech Republic, pp. 177-180. DOI: 10.1109/RADIOELEK.2010.5478562

[147] RADWAN A. G.; SOLIMAN A. M.; ELWAKIL A. S.; SEDEEK A. On the stability of linear systems with fractional-order elements. Chaos Solitons Fractals, 2009, Vol. 40, No. 5, pp. 2317–28. DOI: 10.1016/j.chaos.2007.10.033

[148] PETRÁŠ I. Stability of fractional-order systems with rational orders: a survey. Fractional Calculus Applied Analysis, 2009, Vol. 12, No. 3, pp. 269–98.

Own papers relevant to the content of the thesis

[149] LANGHAMMER L.; SOTNER R.; DVORAK J.; JERABEK J.; USHAKOV, P. Novel Reconnection-less Reconfigurable Filter Design Based on Unknown Nodal Voltages Method and Its Fractional-Order Counterpart. Elektronika Ir Elektrotechnika, 2019, Vol. 25, No. 3, pp. 34–38. DOI: 10.5755/j01.eie.25.3.23673

[150] LANGHAMMER L.; SOTNER, R.; DOSTAL, T. New Solution of a Frequency Filter with Reconnection-less Reconfiguration of Its Transfer. In Proc. 29th International Conference Radioelektronika, 2019, Pardubice, Czech Republic, pp. 51–54. DOI: 10.1109/RADIOELEK.2019.8733544

[151] LANGHAMMER L.; SOTNER R.; DOMANSKY O.; HRICKO, T. Electronically Reconfigurable Universal Filter Based on VDTAs. In Proc. 28th International Conference Radioelektronika, 2018, Prague, Czech Republic, pp. 1–4. DOI: 10.1109/RADIOELEK.2018.8376353

[152] LANGHAMMER L.; SOTNER R. Conversion of a MISO Filter into its Reconnectionless Reconfigurable Form with Complex Active elements. In Proc. 30th International Conference Radioelektronika, 2020, Bratislava, Slovakia, pp. 1–4. DOI: 10.1109/RADIOELEKTRONIKA49387.2020.9092421

[153] LANGHAMMER L.; SOTNER R.; DVORAK J.; JERABEK J.; USHAKOV, P. Novel Electronically Reconfigurable Filter and Its Fractional-Order Counterpart. In Proc. 26th IEEE International Conference on Electronics Circuits and Systems, 2019, Genoa, Italy, pp. 538–541. DOI: 10.1109/ICECS46596.2019.8965165

[154] LANGHAMMER L.; SOTNER R.; DVORAK J.; DOSTAL, T. Novel Design Solution of Reconnection-less Electronically Reconfigurable Filter. In Proc. 26th International Conference "Mixed Design of Integrated Circuits and Systems" - MIXDES 2019, 2019, Rzeszow, Poland, pp. 365–369. DOI: 10.23919/MIXDES.2019.8787140

[155] LANGHAMMER L.; SOTNER R.; DVORAK J.; DOSTAL, T. Dual-Mode Multifunctional Reconnection-less Reconfigurable Filter. Elektronika Ir Elektrotechnika, 2020, Vol. 26, No. 3, pp. 36–41. DOI: 10.5755/j01.eie.26.3.25856

[156] LANGHAMMER L.; SOTNER R. Third-Order Reconnection-Less Electronically Reconfigurable Multifunctional Filter. In Proc. 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, Seville, Spain, pp. 1–5. DOI: 10.1109/ISCAS45731.2020.9180562

[157] LANGHAMMER L.; DVORAK J.; SOTNER R.; JERABEK J.; BERTSIAS P. Reconnection-less Reconfigurable Low-Pass Filtering Topology Suitable for Higher-Order Fractional-Order Design. Journal of Advanced Research, 2020, Vol. 25, No. 9/2020, pp. 257–274. DOI: 10.1016/j.jare.2020.06.022

[158] LANGHAMMER L.; SOTNER R.; DVORAK, J. Modification of Current Follower/Amplifier with Controllable Intrinsic Resistance, In Proc. IEEE 2018 41st International Conference on Telecommunications and Signal Processing (TSP2018), 2018, Athens, Greece, pp. 70–73. DOI: 10.1109/TSP.2018.8441237

[159] LANGHAMMER L.; SOTNER R.; DVORAK J.; SLADOK O.; JERABEK J.; BERTSIAS P. Current–Mode Fractional–Order Electronically Controllable Integrator Design, In Proc. 2020 IEEE International Conference on Electronics Circuits and Systems (ICECS), 2020, Glasgow, Scotland, pp. 1–4. DOI: 10.1109/ICECS49266.2020.9294923

[160] LANGHAMMER L.; SOTNER R.; DVORAK J.; JERABEK J.; ANDRIUKAITIS D. Reconnection–less Reconfigurable Fractional–Order Current–Mode Integrator Design with Simple Control, IEEE Access, 2021, Vol. 9, No. 10, pp. 136395–136405. DOI: 10.1109/ACCESS.2021.3117016

Other own publications unrelated to the topic of the thesis

[161] LANGHAMMER L.; SOTNER R.; DVORAK J.; JERABEK J.; POLAK J. Fully-Differential Tunable Fractional-Order Filter with Current Followers and Current Amplifiers, In Proc. 27th International Conference Radioelektronika 2017, 2017, Brno, Czech Republic, pp. 102–107. DOI: 10.1109/RADIOELEK.2017.7937576

[162] LANGHAMMER L.; SOTNER R.; DVORAK J.; DOMANSKY O.; JERABEK J.; UHER J. A 1+α Low-Pass Fractional-Order Frequency Filter with Adjustable Parameters. In Proc. 40th International Conference on Telecommunications and Signal Processing (TSP), 2017, Barcelona, Spain, pp. 724–729. DOI: 10.1109/TSP.2017.8076083

[163] LANGHAMMER L.; DVORAK J.; SOTNER R.; JERABEK J. Electronically Tunable Fully-Differential Fractional-Order Low-Pass Filter. Elektronika Ir Elektrotechnika, 2017, Vol. 23, No. 3, pp. 47–54. DOI: 10.5755/j01.eie.23.3.18332

[164] LANGHAMMER L.; SOTNER R.; DVORAK J.; JERABEK J.; ZAPLETAL, M. Fully-Differential Universal Frequency Filter with Dual-Parameter Control of the Pole Frequency and Quality Factor, In Proc. 2018 IEEE International Symposium on Circuits and Systems (ISCAS), 2018, Florence, Italy, pp. 1–5. DOI: 10.1109/ISCAS.2018.8351005

[165] LANGHAMMER L.; DVORAK J.; JERABEK J.; KOTON J.; SOTNER R. Fractional-Order Low-Pass Filter with Electronic Tunability of Its Order and Pole Frequency. Journal of Electrical Engineering, 2018, Vol. 69, No. 1, pp. 3–13. DOI: doi.org/10.1515/jee-2018-0001

[166] LANGHAMMER L.; SOTNER R.; DOMANSKY, O. Electronically Tunable Oscillator Utilizing Reinforced Controllable Parameters. In Proc. 2019 11th International Congress on Ultra Modern Telecommunications and Control Systems and Workshops (ICUMT), 2019, Dublin, Ireland, pp. 1–5. DOI: 10.1109/ICUMT48472.2019.8970997

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- Doktorské studium - obor Elektronika a sdělovací technika

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2003 - 2007: ISŠ - COP Olomoucká

- střední vzdělání s maturitou - obor mechanik elektrotechnik (26-41-L/01)

PEDAGOGICKÁ PRAXE

- výuka laboratorních cvičení kurzu Komunikační technologie, Pokročilé komunikační techniky a Architektura sítí na ústavu telekomunikací, výuka laboratorních cvičení kurzu Teorie elektronických obvodů a Návrh analogových filtrů na ústavu rádio elektroniky

- vedení 14 diplomových a 7 bakalářských prací

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Projekty podporované Grantovou Agenturou České Republiky:

- GA16-06175S Syntéza a analýza systémů fraktálního řádu využívající netradiční aktivní prvky
- GA102/09/1681 Počítačové automatizování metod syntézy lineárních funkčních bloků a výzkum nových aktivních prvků
- GA19-22248S Deterministické, chaotické a stochastické jevy v sub-mikronových integrovaných strukturách

Projekty Ministerstva školství, mládeže a tělovýchovy

- LO1401 Interdisciplinární výzkum bezdrátových technologií (INWITE)
- ED2.1.00/03.0072 Centrum senzorických, informačních a komunikačních systémů (SIX)

Projekty Evropské Unie

- CZ.1.07/2.2.00/28.0096 Příprava specialistů pro telekomunikace a informatiku - magisterské studium telekomunikační a informační technika
- CZ.1.07/2.2.00/28.0193 Komplexní inovace studijních programů a zvyšování kvality výuky na FEKT VUT v Brně
- CZ.1.07/2.2.00/28.0062 Společné aktivity VUT a VŠB - TUO při vytváření obsahu a náplně odborných akreditovaných kurzů ICT

Projekty Vysokého učení technického v Brně

- FEKT-S-14-2352 Výzkum elektronických komunikačních a informačních systémů
- FEKT-S-11-15 Výzkum elektronických komunikačních systémů
- FEKT-S-17-4707 Návrhy nových funkčních bloků a algoritmů pro moderní komunikační systémy
- FEKT-S-20-6361 Výzkum moderních obvodových řešení a algoritmů pro bezdrátové komunikační systémy

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