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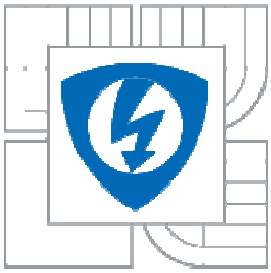

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FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
DEPARTMENT OF MICROELECTRONICS

ANALOG SIGNAL PROCESSING WITH INTEGRATED CURRENT FEEDBACK AMPLIFIERS

DOKTORSKÁ PRÁCE
DOCTORAL THESIS

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ABSTRACT

This dissertation thesis deals with the design of new functional blocks usable in area of analogue signal processing. The current feedback circuits (which in a suitable configuration can operate in voltage or current mode) are used here. This allows to achieve very promising results in the systems with a very low power supply. The versatility of the circuits will find applications in many areas. The curreent-feedback amplifier is chosen as the main building block for the detailed studies on the analog signal processing circuit design and realisation through various RC configurations. The thesis deals mainly with the study, synthesis, and design aspects of deriving new immittance functions covering inductive and supercapacitive admittances, current conveyors, voltage conveyors, high quality selective filters utilizing the transimpedance, integrators and differentiators, non-minimum phase allpass equalizers, and voltage controlled oscillators. The work deals in detail with these new particular blocks which are described theoretically and evaluated by simulations.

KEYWORDS

Analog signal processing, operational amplifier, current feedback amplifier, conveyor, integrator, differentiator, sensitivity

ANOTACE

Tato disertační práce pojednává o návrhu nových funkčních bloků použitelných v oblasti zpracování analogového signálu. Jde o obvody v proudové módu, které mohou ve vhodné konfiguraci pracovat v proudovém i v napěťovém módu. To umožnílo získat velmi nadějné výsledky v soustavách s nízkým napájecím napětím. Mnohostrannost těchto obvodů nalezne uplatnění v mnoha aplikacích. Zesilovač s proudovou zpětnou vazbou byl zavolen jako hlavní stavební blok pro detailní zkoumání funkce obvodů s RC operační sítí. Tato disertační práce pojednává o studiu, syntéze a návrhových aspektech realizace nových imitančních funkcí, jmenovitě induktivních a superkapacitních, proudových a napěťových konvejorech, kmitočtových filtrech s velkou jakostí, integrátorech a diferenciátorech, fázovacích členech s neminimální fází a napětím řízených oscilátorech. Disertační práce se detailně zabývá těmito novými bloky, které jsou popsány teoreticky a vyhodnoceny na základě simulací vlastností.

KLÍČOVÁ SLOVA

Zpracování analogového signálu, operační zesilovač, zesilovač s proudovou zpětnou vazbou, konvejor, integrátor, diferenciátor, citlivost

Bibliografická citace mé práce:

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Prohlášení

Prohlašuji, že svou disertační práci na téma *Zpracování analogového signálu s integrovanými zesilovači s proudovou zpětnou vazbou* jsem vypracoval samostatně pod vedením vedoucího disertační práce a s použitím odborné literatury a dalších informačních zdrojů, které jsou všechny citovány v práci a uvedeny v seznamu literatury na konci práce.

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V Brně dne 16.12.2010..... .....

(podpis autora)

CONTENT

List of used shorts and symbols

ASP	Analog Signal Processing
BP	Band Pass
CMOS	Complementary Metal Oxide Semiconductor
CCCS	Current Controlled Current Source
CFA	Current Feedback Amplifier
DAC	Digital to Analog Converter
DVCCS	Differential Voltage Controlled Current Source
DIL	Double Integrator Loop
F(*p*)	Complex Variable (also *s*)
FDNR	Frequency Depend Negative Resistance
FET	Field Effect Transistor
GB	Gain Bandwidth
HP	High Pass
LP	Low Pass
LSI	Large Scale Integration
MP	Microprocessor
IC	Integrated Circuit
OA	Operation Amplifier
OTA	Operation Transconductance Amplifier
PLL	Phase Locked Loop
PRA	Programmable Resistor Array
VCI	Voltage Controlled Integrator
VCO	Voltage Controlled Oscillator
VCD	Voltage Controlled Differentiator
VCSO	Voltage Controlled Sinusoid Oscillator
VLSI	Very Large Scale Integration
VCVS	Voltage Controlled Voltage Source
V_1	voltage amplitude
Z	impedance

1. INTRODUCTION

During the years the analog, but also the digital designers began to think and calculate only in terms of voltages rather than currents, although many of the signals handled by the analog circuits are actually currents in their initial state. Examining the analog paths of the signal processing system in Fig. 1.1. shows that the output signals of the sensors, which are often currents or charge, were first converted to voltages by I/V converters, before they were processed in pure voltage signal processing circuits; see Fig. 1.2. The pre-processed voltage was input signal. A similar situation occurred at the output of the signal processing system, where the output current of the D/A converter was first converted to voltage, the post-processed and finally often converted back to current to drive a physical transducer.

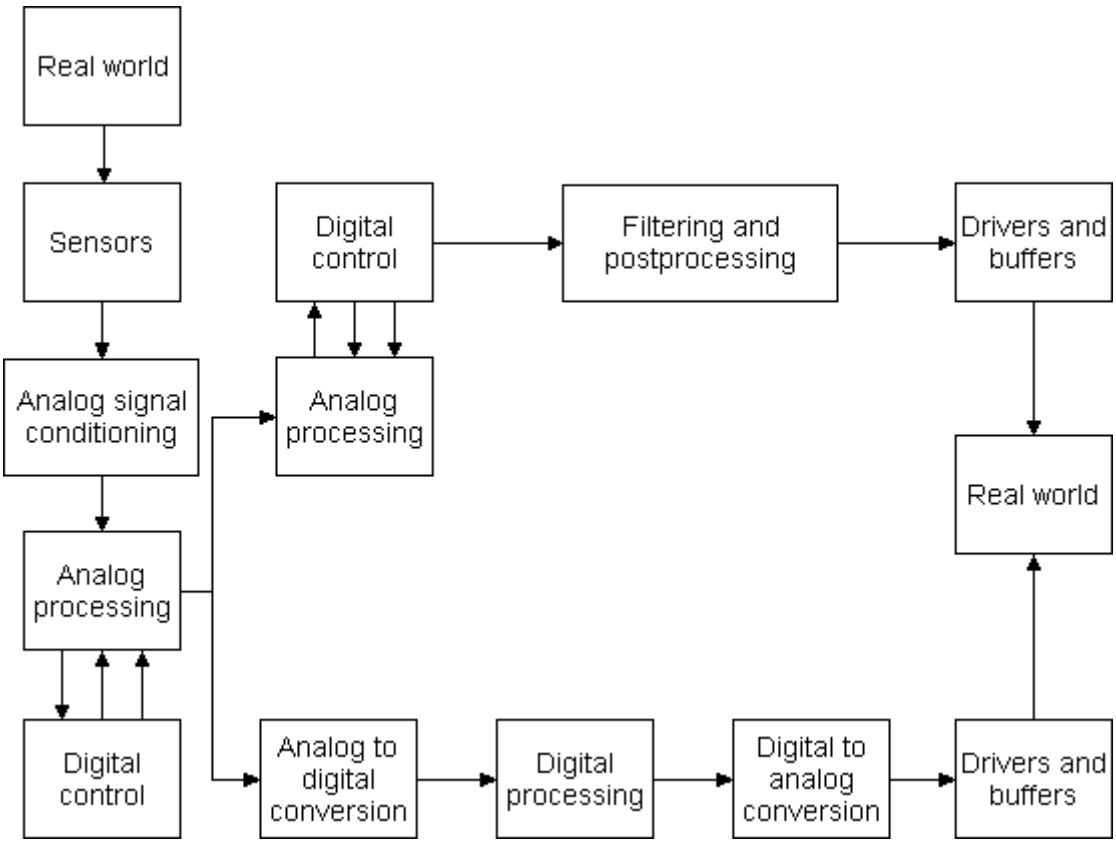


Fig. 1.1: General signal processing system [1]

A much simpler way here is to use analog circuits directly processing the signals in form of currents, like indicated in Fig. 1.3. This would skip the V/I and I/V converters necessary to adjust the input signal for voltage processing and for converting to digital signals. The chip area as well as the energy needed to drive the signal processing could be higher, because a possible sources of errors would be cancelled too.

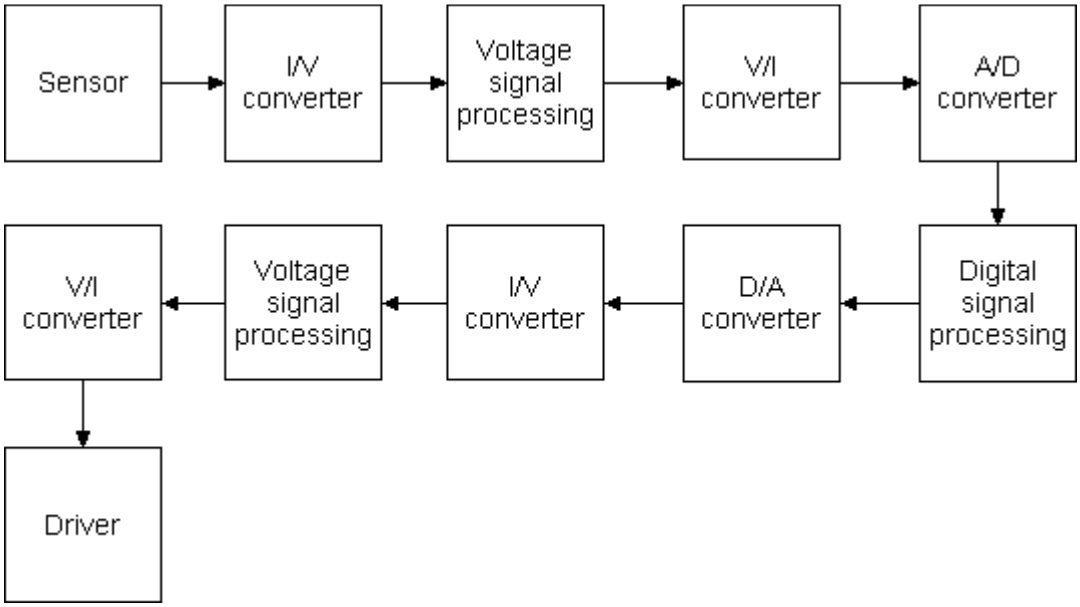


Fig. 1.2: Voltage signal processing system [1]

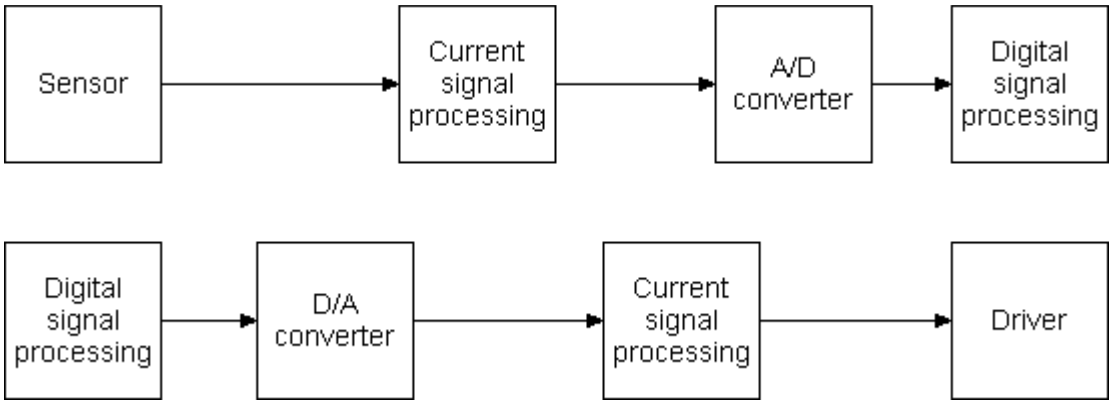


Fig. 1.3: Current signal processing system [1]

The reason, why current signal processing was not able to establish itself until now, was the missing high-performance current processing circuits. While there are number of well established building blocks for voltage processing ones, e.g. operational amplifiers, comparators, etc., there was not enough attention paid to the design of similar building blocks for current processing circuits.

A current conveyor belongs among those current processing blocks. It is very useful building block consisting of both voltage and current sub-blocks. Current conveyors were introduced in the late sixties, early seventies by Smith and Sedra. They were considered to be used as controlled voltage and current sources, impedance converters, etc., but also as function

generators, amplifiers, filters, etc., in current processing circuits mainly for instrumentation and measurement applications.

In the first years of their appearance the performance of current conveyors was severally limited by the available technologies, which didn't allow well-matched devices on fabricated chips. Since the technologies have improved, the current gained attention of many analog designers. Today the current conveyors have developed to very useful building blocks of analog electronics and their main application areas are in high-speed, high-frequency circuits for both voltage and current signal processing.

A conveyor is generally a three-port device (except special types) operating mostly in the current mode. It consists of two blocks, a voltage VF and a current CF follower. By the order of their arrangement, a voltage (Fig. 1.4) and a current (Fig. 1.5) conveyor can be recognized.

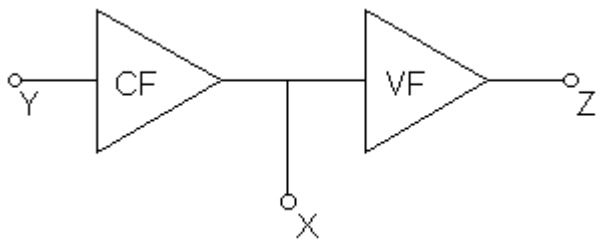


Fig. 1.4: Voltage conveyor

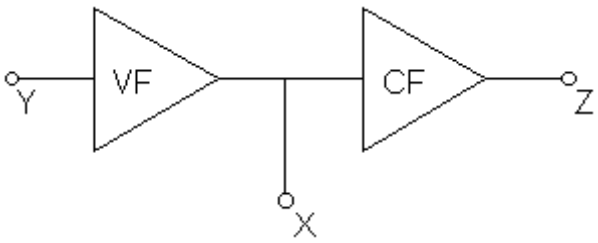


Fig. 1.5: Current conveyor

2. AIM OF DISSERTATION

This work is focused on the field of the active building blocks for the modern integrated circuits operated in current-mode or mixed-mode.

The main idea of the thesis consists in taking a commercially available modern integrated circuit-CFA and studying its application in various new electronic blocks even if some of them are already known in their voltage-mode versions. The thesis will be more oriented to the applied research than to the fundamental one and focused to the currently available current mode amplifiers.

Aims of the dissertation are in the following:

1) Investigations of the effects of the imperfections in current mode amplifiers.

2) Design and verification of the insensitive circuits with current mode amplifiers.

3) New designs of an integrator and a differentiator in both current- mode and voltage-mode forms.

3. STATE-OF-THE-ART

Analogue integrated circuit design is becoming increasingly important with growing opportunities. IC processing techniques have now evolved to the point where high-performance and novel “special” devices are being integrated. This in turn has led to a renewed interest in circuit design techniques, which were previously limited by the technology available – essentially we are now seeing technology-driven advances in circuit design. An example is the development of “current-mode” techniques (Toumazou 1990, Current mode approach [11]), many of which have only become practically feasible with the development of true complementary bipolar and MOS technology processes.

Voltage-mode analogue circuit design has called as a “traditional” nowadays. Current-mode signal processing circuits have recently demonstrated many advantages over their voltage-mode counterparts including increased bandwidth, higher dynamic range and better suitability for operational in reduced supply environments (e.g. supply voltage 3.3 V and lower). In addition, current-mode processing often lead to simpler circuitry (e.g. processing of current signals from measurements probes) and lower consumption.

There are some limitations in obtaining high current gain and wide bandwidth for low offset current and high-speed gain operation. Usually, higher gain can be achieved by using a closed-loop feedback gain configuration formed by a feedback resistor ratio. The signal processing speed is determined by the amount of voltage swing on each delay path. Ideally, a current-controlled current source (CCCS) has zero input impedance and infinite output impedance. The conceptual justification for high-speed operation in current-mode circuit results from the small voltage swing of each low-impedance node, operation near transition frequency f_T, and wide-band frequency response.

In CMOS technology developments have centred on a new generation of analogue sampled data processing that may refer to as switched or dynamic current circuits. These circuits include switched current filters, dynamic current mirrors and current copier and memory cells. At the other hand, there have been developed novel special analogue building blocks opposite to voltage-mode classical blocks. These blocks, including current amplifiers, current followers, current conveyors and others, can be called as “adjoint” refer to voltage amplifiers, voltage comparators, followers and so on. One of the primary motivations behind these developments has been the shrinking feature size of digital CMOS devices, which necessitates the reduction of supply voltages. This is the fact that 3.3 V is CMOS process standard nowadays (near future follows 1.5 V). Due this, process parameters such as threshold voltage will be chosen to optimise digital performance and so voltage domain behaviour will suffer as

a consequence. Such difficulties can be over come by operating exclusively or selectively in the current domain. Current conveyor and current follower based filters replace traditional voltage-mode filters. Similarly current-mode implementations of VLSI CMOS A to D converters and neural computing processors represent exciting new developments and are clear examples of technology driven design. CMOS technology has become a dominant analogue technology because of good quality capacitors and switches. BiCMOS technology combines both the advantages of bipolar and CMOS providing a very attractive low power, high-speed technology for which current-mode techniques would be ideally suited.

Furthermore, with maturing CMOS VLSI, BiCMOS and true complementary bipolar technology, current-mode analogue design techniques play an important role in successfully exploiting these technologies in the analogue domain. As a consequence many of the early current-mode circuit techniques are enjoying a renaissance and a new generation of current-mode analogue building blocks and systems are being developed and described throughout this thesis.

The advancement of the semiconductor technology in the recent past had significant impact to the research and development (R&D) activities on electronic circuit and systems with vast coverage on Analog signal processing (ASP). The impact had renewed impetus with introduction of the versatile monolithic integrated circuit (IC) building block termed as Operational amplifier (OA) [21, 22].

The OA device is essentially a voltage controlled voltage source (VCVS) element. Since its inception, the OA element had been widely used for various voltage mode circuit design covering widespread areas of applicabilities in ASP [21, 22].

Among these, the design of passive inductorless active OA-RC function circuits, e.g., selective filters, phase equalizers, wave processors like integrators / differentiator, wave generator are quite popular, useful and IC- adaptable, since passive inductances are not compatible to IC technology . The approach subsequently gave way to synthesizing active immittance functions by OA-RC methods. During this course of research activity, Bruton suggested a new type of immittance function known as the Frequency Dependent Negative Resistance (FDNR) [24]. Popularized later either as Supercapacitor $(Y(p) = p^2)$ or Superinductor $(Y(p) = p^{-2})$.In course of the progress on ASP circuit and system (CAS) design there emerged newer types of active building block viz., the Operational Transconductance Amplifier (OTA) and the current conveyor (CC) [12 - 20].The OTA is essentially a Differential Voltage Controlled Current Source (DVCCS). Whereas the Current Conveyor is basically a Current Controlled Current Source (CCCS) element suitable for

current mode ASP [36-38]. Many workers had contributed elegant schemes on ASP function circuit design using the OTA and the current conveyor in its various forms in the recent past [11].

Most recently, another new device, known as the Current Feedback Amplifier (CFA) had been introduced which is a versatile building block compatible to both voltage mode and current mode functioning [11]. This is essentially a unity gain current transfer device wherein the voltage across its trans impedance can be copied at a voltage source output nodes.

The unique property of the device, now commercially available as an off the shelf items as AD-844 IC. The notable advantage of the device may be summarized as:

- accurate port transfer characteristics at extremely low tracking errors
- improved ac performance with better linearity.
- gain-independent constant bandwidth at moderate to high gains.
- high slew rate (SR) specification.
- both current and voltage signal cascadability
- low sensitivity design owing to accurate port tracking property.
- fast settling time.

Recently the CFA element is receiving considerable interest on the R&D activities in areas of ASP Circuits [25, 26]. In particular, the features of high SR and fast settling speed make the CFA readily adaptable to some special function circuits, video amplifiers, analog dividers, D/A current to voltage converters, high frequency current copiers, high speed data communication system etc.

Albeit many analog only domain CFA-based ASP designs had been presented in the literature, there is further possibility of R&D work in the domain of mixed analog-digital mode signal processing applications wherein the tuning component of an analog function circuit can be tuned through a digital word(code) [27,28].

We have chosen the CFA as the potential active element for our work on ASP circuit design and realization schemes through CFA-RC configurations in the thesis.

We like to study the design, synthesis and realization as aspects of deriving new immittance functions covering inductive and super capacitive admittances, high quality selective filters utilizing the CFA trans impedance integrators/ differentiators , non-minimum phase all pass(AP) equalizers, and Sine wave oscillators/Voltage Controlled Oscillator (VOC) [29].

4. CURRENT AND VOLTAGE CONVEYORS

Classical voltage operational amplifier (VOA) is a one of the most famous and common used blocks. VOA can be described as active building block that operates in voltage-mode. Another similar block is voltage follower (VF). A number of blocks with reciprocal behavior to previous voltage mode blocks have been proposed during last 15 years. Current operational amplifier (COA) and current follower (CF) can be mention as examples.

Moreover, some of basic building blocks can operate in both, voltage and current, modes. This type of bocks has been sorted as mixed-mode. Mixed-mode block usually has both, "voltage" and "current" terminals. The most famous mixed-mode active block is current conveyor [2, 3]. Nowadays becomes renaissance of these universal building blocks. Current conveyors appear in many modern constructions of wideband and high-speed operational amplifiers, etc.

4.1. CURRENT CONVEYORS - HISTORY AND PRESENCE [20]

One of the most basic building blocks in the area of current-mode analogue signal processing is the current conveyor (CC). It is a four (in basic form) terminal device which when arranged with other electronic elements in specific circuitry can perform many useful analogue signal processing functions. In many ways current conveyor simplifies circuit design in much the same manner as the conventional operational amplifier. The current conveyor offers an alternative way of abstracting complex circuit functions, thus aiding in the creation of new and useful implementations. Moreover, CC is a mixed-mode universal building block (in VLSI terms), which can substitute classical op-amps in voltage-mode applications or gives us chance to transform these applications to current-mode.

Many papers have demonstrated the universality, advantages and novel applications of the current conveyor since its first introduction in 1968 [2]. Concurrently with these papers, a number of authors have outlined improved implementations designed to enhance the performance and utility of this circuit building block. Unfortunately, there is still lack of available current conveyors in form of IC. Many designers cannot use this block in their developed applications and systems due this. If the situation will change, the designers will get the chance to be more familiar with the current conveyor and its usability. There is only one monolithic IC of “pure” current conveyor – CCII01. Paradoxically, many novel constructions of modern wideband and high-speed op-amps are based on current conveyor (OPA660, AD840).

In following chapters are reported existing types of current conveyor and will be discus novel types and techniques that lead to improvement of their features.

4.2. CURRENT CONVEYOR OF THE 1ST. GENERATION – CCI

The *current conveyor* was originally introduced as *3-port* device [2]. The operation of this device can be described by followings terms: if a voltage is applied to input terminal Y, an equal potential will appear on the input terminal X. In a similar fashion, an input current I being forced into terminal X will result in an equal amount of current flowing into terminal Y. Finally, the current I will be conveyed to output Z. Note, that Y output has characteristics of a current source of value I with high output impedance. Voltage at X terminal is independent on the current forced into this port. Similarly, the current flows through input Y is fixed by current through X terminal and is independent on Y potential. The CCI device exhibits a virtual short-circuit input characteristics at port X and dual virtual open-circuit input characteristic at port Y. This functionality can be described by following hybrid equation:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad (1)$$

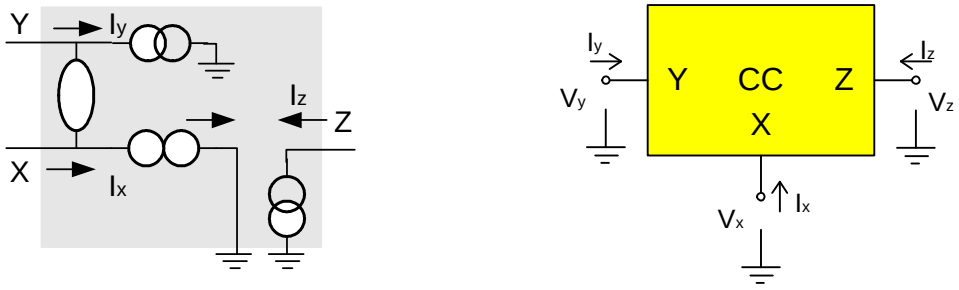
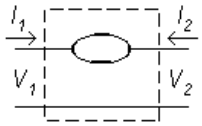
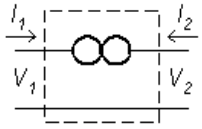
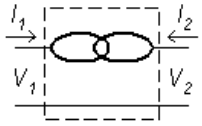
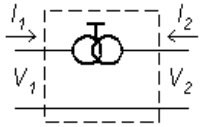


Fig. 4.1: CCI nullator-norator model and block diagram

Macromodels of conveyors types are used in this section. Macromodels consist from basic ideal elements – nullator, norator, ideal current- and voltage-sources, Tab. 4.1.

Basic elements		
Type	**Symbol**	**Definition**
nullator		$V_1 = V_2$ $I_1 = I_2 = 0$
norator		$I_1 = -I_2$ V_1, V_2 *are arbitrary*
voltage mirror		$V_1 = -V_2$ $I_1 = I_2 = 0$
current mirror		$I_1 = I_2$ V_1, V_2 *are arbitrary*

Tab. 4.1: Basic elements

4.3. CURRENT CONVEYOR OF THE 2ND GENERATION – CCII

To increase the versatility of the current conveyor, a second generation in which no current flows in terminal Y, was introduced [9]. This building block has since proven be more useful than CCI. CCI can be described by following matrix:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{2}$$

From above equations is clear that terminal Y exhibits infinite input impedance. The voltage at X terminal follows the Y potential, X exhibits zero input impedance, and current flows through X port is again conveyed to the high impedance current output Z. Current flows

through Z terminal has same orientation as current through the terminal X (CCII+) or opposite polarity in case of CCII-.

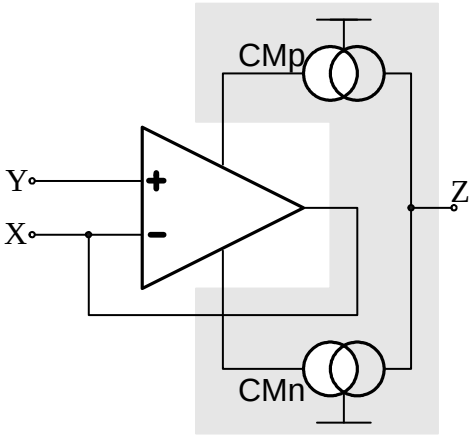


Fig. 4.2: CCII based on classical voltage opamp

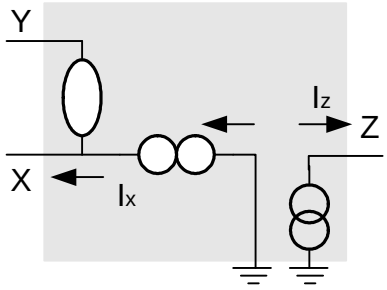


Fig. 4.3: CCI nullator-norator model and simple CMOS implementation

CCII has proven to be by far the more useful of the current conveyor family types. Wide range of applications was published. It's very suitable building block for design of the active-RC filters or number of special imitance (admittance) converters. In the last decade the number of high-speed and wide-range opamps are based on current conveyor structure. And also for low voltage applications CCII is starting to be very powerful building block.

4.4. CURRENT CONVEYOR OF THE 3RD GENERATION – CCIII

CCIII was introduced in [4]. This type is similar to CCI, there is opposite current transfer between X and Y terminal. Matrix described this CC type is following:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{3}$$

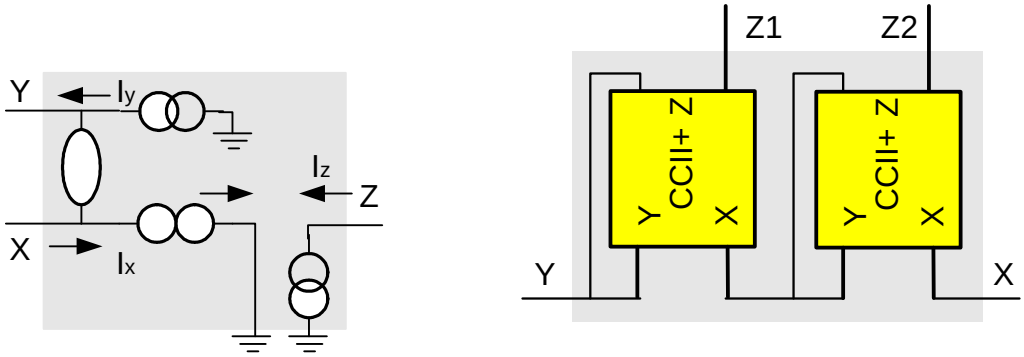
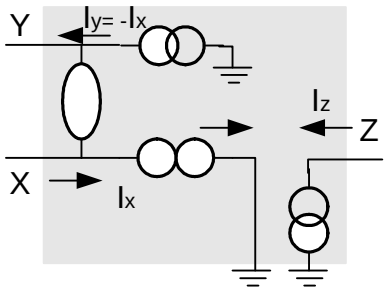


Fig. 4.4: CCIII nullator-norator model and simple implementation based on CCIIs

4.5. INVERTING CURRENT CONVEYOR OF THE 2ND GENERATION ICCII

The first inverting current conveyor, the inverting second-generation current conveyor (ICCII), was described in [5]. The general matrix description of the second generation inverting current conveyor is:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & b & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{4}$$



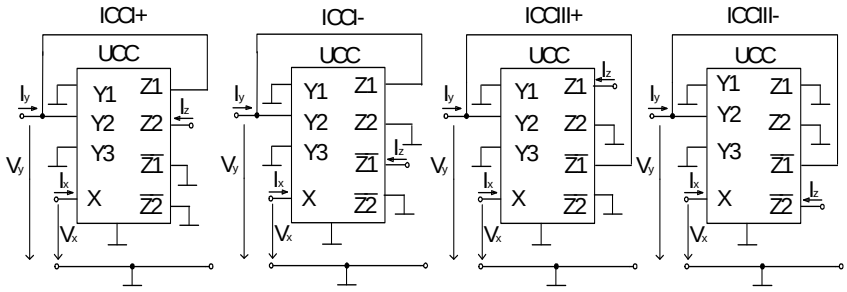


Fig. 4.5: ICCI nullator-norator model and implementation of the ICC family using UCC

b determines the current transfer of current conveyor from the X-terminal to the Z-terminal. For *b* positive the matrix describes the current conveyor with positive current transfer. The negative current conveyor has *b* negative in its matrix description. The realisation using UCC is in Fig.4.5.

4.6. CURRENT CONVEYORS WITH DIFFERENTIAL INPUT

The most used type is the second-generation current conveyor (CCII+/-) [3] in these days. Number of very important analogue building blocks can be realized with CCII: all types of control sources, impedance inverters and converters, and many others. However, one disadvantage of CCII in some cases can be observed. Conventional CCII can't be used in applications demanding differential or floating inputs like impedance converter circuits and current-mode instrumentation amplifiers. Then the design of such an amplifier requires two or more CCIIs. A basic structure used in realizing floating input applications built by CCIIs is shown in Fig.1.11. This circuit uses two CCIIs and a floating resistor (connected between the X-terminals of the two CCIIs) to provide floating input handling capability. As each X-terminal has an output resistance R_x then the effective resistance between the two X-terminals is $R-2R_x$, and the error caused by the nonzero resistance is doubled.

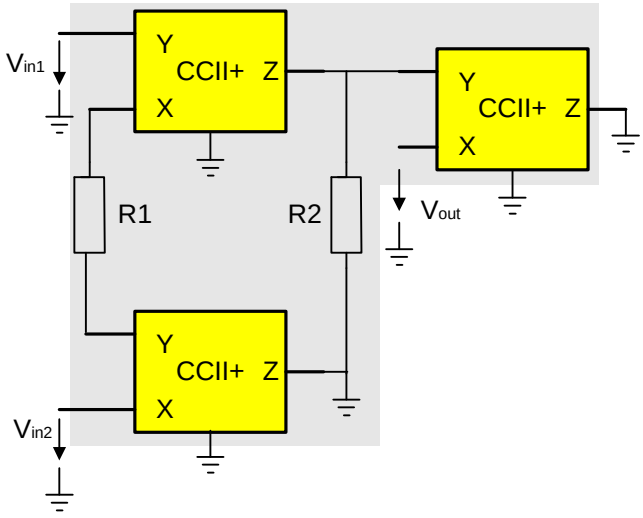


Fig. 4.6: Floating input realized by the three CCIIs

This problem has been solved with the help of special current conveyors - current conveyors with differential input (DDCC, DVCC) [6, 7]. The DVCC and DDCC are relatively simple and useful building blocks, which keep all advantages of CCII and cancel the disadvantage of simple high-impedance input terminal.

Summary: At the time of the introduction of the current conveyor (1968, 1970) it was not clear the advantages the current conveyor offered over the conventional operational amplifier. Without clearly stated advantages, the electronic industry lacked the motivation to develop a monolithic current conveyor realization.

Research in analog integrated circuits has recently gone in the direction of *low-voltage* (LV) and *high-speed* design, especially in the environment of the portable systems where a low supply voltage, given by a single-cell battery, is used. In this area, traditional voltage-mode techniques are going to be substituted by the current-mode approach, which has to be recognized advantages to overcome the gain-bandwidth product limitation, typical of operational amplifiers. Then they do not require high voltage gains and have good performance in terms of speed, bandwidth and accuracy. Inside the current-mode architectures, the *current conveyor* (CCII) can be considered the basic circuit block because all active devices can be made of a suitable connection of one or two CCIIs. CCII is particularly attractive in portable systems, where LV constraints have to be taken into account. In fact it suffers less from the limitation of low current utilization, while showing full dynamic characteristics at reduced supplies (especially CMOS versions) and good high frequency performance. Recent advances in integrated circuit technology have also

highlighted the usefulness of CCII solutions in large number of signal processing applications.

In previous chapters a number of current conveyor types were presented. Some of them are important only in theoretical point of view, the others could become powerful functional building blocks for monolithic ICs. All existing building blocks suffer from nonidealities due to real behavior of the transistors and technology process. The focus will be move on the design techniques which reducing the main parasitic parameters of current conveyors – parasitic resistance of the X terminal.

A number of current conveyor types have been introduced since 1968. But still there is no commercial IC with pure current conveyor structure. In this case designers could not use any type of current conveyor as discrete device or IC.

4.7. VOLTAGE CONVEYOR

The novel active mixed-mode blocks with one independent voltage from family of immitance converter can be described. These blocks have been called as *voltage conveyors*). Note that title voltage can be a little misguided because voltage conveyor can operate in voltage-, current- or mixed-mode (as current conveyor).

A generally three port voltage conveyor is defined by following matrix equation:

$$\begin{bmatrix} I_z \\ V_w \\ V_p \end{bmatrix} = \begin{bmatrix} 0 & \alpha & \beta \\ \gamma & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_z \\ I_w \\ i_p \end{bmatrix} \tag{5}$$

The general voltage conveyor has reciprocal behaviour with respect to the well-known general current conveyor. Then whole group of voltage conveyor types can be found and declared using reciprocal principle that is illustrated in Fig.4.7.

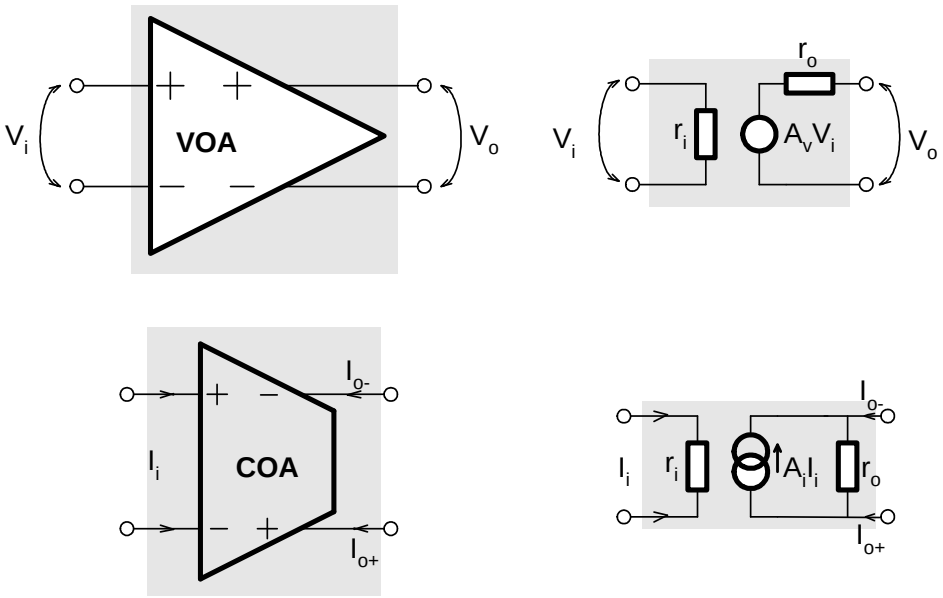
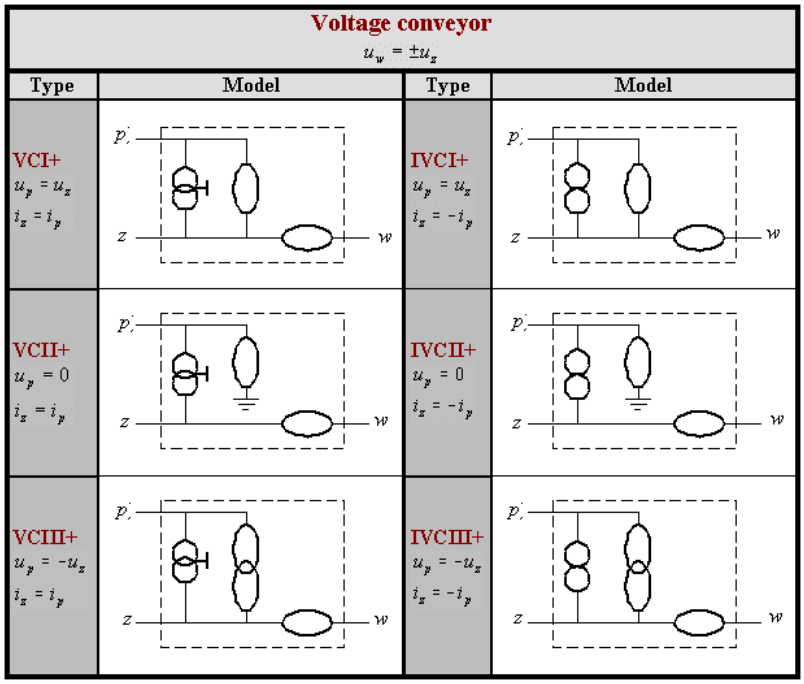
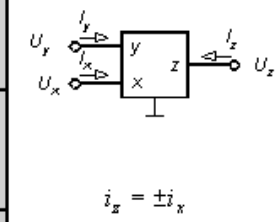
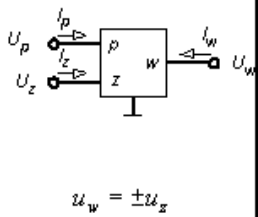


Fig. 4.1: VOA versus COA (diagrams and macromodels) – Illustration of the reciprocal principle

Fig. 4.1 shows macromodels of the basic voltage conveyors, it means voltage conveyors with single input and single output. The macromodels of more complex voltage conveyors (with differential input, multiply outputs) can be synthesizing in similar way.



Tab. 4.2: Macromodels of the basic Voltage conveyors

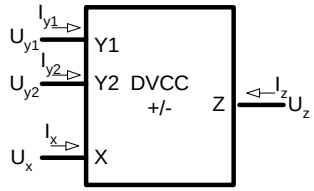
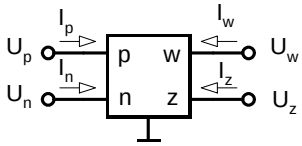
Current conveyor			Voltage conveyor		
Type	Symbol	def.	Type	Symbol	def.
CCI +/-	 $i_z = \pm i_x$	$i_y = i_x$ $u_x = u_y$	VCI +/-	 $u_w = \pm u_z$	$u_y = u_z$ $i_z = i_y$
CCII +/-		$i_y = 0$ $u_x = u_y$	VCII +/-		$u_y = 0$ $i_z = i_y$
CCIII +/-		$i_y = -i_x$ $u_x = u_y$	VCIII +/-		$u_y = -u_z$ $i_z = i_y$
ICCI +/-		$i_y = i_x$ $u_x = -u_y$	IVCI +/-		$u_y = u_z$ $i_z = -i_y$
ICCII +/-		$i_y = 0$ $u_x = -u_y$	IVCII +/-		$u_y = 0$ $i_z = -i_y$
ICCIII +/-		$i_y = -i_x$ $u_x = -u_y$	IVCIII +/-		$u_y = -u_z$ $i_z = -i_y$

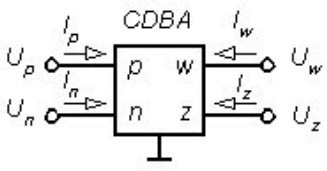
Tab. 4.3: Macromodels of the basic Current and Voltage conveyors

4.8. CIRCUITRY IMPLEMENTATION

Voltage conveyor is newly introduced active block and then its circuitry implementations do not exist yet. There is only one exception – the CDBA circuitry implementation can be found in [8], where the CDBA is implemented using two standard operational amplifiers AD844.

The novel active mixed-mode block called *current differential buffered amplifier* (CDBA) was published at 1999 [8]. CDBA is four-port block and its symbol and matrix description is shown in Fig. 4.8. Terminal *n* and *p* are low-impedance (current) inputs, terminal *z* is input-output node and terminal *w* is voltage output terminal. Moreover, it can be proved that using previously introduced reciprocal principle the CDBA is reciprocal block to DVCC+.

Current conveyor		Voltage conveyor	
Type	**Symbol and definition**	**Type**	**Symbol and definition**
DVCC+		DCVC+ (CDBA)	
DVCC-	$i_z = \pm i_x$ $i_{y1} = i_{y2} = 0$ $u_x = u_{y1} - u_{y2}$	DCVC-	$u_w = \pm u_z$ $u_p = u_n - 0$ $i_z = i_p - i_n$



$$\begin{bmatrix} i_z \\ v_w \\ v_p \\ v_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_z \\ i_w \\ i_p \\ i_n \end{bmatrix}$$

Fig. 4.7: Symbol and matrix description of CDBA block

Differential current input (realized by input *n* and *p*) is very useful advantage of this block. Current that flows through terminal *z* resulted from this differential input stage. Voltage drop, which is created due to the flowing current, is then copied on output terminal *w*. Detailed description and some applications can be found in [8, 9, 10].

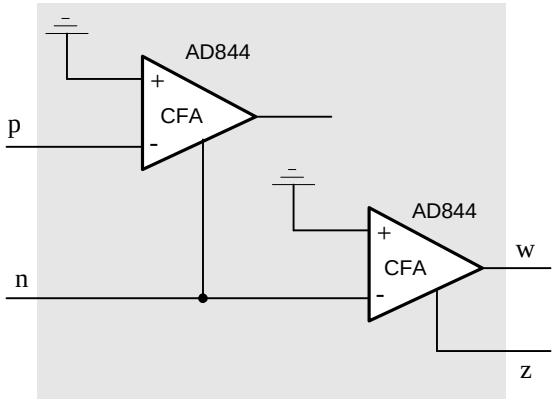


Fig. 4.8: Realisation CDBA using commercial ICs AD844

Usability of this novel group of active building blocks have to be prove in applications as filters, converters circuitries or novel structures of the modern voltage or current operational amplifiers. It is possible to implement the differential inputs, multiply and complementary outputs to voltage conveyor as in case of current conveyor.

5. CFA-BASED DESIGN OF ACTIVE IMMITTANCE

The CFA device we propose some new design schemes for low sensitivity immittance functions using CFA device. The proposed design is for deriving the driving point admittance for

i. ideal inductance (L)

ii. ideal supercapacitor type FDNR (D)

The topic of inductive (L) and FDNR type (D) immittance function simulation had been examined by various researchers using Operational amplifier (OA) current conveyor (CC) [49, 55-59] and the differential voltage controlled current source (DVCCS) devices [12 - 20].

We propose similar function realization schemes using the most recent device, the current feedback amplifier (CFA). The advantages of such CFA based realizations are derived mainly owing to the accurate port tracking characteristics of the CFA device which leads to practically insensitive design [29, 30].

The effects of the port tracking errors on the simulation element L and D were examined and subsequent compensation design equation have been derived. First we present the inductance simulation followed by the FDNR simulation scheme.

Measurement on the VI characteristics of the proposed inductor exhibited good quality response of the synthetic coil up to 330 kHz. Responses of frequency selective resonator circuit using the simulated element have been examined. The responses were verified both with hardware implementation and by PSPICE macro model simulation.

5.1. ANALYSIS FOR INDUCTANCE L

The CFA device we propose some new design schemes for low sensitivity imitance. The CFC is a 3- terminal current mode device with port relations

$$\begin{pmatrix} I_Y \\ V_x \\ I_z \end{pmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta & 0 & 0 \\ 0 & \pm a & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \text{ and } V_0 = \delta V_Z \qquad (5.1)$$

Where the port transfer ratio may be expressed in terms of error coefficients ($\in$) as

$$\alpha = 1 - \in_i \quad \beta = 1 - \in_v \quad \delta = 1 - \in_z \tag{5.2}$$

According to available literature report these tracking errors are extremely small

$$(0.01 \leq \in_{i,v,z} \leq 0.004)$$

Analysis of the proposed circuit in Fig. 5.1 using the above expression, we get the driving point admittance.

$$Yi = (\alpha_1 \alpha_2 \beta_1 \beta_2)\ (y_1 y_2 / y_0) \tag{5.3}$$

The derivation of this equation does not necessitate any reliability condition. For a lossless inductor assuming ideal $(\alpha = \beta = \delta = 1, \in_{i,v,z} = 0)$ CFAs, we may select

$$\begin{aligned} Y_0 &= pC; \quad Y_{1,2} = 1/R_{1,2} \\ \mathrm{L}_{eq} &= CR_1R_2 \end{aligned} \tag{5.4}$$

The inductance value slightly increases because of the increment in the resistor value given by

$$\left.\begin{aligned} \tilde{R}J &= RJ(1 + \in_{0j}) \\ Where\ \in_{oj} &= 1 - (\in_{ij} + \in_{vj}) \end{aligned}\right\} \tag{5.5}$$

Here products of error terms have been neglected since $\in_{i,v,z} << 1$.

The inductance may be varied independently by any of the RC components. In the event of non ideal CFAs $(\in_{i,v,z} \neq 0)$, the modified impedance function is

$$Z_i' = pCR_1'R_2' = pL_{eq}' \tag{5.6}$$

where $R'_j = R/\alpha_j\beta_j; \qquad j = 1,2$ (5.7)

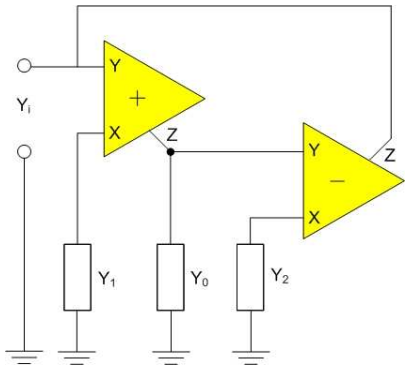


Fig. 5.1: Lossless grounded inductor

On the Fig. 5.1. is lossless grounded inductor ($L_{eq} = CR_1R_2$) with $y_{1,2} = 1/R_{1,2}$ and $y_0 = pC$.

5.2. COMPENSATION DESIGN

The compensation scheme calls the reduction of increments indicated in eq. (5.5) caused by the port errors of the non ideal CFAs. This may be done by shunting $R_{1,2}$ by suitable compensating resistors $r_{1,2}$ given

$$\tilde{R}_j^{-1} + r_j^{-1} = R_j^{-1} \quad \text{j = 1,2} \tag{5.8}$$

Which yields the compensation design equation

$$r_j = R_j / \in_{0j} \quad \text{j = 1,2} \tag{5.9}$$

5.3. SENSITIVITY

The classical sensitivity figure may be defined $\left(S_a^{\ b}\right) = a(db)/b(da)$ the active sensitivity figures for the simulated inductance are given by

$$\left.\begin{aligned} s^{L}_{\epsilon_{j,v_j}} &= \frac{\epsilon_{j,v_j}}{1+\epsilon_{01}+\epsilon_{02}} << 1 \qquad \text{j = 1,2} \\ s^{L}_{\epsilon_j} &= 0 \end{aligned}\right\} \tag{5.10}$$

The immittance function realization is therefore practically active insensitive. The passive sensitivity may be computed considering the fractional change expressed in terms of the sensitivity summation and incremental change in RC components (due to temperature variations , ageing .) given by

$$\Delta L / L = \sum_{J=1}^{2} \left(S_{R_j}{}^{L}\right)(\Delta R_j / R_J) + S_C{}^{L}(\Delta C / C) \tag{5.11}$$

In monolithic or hybrid IC Technology , increments in one kind of component track quite closely, i.e., $\Delta R_j / R_j = \Delta R / R.$ Calculation of the sensitivity and noting that average fractional change in resistors can be made equal to that of capacitors, we get $\Delta L / L = (\Delta R / R) + (\Delta C / C).$ It is possible to get RC components with equal opposite temperature coefficients in thin film technology i.e., $\Delta R = -\Delta C$; therefore

$$\Delta L / L = 0 \tag{5.12}$$

Hence the incremental passive sensitivities may be significantly reduced with appropriately matched RC components in microcircuit fabrication .It may be noted in eq.(5.3) that even with nonideal CFA devices, the proposed configuration is able to realize lossless inductance element, but with slightly altered magnitude an added advantage.

5.4. FLOATING IMMITTANCE

The circuit of Fig. 5.1 may be modified for the realization of floating lossless inductor, by insertion of another CFA as shown in FIg. 5.2 a unity gain buffer may be needed to isolate y1 from the input port. Here the realizability condition is $y_2 = y_3$, and for a floating inductive immittance we make $y_0 = pC$, $y_1 = y_3 = 1/R$ then the driving point admittance matrix is

$$Y = \left[\frac{1}{pL_{eq}}\right]\begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \qquad (5.13)$$

where $L_{eq} = CR^2$

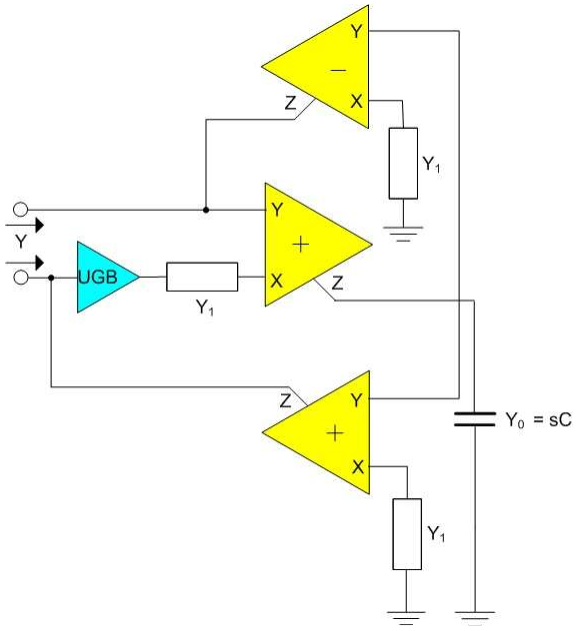


Fig. 5.2: Lossless grounded inductor ($L_{eq} = CR^2$) with $y_1 = y_2 = 1/R$ and $y_0 = pC.$

5.5. AN INSENSITIVE IDEAL SUPERCAPACITOR

A super capacitor type FDNR (D) element is a second order immittance function which is generally obtained by the frequency transformation of capacitive immittance (sc) multiplied by a Laplace operator sτ,that yields D = Cτ. The driving point admittance (Y_i) has been synthesized as multiplicative form $Y_i = Y_{a.}.Y_b / K$ where K must be another admittance for dimensional equality. The CFA device with a high gain operational Amplifier (OA) in the feedback loop as in Fig 5.2(b) has been used to generate an immittance function of the form $Y_{in} = Y_a.Y_b / Y_c$, The port errors introduce slight deviations in the element values (D' or L') and there appears some shunt lossy terms (r_x with L, C_x with D) whose effects are insignificant since $\in$ << 1. A simple design application of the FNDR- a third order low pass Butterworth filter realization had been proposed and maximally flat response had been verified.

5.6. ANALYSIS FOR SUPERCAPACITOR

Analysis of the circuit in Fig. 5.3using the ideal CFA ($\in = 0$), yields

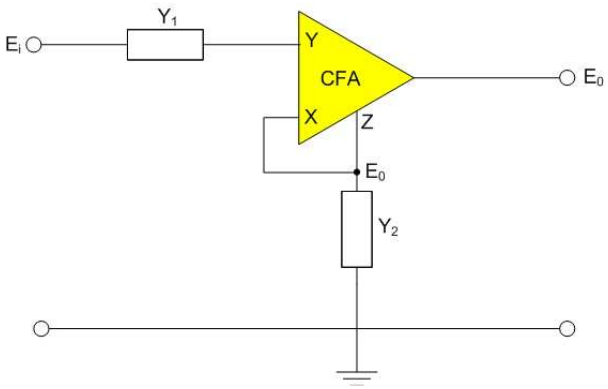


Fig. 5.3: Realization of F(p)

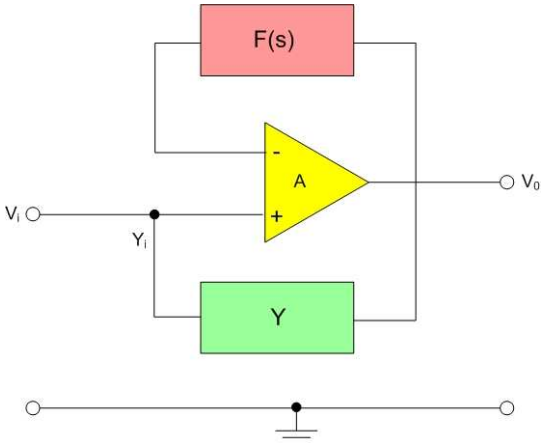


Fig. 5.4: Generation of Inverse of F(p)

$$E_0 / E_i = Y_1 /(Y_1 - Y_2) \tag{5.14}$$

$$E_0 / E_i = Y_1 /(Y_1 - Y_2) \tag{5.15}$$

$$\text{Denoting } E_0 / E_i = F(p) \text{, we get } F(p) = \{1 - (Y_2 / Y_1)\}^{-1} \tag{5.16}$$

The CFA has been connected in feedback of a high gain operational amplifier of gain A ($A \to a$), Fig. 5.4. The gain of the circuit

$$\frac{V_0}{V_i} = \frac{A}{1 + F(p)A} \approx \frac{1}{F(p)} \tag{5.17}$$

Analyzing for Y_{in} in Fig. 5.4 we get

$$Y_{in} = \left(1 - \frac{1}{F(p)}\right) y_0 \tag{5.18}$$

$$Y_{in} = \frac{y_2 . y_0}{y_1}$$

where Y_{in} = Driving point impedance of Fig. 5.4

For a supercapacitor simulation, $y_{0.2} = pC_{0.2}$ and $y_1 = 1/R_1$

Then $Y_{in} = p^2 . C_0 C_2 . R_1 = p^2 D$

where supercapacitor element or FDNR is

$$D = C_0 C_2 R_1 \tag{5.19}$$

The FDNR elements are tunable by one of the components is no matching constraint-an advantage for microcircuit fabrication.

The effects of the CFA port errors are estimated by assuming non ideal CFA and considering finite port errors $(\in_{i,v,z} \neq 0)$ we get the modified admittance function

$$Y_{in}(p) = pC_x + p^2 D' \tag{5.20}$$

$$\text{Where } D'/D = 1/1 - \in_i \text{ and } C_x = \in_v C_0 \tag{5.21}$$

5.7. DESIGN APPLICATION

The active immitances proposed had been used in frequency selective filter design, e.g., the grounded –L in the Fig 5.2 and Fig5.3 for a band pass type shunt –LC resonator see Fig. 5.5 and the grounded –D in Fig. 5.4 had been utilized for the design of a third low pass (LP).

The transfer function H(s) and the filter parameters of the LC-resonator are

$$H(s) = V_{out} / V_{in} = \frac{p / C_X R_X}{p^2 = p / C_X R_X + 1 / LC_X} \tag{5.22}$$

$$f_0 = 1/\sqrt{LC_X} \tag{5.23}$$

$$Q = R_X \sqrt{C_X / L} \tag{5.24}$$

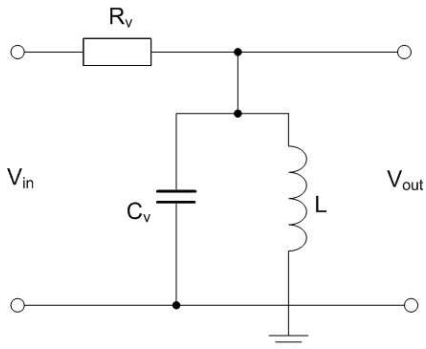


Fig. 5.5: Resonator

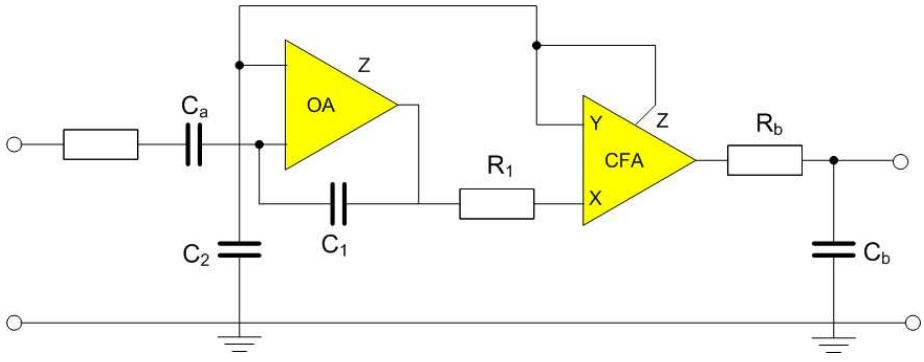


Fig. 5.6: Realization of third-order network

We consider the application of D element. A simple design application of the D-

element for the realization of third order low pass filter is shown in the Fig. 5.6.

Where the voltage transfers

$$V_{out}/V_{in} = H(p) = \frac{1}{d_3 p^3 + d_2 p^2 + d_1 p + 1} \qquad (5.25)$$

Where $d_3 = DR_0R_bC_b; D = C_0R_1R_2; d_2 = D(R_0 + R_b(C_b/C_0))$. The filter response had been tested using AD-844 device with ± 12 V dc supply and selecting all equal-value passive components suitable for $f_0 = 1kHz$.

5.8. EXPERIMENTAL RESULT

The simulation circuit had been tested by using AD-844 CFA element biased at ± 12 V dc A tuned-LC resonator had been formed for verifying the band pass characteristics. A typical response for $f_0 = 65kHz$ Q = 2.9 and Q = 1 is shown in Fig. 5.7.variation of the resonance frequency (f_0) could be done by adjustment of R_1 or R_2. Independent tuning of f_0 had been verified up to 210 kHz with Q-values in the range 1 < Q < 10. Next the self oscillation of the parallel LC section had been observed with a smooth variation of the oscillation frequency in the range of 10 kHz - 200 kHz; a typical waveform is shown in Fig. 5.7. The results had been obtained by the PSPICE macromodel simulation. The response of the 3^{rd} order filter tuned at $f_0 = 1kHz$ shown in Fig. 5.9.

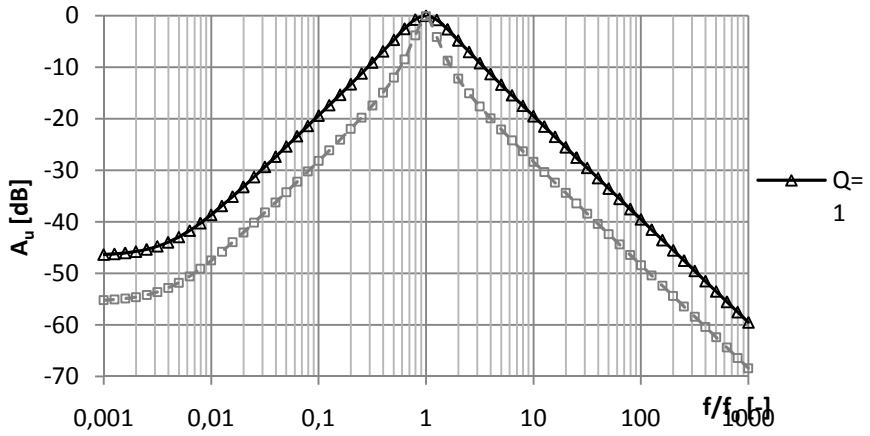


Fig. 5.7: Typical frequency response, LC resonator

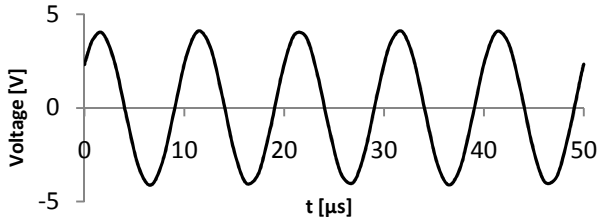


Fig. 5.8: Self-oscillator waveform

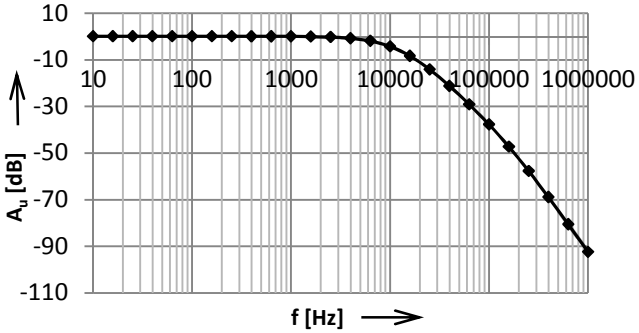


Fig. 5.9: Experimental response

Experimental results:

Fig. 5.7 - Frequency response obtained with a shunt - LC tuned for f_0 = 65 kHz at Q = 2.9 (with R = 7 kΩ) and Q = 1 (with R_x = 2.4 kΩ); R_1 = 1 kΩ, and C = C_x = 1 nF for L_{eq} = 6 mH.
Fig. 5.8 - Self-oscillatory waveform of LC tank circuit tuned at f_0 = 100 kHz.
Fig. 5.9 - Experimental response of the 3^{rd} order lowpass Butterworth characteristics.

5.9. SUMMARY

We have presented some CFA based circuit configuration for realizing high-quality imbalance function. These circuit synthesize, lossless inductance (L) and ideal supercapacitor (D) element, which are independently tunable. In the case of nonideal CFAs the compensation design equation has been derived for both the Land D type immittance functions. Both the Land D element can be varied independently by any one passive of the RC component. These simulation does not require any realizability conditions and the value of L or D may be tuned at extremely low active sensitivity.

Application of the L element in the design of high Q filter has also presented for verification of experimental results. The practical performance of the proposed BP filter circuit had been verified with continuous f_0 - tenability in the range of 100 kHz - 200 kHz at

a selectivity range $1 < Q < 10$, both hardware testing and PSPICE macromodel simulation have been carried out. In the realization lowpass Butterworth characteristics, the frequency response has been limited due to the limitation of OA.

It may be mentioned here that the usable frequency range of the proposed circuit may be significantly enhanced if the recently forwarded improved version OPA-695 CFA device is embedded in the circuits in place of AD-844. The new chip operates on single rail positive DC Bias and offers typical value of BW ≥450 MHz and slew rate = 4.3 kV/ μs with improved current mirror accuracy.

6. INTEGRATOR/DIFFERENTIATOR AND FILTER DESIGN

In the communication system, wave processing/ conditioning, by active – RC integrator/differentiator find wide application. These Integrators and Differentiator are involving active devices like the voltage operational amplifier (OA) and current conveyer (CC). Several active Integrators/ Differentiators circuit using OA [21, 22], OTA [21] and CC [12 - 20] have been developed in the pas.

The design of analog signal processing circuits and system in current mode is receiving attention at present. The current mode circuit offer substantive improvements over the voltage mode ones relative to linearity and bandwidth.

Usually these designs were carried out in the recent past using the voltage controlled current source (VCCS) or current conveyor (CC) element. Here CFA has been for this purpose.

The literature presents a number of integrator schemes using two or three CFAs. Some of these realizations are based on selection of design parameters with external discrete RC-components, while recently some are proposed utilizing the CFA device transimpedance. It is seen that the usable frequency range of such circuits can be significantly enhanced by taking into consideration the transimpedance elements in the analysis. Previously some CFA based single and dual input circuits with passive tuning of the time constant for the realization of Integrator and Differentiators have been made.

In this chapter, first we propose new dual input integrator using CFA device .next we propose a simplified version of integrator and differentiator using a single CFA. The CFA provides both current source (z-port pin#5) and voltage source pin (#6) for easy cascadibility.

Analysis has been made using the practical CFA model (e.g. AD 844) with finite port errors ($\in$ #0). The circuits use a single resistor or capacitor without the need of large spread of passive components to tune the time constant (τ). The value of τ changes slightly to τ' due to the device imperfection. Subsequently compensation design equations have been derived for correcting the imperfection. The sensitivity analysis also reveals a low value.

The single –CFA configuration had been designed for a range of signal processing/generation function on the same topology .the analysis has been carried out utilizing the y- port parasitic element s and the z-port transadmittance of the CFA. The design equations had been derived for extended- range frequency operation (1 MHz - 30 MHz) for realizing the functions of:

- Ideal inverting integrator/differentiator,
- Filters (BP, LP, HP) with high-selectivity (Q≥ 20),
- Sinusoid Oscillator circuit.

The tuning parameters, e.g., time-constant (τ), selectivity (Q) and resonant/oscillation frequency (ω_0) may be varied by single R or C components. The performance on time-domain and frequency-domain processing of appropriate input signals, square/triangular wave for integrator/differentiator and sine wave for the filters have been verified by PSPICE macro model simulation and hardware implementation. Some simulated are included.

6.1. NEW DUAL INPUT INTEGRATOR

Next we present the derivation of two current mode structures which are derivable conveniently from those in Fig. 6.1 and Fig. 6.2.

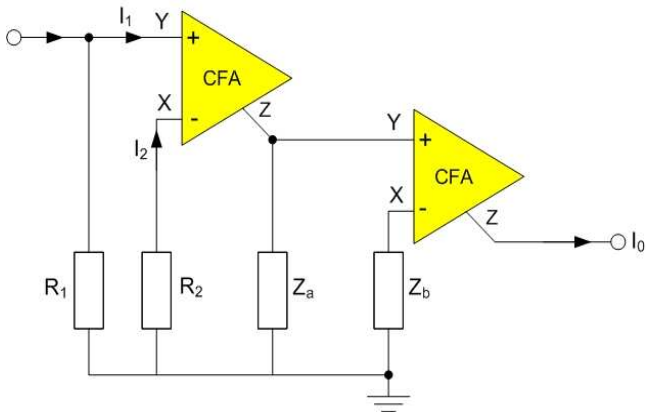


Fig. 6.1: Dual - input diferentiator ratio function (Z_b / Z_a)

$$H(P) = I_0 / I_d = Z_a / Z_b, \quad R_1 = R_2$$

Integrator, $Z_a = 1/pc, Z_b = Z$

Differentiator, $Z_a = R, \quad Z_b = 1/pc$

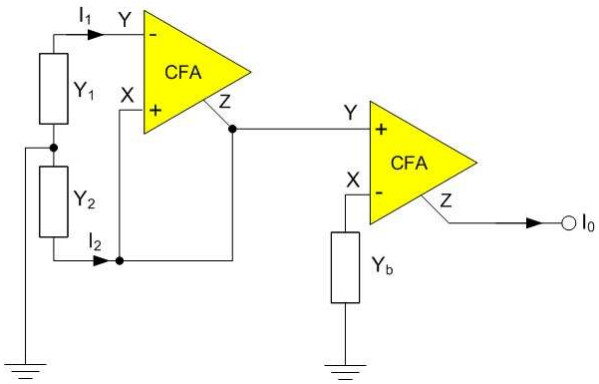


Fig. 6.2: Dual - input integrator ratio function (Z_b / Z_a)

$$H(P) = I_0 / I_d = Y_b / Y_a \qquad Y_2 = Y_1 + Y_a$$

Integrator, $Y_a = pc$, $Y_a = pc$,

Differentiator, $Y_a = 1/R$, $Y_b = pc$

Analysis for Fig. 6.1 yields the output current (I_0)

$$I_0 = a_1 a_2 \beta_2 (k\beta_1 I_2 - I_1) \qquad (Z_a / Z_b) \tag{6.1}$$

where k = R_2/R_1

With ideal CFAs where $\alpha = \beta = \delta = 1$ we get true differential input ($I_d = I_2 - I_1$) current transfer from eq. (6.1), with the realizability design of k = 1, Fig. 6.1 as

$$H = I_0 / I_d = Z_a / Z_b \tag{6.2}$$

Hence with $Z_a = 1/pC$ and $Z_b = R$, one gets an integrator function

$$H(p) = 1/p\iota, \qquad \iota = RC \tag{6.3}$$

Interchanging the R and C components, a differentiator function is obtained

Similar analysis for fig 3.2 (b) yields

$$I_0 = \frac{\alpha_2 \beta_2 y_b}{y_2 - \alpha_1 \beta_1 y_b}(I_2 - \alpha_1 I_1) \tag{6.4}$$

With ideal CFAs, we get

$$H = I_0 /(I_2 - I_1) = \frac{y_b}{y_2 - y_1} \tag{6.5}$$

Selecting $y_2 = y_a + y_1$ as realizability design, we get a ratio function

$$H = y_b / y_a \tag{6.6}$$

Here taking $y_a = pC$ and $y_b = I / R$, we have an integrator, and interchanging R and C, we get a differentiator, both with $\tau = CR$. Here must be taken as $y_{1.2} = 1/r_{1.2}$

The effects of CFA port-errors in Fig. 6.1 have been examined and subsequently, the modified expressions are derived. It may be concluded that both configurations in Fig. 6.1 and Fig. 6.2 provide dual-input capability on differential current (I_d) signal. The circuit of fig. Fig. 6.2, this input signal is modified to $I_d = I_2 - I_1(1 - \in_{i1})$, where I_1 signal is slightly reduced in magnitude. Both configurations realize ideal current mode integrator/differentiator function with signale-tunable time constant (ι) by (R or C). The effects of the CFA port errors $(\in_{i,v,z} << 1)$ can be precisely compensated. The relevant compensation design equation is shown in Tab. 6.1.

Tab. 6.1: Modified design equations for new dual-input current-mode integrator/differentiator realization in Fig. 6.1 and Fig. 6.2

Fig 3.1.	Output current	Realizability
(a)	$I_0 = (1-\epsilon_1)(Z_a/Z_b)\{(1-\epsilon_{I_1})kI_2 - I_1\}$ $\epsilon_1=\epsilon_{1_1}+\epsilon_{I_1}+\epsilon_{v_2}$	$k = r_2/r_1 = 1/(1-\epsilon_{1_1})$
(b)	$I_0 = \frac{1-\epsilon\, x_2 y_b}{y_2-(1-\epsilon_{x_1})y_1}\widetilde{I_d}$ $\widetilde{I_d} = I_2 - I_1(1-\epsilon_{i1})$ $\epsilon_{x2}=\epsilon_{I2}+\epsilon_{v2}$ $\epsilon_{x1}=\epsilon_{I1}+\epsilon_{v2}$	$y_2 = y_a + y_1(1-\epsilon_{x4})$

Fig 3.1.	Modified Expressions			Compensation Design	
	Current Transfer H	Integrator	Differentiator	Integrator	Diferentiator
(a)	$I_0/I_d = (1-\epsilon_1)Z_a/Z_b$ $I_d = I_2 - I_1$	$\widetilde{H} = 1/\widetilde{s\tau}$ $\tilde{\tau} = \widetilde{R}C$ $\widetilde{R} = R/(1-\epsilon)$ $Z_a = 1/sC$ $Z_b = R$	$\widetilde{H} = 1/s\tilde{\tau}$ $\tilde{\tau} = R\widetilde{C}$ $\widetilde{C} = C/(1-\epsilon)$ $y_a = 1/R$ $y_b = sC$	$R_c = R/\epsilon$ Parallel to R	$C_c = \epsilon_i\, C$ Parallel to C
(b)	$I_0/\widetilde{I_d} = (1-\epsilon_{x2})(y_b/y_a)$ $\widetilde{I_d} = I_2 - I_1(1-\epsilon_{i1})$	$\widetilde{H} = 1/s\tilde{\tau}$ $\tilde{\tau} = R\widetilde{C}$ $\widetilde{R} = R/(1-\epsilon_{x2})$ y_a=sC $y_b = 1/R$ $y_1 = g$ $y_2 = sC + g$ $\tilde{g} = g(1-\epsilon_{x1})$	$\widetilde{H} = 1/s\tilde{\tau}$ $\tilde{\tau} = R\widetilde{C}$ $\widetilde{C} = C(1-\epsilon_{x2})$ y_a=1/R $y_b = sC$ $y_1 = 1/r$ $y_2 = R^{-1} + \epsilon_{x1}\, r^{-1}$	$R_c = R/\epsilon_{x2}$ Parallel to R	$C_c = \epsilon_{x2}$ Parallel to C

6.2. SENSITIVITY FOR DUAL INPUT INTEGRATOR

The active sensitivities relative to the CFA imperfections of the time-constant may be calculated on the residues of the negative-real (ι) pole/zero. It shows single resistor/capacitor tenability at low sensitivity and realization of the pole/zero at the origin [114].

The classical sensitivity figure is defined as $S_a^{\ b} = (db/b)/(da/a)$. The active τ-sensitivity figures are calculated after normalizing all passive components equal to unity; for all the circuits in Fig. 6.1 and Fig. 6.2, the sensitivity figures are

$$\left.\begin{bmatrix}\tilde{\tau} \\ S_{\in_{i,v}}\end{bmatrix} = \frac{\in_{i,v}}{\in_i + \in_v} \qquad \begin{bmatrix}\tilde{\tau} \\ S \in_0\end{bmatrix} = \frac{\in_0}{1+\in_0}\right\} \quad << 1 \tag{6.7}$$

Hence the proposed networks exhibit extremely low active-sensitivity.

In the case of non ideal CFA, the circuit has been reanalyzed and we get,

$$I_0^{\ \prime} = (K' I_2 - I_1)(n.\frac{Z_2}{Z_1}) \tag{6.8}$$

where

$\frac{K'}{K} \cong 1+\in_{i1} -\in_{v2}$ and $n \cong 1-(\in_{i1} +\in_{iz} +\in_{v2})$

The design equation for differential reliability now becomes

$$K' = 1 \text{ i.e } r_1 = (1+\in_{i1} -\in_{v1}) \ r_2 \tag{6.9}$$

so, τ changes to $\tau' = \frac{RC}{n}$

6.3. COMPENSATION FOR DUAL INPUT INTEGRATOR S

The alteration of τ due to CFA errors call for appropriate compensation so that its nominal value may be reset.

When n<1, $\tau' > \tau$ and R(= Z_1) increases by $\frac{R}{n}$

This increment may be reduced by a parallel compensating resistor (RC) formulated by

$$G_c + nG = G$$

Here the compensation design is

$$R_c = R / \in_{i1} + \in_{iz} + \in_{v2}$$

For the differentiator, $Z_1\left(=\frac{1}{pC}\right)$ should be shunted by a compensating capacitor

$$C_C = (\in_{i1} + \in_{iz} + \in_{v2})^C$$

The active τ-sensitive sensitivities may, in general, be expressed by

$$S^{\tau}_{r} = \in / \{1 - \sum \in\} << 1,$$

where denotes the CFA errors.

6.4. SINGLE - CFA STRUCTURE

The proposed configuration is shown in Fig. 6.3.where routine analysis using the CFA port relation $i_z = i_x, v_x = v_y$, and $i_z = i_x, v_x = v_y$ yields the transfer

$$V_0 / V_i(p) = H(p) = \frac{Y_1}{(Y_A + Y_B) - [Y_1 + Y_y + Y_3 + Y_Z + \{(Y_1 + Y_Y)(Y_3 + Y_z)/Y_2\}]} \qquad (6.10)$$

Where $Y_{y,z}$ denote the y-port parasitic input- admittance and the z-port transadmittance elements of the device ; both of these appear in the form of shunt-RC arms, defined as

$Y_{y,z} = G_{y,Z} + pC_{y,z}$ where G is transconductance. Typical value for these components are $R_y = 1/G_Y = 2M\Omega, C_y = 3pF, R_z = 1/G_z = 4M\Omega$ and $C_Z = 6\,pF$. For an ideal device the parasitic capacitors are extremely small $(C_{y,z} \to 0)$ thus dragging the attenuating poles to infinity. Some earlier designs were presented using this assumption which had been found to be suitable for relatively low-frequency applications. Recently the implementation of sinusoid oscillator using the nominal CFA model of the two current conveyors, along with some discussions on the device parasitic had been proposed [87].

6.5. INTEGRATOR/DIFFERENTIATOR

Active RC integrator/differentiator circuit have been found to be quit useful for various signal conditioning and wave processing application in the fields of instrumentation/communication [51-55]. Here we present the design of such functions suitable for relatively high-frequency applications using a simple single - CFA topology. The nominal design of an inverting integrator is obtained in the circuit of Fig. 6.3., initially after assuming $Y_{y,z} = 0$ and selecting $Y_A = Y_1 = G_1, Y_2 = G_2$ and $Y_B = Y_3 = pC$ as shown in Fig. 6.3.

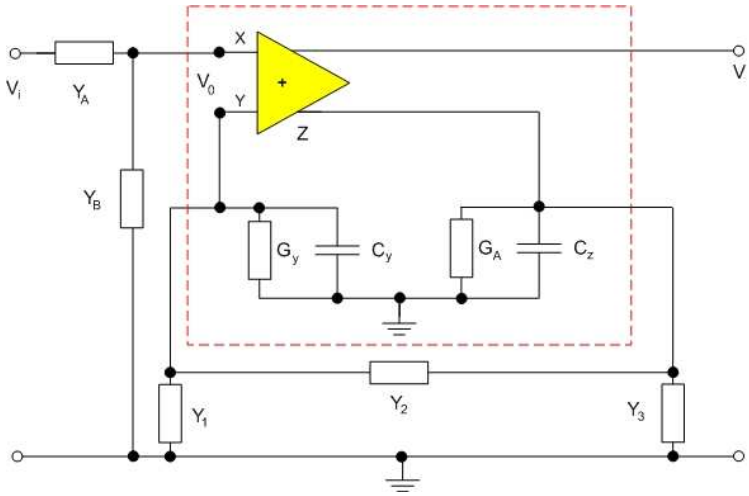


Fig. 6.3: Single-CFA multifunction structure the input port parasitics $Y_y = G_y + pC_y$ and transadmittance $Y_Z = G_z + pC_z$

The transfer is

$$-H_i(p) = G_2 / pC = 1/ p\mathrm{T}_i, \quad \mathrm{T}_i = R_2 C \tag{6.11}$$

The time-constant is adjustable independently by R_2.

For an inverting differentiator as in Fig. 6.5., we take

$Y_A = Y_1 = G_1$, $Y_B = Y_3 = G$

and

$Y_2 = pC$ which yields.

$$-H_d(p) = -p\mathrm{T}_d, \quad \mathrm{T}_d = R_2 C \tag{6.12}$$

Where T_d is adjustable by C.

The effects of the parasitics/transadmittance elements on the quality of these functions may now be derived after substitution of the values of $Y_{y,z}$ in eq.(6.10); one then gets

$$\frac{V_0}{V_i(p)} = -H_i(p) = \frac{G_1 G_2}{p^2 C_y (C + C_z + p\{g_1(C + C_z) + G_z C_y + G_2 C_\mathrm{T}\} + G_2 G_1 + g_1 G_z} \tag{6.13}$$

where $C_\mathrm{T} = C_y + C_z$, $G_\mathrm{T} = G_y + G_z$ and $g_1 = G_1 + G_y \approx G_1$.

Realization of integrator and differentiator, see Fig. 6.4. bellow:

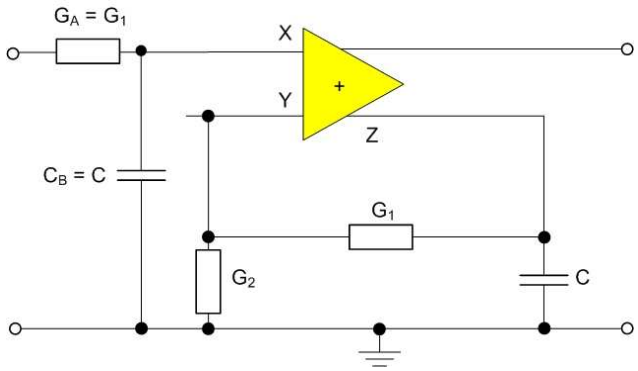


Fig. 6.4: Inverting integrator with time constant $T_i = CR_2$

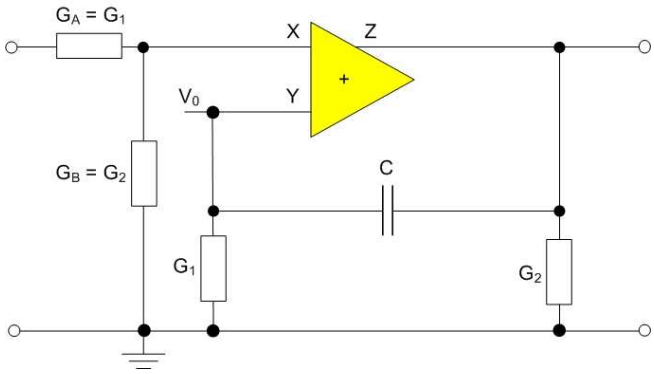


Fig. 6.5: Inverting differentiator with time constant $T_d = CR_2$

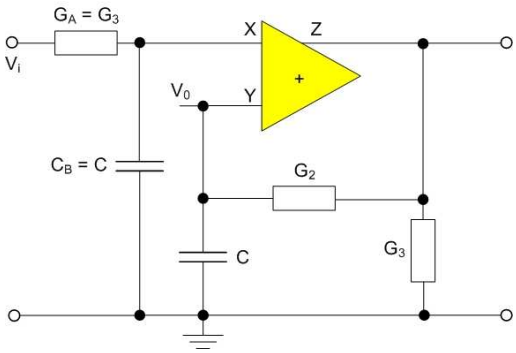


Fig. 6.6: Another integrator with same T_i

The quality (q_i) of an inverting integrator may be defined by writing

$$\left.\begin{aligned} & H_i(\omega) = [m(\omega)]^{-1} \\ & \textit{and} \qquad q_i(\omega) = n(\omega)/m(\omega) \end{aligned}\right\} \tag{6.14}$$

Combining (6.13) and (6.14) one gets

$$n(\omega) = \omega\omega_n(C/C_y)[1+(G_2C_{\mathrm{T}}/G_1C)+(G_zC_y/G_1C)]$$

$$\left.\begin{aligned} & n(\omega) = \omega\omega_n(C/C_y)[1+(G_2C_{\mathrm{T}}/G_1C)+(G_zC_y/G_1C)] \\ & \approx \omega\omega_n(C/C_y) \qquad , \qquad \omega_n = G_1/C_{\mathrm{T}} \end{aligned}\right\} \tag{6.15}$$

Since $C_{y,z} << C$ and $G_z << G_1$. Also we have

$$\left.\begin{aligned} & m(\omega) = \omega_P{}^2 - \omega \\ & \textit{where} \qquad \omega_p{}^2 = (G_1G_z + G_2G_{\mathrm{T}})/C_y(C+C_z)_{\mathrm{T}} \end{aligned}\right\} \tag{6.16}$$

For high-frequency applications $\omega >> \omega_p$, hence

$$q_i(\omega) = C\ \omega_n/C_y\omega >> 1 \tag{6.17}$$

An alternate design of inverting integrator with a similar quality-factor is shown in Fig.6.6.

For the differentiator in Fig.6.5. we can write

$$\frac{V_o}{V_i(p)} - H_d(p) = \frac{pCG_1}{p^2(C_yC_z + CC_T) + p(CG_T + C_yg_2 + C_zg_1) + g_1g_2} \qquad (6.18)$$

The quality of the inverting differentiator may be obtained by writing

$$\left.\begin{aligned} -H_d(\omega) &= u(\omega) + jb(\omega) \\ and \qquad q_d(\omega) &= b(\omega)/u(\omega) \end{aligned}\right\} \qquad (6.19)$$

Here we have

$$\left.\begin{aligned} b(\omega) &= \omega_b{}^2 - \omega^2 \\ u(\omega) &= \omega\omega_T \end{aligned}\right\} \qquad (6.20)$$

Where

$$\left.\begin{aligned} \omega_b{}^2 &= \frac{g_1g_2}{C_yC_z + CC_T} \approx \frac{G_1G_2{}^2}{CC_T} \\ and \qquad \omega_T &= \frac{G_T}{C_T}[1 + (G_2C_y/CG_1) + (G_1G_z/G_TC)] \approx G_T/C \end{aligned}\right\} \qquad (6.21)$$

If we write $W_t = 1/R_1C_T$ and $T_d = R_2C$, then $\omega_b{}^2 = \omega_t/T_d$. Calculations with typical parasitic values and nominal time-constant value for usability in the MHZ range, indicate that usually $\omega << \omega_t/T_d$; hence

$$q_d(\omega) = \omega_b{}^2/\omega\omega_T >> 1 \qquad (6.22)$$

Thus while R_2 controls the time-constant (T_d), the ratio G_1/G_T may be adjusted through R_1 to obtain high quality differentiation at relatively higher frequency bands.

6.6. FILTER DESIGN

The same circuit topology in Fig. 6.3. is able to realize high-selectivity tunable resonant filters with appropriate choice of RC component along with the use of the device-transadmittance. A high-pass (HP) filter may be designed with $Y_A = pC_A$, $Y_B = G_B$ and , $Y_1 = G_1$, $Y_2 = pC_2$ and $Y_3 = G_3$ as shown in Fig. 6.7.; this yields

$$-V_o/V_i(p) = H_h(p) = \\ = \frac{p^2 C_A C_2}{p^2\{C_y C_Z + C_2(C_T - C_A)\} + p[g_1 C_2 + g_3 C_y + C_2(G_1 + G_3 + G_T - G_B) + g_1 g_3]} \quad (6.23)$$

Where $g_1 = G_1 + G_y$ and $g_3 = G_3 + G_z$.

The filter parameters are

$$\omega_0 = \left\{\frac{g_1 g_3}{C_y C_z + C_2(C_T - C_A}\right\}^{1/2} \approx \left\{\frac{G_1 G_3}{C_2(C_T - C_A}\right\}^{1/2} \quad (6.24)$$

$$\text{and} \quad Q = \frac{\omega_o C_2(C_T - C_A)}{g_1 C_z + g_3 C_y + C_2(G_1 + G_3 + G_T - G_B)} \quad (6.25)$$

since $C_{y,z}$ are small, they may be neglected and the design equations may be simplified, after assuming equal-value resistors $G_1 = G_3 = G = 1/R$, then

$$\left.\begin{aligned} &\omega_0 = G/\sqrt{\{C_2(C_T - C_A)\}} \\ &and \qquad Q = \{(C_T - C_A)/C_2\}^{1/2}/[2 - (R/R_B)] \end{aligned}\right\} \quad (6.26)$$

Thus while the center-frequency (f_0) may be set by C_A to a prescribed value, the selectivity (Q) may be adjusted by R_B. A bandpass (BP) filter characteristics in the same circuit is obtained by interchanging C_A and R_B as shown in Fig. 6.8.. The BP-transfer is obtained as

$$-H_b(P) = (pC_2 G_A/G_1 G_3/D(S) \quad (6.27)$$

Where the denominator polynomial is the same as in (14) and filter parameters (f_0, Q) are same as in (6.26).The lowpass (LP) filter is shown in Fig. 6.9.; the LP transfer is analyzed to be

$$-H_t(p) = \frac{G_A G_2}{p^2 C_y C_z + p[C_z(G_1+G_2+G_y)+C_y(G_2+G_3+G_z)-C_B G_2]+g_1 g_3+G_2(g_1+g_3-G_A)} \tag{6.28}$$

Here the parameters

$$\left\{\frac{g_1 g_3 + G_2(g_1+g_3-G_A}{C_y C_z}\right\}^{1/2} = \left\{\frac{G_1 G_3 + G_2(G_1+G_3-G_A}{C_y C_z}\right\}^{1/2} \tag{6.29}$$

$$\text{and} \quad Q = \frac{\omega_0 C_y C_z}{(G_1+G_2+G_y)C_z + (G_2+G_3+G_z)C_y - G_2 C_B} \tag{6.30}$$

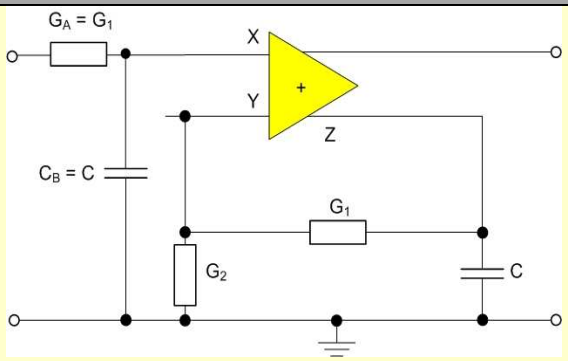
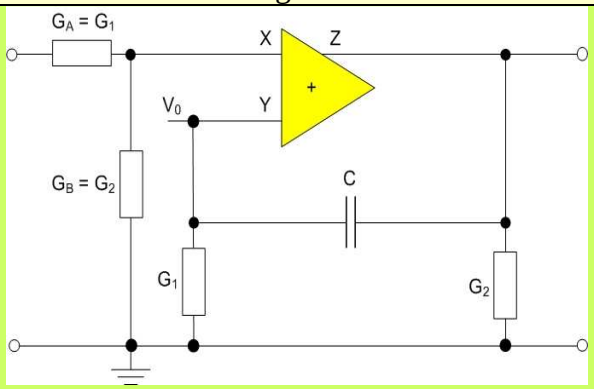
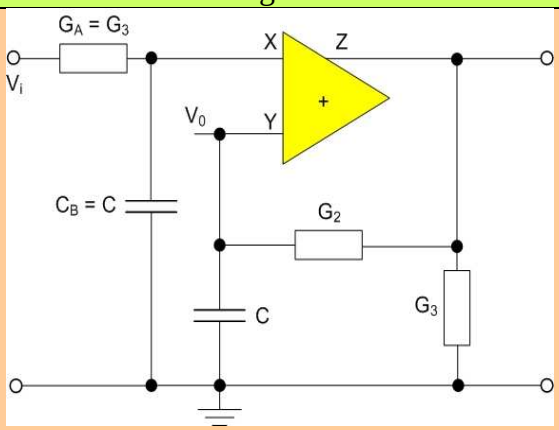
One may simplify by taking $G_{1,2,3} = G = 1/R$ which gives

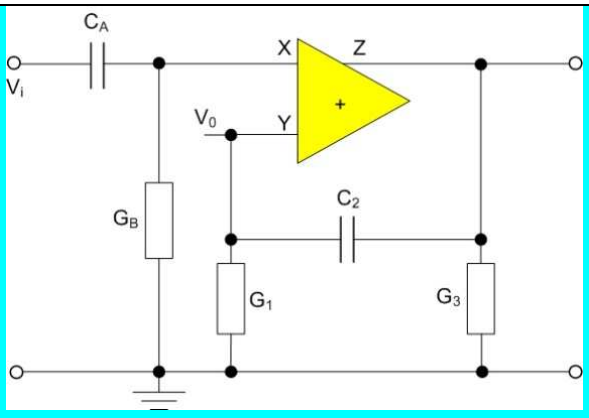
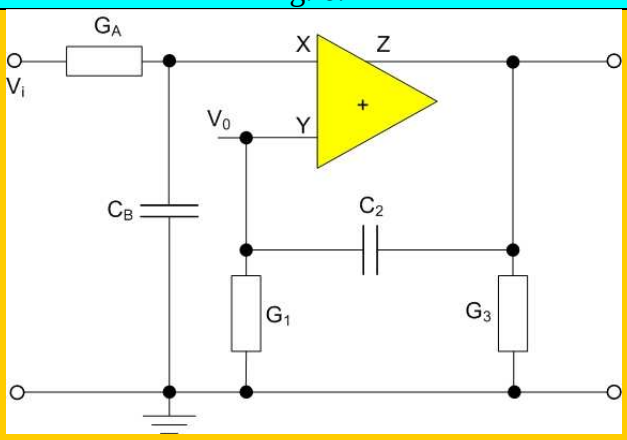
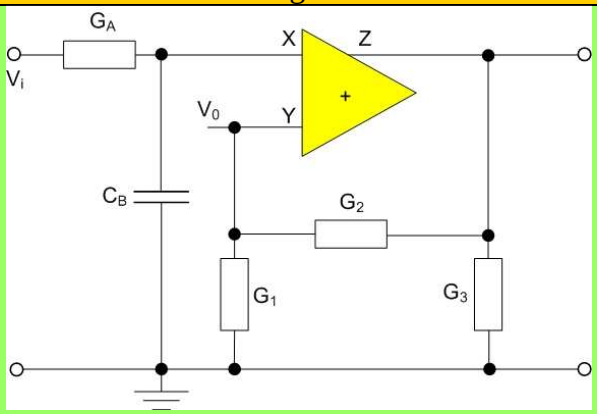
$$\omega_0 = G[(3-K_l)/C_y C_z]^{1/2} \ , \ K_l = R/R_B \tag{6.31}$$

$$\text{and} \quad Q = [(3-K_l)C_y C_z]^{1/2}/(2C_{\mathrm{T}} - C_B) \tag{6.32}$$

It is that in theses filter design schemes, high-Q response could be obtained by adjusting a resistor-ratio (for HP and BP), or by selecting an appropriate capacitor - value with respect to the parasitic capacitance (for LP). The simplified from of all these equations are summarized in table Tab.6.2.

Tab. 6.2: Simplified Design Equations for the Multifunction Circuit

Fig.	function	Design / realizability eq.
 Fig.6.4	Integrator	$R_2 = 1/CT_i$ $R_1 = (C/C_y)/\omega C_{Tq_i}$
 Fig.6.5	Differentiator	$C = 1/R_2 Td$ $R_1 = R_p/\omega CR_2 q_d, R_p = 1/G_T$
 Fig.6.6	Integrator	$R_2 = 1/CT_i$ $\omega >> [R_y CC_z(R_2 \Vert R_3)]^{-1/2}$

 Fig. 6.7	HP Filter	$\frac{C_A}{C_T} = K_h = 1-(w_0 R C_T)^{-2}$ $R/R_B = \lambda_h = 2-[(1-K_h)^{1/2}/Q]$
 Fig. 6.8	BP Filter	$C_B/C_T = K_b = 1-(\omega_0 R C_T)^{-2}$ $R/R_A = \lambda_b = 2-[(1-K_b)^{1/2}/Q]$ if $G_1 = G_3 = 1/R$, $C_2 = C_T$
 Fig. 6.9	LP Filter	$R/R_A = K_t 3 - C_y C_z (\omega_0 R)^2$ $C_B/C_T = \lambda_t = 2-(\omega_0 C_e R/Q)$; $C_e = C_y C_z C_T$

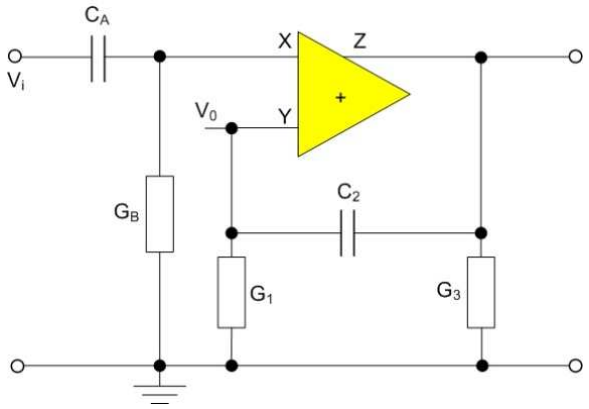


Fig. 6.7: Design of Highpass (HP)

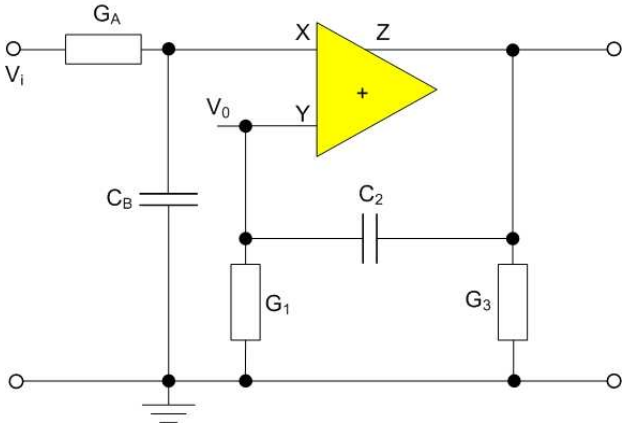


Fig. 6.8: Design of Bandpass (BP)

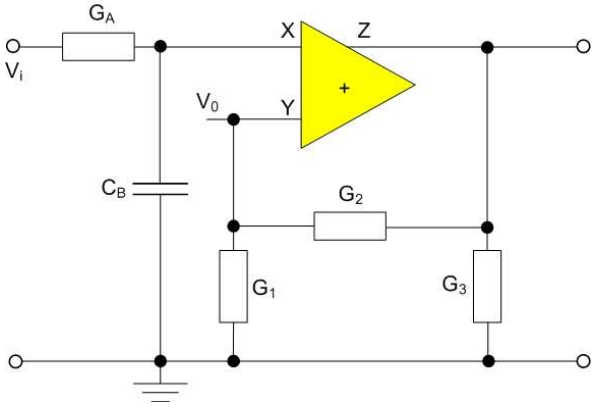


Fig. 6.9: Design of Lowpass (LP)

6.7. PORT MISMATCH AND SENSITIVITY

The effect of the tracking mismatch among the ports of the device may be evaluated in terms of the device may be evaluated in terms of the finite tracking errors (ε) of the CFA . For such a non-ideal device, the port relations are expressed as $i_y(1-\in_i)i_x$, $v_x=(1-\in_v)v_y$ and $V=(1-\in_0)v_z$. These errors introduce certain deviation from the nominal design leading to undesirable active-sensitivity of the filter parameters. the magnitudes of these errors, however, are quite small. $(.01 \le \in \le 0.4)$),and the sensitivities according are low, For an ideal device the errors vanish $(\in = 0)$.

Re-analysis assuming finite errors $\in \neq 0$ shows that the value of the filter parameters deviate slightly from the actual design value. For example, in case of the BP-realization of Fig. 6.8., we get the modified values as

$$\left.\begin{aligned} &\omega_0'/\omega_0=(1-K_b)/\{1-K_b(1-\in_i)\}, \qquad K_b=C_B/C\mathrm{T} \\ &and \qquad Q'=\omega_0' RC_e/\{2-\lambda_b(1-\in_t)\} \end{aligned}\right\} \qquad (6.33)$$

Where $C_e=C_yC_z/C_\mathrm{T}$ and $\in_t=\in_i+\in_v$, product of errors neglected.

We calculated the active- sensitivities based on the classical sensitivity figure

$$S_\in^{\,F}=(dF/F)/(d\in/\in)$$

these are

$$S_{\in_{i,v}}^{\;Q}=\in_{i,v}/(1-\in_t)<<1$$

$$S_{\in i,v}^{\;\omega_0}=0{,}5\in_{i,v}/(1-\in_t)<<0.5$$

and $$S_{\in_0}^{\;Q,\omega_0}=0$$

The proposed realizations are therefore practically active-insensitive-a feature desirable for microcircuit adaptation of the design.

6.8. EXPERIMENTAL RESULTS

All the proposed functions had been verified through hardware implementation and PSPCE macro model simulation. The internal parameters of AD-488 CFA device were measured to be $R_y = 3M\Omega$, $R_z = 5M\Omega$, $C_y = 3pF$ and $C_Z = 5.5\,pF$. The integrator/differentiator structures had been tested for time-domain response using square/triangular wave inputs respectively. Good quality response on wave conversion up to 5 MHz was obtained as shown in Fig. 6.10 and Fig. 6.11. We also measured the phase lag/lead response in the frequency-domain; phase-errors of less than 5% from the nominal value $(\pi/2)$ had been observed up to about 10 MHz.

The LP.BP and HP responses had also been verified; some typical simulated responses for responses for $f_0 = 23MHz$ at Q = 20 for the BP characteristics, and $f_0 = 10MHz$ at Q = 12 for the LP characteristics are shown in Fig. 6.12. and Fig. 6.13. The single element tenability of all these functions had been satisfactorily verified. The d.c power source used with the device was regulated 0 ± 12 V.d.c in all these tests.

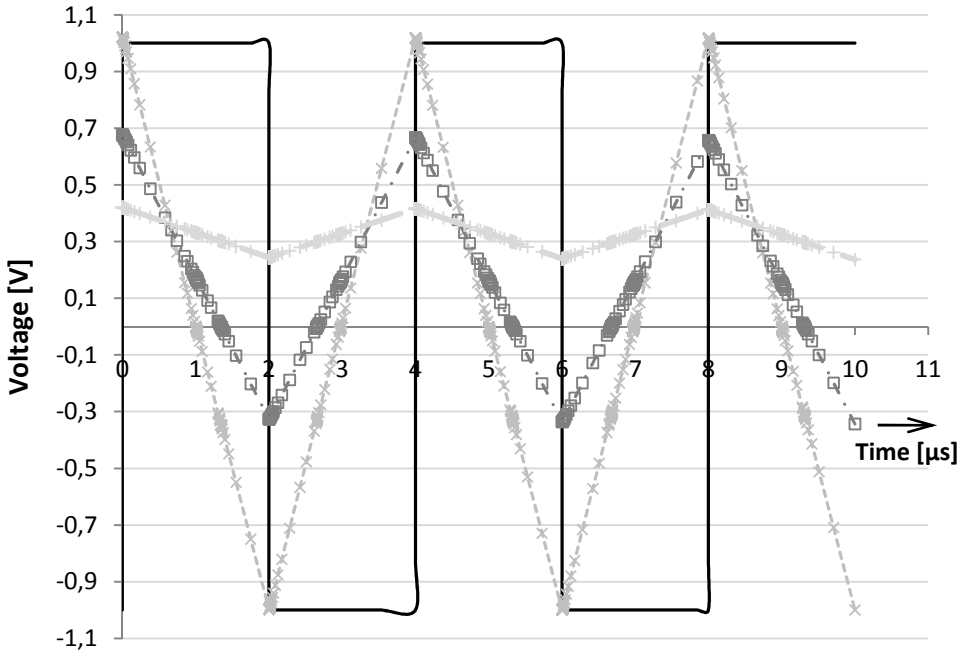


Fig. 6.10: Simulated response of integrator of Fig. 6.4. V_{ipp} = 2 V square wave at 1 Mhz. C = 100 pF, R_2 = 12 kΩ = R_A for q_i = 50

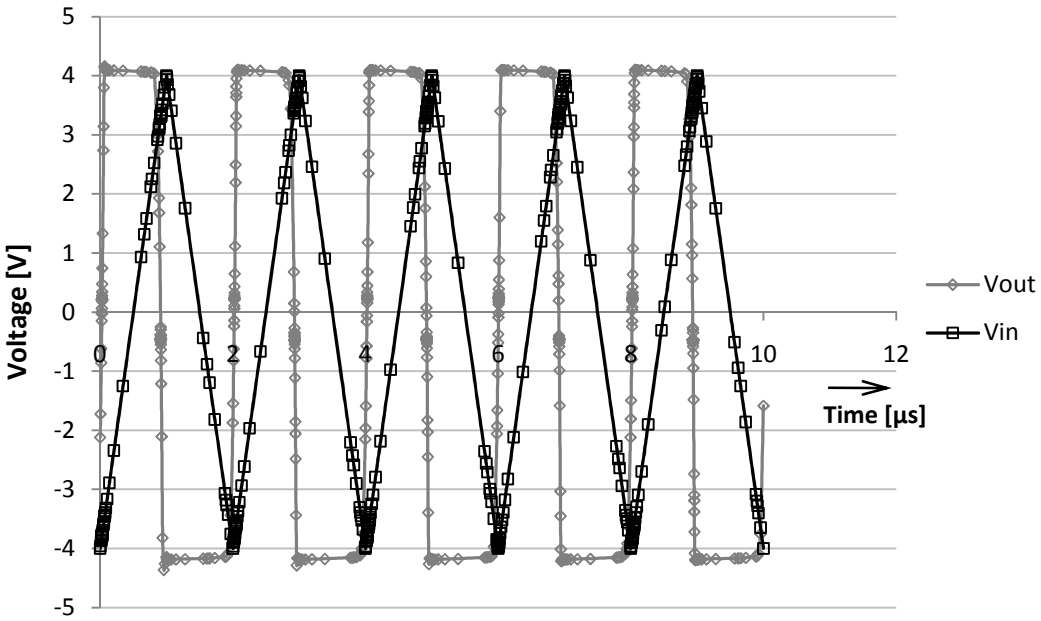


Fig. 6.11: Simulated response of differentiator Fig. 6.5.

V_{ipp} = 2 V triangular wave at 5 Mhz. C = 50 pF, R_2 = 23 kΩ = R_A for q_d = 50

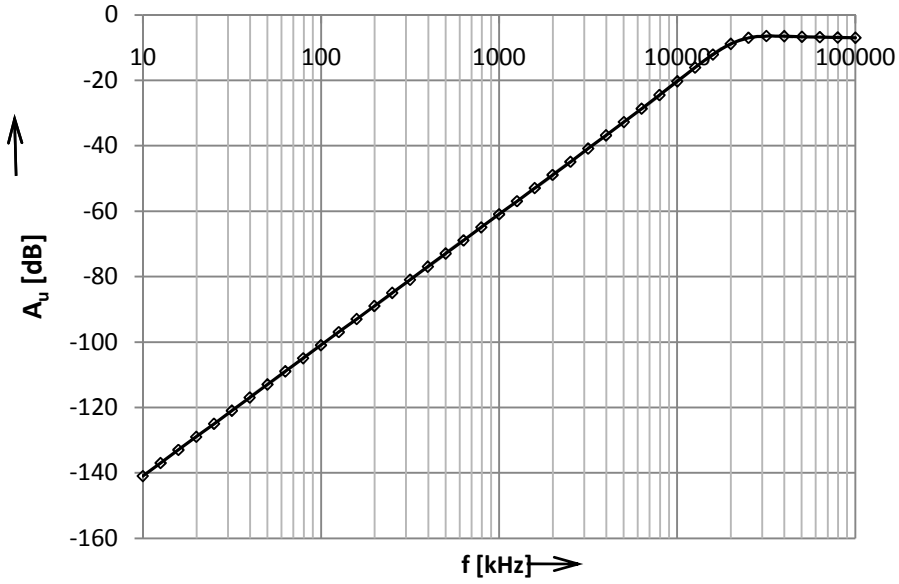


Fig. 6.12: Simulated response of HP characteristics $f_{O_{set}}$ = 23.5 MHz , Q_{set} = 20

Components: C_2 = 8.5 pF = C_T , C_A = 3 pF, R_1 = R_3 = R = 1 kΩ and R_B = 510 Ω

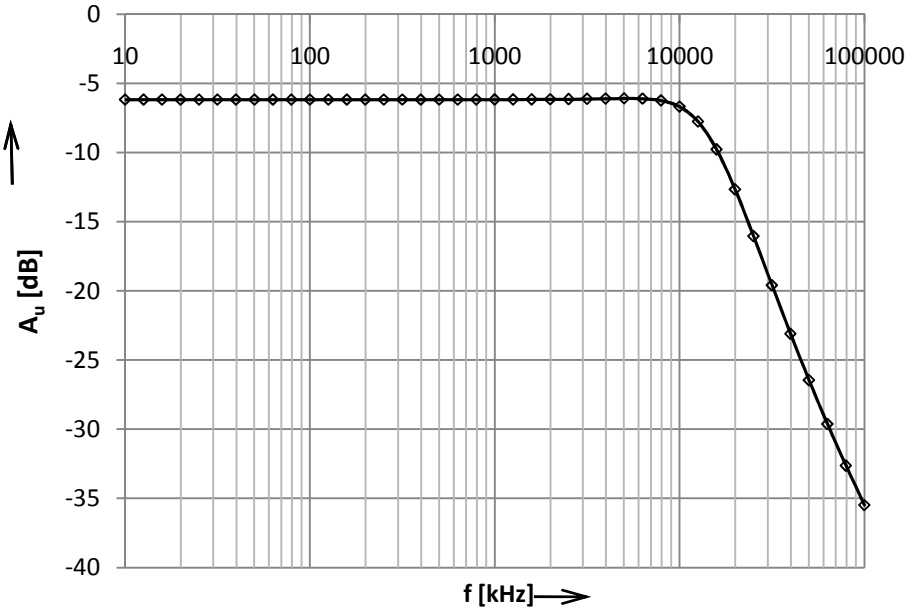


Fig. 6.13: LP characteristics: $f_{O_{set}}$ = 10 MHz , Q_{set} = 12
Components: C_B = 16.5 pF, $R_{1,2,3}$ = R = R = R_A = 5.6 kΩ

6.9. SUMMARY

In this chapter the CFA-based circuit topology suitable for realizing multifunction analog signal/wave processing capabilities with appropriate design. Detailed analysis for the realizability equations and the tuning-parameters, e.g., time constant (T) and quality (q) for integrator/differentiator, (ω_0) and selectivity(Q) for the filters are presented after taking into account the internal parasitic/transadmittance elements of the AD-844 type CFA device.Here by controlling the tuning component we observed a smooth variation of oscillation frequency upto 24 MHz, after utilizing the device transadmittance, in comparison to about 190 KHz. For a voltage source output in the proposed scheme, a wide-band buffer maybe cascaded. In our analysis, the series resistance (R_x) at the x-port had been neglected since it is quite small $(30\Omega - 40\Omega)$.

All the proposed functions had been experimentally verified in the frequency range of 1 MHz- 30 MHz with high Q-values $(Q \geq 20)$. Satisfactory wave conversion has been verified for the integrator/differ designs. Some typical simulated responses are included.

7. CURRENT MODE NONMINIMUM-PHASE ALLPASS FILTERS

The non minimum-phase all pass filters are useful for various phase processing applications such as correcting signal phase aberrations, phase recondition at a constant magnitude transmission over arrange of frequencies of interest.

In this chapter, we present a new design of current mod non minimum phase all filter using a current feedback (CFA). The type of filters have been realized in the past using operational amplifier (OA) and current conveyor (CCII) [5-9] devices for both voltage mode and current mode applications. But now the design of current mode analog signal processing circuits is gaining importance owing to certain advantages.

The CFA, AD-488 provides an advantage over the basic current conveyor element because of the low output impedance buffer between the z-port and the V_0 terminals, that allows the voltage (V_z) at z node to be accessed without affecting output current (I_0), which helps cascadability [31].

The current output stages of such advice can be designed with high accuracy (low tracking error) and with extremely large output impedance [21].

The CFA had recently been for the realization of magnitude selective filters. In this chapter we have utilized CFA to design, cascade current mode first and second order phase-selective all-pass with a simple active circuit topology. The effects of the device imperfections in view of finite tracking errors $(\in_{i,v} \neq 0)$ have been examined which shows slight deviations in the network parameters from the nominal values. It has been shown that even with nonideal CFA, the circuit realizes the nominal function but at a slight altered center-frequency.

We present here four schemes for the first order and two schemes for second order functions that can be generated from the basic topology. The design equations for all these realizations have been derived under both ideal and nonideal conditions. The active sensitivities in all these cases are been to be extremely low.

7.1. REALIZATION

Analysis of the proposed circuit in **Fig. 7.1** using eq.(7.1) and assuming ideal CFA we get the current transfer function $I_0 / I = F(p)$ as

$$F(p) = (y_1 y_4 - y_2 y_3)/(y_1 + y_2) y_4 \tag{7.1}$$

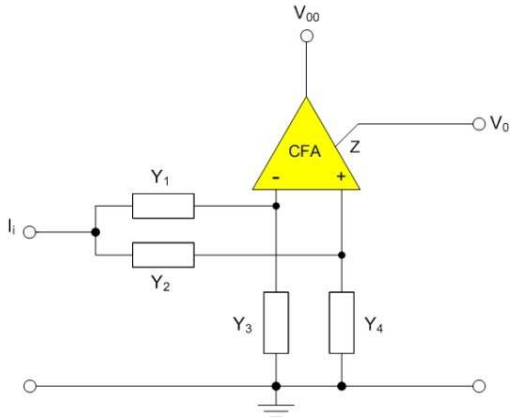


Fig. 7.1: Nonminimum phase network using a CFA.

Where $y_j (j = 1 to 4)$ are positive immittances to be chosen appropriately for obtaining the first and second order functions.

It may be mentioned that similar realizations of first order functions had been reported earlier [8] with an inverting CCII conveyor element. Here the additional advantage by the use of the CFA device is that a voltage signal (V_0) output at the follower, proportional to current output (I_0), could be obtained by resistive termination of the z-port without affecting (I_0), as it is being drawn from the current source node.

7.2. FIRST-ORDER FUNCTIONS

We have the following four first order functions by selecting the component set as listed in Tab. 7.1.

$$\left.\begin{aligned} F1(p) &= (1 - pk\tau)/D(s) \\ F2(p) &= (p\tau - k)/D(s) \\ F3(p) &= 1/2(1 - p\tau(k-1))/D(p) \\ F4(p) &= 1/2(p\tau - (k-1))/D(p) \end{aligned}\right\} \tag{7.2}$$

where nominal time constant $\tau = RC$ and $D(p) = (1 + p\tau)$.

The realizability conditions and phase variation for these functions are shown in Tab. 7.1. The gain is constant at unity for F1 and F2 while it is 0.5 for F3 and F4. It may be mentioned that F3 and F4 need one more resistor but the capacitor is grounded. Note that the CFA has voltage source output at node V_0 which is to be obtained, if desired, by passing I_0 through a suitable resistive load. This would provide a transimedance function corresponding to a constant resistance with phase shifting characteristics.

Tab. 7.1: Summary of first order function realizations

Function	Components						Relizability	Gain	Phase
	Z_1	Z_2	Z_3	Z_4	K	τ	k	F_0	φ
F1	R	$1/pC$	r_3	r_4	r_4/r_3	RC	1	1	0 to $-\pi$
F2	$1/pC$	R	r_3	r_4	r_4/r_3	RC	1	1	π to 0
F3	r_1	r_2	$\frac{(pR_3C+1)}{pC}$	R_4	R_4/R_3	RC $R_3 = R$	2	0.5 if $r_1 = r_2$	0 to $-\pi$
F4	r_1	r_2	r_3	$\frac{R_4}{(pR_4C+1)}$	R_4/R_3	RC $R_4 = R$	2	0.5 if $r_1 = r_2$	π to0

7.3. SECOND ORDER FUNCTIONS

We derive to alternative second order functions F5 and F6 from Fig. 7.1 by taking the following two sets of passive immittances.

$$y_1 = (p\tau + 1)/R\ ,\ y_2 = pC/(p\tau + 1)\ ,\ y_{3,4} = 1/r_{3,4} \qquad \textit{and} \qquad k = r_4/r_3 \quad (7.3)$$

$$y_{1,2} = 1/r_{1,2}\ ,\quad y_3 = pC/(p\tau + 1)\ ,\ y_4 = (p\tau + 1)/R \qquad \textit{and} \qquad \lambda = r_1/r_2 \quad (7.4)$$

Combining (1) and (2) we get the function in the form

$$F(p) = F_0 \frac{(p\varpi n_2)^2 - p\varpi n_1 + n_0}{(p\varpi d_2)^2 + p\varpi d_1 + d_0} \tag{7.5}$$

Where the coefficients of F5(p) and F6(p) corresponding to eq. (7.3) and eq. (7.4) Respectively are given below by eq. (7.6) and eq. (7.7)

$$\left.\begin{array}{l} n_1 = k - 2, n_2 = 1 \\ d_0 = 1, d_1 = 3, d_2 = 1, F_0 = 1 \end{array}\right\} \tag{7.6}$$

and

$$\left.\begin{array}{l} n_0 = 1, n_1 = \lambda - 2, n_2 = 1 \\ d_0 = 1, d_1 = 2, d_2 = 1, F_0 = 1(1 + \lambda \end{array}\right\} \tag{7.7}$$

Equation (7.5) yields an allpass (AP) function with $n_1 = d_1$ and additional band-reject functions (BR) with $n_1 = 0$. These realizability conditions for F5(p) are F6(p) are given by eq.(7.8) and eq. (7.9) respectively as

$$\text{K (AP) =5} \qquad \text{k (BR) =2} \tag{7.8}$$

$$\lambda\text{(AP)=4} \qquad \lambda\text{(BR) =2} \tag{7.9}$$

Note that F6(p) realized by component set of eq. (7.4) has equal-value grounded capacitor. The phase shift for both F5 and F6 are lagging. The phase responses may be expressed in terms of the normalized frequency parameter u= (ω/ω_0) as

$$\begin{array}{l} \phi 5(u) = 2\arctan\{3u/(1-u)^2\} \\ \phi 6(u) = 2\arctan\{2u/(1-u)^2\} \end{array} \tag{7.10}$$

Both these variation are in the range (lagging) of $0 \le \phi_{5,6}(s) \le 2\pi$.

7.4. EFFECTS OF CFA NON- IDEALITIES

Reanalysis of Fig. 7.1 assuming a non-ideal CFA $(\in \neq 0)$ modifies eq.(5.1) to

$$F = (1-\varepsilon_i)\frac{y_1 y_4 - b y_2 y_3 + \varepsilon_v y_1 y_2}{y_4(y_1 + y_2) + \varepsilon_v y_1 y_2} \tag{7.11}$$

the nominal function F_j ($j = 1$ to 6) will be modified which we examine next

7.5. MODIFIED FUNCTION

Reanalysis with eq.(7.11) for the realization of F_1 yields

$$\tilde{F}1(p) = (1-\varepsilon_i)\frac{1 - p\tau k(1-\varepsilon_v) - m\varepsilon_v}{1 + p\tau(1+m\varepsilon_v} \tag{7.12}$$

where $m = r_4 R$

The modified design equation is

$$k = \frac{1 + 2m \in_v}{1 - \varepsilon_v} \tag{7.13}$$

This may be simplified after writing $(1-\in_v)^{-1} \approx (1+\in_v)$, since $\in_v << 1$, and then neglecting products of errors, given by

$$k \cong (1 + 2m \in_v)(1 + \varepsilon_v) \tag{7.14}$$

which yields

$$r_3 = \frac{r_4}{1+\in_v (1+2r_4/R)} \tag{7.15}$$

In practice, if one selects $r_4 = R$, this further reduces to

$$r_3 = R/(1+3\in_v) \tag{7.16}$$

which may be set precisely. We observe that with an ideal CFA ($\in_v = 0$) this equation reduces to the nominal design of $k = 1$.

Substitution of eq.(7.13) in eq. (7.12) gives

$$\tilde{F}1(p) = (1-\in_i)(1-p\tilde{\tau})/(1+p\tilde{\tau}) \tag{7.17}$$

$$\text{Where} \quad \tilde{\tau} = C(R+\in_v r_4) \tag{7.18}$$

Equation (7.17) indicates that even with a nonideal CFA the circuit is able to realize the allpass functions but at a slightly altered center-frequency. The voltage error (ε_v) alters only the time constant

Similarly we get F_2 changing to

$$\tilde{F}2(p) = (1-\in_i)\frac{p\tilde{\tau}(1-\varepsilon_v)}{1+p\tilde{\tau}} \tag{7.19}$$

and

$$\tilde{k} \cong 1/(1-\in_v) \cong (1+\in_v) \tag{7.20}$$

The effects of the CFA imperfections on the other two first order functions F3 and F4(p) and on the second order functions F5 and F6 have also been examined which are listed in **Tab. 7.2**. It may be mentioned here that for F6 one gets differing values of ω_p and ω_z since

$$\tilde{d}_0 = 1 - p\in_v \text{ and } \tilde{n}_0 1 + (P\in_v /(1+\lambda) \qquad (7.21)$$

This difference may be insignificant if we note that $\in_v << 1$ and may be further eliminated if r_2 is scaled to a relatively high value ($P = R/r_2 << 1$) such that the quantity $p\in_v$ can be extremely small leading to $\tilde{d}_0 = 1 = \tilde{n}_0$. The design equation are then $\lambda(Ap) = 4/(1-\in_v) \cong 4(1+\in_v)$ and $\lambda(BR) = 2/(1-\in_v) \cong 2(1+\in_v)$.

7.6. SENSITIVITY

The sensitivity figures are obtained by $S = (\Delta y/\Delta x)(x/y)$. It is seen that the time constant (τ) and hence ω_0 are affected by $\in_v$ while gain factor F_0 is affected by $\in_i$. The deviation in phase response is concomitant to that of τ. The active sensitivities are

$$S_{\in_{v\in}}^{\tilde{\tau}} = \in v/(1-\in v) << 1; \quad S_{\in i}^{\tilde{F}_0} = \in i/(1-\in) << 1, \quad S_{\in_v}^{\tilde{\tau}} = 0 = S_{\in vi}^{\tilde{F}_0} \qquad (7.22)$$

The proposed realizations therefore be considered as active insensitive.

As the CFA device may be considered of high output impedance current follower stage cascaded by a low output impedance voltage follower, these sensitivities can be interpreted in terms of the actual deviation in their port transfer ratios from the nominal value of unity. To this end, it may be observed in the recent literature that quite accurate and wide band designs of such stages with extremely low errors ($\in_i < 0.5\%$) and unity gain-bandwidth values in excess of 100 MHz have been reported. Very low offset-error wide band voltage followers are also available. Hence the above sensitivity figures imply practically active insensitive characteristics for the proposed configuration.

The passive sensitivity may be evaluated by the fractional change is expressed by

$$(\Delta\tau/\tau) = \sum(\Delta R/R)(S^{\tau}.R) + \sum(\Delta C/(S^{\tau}.C)$$

Where the sum extends over the number of R and C used. It may be seen that

$$\sum S^{\tau}R = \sum S^{\tau}C = 1. \text{ Hence } (\Delta\tau/\tau) = (\Delta R/R) + (\Delta C/C).$$

Usually in the monolithic or hybrid IC technology components of one kind tract quite closely,

and it is possible to obtain passive RC components with equal but opposite temperature coefficient in thin-film technology, which finally yields $\Delta\tau/\tau = 0$.

Tab. 7.2: Summary of nonminimum phase function realization with nonideal CFA

Function	Modified coefficients						Design Eqns.
	$\tilde{n}_0$	$\tilde{n}_1$	$\tilde{n}_2$	$\tilde{d}_0$	$\tilde{d}_1$	$\tilde{d}2$	$(\tilde{k},\tilde{\lambda})$
$\tilde{F}_1$	1	$bk - m\in_v$	0	1	$1+m\in_v$	0	$(1+2m\in_v)$ $(1+\in_v)$
$\tilde{F}_2$	B	$1+m\in_v$	0	1	n_1	0	$(1+\in_v)$
$\tilde{F}_3$	$(1+kq\in_v)$	$k(1-(1+q)\in_v)^{-1}$	0	1	1	0	$2(1-(1+q)\in_v)$
$\tilde{F}_4$	$bk-(1+q\in_v)$	1	0	$1+0.5\in_v q$	1	0	$2(1+.75q\in_v)$ $(1+\in_v)$
$\tilde{F}_5$	1	$bk-(2+m\in_v)$	1+m	1	$3+m\in_v$	n2	$\tilde{k}(AP) =$ $(5+2m\in_v)(1+\in_v)$ $\tilde{k}(BR) =$ $(2+2m\in_v)(1+\in_v)$
$\tilde{F}_6$	$1+p\in_v$	$b\lambda-(2+p\in_v)$	1	$1+\left(\frac{(p\in_v)}{(1+\lambda)}\right)$	$2+\left(\frac{(p\in_v)}{(1+\lambda)}\right)$	1	$\tilde{\lambda}(AP) = 4(1+\in_v)$ $\tilde{\lambda}(BR) = 2(1+\in_v)$ Assumption $r_2 > R$, $p\in_v << 1$

$\tilde{F}_0 = (1-\in_i)$ in all cases except $\tilde{F}_0 3 = (1-\in_i)/(2+kq\in_v)$, $m = r_4/R$, $p = R/r_2$, $q = R/r_1$

7.7. EXPERIMENTAL RESULT

The proposed circuit had been bread boarded for laboratory test using the AD844 device biased with ± 12 V.d.c supply. The first order AP response was measured for F1(p) and F2(p) with k = 1($r_3 = r_4 = 3.3k\Omega$), C = 5 nF and R = 10 $k\Omega$ (variable in the range $1\,k\Omega \le R \le 100\,k\Omega$); tested were carried out at fixed frequency values of f = 3.3 kHz and f = 10 kHz with variable $\tau(5\mu s \le 500\mu s)$ where the input signal level had been set at Ii=300 μA. The measured response is shown in Fig. 7.2 .The Second order response had also been verified with suitable design at similar frequency ranges; satisfactory phase response of AP function were observed.

It may be mentioned here that for current mode cascadability, the passive components are to be chosen judiciously to avoid the effects of the parasitic capacitances at the high impedance associated with the CFA terminals. For very high frequency operation the parasitic capacitances at the high impedance nodes (noninverting input: 10 pF and compensation node: $\approx$ 15 pF shunted by 3MΩ output resistance), and the resistance at the low impedance inverting input mode ($\approx 60\,\Omega$) should be taken into consideration [61].

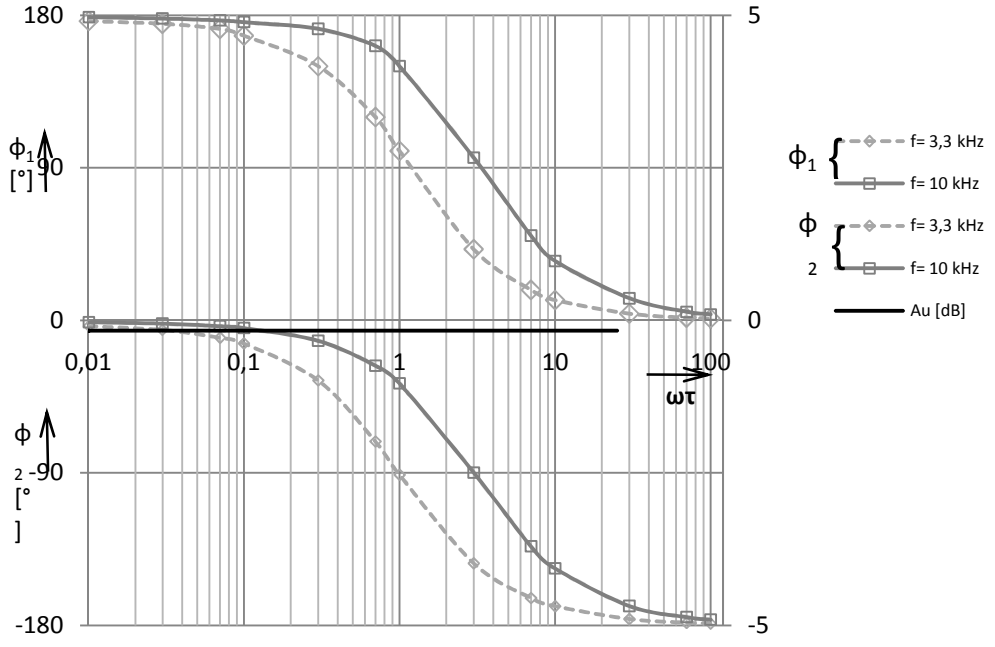


Fig. 7.2: Response of AP function with variable-τ

f = 3.3 kHz (x)
f = 10 kHz (.)
} Phase response

Magnitude response (o)

7.8. SUMMARY

Some simple circuit design schemes using a CFA are presented for the realization of first order and second order nonminimum phase function in the current mode. The network parameters are derived and compared under both ideal and nonideal device characteristics. Sensitivity calculations show that the realization are active insensitive. The output signal (I_0) is available in a current source node and hence are easily cascadable. An additional voltage signal output at a voltage source node is also available, if desired, after passing I_0 through a load resistance; this provides a constant resistive transimpedance with phase shifting property. The response of the nonminmum phase filters have been experimentally verified.

8. MULTIFILTER FUNCTION DESIGN

Recently CFA based circuits fund wide application on signal and wave processing. Here we present two new CFA based circuits to obtain good quality band pass (BP) band reject (BP) and all pass filters (AP). The BP filter has been used with subtract or to derive variable phase all pass (AP) functions

The simulation of lossless inductor and the Bruton's concept of supercapacitor developed earlier has been used in the RC resonator circuit to obtain the above mentioned filters. This idea can also be extended to design a high $Q(Q \to \alpha)$ oscillator function.

All the proposed functions have been verified with hardware implementation and by PSPICE macro model simulation in frequency range of $30\ kHz \leq f_0 \leq 300\ kHz$ .This analysis has also been made taking the effect of finite port errors $(\in)$ in case of nonideal CFAs.

8.1. ANALYSIS

The proposed circuit is shown in the Fig. 8.1. Here I_i = input current and V_i = input voltage. Appling the mesh equation, we find at Node B, [where voltage at node B is V].

$$V = I_z / Y_4$$

$$\text{or , } V.Y_4 = I_z$$

$$\text{or, } V.Y_4 = I_x \text{ [since } I_z = I_x \text{]} \qquad (8.1)$$

At Node D, $(V - V_i)Y_2 = V_i Y_3$ (Since the voltage at node D is V_i)

$$\text{or, } V = \frac{V_i(Y_2 + Y_3)}{Y_2} \qquad (8.2)$$

At Node A,

Putting the value of I_x from eq. (5.1)

$$\text{or}, \quad I_i = V_i.Y_i - \frac{V_i(Y_2+Y_3)(Y_1-Y_4)}{Y_2}$$

$$\text{or}, \quad Y_i = (Y_3Y_4 + Y_2Y_4 \_ Y_1Y_3)/Y_2 \tag{8.3}$$

Writing

$Y_1 = 1/R_1$, $Y_1 = 1/R_2$, $Y_3 = pC_2$, and $Y_4 = pC_1$ in Fig. 8.2 we get

$$Y_i = p^2.C_1C_2.R_2 + pC_1 - pC_2.\frac{R_2}{R_1}$$

$$= p^2.C_1C_2R_2 + pC_2(n-K), \quad n = C_1/C_2 \text{ and } K = R_2/R_1 \tag{8.4}$$

The realizability condition for an ideal supercapacitor is n=K, hence

$$Y_i = p^2D; \quad D = C_1C_2R_2 \tag{8.5}$$

By similar analysis, we get from Fig. 8.3,

$$Y_i = p^2.C_1C_2.R_2 + pC_2\{(1+n)-K\} \tag{8.6}$$

Using the component ratios as above [$n = C_1/C_2$ and $K = R_2/R_1$]

Writing $K = 1 + n$ for the realizability, we get

$$Y_i = p^2.D \tag{8.7}$$

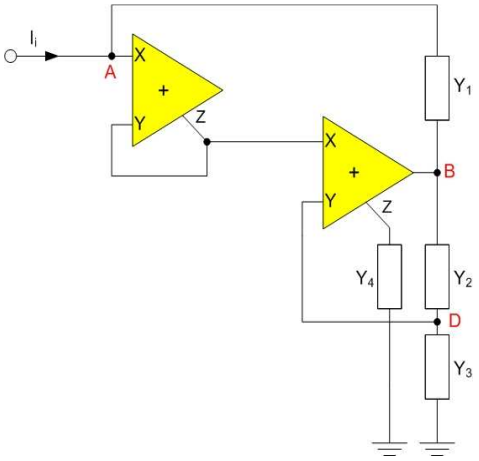


Fig. 8.1: Proposed CFA- based configuration

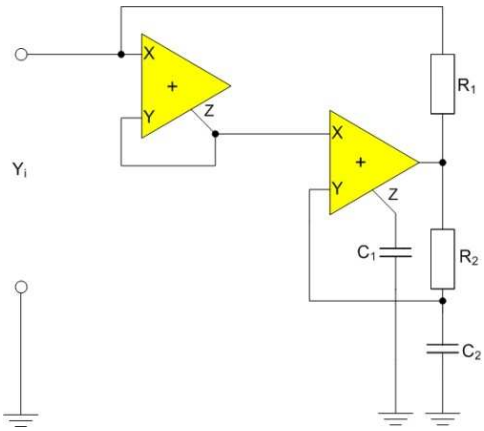


Fig. 8.2: Proposed CFA – based circuit of super capacitor

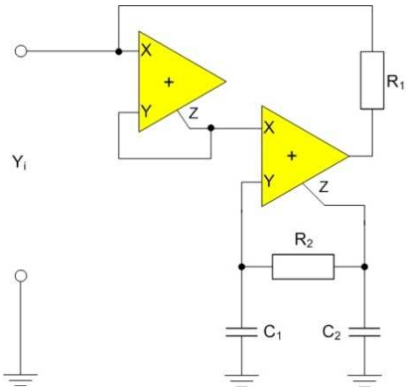


Fig. 8.3: Proposed CFA – based circuit of super capacitor

8.2. EFFECTS OF CFA ERRORS

Re-analysis of **Fig. 8.1** assuming non-ideal CFAs and considering finite port errors $(\in_{i,v,z} \neq 0)$, we get the modified admittance function

$$Y_i'(p) = p^2 D' + pC' + G \tag{8.8}$$

where

$$D' = D(1+\in_i) \tag{8.9}$$

$$C' = C_2[(n-K) + \{n\in_t - K(\in_{v1} + \in_{v2})\}] \tag{8.10}$$

$$G = \frac{-(\in_{v1} + \in_{v2})}{R_1} \tag{8.11}$$

$$\in_t = \in_{i1} + \in_{i2} + \in_{v1} + \in_{v2} + \in_{v2} + \in_{v2} \tag{8.12}$$

Thus the super capacitor becomes non-ideal, being shunted by a lossy capacitor (C') with a low value negative conductance *(G)*. The notified realizability condition for an ideal-D element is

$$K = \frac{n(1+\in_t)}{1+\in_{v1} + \in_{v2}} \tag{8.13}$$

The negative resistance may be cancelled by connecting a high-value shunt resistance (R_c) at the input port, given by $R_c = R_1/(\in_{v1} + \in_{v2})$. Note that with ideal CFAs, eq.(8.13) reduces to the nominal condition K=n. similar analysis had been carried out for the circuit in Fig. 8.2 and the modified expressions are summarized in Tab. 8.1.

8.3. FILTER DESIGN

According to Bruton concept frequency transformation a simple RLC resistor transforms to CRD filter without any change in the overall network transfer function. Hence a shunt in Fig. 8.4 where the supercapctor has generated by simulating circuit of Fig. 8.1.

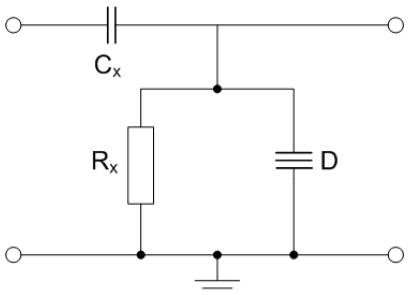


Fig. 8.4: Shunt RD topology for BP

Writing $C_1 = C_2 = C$ for simplicity we get the resistor transfer

$$H_1(p) = \frac{p.R_x.C_x}{p^2.R_x.D + pC_xR_x + 1} \tag{8.14}$$

Similarly in Fig. 8.2, we derived a series RD bandreject resonator while D is simulated by the circuit in Fig. 8.3.

The filter parameter, i.e resonant frequency (ω_0) and selectivity (Q) are

$$\omega_0 = \frac{1}{\sqrt{D.R_X}} \tag{8.15}$$

$$Q_{bp} = \frac{\sqrt{D/R_X}}{C_X} \quad \text{and} \quad Q_{br} = C_X\sqrt{\frac{RX}{D}} \tag{8.16}$$

The simplified design equations for (ω_0) and Q are listed in Table

Tab. 8.1: Effect of CFA-errors.

Fig7.5	Admittance	Realizability	Oscillator Frequency stability
(a)	$Y_i^{'} = S^2D' + sC' + G$ $D' = D(1+\epsilon_1) - k(1+\epsilon_{v1}+\epsilon_{v2})$ $C' = C_2\{n(1+\epsilon_1) - k(1+\epsilon_{v1}+\epsilon_{v2})\}$ $G = -\left(\frac{\epsilon_{v1}+\epsilon_{v2}}{R_1}\right)$ $D = C_1C_2R_2$ $n = \frac{C_1}{C_2}$ $k = \frac{R_2}{R_1}$ $Y_i^{'} = s^2D' + sC' + g$	$k = \frac{n(1+\epsilon_1)}{(1+\epsilon_{v1}+\epsilon_{v2})}$	$\frac{2}{3\varepsilon\sqrt{p}}(1+5\varepsilon)$
(b)	$D' = D(1+\epsilon_0)$ $C' = C_2(1+\epsilon_{v1}+\epsilon_{v2})\{1+n(1+\epsilon_{i1}+\epsilon_{i2})$ $-k(1-\epsilon_{z2})\}$ $g = -\left(\frac{\epsilon_{v1}-(\epsilon_{v1}+\epsilon_{v2})}{R_1}\right)$ $\epsilon_0=\epsilon_1-\epsilon_{z2}$	$k = \frac{(1+n)(1+\epsilon_1+\epsilon_2)}{(1-\epsilon\, z_2)}$	$\frac{1}{3\varepsilon\sqrt{p}}\left(\frac{1+4\varepsilon}{1+2\varepsilon}\right)$

Fig7.5	Filter Design		Active - sensitivity
	CFAs ideal	**CFAs non.- ideal (assuming $\epsilon_{i,v,z} = \epsilon$)**	
(a)	$\omega_0 = \frac{1}{C\sqrt{R \times R}}$ $Q = C\frac{\sqrt{p}}{C_x}$ $p = \frac{R_x}{R_2}$	BP $\frac{\omega'_0}{\omega_0} = \frac{1}{\sqrt{1+5\,\epsilon}}$ $\frac{Q'}{Q} = \sqrt{1+5\,\epsilon}$ BR	$\lvert S^{Q\omega_0}\rvert = \frac{\varepsilon/2}{1+5\varepsilon} \ll 0.5$
(b)	$\omega_0 = \frac{1}{C\sqrt{R \times R}}$ $Q = \frac{C_x}{C\sqrt{p}}$	$\frac{\omega'_0}{\omega_0} = \frac{1}{\sqrt{(1+4\,\epsilon)}}$ $\frac{Q'}{Q} = \sqrt{(1+4\,\epsilon)}$	$\lvert S^{Q\omega_0}\rvert = \frac{\varepsilon/2}{1+4\varepsilon} \ll 0.5$

To develop a second order all pass filter, we used another CFA as a subtract or as shown in the **Fig. 8.5** to obtain a function $H_{ap} = (2H_1 - 1)$, given by

$$H_{ap} = \frac{p^2 - p.(\omega_0 / Q_z) + \omega_0^{\ 2}}{p^2 + p.(\omega_0 / Q_p) + \omega_0^{\ 2}} \tag{8.17}$$

$$\text{where} \quad \omega_0 = \frac{1}{\sqrt{RX.D}} \quad \text{and} \quad Q_p = Q_z = (C / C_x) / \sqrt{R / R_x} \tag{8.18}$$

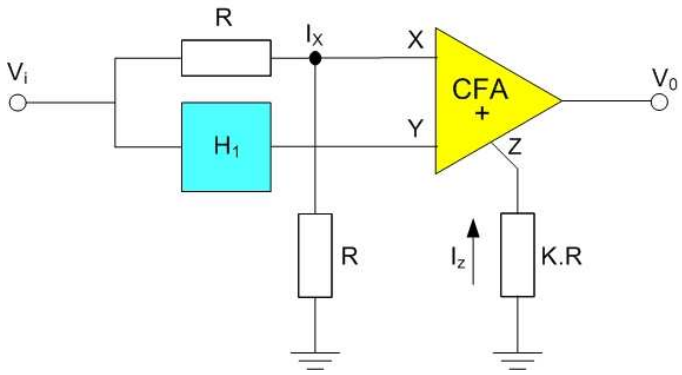


Fig. 8.5: Second order allpass filter

The phase response is given by $\phi_{ap} = \pi - \phi$

The value of ϕ is obtained by putting $s = j\omega$ in the eq. (8.17)

$$H_{ap}(\omega) = \frac{1 - m^2 - j(m/Q)}{1 - m^2 + j(m/Q)} \quad ; \quad m = \omega / \omega_0 \tag{8.19}$$

$$\text{Therefore,} \quad \phi = 2\tan^{-1}\frac{m/Q}{1 - m^2} \tag{8.20}$$

The observed phase- response is shown in Fig. 8.9 during the measurement we verified that the transmission gain remains constant up to 360 kHz at a value of unity.

8.4. SENSITIVITY

The classical sensitivity figure indicates the incremental deviation in the design parameters with respect to the imperfections in the active or passive components. This sensitivity figure is defined by

$$S_a^b = (db/b)/(da/a) \tag{8.21}$$

All the passive ω_0 sensitivities are seen to be $S^{\omega_0} = 0.5$ while the passive Q sensitivities may be made quite low by appropriately fabricated RC components since Q is proportional to ratios of components and in hybrid IC technology variation in components of one kind track quite closely. The device sensitivities with respect to the CFA errors (ε) have been calculated. These figures are listed in Tab. 8.1.

8.5. EXPERIMENTAL RESULT

The characteristic of the super capacitor simulating circuits in Fig. 8.1 and Fig. 8.2 have been experimentally verified with both hardware implementations using the AD-844 CFA device biased with 0 ± 12 V.d.c and by PSPICE macro model simulation.

The resonator type filter functions and the non-minimum phase all pass function have been tested with suitable circuits design covering frequency range of 30 kHz< f_0 <300 kHz at selectivity values $1 \le Q \le 10$. Each circuit of Fig. 8.1, Fig. 8.2 and Fig. 8.3 had been resonated with $R_X C_X$ section to verify both the BP and BR responses. In Fig. 8.6 a typical BP response utilizing the supercapctor of Fig. 8.1, and in Fig. 8.7 a BR response using that of Fig. 8.2 are shown; in Fig. 8.8 a low pass characteristics obtained across the D-element of the series resonator is shown. The all pass response utilizing the BP filter is shown in Fig. 8.9.

Fig. 8.6 to Fig. 8.9: Measured response of RCD resonator design for f_0= 100 kHz with R_2 = 10 $k\Omega$ = R_x, C_x = 160 pF.

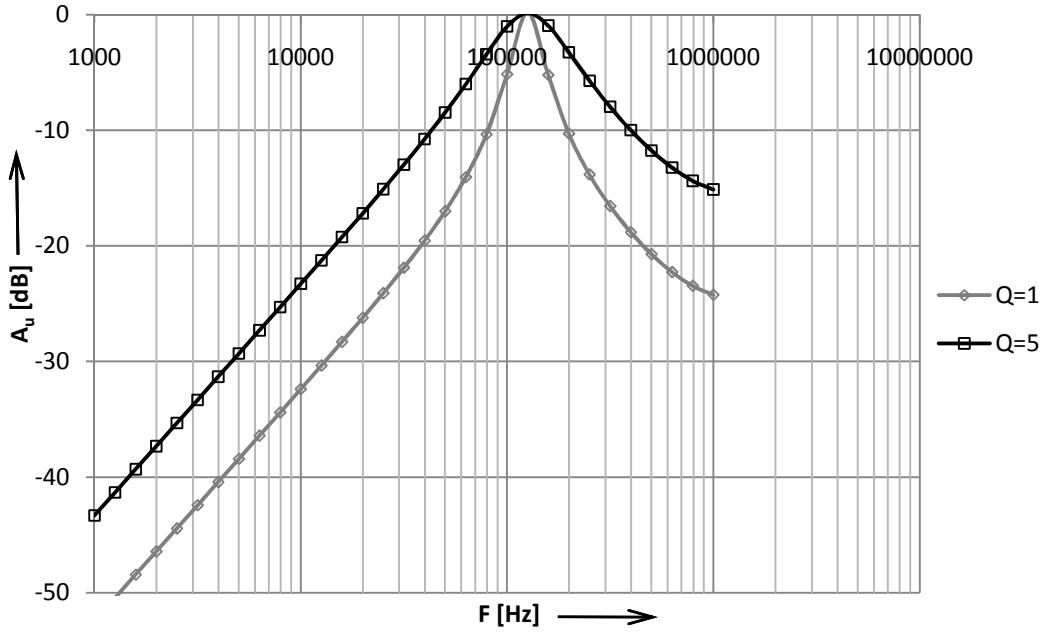


Fig. 8.6: BP filter using shunt-RD technology and its response (H_1 dB)

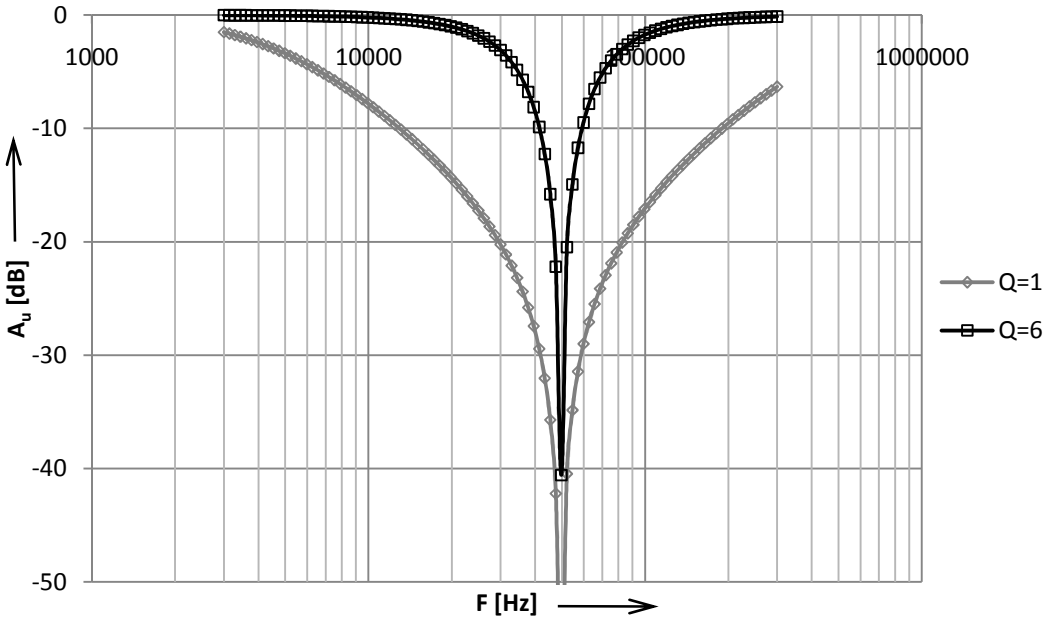


Fig. 8.7: BR filter using shunt-RD technology and its response (H_2 dB)

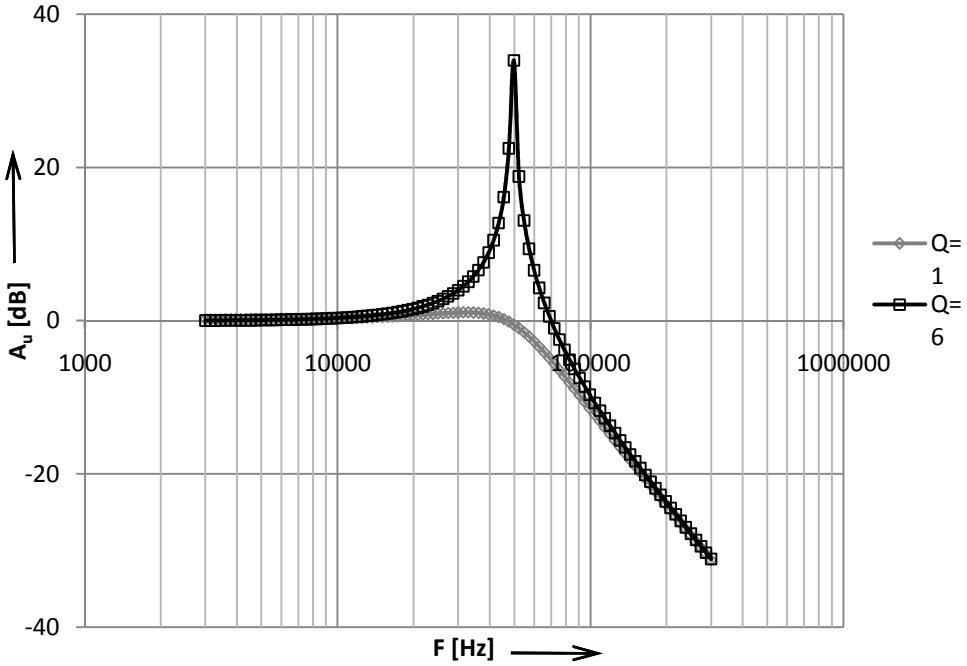


Fig. 8.8: LP response (H_3 dB) across D of series RD resonator

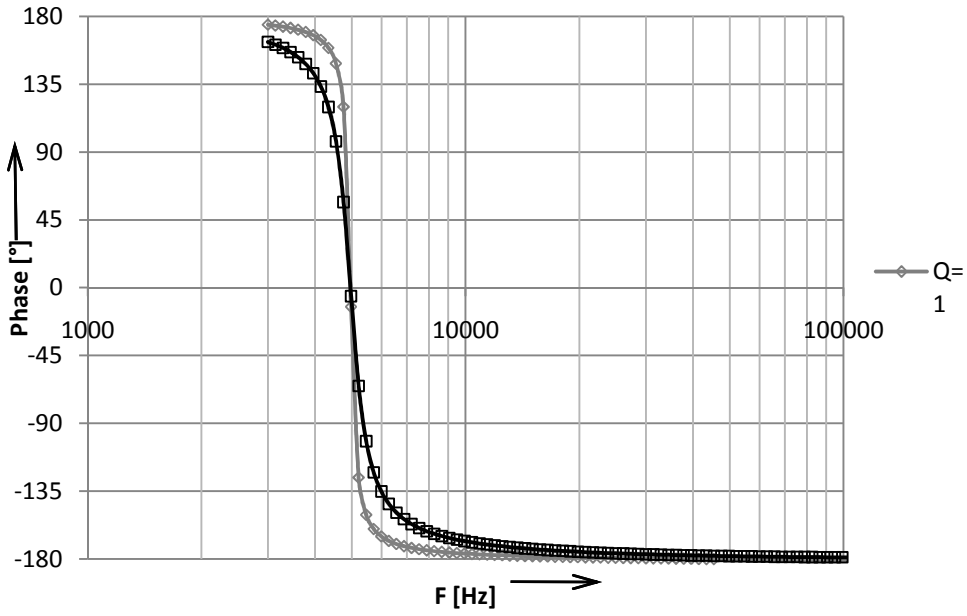


Fig. 8.9: Phase (ϕ°) response of AP function

8.6. SUMMARY

Two new CFA based active circuits are presented. Both the circuits realize ideal grounded super capacitor (D) element which are then to synthesis simple RCD filters and phase variable equalizer. Practical response of the filters have been experimentally verified in the frequency range 1<Q<10. Sinusoid wave generation had also been experimentally verified in the frequency range of 30 kHz < f_0 <300 kHz with moderately high Q values in the range $1 < Q < 10$. Sinusoid wave generation had also been verified after setting $Q \to \infty$ for both the configurations wherein continuous f_0 - tuning by a single resistor could be obtained.

Analysis shows that the CFA device imperfection affect the simulated D and filter parameters quite insignificantly and hence the circuits are active insensitive. The multifunctional analog signal processing and wave generation capabilities at low sensitivity using few components, may make the proposed structure quite suitable for micro circuit fabrication.

9. SINUSOID-OSCILLATOR REALZATION: DOUBLE INTEGRATOR LOOP

In the area of analog signal processing the voltage controlled oscillator (VCO) is being used as building block for the design of phase locked loop (PLL). FM telemetering, swept super heterodyne spectrum analysis, frequency synthesis, and digital voltage measurement by the v-f conversion. In the recent past operational Amplifier (AO) based RC oscillator has been developed where the tuning resister is being replaced by FET-VVR [3] to obtain a VCO.

Some CFA based RC- oscillator have been recently reported here we present sine wave oscillator design utilizing the Double integrator loop (DIL) based on the CFA active element.

In this chapter, we present some voltage tuned DIL- based sinusoid oscillators using the AD844 device. The time constant ($\tau_{0,1,2}$) of the two voltage controlled integrators of an oscillator is tuned by the d.c. control voltage (V_c) of the Multiplier (ICL-8013).The multiplier element with integrator has been used in the feed forward connection in the first DIL.

Here we have also examined CFA based linear voltage controlled sinusoidal oscillator (VCSO) wherein the multiplier element (ICL-8013) is connected with each CFA device in such a way that the d.c. control voltage(V_c) of the multiplier produces the f_0-tuning linearly. The oscillation frequency (f_0) over specific band, set by the different RC components, can be varied by the control voltage (V_c) of the multiplier. The choice of the multiplier element is advantageous since (V_c) may be generated from a digital code through a D-A converter (DAC) [162].

9.1. VOLTAGE CONTROLLED OSCILLATOR (VCO)

We present some new voltage controlled sinusoid oscillators (VCO's) based on the implementation of double integrator loop (DIL) as shown in **Fig. 9.1**. Here anon inverting Voltage Controlled Integrator and inverting Voltage Controlled Integrator, developed using CFA device have been used along with the multiplier element in the loop to control the time constants of the DILs. The oscillation frequency ω_0 (or f_0) is tunable by V_C of the multiplier element. In Fig. 9.1, each integrator is a minimal realization using only one RC-section, one multiplier and a CFA device. In Fig. 9.2, however two resistors have been used for each

integrator. Here two CFA's of same polarity have been used which may be suitable for microminiaturization of the circuit.

Fig. 9.1 and **Fig. 9.2**: The proposed VCO configurations using DIL:

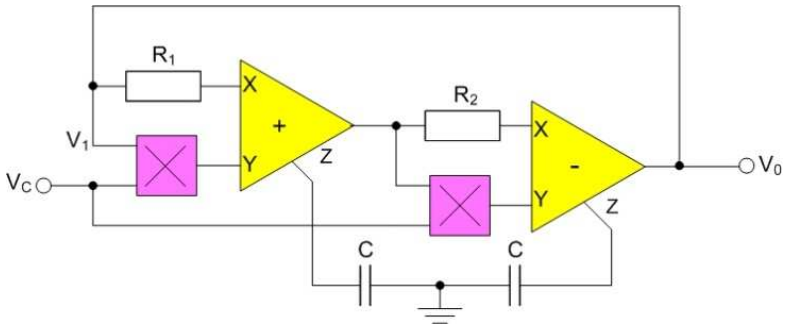


Fig. 9.1: Multiplier element in feed forward connection

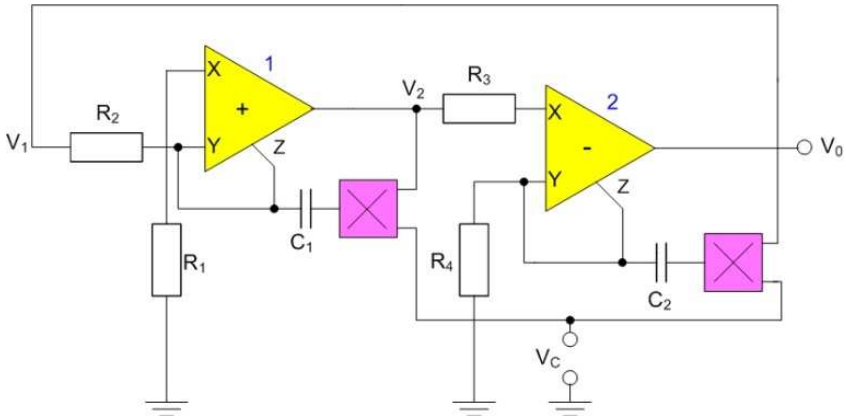


Fig. 9.2: Multiplier element in feedback connection

9.2. ANALYSIS

By analysis assuming ideal CFA, we get the voltage transfer function ($G_{1,2}$) respectively of the VCI#1 and VCI#2 in Fig. 9.1, assuming loop is cut at V_1, as

$$V_2/V_1 = G_1(p) = 1/p\tau_{01} \;;\; \tau_{01} = R_1C_1/(1-kV_C) \qquad (9.1)$$

$$V_0/V_2 = G_2(p) = 1/p\tau_{02} \;;\; \tau_{02} = R_2C_2/(1-kV_C) \qquad (9.2)$$

Where k = 0.1/volt is the multiplier constant.

Hence the loop- transfer is

$$G_0(p) = G_1G_2(p) = -1/\,p^2\tau_{01}\tau_{02} \tag{9.3}$$

The oscillation frequency (ω_0) obtained on closing the loop is

$$\omega_0 = 1/\sqrt{(\tau_{01}\tau_{02})} = (1-kV_C)/\sqrt{(R_1C_1R_2C_2} \tag{9.4}$$

Thus ω_0 is tunable by either the passive RC components or electronically by the dc control voltage in the range $1\ \text{V} \le V_C \le 10\ \text{V}$.

Similar analysis had been carried out for the circuit in Fig. 9.2; the pertinent design equations are listed in Tab. 9.1.

Tab. 9.1: Design Equations for the Proposed VCOs.

Fig.8.2	Transfer Equation	Loop Transfer
(a)	$\frac{V_2}{V_1} = G_1(s) = \frac{1}{s\tau_{o_1}}$ $\frac{V_0}{V_2} = G_2(s) = -\frac{1}{s\tau_{o_2}}$	$G(s) = -\frac{1}{S^2}\tau_{o_1}\tau_{o_1}$
(b)	$\frac{V_2}{V_1} = H_1(s) = \frac{a}{sC_1R_1(1-kV_c)+a-1}$ $a = \frac{R_1}{R_2}$ $\frac{V_0}{V_2} = H_2(s) = \frac{1}{sC_2R_3(1-kV_c)+b-1}$ $b = \frac{R_3}{R_4}$	$H(s) = \frac{a}{s^2\tau_{o_1}\tau_{o_2} + s\left\{\left(\tau_{o_1}(a-1)+\tau_{o_2}(b-1)\right)+(a-1)(b-1)\right\}}$ $\tau_{o_1} = C_1R_1(1-KV_c)$ $\tau_{o_2} = C_2R_3(1-KV_c)$

Fig.8.2	Realizabity Design	ω_0	Modified ω_0
(a)	None	$\frac{1-kV_c}{\sqrt{(R_1C_1R_2C_2)}}$	$\left\{\frac{\alpha_1\alpha_2\delta_1\delta_2(1-\beta_1kV_c)(1-\beta_2kV_c)}{R_1R_2C_1C_2}\right\}^{-\frac{1}{2}}$ $=\frac{\alpha\delta(1-\beta kV_c)}{RC}$ $for\ matched\ components$
(b)	Ideal CFA: $a=1$ $R_1=R_2=R_a$ $b=1$ $R_3=R_4=R_b$ Non ideal CFA: $\frac{R_1}{R_2}=1-\alpha_1\delta_1$ $\frac{R_3}{R_4}=1-\alpha_2\delta_2$	$\frac{1}{\left\{(1-kV_c)\sqrt{(R_aC_1R_bC_2)}\right\}}$	$\{(1-\delta_1kV_c)(1-\delta_1kV_c)R_aC_1R_bC_2\}^{-\frac{1}{2}}$ $=\frac{1}{(1-\delta kV_c)RC}$ $for\ matched\ components$

9.3. EFFECTS OF CFA IMPERFECTIONS

Re-analysis of the circuit in Fig. 9.1 assuming nonideal CFA devices yields the modified expressions

$$\tilde{G}_1(p)=\alpha_1\delta_1(1-kV_c\beta_1)/R_1C_1 \tag{9.5}$$

$$\tilde{G}_2(p)=\alpha_2\delta_2(1-kV_c\beta_2)/R_2C_2 \tag{9.6}$$

$$\text{and}\quad \tilde{G}_0(p)=-1/\,p^2\tilde{\tau}_{01}^{\ 2}\,\tilde{\tau}_{02}^{\ 2} \tag{9.7}$$

where $\tilde{\tau}_{0j} = R_j C_j / \alpha_j \delta_j (1 - kV_C \beta_j)$; j=1,2 (9.8)

The modified value of ω_0 is now

$$\tilde{\omega} = \{\alpha_1 \alpha_2 \delta_1 \delta_2 (1 - kV_c \beta_1)(1 - kV_c \beta_2) / R_1 R_2 C_1 C_2\}^{-1/2} \quad (9.9)$$

Assuming matched-pair of the device, we get

$$\tilde{\omega}_0 = \alpha\delta(1 - kV_C \beta\ )\sqrt{(R_1 R_2 C_1 C_2} \quad (9.10)$$

By similar analysis, we get the modified value of ω_0 for Fig. 9.2 as

$$\tilde{\omega}_0 = 1/RC(1 - \delta kV_c) \quad (9.11)$$

Assuming matched component, i.e.; $\delta_1 = \delta = \delta_2$ and $R_a C_1 = RC = R_b C_2$

Thus the CFA port errors alter slightly (since $\varepsilon << 1$) the value of ω_0 for both the circuits in Fig. 9.1 and Fig. 9.2 as listed in Tab. 9.1. However, their effects are quite insignificant as can be seen from the sensitivity computation.

9.4. SIMPLE LINEAR VOLTAGE CONTROLLED SINUSOID OSCILLATOR (VCSO)

In this section we present a simple linear Voltage Controlled sinusoid Oscillator (VCSO) using the CFA device. A multiplier ICL-8013 element is connect suitably with each CFA device such that electronic tuning of frequency (*fo*) is varied linearly with the d.c. control voltage (V_c) of the multiplier. The structure is based essentially on double integrator loop where in each unit is voltage controlled integrator (VCI) consisting of a CFA multiplier composite block and only one grounded RC section. Two phase quadrate oscillations at the two integrator output would be available upon closing the loop.

9.5. ANALYSIS FOR SIMPLE LINEAR VCO

Analyzing the proposed linear VCO of **Fig. 9.1** using generalized terminal properties for an ideal CFA from eqn.(5.1) and assuming that the loop cuts at V_1, yields

$$G_1(p) = V_2 / V_1 = KV_c /(pR_1C_1) = 1/(p\tau_1) \tag{9.12}$$

$$G_2(p) = V_0 / V_2 = KV_c /(pR_2C_2) = 1/(p\tau_2) \tag{9.13}$$

where $\tau_{1,2} = (RC)_{1,2} /(KV_c)$.

The loop-gain is

$$G_0(p) = G_1(p)G_2(p) = -(KV_c)^2 /(p^2R_1C_1R_2C_2) \tag{9.14}$$

$1 - G_0(p) = 0$ which yields

$$\omega_0 = kV_c / \sqrt{(R_1C_1R_2C_2)} \tag{9.15}$$

For a simplified design equation, we select $R_1 = R = R_2$ and $C_1 = C = C_2$,

Hence $kV_c /(RC)$ (9.16)

Here a minimum passive RC components are needed, all of which are grounded.

This feature of the proposed oscillator is suitable for IC adaptation of the circuit.

9.6. EFFECTS OF CFA IMPERFECTIONS

Re-analysis of **Fig. 9.3** with finite tracking errors ($\in \neq 0$) using eqn.(9.1) yields the modified transfer equations

$$\tilde{G}_1(p) = 1/(p\ \tilde{\tau}_1) \tag{9.17}$$

$$\tilde{G}_2(p) = -1/(p\ \tilde{\tau}_2) \tag{9.18}$$

The modified time constant (τ_1 & τ_2) can be expressed as

$$\tilde{\tau}_{1,2} = (R\ C)_{1,2}\ /(P_j k V_C) \tag{9.19}$$

$P_j = (\alpha_j \beta_j \delta_j)$; j=1,2; are the nonideality coefficients of the CFA.

$$\tilde{\omega}_0 = 1/\sqrt{(\tilde{\tau}_1 \tilde{\tau}_2)} \tag{9.20}$$

This may be expressed in terms of the errors as

$$\tilde{\omega}_0 / \omega_0 = \sqrt{\{1-(\in_{t,1} + \in_{t,2})\}} = \sqrt{}(P_1 P_2)$$

Where $\in_{tj} = \in_{vj} + \in_{ij} + \in_{0j}$; j=1,2 since $|\in| << 1$, the error products are neglected.

For an ideal CFA, the errors vanish ($\in = 0$) and we get, $\tilde{\omega}_0 = \omega_0$

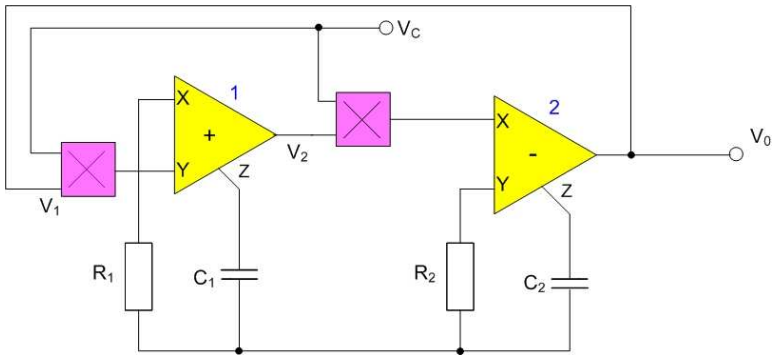


Fig. 9.3: Linear voltage controlled sinusoid oscillator using CFA

9.7. SENSITIVITY

The classical sensitivity figures are

$$S_{\varepsilon_{i,0}}^{\tilde{\omega}_0} = \frac{0.5 \in_{t_1}}{1-(\in_{i1} + \in_{v2} + \in_{01})} << 0.5 \qquad (9.21)$$

and

$$S_{\varepsilon_{v1,2}}^{\tilde{\omega}_0} = \frac{0.5 \in_{t_2}}{1-(\in_{i1} + \in_{v2} + \in_{02})} << 0.5 \qquad (9.22)$$

Similar sensitivity figures had been obtained for the circuit in Fig. 9.3. It may be seen that the passive sensitivities all are $S^{\tilde{\omega}_0} - passive = 0.5$. Hence the proposed design is practically active-insensitive since $|\in| << 1$.

9.8. EXPERIMENTAL RESULTS

The performance of both the circuits in Fig. 9.1 and Fig. 9.2 had been verified experimentally, both with hardware implementation and with PSPICE simulation. The AD-844 CFA chips and ICL-8013 multiplier element, biased by 0 ± 12 V.dc. regulated supply, were used. Good quality sine wave output with quadrate oscillations at V_0 (output of CFA $\neq 2$) and V_2 (output of CFA $\neq 1$) have been observed in the frequency range 50 kHz – 1.5 MHz shown in Fig. 9.4 and Fig. 9.5. A typical test waveform at 500 kHz for Fig. 9.1 is shown in Fig. 9.4, and that at 1 MHz for the circuit of Fig. 9.2 is shown in Fig. 9.5. Fig. 9.6 to Fig. 9.8 shows the variation of f_0 (kHz) relative to the d.c. control voltage (V_c).

The linear tuning characteristics of the circuits in Fig. 9.6, Fig. 9.7 and Fig. 9.8 had been verified experimentally; atypical test result of the linear voltage to frequency variation is shown in Fig. 9.8.

Fig. 9.4 to Fig. 9.5: VCO output waveform obtained with simulation test.

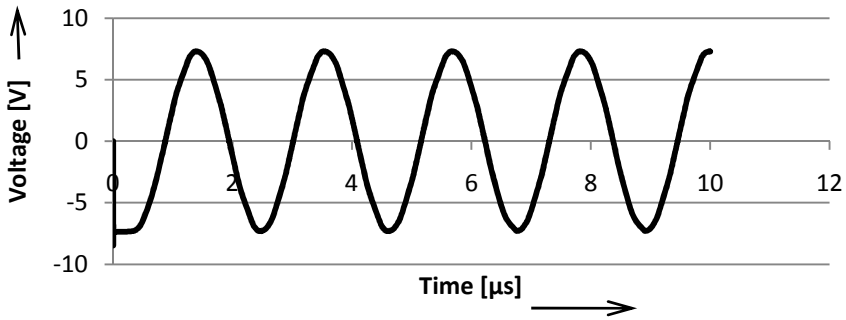


Fig. 9.4: Response of circuit in Fig. 9.1 at 500 kHz with V_C = 2 V d.c., $R_1 = R = R_2 = 1\ k\Omega$ and $C_1 = C = C_2$ = 256 pF

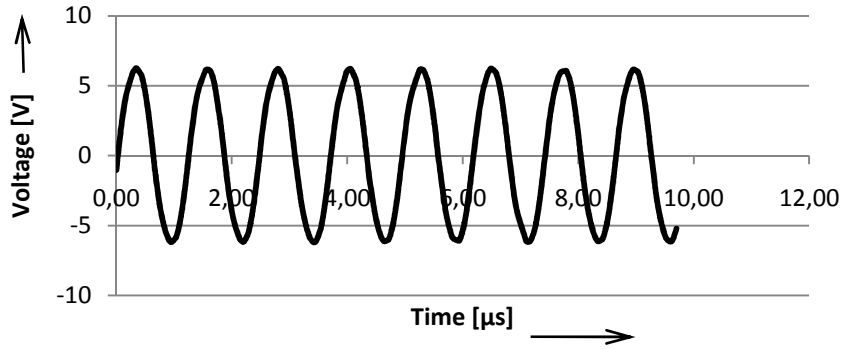


Fig. 9.5: Response of circuit in Fig. 9.2 at 1 MHz with V_C = 8.4 V d.c., $R_a = R = R_b = 1\ k\Omega$ and $C_1 = C = C_2$ = 1 nF

Fig. 9.6 to **Fig. 9.8**: Electronic turning characteristics.

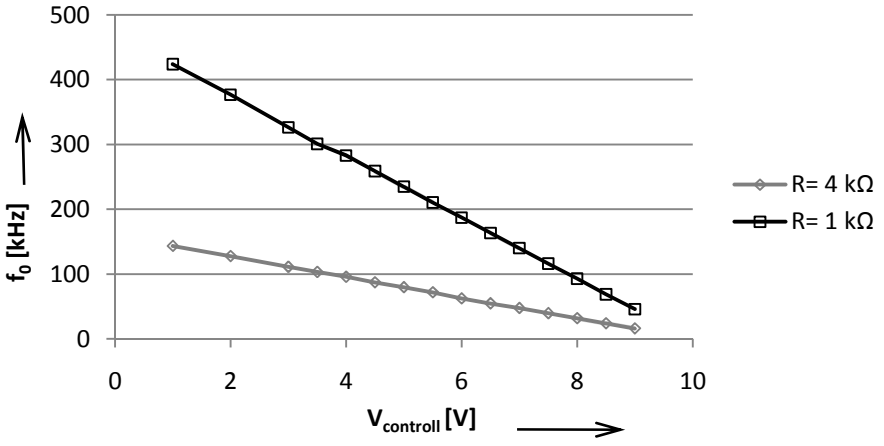


Fig. 9.6: Characteristics of Fig. 9.1 measured with $C_1 = C = C_2$ = 0.32 pF

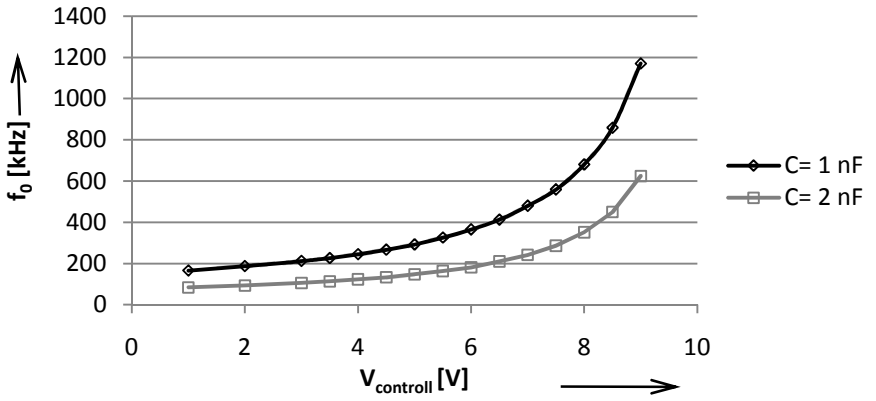


Fig. 9.7: Characteristics of Fig. 9.2 measured with $R_a = R = R_b = 1\ k\Omega$

– – Theoretical, – Experimental

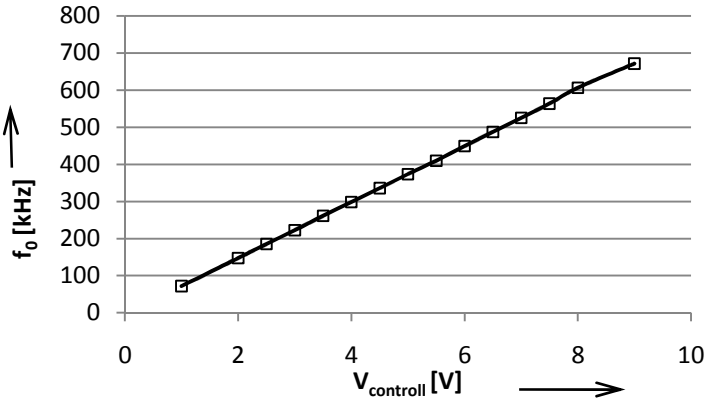


Fig. 9.8: Frequency Response of Simple Linear VCO: C = 0.20 nF, R = 1 $k\Omega$

Discussion: In this chapter new VCO design schemes using two CFA-based VCIs connected in a DIL are proposed; the feature of electronic control is derived by the d.c control voltage (V_c) of multiplier element. The advantages of the designs are the use of minimal active and passive components, practically active- insensitive feature and availability of quadrature-phase oscillation tunable electronically by V_c the work on extending this design to implementing digitally oscillators by deriving V_c from a digital code through DAC [148].

10. CONCLUSIONS

The target of this thesis was to bring the contribution on the field of the active building blocks for the modern integrated circuits operated in current- or mixed- mode. The group of the blocks was made tighter – the works was focused on current feedback amplifiers. The aim was an exploration of the family of the CFA circuits focusing on novel blocks and especially their applications.

The theoretical and practical results of the work were presented in three main chapters, which showed the usability and universality of the novel introduced blocks and moreover proved the possibility of the implementation of these blocks.

With growing importance of designs in voltage-to-current and current-to-current mode domains, we subsequently obtained the OTA, current conveyor, and voltage conveyor building blocks. For easy cascadability and signal translation from voltage/current input to any one of these as output, the designer needed a more versatile building block. Such an element emerged in mid-80s and was termed as the current feedback operational amplifier (CFOA) or more precisely as the current feedback amplifier (CFA). Thanks to its good technical features and parameters, it is one of the few current mode circuits, which have been accepted even by the manufacturers and are already currently available in the market (e.g. AD-844).

The CFA device was being used by many designers for a variety of analog signal processing applications. Because of the timelines of CFA-based research and development activity and its functional superiority over the previous devices, the we had chosen this device as the building block for the work on ASP circuits and systems.

In this thesis I presented some new CFA-based design of active immittance function pertaining to ideal grounded and floating inductance simulation schemes with a further extension to the design of an active ideal FDNR type super capacitor. The theoretical analysis had been verified experimentally through a typical BP filter design. It had been shown that these designs have very low active sensitivity without requiring any passive component

Active integrators and differentiators find wide applications in various, the well-known OA-RC Miller integrator gives rise to some dc instability at high signal levels owing to the capacitive negative feedback; the problem had subsequently been avoided by the modified designs, but here OA compensation pole introduces additional phase shift at higher frequencies.

I have presented some new CFA-based design of an integrator and differentiator in

both current-mode and voltage-mode forms; dual input capability had been derived in some of the designs. It had been shown that these designs are well-suited for monolithic IC fabrication process in which event the sensibility of the time constant may be reduced to extremely low values. Some CFA–based AP phase equalizer circuits of first and second order realization is also described. The effects of the CFA device imperfections had been investigated.

Satisfactory immitance and transfer properties od the proposed functional blocks had been verified after circuit simulation through PSPICE.

I can select the following new and significant contributions ofthis thesis:

- Design and verification of the insensitive ideal FDNR-type supercapacitor.

- New CFA-based designs of integrator/differentiator in both current- mode and voltage-mode forms well suited for IC fabrication.

- Investigations of the effects of the CFA imperfections for some CFA- based AP phase equalizer circuits.

- New results from the investigation of multifiltering capability in an appropriate RCD resonator

- Novel VCO using a multiplier in the CFA-based double integrator loop

Both the current conveyor (CC) and the CFA devices are basically current-mode devices; the CFA (e.g. AD-844) however has an added capability of copying its transimpedance voltage available at the current source output mode, to wide band buffer's voltage source output mode. Hence most of the elegant CC-based function circuits may easily transform the equivalent CFA-based configuration with an added voltage signal output-hence extreme ease on design flexibility and smooth casecadability, recently the next version of the current conveyor of the third generation (CCIII) is receiving considerable attention for current mode ASP applications. It may be examined how a composite CFA structure can be modeled to yield the CCIII characteristics so that either polarity current signals may be handled by the same device. Another potential area of future R and D appears to be the design of digitally programmable current mode circuits.

The presented work represents the investigation on building blocks for modern current-mode and mixed mode based integrated circuits. A number of novel introduced building blocks together with their implementation are the results. The functionality of the proposed blocks was proved by simulations in the SPICE programme.

With respect to the above discussion it can be declared that aims of this thesis were fulfilled.

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