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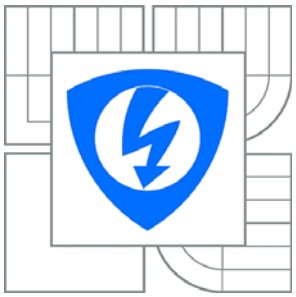

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FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

DEPARTMENT OF TELECOMMUNICATIONS

NOVEL ACTIVE FUNCTION BLOCKS AND THEIR APPLICATIONS IN FREQUENCY FILTERS AND QUADRATURE OSCILLATORS

NOVÉ AKTIVNÍ FUNKČNÍ BLOKY A JEJICH APLIKACE V KMITOČTOVÝCH FILTRECH A KVADRATURNÍCH OSCILÁTORECH

DIZERTAČNÍ PRÁCE

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Nové aktivní funkční bloky a jejich aplikace v kmitočtových filtrech a kvadraturních oscilátorech

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ABSTRACT

Frequency filters and sinusoidal oscillators are linear electric circuits that are used in wide area of electronics and also are the basic building blocks in analogue signal processing. In the last decade, huge number of active building blocks (ABBs) were presented for this purpose. In 2000 and 2006, the universal current conveyor (UCC) and the universal voltage conveyor (UVC), respectively, were designed at the Department of Telecommunication, BUT, Brno, and produced in cooperation with AMI Semiconductor Czech, Ltd. There is still the need to develop new active elements that offer new advantages. The main contribution of this thesis is, therefore, the definition of other novel ABBs such as the differential-input buffered and transconductance amplifier (DBTA), the current follower transconductance amplifier (CFTA), the z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA), the generalized current follower differential input transconductance amplifier (GCFDITA), the voltage gain-controlled modified current-feedback operational amplifier (VGC-MCFOA), and the minus-type current-controlled third-generation voltage conveyor (CC-VCIII–). Using the proposed ABBs, novel structures of first-order all-pass filters, second-order universal filters, KHN-equivalent circuits, inverse filters, active grounded inductance simulators, and quadrature sinusoidal oscillators working in the current-, voltage-, or mixed-mode are presented. The behavior of the proposed circuits has been verified by SPICE simulations and in selected cases also by experimental measurements.

KEYWORDS

Analog signal processing, current-mode, voltage-mode, mixed-mode, frequency filter, first-order all-pass filter, universal filter, KHN-equivalent, inverse filter, active grounded inductance simulator, quadrature oscillator, UCC, UVC, DBTA, PCA, CFTA, ZC-CFTA, CCCFTA, ZC-CCCITA, GCFDITA, CBTA, MCFOA, VGC-MCFOA, CC-VCIII–

ABSTRAKT

Kmitočtové filtry a sinusoidní oscilátory jsou lineární elektronické obvody, které jsou používány v široké oblasti elektroniky a jsou základními stavebními bloky v analogovém zpracování signálu. V poslední dekádě pro tento účel bylo prezentováno velké množství stavebních funkčních bloků. V letech 2000 a 2006 na Ústavu telekomunikací, VUT v Brně byly definovány univerzální proudový konvejor (UCC) a univerzální napět'ový konvejor (UVC) a vyrobeny ve spolupráci s firmou AMI Semiconductor Czech, Ltd. Ovšem, stále existuje požadavek na vývoj nových aktivních prvků, které nabízejí nové výhody. Hlavní přínos práce proto spočívá v definici dalších původních aktivních stavebních bloků jako jsou differential-input buffered and transconductance amplifier (DBTA), current follower transconductance amplifier (CFTA), z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA), generalized current follower differential input transconductance amplifier (GCFDITA), voltage gain-controlled modified current-feedback operational amplifier (VGC-MCFOA), a minus-type current-controlled third-generation voltage conveyor (CC-VCIII–). Pomocí navržených aktivních stavebních bloků byly prezentovány původní zapojení fázovacích článků prvního řádu, univerzální filtry druhého řádu, ekvivalenty obvodu typu KHN, inverzní filtry, aktivní simulátory uzemněného induktoru a kvadraturní sinusoidní oscilátory pracující v proudovém, napět'ovém a smíšeném módu. Chování navržených obvodů byla ověřena simulací v prostředí SPICE a ve vybraných případech experimentálním měřením.

KLÍČOVÁ SLOVA

Analogové zpracování signálu, proudový mód, napět'ový mód, smíšený mód, kmitočtový filtr, fázovací článek prvního řádu, univerzální filtr, KHN-ekvivalent, inverzní filtr, aktivní uzemněný induktor simulátor, kvadraturní oscilátor, UCC, UVC, DBTA, PCA, CFTA, ZC-CFTA, CCCFTA, ZC-CCCITA, GCFDITA, CBTA, MCFOA, VGC-MCFOA, CC-VCIII–

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DECLARATION

I declare that I have elaborated my doctoral thesis on the theme of "Novel active function blocks and their applications in frequency filters and quadrature oscillators" independently, under the supervision of the doctoral thesis supervisor and with the use of technical literature and other sources of information which are all quoted in the thesis and detailed in the list of literature at the end of the thesis.

As the author of the doctoral thesis I furthermore declare that, concerning the creation of this doctoral thesis, I have not infringed any copyright. In particular, I have not unlawfully encroached on anyone's personal copyright and I am fully aware of the consequences in the case of breaking Regulation § 11 and the following of the Copyright Act No 121/2000 Vol., including the possible consequences of criminal law resulted from Regulation § 152 of Criminal Act No 140/1961 Vol.

Brno ....

(author's signature)

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INTRODUCTION

Frequency filters and sinusoidal oscillators are linear electric circuits [148] that are used in wide area of electronics and also are the basic building blocks in analogue signal processing. The analogue frequency filters are the most often used as anti-aliasing video filters in the analogue sections of high-speed data communication systems defined by ITU BT 601 standard [152] or for signal processing in wireless LANs described by IEEE 802.11 standard [94], in IF (Intermediate Frequency) receiver stages of the GSM cellular telephones [46], [69], in receiver baseband blocks of modern radio systems [118], [145], in hard-drive communication interfaces [85], measurement systems [154], automotive industry [50], or in piezoresistive pressure sensors [122]. Oscillators also represent an important unit in many telecommunication, instrumentation and control systems [1], [5], [25], [28], [60], [64], [81], [134].

In the last decade, for analogue signal processing huge number of active building blocks were introduced. However, there is still the need to develop new active elements that offer new and better advantages. This thesis is, therefore, focused on definition of other novel ABBs and, furthermore, novel filter and oscillator structure designs.

In the present days a number of trends can be noticed in the area of analogue filter and oscillator design, namely reducing the supply voltage of integrated circuits and transition to the current-mode [148]. On the other hand, voltage- and mixed-mode circuit design still receive considerable attention of many researchers. Therefore, the the proposed circuits in this work are working in current-, voltage-, or mixed-mode.

The thesis is organized as follows: Chapter 3 presents different active elements, where most of them have been introduced and developed at the Department of Telecommunications, Brno University of Technology. These active building blocks are further used in this thesis for various filter and oscillator designs. This Chapter also introduces novel elements defined within this work. As applications, twelve various current-, voltage-, and mixed-mode first-order all-pass filter structures are presented in Chapter 4. All circuits are novel and their advantages are compared with the literature presented solutions. Second-order filter structures, and especially the Kerwin–Huelsman–Newcomb filtering circuit, have received considerable attention in the last decade. Therefore, Chapter 5 is focused on this issue by presenting one current- and three voltage-mode filter structures, one dual-mode KHN-equivalent structure, and furthermore, one VM general circuit topology to derive second-order inverse filters, which is very unique in current technical literature. During the last few decades, various grounded inductors have been created using different high-performance active building blocks. In the Chapter 6 two resistorless active-C positive inductance simulators are introduced and compared with the literature pre-

sented solutions. Quadrature oscillators are frequently used in various applications, i.e. in telecommunications for quadrature mixers and single-sideband generators, for measurement purposes in vector generators or selective voltmeters. Therefore, quadrature oscillators represent an important unit in many communication, control systems, signal processing, instrumentation and measurement systems [5], [60], [81], [125]. Therefore, Chapter 7 presents five quadrature oscillators using different active elements.

To verify the behavior of the proposed circuits, defined active elements are implemented using bipolar or CMOS internal structures. The feasibility of selected circuits is also confirmed by experimental measurements.

1 STATE OF ART

Nowadays, the presented structures of active frequency filters and oscillators are often employing current conveyors (CCs), where the second-generation current conveyor (CCII) [124] is the most popular. The CCII is the basic block of many other active elements. Here, the current-feedback operational amplifier (CFOA) [42], [138], [43] that is a combination of the CCII and voltage follower (VF) [123] or the composite current conveyor (CCC) [133] that is the interconnection of the plus-type and minus-type CCIIs can be mentioned. Recently, based on the CCC the modified CFOA (MCFOA) [159] was reported. Later, the inverting second-generation current conveyor (ICCII) as a missing building block in analogue signal processing techniques has been introduced [9]. By the combination of CCII and ICCII the dual-X second-generation current conveyor (DXCCII) [165] for the tunable continuous-time filter design has been built. Recently, further research has focused on CCs with variable current and/or voltage gains such as electronically tunable second-generation current conveyor (ECCII) [105], variable gain current conveyor (VGCCII) [163], or voltage and current gain second-generation current conveyor (VCG-CCII) [37].

Using the duality principle, the voltage conveyor (VC) has been presented in 1981 [51]. As in the theory of CCs, also here the first- and second-generation VCs (VCI, VCII, IVCI, and IVCII) were described [51], [39], [106], [110]. The best known VC is the plus-type differential current voltage conveyor (DCVC+) [120] that is more often labelled as the current differencing buffered amplifier (CDBA) [4]. Recently, the current-controlled CDBA (C-CDBA), the current-controlled inverting CDBA (C-ICDBA), and the z copy-controlled gain-CDBA (ZC-CG-CDBA) [13] have also been introduced [102]. By the modification of the CDBA or replacement of the VF by the operational transconductance amplifier (OTA) [53] the differential-input current feedback amplifier (DCFA) [166], and current differencing transconductance amplifier (CDTA) [12] have been presented.

Based on the idea of the "universal" active element [26] the universal current conveyor (UCC) [10], [21], [23], [73], [190] was designed and developed as a sample series containing 50 pieces, using the CMOS 0.35 μm technology, under the designation UCC-N1B 0520 at our workplace, and produced in cooperation with AMI Semiconductor Czech, Ltd., (now ON Semiconductor Czech Republic, Ltd.). On the basis of the UCC, the universal voltage conveyor (UVC) was designed [22], [168], [196], [106], [110] and produced under the designation UVC-N1C 0520. The realizable generations and types of VCs using the UVC were shown by Minarcik and Vrba in [106].

2 THESIS OBJECTIVES

In the last decade, for analogue signal processing huge number of active building blocks (ABBs) were introduced, however, there is still a need to develop new active elements that offer new and better advantages. Therefore, the main aim of this thesis is to define various types of novel active building blocks. The first intention is to define such novel more-terminal ABB with low-impedance current/high-impedance voltage inputs and high-impedance current/low-impedance voltage outputs, which will belong to the group of "universal" active elements, e.g. universal current conveyor (UCC) and universal voltage conveyor (UVC).

Special attention will be paid on active element with only current inputs and outputs. From the cascadability point of view, ABBs with low-input and high-output impedance terminals are the most interesting. The proposed active element will be further studied and, if possible, modified according to special needs.

In the present days a number of trends can be noticed in the area of active function block design. The attention is also focused on ABBs with tunability property. Here the current or voltage gain tuning can be mentioned. Hence, part of this work is focused on such novel ABB design that voltage gain can be controlled by means of external current.

Voltage conveyors are also important and useful elements in analogue signal processing, however, their potentials are still not enough studied. Therefore, special attention will be also paid on novel VC design with tunability feature.

The main part of the thesis will concentrate on application possibilities of the defined functional blocks. First-order all-pass filters are widely used in analogue signal processing. Several current-mode (CM), voltage-mode (VM), or mixed-mode first-order AP filter realizations using different active building blocks have been reported in the literature. These topologies realize either inverting or non-inverting type of filters. For realizing the complementary type, they need to change the circuit topology. Furthermore, most of the reported realizations do not include electronical tunability property. Hence, the intention is to propose such AP filters that enable both the inverting and the non-inverting type AP filter responses simultaneously and easy tunability of the natural frequency.

Part of this work focuses on such second-order filter structures that can provide all standard filter responses without changing the circuit topology. Special attention is paid to Kerwin–Huelsman–Newcomb structure that enables mutually independent control of the quality factor Q and characteristic frequency ω_0.

Due to disadvantages of conventional inductors, active element-based inductor design is very desirable to designers today. During the last few decades, various grounded inductors have been created using different high-performance active build-

ing blocks. However, they employ excessive number of active and passive components. Thus, the aim is to create single grounded capacitor-based positive grounded inductor simulator in compact form.

Quadrature oscillators also represent an important unit in many communication, control systems, instrumentation and measurement systems. Therefore, part of this work attempts this issue.

In the first step the theoretical analyses are done using SNAP software [82]. To verify the behavior of the proposed circuits, defined active elements are implemented using bipolar or CMOS internal structures. The feasibility of selected circuits are also confirmed by experimental measurements.

3 ACTIVE BUILDING BLOCKS AND THEIR PROPERTIES

This Chapter presents different active elements, where most of them have been introduced and developed at the Department of Telecommunications, Brno University of Technology. These active building blocks (ABBs) are further used in this thesis for various filter and oscillator designs.

3.1 Universal current conveyor (UCC)

The first presented ABB is the universal current conveyor [10], [21], [23], [73], [137], [177], [190], [191], which is an eight-port active element that schematic symbol is shown in Fig. 3.1(a). Analogous to the differential difference current conveyor (DDCC) [34] or to differential difference complementary current conveyor (DDCCC) [57], the UCC has three high-impedance voltage inputs Y (one differencing - Y2, and two summing - Y1, and Y3), one low impedance input X, and four current outputs (Z1+, Z1–, Z2+, Z2–). Outputs Z1–, Z2– are inverse to outputs Z1+ and Z2+.

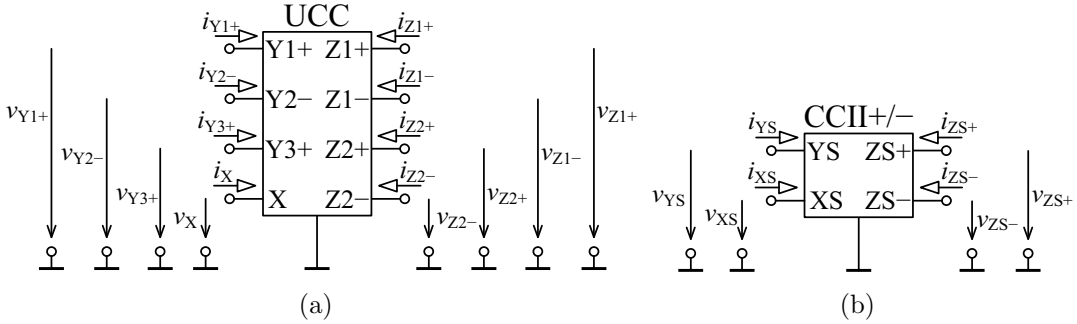


Fig. 3.1: Schematic symbol of (a) universal current conveyor and (b) dual-output second-generation current conveyor

Relations between the individual terminals of non-ideal UCC can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{Y1} \\ i_{Y2} \\ i_{Y3} \\ v_X \\ i_{Z1+} \\ i_{Z1-} \\ i_{Z2+} \\ i_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \alpha_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\alpha_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \alpha_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\alpha_4 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{Y1} \\ v_{Y2} \\ v_{Y3} \\ i_X \\ v_{Z1+} \\ v_{Z1-} \\ v_{Z2+} \\ v_{Z2-} \end{bmatrix}, \tag{3.1}$$

where $\beta_k = 1 - \varepsilon_{vk}$ and $\alpha_j = 1 - \varepsilon_{ij}$ (k = 1, 2, 3 and j = 1, 2, 3, 4) are the non-ideal voltage and current gains, respectively, and ε_{vk} ($|\varepsilon_{vk}| \ll 1$) and ε_{ij} ($|\varepsilon_{ij}| \ll 1$) denote voltage and current tracking errors of the UCC, respectively.

Through suitable interconnection or grounding of the terminals, the UCC enables the realization of all types and generations of CCs with single low-impedance current input X such as CCI+, CCI–, CCI+/–, CCII+, CCII–, CCII+/–, CCIII+, CCIII–, CCIII+/–, inverting-types of current conveyors such as ICCI+, ICCI–, ICCI+/–, ICCII+, ICCII–, ICCII+/–, ICCIII+, ICCIII–, ICCIII+/–, and other types with differential input such as DVCCI+, DVCC–, DVCC+/–, DVCCI–, DVCCIII+, DDCC+, DDCC–, and DDCC+/–. The implementation method of current conveyors mentioned above is shown in [10]. The multiple-output current follower (MO-CF) [73] can be also realized by the UCC, when only current input X and all four current outputs Z are used, while voltage inputs are grounded. Implementation of the balanced-output operational transconductance amplifier (BOTA) using UCC is another option [190]. In this case, voltage inputs Y1 and Y2 are used and admittance G_K is connected to current input X in order to represent transconductance g_m. Terminals Z1+ and Z1– are used as current outputs.

In addition to UCC, the produced UCC-N1B 0520 integrated circuit also includes the dual-output second-generation current conveyor (CCII+/-) that schematic symbol is shown in Fig. 3.1(b). The CCII+/– can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{YS} \\ v_{XS} \\ i_{ZS+} \\ i_{ZS-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \beta_S & 0 & 0 & 0 \\ 0 & \alpha_{S1} & 0 & 0 \\ 0 & -\alpha_{S2} & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{YS} \\ i_{XS} \\ v_{ZS+} \\ v_{ZS-} \end{bmatrix}, \tag{3.2}$$

where $\beta_S = 1 - \varepsilon_{Sv}$ and $\alpha_{Sj} = 1 - \varepsilon_{Sij}$ (j = 1, 2) are the non-ideal voltage and current gains, respectively. Here, ε_{Sv} ($|\varepsilon_{Sv}| \ll 1$) and ε_{Sij} ($|\varepsilon_{Sij}| \ll 1$) denote voltage and current tracking errors of the CCII+/–, respectively.

Thanks to the UCC and the CCII+/– in one chip, the produced integrated circuit is also suitable for the implementation of various active elements such as the current follower transconductance amplifier (CFTA) [167], [181], or the MCFOA [177]. Both ABBs are discussed in following Sections.

Based on the idea of the UCC proposed at our Department, Qiujing *et al.* introduced the fully balanced version of the UCC [117]. The new universal current conveyor is a nine-port building block that has four high-impedance inputs (Y1, Y2, Y3, and Y4), two voltage-tracking terminals (X1 and X2), two current outputs (Z+, Z–), and one current control terminal I_B. The new UCC can also realize the fully differential current conveyor (FDCCII) [40] and the fully balanced second-generation

current conveyor (FDCCII) [7]. Here, it is also worth mention that our papers on UCC ([190] and [191]) have already been cited by international researchers Horng *et al.* in [63], Kumar *et al.* in [83], Lata and Kumar in [91], Parveen in [114], and Tlelo-Cuautle *et al.* in [144].

3.2 Universal voltage conveyor (UVC)

Voltage conveyors have been defined using the duality principle to CCs in 1981 [51]. As in the theory of CCs, also here the first- and second-generation VCs (VCI, VCII, IVCI, and IVCII) were described [39], [51], [106]. The best known VC is the DCVC+ [120] that is more often labelled as the CDBA [4]. Recently, the the C-CDBA and C-ICDBA have also been introduced [102]. Based on the idea of the "universal" active element [26] and also on the basis of the above presented UCC, the UVC [106], [137], [168], [196]–[199] was designed and developed, using the CMOS 0.35 μm technology, under the designation UVC-N1C 0520 at our workplace, and produced in cooperation with AMI Semiconductor Czech, Ltd. as sample series containing 50 pieces. Here, it is also worth mention that our work on UVC [168] has already been cited by international researcher Horng in [62]. The schematic symbol of the UVC is shown in Fig. 3.2. It is defined as a six-port active element, which has one voltage input X, two difference current inputs (YP, YN), two mutually inverse voltage outputs (ZP, ZN), and one auxiliary port W.

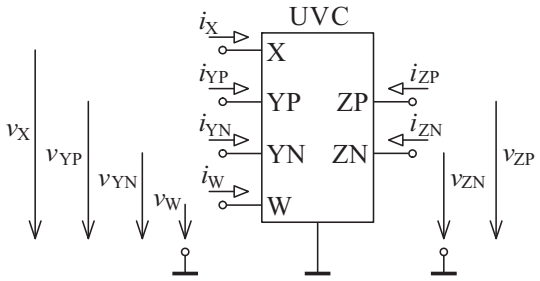


Fig. 3.2: Schematic symbol of the UVC

Using standard notation, the relationship between port currents and voltages of a non-ideal UVC can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{\mathrm{X}} \\ v_{\mathrm{YP}} \\ v_{\mathrm{YN}} \\ i_{\mathrm{W}} \\ v_{\mathrm{ZP}} \\ v_{\mathrm{ZN}} \end{bmatrix} = \begin{bmatrix} 0 & \alpha_1 & -\alpha_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & \delta_1 & 0 & 0 \\ 0 & 0 & 0 & \delta_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \gamma_1 & 0 & 0 & 0 & 0 & 0 \\ -\gamma_2 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{\mathrm{X}} \\ i_{\mathrm{YP}} \\ i_{\mathrm{YN}} \\ v_{\mathrm{W}} \\ i_{\mathrm{ZP}} \\ i_{\mathrm{ZN}} \end{bmatrix}, \tag{3.3}$$

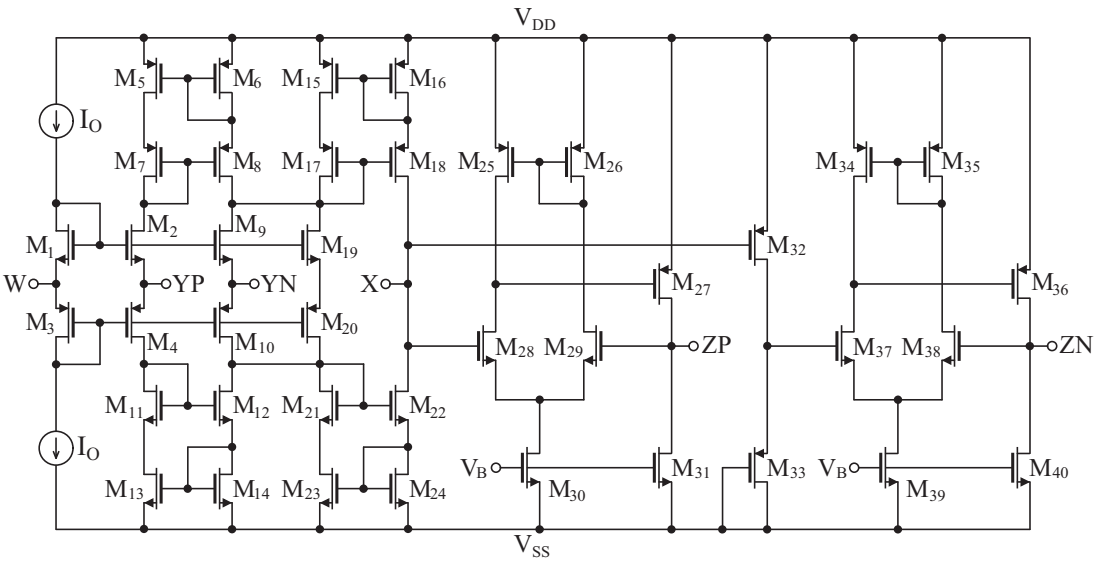


Fig. 3.3: Proposed CMOS implementation of the UVC [175]

Tab. 3.1: Transistor dimensions of the UVC

PMOS transistors	W(μm)/L(μm)
M5–M8, M10, M15–M18, M20	14.0/0.7
M3,M4	28/0.7
M25, M26, M34, M35	4.0/0.5
M27, M36	10.0/0.5
M32, M33	2.1/1.0
NMOS transistors	**W(μm)/L(μm)**
M1, M2	14.0/0.7
M9, M11–M14, M19, M21–M24	28.0/0.7
M28, M29, M37, M38	0.8/0.5
M30, M31, M39, M40	10/0.5

where $\alpha_j = 1 - \varepsilon_{ij}$, $\delta_j = 1 - \varepsilon_{v1j}$, $\gamma_j = 1 - \varepsilon_{v2j}$ for $j = 1, 2$. Here, ε_{ij} ($|\varepsilon_{ij}| \ll 1$) and ε_{v1j}, ε_{v2j} ($|\varepsilon_{v1j}|$, $|\varepsilon_{v2j}| \ll 1$) denote current and voltage tracking errors of UVC, respectively.

By connecting or grounding suitable terminals of the UVC, it helps to realize all existing types of voltage conveyors such as VCI+, VCI–, VCI+/–, VCII+, VCII–, VCII+/–, VCIII+, VCIII–, VCIII+/–, inverting-types of voltage conveyors such as IVCI+, IVCI–, IVCI+/–, IVCII+, IVCII–, IVCII+/–, IVCIII+, IVCIII–, IVCIII+/–, and other types with differential input such as DCVC+ (CDBA), DCVC–, and DCVC+/–. The implementation method of voltage conveyors mentioned above can be found in [196].

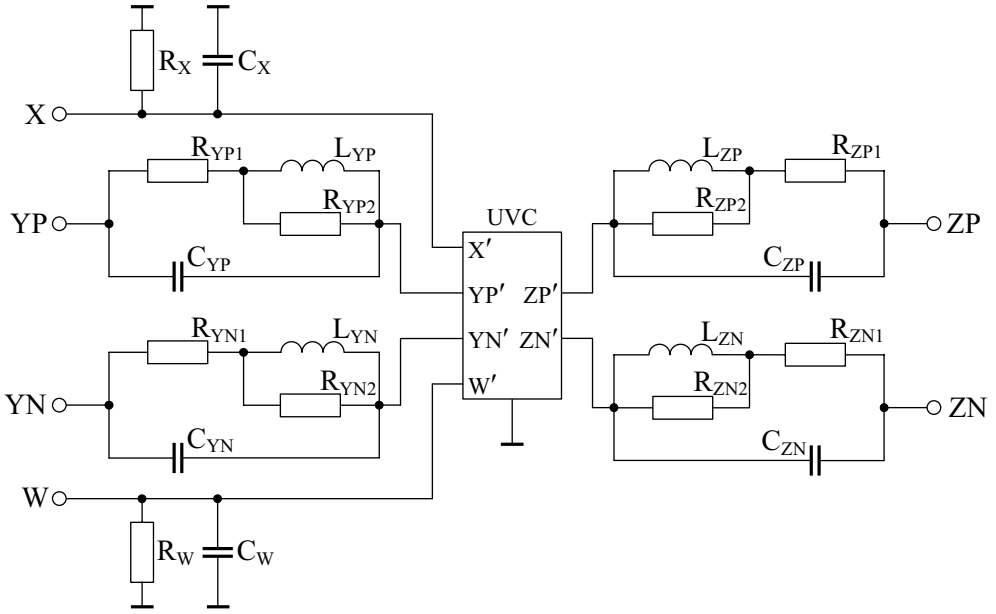


Fig. 3.4: Model of the UVC including parasitic elements [196]

Tab. 3.2: Voltage and current transfers with $f_{-3\ \mathrm{dB}}$ frequencies

Transfer	DC gain (-)	$f_{-3\ \mathrm{dB}}$ (MHz)
$V_{\mathrm{YP}}/V_{\mathrm{W}}$	0.993	52.33
$V_{\mathrm{YN}}/V_{\mathrm{W}}$	0.988	59.89
$V_{\mathrm{ZP}}/V_{\mathrm{X}}$	1.008	69.78
$V_{\mathrm{ZN}}/V_{\mathrm{X}}$	1.012	74.98
$I_{\mathrm{X}}/I_{\mathrm{YP}}$	0.987	64.36
$I_{\mathrm{X}}/I_{\mathrm{YN}}$	1.041	61.83

The novel CMOS implementation of the UVC [175] bases on the input stage of the CDTA [75] and voltage buffer/inverting voltage buffer of the ICDBA [102] as shown in Fig. 3.3. The input stage is formed by transistors M1–M24, transistors M25–M31 form the voltage buffer, and the inverting voltage buffer consists of transistors M32–M40. The transistor dimensions are listed in Tab. 3.1. The transistors are modeled by the TSMC 0.35 μm CMOS process parameters given in Tab. A.2. The DC power supply voltages are equal to $\pm$2.5 V, bias currents I_{O} are 100 μA, and the bias voltage V_{B} is –1.7 V.

As already mentioned above, in cooperation with AMI Semiconductor Czech, Ltd. (now ON Semiconductor Czech Republic, Ltd.) the universal voltage conveyor has been produced as sample series containing 50 pieces in the CMOS 0.35 μm technology under designation UVC-N1C 0520. It is supplied with $\pm$1.65 V and the linear input/output voltage and current range is $\pm$0.60 V and $\pm$0.64 mA, respectively. The

$f_{-3\ \mathrm{dB}}$ frequencies for the voltage and current transfers are summarized in Tab. 3.2 [196]. The parasitic elements of the UVC in Fig. 3.4 have been calculated using SPICE simulation program as $R_{\mathrm{X}} = 378.73$ kΩ, $C_{\mathrm{X}} = 17.41$ pF, $R_{\mathrm{YP1}} = 1.27$ Ω, $R_{\mathrm{YP2}} = 405.7$ Ω, $L_{\mathrm{YP}} = 1.45$ mH, $C_{\mathrm{YP}} = 6.12$ pF, $R_{\mathrm{YN1}} = 0.51$ Ω, $R_{\mathrm{YN2}} = 103.4$ Ω, $L_{\mathrm{YN}} = 0.35$ mH, $C_{\mathrm{YN}} = 28.9$ pF, $R_{\mathrm{W}} = 88.19$ MΩ, $C_{\mathrm{W}} = 4.19$ pF, $R_{\mathrm{ZP1}} = 1.01$ Ω, $R_{\mathrm{ZP2}} = 446.8$ Ω, $L_{\mathrm{ZP}} = 1.43$ mH, $C_{\mathrm{ZP}} = 5.84$ pF, $R_{\mathrm{ZN1}} = 0.71$ Ω, $R_{\mathrm{ZN2}} = 117.3$ Ω, $L_{\mathrm{ZN}} = 0.39$ mH, $C_{\mathrm{ZN}} = 26.8$ pF. These parameters can be found in greater detail in [137].

3.3 Differential-input buffered and transconductance amplifier (DBTA)

The differential-input buffered and transconductance amplifier (DBTA) [169], [170], [178], [180], [194], was introduced at our Department in 2009 and it belongs to the group of "universal" active elements presented above. It is a six-port active element, which schematic symbol is shown in Fig. 3.5. It has low-impedance current inputs p, n and high-impedance voltage input y. The difference of the i_p and i_n currents flows into auxiliary terminal z. The voltage v_z on this terminal is transferred into output terminal w using the VF [123] and also transformed into current using the transconductance g_m, which flows into output terminal x.

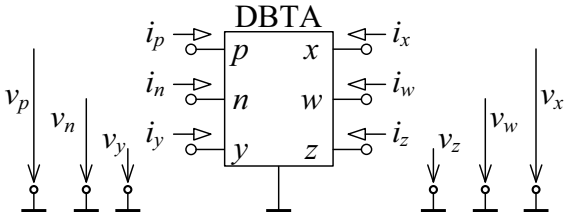


Fig. 3.5: Schematic symbol of DBTA

Relations between the individual terminals of the non-ideal DBTA can be described by following hybrid matrix:

$$\begin{bmatrix} v_p \\ v_n \\ i_y \\ i_z \\ v_w \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_p & 0 & 0 & 0 \\ 0 & 0 & \beta_n & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \gamma & 0 & 0 \\ 0 & 0 & 0 & \pm g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_p \\ i_n \\ v_y \\ v_z \\ i_w \\ v_x \end{bmatrix}, \tag{3.4}$$

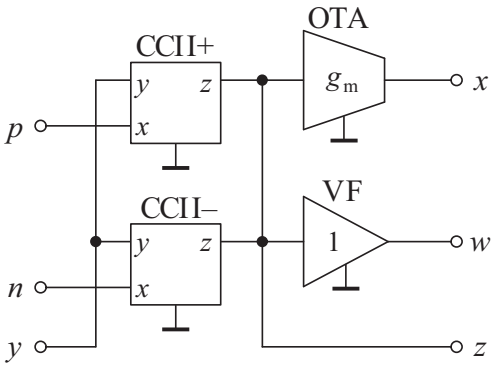


Fig. 3.6: Internal structure of differential-input buffered and transconductance amplifier

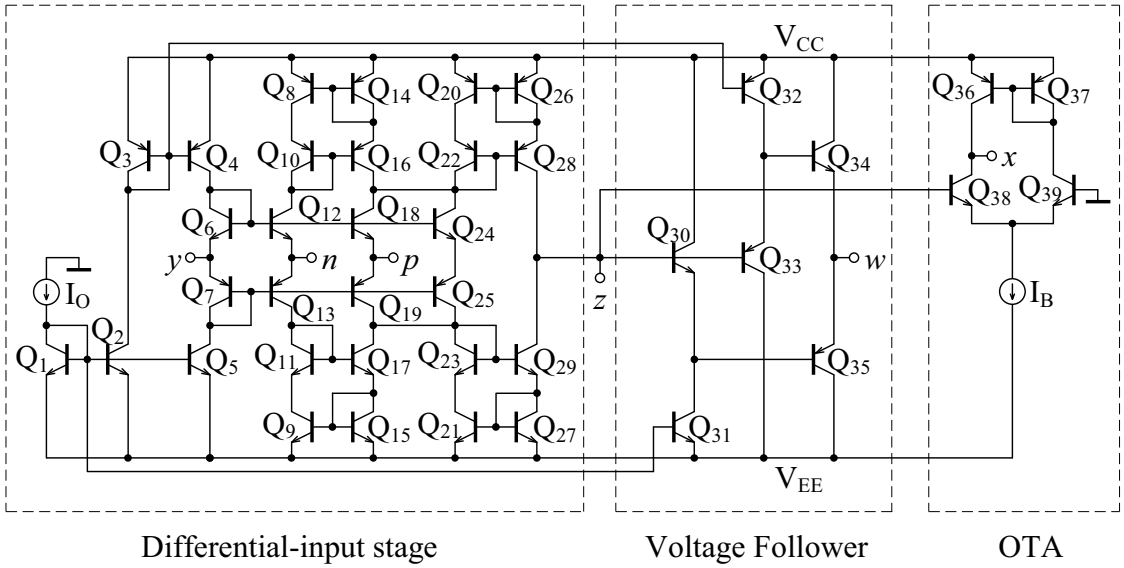


Fig. 3.7: Bipolar implementation of the DBTA [180]

where $\alpha_p = 1 - \varepsilon_i$, $\alpha_n = 1 - \varepsilon_i$ and ε_i ($|\varepsilon_i| \ll 1$) are the current tracking errors from p and n terminals to z terminal, $\beta_p = 1 - \varepsilon_v$, $\beta_n = 1 - \varepsilon_v$ and ε_v ($|\varepsilon_v| \ll 1$) are the voltage tracking errors from p and n terminals to z terminal and $\gamma = 1 - \varepsilon_v$ and ε_v ($|\varepsilon_v| \ll 1$) is the voltage tracking error from z terminal to w terminal of DBTA, respectively.

Here, it is also worth mention that our work on DBTA [170] has already been cited by international researcher Horng in [62].

The internal structure of DBTA using two CCIIs [124], one VF and one OTA is shown in Fig. 3.6 [180]. The input circuitry of the DBTA is the differential current conveyor (DCC) defined by Elwan and Soliman in 1996 [41]. By grounding the y terminal it is reduced to another active building block called modified differential current conveyor (MDCC) [41], which is a simplification of the DCC. In very few

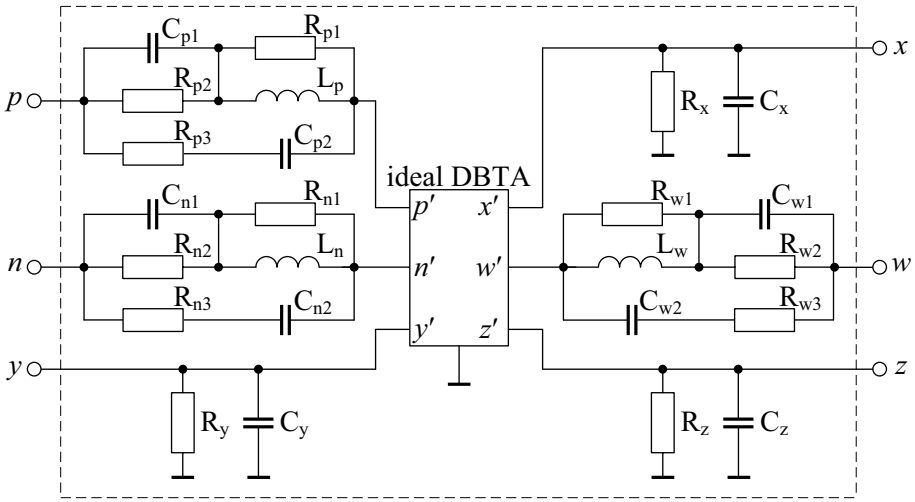


Fig. 3.8: Model of the DBTA including parasitic elements

publications the MDCC is also called current differencing unit (CDU) [78]. By connecting or grounding suitable terminals of the DBTA it helps to realize other foregoing active elements such as the CDBA [4], or the DCFA [166], which is a slight modification of CDBA, the CDTA [12], or the plus-type first- and second-generation voltage conveyors (VCI+, VCII+) [51], [106], and also their inverting versions IVCI+, IVCII+ [106], and others. The DBTA also helps to define novel types of voltage conveyors, especially the first-generation differential current voltage conveyors (DCVCIs).

The bipolar implementation of the DBTA is shown in Fig. 3.7 [180]. The differential-input stage is formed by transistors Q_1–Q_{29}, transistors Q_{30}–Q_{35} form the VF, and the OTA consists of transistors Q_{36}–Q_{39}. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The DC supply voltages are $+V_{\rm CC} = -V_{\rm EE} = 2$ V. Bias current $I_{\rm O} = 400$ μA has been chosen. The transconductance g_m of DBTA can be set by current $I_{\rm B} = 2g_m V_{\rm T}$, where $V_{\rm T}$ is the thermal voltage (approximately 26mV at 27°C). The parasitic elements of the proposed DBTA in Fig. 3.7 have been computed using SPICE simulation program. The parasitic elements in Fig. 3.8 are computed as $C_{\rm p1} = C_{\rm n1} = C_{\rm w1} =$ 3.08 pF, $C_{\rm p2} = 2.73$ pF, $C_{\rm n2} = 2.64$ pF, $C_{\rm y} = 4.41$ pF, $C_{\rm z} = 2.04$ pF, $C_{\rm w2} = 1.65$ pF, $C_{\rm x} = 1.06$ pF, $L_{\rm p} = L_{\rm n} = 119.91$ nH, $L_{\rm w} = 112.03$ nH, $R_{\rm p1} = R_{\rm n1} = 2.84$ kΩ, $R_{\rm p2} = R_{\rm n2} = R_{\rm w2} = 39.34$ Ω, $R_{\rm p3} = R_{\rm n3} = 205.67$ Ω, $R_{\rm y} = 34.17$ kΩ, $R_{\rm z} = 228.21$ kΩ, $R_{\rm w1} = 1.09$ kΩ, $R_{\rm w3} = 281.37$ Ω, $R_{\rm x} = 1.49$ MΩ. The maximum values of terminal voltages and terminal currents without producing significant distortion are computed as ±365 mV and ±605 μA, respectively. The DC voltage gains $\beta_p \cong \beta_n \cong 0.961$ and $\gamma \cong 0.962$ with bandwidths $f_{\beta p} \cong f_{\beta n} \cong 381.1$ MHz and $f_\gamma \cong 417.1$ MHz.

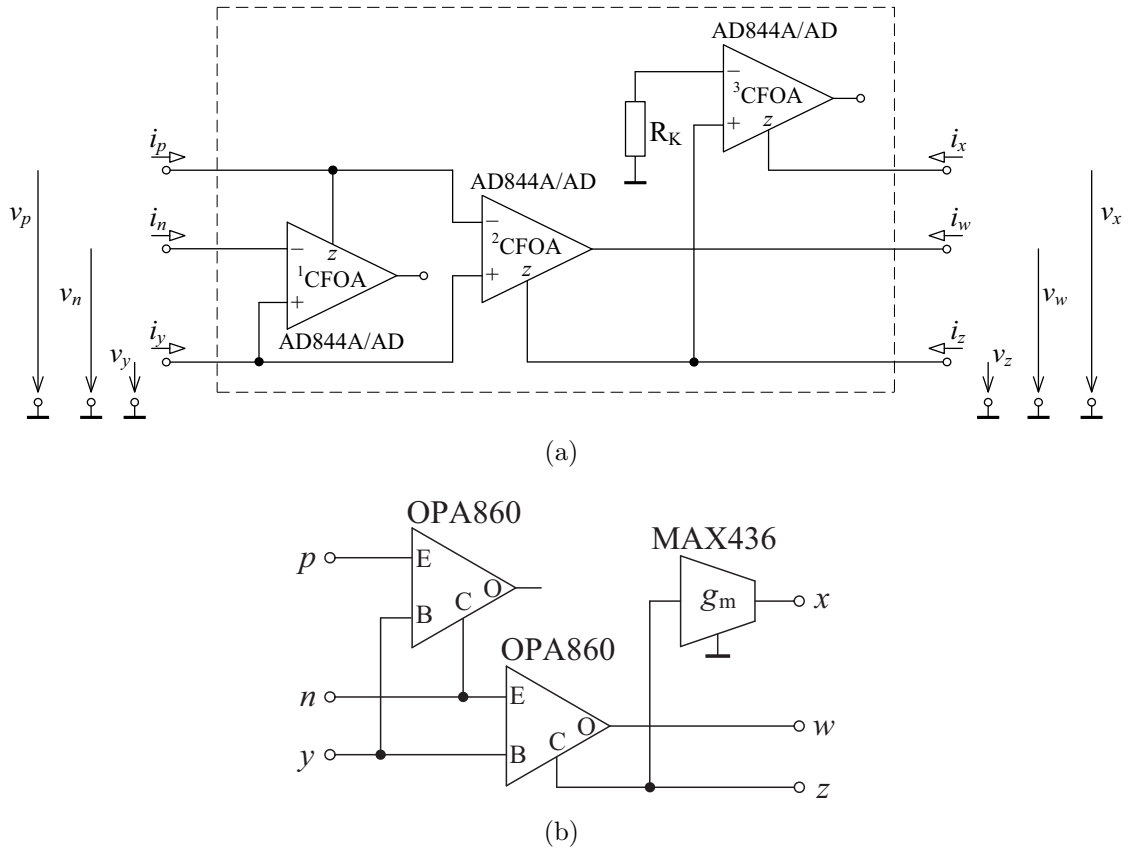


Fig. 3.9: Implementation of DBTA by commercially available amplifiers: (a) using three CFOAs (AD844s), (b) using OPA860s and MAX436

The DC current gains $\alpha_p \cong \alpha_n \cong 0.989$ with bandwidths $f_{\alpha p} \cong 170.9$ MHz and $f_{\alpha n} \cong 173.9$ MHz. The transconductance $g_m \cong 0.951$ mA/V with the bandwidth $f_{gm} \cong 85.8$ MHz.

In the literature for the implementation of the DBTA with commercially available integrated circuits two different structures were published. In [178] the DBTA circuit is constructed with three commercially available CFOAs AD844 ICs by Analog Devices, as shown in Fig. 3.9(a). Note that, the OTA [53] in the structure of the DBTA is replaced by ^{3}CFOA, where the transconductance g_m is defined by resistor R_K [190]. The second structure is shown in Fig. 3.9(b). In this case the commercially available amplifiers OPA860 and MAX436 are used [180]. Both structures are further used in simulations and/or experimental measurements.

3.4 Operational transconductance amplifier (OTA)

The OTA were made commercially available for the first time in 1969 by RCA. The first publications with OTA came out in 1985, when authors in [53] presented to

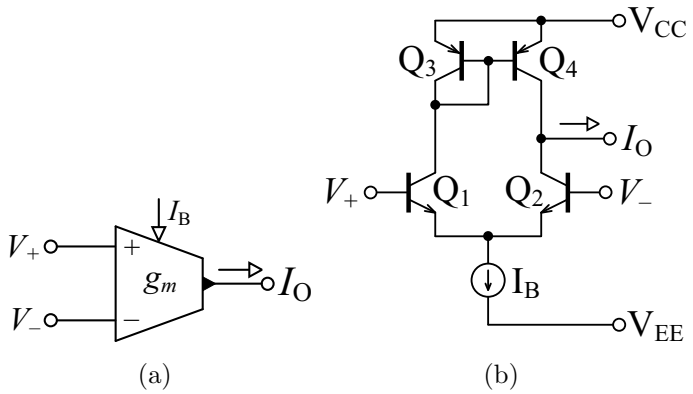


Fig. 3.10: (a) Schematic symbol (b) and bipolar implementation of OTA

the general public the new CMOS OTA architectures and new filter realizations. The schematic symbol and simple bipolar implementation of OTA are shown in Fig. 3.10(a) and Fig. 3.10(b). In Fig. 3.10(b), transistors Q_1 and Q_2 operate as a differential amplifier to convert an input voltage to an output current and transistors Q_3 and Q_4 work as a simple current mirror when I_{B} is an input bias current. The ideal OTA is a voltage-controlled current source (VCCS) characterized by transconductance g_m. The output current of the OTA is given by the following equation [128]:

$$I_{\mathrm{O}} = g_m(V_+ - V_-), \tag{3.5}$$

where V_+ and V_- are the voltages on non-inverting and inverting inputs of OTA with respect to the ground. The ideal OTA amplifier is characterized by a finite, frequency-independent transconductance g_m while its input and output impedances are theoretically infinite. For a bipolar OTA in Fig. 3.10(b), the transconductance can be expressed as:

$$g_m = \frac{I_{\mathrm{B}}}{2V_{\mathrm{T}}}, \tag{3.6}$$

where the V_{T} is the thermal voltage (approximately 26 mV at 27°C) and the I_{B} is the control current adjusting the transconductance g_m of the OTA.

Currently, the OTA elements are supplied on the market by many manufacturers [192]. A commercially available OTA element is the circuit LT1228 (Linear Technology) or MAX435 (MAXIM-Dallas Semiconductor), which is a high-speed wideband transconductance amplifier (WTA) with high-impedance inputs and output. Due to its unique performance features, it is suitable for a wide variety of applications such as high-speed instrumentation amplifiers, wideband, high-speed RF filters, and high-speed differential line driver and receiver applications.

3.5 Programmable current amplifier (PCA)

The programmable current amplifier (PCA) was presented in 2005 [92] at our Department and it is ready to be manufactured by ON Semiconductor Czech Republic, Ltd. in the CMOS 0.35 μm technology, based on the concept presented in [199], and labeled as COAK-NAA. In general, the PCA element (Fig. 3.11) can be characterized by the following hybrid matrix:

$$\begin{bmatrix} v_x \\ i_{z1} \\ i_{z2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ b_1 n & 0 & 0 \\ b_2 n & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ v_{z1} \\ v_{z2} \end{bmatrix}, \tag{3.7}$$

where $b_1, b_2 \in \{1, -1\}$ and n represents the current gain, referred to as the "mu-factor" [183], [189], [199]. Depending on the values of b_1 and b_2 three variants of PCA are possible, namely PCA+/+, PCA+/– and PCA–/–, of which PCA+/– has been used in [183], [189], and [199] for creating CM biquadratic filters and oscillators.

The cascode npn current mirror with adjustable current gain by the external bias currents is shown in Fig. 3.12 [189]. The I_{in} and I_{out} are the input and output signal currents. Transistors Q_1–Q_4 represent a classical translinear loop, and the currents I_1 and I_2 are the external DC bias currents [148]. In addition, the cascode stages Q_5 and Q_6 provide the high output impedance and also lead to minimize the severe peaking of the frequency responses [44]. Applying the translinear principle and

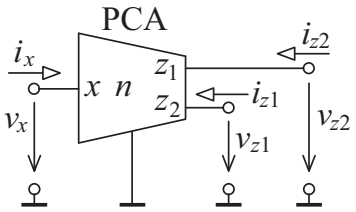


Fig. 3.11: Schematic symbol of general PCA

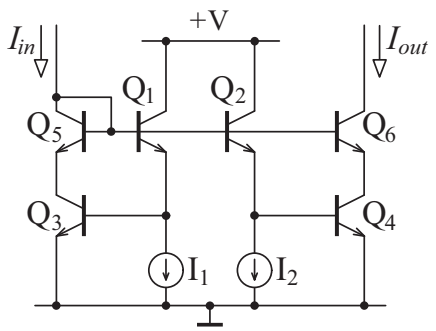


Fig. 3.12: Cascode npn current mirror with adjustable current gain

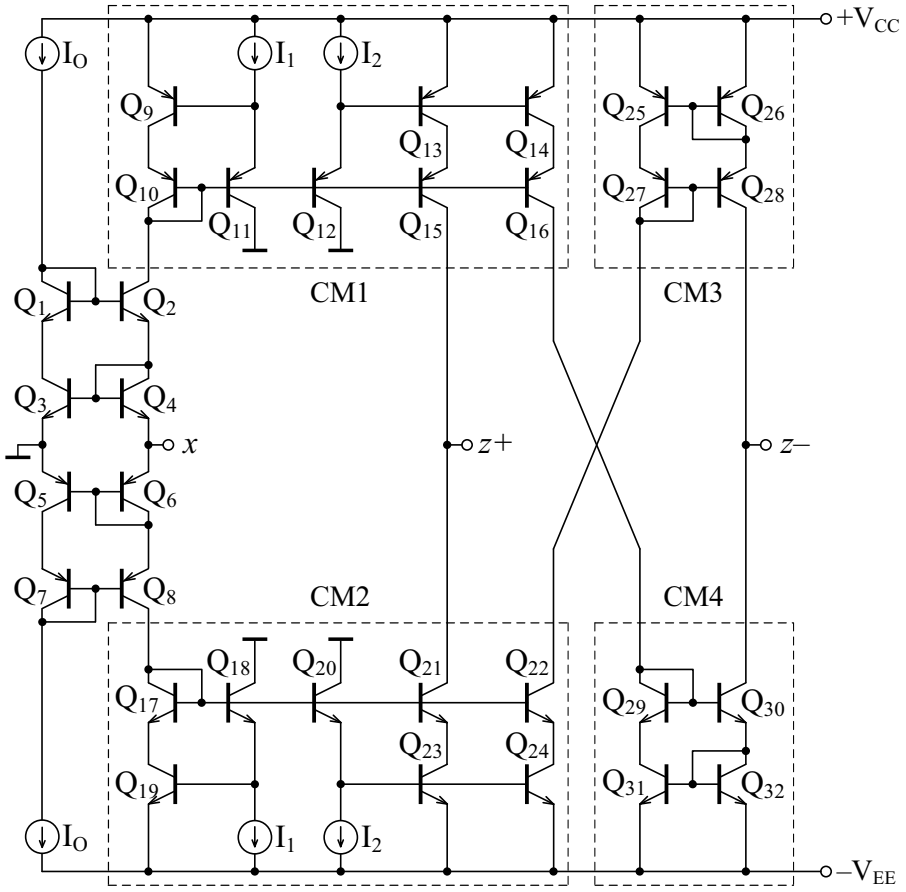


Fig. 3.13: Bipolar implementation of the PCA+/– [189]

assuming that all the transistors are well matched with the common-emitter current gains $\beta \gg 1$, then the relationship of the collector currents can be characterized by the following equation:

$$I_{C1}I_{C3} = I_{C2}I_{C4}, \tag{3.8}$$

where $I_{C1} = I_1$, $I_{C2} = I_2$, $I_{C3} = I_{in}$, and $I_{C4} = I_{out}$. Therefore, the output current I_{out} of this circuit becomes:

$$I_{out} = nI_{in}, \tag{3.9}$$

where n is the current gain of the mirror ("mu-factor") and equals to the ratio of the external bias currents I_1/I_2.

Bipolar implementation of the presented PCA+/– based on the second-generation current conveyor with controlled current gain [44] is shown in Fig. 3.13 [189]. Group of transistors Q_1–Q_8 form an improved translinear cell, in which Q_3–Q_6 function as a dual translinear loop. Ideally, it is required that the pair of transistors Q_3–Q_4 and Q_5–Q_6 are closely matched. The translinear cell performs a current follower, where it allows an input current i_x to source and sink at the terminal x. By two

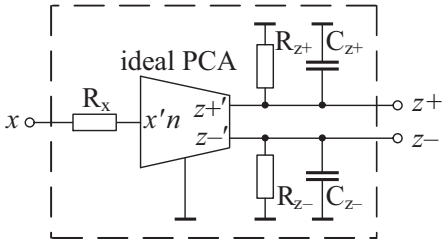


Fig. 3.14: Model of the PCA+/– including parasitic elements

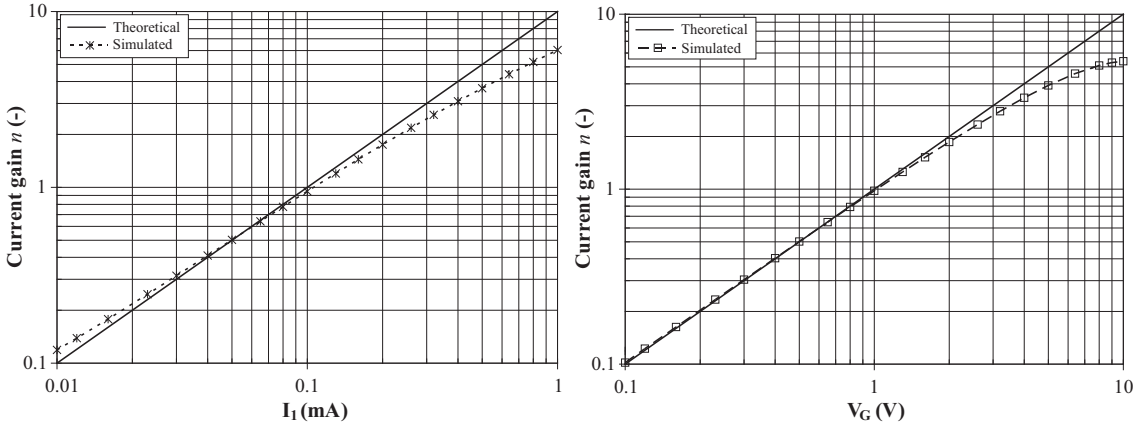


Fig. 3.15: Possibility of adjusting the current gain n of the PCA+/–: (a) by the I_1 (when I_2=100 μA) of the bipolar implementation shown in Fig. 3.13 and (b) by V_G of the implementation in [183]

complementary variable gain current mirrors CM1 and CM2, the current i_x flowing through the port x will be reflected and inverted to the ports $z+$ and $z-$ with the current transfer ratio of n ($= i_z/i_x = I_1/I_2$). The output impedance at the port x is low, since it is looking into the emitters of translinear cell's transistors, while the output impedances of the ports $z\pm$ are high due to the effective parallel combination of output impedances of the current mirrors. Therefore, this device will provide a current transfer between ports x and $z\pm$ that the gain value is equal to n as it is defined by (3.7).

In the BJT implementation of the PCA+/– shown in Fig. 3.13 the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The DC supply voltages were taken as ±3 V. Bias currents I_O = 200 μA and $I_1 = I_2$ = 100 μA have been chosen. The parasitic elements in Fig. 3.14 have been computed as R_x = 69.816 Ω, R_{z+} = 14.280 kΩ, R_{z-} = 13.961 kΩ, C_{z+} = 2.829 pF, and C_{z-} = 1.359 pF. The DC current gains are $\beta_{z+} \cong 0.9343$ and $\beta_{z-} \cong 0.9346$ with bandwidths $f_{\beta_{z+}} \cong$ 125.053 MHz and $f_{\beta_{z-}} \cong$ 132.304 MHz. The maximum values of

terminal currents without producing significant distortion have been computed as $i_{z\pm,max} \cong 19.684$ mA. The total power dissipation of the PCA+/– is calculated as 5.9 mW.

The possibility of adjusting the current gain n by the external bias current I_1 of the proposed PCA+/– is shown in Fig. 3.15(a). In simulations the external bias current I_1 has been adjusted in the interval from 10 μA to 1 mA (equal to gain $n = 0.1$ to 10) whereby I_2 is set to be constant at 100 μA. Fig. 3.15(b) shows the possibility of adjusting the current gain n by external voltage V_G of the previously presented implementation of the PCA+/– [183], where current multiplier EL2082 [35] followed by the BJT structure of the CCII+/– [47] with grounded Y terminal. In this simulation the external voltage V_G has been adjusted in the same current gain interval $n = 0.1$ to 10 ($V_G = 0.1$ V to 10 V). From simulations it is evident that in both cases the most exact result can be obtained for current gain $n = 0.4$ to 1. According to [35], the gain error of the current multiplier EL2082 for $V_G = 2$ V is about –3.8 %. In the case of the proposed bipolar implementation, the gain error can be affected by using not precisely matched bipolar transistors.

3.6 Current follower transconductance amplifier (CFTA)

When the CDTA has been introduction in 2003 [12], it has been considered to be a versatile active building block for current-mode signal processing circuits. Analogous to the CDBA [4], the input circuitry of the CDTA is also formed by the CDU, which is followed by the OTA [53]. In the point of view of the low power dissipation and manufacturing cost, it is important to keep the internal structure transistor count and the count of ABBs at minimum. The earlier reported circuits in [12], [15], [11], [38], [139], [143], [153], do not fully use the potential of the CDTAs, since one of the input terminals p or n is not used. This may cause some noise injection into the monolotic circuit [77]. Thus, to avoid this problem, the CDTA has been simplified by replacing the CDU by a simple current follower (CF) or inverter (CI). The appropriate novel ABBs are called current follower transconductance amplifier (CFTA) [19], [167], [181], [184], and inverted current follower transconductance amplifier (ICFTA) [183], which was in [19] also introduced as current inverter transconductance amplifier (CITA).

Here, it is worth mention that our papers on CFTA have already been cited by international researchers Lahiri in [88], Mongkolwai *et al.* in [108], Sirirat *et al.* in [129] and [130], and Tangsrirat in [140].

The generalized CFTA (GCFTA) element consists of an input CF (positive or

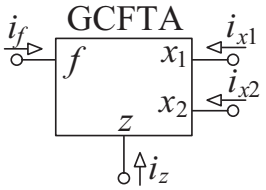


Fig. 3.16: Schematic symbol of GCFTA

Tab. 3.3: Types of CFTAs

Type	a	b_1	b_2
CFTA+/+	1	1	1
CFTA+/–	1	1	–1
CFTA–/–	1	–1	–1
ICFTA+/+	–1	1	1
ICFTA+/–	–1	1	–1
ICFTA–/–	–1	–1	–1

negative) that transfers the input current to the z terminal and a dual-output OTA stage, which is used to convert the voltage at the z terminal to dual-output currents [193]. The transconductance parameter g_m corresponds for the positive output and $-g_m$ for the negative output. In general, the equations describing an ideal GCFTA (Fig. 3.16) are:

$$\begin{bmatrix} v_f \\ i_z \\ i_{x1} \\ i_{x2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ a & 0 & 0 & 0 \\ 0 & b_1 g_m & 0 & 0 \\ 0 & b_2 g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_{x1} \\ v_{x2} \end{bmatrix}, \tag{3.10}$$

where $a,\ b_1,\ b_2 \in \{1, -1\}$. Hence, six different types of CFTA variants can be defined, which are listed in Tab. 3.3.

The CFTA+/– can be easily implemented using commercially available active components such as CFOA (e.g. AD844AN) and dual-output OTA (e.g. MAX435), as given in Fig. 3.17(a) [167], where g_m denotes the transconductance of the OTA and is a function of the bias current. In applications, where two current outputs are not sufficient, the multiple-output CFTA (MO-CFTA) can be used. The realization of the MO-CFTA via the UCC-N1B 0520 IC is shown in Fig. 3.17(b). The CF is realized by using the CCII+/– and the multi-output OTA is realized using the UCC, with the transconductance g_m defined by resistor $\mathrm{R_K}$ [190]. Depending on the direction of the currents at the x terminals, it is possible to realize the following

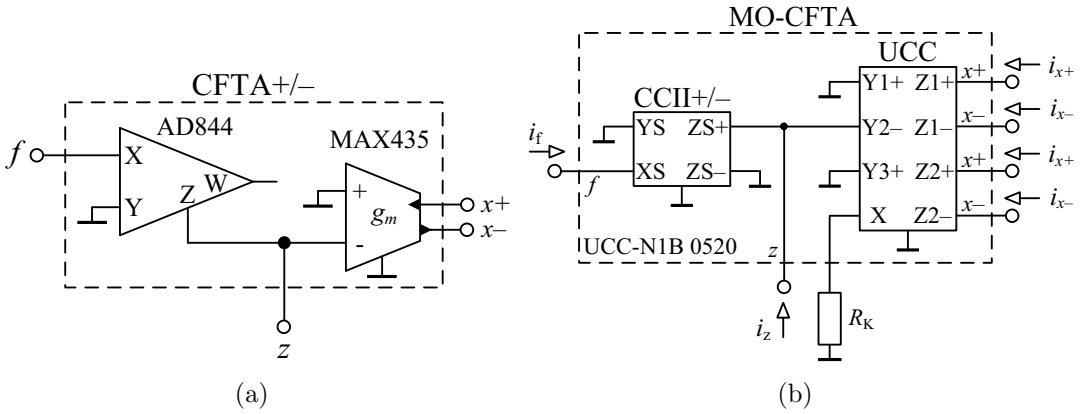


Fig. 3.17: Realization of the (a) CFTA+/– via commercially available amplifiers and (b) multi-output CFTA via the UCC-N1B 0520 IC

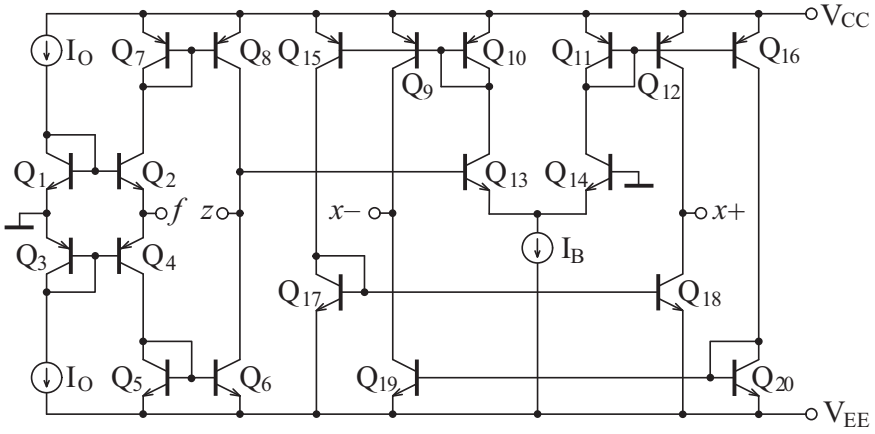


Fig. 3.18: Bipolar implementation of CFTA+/–

MO-CFTAs: CFTA+/–/+, CFTA–/+/–, and CFTA+/–/+/–.

The bipolar implementation of the CFTA+/– is shown in Fig. 3.18 [193]. The input circuitry (e.g. CF) is formed by transistors Q_1–Q_6 and the dual-output OTA consists of transistors Q_7–Q_{20}. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. Bias current $I_O = 400$ μA has been chosen. The transconductance g_m of CFTA+/– can be set by current $I_B = 2g_m V_T$, where V_T is the thermal voltage (approximately 26mV at 27°C). The DC supply voltages are $+V_{CC} = -V_{EE} = 2$ V.

The maximum values of terminal voltages and terminal currents of the CFTA+/– without producing significant distortion are computed as ±29.21 mV and ±16.81 mA, respectively. The DC current gain of the CFTA+/– $\alpha \cong 0.9852$ with bandwidth $f_\alpha \cong 135.225$ MHz and the transconductance $g_m \cong 0.9894$ mA/V (at $I_B = 52$ μA) with the bandwidth $f_{g_m} \cong 31.469$ MHz.

3.7 Z-copy current follower transconductance amplifier (ZC-CFTA)

The first mention about the z-copy current follower transconductance amplifier (ZC-CFTA) (Fig. 3.19) can be found in [18]. Compared to the conventional CFTA, the current i_z is copied to the current i_{zc}. Relations between the individual terminals of the ZC-CFTA can be described by the following hybrid matrix [179]:

$$\begin{bmatrix} v_f \\ i_z \\ i_{zc} \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ \alpha & 0 & 0 & 0 & 0 \\ \gamma & 0 & 0 & 0 & 0 \\ 0 & +g_m & 0 & 0 & 0 \\ 0 & -g_m & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_{zc} \\ v_{x+} \\ v_{x-} \end{bmatrix}, \tag{3.11}$$

where $\alpha = 1 - \varepsilon_i$ and $\gamma = 1 - \varepsilon_j$. Here, ε_i and ε_j ($|\varepsilon_i|, |\varepsilon_j| \ll 1$) are current tracking errors from f terminal to z and zc terminals, respectively.

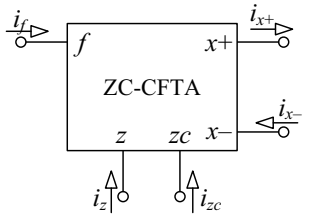


Fig. 3.19: Schematic symbol of ZC-CFTA

The BJT implementation of the ZC-CFTA can be easily obtained by slight modification of the structure in Fig. 3.18. In this case it is necessary to add a transistor pair parallel to transistors Q_6 and Q_8.

3.8 Current-controlled current follower transconductance amplifier (CCCFTA)

The current-controlled current follower transconductance amplifier (CCCFTA) was introduced at our Department in 2009 [171]. The properties of the CCCFTA (Fig. 3.20) are similar to the conventional CFTA expect that input voltage of CCCFTA is not zero and the CCCFTA has finite input intrinsic resistance R_f at the f input terminal, which can be controlled by bias current I_O. Relations between the individual terminals of the CCCFTA can be described by the following hybrid

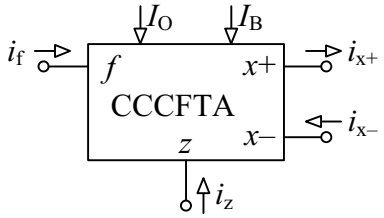


Fig. 3.20: Schematic symbol of CCCFTA

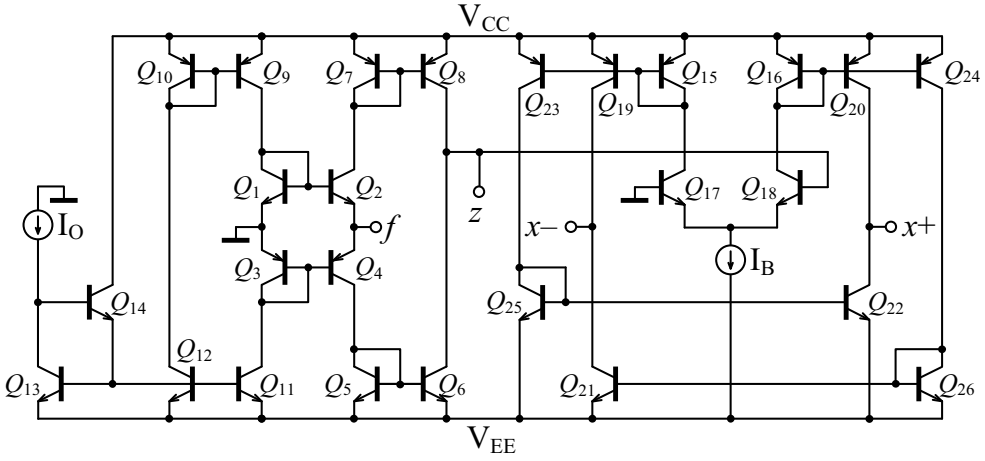


Fig. 3.21: BJT internal structure of CCCFTA

matrix [182]:

$$\begin{bmatrix} v_f \\ i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} R_f & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & g_m & 0 & 0 \\ 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_{x+} \\ v_{x-} \end{bmatrix}, \tag{3.12}$$

where the intrinsic resistance R_f and the transconductance g_m can be defined as follows:

$$R_f = \frac{V_T}{2I_O} \quad \text{and} \quad g_m = \frac{I_B}{2V_T}, \tag{3.13}$$

respectively. Here the V_T is the thermal voltage (approximately 26 mV at 27°C), the I_O is the bias current to control the intrinsic resistance of the input terminal f, and the I_B is the control current adjusting the transconductance g_m of the CCCFTA.

The bipolar implementation of the CCCFTA is shown in Fig. 3.21 [171]. The input current-controlled current follower stage is formed by transistors Q_1–Q_{14} and transistors Q_{15}–Q_{26} form the output transconductance stage. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The DC supply voltages are $+V_{CC} = -V_{EE} = 2$ V.

3.9 Z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA)

The ZC-CCCITA (z-copy current-controlled current inverting transconductance amplifier) is recently presented ABB at our Department [185], which is a derivative of the conventional ZC-CITA [14]. It essentially consists of an input negative current-controlled current follower (i.e. current-controlled current inverter) stage that transfers the input current to the z and zc terminals and a transconductance amplifier stage, which converts the voltage at the z terminal to output current at the x terminal. The schematic symbol of ZC-CCCITA is shown in Fig. 3.22 and the hybrid matrix is as follows:

$$\begin{bmatrix} v_f \\ i_z \\ i_{zc} \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} R_f & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & g_m & 0 & 0 & 0 \\ 0 & -g_m & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_{zc} \\ v_{x+} \\ v_{x-} \end{bmatrix}. \tag{3.14}$$

In (3.14), the intrinsic resistance R_f and the transconductance g_m can be defined as:

$$R_f = \frac{V_\mathrm{T}}{2I_\mathrm{O}} \quad \text{and} \quad g_m = \frac{I_\mathrm{B}}{2V_\mathrm{T}}, \tag{3.15}$$

respectively. Here the V_T is the thermal voltage (approximately 26 mV at 27°C), the I_O is the bias current to control the intrinsic resistance of the input terminal f, and the I_B is the control current adjusting the transconductance g_m of the ZC-CCCITA.

The ZC-CCCITA has the following non-idealities:

- The intrinsic resistance R_f appearing at terminal f, however, in our case this non-ideality is advantageously used and it is adjustable through the bias current of the current inverting stage.
- $i_z = -\beta_1 i_f$ and $i_{zc} = -\beta_2 i_f$, where β_1 and β_2 represent current gains that differ from their ideally unity values by current tracking errors.

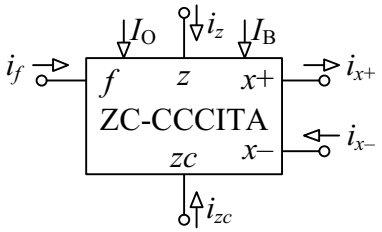


Fig. 3.22: Schematic symbol of ZC-CCCITA

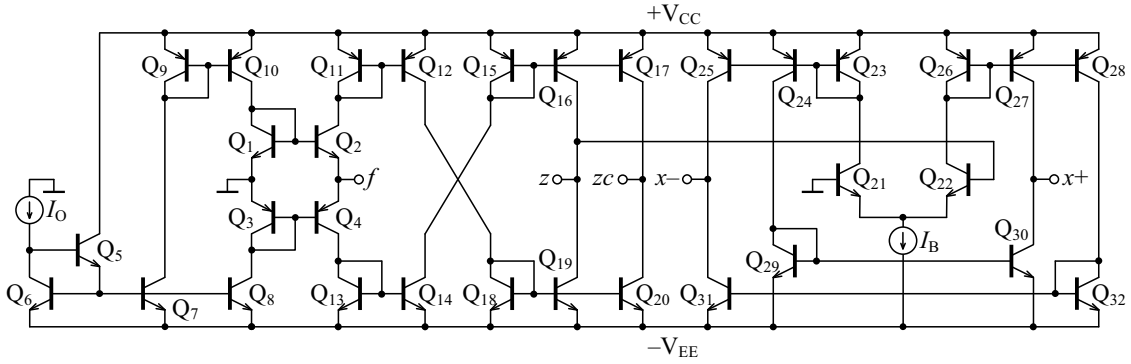
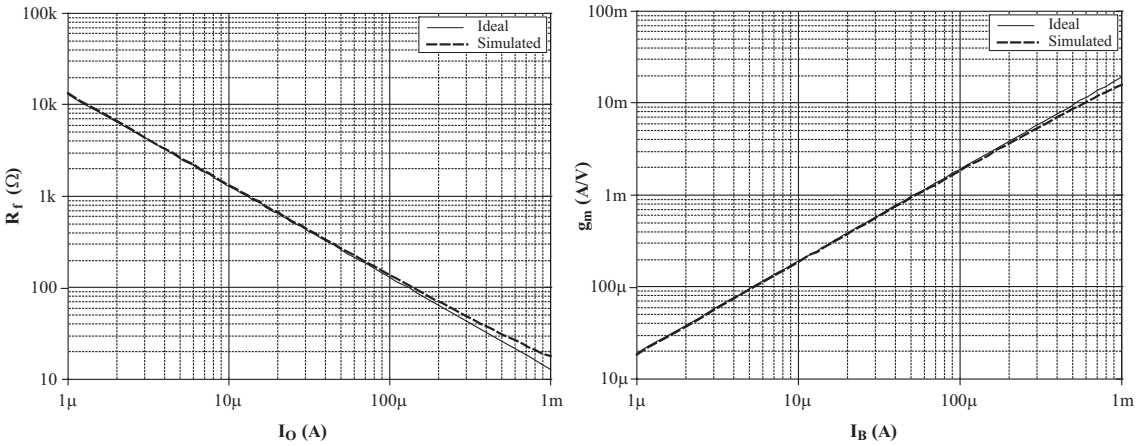


Fig. 3.23: BJT internal structure of ZC-CCCITA [185]



(a) (b)

Fig. 3.24: (a) Intrinsic resistance at input terminal R_f relative to I_{O}, (b) transconductance value g_m relative to I_{B}

- The parasitic resistance R_z and parasitic capacitance C_z appearing between the high-impedance z terminal and ground. Similarly, the parasitic resistance R_{zc} and parasitic capacitance C_{zc} appearing between the high-impedance zc terminal and ground.
- The parasitic resistance R_x and parasitic capacitance C_x appearing between the high-impedance x terminal of the transconductance amplifier and ground.

The bipolar implementation of the ZC-CCCITA is shown in Fig. 3.23 [185]. The input negative current-controlled current follower stage is formed by transistors Q_1–Q_{20} and transistors Q_{21}–Q_{32} form the output transconductance stage. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The DC supply voltages are $+V_{\mathrm{CC}} = -V_{\mathrm{EE}} = 1.45$ V. Ideal and simulated intrinsic resistance R_f at input terminal f and transconductance value g_m relative to I_{O} and I_{B}, respectively, are shown in Fig. 3.24. From Fig. 3.24 it can be seen that both

values can be easily controlled through almost three decades.

3.10 Generalized current follower differential input transconductance amplifier (GCFDITA)

In one of more recent publication [17], authors introduced a modified version of the GCFTA [183] with buffered voltage outputs wherein the transconductance of conventional GCFTA is changed to differential input transconductance amplifier. Here presented new ABB is called generalized current follower differential input transconductance amplifier (GCFDITA), which is a derivative of the circuit presented in [17]. Compared to [17], the new ABB does not have a buffered voltage output terminal. An important advantage of GCFDITA is also that it can be easily created using commercially available amplifiers, to be specific, the input circuitry by AD844 ICs of Analog Devices or OPA860s of Texas Instruments and the balanced-output OTA by MAX435 of Maxim Semiconductors.

The generalized current follower differential input transconductance amplifier (GCFDITA) consists of an input positive or negative current follower that transfers the input current at terminal f to the z terminal and a balanced-output differential input transconductance amplifier (BO-DITA) stage, which is used to convert the difference voltage between the z and v terminals to balanced output currents. The transconductance parameter g_m corresponds for the positive output and $-g_m$ for the negative output. The schematic symbol of GCFDITA is shown in Fig. 3.25. In general, the hybrid matrix characterizing an ideal GCFDITA is:

$$\begin{bmatrix} v_f \\ i_z \\ i_v \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ a & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & g_m & -g_m & 0 & 0 \\ 0 & -g_m & g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_v \\ v_{x+} \\ v_{x-} \end{bmatrix}, \tag{3.16}$$

where $a \in \{1, -1\}$ and $g_m = \frac{I_B}{2V_T}$. Here the V_T is the thermal voltage (approximately

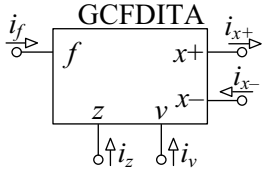


Fig. 3.25: Schematic symbol of GCFDITA

26 mV at 27°C) and the I_{B} and is control current adjusting the transconductance g_m. Depending on the values of a, two variants of GCFDITA are possible, namely current follower differential input transconductance amplifier (CFDITA) for $a = 1$ and current inverter differential input transconductance amplifier (CIDITA) for $a = -1$.

For a complete analysis of the circuit, it is important to take into account the non-idealities of the ABB. Here is provided the non-ideal analysis for the CIDITA, however, similar analysis can be also carried out for the CFDITA. Considering the non-idealities of the CIDITA, hybrid matrix in (3.16) changes as follows:

$$\begin{bmatrix} v_f \\ i_z \\ i_v \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ -\alpha & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & \beta_1 g_m & -\beta_1 g_m & 0 & 0 \\ 0 & -\beta_2 g_m & \beta_2 g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} i_f \\ v_z \\ v_v \\ v_{x+} \\ v_{x-} \end{bmatrix}, \tag{3.17}$$

where $\alpha = 1 - \varepsilon_1$, $\beta_1 = 1 - \varepsilon_2$, and $\beta_2 = 1 - \varepsilon_3$. The parameters ε_1, ε_2, and ε_3 ($|\varepsilon_1|, |\varepsilon_2|, |\varepsilon_3| \ll 1$) denote the current tracking error of the current inverting stage and BO-DITA, respectively. Furthermore, the following parasitic impedances can be considered:

- The non-zero parasitic input resistance at terminal f of the CIDITA is represented by R_f.
- The parasitic resistance R_z and parasitic capacitance C_z appearing between the high output impedance z terminal of the CIDITA and ground.
- The parasitic resistance R_v and parasitic capacitance C_v appearing between the high input impedance v terminal of the CIDITA and ground.
- The parasitic impedances appearing between the high-impedance x terminals of the CIDITA and ground.

The bipolar implementation of CIDITA is shown in Fig. 3.26. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The DC supply voltages are $+\mathrm{V_{CC}} = -\mathrm{V_{EE}} = 2$ V. Bias currents $I_{\mathrm{O}} = 400$ μA have been chosen. In the simulations the SPICE program have been used. The DC current gain $\alpha \cong 0.9938$ with bandwidth $f_\alpha \cong 93.744$ MHz and the transconductance $g_m \cong 0.9894$ mA/V (at $I_{\mathrm{B}} = 52$ μA) with the bandwidth $f_{g_m} \cong 31.085$ MHz. The maximum value of terminal currents without producing significant distortion are computed as ± 16.09 mA.

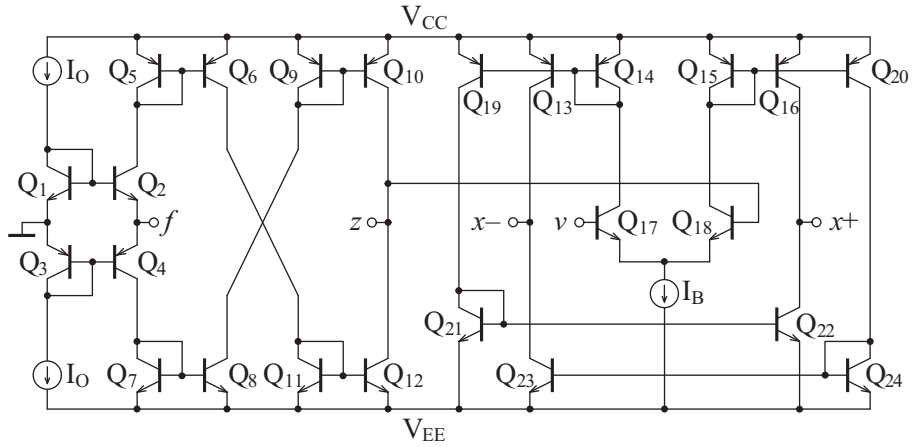


Fig. 3.26: Bipolar implementation of CIDITA

3.11 Current backward transconductance amplifier (CBTA)

The current backward transconductance amplifier (CBTA) is recently presented ABB that versatility has already been demonstrated in [8] in creating CM leapfrog ladder filters and in [119] in proposing a single-input three-outputs (SITO) CM filter, a single-input four-output (SIFO) VM filter, and three-input single-output (TISO) VM filter. The schematic symbol of the CBTA is shown in Fig. 3.27, where p and n are input terminals and w, $z+$, $z-$ are output terminals. The input impedances for the ideal CBTA are infinite at p, n, $z+$, and $z-$ terminals and zero at w terminal. Relations between the individual terminals of the CBTA can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ v_w \\ i_p \\ i_n \end{bmatrix} = \begin{bmatrix} g_m & -g_m & 0 & 0 & 0 \\ -g_m & g_m & 0 & 0 & 0 \\ 0 & 0 & \mu_w & 0 & 0 \\ 0 & 0 & 0 & 0 & \alpha_p \\ 0 & 0 & 0 & 0 & -\alpha_n \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_{z+} \\ v_{z-} \\ i_w \end{bmatrix}, \tag{3.18}$$

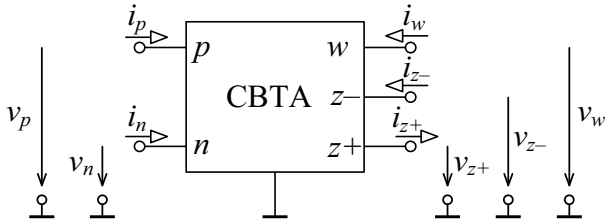


Fig. 3.27: Schematic symbol of current backward transconductance amplifier

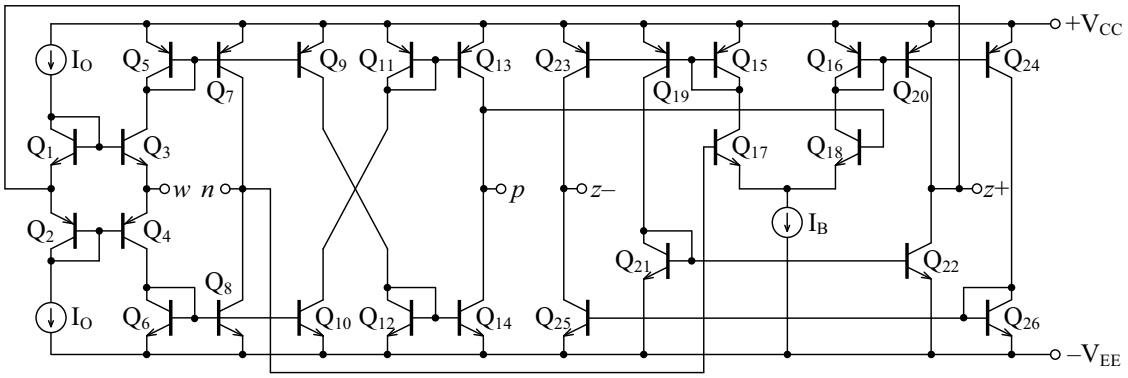


Fig. 3.28: BJT implementation of the CBTA [188]

where g_m, α_p, α_n, and μ_w are the transconductance gain, current and voltage gains of the CBTA, respectively. In the ideal case, the current and voltage gains are $\alpha_p = \alpha_n = 1$ and $\mu_w = 1$. In practice, they can be expressed as $\alpha_p = 1 - \varepsilon_p$, $\alpha_n = 1 - \varepsilon_n$, $\mu_w = 1 - \varepsilon_v$. Here, ε_p and ε_n ($|\varepsilon_p|$, $|\varepsilon_n| \ll 1$) and ε_v ($|\varepsilon_v| \ll 1$) denote current and voltage tracking error of the CBTA, respectively.

According to the above terminal equations, current through $z+$ and $z–$ terminals follows the difference of the voltages at p and n terminals by a transconductance g_m and $–g_m$, respectively. Hence, $z+$ and $z–$ terminals are current outputs. The p terminal is named as positive (non-inverting) input and n terminal as negative (inverting) input. Voltage of w terminal follows the voltage of $z+$.

An important advantage of CBTA is that it can be easily created using familiar ABBs like CCII+/– [124] and BOTA [53]. A new BJT implementation of CBTA with supply voltages of ±2 V is given in Fig. 3.28 [188]. The CCII+/– is formed by transistors Q_1–Q_{14} and the BOTA consists of transistors Q_{15}–Q_{26}. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. Bias current $I_\mathrm{O} = 400$ μA has been chosen. The transconductance g_m of CBTA can be set by current $I_\mathrm{B} = 2g_m V_\mathrm{T}$, where V_T is the thermal voltage (approximately 26 mV at 27°C).

The maximum values of terminal voltages and terminal currents without producing significant distortion have been computed using SPICE simulation program as ±28.179 mV and ±16.159 mA, respectively. The DC voltage gain is $\mu_w \cong 0.9996$ with bandwidth $f_{\mu_w} \cong 879.923$ MHz. The DC current gains are $\alpha_p \cong 0.984$ and $\alpha_n \cong 0.976$ with bandwidths $f_{\alpha_p} \cong 72.495$ MHz and $f_{\alpha_n} \cong 94.234$ MHz, respectively. The transconductance is $g_m \cong 0.989$ mA/V (at $I_\mathrm{B} = 52$ μA) with the bandwidth $f_{g_m} \cong 31.153$ MHz. The total power dissipation of the CBTA is calculated as 10.1 mW.

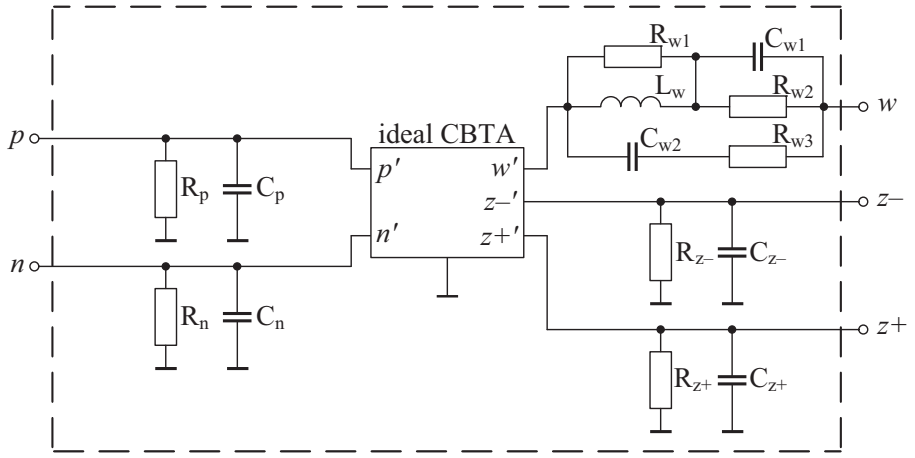


Fig. 3.29: Model of the CBTA including parasitic elements

The parasitic elements in Fig. 3.29 of the proposed CBTA in Fig. 3.28 have been computed as: $R_p = 97.76$ kΩ, $C_p = 1.842$ pF, $R_n = 97.96$ kΩ, $C_n = 1.244$ pF, $R_{w1} = 2.841$ kΩ, $R_{w2} = 37.173$ Ω, $R_{w3} = 309.978$ Ω, $C_{w1} = 0.9968$ pF, $C_{w2} = 1.6674$ pF, $L_w = 106.01$ nH, $R_{z-} = 1.4547$ MΩ, $C_{z-} = 1.651$ pF, $R_{z+} = 1.2546$ MΩ, $C_{z+} = 1.9535$ pF.

3.12 Current-feedback operational amplifier (CFOA)

The schematic symbol of the current-feedback operational amplifier (CFOA) is shown in Fig. 3.30.

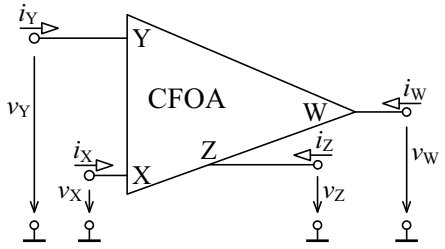


Fig. 3.30: Schematic symbol of CFOA

This device is equivalent to a CCII followed by a voltage follower [138], which can be described by following hybrid matrix:

$$\begin{bmatrix} i_{\mathrm{Y}} \\ v_{\mathrm{X}} \\ i_{\mathrm{Z}} \\ v_{\mathrm{W}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{\mathrm{Y}} \\ i_{\mathrm{X}} \\ v_{\mathrm{Z}} \\ i_{\mathrm{W}} \end{bmatrix}. \tag{3.19}$$

In simulations, the SPICE macro-model of the AD844AN CFOA by Analog Devices is used, which is characterized as follows: $R_{\rm X} = 50\ \Omega$, $R_{\rm Y} = 10\ {\rm M}\Omega$, $R_{\rm Z} = 3\ {\rm M}\Omega$, $R_{\rm W} = 15\ \Omega$, $C_{\rm X} = C_{\rm Y} = 2$ pF, and $C_{\rm Z} = 4.5$ pF. DC power supply voltages are equal to ± 12 V.

3.13 Modified current-feedback operational amplifier (MCFOA)

As already mentioned, the modified CFOA (MCFOA) [159], [174], [177] is the interconnection of the plus-type and minus-type CCIIs, which was proposed based on the CCC [133]. The schematic symbol of the MCFOA is shown in Fig. 3.31(a) and relations between the individual terminals can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{\rm Z} \\ i_{\rm Y} \\ v_{\rm X} \\ v_{\rm W} \end{bmatrix} = \begin{bmatrix} \alpha_1 & 0 & 0 & 0 \\ 0 & -\alpha_2 & 0 & 0 \\ 0 & 0 & \beta_1 & 0 \\ 0 & 0 & 0 & \beta_2 \end{bmatrix} \begin{bmatrix} i_{\rm X} \\ i_{\rm W} \\ v_{\rm Y} \\ v_{\rm Z} \end{bmatrix}, \tag{3.20}$$

where $\alpha_1 = 1 - \varepsilon_{i1}$, $\alpha_2 = 1 - \varepsilon_{i2}$ and ε_{i1}, ε_{i2} ($|\varepsilon_{i1}|$, $|\varepsilon_{i2}| \ll 1$) denote the current tracking errors, $\beta_1 = 1 - \varepsilon_{v1}$, $\beta_2 = 1 - \varepsilon_{v2}$ and ε_{v1}, ε_{v2} ($|\varepsilon_{v1}|$, $|\varepsilon_{v2}| \ll 1$) are the voltage tracking errors of MCFOA, respectively.

As it can be seen from (3.20) the MCFOA is different from the conventional CFOA presented above, because the W terminal current of the MCFOA is copied to the Y terminal in the opposite direction. However, it is well known that the Y-terminal current of the conventional CFOA is equal to zero.

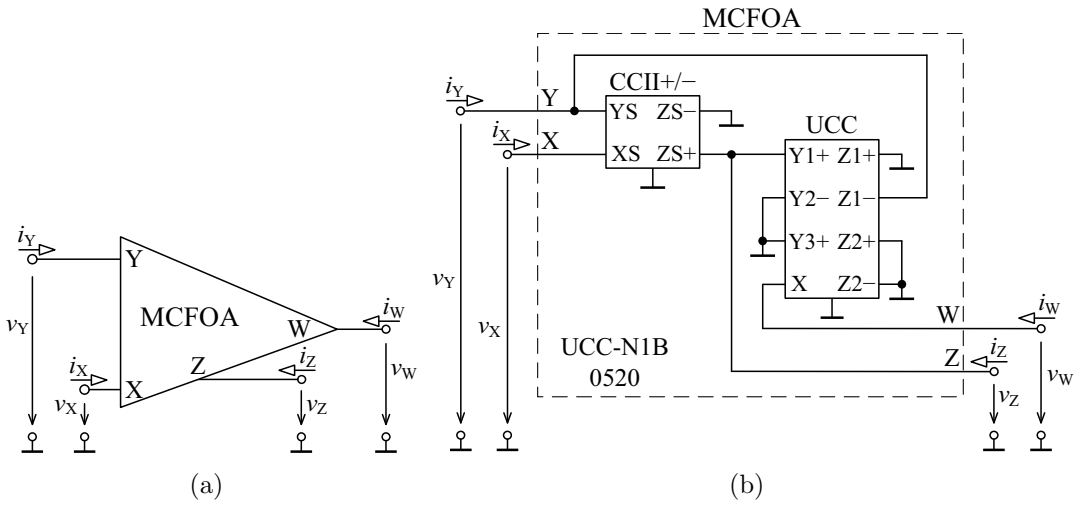


Fig. 3.31: (a) Schematic symbol and (b) block diagram of MCFOA

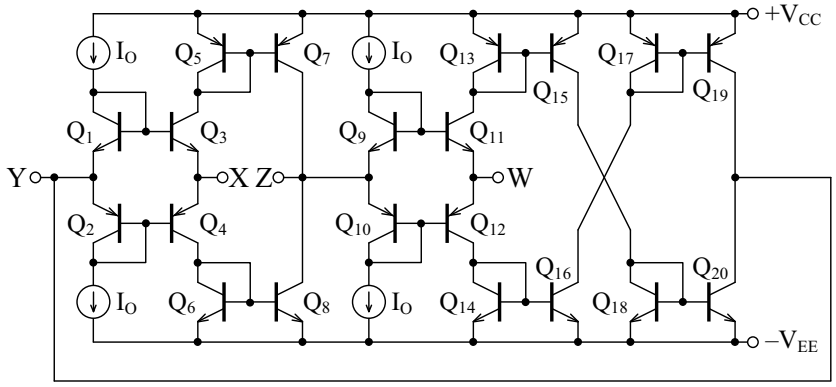


Fig. 3.32: Bipolar implementation of MCFOA [174]

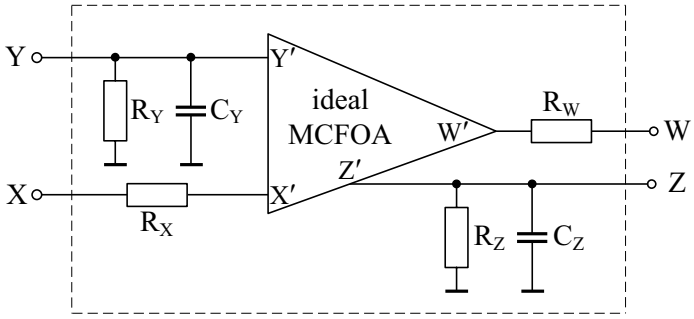


Fig. 3.33: Model of the MCFOA including parasitic elements

The UCC-N1B 0520 integrated circuit is that universal that we have used it for the realization of MCFOA. The realization of the MCFOA by UCC-N1B 0520 device is shown in Fig. 3.31(b) [177]. Other possible realization of the MCFOA based on commercially available AD844 amplifiers of Analog Devices is in [159].

The bipolar implementation of the MCFOA is shown in Fig. 3.32 [174]. The plus-type CCII is formed by transistors Q_1–Q_8 and transistors Q_9–Q_{20} form the minus-type CCII. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The DC supply voltages are $+V_{\rm CC} = -V_{\rm EE} = 2.5$ V. Bias current $I_{\rm O} = 200$ μA has been chosen.

The parasitic elements (Fig. 3.33) of the proposed MCFOA in Fig. 3.32 have been computed using SPICE simulation program as follows: $R_{\rm Y} = 93.82$ kΩ, $C_{\rm Y} = 2.123$ pF, $R_{\rm X} = R_{\rm W} = 36.96$ Ω, $R_{\rm Z} = 95.56$ kΩ, and $C_{\rm Z} = 2.128$ pF. The maximum values of terminal voltages and terminal currents without producing significant distortion are in the full scale of the supply voltage (in this case ±2.5 V) and ±15.53 mA, respectively. The DC current gains are $\alpha_1 \cong 0.990$ and $\alpha_2 \cong 1.010$ with bandwidths $f_{\alpha 1} \cong 135.49$ MHz and $f_{\alpha 2} \cong 90.85$ MHz, respectively. The DC voltage gains are $\beta_1 \cong \beta_2 \cong 0.999$ with bandwidths $f_{\beta 1} \cong f_{\beta 2} \cong 894.69$ MHz.

3.14 Voltage gain-controlled modified current-feedback operational amplifier (VGC-MCFOA)

The voltage gain-controlled MCFOA (VGC-MCFOA) (Fig. 3.34) is recently presented ABB at our Department, which is a derivative of the MCFOA presented in [158]. Relations between the individual terminals of the VGC-MCFOA can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{\mathrm{Y}} \\ i_{\mathrm{Z1}} \\ i_{\mathrm{Z2}} \\ i_{\mathrm{Z3}} \\ v_{\mathrm{X}} \\ v_{\mathrm{W}} \end{bmatrix} = \begin{bmatrix} -\alpha_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha_2 & 0 & 0 & 0 & 0 \\ 0 & -\alpha_3 & 0 & 0 & 0 & 0 \\ \alpha_4 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & h\beta_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \beta_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{W}} \\ i_{\mathrm{X}} \\ v_{\mathrm{Y}} \\ v_{\mathrm{Z1}} \\ v_{\mathrm{Z2}} \\ v_{\mathrm{Z3}} \end{bmatrix}, \tag{3.21}$$

where $\alpha_j = 1 - \varepsilon_{ij}$ and $\beta_k = 1 - \varepsilon_{vk}$ ($j = 1, 2, 3$ and $k = 1, 2$) are the non-ideal current and voltage gains, respectively, and ε_{ij} ($|\varepsilon_{ij}| \ll 1$) and ε_{vk} ($|\varepsilon_{vk}| \ll 1$) denote current and voltage tracking errors of the VGC-MCFOA, respectively. The presented novel ABB can be easily electronically tuned by means of the voltage gain h.

The basic idea for the implementation of the proposed VGC-MCFOA is shown in Fig. 3.35, where the OTA1 and OTA2 are used to control the voltage gain h and two CCII+/– represent the MCFOA. The bipolar implementation of the VGC-MCFOA is shown in Fig. 3.36. The voltage gain control stage is formed by two simple differential pair amplifiers (transistors Q_1–Q_6) and transistors Q_7–Q_{34} form the MCFOA, respectively. For this implementation the voltage gain h can be express as:

$$h = \frac{g_{m1}}{g_{m2}}, \tag{3.22}$$

where $g_{m1} = \frac{I_{\mathrm{B1}}}{2V_{\mathrm{T}}}$ and $g_{m2} = \frac{I_{\mathrm{B2}}}{2V_{\mathrm{T}}}$. Here the V_{T} is the thermal voltage (approximately 26 mV at 27°C) and the I_{B1} and I_{B2} are control currents adjusting the transcon-

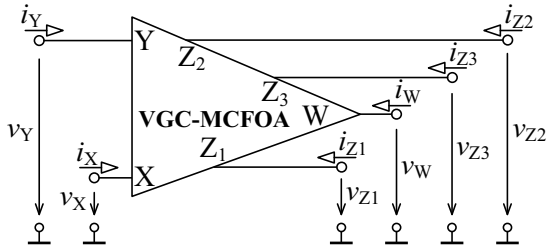


Fig. 3.34: Schematic symbol of VGC-MCFOA

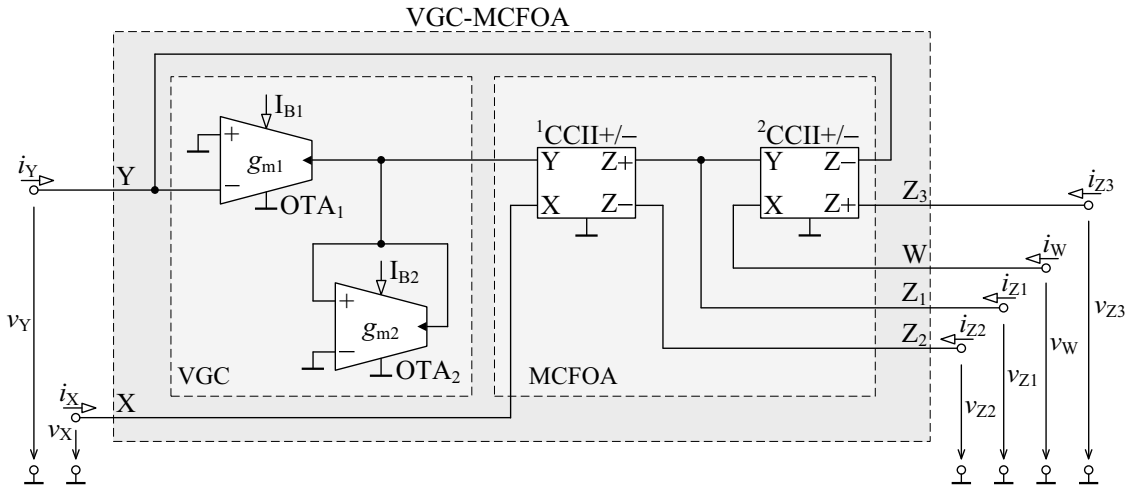


Fig. 3.35: Block diagram of VGC-MCFOA

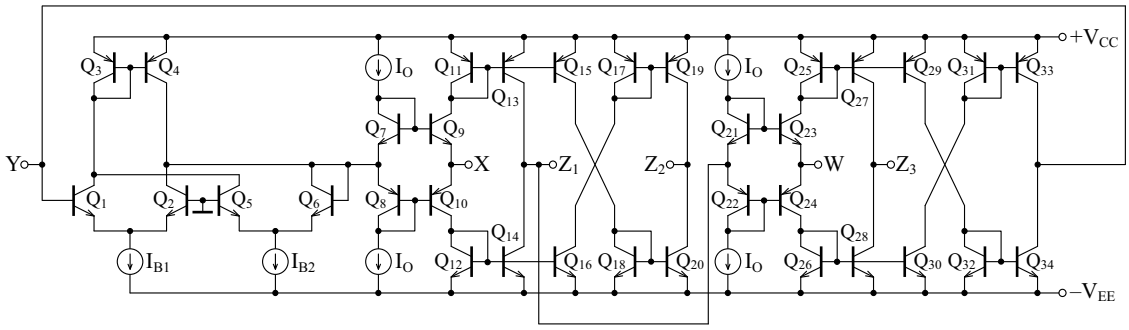


Fig. 3.36: Bipolar implementation of VGC-MCFOA

ductances g_{m1} and g_{m2}, respectively. Therefore, the voltage gain h in (3.22) can be given as:

$$h = \frac{I_{\mathrm{B1}}}{I_{\mathrm{B2}}}. \tag{3.23}$$

From (3.23) it is obvious that the proposed VGC-MCFOA can be easily adjusted electronically by either I_{B1} and/or I_{B2} currents.

For the complete analysis, the non-idealities of the proposed VGC-MCFOA in Fig. 3.36 have been further investigated in SPICE software. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The DC supply voltages are $+V_{\mathrm{CC}} = -V_{\mathrm{EE}} = 2.5$ V. Bias current $I_{\mathrm{O}} = 400$ μA has been chosen.

The parasitic elements of the proposed VGC-MCFOA in Fig. 3.37 have been computed as $R_{\mathrm{Y}} = 55.35$ kΩ, $C_{\mathrm{Y}} = 1.919$ pF, $R_{\mathrm{X}} = 42.01$ Ω, $R_{\mathrm{W}} = 36.96$ Ω, $R_{\mathrm{Z1}} = 94.31$ kΩ, $C_{\mathrm{Z1}} = 2.047$ pF, $R_{\mathrm{Z2}} = 97.61$ kΩ, $C_{\mathrm{Z2}} = 1.272$ pF, $R_{\mathrm{Z3}} = 97.19$ kΩ, and $C_{\mathrm{Z3}} = 1.154$ pF. The maximum values of terminal voltages and terminal cur-

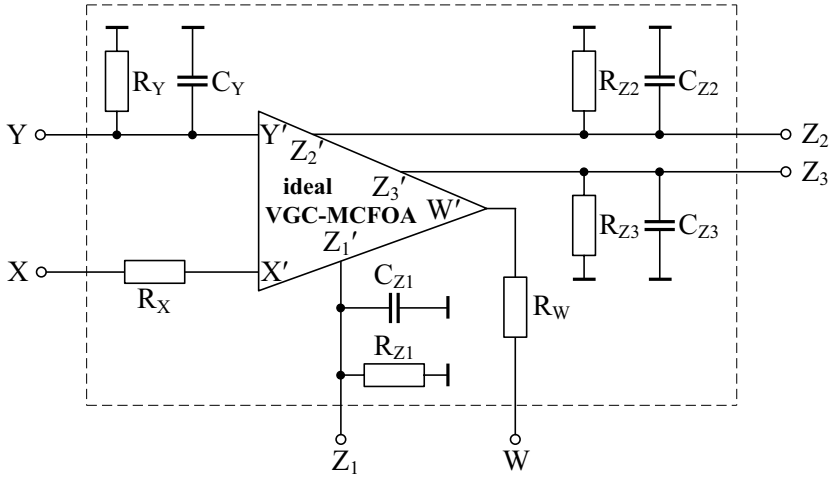
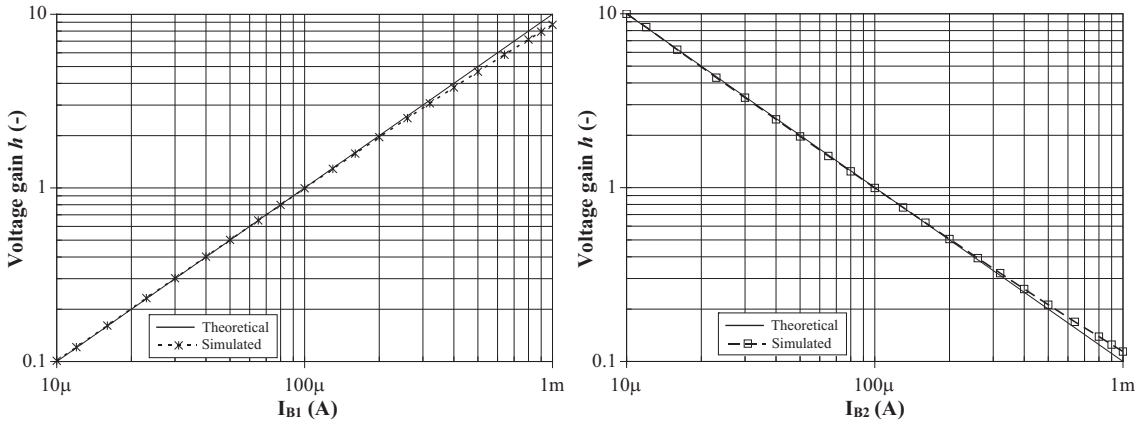


Fig. 3.37: Model of the VGC-MCFOA including parasitic elements



(a) (b)

Fig. 3.38: Voltage gain h responses for: (a) different values of I_{B1} at $I_{\mathrm{B2}} = 100$ μA and (b) different values of I_{B2} at $I_{\mathrm{B1}} = 100$ μA.

rents without producing significant distortion are computed as ± 106.7 mV and ± 16.23 mA, respectively. The DC current gains are $\alpha_1 \cong 1.001$, $\alpha_2 \cong 0.982$, $\alpha_3 \cong 1.001$, and $\alpha_4 \cong 0.982$ with bandwidths $f_{\alpha 1} \cong 49.16$ MHz, $f_{\alpha 2} \cong 89.22$ MHz, $f_{\alpha 3} \cong 67.34$ MHz, and $f_{\alpha 4} \cong 90.91$ MHz, respectively. The DC voltage gains are $\beta_1 \cong 0.995$ and $\beta_2 \cong 0.999$ with bandwidths $f_{\beta 1} \cong 108.15$ MHz and $f_{\beta 2} \cong 879.47$ MHz, respectively.

Ideal and simulated voltage gain h between Y and X terminals are demonstrated in Fig. 3.38. In both simulations external bias currents I_{B1} or I_{B2} have been adjusted in the interval from 10 μA to 1 mA (equal to gain $h = 0.1$ to 10). From Fig. 3.38 it can be clearly seen that due to that above mentioned non-idealities of the VGC-MCFOA, the obtained voltage gains are in interval $0.1 \div 8.7$ and $10 \div 0.114$, respectively.

3.15 Minus-type current-controlled third-generation voltage conveyor (CC-VCIII–)

The minus-type current-controlled third-generation voltage conveyor (CC-VCIII–) is a novel three-port building block with electronic tuning, which schematic symbol and behavioral model are shown in Fig. 3.39 [172]. The current through the X terminal follows the current of the Y terminal. The voltage of the Y terminal follows the voltage of the X terminal. Finally, the voltage of the ZN terminal follows the inverted voltage of the X terminal. The intrinsic resistance of Y terminal can be easily controlled by means of external control current I_{O}, which makes the introduced ABB attractive for resistorless and electronically controllable linear circuit applications. Relations between the individual terminals of the non-ideal CC-VCIII– can be described by the following hybrid matrix:

$$\begin{bmatrix} i_{\mathrm{X}} \\ v_{\mathrm{Y}} \\ v_{\mathrm{ZN}} \end{bmatrix} = \begin{bmatrix} 0 & \alpha & 0 \\ \delta & R_{\mathrm{Y}} & 0 \\ -\gamma & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{\mathrm{X}} \\ i_{\mathrm{Y}} \\ i_{\mathrm{ZN}} \end{bmatrix}, \tag{3.24}$$

where $\alpha = 1-\varepsilon_i$, $\delta = 1-\varepsilon_{v1}$, and $\gamma = 1-\varepsilon_{v2}$. Here, the R_y is the intrinsic resistance of the y terminal, ε_i ($|\varepsilon_i| \ll 1$) and ε_{v1}, ε_{v2} ($|\varepsilon_{v1}|$,$|\varepsilon_{v2}| \ll 1$) denote current and voltage tracking errors of CC-VCIII–, respectively.

Proposed CMOS implementation of the CC-VCIII– is shown in Fig. 3.40 [172]. The internal structure is based on the CCCII [6], which is followed by an inverting voltage follower (IVF). Here, transistors M1–M13 realize mixed-mode translinear cells. Voltage conveyors implemented by using mixed-mode translinear cells have considerably greater frequency bandwidths and employ fewer active and passive elements. The IVF is realized by transistors M14–M22, where M14 and M15 form an inverting amplifier [160] and M16–M22 form a conventional voltage buffer [102]. In case the inverting amplifier is removed and the gate of the M19 is connected to

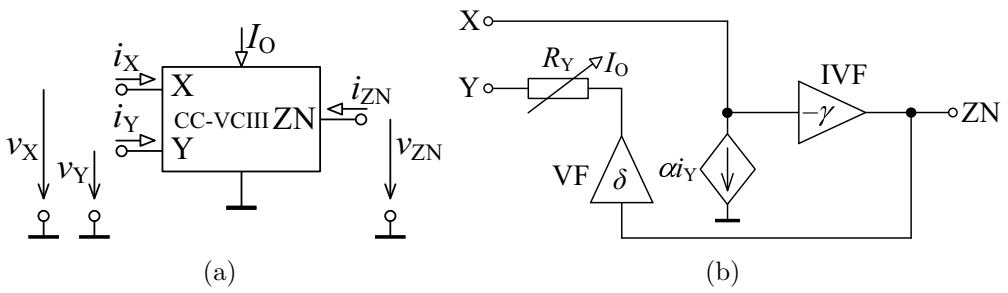


Fig. 3.39: (a) Schematic symbol and (b) behavioral model of CC-VCIII–

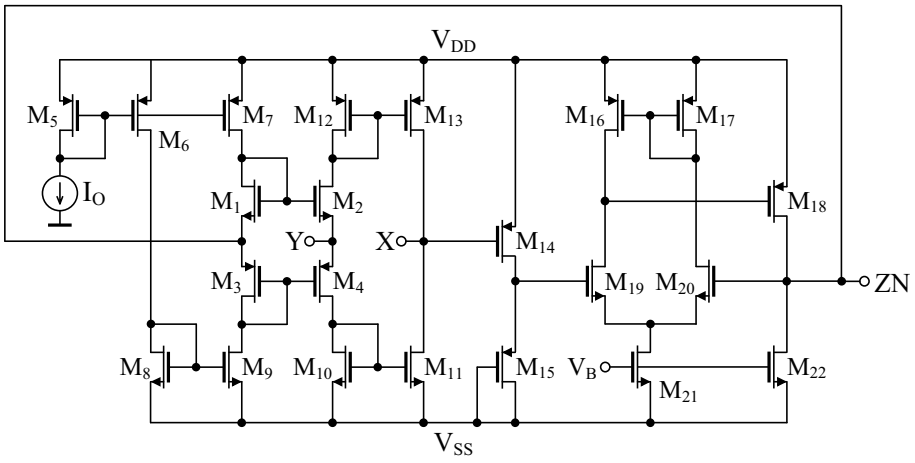


Fig. 3.40: CMOS implementation of CC-VCIII– [172]

Tab. 3.4: Transistor dimensions of the CC-VCIII–

PMOS transistors	W(μm)/L(μm)
M3, M4	60/0.35
M5, M6, M7	30/2.0
M12, M13	30/1.0
M14, M15	50/4.0
M16, M17	4/0.5
M18	10/0.5
NMOS transistors	W(μm)/L(μm)
M1, M2	20/0.35
M8, M9	10/2.0
M10, M11	10/1.0
M19, M20	0.8/0.5
M21, M22	10/0.5

the x terminal, the positive-type current-controlled first-generation voltage conveyor (CC-VCI+) can be easily obtained.

The intrinsic resistance R_{Y}, which is in series to the Y terminal of the CC-VCIII– , depends on operation region of the MOS transistors M2 and M4. If small control current I_{O} is applied, MOS transistors work in weak inversion (subthreshold region) and the model equations of the MOS transistors will be exponential. The drain current can be given as follows:

$$I_{\mathrm{D}} = \frac{W}{L} I_{\mathrm{D0}} e^{\frac{qV_{\mathrm{GS}}}{nkT}} \left(1 - e^{-\frac{qV_{\mathrm{DS}}}{kT}}\right), \tag{3.25}$$

where n is typically $1.2 \div 1.5$ and I_{D0} is the drain current at $V_{\mathrm{DS}} = 0$ for $W/L = 1$. Neglecting the exponential term with V_{DS} in (3.25), the intrinsic resistance R_{Y} can be calculated as follows:

$$R_{\mathrm{Y}} = \frac{V_T}{2I_{\mathrm{O}}}, \tag{3.26}$$

where $V_{\mathrm{T}} \approx \mathrm{kT}/q \approx 26$ mV at 27°C is the thermal voltage. For sufficiently high current values of I_{O} (i.e. in strong inversion), if the MOS transistors work in saturation region, intrinsic resistor R_{Y} serial to the Y terminal can be calculated as follows:

$$R_{\mathrm{Y}} = \frac{1}{g_{m2} + g_{m4}}, \tag{3.27}$$

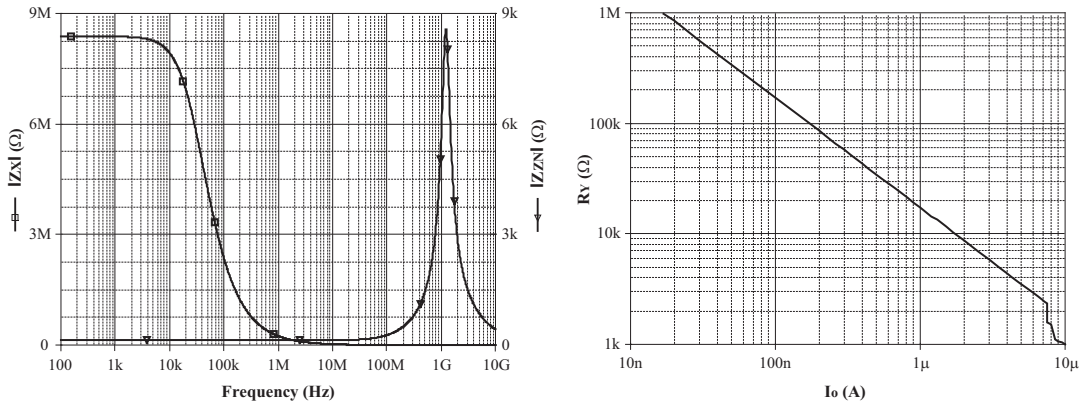
where g_{m2} and g_{m4} are transconductances of M2 and M4, respectively, and they are calculated as:

$$g_{mi} = \sqrt{2\mu_{0i} C_{OX} (W/L)_i I_{\mathrm{O}}}, \tag{3.28}$$

for $i = 2, 4$. Here, $(\mu_{0i} C_{OX})$ is the constant of the MOS technology, where C_{OX} is the gate oxide capacitance per unit area, μ_{0i} is the free electron mobility in the channel, and W and L are the channel width and length, respectively.

For the complete analysis, the real behavior of the proposed CC-VCIII– in Fig. 3.40 has been further investigated in SPICE software. In the design transistors are modeled by the TSMC 0.35 μm CMOS process parameters given in Tab. A.2. Dimensions of transistors are listed in Tab. 3.4. The DC power supply voltages are equal to ± 2.5 V and $V_{\mathrm{B}} = -1.7$ V.

The maximum values of terminal voltages and terminal currents without pro-



(a) (b)

Fig. 3.41: (a) Frequency responses of the input impedance at the termial X and output impedance at the terminal ZN, (b) intrinsic resistance at the input terminal Y versus I_{O}

ducing significant distortion are computed as ±0.71 V and ±5.81 mA, respectively. The DC current gain is $\alpha \cong 1.023$ with bandwidth $f_\alpha \cong 136.31$ MHz at $I_O = 5$ μA. The DC voltage gains are $\delta \cong 0.982$ and $\gamma \cong 0.985$ with bandwidths $f_\delta \cong 1.536$ GHz and $f_\gamma \cong 1.365$ GHz at $I_O = 5$ μA, respectively.

Frequency responses of the input impedances at the terminal X and output impedance at the termial ZN are shown in Fig. 3.41(a). As expected, the input impedance of the terminal X is high, i.e. 8.38 MΩ at 100 Hz, 245.6 kΩ at 1 MHz. The impedance of the output voltage terminal ZN should be theoretically 0 (zero). In practice, the values of output impedance of the terminal ZN are 130.7 Ω at 1 MHz, 268.9 Ω at 100 MHz. Fig. 3.41(b) shows the simulated intrinsic resistance R_Y at input terminal y relative to I_O. The control current is sweeped in interval 17 nA÷7.3 μA and the obtained intrinsic resistance values are 987 kΩ and 2.4 kΩ, respectively.

3.16 Sub-conclusion

In this Chapter different active elements are presented, where most of them have been introduced and developed at our Department. These ABBs are further used in this thesis for various filter and oscillator designs.

In the Section 3.3, the DBTA is defined as novel versatile ABB and it belongs to the group of "universal" active elements [169], [170], [178], [180], [194]. It is a six-port active element with low-impedance current/high-impedance voltage inputs and high-impedance current/low-impedance voltage outputs. For computer simulations and experimental measurements BJT implementation and two different models using commercially available amplifiers were proposed.

Section 3.5 presents the PCA, which was defined in 2005. The contribution of this section is the new BJT implementation of the PCA [189].

The current follower transconductance amplifier, presented in Section 3.6, was introduced in September 2008 as a novel low-input and high-output impedance terminal ABB for CM signal processing [167], [181].

The CCCFTA [171] and the ZC-CCCITA [185], presented in Sections 3.8 and 3.9, are derivatives of the conventional CFTA. In both ABBs the intrinsic resistance of the f terminal can be easily controlled by means of external control current.

In the Section 3.10, the GCFDITA is presented as derivative of the circuit presented in [17].

The main contribution of the Section 3.11 is the novel internal structure of the CBTA using bipolar transistors [188]. Similarly, the Section 3.13 presents novel implementations for the MCFOA [174], [177].

Section 3.14 presents novel ABB with tunability property. Here the voltage gain can be easily controlled by means of external current. The proposed VGC-MCFOA can be also realized using commercially available OTAs and CCIIs.

Finally, Section 3.15 is focused on novel type of voltage conveyor design [172]. The intrinsic resistance of Y terminal can be easily controlled by means of external control current, which makes the introduced ABB attractive for resistorless and electronically controllable linear circuit applications. CMOS internal structure is proposed to verify the behavior of the presented application.

4 FIRST-ORDER ALL-PASS FILTER DESIGN

First-order all-pass (AP) filters are widely used in analogue signal processing in order to shift the phase of an electrical signal while keeping its amplitude constant. First proposed AP filters employing op-amps suffer from the well-known limitations of opamp-based circuits such as frequency limitations, the use of a large number of passive elements and lack of electronic tuning [115]. Therefore, to eliminate these disadvantages, other types of active elements have started to be used for AP filter design. They also play a great role in the design of other types of active circuits such as quadrature or multiphase oscillators and high-Q band-pass filters [24], [49], [147].

In this Chapter various current-, voltage-, and mixed-mode first-order all-pass filter structures are presented. All circuits are novel and their advantages are compared with the literature presented solutions.

4.1 CM signal processing applications using single GCFDITA and grounded passive elements

Recently, a general topology of realizing various VM analogue functions using differential voltage current conveyor (DVCC) has been proposed in [95], however, low-pass (LP) and high-pass (HP) filtering functions are not provided. Here proposed general topologies shown in Fig. 4.1 are created using a single GCFDITA, two grounded passive components and both can realize several CM analogue functions, which include amplifier, integrator, and first-order LP, HP and AP filters. If $a = -1$ is considered, i.e. use of CIDITA, both the topologies are ideally same. Considering the ABB to be a CIDITA and doing routine circuit analysis using (3.16), the output current can

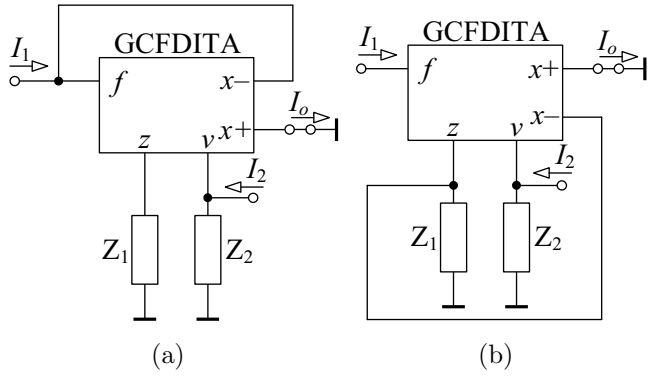


Fig. 4.1: Proposed circuit topologies for realizing CM analogue functions

be given by the following expression:

$$I_o = \frac{g_m(I_1 Z_1 - I_2 Z_2)}{g_m Z_1 + 1} = \frac{I_\mathrm{B}(I_1 Z_1 - I_2 Z_2)}{I_\mathrm{B} Z_1 + 2V_\mathrm{T}}. \tag{4.1}$$

By appropriate choose of different impedances (Z_1 and Z_2 - as combinations of resistor and capacitor) and current inputs (I_1 and I_2), various CM analogue functions can be derived.

CM amplifier:

With $I_2 = I_{in}$, $Z_2 = R$ and $Z_1 = 0$, the transfer function becomes:

$$\frac{I_o}{I_{in}} = -g_m R = -\frac{I_\mathrm{B} R}{2V_\mathrm{T}}, \tag{4.2}$$

which represents an inverting amplifier with electronically tunable gain.

CM integrator:

With $I_2 = I_{in}$, $Z_2 = \frac{1}{sC}$ and $Z_1 = 0$, the transfer function becomes:

$$\frac{I_o}{I_{in}} = -\frac{g_m}{sC} = -\frac{I_\mathrm{B}}{2V_\mathrm{T} sC}, \tag{4.3}$$

which represents an inverting integrator with electronically tunable time constant.

CM first-order low-pass filter (LPF):

With $I_1 = I_{in}$, $I_2 = 0$ and $Z_1 = \frac{1}{sC}$, the transfer function becomes:

$$\frac{I_o}{I_{in}} = \frac{g_m}{sC + g_m} = \frac{I_\mathrm{B}}{2V_\mathrm{T} sC + I_\mathrm{B}}, \tag{4.4}$$

which represents a non-inverting LPF. The pole frequency ω_0, expressed as $\omega_0 = \frac{I_\mathrm{B}}{2V_\mathrm{T} C}$ is electronically tunable by means of the transconductance and hence by the bias current.

CM first-order high-pass filter (HPF):

With $I_2 = I_{in}$, $I_1 = 0$, $Z_1 = \frac{1}{sC}$ and $Z_2 = R$, the transfer function becomes:

$$\frac{I_o}{I_{in}} = -\frac{g_m(sCR)}{sC + g_m} = -\frac{I_\mathrm{B}(sCR)}{2V_\mathrm{T} sC + I_\mathrm{B}}, \tag{4.5}$$

which represents a CM HPF.

CM first-order all-pass filter (APF):

With $I_1 = I_2 = I_{in}$, $Z_1 = \frac{1}{sC}$ and $Z_2 = R$, the transfer function becomes:

$$T(s) = \frac{I_o}{I_{in}} = -\frac{g_m(sCR-1)}{sC+g_m} = -\frac{I_{\mathrm{B}}(sCR-1)}{2V_{\mathrm{T}}sC+I_{\mathrm{B}}}. \tag{4.6}$$

The above transfer function represents an APF under the following condition:

$$g_m R = 1. \tag{4.7}$$

If (4.7) is fulfilled, the phase response of the filter is given as:

$$\varphi(\omega) = -2\mathrm{arctg}(\omega CR) = -2\mathrm{arctg}\left(\frac{\omega C}{g_m}\right) = -2\mathrm{arctg}\left(\frac{2V_{\mathrm{T}}\omega C}{I_{\mathrm{B}}}\right). \tag{4.8}$$

It is worth noting that the APF circuit uses all grounded passive elements, a feature which is absent in previously reported CDTA based APF in [78]. However, unlike the proposed circuit here, the circuit in [78] is free from any matching conditions and constraints. On the other hand, the matching condition in (4.7) should not be considered as a drawback, since for a given value of R the condition could be met by changing the bias current of the transconductance. Moreover, the advantage of realizing several other CM analogue functions from the same topology overshadows the problem of matching constraints.

For the circuit in Fig. 4.1(a) the aforementioned tracking errors and parasitics affect both the gains and the frequency potential of the circuit. Considering the operating natural frequency:

$$\omega < min\left(\frac{1}{R_{x-}C_{x-}}, \frac{1}{R_zC_z}, \frac{1}{R_vC_z}\right), \tag{4.9}$$

then the affects of parasitic capacitances are alleviated. If the impedances Z_1 and Z_2 are chosen such that:

$$|Z_1|, |Z_2| < min(R_z, R_v), \tag{4.10}$$

then the affects of the parasitic resistances at terminals z and v are alleviated. Also, since the value of R_f is very small as compared to R_z, then:

$$R_z||R_f \approx R_f. \tag{4.11}$$

Now considering the effects of the tracking errors as in (3.17), then the transfer

function in (4.1) is modified to:

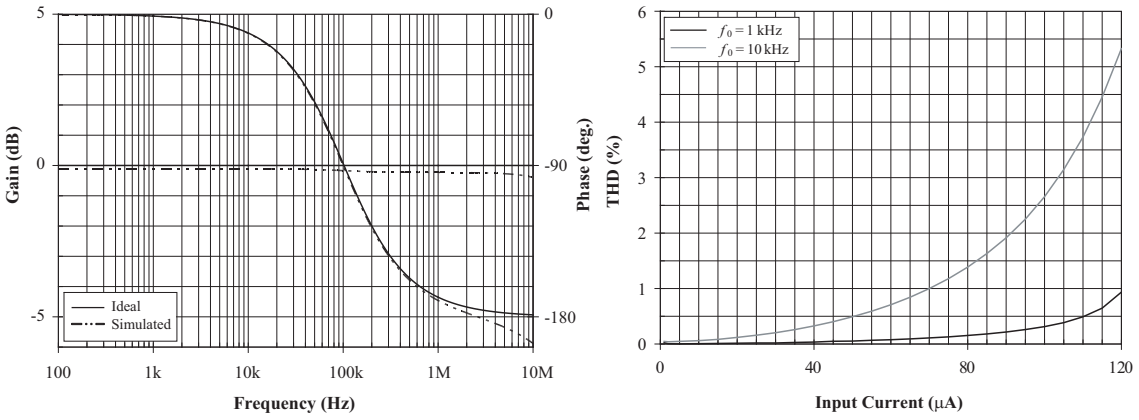
$$I_o = \frac{g_m \beta_1 (\alpha I_1 Z_1 - I_2 Z_2)}{\alpha \beta_2 g_m Z_1 + 1} = \frac{\beta_1 I_{\mathrm{B}} (\alpha I_1 Z_1 - I_2 Z_2)}{\alpha \beta_2 I_{\mathrm{B}} Z_1 + 2V_{\mathrm{T}}}. \tag{4.12}$$

It is evident that the gain of any analogue function derived from (4.12) would be affected by β_1 and/or $\alpha\beta_1$. Also, the natural pole frequency of any first-order filter would change to:

$$\omega_0 = \frac{\alpha \beta_2 g_m}{C} = \frac{\alpha \beta_2 I_{\mathrm{B}}}{2V_{\mathrm{T}} C}. \tag{4.13}$$

Thus, a good design of the ABB with values of α, β_1 and β_2 close to unity should be considered.

Using the bipolar implementation of CIDITA (Fig. 3.26), the workability of the proposed topology in Fig. 4.1(a) has been verified. The CM all-pass filter has been taken as example to demonstrate the workability for characteristic frequency $f_0 \approx 100$ kHz. The component values taken are $C = 3.9$ nF, $R = 400\ \Omega$, and $g_m = 2.5$ mA/V ($I_{\mathrm{B}} = 130\ \mu$A). The ideal and simulated gain and phase response for the proposed all-pass filter are shown in Fig. 4.2(a). From the results it can be seen that both the gain and phase characteristics of the filter are in good agreement with theory. Fig. 4.2(b) shows the total harmonic distortion (THD) variation with respect to amplitude of the applied sinusoidal input current at 1 and 10 kHz (filter parameter: $f_0 \approx 100$ kHz), respectively. An input with the amplitude of 100 μA at 1 and 10 kHz yields THD values of 0.31 and 2.66%, respectively.



(a) (b)

Fig. 4.2: (a) Ideal and simulated gain and phase responses and (b) THD of the proposed all-pass filter with respect to applied sinusoidal input current

4.2 CM electronically tunable all-pass filter using current-controlled CFTAs

Several CM first-order AP filter realizations using different active building blocks have been reported in the literature [59], [98], [99], [135], [151]. These topologies realize either inverting or non-inverting type of filters. For realizing the complementary type, they need to change the circuit topology. Furthermore, most of the reported realizations do not include electronical tunability property. Recently reported CCCFTA includes electronical tunability property by means of external bias current. Hence, this active element for such AP filter design is ideal.

The proposed circuit realizing both inverting and non-inverting type of AP filters is shown in Fig. 4.3 [171]. The circuit is composed of two CCCFTAs, two resistors, and one capacitor. Taking into account non-ideal CCCFTAs, routine analysis yields current transfer functions that can be expressed in following forms:

$$T_1(s) = \frac{I_{\mathrm{AP-}}}{I_{in}} = \frac{\alpha_2 sCR_{f1}R_2 g_{m2} - \alpha_1 R_1 g_{m1}}{sCR_{f1}+1} = \frac{\alpha_2 V_{\mathrm{T}}^2 I_{\mathrm{B2}} sCR_2 - \alpha_1 I_{\mathrm{O1}} I_{\mathrm{B1}} R_1}{V_{\mathrm{T}}^2 sC + 2V_{\mathrm{T}} I_{\mathrm{O1}}}, \tag{4.14}$$

$$T_2(s) = \frac{I_{\mathrm{AP+}}}{I_{in}} = -\frac{\alpha_2 sCR_{f1}R_2 g_{m2} - \alpha_1 R_1 g_{m1}}{sCR_{f1}+1} = -\frac{\alpha_2 V_{\mathrm{T}}^2 I_{\mathrm{B2}} sCR_2 - \alpha_1 I_{\mathrm{O1}} I_{\mathrm{B1}} R_1}{V_{\mathrm{T}}^2 sC + 2V_{\mathrm{T}} I_{\mathrm{O1}}}. \tag{4.15}$$

As it is seen from these equations, both inverting (4.14) and non-inverting (4.15)

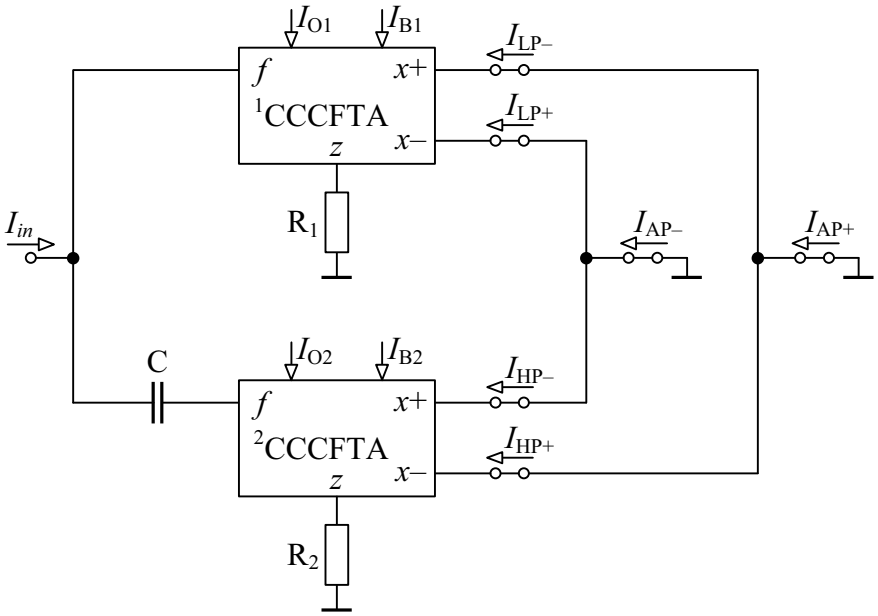


Fig. 4.3: The proposed electronically tunable CM all-pass filter employing CCCFTAs

types of current-mode first-order all-pass filters can be realized with the same circuit topology.

The phase responses of the filter are given as follows:

$$\varphi_1(\omega) = 180^\circ - \text{arctg}\left(\frac{\omega V_\text{T} C}{2I_\text{O1}}\right) - \text{arctg}\left(\frac{\omega\alpha_2 V_\text{T}^2 I_\text{B2} C R_2}{\alpha_1 I_\text{O1} I_\text{B1} R_1}\right), \tag{4.16}$$

$$\varphi_2(\omega) = -\text{arctg}\left(\frac{\omega V_\text{T} C}{2I_\text{O1}}\right) - \text{arctg}\left(\frac{\omega\alpha_2 V_\text{T}^2 I_\text{B2} C R_2}{\alpha_1 I_\text{O1} I_\text{B1} R_1}\right). \tag{4.17}$$

The natural frequency ω_0 can be found as:

$$\omega_0 = \frac{2I_\text{O1}}{V_\text{T} C}. \tag{4.18}$$

As it is seen from above equation, the proposed configuration can provide phase shifting both between 180° to 0° and 0° to –180°. The shifted phase value can be controlled by means of external bias current I_O1.

The active and passive sensitivities of ω_0 are given as:

$$S_{I_\text{O1}}^{\omega_0} = -S_C^{\omega_0} = 1, \quad S_{I_\text{O2},I_\text{B1},I_\text{B2},\alpha_1,\alpha_2,R_1,R_2}^{\omega_0} = 0. \tag{4.19}$$

From Eq. (4.19) it is evident that the sensitivities of active and passive components for natural frequency ω_0 are unity in relative amplitude.

Using the bipolar implementation of CCCFTA (Fig. 3.21), the behavior of the proposed CM all-pass filter has been verified by SPICE simulations. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The passive element values were selected as $C = 10$ nF and $R_1 = R_2 = 1$ kΩ. The parasitic resistances R_{f1} and R_{f2} at the input terminals f and transconductances g_{m1} and g_{m2} of CCCFTAs have been set by the bias and control currents as follows: $I_\text{O1} = 8$ μA ($R_{f1} = 1.63$ kΩ), $I_\text{O2} = 400$ μA ($R_{f1} = 37.2$ Ω), and $I_\text{B1} = I_\text{B2} = 52$ μA ($g_{m1} = g_{m2} = 1$ mA/V). In this case a 90° phase shift is at $f_0 \cong 10$ kHz. The gain and phase characteristics of the simulated inverting and non-inverting type of CM first-order all-pass filter are shown in Fig. 4.4(a). Electronical tunability property of the proposed filter for different controll current values I_O1 and corresponding phase responses are shown in Fig. 4.4(b). Similarly, the possibility of tuning the group delay of the proposed filter by the controll current I_O1 is shown in Fig. 4.4(c). For required values $f_0 \approx \{3; 10; 30; 100\}$ kHz the I_O1 must be $I_\text{O1} = \{2.5;\ 8;\ 25;\ 83\}$ μA ($R_{f1} = \{5.23$ k; 1.63 k; 527; 162$\}$ Ω). The possibility of tuning the natural frequency f_0 by the current I_O1 is shown in Fig. 4.4(d). The THD variation with respect to amplitude of the applied sinusoidal input current at 1 kHz (filter parameter:

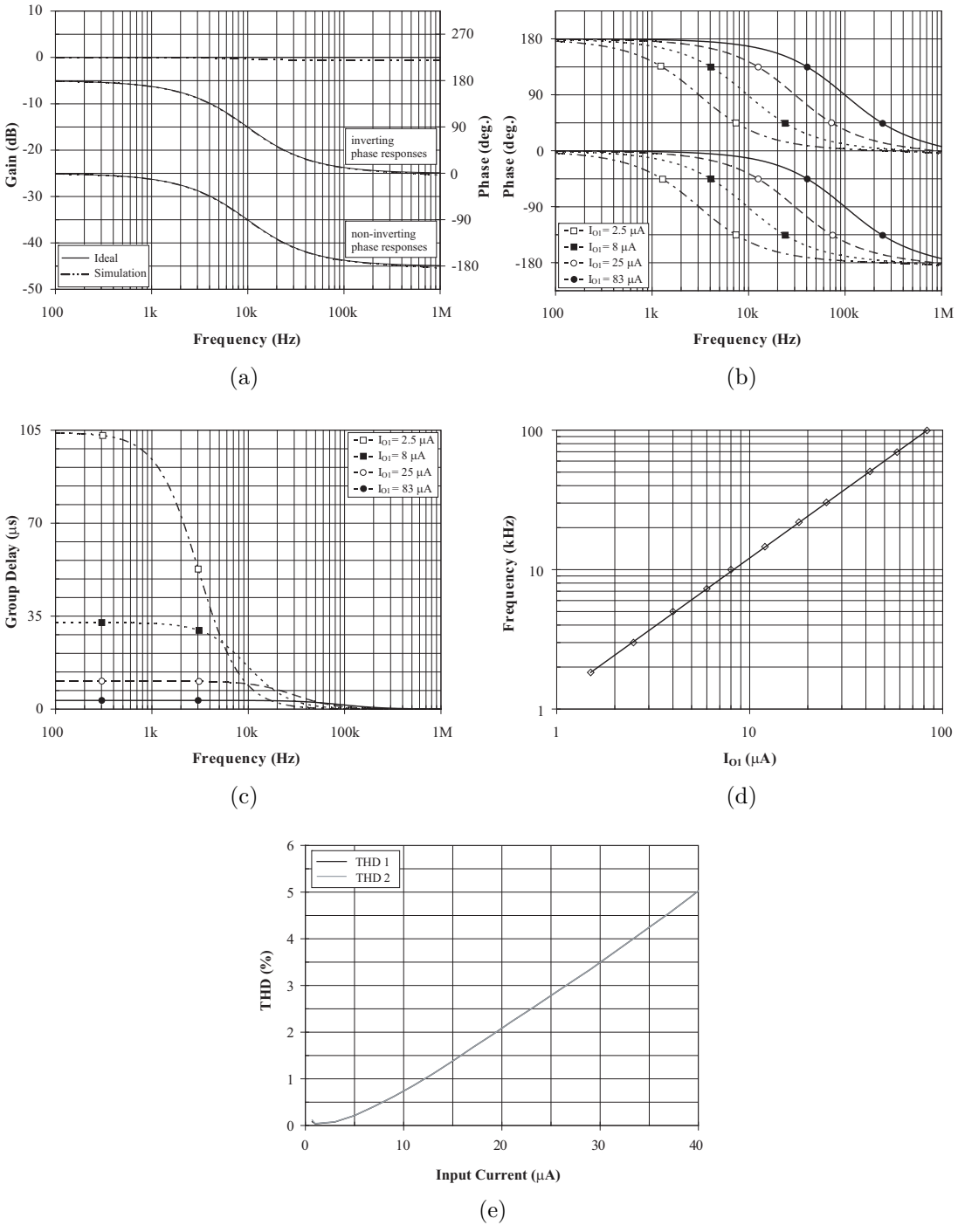


Fig. 4.4: (a) Simulated magnitude and phase characteristics of the proposed inverting and non-inverting type of CM first-order all-pass filter, (b) electronical tunability of phase responses, (c) possibility of tuning the group delay, and (d) possibility of tuning the natural frequency f_0 by means of the bias current I_{O1}, (e) THD variation of the proposed all-pass filter for both responses against applied input current

$f_0 \approx 10$ kHz) is shown in Fig. 4.4(e). An input with the amplitude of 30 μA at 1 kHz yields for both responses THD values of 3.49%. From the simulation results it can be seen that the gain and phase characteristics of the proposed inverting and non-inverting type all-pass filter are in good agreement with theory.

4.3 CM electronically tunable all-pass filter using the novel VGC-MCFOA

Even if the proposed circuit in previous Section realizes both the inverting and non-inverting types of AP filters, because of one of the bias currents to be very large as compared to the other, it is impractical. Moreover, the use of floating capacitor also makes the circuit less attractive for integration. The proposed circuit in this Section (Fig. 4.5) employing single novel VGC-MCFOA and only grounded passive elements, does not suffer these weaknesses and, furthermore, it also realizes both inverting and non-inverting type of AP filter responses simultaneously. The natural frequency of the filter can be easily tuned by means of the voltage gain h.

Considering the ideal VGC-MCFOA (i.e. α_j and β_k are unity) and assuming $R_2 = R_3 = R$ and $I_{i1} = I_{i2} = I_{in}$, routine analysis gives the following transfer functions (TFs):

$$T_1(s) = \frac{I_{o1}}{I_{in}} = \frac{sCR_1 - h}{sCR_1 + h} = \frac{I_{\mathrm{B2}}sCR_1 - I_{\mathrm{B1}}}{I_{\mathrm{B2}}sCR_1 + I_{\mathrm{B1}}}, \tag{4.20}$$

$$T_2(s) = \frac{I_{o2}}{I_{in}} = -\frac{sCR_1 - h}{sCR_1 + h} = -\frac{I_{\mathrm{B2}}sCR_1 - I_{\mathrm{B1}}}{I_{\mathrm{B2}}sCR_1 + I_{\mathrm{B1}}}. \tag{4.21}$$

As it is seen from these equations, both inverting (4.20) and non-inverting (4.21) output of CM first-order all-pass filter can be realized simultaneously with the same circuit topology.

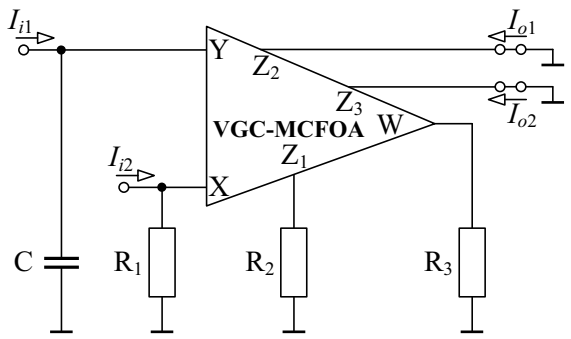


Fig. 4.5: Proposed electronically tunable all-pass filter using VGC-MCFOA

The phase responses of the TFs are calculated as:

$$\varphi_1(\omega) = 180^\circ - 2\text{arctg}\left(\frac{\omega CR_1}{h}\right) = 180^\circ - 2\text{arctg}\left(\frac{\omega I_{\text{B2}} CR_1}{I_{\text{B1}}}\right), \tag{4.22}$$

$$\varphi_2(\omega) = -2\text{arctg}\left(\frac{\omega CR_1}{h}\right) = -2\text{arctg}\left(\frac{\omega I_{\text{B2}} CR_1}{I_{\text{B1}}}\right). \tag{4.23}$$

Therefore, the phases of the AP filter alter from 180° to 0° and 0° to –180°, respectively. Consequently, the natural frequency ω_0 can be found as:

$$\omega_0 = \frac{h}{CR_1} = \frac{I_{\text{B1}}}{I_{\text{B2}} CR_1}. \tag{4.24}$$

From Eq. (4.22) and (4.23) it is clearly seen that the angular frequency value can be easily tuned by means of the bias currents I_{B1} or I_{B2}.

Taking into account non-idealities of the VGC-MCFOA, TFs (4.20) and (4.21) of the filter in Fig. 4.5 convert to:

$$T_1(s) = \frac{I_{o1}}{I_{in}} = \frac{\alpha_3 R_3(sCR_1 - \beta_1 h)}{sCR_1R_3 + \alpha_1\alpha_2\beta_1\beta_2 hR_2} = \frac{\alpha_3 R_3(I_{\text{B2}} sCR_1 - I_{\text{B1}}\beta_1)}{I_{\text{B2}} sCR_1R_3 + I_{\text{B1}}\alpha_1\alpha_2\beta_1\beta_2 R_2}, \tag{4.25}$$

$$T_2(s) = \frac{I_{o2}}{I_{in}} = -\frac{\alpha_2\alpha_4\beta_2 R_2(sCR_1 - \beta_1 h)}{sCR_1R_3 + \alpha_1\alpha_2\beta_1\beta_2 hR_2} = -\frac{\alpha_2\alpha_4\beta_2 R_2(I_{\text{B2}} sCR_1 - I_{\text{B1}}\beta_1)}{I_{\text{B2}} sCR_1R_3 + I_{\text{B1}}\alpha_1\alpha_2\beta_1\beta_2 R_2}, \tag{4.26}$$

and non-ideal phase responses from TFs (4.25) and (4.26) are given as:

$$\varphi_1(\omega) = 180^\circ - \text{arctg}\left(\frac{\omega I_{\text{B2}} CR_1R_3}{I_{\text{B1}}\alpha_1\alpha_2\beta_1\beta_2 R_2}\right) - \text{arctg}\left(\frac{\omega I_{\text{B2}} CR_1}{I_{\text{B1}}\beta_1}\right), \tag{4.27}$$

$$\varphi_2(\omega) = -\text{arctg}\left(\frac{\omega I_{\text{B2}} CR_1R_3}{I_{\text{B1}}\alpha_1\alpha_2\beta_1\beta_2 R_2}\right) - \text{arctg}\left(\frac{\omega I_{\text{B2}} CR_1}{I_{\text{B1}}\beta_1}\right). \tag{4.28}$$

The natural frequency ω_0 changes to:

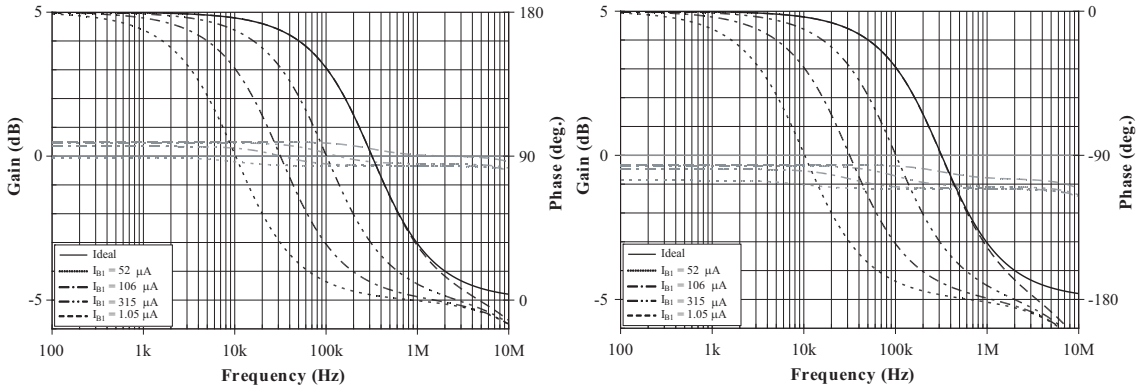
$$\omega_0 = \frac{I_{\text{B1}}\alpha_1\alpha_2\beta_1\beta_2 R_2}{I_{\text{B2}} CR_1R_3}. \tag{4.29}$$

From Eq. (4.29), the active and passive sensitivities of ω_0 are given as:

$$S^{\omega_0}_{I_{\text{B1}},\alpha_1,\alpha_2,\beta_1,\beta_2,R_2} = -S^{\omega_0}_{I_{\text{B2}},C,R_1,R_3} = 1, \quad S^{\omega_0}_{\alpha_3,\alpha_4} = 0, \tag{4.30}$$

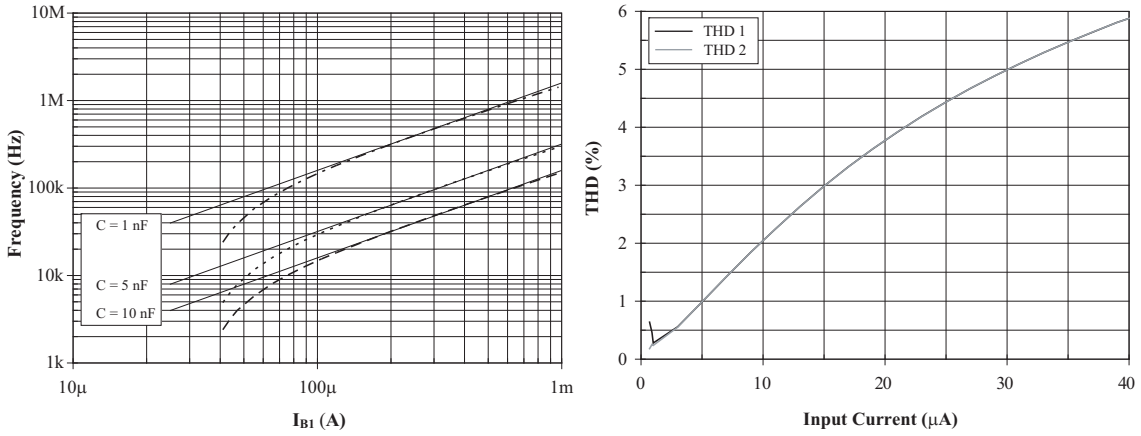
and it is evident that the sensitivities of active parameters and passive components for ω_0 are unity in relative amplitude.

Using the bipolar implementation of the VGC-MCFOA shown in Fig. 3.36, the proposed all-pass filter has been simulated in the SPICE software. The ideal and



(a) (b)

Fig. 4.6: Electronical tunability of the pole frequency by bias current I_{B1}: (a) inverting and (b) non-inverting CM first-order all-pass filter responses



(a) (b)

Fig. 4.7: (a) Possibility of tuning the pole frequency by the bias current I_{B1} at different values of C, (b) THD variation of the proposed all-pass filter for both responses against applied input current

simulated gain and phase responses and electronical tunability of the circuit by the bias current I_{B1} (when $I_{\mathrm{B2}} = 100$ μA) are demonstrated in Fig. 4.6. In the simulations the passive element values were selected as $C = 5$ nF, $R_1 = R_2 = R_3 = 1$ kΩ and the voltage gain h has been varied as $h = \{0.52; 1.06; 3.15; 10.5\}$ to set the pole frequency of the proposed circuit as $f_0 \approx \{10.2; 31.5; 101; 316\}$ kHz. Similarly, possibility of tuning the pole frequency by the bias current I_{B1} at three different values of C is shown in Fig. 4.7(a). The THD variation with respect to amplitude of the applied sinusoidal input current at 10 kHz (filter parameter: $f_0 \approx 101$ kHz) is shown in Fig. 4.7(b). An input with the amplitude of 15 μA yields for both responses THD values of 2.98%. From the simulations it is evident that the gain and phase

characteristics of the filter are in good agreement with theory. The deviation shown is Fig. 4.7(a) is caused by the non-idealities of the active element used.

4.4 Electronically tunable resistorless CM all-pass filter employing single grounded capacitor

A close investigation of CM all-pass filters presented in the previous Sections reveals that the proposed circuits suffer from weaknesses such as the use of excessive number of passive/active components or floating capacitor. Both of the aforementioned disadvantages are solved in the recently reported CITA-based realization in [14] and CDTA-based realization in [90]. The features like the use of single active element, no external resistors, single grounded capacitor, and electronic tunability of the pole frequency makes the realizations in [14] and [90] by far the most appropriate CM all-pass filters.

In [188], additional realization of such all-pass filter is presented, which consists of a single CBTA [8], [119], and only grounded capacitor. The proposed CM CBTA-C first-order APF is shown in Fig. 4.8. Assuming an ideal CBTA, for the proposed CBTA-C all-pass filter in Fig. 4.8 routine circuit analysis yields the following transfer function:

$$T(s) = \frac{I_{out}}{I_{in}} = \frac{sC - g_m}{sC + g_m}. \tag{4.31}$$

Considering the transconductance g_m of the CBTA as $g_m{=}I_{\mathrm{B}}/2V_{\mathrm{T}}$ as stated above, the (4.31) changes as follows:

$$T(s) = \frac{I_{out}}{I_{in}} = \frac{2V_{\mathrm{T}}sC - I_{\mathrm{B}}}{2V_{\mathrm{T}}sC + I_{\mathrm{B}}}. \tag{4.32}$$

The phase response from the TF (4.32) is calculated as:

$$\varphi(\omega) = 180^\circ - 2\mathrm{arctg}\left(\frac{2V_{\mathrm{T}}\omega C}{I_{\mathrm{B}}}\right). \tag{4.33}$$

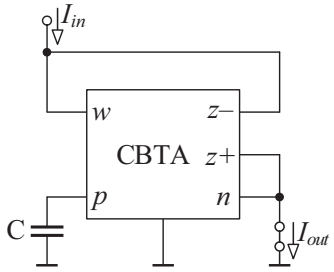


Fig. 4.8: Proposed current-mode CBTA-C first-order all-pass filter

From (4.33) it can be clearly seen that the natural pole frequency $\omega_0 = I_\mathrm{B}/2V_\mathrm{T}C$ is easily tunable by means of the bias current I_B.

The sensitivities of the natural pole frequency are given as:

$$S_{I_\mathrm{B}}^{\omega_0} = -S_C^{\omega_0} = 1, \tag{4.34}$$

which are not higher than unity in magnitude.

Taking into account non-idealities of the CBTA, the TF (4.32) of the filter in Fig. 4.8 converts to:

$$T(s) = \frac{I_{out}}{I_{in}} = \frac{\alpha_p 2V_\mathrm{T}sC - \alpha_n I_\mathrm{B}}{2V_\mathrm{T}sC + \alpha_n I_\mathrm{B}}, \tag{4.35}$$

and non-ideal phase response from TF (4.35) is given as:

$$\varphi(\omega) = 180^\circ - \mathrm{arctg}\left(\frac{\alpha_p 2V_\mathrm{T}\omega C}{\alpha_n I_\mathrm{B}}\right) - \mathrm{arctg}\left(\frac{2V_\mathrm{T}\omega C}{\alpha_n I_\mathrm{B}}\right). \tag{4.36}$$

From (4.35) and (4.36) it is clear that both gain and phase of the filter are slightly affected by the non-idealities, and hence, a good design of CBTA should be considered to alleviate the non-ideal effects. The natural pole frequency of the presented filter changes to:

$$\omega_0 = \frac{\alpha_n I_\mathrm{B}}{2V_\mathrm{T}C}. \tag{4.37}$$

From (4.37) it can be realized that the non-idealities of the CBTA slightly affect the natural pole frequency, however, the influence can be easily compensated by the bias current I_B.

Using the bipolar implementation of the CBTA shown in Fig. 3.28, the proposed all-pass filter has been simulated in the SPICE software. The value of the capacitor C was selected as 1.5 nF and the transconductance $g_m = 1$ mA/V ($I_\mathrm{B} = 52$ μA), which

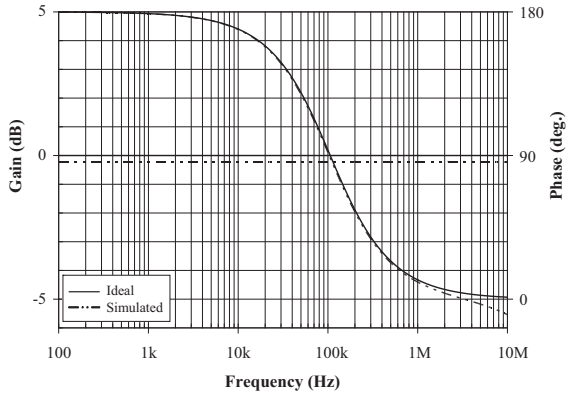
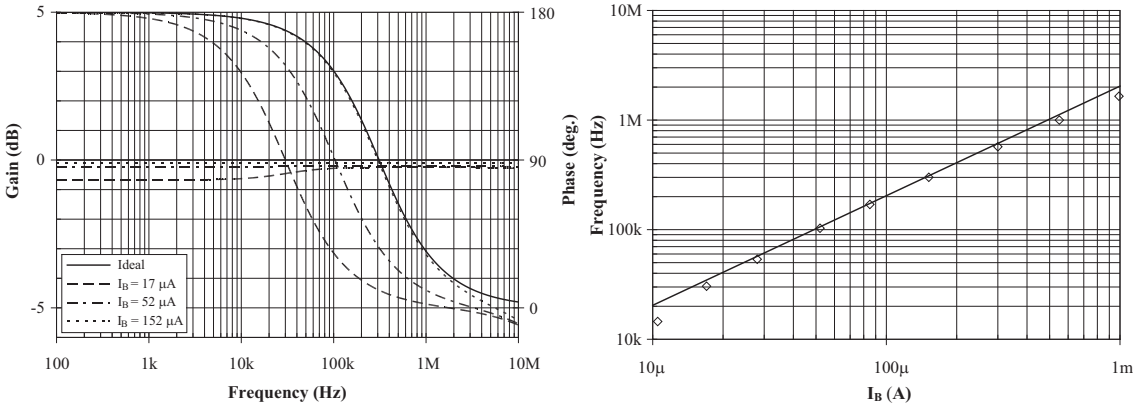


Fig. 4.9: Simulated gain and phase characteristics of the proposed CM first-order all-pass filter



(a) (b)

Fig. 4.10: (a) Electronical tunability of phase response and (b) possibility of tuning the pole frequency f_0 by the bias current I_B

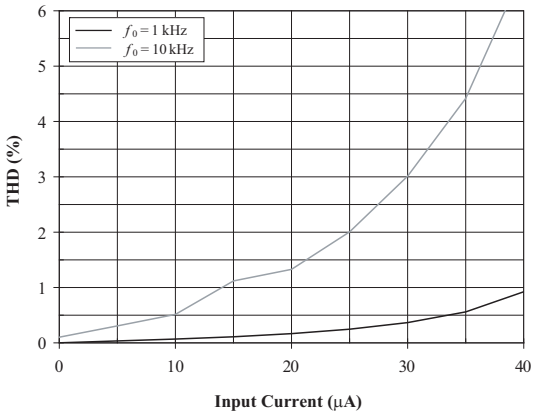


Fig. 4.11: THD of the proposed all-pass filter with respect to applied sinusoidal input current

results in a 90° phase shift at $f_0 \cong 100$ kHz. The gain and phase characteristics of the simulated circuit are shown in Fig. 4.9. Fig. 4.10(a) shows the ideal and simulated phase and gain responses illustrating the electronical tunability of the filter. The pole frequency of the proposed circuit is varied for $f_0 \approx \{30; 100; 300\}$ kHz using the bias current $I_\mathrm{O} = \{17; 52; 152\}$ μA, respectively. Similarly, possibility of tuning the pole frequency by the bias current I_O is shown in Fig. 4.10(b). The THD variation with respect to amplitude of the applied sinusoidal input current at 1 and 10 kHz (filter parameter: $f_0 \approx 100$ kHz) is shown in Fig. 4.11. An input with the amplitude of 30 μA at 1 and 10 kHz yields THD values of 0.37 and 3.01%, respectively. The harmonic distortion at 10 kHz rapidly increases if the input signal amplitude is increased beyond 20 μA. From the simulation results it can be seen that the final soulution is in good agreement with the theory.

4.5 High-input and low-output impedance VM all-pass filters using single UVC

For the VM all-pass filters the high-input and low-output impedance is important, if these circuits are used as a load to another analog filter in the signal-processing path for compensating phase shifts. Due to this property, there will be no need for an additional buffer or current conveyor for cascading and this will decrease the number of active elements in the design. From the complexity point of view such all-pass filter is extremely interesting that moreover provides both inverting and non-inverting outputs at the same configuration simultaneously. For this purpose the UVC is ideal for such all-pass filter design due to its unique internal structure, be specific, high impedance voltage input and mutually inverse low impedance voltage outputs.

4.5.1 Cascadable all-pass filters without electronic tuning

The proposed VM first-order all-pass filters with high-input/low-output impedance that provide both inverting and non-inverting outputs at the same configuration simultaneously are shown in Fig. 4.12 [175]. For further analysis the circuit in Fig. 4.12(a) has been chosen, which employs one UVC, three resistors and a capacitor. Assuming $R_1 = R_2 = R_3/5 = R$, routine analysis yields voltage transfer functions that can be expressed in following forms:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{sCR - 1}{sCR + 1}, \tag{4.38}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{sCR - 1}{sCR + 1}. \tag{4.39}$$

As it is seen from these equations, both inverting (4.38) and non-inverting (4.39) output of VM first-order all-pass filter can be realized with the same circuit topology.

The phase responses of the filter are given as follows:

$$\varphi_1(\omega) = 180^\circ - 2\text{arctg}(\omega CR), \tag{4.40}$$

$$\varphi_2(\omega) = -2\text{arctg}(\omega CR). \tag{4.41}$$

The natural frequency ω_0 can be found as:

$$\omega_0 = \frac{1}{CR}. \tag{4.42}$$

As it is seen from above equations, the proposed configuration can provide phase

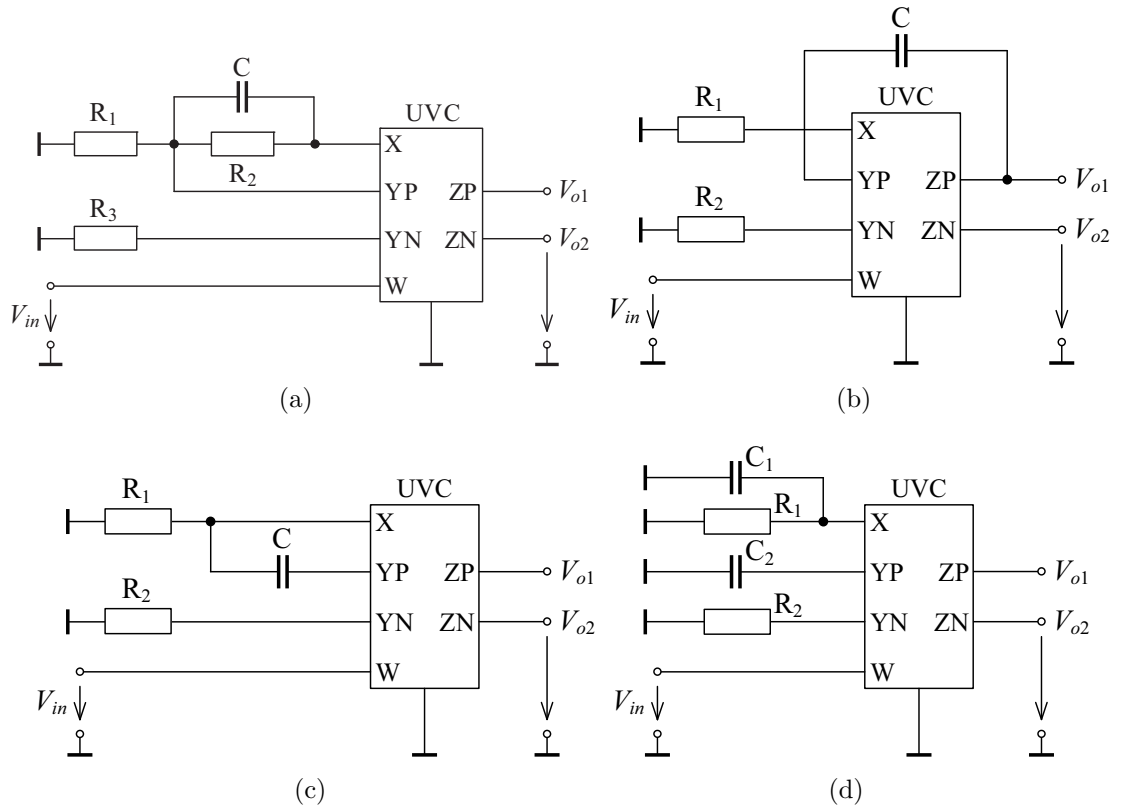


Fig. 4.12: Proposed all-pass filters with high-input and low-output impedance VM all-pass filters using single UVC

shifting both between 180° to 0° and 0° to –180°, respectively.

Taking into account the non-idealities of UVC and assuming again $R_1 = R_2 = R_3/5 = R$, the proposed all-pass filter transfer functions (4.38) and (4.39) become:

$$T_1(s) = \frac{\gamma_1[\delta_1 sCR(\alpha_1+1) - 5\alpha_2\delta_2 + 2\alpha_1\delta_1 + \delta_1]}{(\alpha_1+1)[sCR+1]}, \tag{4.43}$$

$$T_2(s) = -\frac{\gamma_2[\delta_1 sCR(\alpha_1+1) - 5\alpha_2\delta_2 + 2\alpha_1\delta_1 + \delta_1]}{(\alpha_1+1)[sCR+1]}. \tag{4.44}$$

The natural frequency ω_0 (4.42) can be expressed as:

$$\omega_0 = \frac{1}{CR}. \tag{4.45}$$

The active and passive sensitivities of ω_0 are given as:

$$S_R^{\omega_0} = S_C^{\omega_0} = -1, \quad S_{\alpha_1}^{\omega_0} = S_{\alpha_2}^{\omega_0} = S_{\delta_1}^{\omega_0} = S_{\delta_2}^{\omega_0} = S_{\gamma_1}^{\omega_0} = S_{\gamma_2}^{\omega_0} = 0. \tag{4.46}$$

From Eq. (4.46) it is evident that the natural frequency ω_0 is not affected by

Tab. 4.1: Non-ideal transfer functions and properties of circuits in Fig. 4.12(b)–(d)

Circuit	$T_1(s) = V_{o1}/V_{in}$	$T_2(s) = V_{o2}/V_{in}$	Natural pole frequency, ω_0	Matching conditions
Fig. 4.12(b)	$\frac{\gamma_1(\alpha_1\delta_1 sCR-\alpha_2\delta_2)}{\alpha_1\gamma_1 sCR+1}$	$-\frac{\gamma_2(\alpha_1\delta_1 sCR-\alpha_2\delta_2)}{\alpha_1\gamma_1 sCR+1}$	$\frac{1}{\alpha_1\gamma_1 CR}$	$R_1 = R_2 = R$
Fig. 4.12(c)	$\frac{\gamma_1[\delta_1 sCR(\alpha_1+1)-\alpha_2\delta_2]}{sCR(1+\alpha_1)+1}$	$-\frac{\gamma_2[\delta_1 sCR(\alpha_1+1)-\alpha_2\delta_2]}{sCR(1+\alpha_1)+1}$	$\frac{1}{CR(1+\alpha_1)}$	$R_1 = R_2 = R$
Fig. 4.12(d)	$\frac{\gamma_1(\alpha_1\delta_1 sCR-\alpha_2\delta_2)}{sCR+1}$	$-\frac{\gamma_2(\alpha_1\delta_1 sCR-\alpha_2\delta_2)}{sCR+1}$	$\frac{1}{CR}$	$R_1 = R_2 = R$ and $C_1 = C_2 = C$

non-idealities of the UVC. The sensitivities of passive components for ω_0 are unity in relative amplitude. Hence, the proposed filter shows low sensitive performance.

Non-ideal transfer functions and properties of circuits in Fig. 4.12(b)–(d) are given in Tab. 4.1. From Tab. 4.1 and from the description above of the circuit in Fig. 4.12(a) it can be seen that all circuits require at least one component-matching condition that might be disadvantage of the proposed circuits, however, it is possible to match resistors with much better precision than 0.1% in the current IC technology [54]. The use of floating capacitor in Fig. 4.12(a)–(c) can be also seen as disadvantage from easier IC implementation and absorbing parasitic capacitance points of view. However, as mentioned above, using advanced IC technologies the floating capacitor can easily be implemented. Only circuit in Fig. 4.12(d) employs only grounded passive elements, but the use of two capacitors is not that economical. From Tab. 4.1 the circuit in Fig. 4.12(d) shows the least sensitive performance.

Using the CMOS implementation of the UVC (Fig. 3.3), the proposed first-order all-pass filter in Fig. 4.12(a) has been designed for natural frequency $f_0 \approx 3.5$ MHz and simulated in SPICE software. The following values have been chosen: $C = 1$ pF, $R_1 = R_2 = 45\ \text{k}\Omega$ and $R_3 = 9\ \text{k}\Omega$. The transistor dimensions of the UVC from Fig. 3.3 are listed in Tab. 3.1. The transistors are modeled by the TSMC 0.35 μm CMOS process parameters given in Tab. A.2. The DC power supply voltages are equal to ± 2.5 V and bias currents I_O are 100 μA. The magnitude and phase characteristics of the simulated inverting and non-inverting output of VM first-order all-pass filter are shown in Fig. 4.13. From Fig. 4.13 it can be seen that the simulation results are in close proximity to the ideal ones. The total power dissipation of the proposed all-pass filter is found to be 6.14 mW. The THD variations with respect to amplitudes of the applied sinusoidal input voltages at 100 kHz (filter parameter: $f_0 \approx 3.5$ MHz) are shown in Fig. 4.14(a). An input with the amplitude of 100 mV yields THD values of 2.59% and 2.71%, respectively. Using the INOISE and ONOISE statements, the input and output noise behavior for both responses with respect to

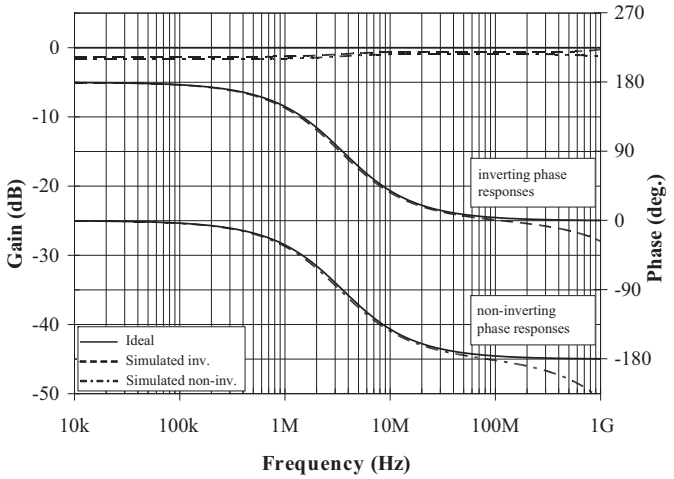
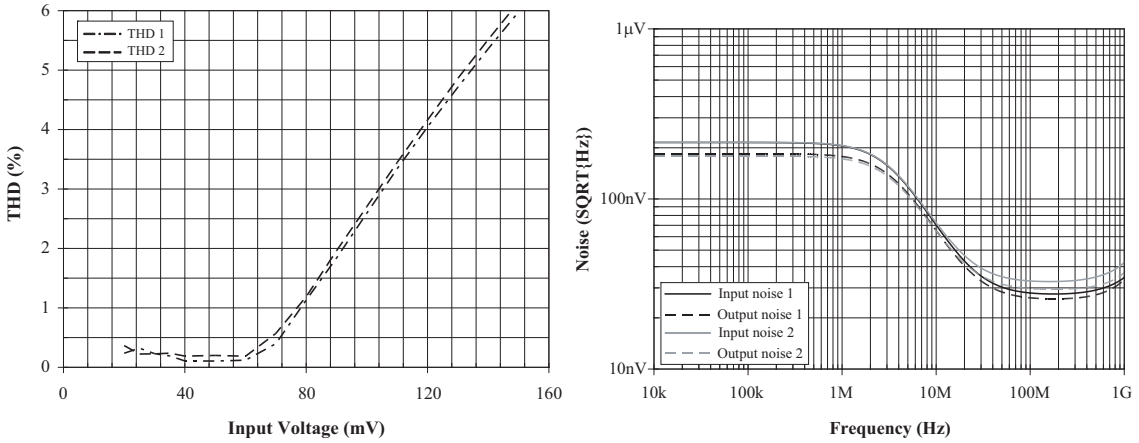


Fig. 4.13: Simulated magnitude and phase characteristics of the proposed inverting and non-inverting VM first-order all-pass filter in Fig. 4.12(a)

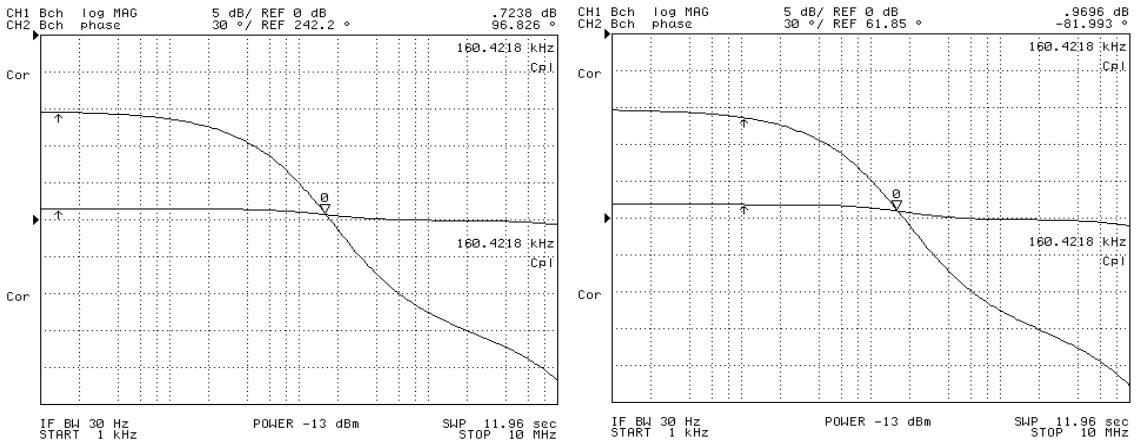


(a) (b)

Fig. 4.14: (a) THD variation of the proposed all-pass filter for both responses against applied input voltage, (b) input and output noise variations for both responses versus frequency

frequency have also been simulated, as it is shown in Fig. 4.14(b). The equivalent input/output noises for both responses at operating frequency ($f_0 \cong 3.5$ MHz) are found as 0.146/0.131 $\mu V/\sqrt{Hz}$ and 0.147/0.128 $\mu V/\sqrt{Hz}$, respectively.

In order to confirm the simulation results, the behavior of the proposed UVC-based all-pass filter has also been verified by experimental measurements. In the measurements the UVC-N1C 0520 [137], [196] integrated circuit has been used and the capacitor and resistors have been chosen as follows: $C = 1$ nF, $R_1 = R_2 = 1$ kΩ and $R_3 = 200$ Ω. In this case a 90° phase shift is at $f_0 \cong 159.15$ kHz. In the measurements the network analyzer Agilent 4395A has been used and the results are shown in Fig. 4.15. The real behavior of the filter is very satisfactory.

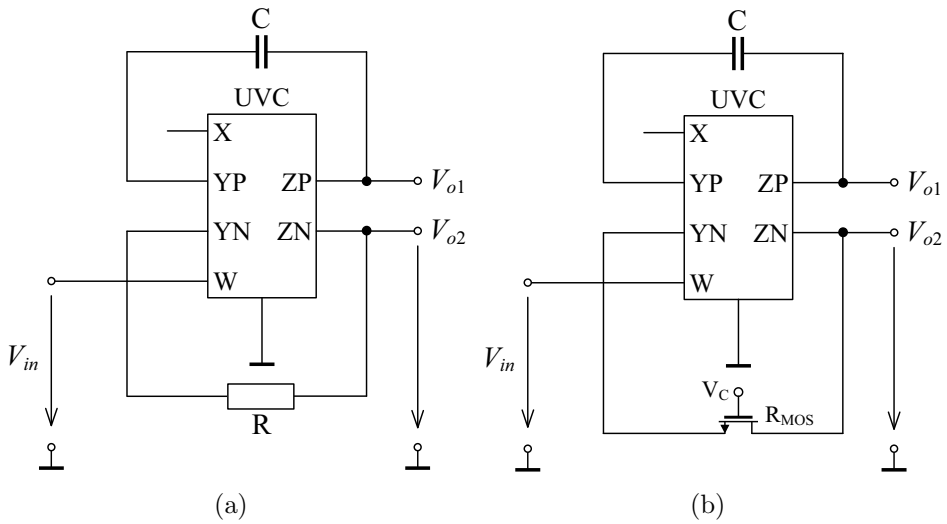


(a) (b)

Fig. 4.15: Measured gain and phase characteristics of the proposed inverting and non-inverting VM first-order all-pass filter: (a) $T_1(s)$, (b) $T_2(s)$

4.5.2 Electronically tunable MOSFET-C all-pass filter

In Fig. 4.12 four various cascadable all-pass filters with high-input and low-output impedance were presented, however, in all circuits at least one resistor matching-condition is needed that might be disadvantage from easy IC implementation point of view. This disadvantage is eliminated in circuit presented in Fig. 4.16(a). Since no admittance is connected to the X-port, the behavior of the UVC is similar to the conventional CFOA [138]. By replacing the appropriate floating resistor by OTA-



(a) (b)

Fig. 4.16: Proposed cascabable all-pass filter: (a) basic circuit, (b) MOSFET-C active equivalent circuit

based resistor equivalent and, furthermore, considering the electronical tunability property of the OTA used, phase responses of the proposed active-C circuit in [168] is controlled by an external bias current. This approach, however, results electronically tunable floating resistor simulator with large transistor count. As an alternative approach, the floating resistor of the proposed filter in Fig. 4.16(a) can be more effectively realized via n-channel MOSFET-based voltage-controlled resistor (VCR) [149]. The obtained MOSFET-C all-pass filter is given in Fig. 4.16(b), where the resistance R_{MOS} of the MOSFET transistor used can be calculated as follows:

$$R_{\mathrm{MOS}} = \frac{1}{\mu_0 C_{OX}(W/L)(V_{\mathrm{C}} - V_{\mathrm{T}})}, \tag{4.47}$$

where C_{OX} is the gate oxide capacitance per unit area, μ_0 is the free electron mobility in the channel, W and L are the channel width and length, V_{T} is the threshold voltage of the transistor, and V_{C} is DC control voltage used for tuning.

For the circuit in Fig. 4.16(b), routine analysis yields voltage transfer functions that can be expressed in following forms:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{sCR_{\mathrm{MOS}} - 1}{sCR_{\mathrm{MOS}} + 1}, \tag{4.48}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{sCR_{\mathrm{MOS}} - 1}{sCR_{\mathrm{MOS}} + 1}. \tag{4.49}$$

As it is seen from these equations, both inverting (4.50) and non-inverting (4.51) output of VM first-order all-pass filter can be realized with the same circuit topology.

The phase responses of the filter are given as follows:

$$\varphi_1(\omega) = 180^\circ - 2\mathrm{arctg}(\omega CR_{\mathrm{MOS}}), \tag{4.50}$$

$$\varphi_2(\omega) = -2\mathrm{arctg}(\omega CR_{\mathrm{MOS}}). \tag{4.51}$$

The natural frequency ω_0 can be found as:

$$\omega_0 = \frac{1}{CR_{\mathrm{MOS}}}. \tag{4.52}$$

As it is seen from above equations, the proposed configuration can provide phase shifting both between 180° to 0° and 0° to –180°. The shifted phase value can be easily controlled via the DC control voltage V_{C}.

Taking into account the non-idealities of UVC, the proposed all-pass filter transfer functions (4.50) and (4.51) become:

$$T_1(s) = \frac{V_{o1}}{V_{in}} = \frac{\gamma_1(\alpha_1\delta_1 sCR_{\mathrm{MOS}} - \alpha_2\delta_2)}{\alpha_1\delta_2\gamma_1 sCR_{\mathrm{MOS}} + \alpha_2\gamma_2}, \tag{4.53}$$

$$T_2(s) = \frac{V_{o2}}{V_{in}} = -\frac{\gamma_2(\alpha_1\delta_1 sCR_{\mathrm{MOS}} - \alpha_2\delta_2)}{\alpha_1\gamma_1 sCR_{\mathrm{MOS}} + \alpha_2\gamma_2}. \tag{4.54}$$

The natural frequency ω_0 (4.52) can be expressed as:

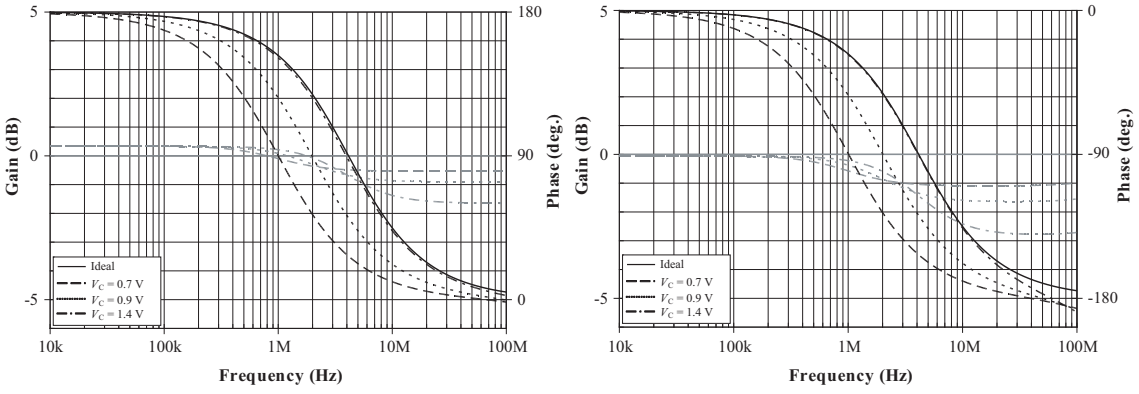
$$\omega_0 = \frac{\alpha_2\gamma_2}{\alpha_1\gamma_1 CR_{\mathrm{MOS}}}. \tag{4.55}$$

The active and passive sensitivities of ω_0 are given as:

$$S_{\alpha_2}^{\omega_0} = S_{\gamma_2}^{\omega_0} = -S_{\alpha_1}^{\omega_0} = -S_{\gamma_1}^{\omega_0} = -S_C^{\omega_0} = -S_{R_{\mathrm{MOS}}}^{\omega_0} = 1,\ S_{\delta_1}^{\omega_0} = S_{\delta_2}^{\omega_0} = 0. \tag{4.56}$$

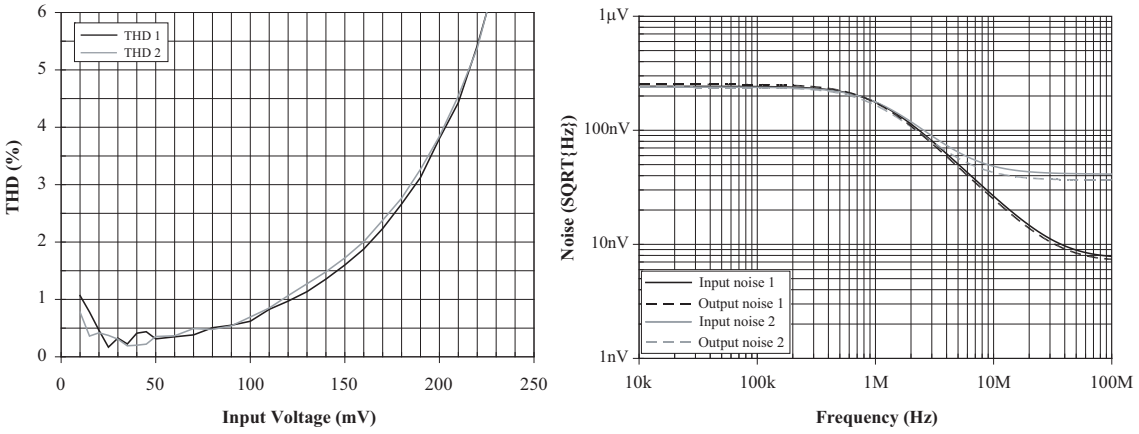
From Eq. (4.56) it is evident that the sensitivities of active and passive components for natural frequency ω_0 are unity in relative amplitude.

To verify the theoretical study, the behavior of the proposed VM all-pass filter has been verified by SPICE simulations. In the simulation the CMOS implementation of the UVC (Fig. 3.3) have been used. For this purpose the transistors are modeled by the TSMC 0.35 μm CMOS process parameters given in Tab. A.2. The transistor dimensions are listed in Tab. 3.1. The DC power supply voltages are equal to $\pm$2.5 V and bias currents I_{O} are 100 μA. The value of the capacitor C has been chosen as 5 pF. The NMOS based resistor, R_{MOS}, ($W = 2\mu$m, $L = 2\mu$m) is biased with the control voltages of $V_{\mathrm{C}} = \{0.7;\ 0.9;\ 1.4\}$ V to obtain $R_{\mathrm{MOS}} = \{31;\ 16;\ 7.7\}$ kΩ resistance values, respectively. The ideal and simulated gain and phase responses and electronical tunability of the circuit with V_{C} are shown in Fig. 4.17. The pole frequency of the presented filter is changed between 1 MHz and 3.95 MHz



(a) (b)

Fig. 4.17: Electronical tunability of the pole frequency with control voltage V_{C}: (a) inverting and (b) non-inverting VM first-order all-pass filter responses



(a) (b)

Fig. 4.18: (a) THD variation of the proposed all-pass filter for both responses against applied input voltage, (b) input and output noise variations for both responses versus frequency

successfully. From the simulation results it can be seen that the gain and phase characteristics of the proposed filter are in good agreement with theory.

The total power dissipation of the circuit is found to be 6.21 mW. The THD variations with respect to amplitudes of the applied sinusoidal input voltages at 10 kHz (filter parameter: $f_0 \approx 1$ MHz) are shown in Fig. 4.18(a). An input with the amplitude of 180 mV yields THD values of 2.66% and 2.76%, respectively. Using the INOISE and ONOISE statements, the input and output noise behavior for both responses with respect to frequency have also been simulated, as it is shown in Fig. 4.18(b). The equivalent input/output noises for both responses at operating frequency ($f_0 \cong 1$ MHz) are found as 0.176/0.174 $\mu V/\sqrt{Hz}$ and 0.177/0.166 $\mu V/\sqrt{Hz}$, respectively.

4.6 Electronically tunable resistorless all-pass filter using novel voltage conveyor

Nowadays, as already mentioned, the electronically tunable resistorless VM all-pass filters receive considerable attention. In current technical literature huge number of such filters are presented, where the tunability feature of circuits used are solved in different ways. For example, in recently presented voltage differencing-differential input buffered amplifier (VD-DIBA)-based VM all-pass filter [16] the tunability property of the OTA is used to shift the phase response of the circuit. Another technique is given in [101] and in circuit in Fig. 4.16(b), where the appropriate resistor is replaced via MOSFET-based VCR. After the CCCII [48] was introduced,

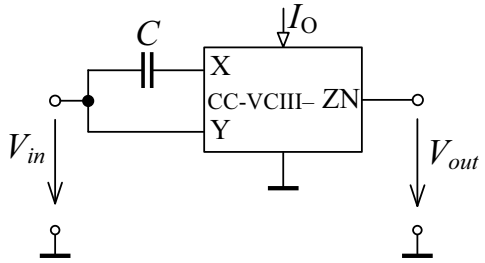


Fig. 4.19: Proposed electronically tunable resistorless first-order all-pass filter

a new period has been opened with respect to electronical tunability in the analog filter design. Here the intrinsic X-input resistance of the CCCII is controlled via an external current, as shown in [104]. The same technique is adapted to the novel type of voltage conveyor, namely CC-VCIII– [172], where analogously the input circuitry is formed by the CCCII.

The novel VM all-pass filter using canonic number of passive and active elements (i.e. single capacitor, and single CC-VCIII–) is shown in Fig. 4.19 [172]. Considering the ideal CC-VCIII– (i.e. α, δ, and γ are unity), routine analysis yields voltage transfer function in following form:

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{sCR_{\mathrm{Y}} - 1}{sCR_{\mathrm{Y}} + 1}. \tag{4.57}$$

From (4.57), the phase of the filter is found as:

$$\varphi(\omega) = -2\mathrm{arctg}(\omega CR_{\mathrm{Y}}), \tag{4.58}$$

and the natural frequency ω_0 can be express as:

$$\omega_0 = \frac{1}{CR_{\mathrm{Y}}}. \tag{4.59}$$

Taking into account the non-idealities of the CC-VCIII–, the TF in (4.57) converts to:

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{\gamma(sCR_{\mathrm{Y}} - \alpha)}{sCR_{\mathrm{Y}} + \alpha\delta\gamma}, \tag{4.60}$$

Assuming that all of the nonideal gains are constant in our frequency range of interest, the phase response of the filter is given as:

$$\varphi(\omega) = -\mathrm{arctg}\left(\frac{\omega CR_{\mathrm{Y}}}{\alpha}\right) - \mathrm{arctg}\left(\frac{\omega CR_{\mathrm{Y}}}{\alpha\delta\gamma}\right). \tag{4.61}$$

From (4.60) and (4.61) it can be seen that the non-idealities of the CC-VCIII– slightly affect the magnitude and phase responses of the filter. Consequently, the

pole frequency of the presented filter is found as:

$$\omega_0 = \frac{\alpha\delta\gamma}{CR_{\rm Y}}, \tag{4.62}$$

and the active and passive sensitivities of ω_0 are given as:

$$S_{\alpha}^{\omega_0} = S_{\delta}^{\omega_0} = S_{\gamma}^{\omega_0} = 1, \quad S_{C}^{\omega_0} = S_{R_{\rm Y}}^{\omega_0} = -1. \tag{4.63}$$

From Eq. (4.63) it is evident that all sensitivities of active parameters and passive components for ω_0 are unity in relative amplitude. Hence, the proposed filter shows low sensitive performance.

For a complete analysis of the circuit, it is also important to take into account parasitic impedances of the CC-VCIII–. Therefore, the matrix relationship of (3.24) changes as follows:

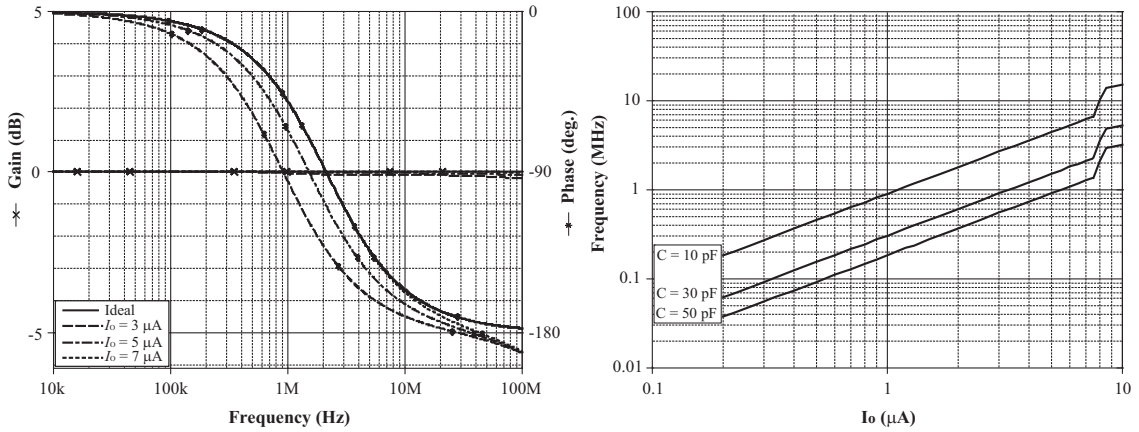
$$\begin{bmatrix} i_{\rm X} \\ v_{\rm Y} \\ v_{\rm ZN} \end{bmatrix} = \begin{bmatrix} sC_{\rm X} + \frac{1}{R_{\rm X}} & \alpha & 0 \\ \delta & R_{\rm Y} & 0 \\ -\gamma & 0 & sC_{\rm ZN} + \frac{1}{R_{\rm ZN}} \end{bmatrix} \begin{bmatrix} v_{\rm X} \\ i_{\rm Y} \\ i_{\rm ZN} \end{bmatrix}. \tag{4.64}$$

Here $R_{\rm X}$, $R_{\rm ZN}$, $C_{\rm X}$, and $C_{\rm ZN}$ are the parasitic resistances and capacitances at their relevant terminals. Considering these parasitics of the all-pass filter in Fig. 4.19, the ideal TF of (4.57) turns to be:

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{\gamma R_{\rm X}(sCR_{\rm Y} - \alpha)}{R_{\rm Y}R_{\rm X}s(C + C_x) + R_{\rm Y} + \alpha\delta\gamma R_{\rm X}}, \tag{4.65}$$

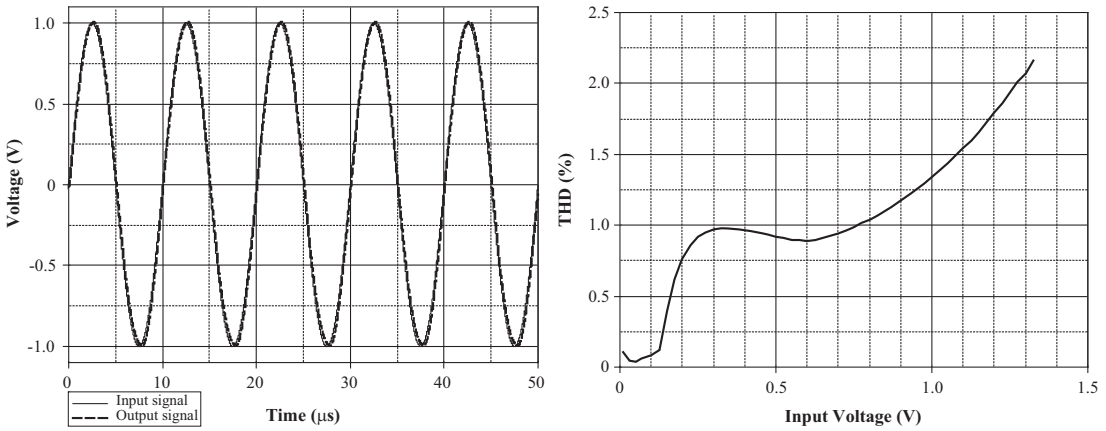
where $R_{\rm X}$ and $C_{\rm X}$ denote parasitic resistance and capacitance at X terminal of the CC-VCIII–. Note that the parasitic capacitance $C_{\rm X}$ can be absorbed into the external capacitor as it appears in parallel with it. If $R_{\rm Y}$ is sufficiently higher than $R_{\rm X}$ and $C \gg C_{\rm X}$, the TF in (4.65) become to form presented in (4.60).

Using the CMOS implementation of the CC-VCIII– (Fig. 3.40), the proposed circuit in Fig. 4.19 has been simulated in SPICE software. The transistor dimensions of the active element are listed in Tab. 3.4. The transistors are modeled by the TSMC 0.35 μm CMOS process parameters given in Tab. A.2. The DC power supply voltages are equal to ± 2.5 V and $V_{\rm B} = -1.7$ V. Fig. 4.20(a) shows the ideal and simulated phase and gain responses illustrating the electronic tunability for $C = 30$ pF. The pole frequency of the proposed filter is varied for $f_0 \approx = \{0.908; 1.52; 2.12\}$ MHz using the bias current $I_{\rm O} = \{3;\ 5;\ 7\}$ μA, respectively. Similarly, possibility of tuning the pole frequency by the bias current $I_{\rm O}$ at three different values of C is shown in Fig. 4.20(b). To illustrate the time-domain performance, transient analysis is performed to evaluate the voltage swing capability and phase errors of the filter



(a) (b)

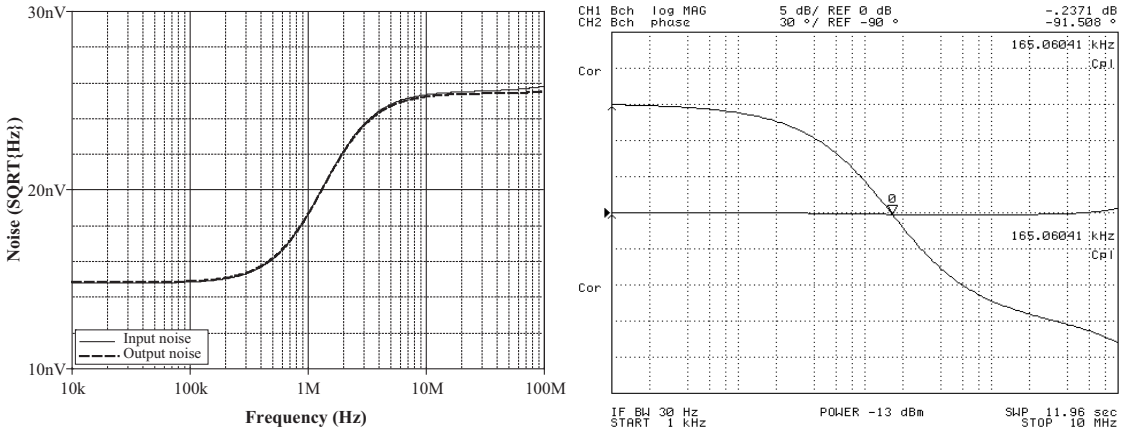
Fig. 4.20: a) Electronical tunability of gain and phase responses by the bias current I_{O}, (b) possibility of tuning the pole frequency by the bias current I_{O} at different values of C



(a) (b)

Fig. 4.21: (a) Time-domain responses of the proposed all-pass filter at 100 kHz, (b) THD of the all-pass filter at 100 kHz

as shown in Fig. 4.21(a). A sine-wave input of 1 V amplitude and frequency of 100 kHz was applied to the filter while keeping the bias current $I_{\mathrm{O}} = 5$ μA and $C = 30$ pF. Note that the output waveform is very close to the input one. The THD variation with respect to amplitude of the applied sinusoidal input voltage at 100 kHz (filter parameter: $I_{\mathrm{O}} = 5$ μA and $C = 30$ pF) is shown in Fig. 4.21(b). The THD rapidly increases when the input signal is increased beyond 0.7 V amplitude. An input with the amplitude of 1 V yields THD value of 1.34%. Using the INOISE and ONOISE statements, the input and output noise behavior with respect to frequency has also been simulated, as it is shown in Fig. 4.22(a). The equivalent input and output noises at pole frequency ($f_0 \cong 1.52$ MHz) are found as 20.83 and



(a) (b)

Fig. 4.22: (a) Input and output noise variations versus frequency, (b) measured gain and phase characteristics of the proposed VM first-order all-pass filter

20.82 nV/$\sqrt{\text{Hz}}$, respectively. The total power dissipation of the proposed all-pass filter at $f_0 \approx 1.52$ MHz is found to be 15.6 mW.

In order to confirm the simulation results, the behavior of the proposed all-pass filter has also been verified by experimental measurements. In the measurements the UVC-N1C 0520 [137], [196] integrated circuit has been used. The capacitor value has been chosen as 1 nF and the intrinsic resistance value of the Y terminal has been selected as 1 kΩ. In this case a 90° phase shift is at $f_0 \cong 159.15$ kHz. In the measurements the network analyzer Agilent 4395A has been used and the results are shown in Fig. 4.22(b). The real behavior of the filter corresponds to theory well.

4.7 Dual-mode first-order all-pass filters using single DBTA

In previous Sections various CM or VM all-pass filters are presented. Currently however, more interesting are the trans-admittance circuits that are used as an interface connecting a voltage-mode circuit to a current-mode circuit [145]. One of the most important application areas of trans-admittance-mode filters are the receiver baseband blocks of modern radio systems. Since there is no all-pass filter structure in the current technical literature that operates in trans-admittance- and voltage-mode simultaneously. Such filter could be operated in dual mode at the same time. Therefore, in [170] a new general configuration realizing trans-admittance- and voltage-mode first-order all-pass filters using a single DBTA and four passive admittances was presented. By systematic generation various dual-mode filters have been derived from the presented configuration. This kind of approach requires an

Tab. 4.2: Transfer functions and properties of the circuits

Circuit no.	Y_1	Y_2	Y_3	Y_4	$T_V(s) = V_{out}/V_{in}$	$T_{TA}(s) = I_{out}/V_{in}$	Natural pole frequency, ω_0	Matching conditions
1	G_1	G_2	sC_3	–	$\frac{2sC_3-G_2}{2sC_3+G_2}$	$-g_m\frac{2sC_3-G_2}{2sC_3+G_2}$	$\frac{G_2}{2C_3}$	$G_1 = 2G_2$
2	G_1	sC_2	G_3	–	$\frac{sC_2-2G_3}{sC_2+2G_3}$	$-g_m\frac{sC_2-2G_3}{sC_2+2G_3}$	$\frac{2G_3}{C_2}$	$G_1 = 4G_3$
3	G_1	sC_2	–	G_4	$\frac{sC_2-G_1}{sC_2+G_1}$	$-g_m\frac{sC_2-G_1}{sC_2+G_1}$	$\frac{G_1}{C_2}$	$G_1 = G_4$
4	G_1	–	sC_3	G_4	$\frac{2sC_3-G_1}{2sC_3+G_1}$	$-g_m\frac{2sC_3-G_1}{2sC_3+G_1}$	$\frac{G_1}{2C_3}$	$G_1 = G_4$

exhaustive analysis and time-consuming algebraic manipulations on complicated equations.

The proposed general configuration for realizing all-pass filters is shown in Fig. 4.23. Routine analysis yields the trans-admittance (TA) and voltage (V) transfer functions that can be expressed in following forms:

$$T_{TA}(s) = \frac{I_{out}}{V_{in}} = g_m\frac{Y_1 - Y_2 - 2Y_3}{Y_2 + 2Y_3 + Y_4}, \tag{4.66}$$

$$T_V(s) = \frac{V_{out}}{V_{in}} = -\frac{Y_1 - Y_2 - 2Y_3}{Y_2 + 2Y_3 + Y_4}. \tag{4.67}$$

Selecting of different components for Y_1 to Y_4 ideally realizes twelve different all-pass filter realizations. Tab. 4.2 presents only four most interesting cases in the meaning of integration. From Tab. 4.2 it can be seen that all proposed circuits employ three passive elements. All circuits require at least one component-matching condition that might be disadvantage of the proposed circuits. Other eight possible cases exist, however, they employ two capacitors or two component-matching conditions are required. Hence, they are not attractive for integration.

For further analysis from the Tab. 4.2 the circuit no. 3 has been chosen. The selected filter is shown in Fig. 4.24. Transfer functions, natural pole frequency, and

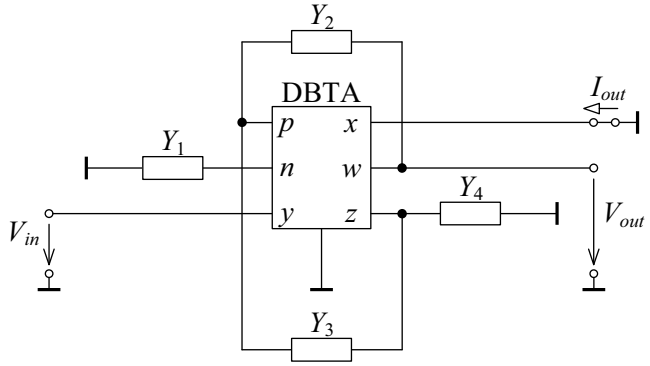


Fig. 4.23: The proposed general configuration for realizing all-pass filters

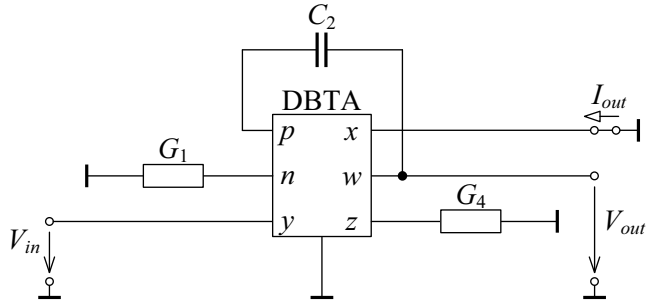


Fig. 4.24: Filter design example no. 3 for analysis

the matching condition are shown in Tab. 4.2. The phase responses of this filter can be given as follows:

$$\varphi_{TA3}(\omega) = -2\text{arctg}\left(\frac{\omega C_2}{G_1}\right), \tag{4.68}$$

$$\varphi_{V3}(\omega) = 180^\circ - 2\text{arctg}\left(\frac{\omega C_2}{G_1}\right). \tag{4.69}$$

Taking into account the non-idealities of DBTA, the proposed all-pass filter transfer functions become:

$$T_{TA3}(s) = \frac{I_{out}}{V_{in}} = -g_m \frac{\alpha_p\beta_p sC_2 - \alpha_n\beta_n G_1}{\alpha_p\gamma sC_2 + G_1}, \tag{4.70}$$

$$T_{V3}(s) = \frac{V_{out}}{V_{in}} = \frac{\alpha_p\beta_p\gamma sC_2 - \alpha_n\beta_n\gamma G_1}{\alpha_p\gamma sC_2 + G_1}. \tag{4.71}$$

The non-ideal natural pole frequency ω_0 can be expressed as:

$$\omega_0 = \frac{G_1}{\alpha_p\gamma C_2}. \tag{4.72}$$

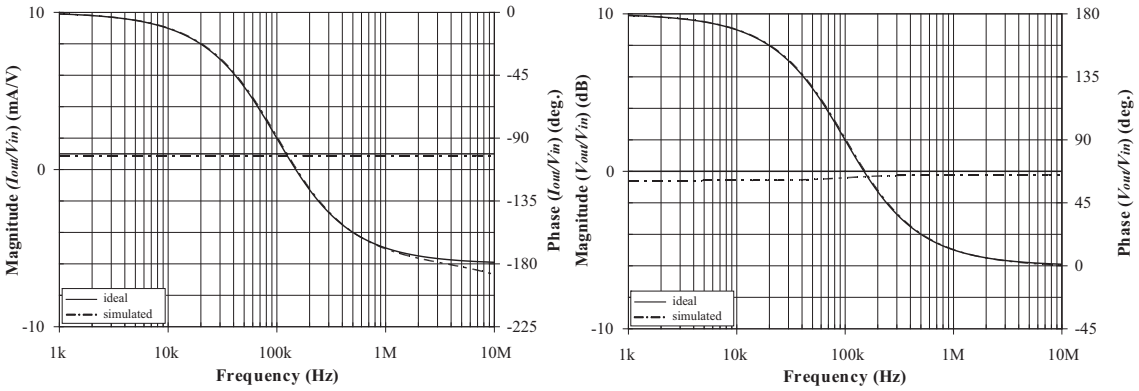
Note that by replacing resistors by FET-based VCR [126] or by the OTA, as it is shown in [168], the phase of the proposed circuit can be electronically tuned, which is also particular advantage of the proposed circuit.

The low active and passive sensitivities of ω_0 are given as:

$$|S^{\omega_0}_{\alpha_p,\gamma,C_2,G_1}| = 1, \quad S^{\omega_0}_{\alpha_n,\beta_p,\beta_n,g_m} = 0. \tag{4.73}$$

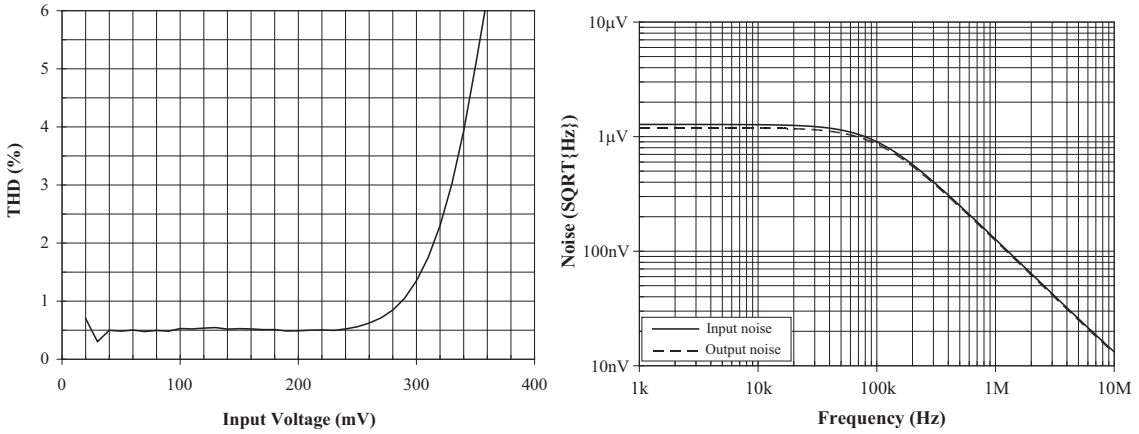
From Eq. (4.73) it is evident that the sensitivities of active and passive components for pole frequency ω_0 are no more than unity in relative amplitude.

Using the bipolar implementation of the DBTA shown in Fig. 3.7, the proposed all-pass filter has been simulated in the SPICE software. The passive element values were selected as: $C_2 = 120$ pF, $R_1 = R_4 = 13.3$ kΩ and the transconductance



(a) (b)

Fig. 4.25: The magnitude and phase characteristics of the proposed (a) non-inverting type trans-admittance- and (b) inverting type voltage-mode first-order all-pass filter



(a) (b)

Fig. 4.26: (a) THD variation of the proposed all-pass filter for the VM response against applied input voltage, (b) input and output noise variations for the VM response versus frequency

$g_m = 1$ mA/V ($I_B = 52$ μA), which results in a 90° phase shift at $f_0 \cong 100$ kHz. The magnitude and phase characteristics of the simulated circuit are shown in Fig. 4.25. From the results it can be seen that both the magnitude and phase characteristics are in good agreement with theory. The total power dissipation of the proposed all-pass filter is found to be 14.6 mW. The THD variation of the VM response with respect to amplitude of the applied sinusoidal input voltage at 10 kHz is shown in Fig. 4.26(a). An input with the amplitude of 300 mV yields THD value of 1.35%. Using the INOISE and ONOISE statements, the input and output noise behavior for the VM response has also been simulated. From the simulation results in Fig. 4.26(b) it can be seen that the input and output noise at $f_0 \cong 100$ kHz are found as 0.902 and 0.861 $\mu V/\sqrt{Hz}$, respectively.

4.8 Sub-conclusion

This Chapter presents four current-, seven voltage-, and one mixed-mode first-order all-pass filter structures. The comparison of the proposed circuits is given in Tab. B.1.

Although a vast catalogue on first-order filter, amplifier, and integrator realizations is available in the literature, a unified structure capable of realizing these functions simultaneously in current-mode has not been previously reported. Therefore, the first Section remits on this problem by presenting new topologies using single here defined GCFDITA that are suitable to realize CM amplifier, integrator, first-order low-, high-, and all-pass filters by the same circuit topology.

Proposed circuits in Fig. 4.3 [171] and Fig. 4.5 employing CCCFTAs and VGC-MCFOA, respectively, enable both the inverting and the non-inverting type of AP filter responses simultaneously. Hence, for realizing the complementary type, there is no need to change the circuit topology. Moreover, the natural frequency of the filters can be easily tuned by means of the external control current or the voltage gain h, respectively.

In the Section 4.4, the versatility of the CBTA has been demonstrated in creating CM all-pass filter [188], which offers advantages such as no use any external resistors, use of grounded capacitor, and easy tunability of the pole frequency by means of external current. Furthermore, a low input impedance and high output impedance make the proposed circuit attractive for cascading to synthesize higher-order filters.

For cascading the VM all-pass filters, the high-input and low-output impedance is important. Moreover, from the complexity point of view all-pass filters that provide both inverting and non-inverting outputs at the same configuration simultaneously are extremely interesting. The Section 4.5, therefore, is focused on this problem by presenting four circuits without electronic tuning [175] and one circuit with easy tuning of pole frequency via single n-channel MOSFET-based VCR.

The application possibilities of here defined electronically tunable novel voltage conveyor (CC-VCIII–) is demonstrated on the resistorless first-order VM all-pass filter design. The pole frequency of the circuit is controlled with an external current of the intrinsic Y-input resistance. The circuit shows low sensitive performance and it contributes a wide range of frequency response, which is also confirmed by experimental measurements.

Finally, the Section 4.7 presents the first all-pass filter structure in the current technical literature, which operates in trans-admittance- and voltage-mode simultaneously [170]. From the new general configuration twelve different circuits have been derived, however from the integration point of view, only four most interesting cases are presented.

The SPICE simulations and experimental measurements confirm the workability of proposed circuits and results are in good agreement with theory.

5 SECOND-ORDER MULTIFUNCTION AND UNIVERSAL FILTERS

In the present days the highest attention is paid on such second-order filter structures that can provide at least the basic three standard filter functions, i.e. low-, band-, high-pass or all standard (also band-stop and all-pass) filter responses without changing the circuit topology. Such circuit topologies are called multifunction or universal filters, respectively. Probable the best known multifunction filtering structure is the KHN (Kerwin–Huelsman–Newcomb) that, furthermore, enables mutually independent control of the quality factor Q and characteristic frequency ω_0 [76]. This Chapter is focused on this issue by presenting one current- and three voltage-mode filter structures, one dual-mode KHN-equivalent structure, and furthermore, one VM general circuit topology to derive second-order inverse filters, which is very unique in current technical literature.

5.1 Single CCCFTA-based resistorless CM multifunction filter

A number of solutions concerning single ABB-based compact CM universal filter can be found in [29], [111], [132]. All three mentioned CM filters employ at least one resistor. Hence, they are not resistorless and thus less attractive for integrated circuit implementation. The only resistorless CM filter structure found is in [79] using two CDTAs are used. However, the use of two ABBs is not that economical and, furthermore, the presented circuit does not fully exploit the characteristics of the used CDTAs, since one of the input terminals n is not used. Thus, the aim of this Section is to introduce equivalent structure that is presented in [79], but using only single ABB. For this purpose the CCCFTA [171] is ideal due to its external features such as possibility of control the input impedance and the transconductance g_m.

The proposed CM SITO filter employing single CCCFTA and two capacitors is shown in Fig. 5.1 [182]. Routine analysis yields following non-ideal current TFs:

$$K_{\mathrm{CM_{HP}}} = \frac{I_{\mathrm{HP}}}{I_{in}} = -\frac{s^2 R_f C_1 C_2}{s^2 R_f C_1 C_2 + s C_2 + \alpha g_m}, \tag{5.1}$$

$$K_{\mathrm{CM_{BP}}} = \frac{I_{\mathrm{BP}}}{I_{in}} = \frac{\alpha s C_2}{s^2 R_f C_1 C_2 + s C_2 + \alpha g_m}, \tag{5.2}$$

$$K_{\mathrm{CM_{LP}}} = \frac{I_{\mathrm{LP}}}{I_{in}} = -\frac{\alpha g_m}{s^2 R_f C_1 C_2 + s C_2 + \alpha g_m}, \tag{5.3}$$

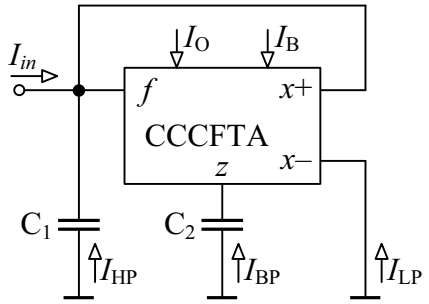


Fig. 5.1: Proposed CM multifunction filter employing single CCCFTA

where the natural frequency ω_0 and quality factor Q are defined as:

$$\omega_0 = \sqrt{\alpha \frac{g_m}{R_f C_1 C_2}}, \tag{5.4}$$

$$Q = \sqrt{\alpha \frac{R_f g_m C_1}{C_2}}. \tag{5.5}$$

From Eqs. (5.1)-(5.3) it can be observed that the proposed CM filter enables low-, band-, and high-pass responses simultaneously. Moreover, band-stop filter can be obtained by adding up the low- and high-pass responses and all-pass can also be obtained by adding up all three responses of the proposed circuit in Fig. 5.1. Hence, the proposed filter is universal.

The active and passive sensitivities of ω_0 and Q are:

$$S^{\omega_0}_{\alpha,g_m} = -S^{\omega_0}_{R_f,C_1,C_2} = \frac{1}{2}, \quad S^{Q}_{\alpha,R_f,g_m,C_1} = -S^{Q}_{C_2} = \frac{1}{2}. \tag{5.6}$$

From Eq. (5.6) it can be seen that the sensitivities are low and not higher than 0.5 in absolute value.

Using the bipolar implementation of CCCFTA (Fig. 3.21), the behavior of the proposed CM SITO universal filter has been verified by SPICE simulations. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1.

The active parameters and the passive elements in the proposed filter are selected as $I_O = 13$ μA ($R_f = 1$ kΩ), $I_B = 52$ μA ($g_m = 1$ mA/V), and $C_1 = C_2 = 160$ pF, which results in $f_0 = 1$MHz and $Q = 1$. The low-, band-, high-pass, and band-stop characteristics of the current-mode filter are shown in Fig. 5.2(a). In addition, the theoretical and simulated gain and phase responses of the all-pass filter are in Fig. 5.2(b).

Time-domain simulation result for the band-pass response of the proposed filter

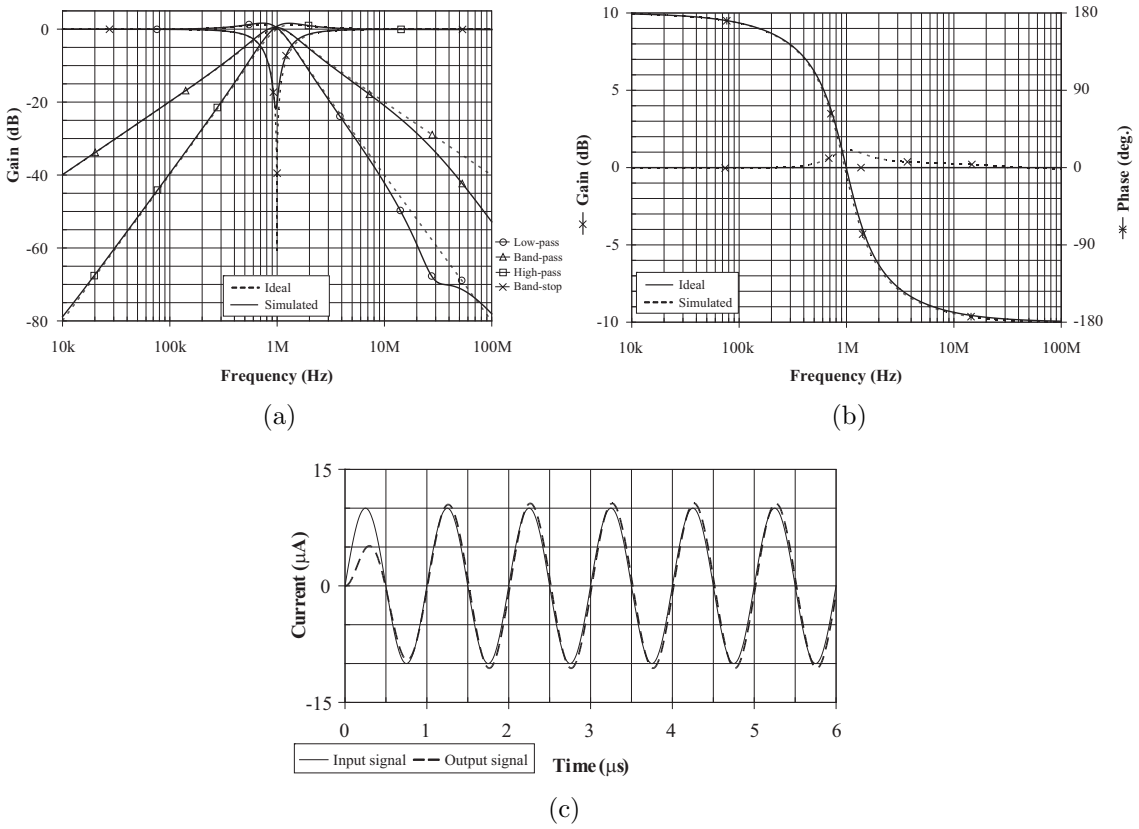


Fig. 5.2: Ideal and simulated (a) low-pass, band-pass, high-pass, and band-stop filter responses, (b) gain and phase responses of the all-pass filter, (c) time-domain band-pass response of the proposed filter

is shown in Fig. 5.2(c) in which a sinusoidal input current signal with 10 μA peak value at 1 MHz is applied to the filter. The THD is found to be 0.822%. The total power dissipation of the filter is found as 0.86 mW.

Here it should be noted that using the conventional CFTA five other CM universal filter structures have been proposed. The first circuit employing three CFTAs and three CMIs (current mirror and inverter) [72] enables realizing all standard filter functions at low-input and high-output impedances [181]. Unfortunately, the circuit does not allow independent control of Q and ω_0, therefore, in [183] PCAs have been used instead of CMIs. This replacement allows easy control of Q by means of "mu-factor" of the appropriate PCA. In [167] and [184] CM MISO (multi-input single-output) and CM SIMO (single-input multi-output) type of structures are proposed, respectively, and behavior of both circuits have been simulated using the UCC-N1B 0520 IC as shown in Fig. 3.17(b). Finally, the last paper concerning this ABB presents SITO CFTA-grounded-C universal filter [173]. The behavior of the circuit has been simulated using BJT CFTA implementation based on two CCIIs.

5.2 Universal VM filter employing single DBTA

This Section presents the application possibilities of the recently defined DBTA in VM universal filter. The proposed VM second-order filtering structure employing single DBTA and four passive components is shown in Fig. 5.3 [180]. Note that even if all passive elements are shown as floating, which might be not attractive for integration [2], [20], it should be mentioned that unused voltage inputs are always grounded, as described below.

The output voltages V_{o1} and V_{o2} of this circuit are given by the relations:

$$V_{o1} = \frac{G_1 g_m V_{i1} + sC_2 G_2 V_{i2} + s^2 C_1 C_2 V_{i3} - sC_2 g_m V_{i4}}{D}, \tag{5.7}$$

$$V_{o2} = \frac{-\left(sC_1 G_1 + G_1 G_2\right) V_{i1} + G_1 G_2 V_{i2} + sC_1 G_1 V_{i3} + \left(s^2 C_1 C_2 + sC_2 G_2\right) V_{i4}}{D}, \tag{5.8}$$

where

$$D = s^2 C_1 C_2 + sC_2 G_2 + G_1 g_m. \tag{5.9}$$

For the proposed filter depending on the status of circuit input four voltages V_{i1}, V_{i2}, V_{i3} and V_{i4} numerous filter functions are obtained. Based on the output selected there are two cases shown as presented below:

Case I. If the $V_o = V_{o1}$ is used as output, then from (5.7) the realizable transfer functions in voltage mode are:

(i) If $V_{i2} = V_{i3} = V_{i4} = 0$ (grounded), a low-pass filter (LP1) can be obtained with V_o / V_{i1};

(ii) If $V_{i1} = V_{i3} = V_{i4} = 0$ (grounded), a band-pass filter (BP1) can be obtained with V_o / V_{i2};

(iii) If $V_{i1} = V_{i2} = V_{i4} = 0$ (grounded), a high-pass filter (HP1) can be obtained

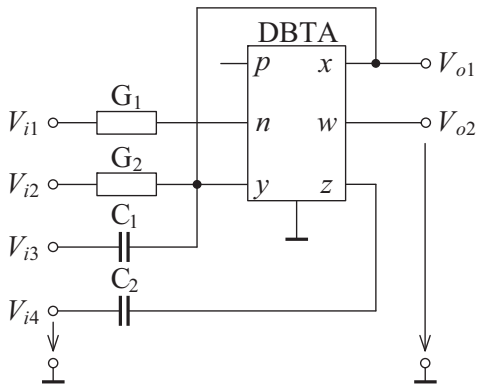


Fig. 5.3: Proposed voltage-mode universal filter using single DBTA

with V_o/V_{i3};

(iv) If $V_{i1} = V_{i2} = V_{i3} = 0$ (grounded), a band-pass filter (BP2) can be obtained with V_o/V_{i4};

(v) If $V_{i2} = V_{i4} = 0$ (grounded) and $V_{i1} = V_{i3} = V_{in}$, a band-stop filter (BS) can be obtained with V_o/V_{in};

(vi) If $V_{i1} = 0$ (grounded) and $V_{i2} = V_{i3} = V_{i4} = V_{in}$, an all-pass (AP) can be obtained with V_o/V_{in}.

In this case the proposed circuit is universal and can provide all standard types of filter functions, i.e. low-, band-, high-pass, band-stop, and an all-pass response without changing the circuit topology.

Case II. If the $V_o = V_{o2}$ is used as output, then from (5.8) the realizable transfer functions in voltage mode are:

(vii) If $V_{i1} = V_{i3} = V_{i4} = 0$ (grounded), a low-pass filter (LP2) can be obtained with V_o/V_{i2};

(viii) If $V_{i1} = V_{i2} = V_{i4} = 0$ (grounded), a band-pass filter (BP3) can be obtained with V_o/V_{i3};

(ix) If $V_{i3} = 0$ (grounded) and $V_{i1} = V_{i2} = V_{i4} = V_{in}$, a high-pass filter (HP2) can be obtained with V_o/V_{in}.

Thus, the circuit is multifunction and it is capable of realizing low-, band- and high-pass response without changing the circuit topology. In case of HP2 response the proposed circuit requires component matching conditions $C_1 = C_2$ and $G_1 = G_2$.

For all filters the natural frequency ω_0, quality factor Q and bandwidth BW derived from (5.9) are:

$$\omega_0 = \sqrt{\frac{G_1 g_m}{C_1 C_2}},\ Q = \frac{1}{G_2}\sqrt{\frac{C_1 G_1 g_m}{C_2}},\ \mathrm{BW} = \frac{\omega_0}{Q} = \frac{G_2}{C_1}. \tag{5.10}$$

Note that the quality factor Q can be controlled independently of natural frequency ω_0 by G_2. By replacing appropriate conductor by FET-based VCR [66], [126], the quality factor Q can be controlled electronically, which is particular advantage of the proposed circuit. The natural frequency ω_0 can be independently adjusted from the bandwidth, by varying C_2, G_1 or g_m of the proposed frequency filter. Here, the appropriate capacitor can be replaced by a voltage-controlled capacitor (VCC) [93], [109], or by digitally-controlled varactor (DCV) [30] for electronical control of the natural frequency ω_0 independently from the bandwidth.

The relative sensitivities of the ω_0, Q and BW parameters of the designed circuit derived from (5.10) are:

$$S^{\omega_0}_{G_1,g_m} = -S^{\omega_0}_{C_1,C_2} = \frac{1}{2}, \quad S^{\omega_0}_{G_2} = 0,$$

$$S^{Q}_{C_1,G_1,g_m} = -S^{Q}_{C_2} = \frac{1}{2}, \quad S^{Q}_{G_2} = -1, \tag{5.11}$$
$$S^{\mathrm{BW}}_{G_2} = -S^{\mathrm{BW}}_{C_1} = 1, \quad S^{\mathrm{BW}}_{C_2,G_1,g_m} = 0.$$

From the results it is evident that the sensitivities are low and not larger than unity of absolute value.

Taking into account the non-idealities of DBTA and assuming the transconductance g_m of its OTA as follows [33], [150]:

$$g_m = \frac{g_m \omega_g}{s + \omega_g} \cong g_m(1 - \mu s), \tag{5.12}$$

where ω_g is the first-pole of the OTA and $\mu = 1/\omega_g$, the denominator of (5.7), (5.8) becomes:

$$D = s^2 C_1 C_2 + s C_2 G_2 \left(1 - \frac{\alpha_{\mathrm{n}} \beta_{\mathrm{n}} G_1 g_m \mu}{C_2 G_2}\right) + \alpha_{\mathrm{n}} \beta_{\mathrm{n}} G_1 g_m. \tag{5.13}$$

Due to the parasitic effect, the characteristic departs from the ideal responses. But, the parasitic effect can be made negligible satisfying the following condition:

$$\frac{\alpha_{\mathrm{n}} \beta_{\mathrm{n}} G_1 g_m \mu}{C_2 G_2} \ll 1. \tag{5.14}$$

Using the bipolar implementation of the DBTA (Fig. 3.7), the proposed universal filter structure (*Case I*) has been designed for characteristic frequency $f_0 \approx 1$ MHz and the quality factor of filters $Q = 1$, and simulated in SPICE software. The following values have been chosen: $C_1 = C_2 = 150$ pF, $G_1 = G_2 = 1$ mA/V ($R_1 = R_2 = 1$ kΩ) and $g_m = 1$ mA/V ($I_{\mathrm{B}} = 50$ μA). For the practical measurements the DBTA has been implemented by using commercially available amplifiers,

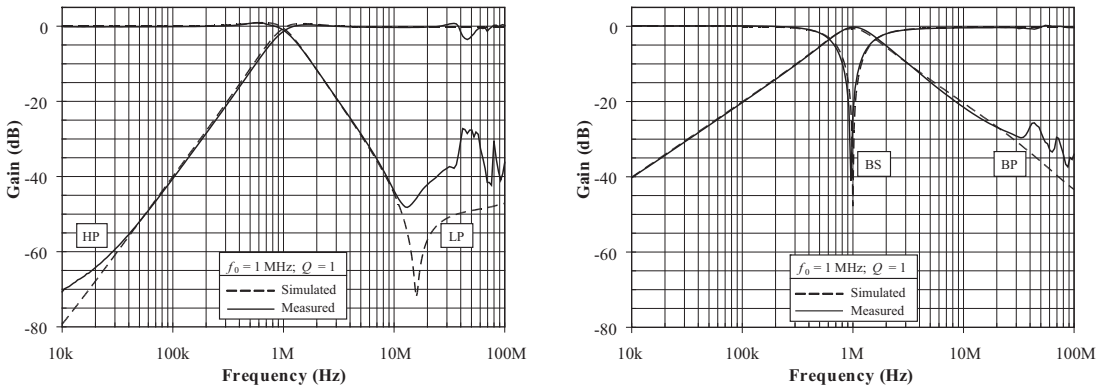


Fig. 5.4: Simulated and measured frequency characteristics for: (a) LP1 and HP1, (b) BP2 and BS responses of the proposed circuit of Fig. 5.3

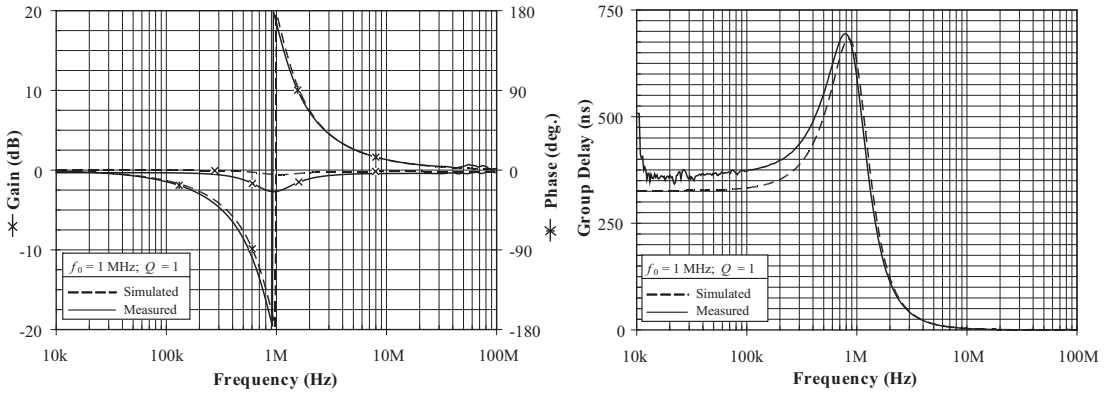


Fig. 5.5: Simulated and measured frequency responses of the all-pass (AP) filter: (a) gain and phase responses, (b) group delay response

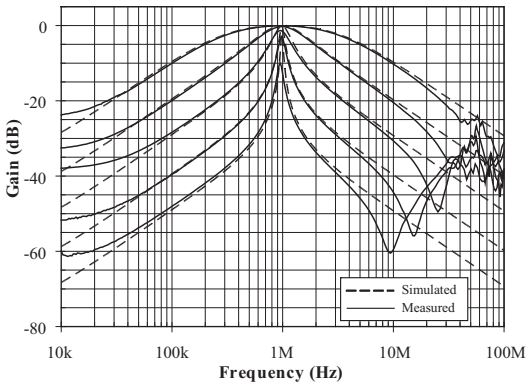


Fig. 5.6: Simulated and measured results of proposed voltage-mode band-pass filter (BP1) for values of quality factor $Q = \{0.3; 1; 3; 10; 30\}$

as shown in Fig. 3.9(b). The simulation and measurement results of the low- (LP1), band- (BP2), high-pass (HP1), band-stop (BS), and all-pass (AP) frequency filter working in voltage mode are shown in Fig. 5.4 and Fig. 5.5. Simulation and measurement results of the band-pass filter BP1 working in voltage mode are shown in Fig. 5.6. Here, the possibility of adjusting the quality factor Q is demonstrated. For required values $Q = \{0.3; 1; 3; 10; 30\}$ the conductivity must be $G_2 = \{3.333; 1.000; 0.333; 0.100; 0.033\}$ mA/V ($R_2 = \{0.3; 1; 3; 10; 30\}$ kΩ). From the results it is evident that the results of the measurements are in agreement with the simulations. In the higher-frequency region the real properties of the OPA860, MAX436 amplifiers and parasitic capacities or inductances of the constructed prototypes begin to be more significant.

5.3 Single MCFOA-based universal VM filters

The versatility of the MCFOA has already been demonstrated in grounded and floating inductors, capacitance multiplier, FDNR, and VM and CM filters [159]. However, to realize VM universal filter one of the input voltages have to be inverted. This weakness is eliminated in here presented circuits. The proposed VM universal filters in Fig. 5.7 require the minimum number of active and passive elements [174]. However, the passive elements are floating and the proposed filter topologies might be not attractive for integration [20]. Anyway, it should be mentioned that unused voltage inputs are always grounded, as described later. The ideal output voltage V_o of the circuit topology in Fig. 5.7(a) is given by the relation as follows:

$$V_o = \frac{G_1G_2V_{i1} + sC_1G_2V_{i2} - sC_1G_2V_{i3} + sC_1G_3V_{i4} + s^2C_1C_2V_{i5}}{s^2C_1C_2 + sC_1G_3 + G_1G_2}. \tag{5.15}$$

For the proposed filter depending on the status of circuit input five voltages V_{i1}, V_{i2}, V_{i3}, V_{i4} and V_{i5} numerous filter functions are obtained. From (5.15), we can see that:

(i) If $V_{i2} = V_{i3} = V_{i4} = V_{i5} = 0$ (grounded), a low-pass filter (LP) can be obtained with V_o/V_{i1};

(ii) If $V_{i1} = V_{i3} = V_{i4} = V_{i5} = 0$ (grounded), a band-pass filter (BP1) can be obtained with V_o/V_{i2};

(iii) If $V_{i1} = V_{i2} = V_{i4} = V_{i5} = 0$ (grounded), a band-pass filter (BP2) can be obtained with V_o/V_{i3};

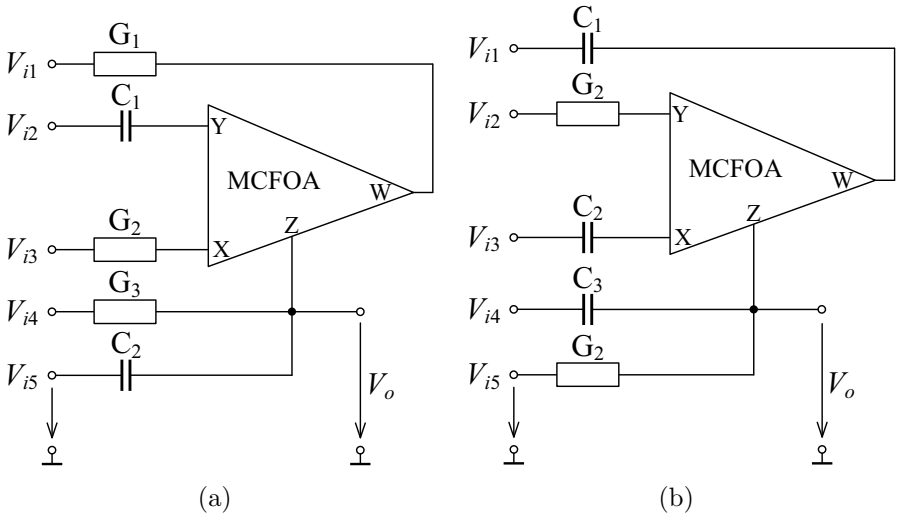


Fig. 5.7: Proposed voltage-mode universal filter topologies employing single MCFOA

(iv) If $V_{i1} = V_{i2} = V_{i3} = V_{i5} = 0$ (grounded), a band-pass filter (BP3) can be obtained with V_o/V_{i4};

(v) If $V_{i1} = V_{i2} = V_{i3} = V_{i4} = 0$ (grounded), a high-pass filter (HP) can be obtained with V_o/V_{i5};

(vi) If $V_{i2} = V_{i3} = V_{i4} = 0$ (grounded) and $V_{i1} = V_{i5} = V_{in}$, a band-stop filter (BS) can be obtained with V_o/V_{in};

(vii) If $V_{i2} = V_{i4} = 0$ (grounded), $V_{i1} = V_{i3} = V_{i5} = V_{in}$, and $G_2 = G_3$ an all-pass filter (AP) can be obtained with V_o/V_{in}.

Thus, the circuit is capable of realizing all standard filter functions such as low- (LP), band- (BP), high-pass (HP), band-stop (BS), and all-pass (AP) response without changing the circuit topology.

For all filters the natural frequency ω_0, quality factor Q and bandwidth BW derived from the denominator of (5.15) are:

$$\omega_0 = \sqrt{\frac{G_1 G_2}{C_1 C_2}},\ Q = \frac{1}{G_3}\sqrt{\frac{C_2 G_1 G_2}{C_1}},\ \mathrm{BW} = \frac{\omega_0}{Q} = \frac{G_3}{C_2}. \tag{5.16}$$

Note that, the quality factor Q of the proposed filter in Fig. 5.7(a) can be controlled independently of natural frequency ω_0 by varying G_3. By replacing appropriate conductor by FET-based VCR [66], [126] the quality factor Q can be controlled electronically that is a particular advantage of the proposed circuit. The natural frequency ω_0 can be independently adjusted from the bandwidth, by varying C_1, G_1 or G_2 of the proposed frequency filter.

Taking into account non-idealities of the MCFOA, the denominator of (5.15) becomes:

$$D_1 = s^2 C_1 C_2 + s C_1 G_3 + \alpha_1 \alpha_2 \beta_1 \beta_2 G_1 G_2. \tag{5.17}$$

The natural frequency ω_0, quality factor Q and bandwidth BW from (5.17) can be rewritten as:

$$\omega_0 = \sqrt{\alpha_1 \alpha_2 \beta_1 \beta_2 \frac{G_1 G_2}{C_1 C_2}},\ Q = \frac{1}{G_3}\sqrt{\alpha_1 \alpha_2 \beta_1 \beta_2 \frac{C_2 G_1 G_2}{C_1}},\ \mathrm{BW} = \frac{\omega_0}{Q} = \frac{G_3}{C_2}. \tag{5.18}$$

The active and passive sensitivities of the proposed VM universal filter topology in Fig. 5.15(a) derived from (5.18) are as follows:

$$\begin{aligned}
&S^{\omega_0}_{\alpha_1,\alpha_2,\beta_1,\beta_2,G_1,G_2} = -S^{\omega_0}_{C_1,C_2} = \frac{1}{2}, \quad S^{\omega_0}_{G_3} = 0, \\
&S^{Q}_{\alpha_1,\alpha_2,\beta_1,\beta_2,C_2,G_1,G_2} = -S^{Q}_{C_1} = \frac{1}{2}, \quad S^{Q}_{G_3} = -1, \\
&S^{\mathrm{BW}}_{G_3} = -S^{\mathrm{BW}}_{C_2} = 1, \quad S^{\mathrm{BW}}_{\alpha_1,\alpha_2,\beta_1,\beta_2,C_1,G_1,G_2} = 0.
\end{aligned} \tag{5.19}$$

From the results it is evident that the sensitivities are low and not larger than unity in absolute value.

By simple RC:CR transformation of the circuit of Fig. 5.7(a), the second VM universal filter topology employing single MCFOA and five passive elements has been derived. Routine analysis of the proposed filter topology in Fig. 5.7(b) yields the following voltage transfer functions:

$$K_{\mathrm{VM_{HP}}} = \frac{V_o}{V_{i1}} = \frac{s^2 C_1 C_2}{D_2}, \tag{5.20}$$

$$K_{\mathrm{VM_{BP1}}} = \frac{V_o}{V_{i2}} = \frac{sC_2 G_1}{D_2}, \quad K_{\mathrm{VM_{BP2}}} = \frac{V_o}{V_{i3}} = -\frac{sC_2 G_1}{D_2}, \quad K_{\mathrm{VM_{BP3}}} = \frac{V_o}{V_{i4}} = \frac{sC_3 G_1}{D_2}, \tag{5.21}$$

$$K_{\mathrm{VM_{LP}}} = \frac{V_o}{V_{i5}} = \frac{G_1 G_2}{D_2}, \tag{5.22}$$

$$K_{\mathrm{VM_{BS}}} = \frac{V_o}{V_{i1} + V_{i5}} = \frac{s^2 C_1 C_2 + G_1 G_2}{D_2}, \tag{5.23}$$

$$K_{\mathrm{VM_{AP}}} = \frac{V_o}{V_{i1} + V_{i3} + V_{i5}} = \frac{s^2 C_1 C_2 - sC_2 G_1 + G_1 G_2}{D_2}, \tag{5.24}$$

where

$$D_2 = s^2 C_1 C_2 + sC_3 G_1 + G_1 G_2. \tag{5.25}$$

As seen from (5.20)-(5.24), the proposed filter in Fig. 5.7(b) is capable of realizing all standard filter functions mentioned above. For all filters the natural frequency ω_0, quality factor Q and bandwidth BW derived from (5.25) are:

$$\omega_0 = \sqrt{\frac{G_1 G_2}{C_1 C_2}}, \; Q = \frac{1}{C_3}\sqrt{\frac{C_1 C_2 G_2}{G_1}}, \; \mathrm{BW} = \frac{\omega_0}{Q} = \frac{C_3 G_1}{C_1 C_2}. \tag{5.26}$$

The quality factor Q of the proposed filters can be controlled independently of natural frequency ω_0 by varying C_3. By replacing appropriate capacitor by VCC designed using a current-controlled voltage source (CCVS) and a current-controlled current source (CCCS) [109] or by DCV [30] the quality factor Q can be controlled electronically, which is advantage of the proposed circuit. The natural frequency ω_0 can be independently adjusted from the bandwidth, by varying G_2 of the proposed frequency filter.

Taking into account the non-ideal MCFOA, the denominator (5.25) of the transfer functions (5.20)-(5.24) becomes:

$$D_2 = \alpha_1 \alpha_2 \beta_1 \beta_2 s^2 C_1 C_2 + sC_3 G_1 + G_1 G_2, \tag{5.27}$$

and the natural frequency ω_0, quality factor Q and bandwidth BW can be rewritten

as:

$$\omega_0 = \sqrt{\frac{G_1 G_2}{\alpha_1\alpha_2\beta_1\beta_2 C_1 C_2}},\ Q = \frac{1}{C_3}\sqrt{\alpha_1\alpha_2\beta_1\beta_2\frac{C_1 C_2 G_2}{G_1}},\ \mathrm{BW} = \frac{\omega_0}{Q} = \frac{C_3 G_1}{\alpha_1\alpha_2\beta_1\beta_2 C_1 C_2}. \tag{5.28}$$

The active and passive sensitivities of the proposed VM universal filter topology in Fig. 5.7(b) derived from (5.28) are as follows:

$$\begin{aligned} S^{\omega_0}_{G_1,G_2} &= -S^{\omega_0}_{\alpha_1,\alpha_2,\beta_1,\beta_2,C_1,C_2} = \frac{1}{2}, \quad S^{\omega_0}_{C_3} = 0, \\ S^{Q}_{\alpha_1,\alpha_2,\beta_1,\beta_2,C_1,C_2,G_2} &= -S^{Q}_{G_1} = \frac{1}{2}, \quad S^{Q}_{C_3} = -1, \\ S^{\mathrm{BW}}_{C_3,G_1} &= -S^{\mathrm{BW}}_{\alpha_1,\alpha_2,\beta_1,\beta_2,C_1,C_2} = 1, \quad S^{\mathrm{BW}}_{G_2} = 0. \end{aligned} \tag{5.29}$$

From the results it is evident that the sensitivities are again low and not larger than unity in absolute value.

The behavior of the proposed VM universal filter topology in Fig. 5.7(a) has been verified by SPICE simulations. Used internal BJT structure of the MCFOA is shown in Fig. 3.32. In the simulations the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The behavior of the filter in Fig. 5.7(a) has also been simulated by SPICE software using model shown in Fig. 3.31(b). In the simulations the 3rd level model [137] of the UCC-N1B 0520 device has been used, which is based on the measurement of the fabricated 50 laboratory prototypes. Simulations using the real model of the UCC-N1B 0520 help more to verify and confirm the workability of the proposed circuit.

For the characteristic frequency $f_0 \approx 100$ kHz and the quality factor of filters $Q = 1$ the following passive component values have been chosen: $C_1 = C_2 = 1.5$ nF and $G_1 = G_2 = G_3 = 1$ mS ($R_1 = R_2 = R_3 = 1$ kΩ). The simulation results of the low- (LP), band- (BP2), high-pass (HP), band-stop (BS) and all-pass (AP) filter working in voltage mode are shown in Fig. 5.8(a)-(c). For the band-pass filter response BP3, the independent adjustment of the quality factor Q by varying the value of G_2 without affecting of the natural frequency ω_0 is shown in Fig. 5.8(d). Here, for chosen values $Q = \{0.3;\ 1;\ 3;\ 10;\ 30\}$ the conductivity must be $G_3 = \{3.333;\ 1.000;\ 0.333;\ 0.100;\ 0.033\}$ mA/V ($R_3 = \{0.3;\ 1;\ 3;\ 10;\ 30\}$ kΩ). The SPICE simulations confirm the feasibility of the proposed circuit. From the simulation results it is also evident that the final solution corresponds to the theory and both the MCFOA realizations are almost equivalent.

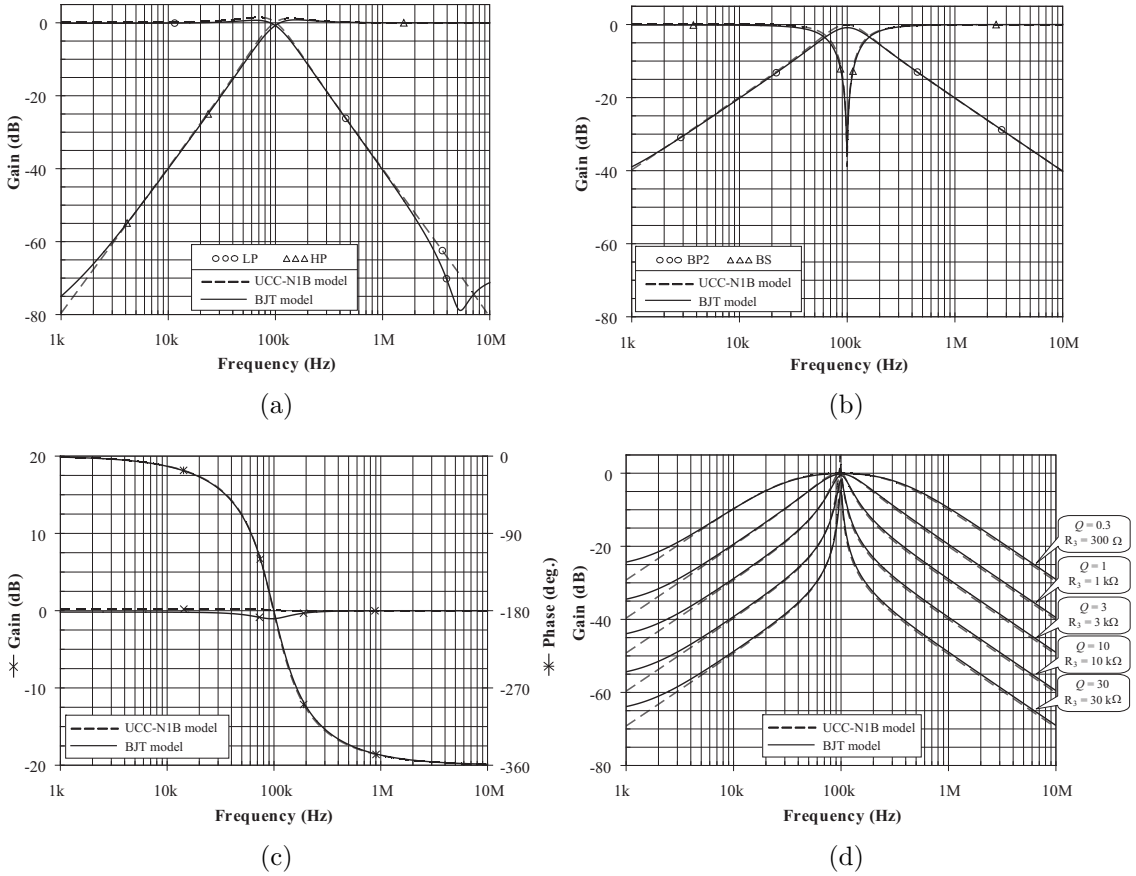


Fig. 5.8: Simulated frequency characteristics for (a) LP and HP, (b) BP2 and BS, (c) AP responses, (d) and BP3 for the values of quality factor $Q = \{0.3; 1; 3; 10; 30\}$ of the circuit in Fig. 5.7(a)

5.4 Dual-mode KHN-equivalent filter employing ZC-CFTAs

In the last decade, the KHN-equivalent filter design has received considerable attention due to their advantages, such as the universality, independent control of natural frequency and quality factor, and low sensitivity [76]. Large number of solutions concerning this issue can be found in the literature. The selected solutions working in current- and/or voltage-mode employ different active elements, such as CDBAs [121], CCCIIs [6], DDCCs [67], DVCCs [69], [195], VCs and current active elements [199], or UVCs [196]. Only [103] presents mixed-mode realization, where DVCCs are used as active elements. Therefore, there is still the need to propose novel KHN-equivalents with better properties. Hence, the aim of this Section is to present new mixed-mode KHN-equivalent using z-copy current follower transconductance amplifiers (ZC-CFTAs). Compared with above mentioned circuit in [103], here

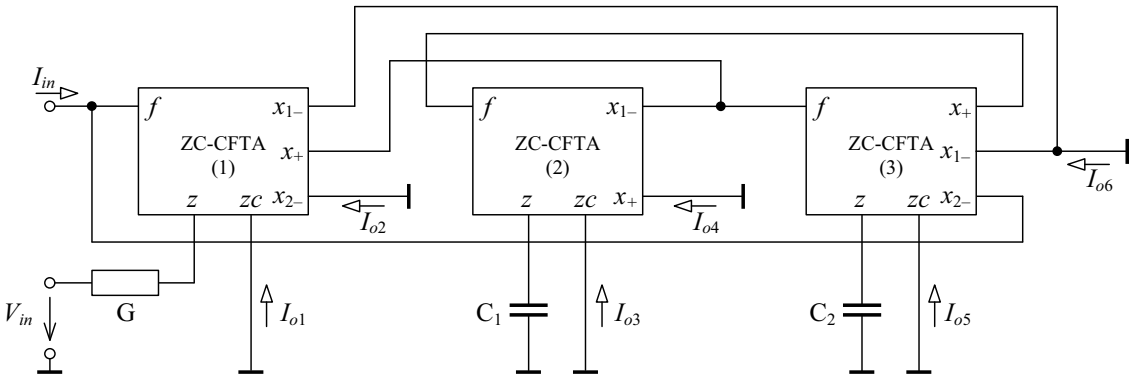


Fig. 5.9: Proposed dual-mode KHN-equivalent filter employing ZC-CFTAs

presented solution simultaneously provides all five standard filter functions directly without using additional active elements.

The proposed filter employing three ZC-CFTAs, single resistor, and two grounded capacitors is shown in Fig. 5.9 [179]. Routine analysis yields the following filter transfer functions:

(a) For CM operation, set $V_{in} = 0$; then:

$$K_{\mathrm{CM_{LP}}} = \frac{I_{o4}}{I_{in}} = -\frac{\frac{\alpha_1\alpha_2\alpha_3 g_{m1} g_{m2} g_{m3}}{C_1 C_2 G}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1} g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2} g_{m3}}{C_1 C_2}}, \tag{5.30}$$

$$K_{\mathrm{CM_{BP}}} = \frac{I_{o3}}{I_{in}} = \frac{s\frac{\alpha_1\alpha_3\gamma_2 g_{m1} g_{m3}}{C_2 G}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1} g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2} g_{m3}}{C_1 C_2}}, \tag{5.31}$$

$$K_{\mathrm{CM_{HP}}} = \frac{I_{o5}}{I_{in}} = -\frac{s^2\frac{\alpha_1\gamma_3 g_{m1}}{G}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1} g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2} g_{m3}}{C_1 C_2}}, \tag{5.32}$$

$$K_{\mathrm{CM_{BS1}}} = \frac{I_{o1}}{I_{in}} = \frac{s^2\gamma_1 + \frac{\alpha_2\alpha_3\gamma_1 g_{m2} g_{m3}}{C_1 C_2}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1} g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2} g_{m3}}{C_1 C_2}}, \tag{5.33}$$

$$K_{\mathrm{CM_{BS2}}} = \frac{I_{o2}}{I_{in}} = -\frac{s^2\frac{\alpha_1 g_{m1}}{G} - \frac{\alpha_1\alpha_2\alpha_3 g_{m1} g_{m2} g_{m3}}{C_1 C_2 G}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1} g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2} g_{m3}}{C_1 C_2}}, \tag{5.34}$$

$$K_{\mathrm{CM_{AP}}} = \frac{I_{o6}}{I_{in}} = -\frac{s^2\frac{\alpha_1 g_{m1}}{G} - s\frac{\alpha_1\alpha_3 g_{m1} g_{m3}}{C_2 G} + \frac{\alpha_1\alpha_2\alpha_3 g_{m1} g_{m2} g_{m3}}{C_1 C_2 G}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1} g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2} g_{m3}}{C_1 C_2}}, \tag{5.35}$$

(b) For TA-M (trans-admittance-mode) operation, set $I_{in} = 0$; then:

$$K_{\mathrm{TA-M_{LP}}} = \frac{I_{o4}}{V_{in}} = g_{m1}\frac{\frac{\alpha_2\alpha_3 g_{m2} g_{m3}}{C_1 C_2}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1} g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2} g_{m3}}{C_1 C_2}}, \tag{5.36}$$

$$K_{\mathrm{TA-M_{BP1}}} = \frac{I_{o1}}{V_{in}} = g_{m1}\frac{s\frac{\alpha_3\gamma_1 g_{m3}}{C_2}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1} g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2} g_{m3}}{C_1 C_2}}, \tag{5.37}$$

$$K_{\mathrm{TA-M_{BP2}}} = \frac{I_{o3}}{V_{in}} = -g_{m1}\frac{s\frac{\alpha_3\gamma_2 g_{m3}}{C_2}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1}g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2}g_{m3}}{C_1C_2}}, \tag{5.38}$$

$$K_{\mathrm{TA-M_{HP}}} = \frac{I_{o5}}{V_{in}} = g_{m1}\frac{s^2\gamma_3}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1}g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2}g_{m3}}{C_1C_2}}, \tag{5.39}$$

$$K_{\mathrm{TA-M_{BS}}} = \frac{I_{o2}}{V_{in}} = g_{m1}\frac{s^2 + \frac{\alpha_2\alpha_3 g_{m2}g_{m3}}{C_1C_2}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1}g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2}g_{m3}}{C_1C_2}}, \tag{5.40}$$

$$K_{\mathrm{TA-M_{AP}}} = \frac{I_{o6}}{V_{in}} = g_{m1}\frac{s^2 - s\frac{\alpha_3 g_{m3}}{C_2} + \frac{\alpha_2\alpha_3 g_{m2}g_{m3}}{C_1C_2}}{s^2 + s\frac{\alpha_1\alpha_3 g_{m1}g_{m3}}{GC_2} + \frac{\alpha_2\alpha_3 g_{m2}g_{m3}}{C_1C_2}}. \tag{5.41}$$

Thus, the proposed circuit is universal and it is capable to realize all five standard filter functions simultaneously and without changing the circuit topology.

The natural angular frequency ω_0, the quality factor Q, and the bandwidth BW (ω_0/Q) of the filter can be found as:

$$\omega_0 = \sqrt{\alpha_2\alpha_3\frac{g_{m2}g_{m3}}{C_1C_2}}, \tag{5.42}$$

$$Q = \frac{G}{\alpha_1 g_{m1}}\sqrt{\frac{\alpha_2 g_{m2}C_2}{\alpha_3 g_{m3}C_1}}, \tag{5.43}$$

$$\mathrm{BW} = \frac{\omega_0}{Q} = \frac{\alpha_1\alpha_3 g_{m1}g_{m3}}{GC_2}. \tag{5.44}$$

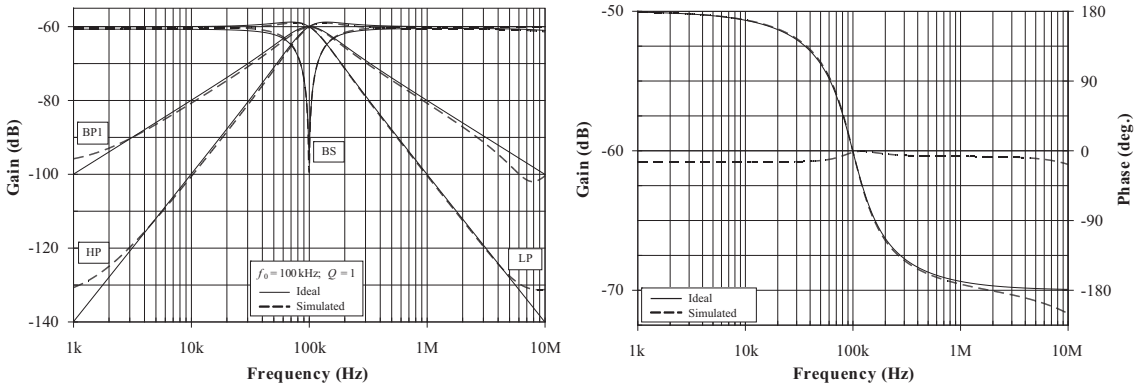
It should be noted that the parameters Q and BW can be adjusted by changing the g_{m1} of the ZC-CFTA1 without disturbing the parameter ω_0.

The relative sensitivities of the ω_0, Q and BW parameters of the designed circuit derived from (5.42)–(5.44) are:

$$\begin{gathered} S^{\omega_0}_{\alpha_2,\alpha_3,g_{m2},g_{m3}} = -S^{\omega_0}_{C_1,C_2} = \frac{1}{2}, \quad S^{\omega_0}_{\alpha_1,\gamma_1,\gamma_2,\gamma_3,g_{m1},G} = 0, \\ S^{Q}_{\alpha_2,g_{m2},C_2} = -S^{Q}_{\alpha_3,g_{m3},C_1} = \frac{1}{2}, \quad S^{Q}_{G} = -S^{Q}_{\alpha_1,g_{m1}} = 1, \quad S^{Q}_{\gamma_1,\gamma_2,\gamma_3} = 0, \\ S^{\mathrm{BW}}_{\alpha_1,\alpha_3,g_{m1},g_{m3}} = -S^{\mathrm{BW}}_{G,C_2} = 1, \quad S^{\mathrm{BW}}_{\alpha_2,\gamma_1,\gamma_2,\gamma_3,g_{m2},C_1} = 0. \end{gathered} \tag{5.45}$$

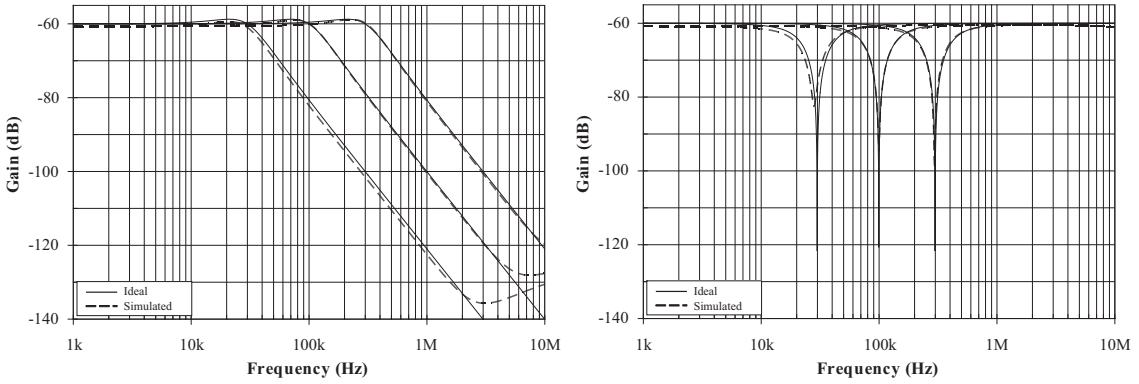
From the results it is evident that the sensitivities are low and not larger than unity of absolute value. The value of the angular frequency may be altered slightly by effects of current tracking errors of ZC-CFTA1 and ZC-CFTA2. In this case, the deviations can be easily compensated by transconductances of mentioned active elements.

Using the BJT implementation of the ZC-CFTA, the proposed trans-admittance-mode KHN-equivalent filter structure has been designed for characteristic frequency $f_0 \approx 100$ kHz and the quality factor of filters $Q = 1$, and simulated in SPICE



(a) (b)

Fig. 5.10: Simulated frequency characteristics for (a) LP, BP1, HP, BS, and (b) AP responses of the circuit in Fig. 5.9



(a) (b)

Fig. 5.11: Simulation results of the (a) low-pass, (b) band-stop filter for the values of characteristic frequency $f_0 = \{30; 100; 300\}$ kHz

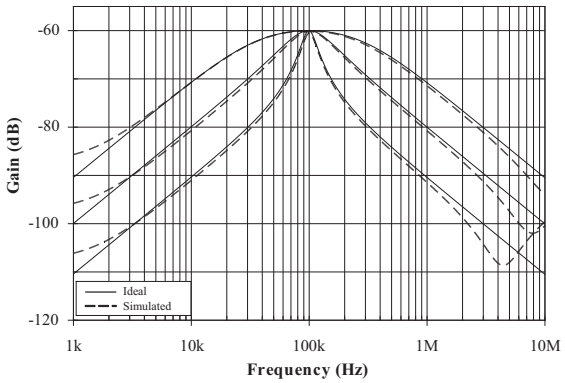


Fig. 5.12: Simulation results of proposed TA-M band-pass filter (BP1) for values of the quality factor $Q = \{0.3; 1; 3\}$

software. The following values have been chosen: $C_1 = C_2 = 1.6$ nF, $R = 1$ kΩ, and $g_{m1} = g_{m2} = g_{m3} = 1$ mA/V ($I_{B1} = I_{B2} = I_{B3} = 52$ μA). The simulation results of the low- (LP), band- (BP1), high-pass (HP), band-stop (BS), and all-pass (AP) characteristics of the filter are shown in Fig. 5.10.

The possibility of the natural frequency ω_0 control of the TA-M low-pass and band-stop filter in Fig. 5.9 is shown in Fig. 5.11(a) and Fig. 5.11(b). For required characteristic frequencies of 30, 100, and 300 kHz the external bias currents $I_{B2} = I_{B3}$ must be 15.6 μA, 52 μA, and 156 μA. The assumed quality factor is $Q = 1$.

Simulation results of the band-pass filter (BP1) are shown in Fig. 5.12. Here the possibility of adjusting the quality factor Q is demonstrated. For required values $Q = \{0.3; 1; 3\}$ the external bias current I_{B1} must be of value 15.6 μA, 52 μA, and 156 μA, respectively.

5.5 Second-order inverse VM filters using minimum passive components and DDCCs

In previous Sections various second-order filters were presented. However, inverse active filters are also important circuits in communication and control systems, wherein they are used to correct the distortion of the signal caused by signal processing or transmitting circuits [56], [131]. This correction is accomplished by using the inverse filter having the frequency response reciprocal of the frequency response of the circuit that caused the distortion. Since second-order biquadratic filters are very commonly used in communication systems, as discussed in previous Sections, in the last decade the realizations of second-order inverse active filters also received significant interest [56], [155].

The general topology for designing a second-order inverse filter is shown in Fig. 5.13 [186]. Depending on the transfer functions $T_1(s)$, $T_2(s)$, and $T_3(s)$, different realizations of inverse low-pass filter (ILPF), inverse band-pass filter (IBPF),

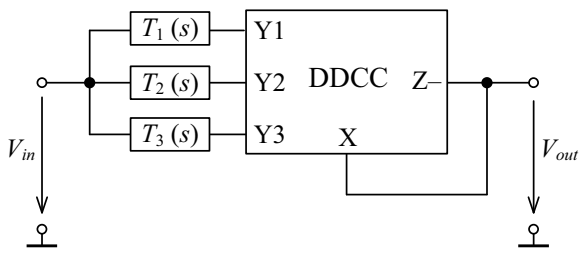


Fig. 5.13: The general circuit topology to derive second-order inverse filters

Tab. 5.1: Possible solutions of ILPF circuits

Solution	$T_1(s)$	$T_2(s)$	$T_3(s)$
A	1	$-s\tau_1$	$s^2\tau_1\tau_2$
B	1	$-s^2\tau_1\tau_2$	$s\tau_1$
C	$s\tau_1$	–1	$s^2\tau_1\tau_2$
D	$s\tau_1$	$-s^2\tau_1\tau_2$	1
E	$s^2\tau_1\tau_2$	–1	$s\tau_1$
F	$s^2\tau_1\tau_2$	$-s\tau_1$	1

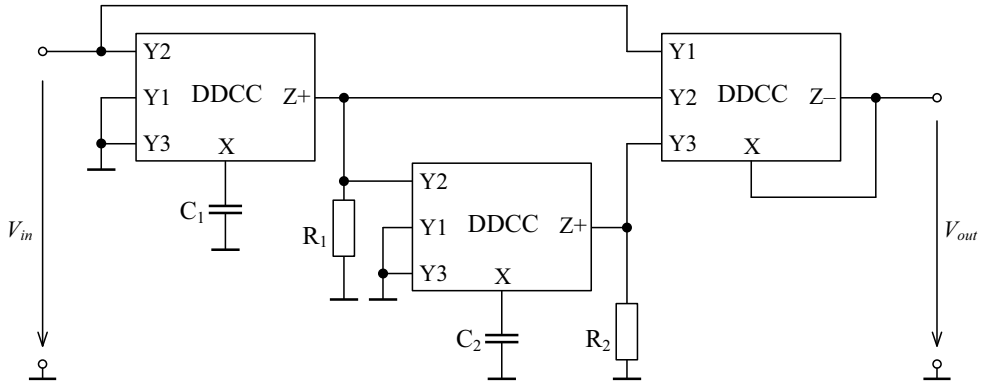


Fig. 5.14: DDCC-based implementation of ILPF solution A

and inverse high-pass filter (IHPF) are obtained. In the general topology, the DDCC [34] is used as active element. In fact, this function block can be characterized by the same hybrid matrix (3.1) as the UCC, however, it has reduced number of current outputs Z, i.e. only one Z+ or one Z– terminal is used.

Inverse low-pass filter (ILPF) design:

The general transfer function of ILPF can be written as:

$$K_{\mathrm{ILPF}} = \frac{V_{out}}{V_{in}} = 1 + s\tau_1 + s^2\tau_1\tau_2, \tag{5.46}$$

where $\tau_1 = R_1C_1$ and $\tau_2 = R_2C_2$. A total of six different ILPF circuits are evolved using different transfer functions, as listed in Tab. 5.1. As an example, the complete DDCC-based circuit for the ILPF solution A is shown in Fig. 5.14.

Inverse band-pass filter (IBPF) design:

The general transfer function of IBPF can be written as:

$$K_{\mathrm{IBPF}} = \frac{V_{out}}{V_{in}} = 1 + \frac{1}{s\tau_1} + s\tau_2. \tag{5.47}$$

Tab. 5.2: Possible solutions of IBPF circuits

Solution	$T_1(s)$	$T_2(s)$	$T_3(s)$
G	1	$-\frac{1}{s\tau_1}$	$s\tau_2$
H	1	$-s\tau_2$	$\frac{1}{s\tau_1}$
I	$\frac{1}{s\tau_1}$	–1	$s\tau_2$
J	$\frac{1}{s\tau_1}$	$-s\tau_2$	1
K	$s\tau_2$	–1	$\frac{1}{s\tau_1}$
L	$s\tau_2$	$-\frac{1}{s\tau_1}$	1

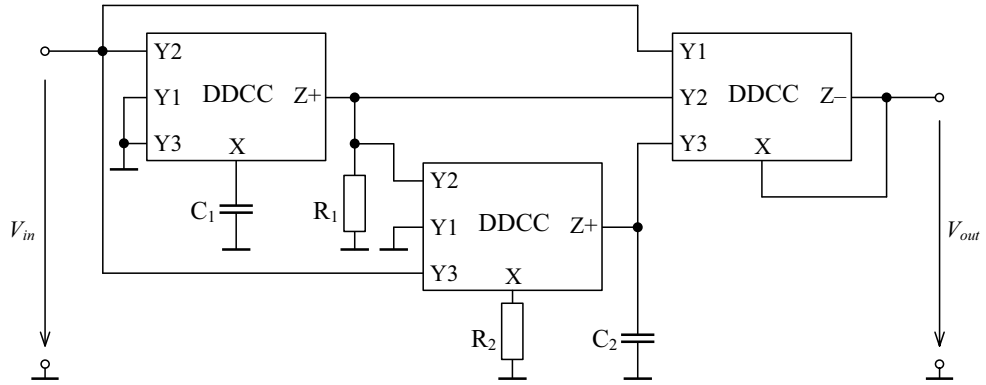


Fig. 5.15: DDCC-based implementation of IBPF solution G

Interestingly, the transfer function is analogous to that of a proportional–integral–derivative (PID) controller [56], [164]. A total of six different IBPF circuits evolved using different transfer functions are given in Tab. 5.2. As an example, the complete DDCC-based circuit for the IBPF solution G is shown in Fig. 5.15.

Inverse high-pass filter (IHPF) design:

The general transfer function of IHPF can be written as:

$$K_{\mathrm{IHPF}} = \frac{V_{out}}{V_{in}} = 1 + \frac{1}{s\tau_1} + \frac{1}{s^2\tau_1\tau_2}. \tag{5.48}$$

A total of six different IHPF circuits are evolved using different transfer functions, as tabulated in Tab. 5.3. As an example, the complete DDCC-based circuit for the IHPF solution M is shown in Fig. 5.16.

The workability of the proposed circuits in Fig. 5.14–5.16 has been verified using SPICE simulations. The DDCCs have been implemented using UCCs and in the simulations the 3rd level model [137] of the UCC-N1B 0520 integrated circuit has been used, which has been produced based on the measurement of the fabricated laboratory prototypes. For the characteristic frequency $f_0 \approx 100$ kHz and the quality

Tab. 5.3: Possible solutions of IHPF circuits

Solution	$T_1(s)$	$T_2(s)$	$T_3(s)$
M	1	$-\frac{1}{s\tau_1}$	$\frac{1}{s^2\tau_1\tau_2}$
N	1	$-\frac{1}{s^2\tau_1\tau_2}$	$\frac{1}{s\tau_1}$
O	$\frac{1}{s\tau_1}$	-1	$\frac{1}{s^2\tau_1\tau_2}$
P	$\frac{1}{s\tau_1}$	$-\frac{1}{s^2\tau_1\tau_2}$	1
Q	$\frac{1}{s^2\tau_1\tau_2}$	-1	$\frac{1}{s\tau_1}$
R	$\frac{1}{s^2\tau_1\tau_2}$	$-\frac{1}{s\tau_1}$	1

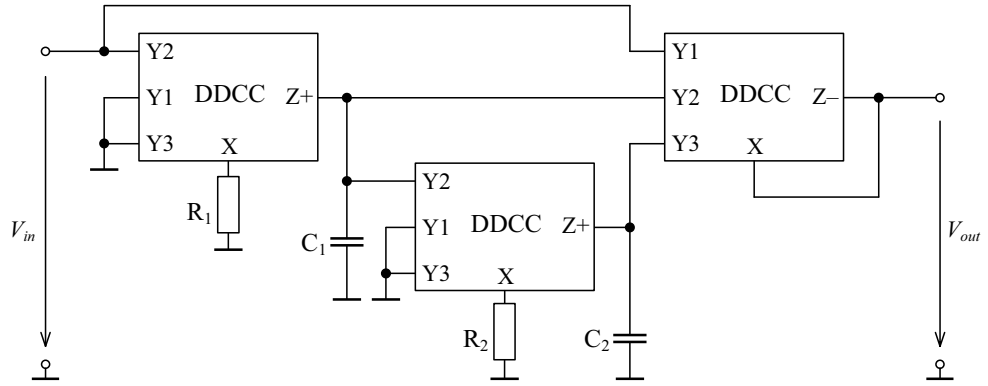


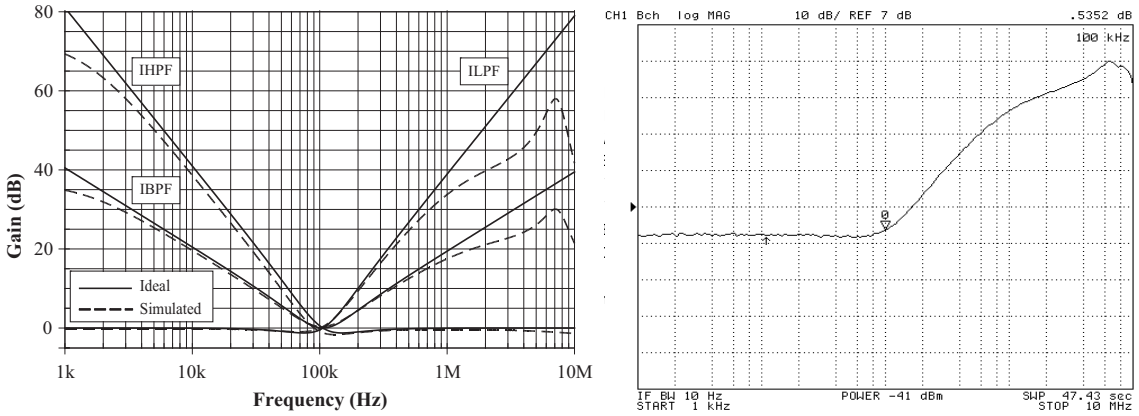
Fig. 5.16: DDCC-based implementation of IHPF solution M

factor of filter $Q = 1$ the following passive component values have been chosen: $C_1 = C_2 = 150$ pF, $R_1 = R_2 = 10$ kΩ. The ideal and simulated responses of the inverse low-, inverse band-, and inverse high-pass filters are shown in Fig. 5.17(a). From the simulation results it is evident that the final solutions correspond to the theory.

In order to confirm the above given theoretical analysis, the behavior of the proposed inverse low-pass filter from Fig. 5.14 has also been verified by experimental measurements using the fabricated UCC-N1B 0520 chips. In the measurements the network analyzer Agilent 4395A has been used and the results are shown in Fig. 5.17(b). The stability of the proposed ILPF is proved by transient analysis. The responses of the ILPF to an input voltage with the 250 mV amplitude at frequency 100 kHz are given in Fig. 5.18. The real behavior largely agrees with the simulations and, hence, is very satisfactory.

5.6 Sub-conclusion

In this Chapter one current-mode, three voltage-mode universal filter structures, one dual-mode KHN-equivalent structure, and one VM general circuit topology to



(a) (b)

Fig. 5.17: (a) Ideal and simulated magnitude responses of the ILPF, IBPF, IHPF from Fig. 5.14–5.16, (b) measurement results of the ILPF from Fig. 5.14

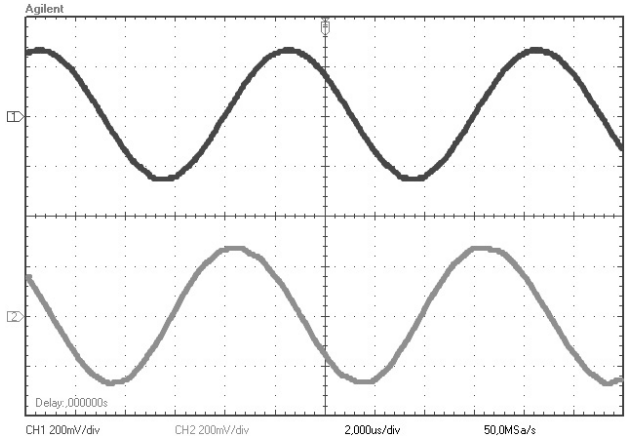


Fig. 5.18: Transient analysis: input (black) and output (gray) waveforms of the ILPF from Fig. 5.14

derive second-order inverse filters are presented. The comparison of the proposed circuits is given in Tab. B.2.

The first presented circuit employing single CCCFTA is shown in Fig. 5.1 [182]. Due to external features (R_f and g_m) of used active element, the proposed CM universal filter is resistorless. Proposed circuit is equivalent to the presented ones in [79], but it uses only single ABB.

In the next Section 7.2, the application possibilities of the novel versatile active function block for analogue signal processing, namely the differential-input buffered and transconductance amplifier (DBTA), have been demonstrated in voltage-mode universal filter design [180]. The circuit requires minimal number of active and passive elements with no conditions for component matching.

The versatility of the MCFOA has already been earlier demonstrated [159], however, to realize VM universal filter one of the input voltages have to be inverted. This weakness is eliminated in here presented circuits. The proposed VM universal filters in Fig. 5.7 also require minimal number of active and passive elements [174].

The presented novel mixed-mode KHN-equivalent filter in the Section 7.4 [179] enjoys the following advantages: it provides simultaneously all standard filter functions, uses only grounded capacitors, it allows control of the quality factor Q without disturbing the parameter ω_0 of the filter, and it has low active and passive sensitivities.

Inverse active filters are also important circuits in communication and control systems. In the more recent publication on inverse filters [56], authors use excessive number of passive components including floating ones. The Section 7.5 attempts this problem by providing realizations of ILPF, IBPF, and IHPF [186] using three DDCCs [34], two resistors, and two capacitors, where all are in grounded form.

From simulation and measurement results it is evident that the final solutions correspond to theoretical expectations.

6 APPLICATIONS ON GROUNDED INDUCTANCE SIMULATORS

Conventional spiral inductors are too big, too heavy, too costly, and they require tuning. Due to these disadvantages, active element-based inductor design is very desirable to designers today. The positive inductance simulators (PIS) can be used in many applications such as active filter design, oscillator design, analog phase shifters and cancellation of parasitic element [70]. Not only the PIS, but also a negative inductance simulator (NIS) plays an importance role in cancellation/compensation of parasitic inductances. Actively simulated NISs also find in several applications such as in microwave circuits for impedance matching, in chaotic oscillations, in antenna to minimize reflection at the input so that it provides a better radiation pattern, to compensate bond wire inductance which is an increasing problem in high-speed/low-power integrated circuits because of reduced noise margin and cancellation of undesired inductance. It is well known that, unlike capacitance, the magnitude of the negative inductance increases with frequency in the same way as for positive inductances. However, a negative inductance provides a negative 90° phase like a capacitor [80].

During the last few decades, various grounded inductors have been created using different high-performance active building blocks. In this Chapter two resistorless active-C PIS are introduced.

6.1 Active-C grounded positive inductance simulator based on CFTAs

The first realization of grounded PIS employs two CFTAs and grounded capacitor, as it is shown in Fig. 6.1 [176]. Based on the behavior description (3.10) (i.e. $a = 1$, $b_1 = 1$, and $b_2 = -1$) of the active elements used, routine circuit analysis yields the following input impedance for the circuit:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sC_L}{g_{m1}g_{m2}}. \tag{6.1}$$

From Eq. (6.1) it is obvious that the circuit shown in Fig. 6.1 performs a grounded inductance with a value:

$$L_{eq} = \frac{C_L}{g_{m1}g_{m2}}. \tag{6.2}$$

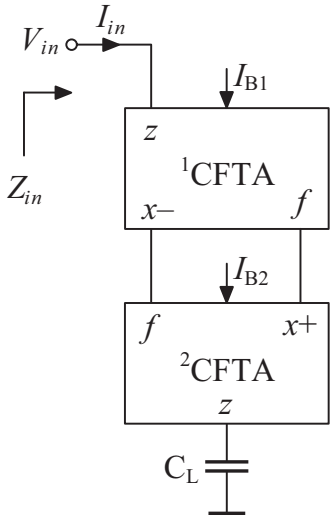


Fig. 6.1: Proposed grounded positive inductance simulator employing two CFTAs and grounded capacitor

It is clearly seen that, the positive inductance value L_{eq} can be adjusted electronically by either I_{B1} or I_{B2}.

6.2 Active-C grounded positive and negative inductor simulators in compact form

In previous Section, the proposed grounded PIS employs two CFTAs, however, the use of two active elements is not that economical. Therefore, the proposed PIS and NIS in this Section (Fig. 6.2) use canonic number of passive and active elements (i.e. single grounded capacitor, single ZC-CCCITA). Using (3.14) and doing routine

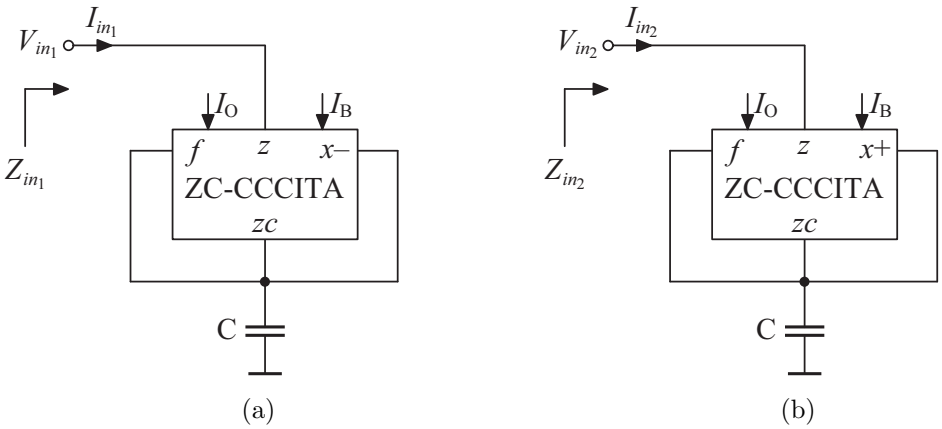


Fig. 6.2: Proposed grounded (a) positive and (b) negative inductance simulators

circuit analysis yields the following input impedances for both the circuits:

$$Z_{in_1} = -Z_{in_2} = sL_{eq} = \frac{sCR_f}{g_m} = \frac{sCV_{\mathrm{T}}^2}{I_{\mathrm{O}}I_{\mathrm{B}}}. \tag{6.3}$$

From (6.3) it is obvious that circuits in Fig. 6.2 represent lossless positive and negative inductor simulators, respectively. In both circuits it can be also clearly seen that the inductance value L_{eq} can be adjusted electronically by either I_{O} and/or I_{B} currents.

Here, the non-ideal analysis will only focus on the grounded PIS circuit (i.e. Fig. 6.2(a)). It is sufficient since in case of the NIS it involves only sign change. Hence, taking into account the non-idealities of the ZC-CCCITA, except for the parasitics R_z and C_z, the input impedance of the circuit from Fig. 6.2(a) is given as:

$$\begin{aligned} Z'_{in_1} &= R_{lossy} + sL_{eq} = \\ &= \frac{1-\beta_2}{\beta_1 g_m} + \frac{R_f}{\beta_1 g_m (R_{zc}||R_x)} + \frac{s(C+C_{zc}+C_x)R_f}{\beta_1 g_m} = \\ &= \frac{2V_{\mathrm{T}}(1-\beta_2)}{I_{\mathrm{B}}\beta_1} + \frac{V_{\mathrm{T}}^2}{I_{\mathrm{O}}I_{\mathrm{B}}\beta_1(R_{zc}||R_x)} + \frac{V_{\mathrm{T}}^2 s(C+C_{zc}+C_x)}{I_{\mathrm{O}}I_{\mathrm{B}}\beta_1}. \end{aligned} \tag{6.4}$$

This equation clearly indicates that there is a lossy term (resistance) in the simulated impedance and thus the quality factor of the inductor is not infinite. To increase the quality factor of the simulated inductor, the lossy term needs to be minimized and this can be achieved by:

(i) making the β_2 very close to unity (by using high-output resistance current mirrors) and,

(ii) choosing $R_f \ll R_{zc}||R_x$.

Assuming now the lossy term being minimized, the input impedance Z'_{in_1} approximates to the inductance of value $L_{eq} = \frac{(C+C_{zc}+C_x)R_f}{\beta_1 g_m}$. In practice, the external capacitor is chosen such that $C \gg C_{zc} + C_x$.

Till now, we have neglected the effects of parasitics R_z and C_z. Taking into account them we get the input admittance as:

$$Y_{in_1} = \frac{1}{R_z} + sC_z + \frac{1}{sL_{eq}}. \tag{6.5}$$

Assuming the operating frequency $\omega_0 \ll min\left(\frac{R_z}{L_{eq}}, \sqrt{\frac{1}{C_z L_{eq}}}\right)$, the upper frequency potential of the circuit is limited, but the effects of the parasitics on the simulated inductance can be reduced.

To illustrate an application of the proposed grounded PIS using ZC-CCCITA, it is used in an fourth-order high-pass filter (HPF) realization [84]. The passive RLC

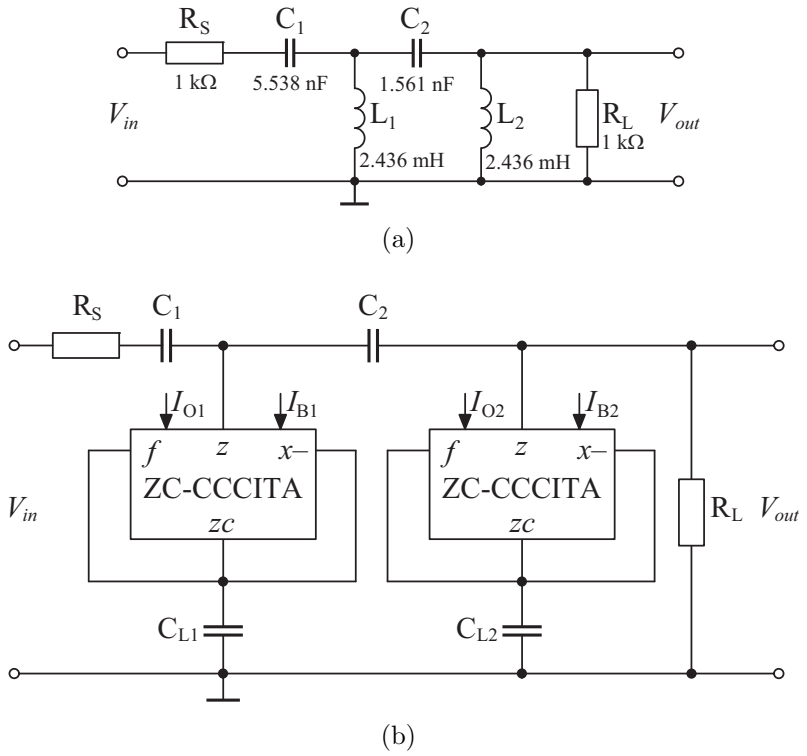


Fig. 6.3: (a) Fourth-order high-pass prototype with Butterworth response and (b) the transformed equivalent circuit diagram

prototype is shown in Fig. 6.3(a), which transfer function is given by:

$$K_{\mathrm{HPF}}(s) = \frac{V_{out}}{V_{in}} = \frac{s^4}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}, \tag{6.6}$$

where

$$\begin{aligned} a_4 &= 1 + \frac{R_S}{R_L}, \\ a_3 &= \frac{R_S}{L_1} + \frac{R_S}{L_2} + \frac{1}{C_1 R_L} + \frac{1}{C_2 R_L}, \\ a_2 &= \frac{1}{L_1 C_1} + \frac{1}{L_2 C_1} + \frac{1}{L_2 C_2}, \\ a_1 &= \frac{1}{L_1 C_1 R_L C_2} + \frac{R_S}{L_1 L_2 C_2}, \\ a_0 &= \frac{1}{L_1 L_2 C_1 C_2}. \end{aligned} \tag{6.7}$$

The transformed equivalent active circuit using the proposed grounded PIS is shown in Fig. 6.3(b). Here the L_1 and L_2 are $\frac{C_{L1} V_{\mathrm{T}}^2}{I_{\mathrm{O1}} I_{\mathrm{B1}}}$ and $\frac{C_{L2} V_{\mathrm{T}}^2}{I_{\mathrm{O2}} I_{\mathrm{B2}}}$, respectively.

As a second application of the proposed grounded PIS using ZC-CCCITA, the parallel resonant circuit in Fig. 6.4(a) is given [162]. The transformed equivalent

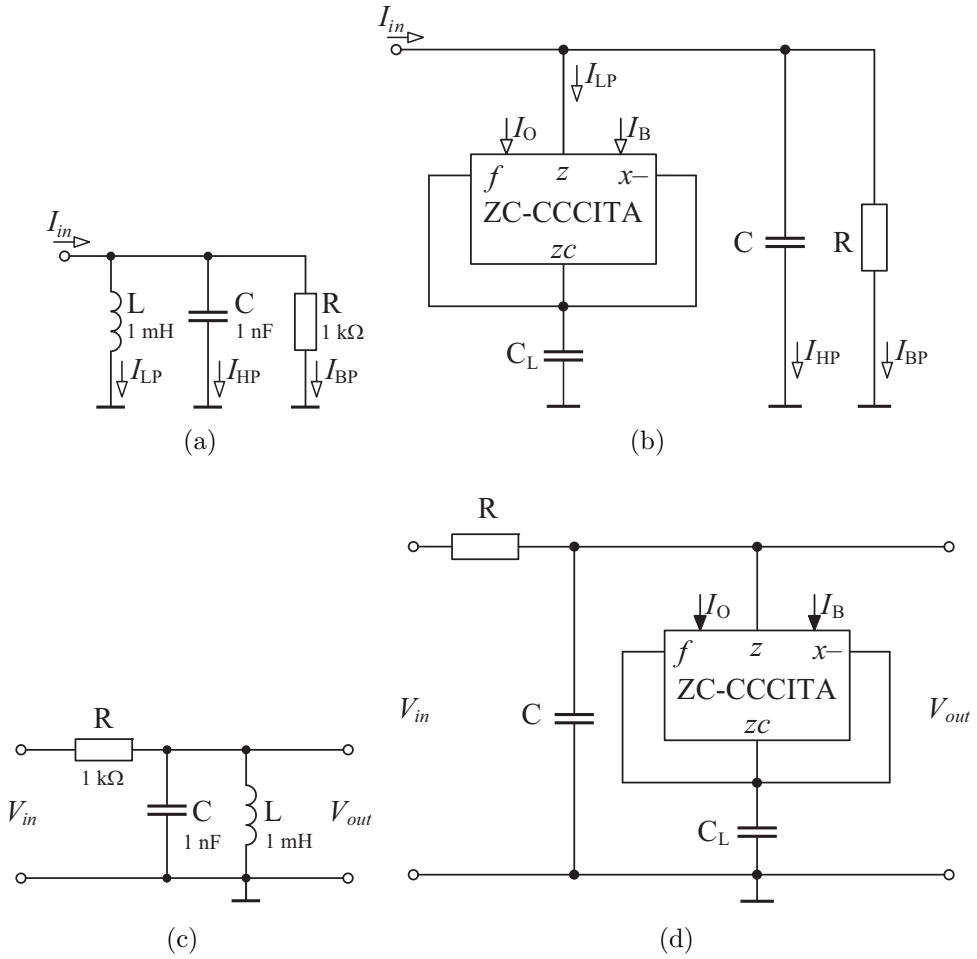


Fig. 6.4: (a) Second-order parallel resonant circuit and (b) its transformed equivalent current-mode multifunction filter, (c) second-order band-pass prototype and (d) its transformed equivalent circuit diagram

current-mode multifunction filter is shown in Fig. 6.4(b). The current transfer functions of the LP, HP, and BP filter responses are calculated as:

$$K_{\mathrm{LPF}}(s) = \frac{I_{LP}}{I_{in}} = \frac{\frac{1}{CL}}{s^2 + s\frac{1}{CR} + \frac{1}{CL}} = \frac{\frac{I_{\mathrm{O}}I_{\mathrm{B}}}{CC_LV_{\mathrm{T}}^2}}{s^2 + s\frac{1}{CR} + \frac{I_{\mathrm{O}}I_{\mathrm{B}}}{CC_LV_{\mathrm{T}}^2}}, \tag{6.8}$$

$$K_{\mathrm{HPF}}(s) = \frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2 + s\frac{1}{CR} + \frac{1}{CL}} = \frac{s^2}{s^2 + s\frac{1}{CR} + \frac{I_{\mathrm{O}}I_{\mathrm{B}}}{CC_LV_{\mathrm{T}}^2}}, \tag{6.9}$$

$$K_{\mathrm{BPF}}(s) = \frac{I_{BP}}{I_{in}} = \frac{s\frac{1}{CR}}{s^2 + s\frac{1}{CR} + \frac{1}{CL}} = \frac{s\frac{1}{CR}}{s^2 + s\frac{1}{CR} + \frac{I_{\mathrm{O}}I_{\mathrm{B}}}{CC_LV_{\mathrm{T}}^2}}. \tag{6.10}$$

The second-order parallel resonant circuit in Fig. 6.4(a) has also been transformed to second-order VM band-pass filter (BPF). The passive RLC BPF is shown in Fig. 6.4(c) [116] and the appropriate active circuit using the proposed grounded

PIS is shown in Fig. 6.4(d). Routine circuit analysis yields the following voltage transfer function of the BPF:

$$K_{\mathrm{BPF}}(s) = \frac{V_{out}}{V_{in}} = \frac{s\frac{1}{CR}}{s^2 + s\frac{1}{CR} + \frac{1}{CL}} = \frac{s\frac{1}{CR}}{s^2 + s\frac{1}{CR} + \frac{I_{\mathrm{O}}I_{\mathrm{B}}}{CC_LV_{\mathrm{T}}^2}}. \tag{6.11}$$

The denominator of circuits in Fig. 6.4 is identically same, therefore, the natural angular frequency ω_0, the quality factor Q, and the bandwidth BW (ω_0/Q) can be found as:

$$\omega_0 = \frac{1}{V_{\mathrm{T}}}\sqrt{\frac{I_{\mathrm{O}}I_{\mathrm{B}}}{CC_L}}, \quad Q = \frac{R}{V_{\mathrm{T}}}\sqrt{\frac{I_{\mathrm{O}}I_{\mathrm{B}}C}{C_L}}, \quad BW = \frac{1}{CR}. \tag{6.12}$$

The active and passive sensitivities of the filter parameters are following:

$$S^{\omega_0}_{I_{\mathrm{O}},I_{\mathrm{B}}} = -S^{\omega_0}_{C,C_L} = \frac{1}{2},\ S^{\omega_0}_{V_{\mathrm{T}}} = -1,\ S^{\omega_0}_{R} = 0, \tag{6.13}$$

$$S^{Q}_{I_{\mathrm{O}},I_{\mathrm{B}},C} = -S^{Q}_{C_L} = \frac{1}{2},\ S^{Q}_{R} = -S^{Q}_{V_{\mathrm{T}}} = 1, \tag{6.14}$$

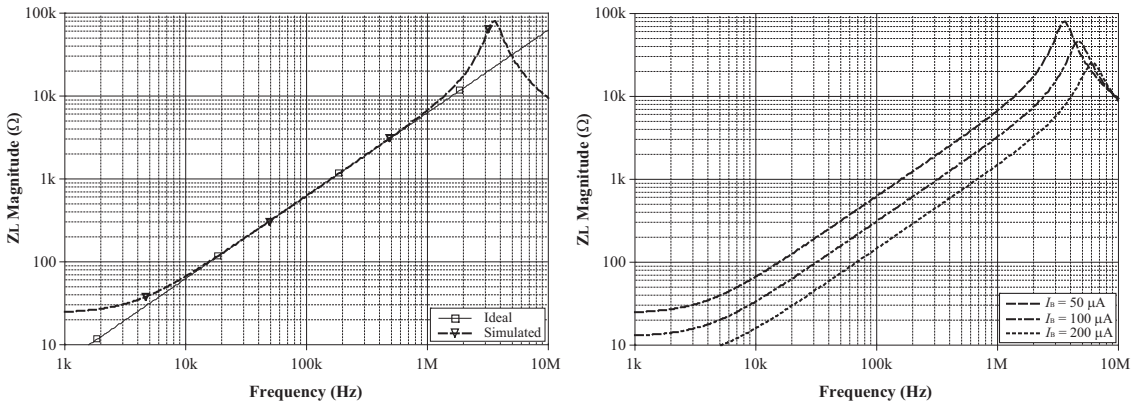
$$S^{BW}_{C,R} = -1,\ S^{BW}_{I_{\mathrm{O}},I_{\mathrm{B}},V_{\mathrm{T}},C_L} = 0, \tag{6.15}$$

that are all not more than unity in magnitude.

To verify the theoretical analyses, the proposed grounded PIS in Fig. 6.2(a) and filter examples in Fig. 6.3(b), Fig. 6.4(b), and Fig. 6.4(d) have been simulated using SPICE. The bipolar implementation of the ZC-CCCITA is shown in Fig. 3.23. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1.

The ideal and simulated impedances of the grounded PIS are shown in Fig. 6.5(a). The inductor simulator is realized with the following active parameters and passive element values: $g_m = 1$ mA/V ($I_{\mathrm{B}} = 52\,\mu$A), $R_f = 1$ kΩ ($I_{\mathrm{O}} = 13\,\mu$A), and $C = 1$ nF to obtain $L = 1$ mH. Due to parasitic elements restricting the performances of the proposed circuits at the higher frequencies the usable frequency ranges can be up to 1 MHz. Fig. 6.5(b) shows impedance values relative to frequency with different I_{B}. It confirms that the simulated inductance can be adjusted by input bias current of the ZC-CCCITA.

To design the fourth-order high-pass filter for a cut-off frequency of $f_0 = 50$ kHz with a Butterworth approximation, the normalized design ($f_0 = 1$ Hz) was obtained with the following component values: $R_{\mathrm{S}} = R_{\mathrm{L}} = 1\ \Omega$, $L_1 = L_2 = 0.1217$ H, $C_1 = 0.2768$ F, and $C_2 = 0.0780$ F. To get the required cut-off frequency, appropriate frequency scaling has been performed. The resulting values of the components have been found to be as shown in Fig. 6.3(a) [84]. The derived equivalent fil-



(a) (b)

Fig. 6.5: (a) Ideal and simulated impedance values of the grounded PIS relative to frequency for $L = 1$ mH, (b) simulated impedance values of the grounded PIS relative to frequency for different I_{B}

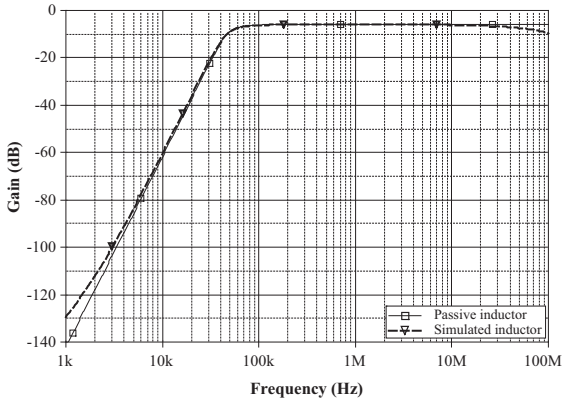


Fig. 6.6: Ideal and simulated gain responses of the fourth-order HPF

ter in Fig. 6.3(b) has been designed by using two simulated inductors with values $L_1 = L_2 = 2.436$ mH ($g_{m1} = g_{m2} = 1$ mA/V ($I_{\mathrm{B1}} = I_{\mathrm{B2}} = 52$ μA), $R_{f1} = R_{f2} = 1$ kΩ ($I_{\mathrm{O1}} = I_{\mathrm{O2}} = 13$ μA), and $C_{L1} = C_{L2} = 2.436$ nF). Fig. 6.6 compares the gain response of the simulated high-pass filter with passive inductor and simulated inductor.

The second-order current-mode multifunction filter and voltage-mode band-pass filter from Fig. 6.4(b) and Fig. 6.4(d), respectively, have been simulated for the characteristic frequency $f_0 = \omega_0/2\pi \cong 159.15$ kHz and the quality factor $Q = 1$. The passive component values are shown in Fig. 6.4(a) and Fig. 6.4(c), respectively. The inductor simulator is realized with the following active parameters and passive element values: $g_m = 1$ mA/V ($I_{\mathrm{B}} = 52$ μA), $R_f = 1$ kΩ ($I_{\mathrm{O}} = 13$ μA), and $C_L = 1$ nF to obtain the required $L = 1$ mH. Ideal and simulated gain responses of the second-order CM multifunction filter and VM BPF are shown in Fig. 6.7(a)

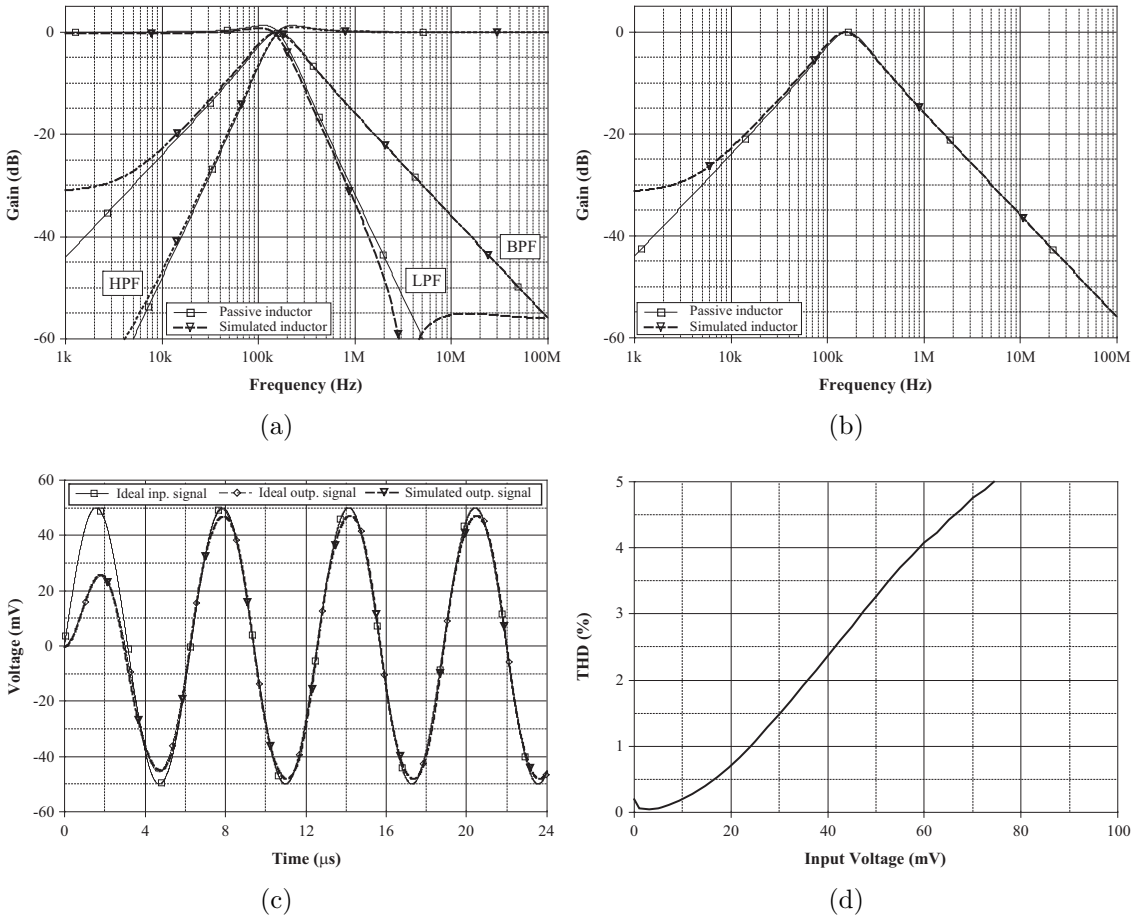


Fig. 6.7: Ideal and simulated gain responses of the (a) second-order CM multifunction filter and (b) VM BPF, (c) time-domain responses of the proposed second-order BPF at 159.15 kHz, (d) THD of the proposed second-order BPF at 159.15 kHz

and Fig. 6.7(b), respectively. Additionly, transient simulation result of the filter is shown in Fig. 6.7(c) in which a sinusoidal input voltage signal with 50 mV peak value at 159.15 kHz is applied to the filter. In order to investigate distortion of the proposed BPF, the THD at 159.15 kHz has been simulated and the results are shown in Fig. 6.7(d).

The SPICE simulations confirm the feasibility of the proposed PIS and results are in good agreement with theory.

6.3 Sub-conclusion

As it was mentioned above, during the last few decades, various grounded inductance simulators have been created using different ABBs, such as CCIIs [27], [124], [156], modified inverting CCII (MICCII) [161], gain-variable third-generation CC

(GVCCIII) [162], FDCCII [74], CFOA [89], [157], which is commercially available as the AD844 integrated circuit by Analog Devices, or positive four terminal floating nullor (PFTFN) [84]. Comparison of here proposed PIS with the technical literature ones is given in Tab. B.3. Both proposed configurations in [156] are derived from the inductor simulators of [27] and [124] and both employ grounded capacitor and three plus-type CCIIs. Hence, they can be easily implemented by the AD844 ICs. In [74], [161], [162], other types of CCs are used to realize grounded inductors. In [157], four new grounded inductor simulators are described using single CFOA and three passive elements. In another CFOA-based grounded inductor simulator [89] the intrinsic capacitance of the AD844 is used instead of external capacitor. The PFTFN-based inductor [84] requires component matching constraint. Inductor simulators in [84], [157], [161], and [162] are realized with floating capacitor, however, the use of grounded capacitor is very important, because it is easy to fabricate in a fully integrated circuit technology [20]. Moreover, all above mentioned circuits employ external resistors. Therefore, the aim of this Section was to introduce such grounded PISs, which employ only active elements and single grounded capacitor.

7 QUADRATURE SINUSOIDAL OSCILLATORS

The quadrature oscillator (QO) is a circuit that provides two sinusoids with 90° phase difference. Such circuit is frequently used in various applications, i.e. in telecommunications for quadrature mixers and single-sideband generators, for measurement purposes in vector generators or selective voltmeters. Therefore, quadrature oscillators represent an important unit in many communication, control systems, signal processing, instrumentation and measurement systems [5], [60], [81], [125]. This Chapter presents five quadrature oscillators using various active elements such as CCCFTAs, PCAs, CFOAs, GCFTA and UGVF (unity-gain voltage follower), and DBTA.

7.1 Current-mode resistorless oscillator using CCCFTAs

The first proposed CM quadrature oscillator presented in [182] has been designed by expanding the CM filter in Fig. 5.1 via CCCFTA-based negative resistor. Assuming ideal CCCFTAs ($\alpha_i = 1$, where $i = 1, 2$), for the proposed CM quadrature oscillator in Fig. 7.1 routine analysis yields the following characteristic equation (CE):

$$\text{CE:} \quad s^2 C_1 C_2 R_{f1} + sC_2(1 - R_{f1} g_{m2}) + g_{m1} = 0. \tag{7.1}$$

From (7.1), the condition of oscillation (CO) and the frequency of oscillation (FO) are:

$$\text{CO:} \quad g_{m2} \geq 1/R_{f1}, \tag{7.2}$$

$$\text{FO:} \quad f_0 = \frac{1}{2\pi}\sqrt{\frac{g_{m1}}{R_{f1} C_1 C_2}}. \tag{7.3}$$

From (7.2) and (7.3) it is clear that the CO can be controlled independently of FO by means varying of the transconductance g_{m2} and the FO can be controlled

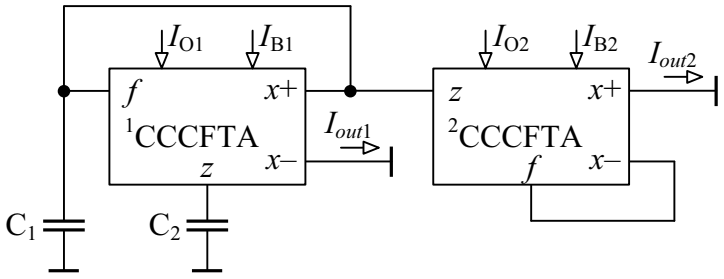


Fig. 7.1: Proposed CM quadrature oscillator employing CCCFTAs

by adjusting the transconductance g_{m1}, respectively. Thus, the proposed oscillator provides independent control of the CO and the FO. The two marked explicit quadrature current outputs in Fig. 7.1 are related as:

$$\frac{I_{out2}}{I_{out1}} = \frac{g_{m1}}{sC_2R_{f1}g_{m2}}, \tag{7.4}$$

where the phase difference is $\phi = 90°$, ensuring the current I_{out1} and I_{out2} to be quadrature.

Taking into account the non-idealities of the CCCFTAs, the CE from (7.1) modifies as follows:

$$\text{CE:} \quad s^2C_1C_2R_{f1} + sC_2(1 - \alpha_2R_{f1}g_{m2}) + \alpha_1g_{m1} = 0. \tag{7.5}$$

In this case, the modified CO and FO can be expressed as:

$$\text{CO:} \quad \alpha_2g_{m2} \geq 1/R_{f1}, \tag{7.6}$$

$$\text{FO:} \quad f_0 = \frac{1}{2\pi}\sqrt{\frac{\alpha_1g_{m1}}{R_{f1}C_1C_2}}. \tag{7.7}$$

It should be noted from (7.6) and (7.7) that the CO and FO of the proposed quadrature oscillator are slightly affected by non-idealities of CCCFTAs. However, they can still be controlled independently.

The active and passive sensitivities of the quadrature oscillator parameters are:

$$S^{f_0}_{\alpha_1,g_{m1}} = -S^{f_0}_{C_1,C_2,R_{f1}} = \frac{1}{2}, \qquad S^{f_0}_{\alpha_2,g_{m2},R_{f2}} = 0. \tag{7.8}$$

From Eq. (7.8) it is evident that the sensitivities are low and again not higher than 0.5 in absolute value.

In order to confirm the above given theoretical analysis of the proposed quadrature oscillator in 7.1, it has been simulated using SPICE. In the simulations the CMOS implementation of the CCCFTA has been used, which is based on the CCCII with grounded y-terminal [150] and BOTA [150]. The simulations have been performed based on the MOSIS 0.5 μm CMOS technology parameters and it was designed with the oscillation frequency of $f_0 = \omega_0/2\pi \cong 1$ MHz. For more details regarding the simulation results, refer [182]. From the simulation results the oscillation frequency of $f_0 \cong 996$ kHz is obtained, which agrees very well with the theory as expected. The THD at both the outputs are less than 5%. The SPICE simulations confirm the feasibility of both proposed circuits and results are in good agreement with theory.

7.2 PCA-based 2C-2R class CM oscillator

It is well known that any active RC sinusoidal oscillator providing independent control of the CO and the FO, requires the use of at least three resistors and two capacitors [58]. This class of 3R-2C "single-resistance-controlled oscillators" (SRCOs) has been extensively researched and a large group of its realizations is available in the literature. On the contrary, the proposed oscillator circuit in [189] requires a bare minimum of two resistors and two capacitors (thereby reducing the passive component count by one). The circuit offers independently tunable CO and the FO by means of the PCA current gains and is capable of simultaneously providing two explicit quadrature current outputs. This feature of the circuit makes it suitable to be used as CM quadrature oscillator.

The proposed CM electronically tunable quadrature oscillator (ETQO) using only three PCAs, two resistors and two capacitors is shown in Fig. 7.2. Using (3.7) and doing routine circuit analysis yields the following characteristic equation:

$$\text{CE:} \quad s^2C_1C_2R_1R_2 + s[C_1R_2(1-n_1) + C_2R_1 - n_1n_3C_1R_2] + 1 + n_1n_2 - n_1 = 0. \quad (7.9)$$

For the start-up of oscillation the roots of the CE should be in the right-hand plane and which indicates that the coefficient of 's' term in (7.9) should be negative. Thus the CO and the FO are given as:

$$\text{CO:} \quad C_1R_2(1-n_1) + C_2R_1 \leq n_1n_3C_1R_2, \quad (7.10)$$

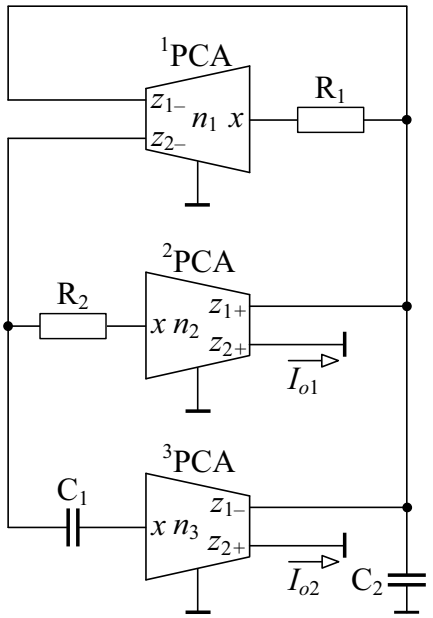


Fig. 7.2: The proposed current-mode electronically tunable quadrature oscillator

$$\text{FO:} \quad f_o = \frac{1}{2\pi}\sqrt{\frac{1+n_1(n_2-1)}{C_1C_2R_1R_2}}. \tag{7.11}$$

It is evident from (7.10) and (7.11) that the CO and FO are independently tunable by means of the mu-factors n_3 and n_2, respectively. For the specific case when $n_1 = 1$ (i.e. PCA is reduced to simply an inverting current follower) the CO and FO in (7.10) and (7.11) can be rewritten as:

$$\text{CO:} \quad C_2R_1 \leq n_3C_1R_2, \tag{7.12}$$

$$\text{FO:} \quad f_0 = \frac{1}{2\pi}\sqrt{\frac{n_2}{C_1C_2R_1R_2}}. \tag{7.13}$$

The two marked explicit current outputs (ECOs) in Fig. 7.2 are related as:

$$|I_{o2}| = jk|I_{o1}|, \tag{7.14}$$

where

$$k = \frac{\omega_0 n_3 C_1 R_2}{n_2}. \tag{7.15}$$

It is evident from (7.14) and (7.15) that the ECOs are ideally 90° phase shifted and have equal amplitudes for $k = 1$.

For a complete analysis of the circuit, it is important to take into account important PCA non-idealities that affect the oscillator behavior.

- The non-ideal PCA suffers from current tracking errors between the input and output currents. Let β_{ij} represent the current transfer gains from the input terminal to j^{th} output terminal (either $z+$ or $z-$ terminal) of the i^{th} PCA, respectively. Ideally these values are unity, but they differ slightly from unity ($\beta_{ij} = 1 - \varepsilon_{ij}$) by small current tracking errors ε_{ij} ($|\varepsilon_{ij}| \ll 1$). Considering these non-idealities the expressions in (7.10) and (7.11) modify to:

$$\text{CO:} \quad C_1R_2(1 - n_1\beta_{11-}) + C_2R_1 \leq n_1n_3\beta_{12-}\beta_{31-}C_1R_2, \tag{7.16}$$

$$\text{FO:} \quad f_0 = \frac{1}{2\pi}\sqrt{\frac{1+n_1(n_2\beta_{12-}\beta_{21+} - \beta_{11-})}{C_1C_2R_1R_2}}. \tag{7.17}$$

  Use of cascode mirrors (as in our scheme) reduces the current tracking errors associated with current following. The passive f_0 sensitivities using (7.17) are:

$$|S^{f_0}_{C_1,C_2,R_1,R_2}| = \frac{1}{2}, \tag{7.18}$$

  which indicates a satisfactory sensitivity performance. The active f_0 sensitiv-

ities with respect to n_1, n_2, β_{12-}, β_{21+}, and β_{11-} are also less than unity in magnitudes.

- Another non-ideality that should be considered is the non-zero input parasitic resistance of the PCA, denoted by R_x. This parasitic resistance is absorbed in the external impedance connected at the input of the PCA, if it is of resistive nature. However, if the external impedance is a capacitor then the presence of the parasitic resistance would change the character of the impedance, which should be purely capacitive in nature. Considering Fig. 7.2, it is evident that the parasitic resistances at ^{1}PCA and ^{2}PCA are absorbed in the external resistors R_1 and R_2, respectively. For ^{3}PCA, the effect discussed in [45] can be alleviated by considering the operating frequency $\omega_0 < 1/C_1R_{x3}$. The parasitic resistance R_x associated with the low input impedance x terminal can be reduced by increasing the value of bias current $I_{\rm O}$.
- The parasitic resistance $R_{z_{ij}}$ and parasitic capacitance $C_{z_{ij}}$ appear between the high output impedance z_j (where $j = 1, 2$) of the i^{th} PCA and ground. The parasitic capacitance $C_{z_{21+}}$ and $C_{z_{31-}}$ are absorbed into external capacitor C_2 as they appear in shunt with it. Considering that the input terminals of PCA are at virtual ground (i.e. considering $R_x \rightarrow 0$), then the parasitic resistance $R_{z_{12-}}$ and capacitance $C_{z_{12-}}$ appear in parallel with external resistor R_2 and capacitor C_1, respectively. The effects of these parasitics can be alleviated by considering external capacitors $C_1, C_2 \gg C_{z_{ij}}$, external resistor $R_2 \ll R_{z_{12-}}$ and the operating frequency $\omega_0 > 1/C_2(R_{z_{21+}}||R_{z_{31-}})$.

Considering the aforementioned non-idealities, the quadrature relation between the two marked ECOs in Fig. 7.2 is slightly modified to:

$$I_{o2}(s) = \frac{s\beta_{23}n_3C_1(R_2 + R_{x2})}{\beta_{22}n_2(1 + sC_1R_{x3})}I_{o1}(s). \tag{7.19}$$

Using reasonable assumptions that the operating frequency $\omega_0 \ll 1/C_1R_{x3}$ and the external resistor $R_2 \gg R_{x2}$, (7.19) approximates to the a similar equation as in (7.14):

$$I_{o2}(s) = \frac{s\beta_{23}n_3C_1R_2}{\beta_{22}n_2}I_{o1}(s). \tag{7.20}$$

To verify the theoretical study, the proposed CM ETQO in Fig. 7.2 has been verified by SPICE simulations. In the simulations the BJT implementation of the PCA (Fig. 3.13) have been used. The proposed circuit was designed using the following passive and active component values: $C_1 = C_2 = 1$ nF, $R_1 = R_2 = 1$ kΩ, and $n_1 = n_2 = 1$, where the value of the mu-factor n_3 of the ^{3}PCA was chosen as $n_3 = 1.45$ to start the oscillations. In this case the external DC bias current I_1 of ^{3}PCA was set as 145 μA when I_2 was set to be constant as 100 μA. This yields

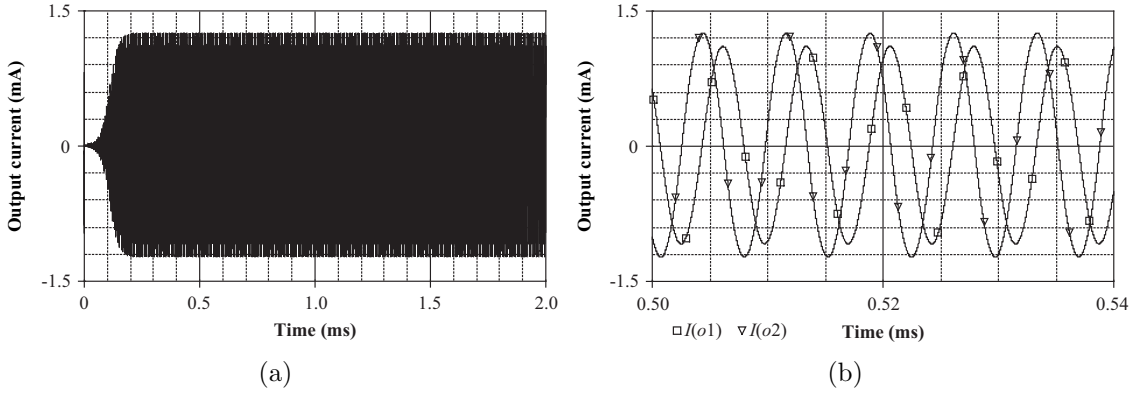


Fig. 7.3: Simulated output waveforms I_{o1} and I_{o2} of the proposed oscillator in Fig. 7.2: (a) at transient stage and (b) at steady stage

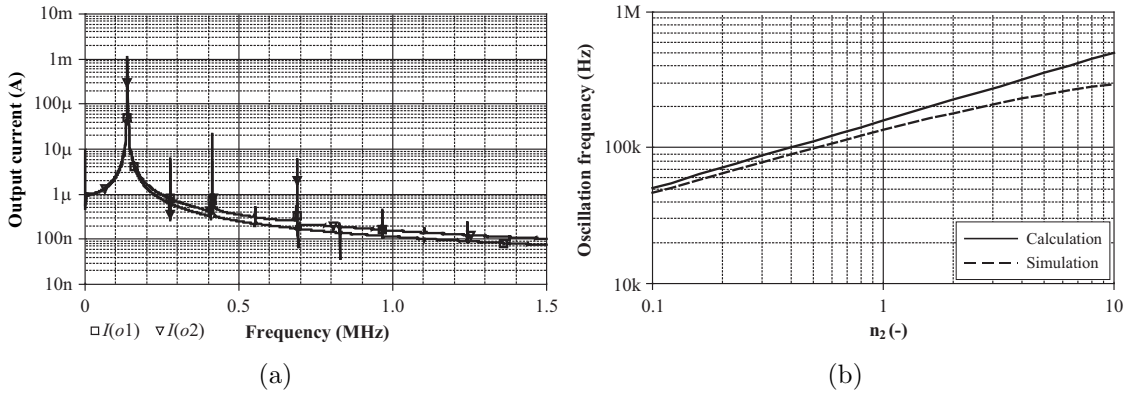


Fig. 7.4: (a) Simulated frequency spectrums of outputs I_{o1} and I_{o2}, (b) variation of oscillation frequency with mu-factor n_2 of the ^{2}PCA

oscillation frequency of 138 kHz, where the calculated value of this parameter from Eq. (7.13) yields 159.2 kHz. The simulated waveforms of the quadrature current outputs I_{o1} and I_{o2} in transient state and steady state are shown in Fig. 7.3(a) and Fig. 7.3(b), respectively. The steady state oscillations were reached within 200 μs after turning the supply sources on. No auxiliary amplitude control circuit is used for amplitude stabilization, rather the non-linearity of the active device itself limits the amplitude. If however, tight amplitude control is required, then the peak amplitude (magnitude sensing by either peak-detector or valley-detector [113]) can be sensed and resulting voltage can be used to reduce the bias current I_2 of ^{3}PCA to reduce n_3. This will reduce positive feedback action and help in achieving reduced amplitude of oscillation with low THD. For the chosen active parameters and passive component values, theoretically, the ratio of amplitudes of the generated orthogonal signals according to (7.14) should be 1.45 and through simulations the value comes

out to be 1.14. Fig. 7.4(a) shows the frequency spectrums of the output waveforms and the value of THD at both the outputs are less than 2%. The variation of FO with mu-factor n_2 (by DC bias current I_1 of the ^{2}PCA when $I_2 = 100$ μA) without affecting the CO is shown in Fig. 7.4(b). The total power dissipation of the proposed CM ETQO is calculated as 24.4 mW. Simulation results agree quite well with the theoretical analysis. Note that the inconsistencies in output current amplitudes are due to the non-ideal effects of the PCA that are partially examined above.

It should be pointed that conventional unity gain current followers and current inverters [58] are a special class of more general PCA. PCAs simulate these unity gain cells when the $n = 1$. Thus, in a way the proposed realization here can be equivalently created using a generalized current follower with dual/multiple outputs and which can act as either a current follower or a current conveyor. Note, however, that the resultant oscillator circuit using GCF will not have non-interactive tuning laws (a degree of freedom which is sacrificed by making $n_i = 1$). As pointed previously, a simpler realization takes place, when ^{1}PCA is replaced by a dual-output inverting current follower. This realization still provides independent electronic control of the CO and the FO, as according to (7.12) and (7.13).

Another important point that is to be addressed is the aspect of tunability. Over the last few years, numerous oscillator realizations were reported, which provide tunable CO and FO. These are primarily based on either OTA and variants as in [136], or CCCIIs as in [96] or OTA/CCCII hybrid elements as in [86]. The electronic control in such circuits is via the transconductance and which is a function of the bias current ($g_m = I_\mathrm{B}/2V_\mathrm{T}$ in BJTs, where V_T is the thermal voltage or $g_m = \sqrt{2I_\mathrm{B}\mu_0 C_{ox}(W/L)}$ in MOSFETs). Considering that I_B is temperature compensated (e.g. bias derived from a first-order band-gap provides a low temperature compensated (TC) bias current), then temperature variations in g_m in BJTs is primarily due the V_T term and in MOSFETs due to the μ term ($\mathrm{T}^{-1.5}$, typically). Thus, FO controlled by g_m varies inversely with temperature. Similarly, current from beta-multiplier current source $I_\mathrm{B} = \frac{1}{\mu_0 C_{ox}(W/L)R^2}$ will lead to temperature compensated g_m only if low TC resistor R is used. In such a case, the control of g_m (and thus the CO and FO) can be achieved only by varying R (creating electronically tunable R, for e.g. using MOSFETs working in triode region, would again feature temperature dependent terms). On the contrary, the controlling mu-factor in PCA proposed here is a ratio of two currents (preferably, temperature compensated) and thus FO variations with temperature are primarily due to the variations in passive component values (due to their non-zero temperature coefficients) and non-ideal current tracking coefficients, which have non-zero TCs. Low TC resistors should be used wherever FO spread with temperature is to minimized. A detailed discussion on this topic and corresponding simulation results are beyond the scope of the present

communication; the information is added just to provide a basic insight into how the presented scheme differs from OTA-C and CCCII-C oscillators.

7.3 Voltage-mode SRCO design from general topology

The proposed topology for realizing VM QO is shown in Fig. 7.5 [187]. Block A consists of a lossless inverting integrator providing the quadrature functionality and block B consists of a first-order stage with right hand pole, courtesy the negative resistance ($-R_3$). The topology is general and can be implemented using variety of ABBs depending on performance and application requirements. Doing routine analysis of the general topology in Fig. 7.5, yields the following CE:

$$\text{CE:} \quad s^2 C_1 C_2 R_1 R_2 R_3 + s C_1 R_1 (R_3 - R_2) + R_3 = 0. \tag{7.21}$$

From (7.21), the CO and the FO are given as:

$$\text{CO:} \quad R_3 \leq R_2, \tag{7.22}$$

$$\text{FO:} \quad f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{C_1 C_2 R_1 R_2}}. \tag{7.23}$$

Therefore, the CO and FO are independently controllable for two different resistors, R_3 and R_1, respectively. Thus, the topology is suitable for realizing single-resistance-controlled oscillators. The topology shown in Fig. 7.5 employs three resistors and two grounded capacitors, wherein the resistors symbolically represent both discrete resistors (R) and resistors simulated using any active device (e.g. by transconductance amplifiers).

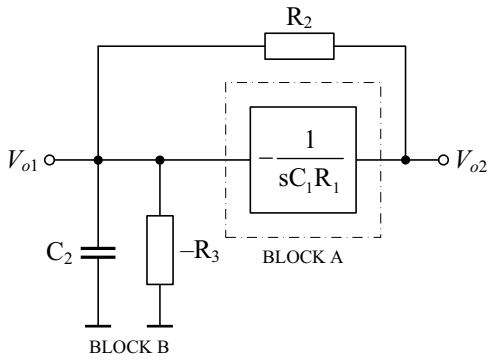


Fig. 7.5: The proposed topology for creating quadrature sinusoidal oscillators

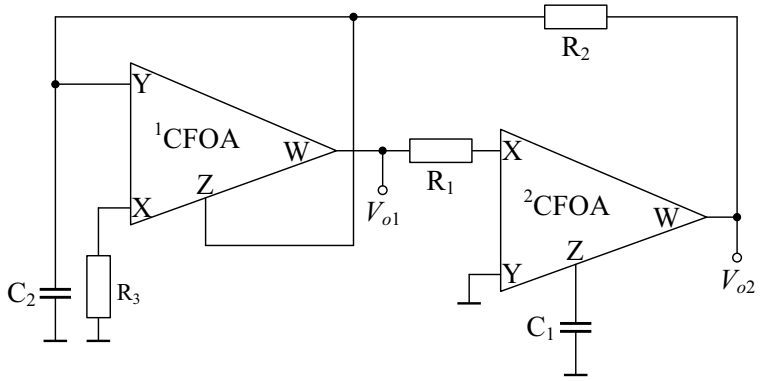


Fig. 7.6: Proposed new CFOA-based VM QO

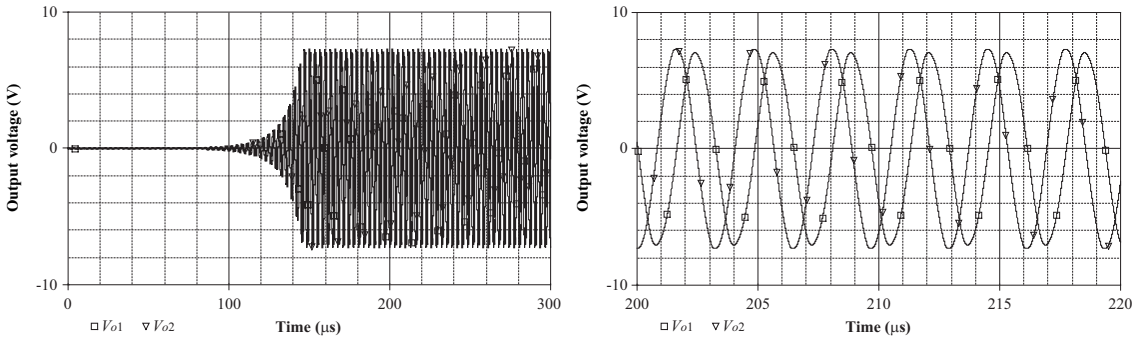
The topology shown in Fig. 7.5 is useful for realizing QOs. The VM QOs is shown in Fig. 7.6 and all of which are created using two CFOAs, three resistors and two capacitors. As compared to the recently proposed and so-claimed "first" CFOA based VM QO in [142], the circuit here uses grounded capacitors which is advantageous from monolithic integration point of view [141]. The circuit is governed by the tuning laws as indicated in (7.22) and (7.23) and provides two buffered quadrature voltage outputs, V_{o1} and V_{o2} that are related as:

$$V_{o1} = -jk_1 V_{o2}, \quad \text{where} \quad k_1 = \omega_0 C_1 R_1. \tag{7.24}$$

From (7.24) it is evident that the voltages are ideally 90° phase shifted and have equal amplitudes for $k_1 = 1$. Interestingly, the circuit in Fig. 7.6 can be further modified to provide explicit current outputs by using multiple Z copy terminals. However, commercially available CFOAs (e.g. AD844AN) do not have such features. Using multiple output CCII (MO-CCII) along with voltage buffers can easily create a complete mixed-mode QO.

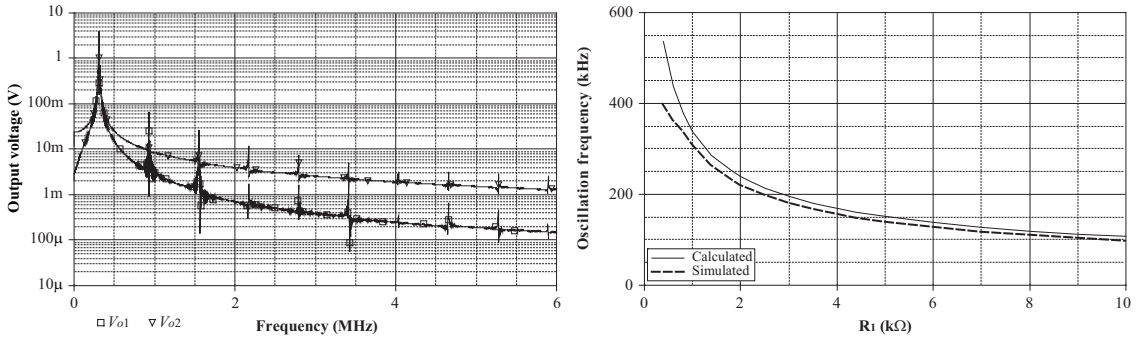
It is also necessary to point out that the similarity of the proposed VM QOs with already existing circuits in the literature. The circuit in [127] is another example of an oscillator derived from the topology in Fig. 7.5. The circuit is also very similar to the one proposed in [55]. It is worth mentioning that the first CFOA simulating the negative resistance has same voltage at all its terminals: Y, X, Z, and W; a unique feature which helps in creating different realizations by appropriately connecting the terminals [55]. All circuits in Fig. 7.6 and [55], [127] are ideally same.

The circuit in Fig. 7.6, i.e. the VM QO, is chosen as the design example. In simulations, the SPICE macro-model of the AD844AN CFOA by Analog Devices is used, which is characterized as follows: $R_{\rm X} = 50\ \Omega$, $R_{\rm Y} = 10\ {\rm M}\Omega$, $R_{\rm Z} = 3\ {\rm M}\Omega$, $R_{\rm W} = 15\ \Omega$, $C_{\rm X} = C_{\rm Y} = 2$ pF, and $C_{\rm Z} = 4.5$ pF. DC power supply voltages are equal to ± 12 V. The circuit has been designed with $R_1 = R_2 = R_3 = 1\ {\rm k}\Omega$ and



(a) (b)

Fig. 7.7: Simulated output waveforms V_{o1} and V_{o2} of the proposed oscillator in Fig. 7.6: (a) at transient stage and (b) at steady stage



(a) (b)

Fig. 7.8: (a) Simulated frequency spectrums of outputs V_{o1} and V_{o2}, (b) calculation and simulation results of the FO by varying the value of the resistor R_1

$C_1 = C_2 = 470$ pF. In practice, the value of $R_2 = 1.1$ kΩ is chosen greater than R_3 to ensure the startup (build-up) of oscillations. The simulated waveforms of the quadrature voltage outputs V_{o1} and V_{o2} in transient state and steady state are shown in Fig. 7.7(a) and Fig. 7.7(b), respectively. The steady state oscillations were reached within 150 μs after turning the supply sources on. The start-up time can be reduced further by increasing the value of R_2 (and thereby increasing the start-up open-loop gain and positive feedback). The simulated frequency is 310 kHz, which is in close correspondence with the theoretical value of 338 kHz. Fig. 7.8a shows the simulated frequency spectrum of the outputs V_{o1} and V_{o2}. The THD is equal to 2.1 % and 0.68 %, respectively. The variability of the FO with resistor R_1 is shown in Fig. 7.8(b) and is seen to be in good agreement with the corresponding theoretical values. The difference in simulated and theoretical values is primarily due to the non-idealities of the CFOA.

7.4 VM SRCO design using generalized CFTA and UGVF

The generalized configuration realizing VM SRCOs using GCFTA and UGVF is shown in Fig. 7.9. Using (3.10) and doing routine circuit analysis, the CE for the circuit topology can be found as:

$$\text{CE:} \quad s^2C_1C_2R_1R_2 + sC_2R_2(1 - ab_1g_mR_1) - ab_2g_mR_1 = 0. \tag{7.25}$$

For the above equation to represent a valid CE for an oscillator, the following conditions should be simultaneously satisfied:

$$ab_1 = 1, \quad ab_2 = -1. \tag{7.26}$$

Only two structures confirm these, as described in Tab. 7.1.

From (7.25) and (7.26), it is clear that for both the structures A and B, the CO, i.e. the term with s has to be 0 (zero), is:

$$\text{CO:} \quad g_mR_1 \geq 1, \tag{7.27}$$

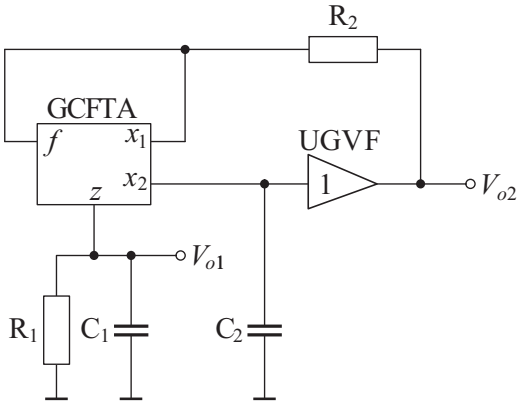


Fig. 7.9: The proposed generalized single-resistance-controlled quadrature oscillator using GCFTA and UGVF

Tab. 7.1: Coefficients of GCFTA

variant	a	b_1	b_2
A	1	1	–1
B	–1	–1	1

and the FO is:

$$\text{FO:} \quad f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{C_1 C_2 R_2}}. \tag{7.28}$$

It should be pointed out that although (7.27) defines the strict CO, however in practise $g_m R_1$ is made slightly more than unity for the start-up of oscillations. It is evident from (7.27) and (7.28) that the CO can be controlled independently of FO by changing R_1 and the FO can be controlled by means of resistor R_2. Therefore, the circuit truly describes a SRCO. The two quadrature voltage outputs of the general circuit topology as depicted in Fig. 7.9, are related as:

$$V_{o1} = jb_2 k V_{o2}, \quad \text{where} \quad k = \frac{\omega_0 C_2}{g_m}. \tag{7.29}$$

Clearly, for $k = 1$ the two quadrature voltages have equal amplitude.

For a complete analysis, it is important to take into account the non-idealities of the GCFTA. Here, we provide the non-ideal analysis for variant A (i.e. the one using CFTA+/–). The model of the CFTA+/– including parasitic elements is shown in Fig. 7.10. The non-ideal analysis for variant B can be carried on similar lines.

- The non-zero parasitic input resistance at the terminal f is represented by R_f.
- $I_z = \alpha I_f$, where α represents the parasitic current gain, whose ideal value is unity. Similarly, the voltage transfer gain γ for the unity-gain voltage follower (buffer) differs slightly from its ideal value of unity because of the voltage tracking error.
- The parasitic resistance R_z and parasitic capacitance C_z appears between the high-impedance z terminal and ground. The stray/parasitic capacitance C_z is absorbed into the external capacitance C_1 as it appears in parallel with it. Also, since the value of R_z is in the order of MΩ, hence for an external resistor of value $R_1 \ll R_z$ connected at this terminal, $R_z||R_1 \approx R_1$. Thus, the non-ideal effects of parasitic impedance at terminal z are reduced, if not

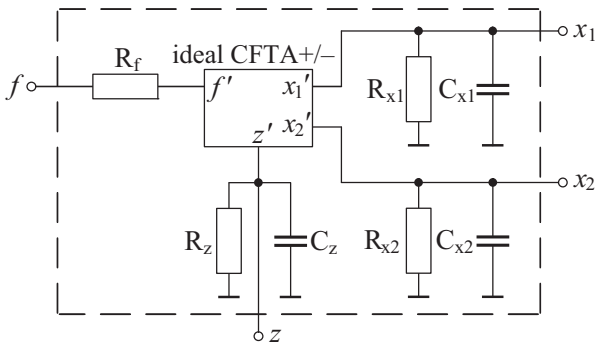


Fig. 7.10: Model of the CFTA+/– including parasitic elements

completely eliminated.

- The parasitic resistance R_{x_2} and parasitic capacitance C_{x_2} appears between the high-impedance x_2 terminal and ground. The parasitic capacitance can be absorbed in the external capacitance C_2, but the presence of parasitic resistance at terminal x_2 would change the type of the impedance, which should be of a purely capacitive character. A possible solution is to make the operating frequency $\omega_o > \frac{1}{R_{x_2}C_2}$.
- The parasitic resistance R_{x_1} and parasitic capacitance C_{x_1} appears between the high-impedance x_1 terminal and ground. To alleviate the effects of parasitic impedance at terminal x_1, the CFTA should be designed to have a very low input parasitic resistance at terminal f. Ideally, the value of input parasitic resistance at terminal f is zero and terminal f is virtually grounded. Thus, the parasitic impedance at terminal x_1 is connected between a virtual ground and a true ground.

Considering the first non-ideality and the parasitic capacitances at terminal z and x_2, the CO and FO of the proposed SRCO in Fig. 7.9 get modified and are given as:

$$\text{CO:} \quad \alpha g_m R_1 \geq 1, \tag{7.30}$$

and

$$\text{FO:} \quad f_0 = \frac{1}{2\pi}\sqrt{\frac{\alpha\gamma g_m}{(C_1+C_z)(C_2+C_{x_2})R_2}}. \tag{7.31}$$

The sensitivity study indicates that:

$$|S^{f_0}_{\alpha,\gamma,g_m,R_2}| = \frac{1}{2}, \tag{7.32}$$

$$S^{f_0}_{C_1} = -\frac{C_1}{2(C_1+C_z)}, \tag{7.33}$$

$$S^{f_0}_{C_z} = -\frac{C_z}{2(C_1+C_z)}, \tag{7.34}$$

$$S^{f_0}_{C_2} = -\frac{C_2}{2(C_2+C_{x_2})}, \tag{7.35}$$

$$S^{f_0}_{C_{x_2}} = -\frac{C_{x_1}}{2(C_2+C_{x_2})}. \tag{7.36}$$

It is evident from (7.32)–(7.36) that the magnitude values of all f_0 sensitivities are less than unity and hence the proposed SRCO exhibits an attractive sensitivity performance. Also, both the CO and the FO in (7.30) and (7.31) are subject to process and temperature variations, to the presence of g_m term in the expressions. Similar tuning laws are also present in [87] and [71]. This should not be seen as

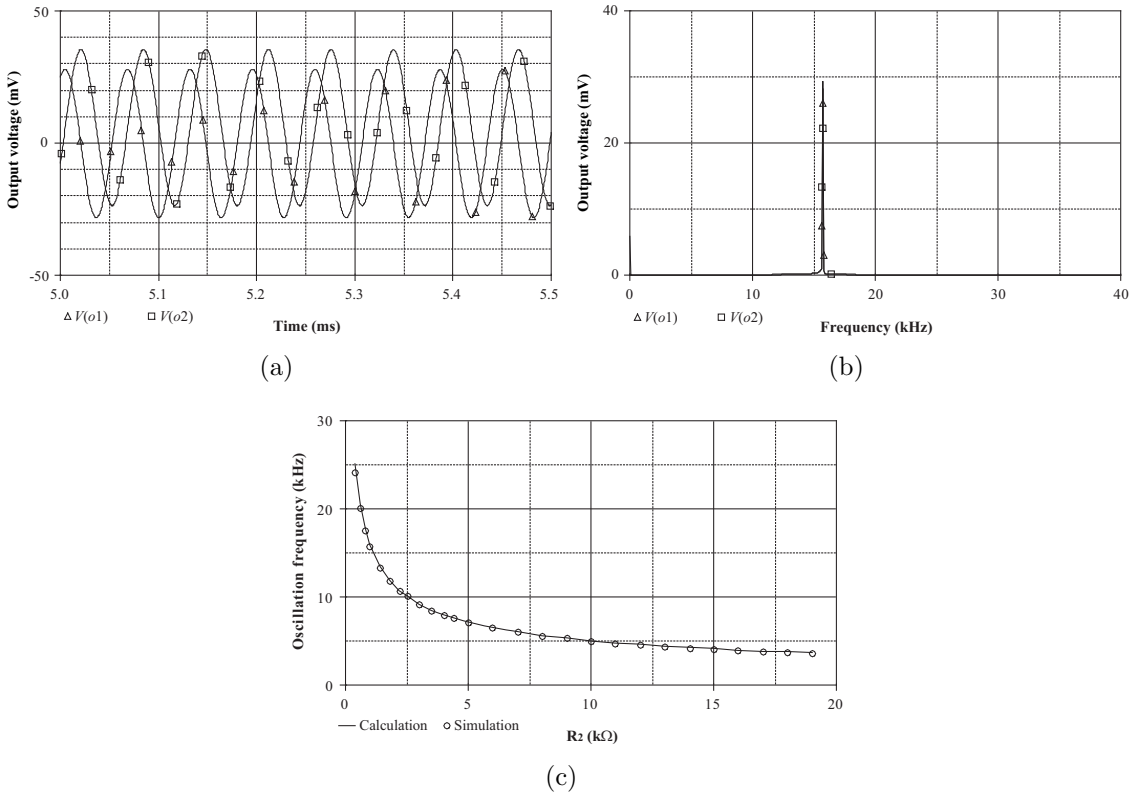


Fig. 7.11: (a) Quadrature voltage outputs V_{o1} and V_{o2} during steady stage, (b) simulated frequency spectrums of outputs V_{o1} and V_{o2}, (c) variation of oscillation frequency with R_2

a drawback for the FO, since the designer can control it using R_2. For the CO, a common practice is to make $R_1 > \frac{1}{g_m}$, so that even for any changes in the right-hand side value (g_m) the inequality is satisfied and there is an appropriate start-up of the oscillations. For more accurate tuning, the external resistors could be replaced by non-linearity canceled MOSFETs (working in triode region) [126]. This shall provide electronic tuning properties via gate voltages to both the CO and FO and a voltage-controlled oscillator (VCO) is created.

In order to confirm the above given theoretical analysis, the proposed CFTA-based SRCO (variant A) has been simulated with SPICE simulation program. The bipolar implementation of the CFTA+/–, shown in Fig. 3.18, and the bipolar implementation of the UGVF, presented in [112] as output stage of CFOA, has been used with the DC supply voltages of $+V_{CC} = -V_{EE} = 2$ V. In the design the transistor model parameters NR100N (NPN) and PR100N (PNP) of bipolar arrays ALA400-CBIC-R from AT&T were used [52] that are also listed in Tab. A.1. The maximum value of terminal voltage of the UGVF without producing significant distortion is in the full scale of the supply voltage (in this case ±2 V). The DC voltage gain of

Tab. 7.2: Total harmonic distortion analysis of the proposed CFTA and UGVF-based quadrature oscillator: (a) output V_{o1}, (b) output V_{o2}

Harmonic no.	Frequency (Hz)	Fourier component	Normalized component	Phase (Deg)	Normalized phase
1	1.592E+04	2.796E–02	1.000E+00	–1.113E+02	0.000E+00
2	3.183E+04	3.358E–04	1.201E–02	–1.289E+02	9.365E+01
3	4.775E+04	3.080E–04	1.102E–02	–7.385E+01	2.600E+02
4	6.366E+04	8.644E–05	3.091E–03	–1.232E+02	3.219E+02
5	7.958E+04	4.949E–05	1.770E–03	–1.303E+02	4.260E+02
DC component = 2.517015E–04					
Total harmonic distortion = 1.667991E+00 PERCENT					

(a)

Harmonic no.	Frequency (Hz)	Fourier component	Normalized component	Phase (Deg)	Normalized phase
1	1.592E+04	2.796E–02	1.000E+00	–1.111E+02	0.000E+00
2	3.183E+04	3.358E–04	1.201E–02	–1.286E+02	9.354E+01
3	4.775E+04	3.069E–04	1.098E–02	–7.338E+01	2.599E+02
4	6.366E+04	8.617E–05	3.082E–03	–1.229E+02	3.214E+02
5	7.958E+04	4.938E–05	1.766E–03	–1.300E+02	4.254E+02
DC component = 2.527028E–04					
Total harmonic distortion = 1.665571E+00 PERCENT					

(b)

the UGVF $\gamma \cong 0.9992$ with bandwidth $f_\gamma \cong 3.971$ GHz.

The proposed circuit was designed using the following component values: $C_1 = C_2 = 10$ nF, $R_2 = 1$ kΩ, and $g_m = 1$ mS ($I_B = 52\ \mu$A). The value of R_1 is kept slightly more than 1 kΩ to start the oscillations. The simulated output waveforms for V_{o1} and V_{o2} at steady stage are shown in Fig. 7.11(a). It is evident from Fig. 7.11(a) that the proposed circuit provides nearly equal sinusoidal waves and which is in accordance with (7.28). The offset (about 12 mV) of the V_{o2} is caused by the simple structure of the UGVF used [112] that does not enable suppress this parameter. Fig. 7.11(b) shows the frequency spectrum of the output waveforms and the value of THD at both the outputs are 1.67%. The results are summarized in Tab. 7.2. The variation of FO with resistor R_2 without affecting the CO is shown in Fig. 7.11(c) and it is seen that the simulated values exhibit a close correspondence with the theoretical predictions.

7.5 Single active element-based VM SRCOs in compact form

Presented VM oscillator circuits in previous Sections employ two active building blocks and five or four passive components, respectively, wherein some of them are in floating form. Therefore, the aim of this Section is to present single active element-based VM oscillator with grounded capacitors, which is ideal for integration.

The proposed circuit in compact form in [178] consists of single DBTA and only grounded passive elements, as shown in Fig. 7.12. The characteristic equation of the circuit can be expressed as:

$$\text{CE:} \quad s^2 C_2 C_3 + s(C_2 G_2 - C_1 g_m) + G_1 g_m = 0. \tag{7.37}$$

The oscillation condition and oscillation frequency ω_0 of this circuit can be obtained as:

$$\text{CO:} \quad C_1 R_2 = \frac{C_2}{g_m}, \tag{7.38}$$

$$\text{FO:} \quad \omega_0 = \sqrt{\frac{g_m}{C_2 C_3 R_1}}. \tag{7.39}$$

It should be noted that the condition of oscillation (7.38) can be controlled by adjusting the value of the resistor R_2 and/or the capacitor C_1 without affecting the oscillation frequency ω_0 (7.39). Analogously, oscillation frequency ω_0 can be adjusted by controlling the value of the resistor R_1 and/or the capacitor C_3 without affecting the oscillation condition. This means that the oscillation condition and oscillation frequency ω_0 are independently adjustable by different grounded resistor and/or capacitor. The use of grounded capacitors is particularly attractive for integrated circuit implementation [20]. Here can be mentioned that by replacing appropriate resistor with FET-based voltage-controlled resistor [126], the oscillation condition and the condition frequency ω_0 of this solution can be adjusted electronically, which

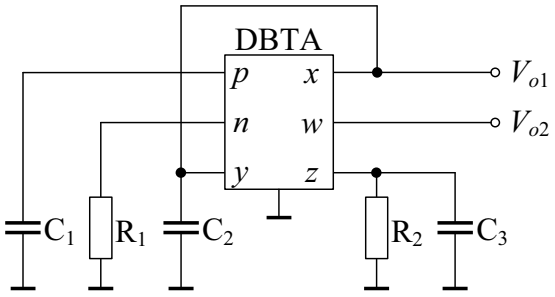
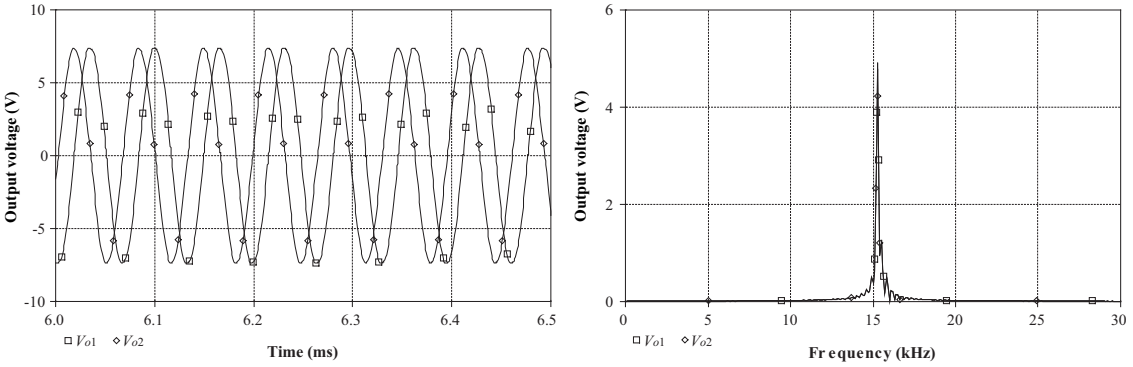


Fig. 7.12: Proposed DBTA-based voltage-mode quadrature oscillator



(a) (b)

Fig. 7.13: (a) Possible implementation of DBTA using three CFAs (AD844s); The simulated quadrature outputs V_{o1} and V_{o2} of the proposed oscillator: (b) output waveforms, (c) output spectrums

is also a particular advantage of the proposed circuit.

From Fig. 7.12, the voltage transfer function between two quadrature outputs V_{o1} and V_{o2} can be expressed as:

$$\frac{V_{o2}}{V_{o1}} = -\frac{g_m}{sC_2}, \tag{7.40}$$

where the phase difference is $\phi = 90^\circ$ ensuring the voltage V_{o1} and V_{o2} to be in quadrature.

Taking into account the non-idealities of DBTA, the characteristic equation becomes:

$$\text{CE:} \quad s^2C_2C_3 + s(C_2G_2 - \alpha_p\beta_pC_1g_m) + \alpha_p\alpha_n\beta_nG_1g_m = 0. \tag{7.41}$$

In this case, the modified oscillation condition and oscillation frequency ω_0 can be expressed as:

$$\text{CO:} \quad \alpha_p\beta_pC_1R_2 = \frac{C_2}{g_m}, \tag{7.42}$$

$$\text{FO:} \quad \omega_0 = \sqrt{\frac{\alpha_p\alpha_n\beta_ng_m}{C_2C_3R_1}}. \tag{7.43}$$

It should be noted from (7.42) and (7.43) that the oscillation condition and oscillation frequency ω_0 of the proposed quadrature oscillator are slightly altered by the effects of the DBTA current- and voltage-tracking errors. However, they can still be controlled independently.

The active and passive sensitivities of the quadrature oscillator parameters are:

$$S^{\omega_0}_{\alpha_p,\alpha_n,\beta_n,g_m} = -S^{\omega_0}_{C_2,C_3,R_1} = \frac{1}{2}. \tag{7.44}$$

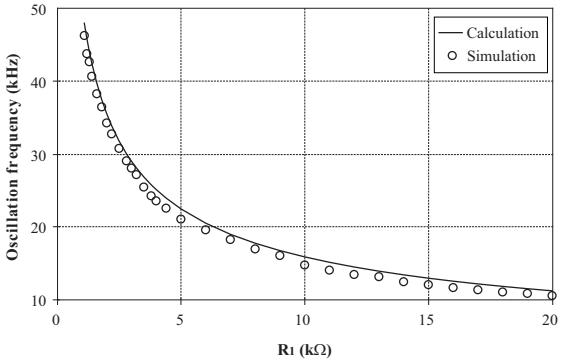


Fig. 7.14: Calculation and simulation results of the oscillation frequencies by varying the value of the resistor R_1

From Eq. (7.44) it is evident that the circuit has optimum sensitivity performance in the sense that all values are equal to 0.5 in magnitude.

In order to confirm the above given theoretical analysis, the proposed DBTA-based quadrature oscillator in Fig. 7.12 has been simulated using SPICE software. In simulations, the DBTA circuit was constructed with three commercially available current feedback amplifiers as shown in Fig. 3.9(a). The model parameters of AD844 were taken from the built-in library (AD844A/AD), and the supply voltages were taken as ±12 V. To obtain the sinusoidal output waveforms with the oscillation frequency of $f_0 = \omega_0/2\pi \cong 15.92$ kHz, the following passive component values have been chosen: $R_1 = R_2 = 10$ kΩ, $R_{\rm K} = 1/g_m = 10$ kΩ and $C_1 = C_2 = C_3 = 1$ nF, where $R_2 \cong 10.5$ kΩ was designed to be larger than $R_{\rm K} = 1/g_m$ to ensure the oscillations would start.

The simulated sinusoidal outputs V_{o1} and V_{o2} of the proposed quadrature oscillator is shown in Fig. 7.13(a). From the simulation results, the oscillation frequency of $f_0 \cong 15.61$ kHz is obtained, which agrees very well with the theoretical analysis. Fig. 7.13(b) shows the simulated frequency spectrum of the outputs V_{o1} and V_{o2}. For the both outputs the total harmonic distortion is equal to 1.63 %. The control of f_0 via resistor R_1 without affecting the oscillation condition is shown in Fig. 7.14.

7.6 Sub-conclusion

In this Chapter two current- and three voltage-mode quadrature oscillators are presented. The comparison of these circuits is given in Tab. B.4 and they offer the following advantages:

(i) Non-interactive (independent) control of condition of oscillation and frequency of oscillation.

(ii) Low incremental active and passive sensitivities.

(iii) Availability of two quadrature current or voltage outputs, which makes the proposed circuits suitable to be used in quadrature mixers or other communication systems wherein there is a requirement of multiple sinusoids which are 90° phase shifted, e.g. quadrature mixers and single sideband modulators [65], [81].

The first presented circuit employing two CCCFTAs is shown in Fig. 7.1. Due to external features (R_f and g_m) of used active elements, the proposed current-mode quadrature oscillator is resistorless. The behavior of the circuit has been verified by SPICE simulations and performed based on the MOSIS 0.5 μm CMOS technology parameters [182].

In the next Section, the first of its kind PCA-based CM ETQO has been reported (Fig. 7.2) [189]. The advantages of PCA in oscillator design have been proved since the proposed circuit employs only a bare minimum of four passive components. As it has been mentioned earlier that a PCA prototype using the implementation in [199] is ready to be manufactured by AMI Semiconductor Czech, Ltd., (part of the ON Semiconductor, Ltd.) in the CMOS 0.35 μm and labeled as COAK-NAA.

A new topology for realizing VM QO has been reported in Fig. 7.6 [187]. In general, any other ABB can be used depending on application requirements, e.g. frequency potential, non-idealities, dynamic range and cost.

Fig. 7.9 presents a first of its kind SRCO employing reduced number of components, i.e. single GCFTA, single UGVF, two resistors, and two capacitors [193]. It serves as a new application of GCFTA and offers advantages such are listed above.

In the last Section, the first VM QO using the novel DBTA has been demonstrated. The proposed oscillator in Fig. 7.12 consists of single DBTA, three grounded capacitors and two grounded resistors [178]. The use of only grounded passive elements makes the proposed circuit attractive for integrated circuit implementation.

The SPICE simulations confirm the feasibility of all proposed circuits and results are in good agreement with theory.

8 CONCLUSION

In the last decade, for analogue signal processing huge number of active building blocks were introduced, however, there is still the need to develop new active elements that offer new and better advantages. Therefore, the main contribution of this thesis was the definition of such novel ABBs, and their application possibilities.

Chapter 3 presents various active elements and introduces novel ones, such as the differential-input buffered and transconductance amplifier (DBTA), the current follower transconductance amplifier (CFTA), the z-copy current-controlled current inverting transconductance amplifier (ZC-CCCITA), the generalized current follower differential input transconductance amplifier (GCFDITA), the voltage gain-controlled modified current-feedback operational amplifier (VGC-MCFOA), and the minus-type current-controlled third-generation voltage conveyor (CC-VCIII–).

Using the proposed ABBs, in Chapter 4, novel structures of first-order all-pass filters are proposed. Chapter 5 presents novel structures of second-order universal filters, KHN-equivalent circuits, and inverse filters. Active grounded inductor simulators are discussed in Chapter 6, and in the Chapter 7 various quadrature sinusoidal oscillators are proposed. The proposed circuit work in the current-, voltage-, or mixed-mode and their comparison can be found in Appendix B.

To verify the behavior of the proposed circuits, all defined active elements are implemented using either bipolar or CMOS internal structure. The feasibility of selected circuits is also confirmed by experimental measurements.

Here, it is worth mention that part of this work has already been published in journals with impact factor (10 papers in the following journals: International Journal of Electronics, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, IEICE Electronics Express, and AEU - International Journal of Electronics and Communications) and presented at international conferences (17 papers): PWC'07 (12th IFIP International Conference on Personal Wireless Communications, Prague, Czech Republic), TELFOR'08 (16th Telecommunications Forum, Belgrade, Serbia), ICONS'08 (Third International Conference on Systems, Cancun, Mexico), APPEL'08, APPEL'09, and APPEL'10 (Applied Electronics, Pilsen, Czech Republic), NCSP'09 (RISP International Workshop on Nonlinear Circuits and Signal Processing, Honolulu, Hawaii, USA), ELECO'09 (6th International Conference on Electrical and Electronics Engineering, Bursa, Turkey), TSP'08 (International Conference on Telecommunications and Signal Processing, Paradfurdo, Hungary), TSP'09 (32th International Conference on Telecommunications and Signal Processing, Dunakiliti, Hungary), TSP'10 (33th International Conference on Telecommunications and Signal Processing, Baden near Vienna, Austria), and CSS'10 (4th International Conference on Circuits, Systems and Signals, Corfu

Island, Greece).

Moreover, here it should be also noticed that my works have received 12 citations from international researchers (for more details, please refer my CV).

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LIST OF ABBREVIATIONS

ABB active building block

AP all-pass

BJT bipolar junction transistor

BO-DITA balanced-output differential input transconductance amplifier

BOTA balanced-output operational transconductance amplifier

BP band-pass

BS band-stop

CBTA current backward transconductance amplifier

CCC composite current conveyor

CCCFTA current-controlled current follower transconductance amplifier

CCCII second-generation current-controlled current conveyor

CCCS current-controlled current source

C-CDBA current-controlled current differencing buffered amplifier

CCII second-generation current conveyor

CCII+/- dual-output second-generation current conveyor

CCs current conveyors

CC-VCIII– minus-type current-controlled third-generation voltage conveyor

CC-VCI+ current-controlled first-generation voltage conveyor

CCVS current-controlled voltage source

CDBA current differencing buffered amplifier

CDTA current differencing transconductance amplifier

CDU current differencing unit

CE characteristic equation

CF current follower

CFDITA current follower differential input transconductance amplifier

CFOA current-feedback operational amplifier

CFTA current follower transconductance amplifier

CFTA current follower transconductance amplifier

CI current inverter

C-ICDBA current-controlled inverting current differencing buffered amplifier

CIDITA current inverter differential input transconductance amplifier

CITA current inverter transconductance amplifier

CM current-mode

CMI current mirror and inverter

CMOS complementary metal oxide semiconductor

CO condition of oscillation

DBTA differential-input buffered and transconductance amplifier

DCC differential current conveyor

DCFA differential-input current feedback amplifier

DCV digitally-controlled varactor

DCVC+ plus-type differential current voltage conveyor

DCVCI first-generation differential current voltage conveyor

DDCC differential difference current conveyor

DDCCC differential difference complementary current conveyor

DVCC differential voltage current conveyor

DXCCII dual-X second-generation current conveyor

ECCII electronically tunable second-generation current conveyor

ECOs explicit current outputs

ETQO electronically tunable quadrature oscillator

FDCCII fully balanced second-generation current conveyor

FDCCII fully differential current conveyor

FDNR frequency dependent negative resistances

FO frequency of oscillation

GCFDITA generalized current follower differential input transconductance amplifier

GCFTA generalized current follower transconductance amplifier

GSM Global System for Mobile communication

GVCCIII gain-variable third-generation current conveyor

HP high-pass

IBPF inverse band-pass filter

ICCII inverting second-generation current conveyor

ICFTA inverted current follower transconductance amplifier

IEEE Institute of Electrical and Electronics Engineers

IF Intermediate Frequency

IHPF inverse high-pass filter

ILPF inverse low-pass filter

ITU International Telecommunication Union

IVF inverting voltage follower

KHN Kerwin-Huelsman-Newcomb

LAN Local Area Network

LP low-pass

MCFOA modified current-feedback operational amplifier

MDCC modified differential current conveyor

MICCII modified inverting second-generation current conveyor

MISO multi-input single-output

MO-CF multiple-output current follower

MO-CFTA multiple-output current follower transconductance amplifier

MOSFET metal oxide semiconductor field effect transistor

NIS negative inductance simulator

OTA operational transconductance amplifier

PCA programmable current amplifier

PFTFN positive four terminal floating nullor

PID proportional-integral-derivative

PIS positive inductance simulator

QO quadrature oscillator

SIFO single-input four-output

SIMO single-input multi-output

SITO single-input three-outputs

SNAP Symbolic Network Analysis Program

SPICE Simulation Program with Integrated Circuit Emphasis

SRCO single-resistance-controlled oscillator

TA-M trans-admittance-mode

TC temperature compensated

THD total harmonic distortion

TI-M trans-impedance-mode

TISO three-input single-output

TSMC Taiwan Semiconductor Manufacturing Company

UCC universal current conveyor

UGVF unity-gain voltage follower

UVC universal voltage conveyor

VC voltage conveyor

VCC voltage-controlled capacitor

VCCS voltage-controlled current source

VCG-CCII voltage and current gain second-generation current conveyor

VCI+ plus-type first-generation voltage conveyor

VCII+ plus-type second-generation voltage conveyor

VCR voltage-controlled resistor

VD-DIBA voltage differencing-differential input buffered amplifier

VF voltage follower

VGCCII variable gain current conveyor

VGC-MCFOA voltage gain-controlled modified current-feedback operational amplifier

VM voltage-mode

WTA wideband transconductance amplifier

ZC-CCCITA z-copy current-controlled current inverting transconductance amplifier

ZC-CFTA z-copy current follower transconductance amplifier

ZC-CG-CDBA z copy-controlled gain-current differencing buffered amplifier

LIST OF SYMBOLS

a, b general current transfer coefficients

a_i coefficients of non-cascade synthesis

α non-ideal current gain

β, δ, γ, μ_w non-ideal voltage gains

β_{z+}, β_{z-} non-ideal current gains of the PCA

C capacitor

CE characteristic equation

C_{OX} gate oxide capacitance per unit area

D denominator of transfer function

ε_i current tracking error

ε_v voltage tracking error

f frequency

f_0 characteristic frequency

φ phase of all-pass filter

f, z, zc, v, x_1, x_2, $x+$, $x-$ input or output current terminals of the CFTA and its derivatives

G conductance

$\mathrm{G_K}$, $\mathrm{R_K}$ conductor, resistor connected to current input X terminal of the UCC

g_m transconductance of the OTA

h voltage gain of the VGC-MCFOA

i terminal current of an active element

I terminal current of a function block

I_B bias current of the transconductance

I_D drain current

I_{O} control current

k Boltzmann constant

K, $T(s)$ current or voltage transfer function

M_i CMOS transistor

μ_0 free electron mobility in the channel

n current gain (mu-factor) of the PCA

ω_g first-pole of the OTA

ϕ phase difference between two outputs in quadrature oscillators

p, n, w, $z+$, $z-$ input or output, current or voltage terminals of the CBTA

p, n, y, x, w, z input or output, current or voltage terminals of the DBTA

q charge of an electron

Q_i BJT transistor

R resistance

R_f intrinsic resistance of the f terminal

$s = j\omega$ complex parameter - Laplace operator

S_R relative sensitivity

v terminal voltage of an active element

V terminal voltage of a function block

V_{B} bias voltage of the UVC

V_{C} control voltage

V_{CC}, V_{EE} supply voltages of BJT structures

V_{DD}, V_{SS} supply voltages of CMOS structures

V_{DS} drain to source voltage

V_{GS} gait to source voltage

V_{T} thermal voltage

W/L CMOS transistor dimensions

XS, YS, ZS+, ZS– input or output, current or voltage terminals of the CCII+/–

X, Y1, Y2, Y3, Z1+, Z1–, Z2+, Z2– input or output, current or voltage terminals of the UCC

X, YP, YN, W, ZP, ZN input or output, current or voltage terminals of the UVC

X, Y, Z, W input or output, current or voltage terminals of the CFOA, MCFOA, VGC-MCFOA

X, Y, ZN input or output, current or voltage terminals of the CC-VCIII–

x, z_1, z_2 input or output current terminals of the PCA

Y admittance

Z impedance

LIST OF APPENDICES

A TRANSISTOR MODEL PARAMETERS

Tab. A.1: Model parameters of the NR100N and PR100N bipolar array transistors

.MODEL NR100N NPN (RB = 524.6 IRB = 0 RBM = 25 RC = 50 RE = 1
+ IS = 121E–18 EG = 1.206 XTI = 2 XTB = 1.538 BF = 137.5 IKF = 6.974E–3
+ NF = 1 VAF = 159.4 ISE = 36E–16 NE = 1.713 BR = 0.7258 IKR = 2.198E–3
+ NR = 1 VAR = 10.73 ISC = 0 NC = 2 TF = 0.425E–9 TR = 0.425E–8
+ CJE = 0.214E–12 VJE = 0.5 MJE = 0.28 CJC = 0.983E–13 VJC = 0.5
+ MJC = 0.3 XCJC = 0.034 CJS = 0.913E–12 VJS = 0.64 MJS = 0.4 FC = 0.5)
.MODEL PR100N PNP (RB = 327 IRB = 0 RBM = 24.55 RC = 50 RE = 3
+ IS = 73.5E–18 EG = 1.206 XTI = 1.7 XTB = 1.866 BF = 110.0 IKF 12.359E–3
+ NF = 1 VAF = 51.8 ISE = 25.1E–16 NE = 1.650 BR = 0.4745 IKR = 6.478E–3
+ NR = 1 VAR = 9.96 ISC = 0 NC = 2 TF = 0.610E–9 TR = 0.610E–8
+ CJE = 0.180E–12 VJE = 0.5 MJE = 0.28 CJC = 0.164E–12 VJC = 0.8
+ MJC = 0.4 XCJC = 0.037 CJS = 1.03E–12 VJS = 0.55 MJS = 0.35 FC = 0.5)

Tab. A.2: 0.35 μm TSMC CMOS parameters

.MODEL CMOSN NMOS (LEVEL = 3 TOX = 7.9E–9 NSUB = 1E17
+ GAMMA = 0.5827871 PHI = 0.7 VTO = 0.5445549 DELTA = 0 UO = 436.256147
+ ETA = 0 THETA = 0.1749684 KP = 2.055786E–4 VMAX = 8.309444E4
+ KAPPA = 0.2574081 RSH = 0.0559398 NFS = 1E12 TPG = 1 XJ = 3E–7
+ LD = 3.162278E–11 WD = 7.046724E–8 CGDO = 2.82E–10 CGSO = 2.82E–10
+ CGBO = 1E–10 CJ = 1E–3 PB = 0.9758533 MJ = 0.3448504
+ CJSW = 3.777852E–10 MJSW = 0.3508721)
.MODEL CMOSP PMOS (LEVEL = 3 TOX = 7.9E–9 NSUB = 1E17
+ GAMMA = 0.4083894 PHI = 0.7 VTO = –0.7140674 DELTA = 0 UO = 212.2319801
+ ETA = 9.999762E–4 THETA = 0.2020774 KP = 6.733755E–5 VMAX = 1.181551E5
+ KAPPA = 1.5 RSH = 30.0712458 NFS = 1E12 TPG = –1 XJ = 2E–7
+ LD = 5.000001E–13 WD = 1.249872E–7 CGDO = 3.09E–10 CGSO = 3.09E–10
+ CGBO = 1E–10 CJ = 1.419508E–3 PB = 0.8152753 MJ = 0.5
+ CJSW = 4.813504E–10 MJSW = 0.5)

B COMPARISON OF PROPOSED CIRCUITS

Tab. B.1: Comparison of proposed first-order all-pass filters in Chapter 4

Proposed circuit	Mode	Active element	External capacitor	External resistor	Tunability	Matching condition	Type of response
Fig. 4.1(a)	CM	1 CIDITA	1 Grounded	1 Grounded	No	Yes	Non-inverting resp.
Fig. 4.3	CM	2 CCCFTA	1 Floating	2 Grounded	Yes	Yes	Both resp. simultaneously
Fig. 4.5	CM	1 VGC-MCFOA	1 Grounded	3 Grounded	Yes	Yes	Both resp. simultaneously
Fig. 4.8	CM	1 CBTA	1 Grounded	No	Yes	No	Inverting resp.
Fig. 4.12(a)	VM	1 UVC	1 Floating	1 Floating 2 Grounded	No	Yes	Both resp. simultaneously
Fig. 4.12(b)	VM	1 UVC	1 Floating	2 Grounded	No	Yes	Both resp. simultaneously
Fig. 4.12(c)	VM	1 UVC	1 Floating	2 Grounded	No	Yes	Both resp. simultaneously
Fig. 4.12(d)	VM	1 UVC	2 Grounded	2 Grounded	No	Yes	Both resp. simultaneously
Fig. 4.16(a)	VM	1 UVC	1 Floating	1 Floating	No	No	Both resp. simultaneously
Fig. 4.16(b)	VM	1 UVC	1 Floating	No	Yes	No	Both resp. simultaneously
Fig. 4.19	VM	1 CC-VCIII–	1 Floating	No	Yes	No	Non-inverting resp.
Fig. 4.24	Mixed	1 DBTA	1 Floating	2 Grounded	No	Yes	Non-inverting TA-M resp. Inverting VM resp.

Tab. B.2: Comparison of proposed second-order filters in Chapter 5

Proposed circuit	Mode	Active element	External capacitor	External resistor	Type of circuit
Fig. 5.1	CM	1 CCCFTA	2 Floating	No	Universal
Fig. 5.3	VM	1 DBTA	2 Floating	2 Floating	Universal
Fig. 5.7(a)	VM	1 MCFOA	3 Floating	2 Floating	Universal
Fig. 5.7(b)	VM	1 MCFOA	3 Floating	2 Floating	Universal
Fig. 5.9	CM	3 ZC-CFTA	2 Grounded	1 Grounded	KHN-equivalent
	TA-M	3 ZC-CFTA	2 Grounded	1 Floating	KHN-equivalent
Fig. 5.14	VM	3 DDCC	2 Grounded	2 Grounded	Inverse low-pass
Fig. 5.15	VM	3 DDCC	2 Grounded	2 Grounded	Inverse band-pass
Fig. 5.16	VM	3 DDCC	2 Grounded	2 Grounded	Inverse high-pass

Tab. B.3: Comparison of proposed grounded inductor simulators in Chapter 6

Simulator in references	Active element	External capacitor	External resistor
[74]	1 FDCCII	1 Grounded	2 Grounded
[84]	1 PFTFN	1 Floating	2 Floating, 2 Grounded
[89]	2 CFOA	None	1 Floating, 1 Grounded
[156]	3 CCII+	1 Grounded	1 Floating, 2 Grounded
	3 CCII+	1 Grounded	2 Grounded
[157]	1 CFOA	1 Floating	1 Floating, 1 Grounded
[161]	1 MICCII–	1 Floating	1 Floating, 1 Grounded
[162]	1 GVCCIII+	1 Floating	1 Floating, 1 Grounded
My work in Fig. 6.1	2 CFTA	1 Grounded	None
My work in Fig. 6.2	1 ZC-CCCITA	1 Grounded	None

Tab. B.4: Comparison of proposed quadrature oscillators in Chapter 7

Proposed circuit	Mode	Active element	External capacitor	External resistor	Non-interactive control of CO and FO
Fig. 7.1	CM	2 CCCFTA	2 Grounded	No	Yes
Fig. 7.2	CM	3 PCA	1 Floating, 1 Grounded	2 Floating	Yes
Fig. 7.6	VM	2 CFOA	2 Grounded	2 Floating, 1 Grounded	Yes
Fig. 7.9	VM	1 GCFTA, 1 UGVF	2 Grounded	1 Floating, 1 Grounded	Yes
Fig. 7.12	VM	1 DBTA	3 Grounded	2 Grounded	Yes

Curriculum Vitae

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- International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom 2009)
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- 12th WSEAS International Conference on Networking, Vlsi and Signal Processing (ICNVS 2010)
- 33rd International Conference on Telecommunications and Signal Processing (TSP 2010)

Results in Total

Paper Reviews: 32

h-index according to Web of Science: 3

Publications: 60

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