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VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF FOREIGN LANGUAGES
ÚSTAV JAZYKŮ

COMMENTED TRANSLATION OF A TEXT ON SCIENCE AND TECHNOLOGY
KOMENTOVANÝ PŘEKLAD ODBORNÉHO TEXTU

BACHELOR'S THESIS
BAKALÁŘSKÁ PRÁCE

AUTHOR — **Libor Smejkal**
AUTOR PRÁCE

SUPERVISOR — **Mgr. Miroslav Kotásek, Ph.D.**
VEDOUCÍ PRÁCE

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VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ

Bakalářská práce

bakalářský studijní obor **Angličtina v elektrotechnice a informatice**
Ústav jazyků

Student: Libor Smejkal ***ID:*** 184269
Ročník: 3 ***Akademický rok:*** 2018/19

NÁZEV TÉMATU:

Komentovaný překlad odborného textu

POKYNY PRO VYPRACOVÁNÍ:

Přeložte 15 stran odborného nebo populárně naučného textu s elektrotechnickým zaměřením do angličtiny. Připravte podklady pro analýzu rozdílů a shody ve vyjádření odborné informace v obou jazycích

DOPORUČENÁ LITERATURA:

Krhutová Milena: Parameters of Professional Discourse,Tribun EU, 2009,

Knittlová Dagmar: Překlad a překládání, Olomouc, 2015

Krhutová Milena: The language of electrical engineering as a special province, CERM, Brno, 2007

Termín zadání: 6.2.2019 ***Termín odevzdání:*** 28.5.2019

Vedoucí práce: Mgr. Miroslav Kotásek, Ph.D.
Konzultant:

doc. PhDr. Milena Krhutová, Ph.D.
předseda oborové rady

ABSTRACT

The aim of this bachelor thesis is a translation of a technical text from Czech to the English language and comment on the aspects of the translation and its problems. The chosen text is an electronic textbook, distributed on e-learning and used by the Brno University of Technology solely for educational purposes on the microelectronics field. Theoretical part presents the translation theory, its processes, procedures and types. It also contains a description of the functional styles, especially the style of science and technology. The practical part is represented by the translation of the first two chapters - *Introduction* and the *CMOS technology*. The final – analytical part contains the commentary on various issues from different linguistic perspectives.

KEYWORDS

translation theory, style of science and technology, commentary, translation procedures, CMOS technology

ABSTRAKT

Cílem této bakalářské práce je překlad technického textu z českého jazyka do anglického a okomentovat aspekty překladu a problémy s tím spojené. Vybraný text jsou elektronická skripta, sdílená na e-learningu a používána Vysokým Učením Technickým v Brně výhradně pro výukové účely v oboru mikroelektrotechnika. Teoretická část uvádí teorii překladu, její procedury, postupy a typy. Také obsahuje popis funkčních stylů, obzvláště stylu odborného. Praktická část je reprezentována překladem prvních dvou kapitol – Úvodem a technologií CMOS. Závěrečná – analytická část obsahuje komentáře různých problémů z odlišných lingvistických hledisek.

KLÍČOVÁ SLOVA

teorie překladu, odborný styl, komentář, překladatelské postupy, technologie CMOS

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Prohlášení

Prohlašuji, že svoji bakalářskou práci na téma Komentovaný překlad odborného textu jsem vypracoval samostatně pod vedením vedoucího semestrální práce a s použitím odborné literatury a dalších informačních zdrojů, které jsou všechny citovány v práci a uvedeny v seznamu literatury na konci práce.

Jako autor uvedené bakalářské práce dále prohlašuji, že v souvislosti s vytvořením této bakalářské práce jsem neporušil autorská práva třetích osob, zejména jsem nezasáhl nedovoleným způsobem do cizích autorských práv osobnostních a/nebo majetkových a jsem si plně vědom následků porušení ustanovení § 11 a následujících zákona č. 121/2000 Sb., o právu autorském, o právech souvisejících s právem autorským a o změně některých zákonů (autorský zákon), ve znění pozdějších předpisů, včetně možných trestně právních důsledků vyplývajících z ustanovení části druhé, hlavy VI. díl 4 Trestního zákoníku č. 40/2009 Sb.

V Brně dne …….. ……

(podpis autora)

ACKNOWLEDGEMENT

I would like to sincerely thank and express my gratitude to my supervisor Mgr. Miroslav Kotásek Ph.D. for his guidance and patience. I would also like to thank to my family, for supporting me during my studies.

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Introduction

English today undoubtedly represents the modern *lingua franca*, the leading language of science, world trade, diplomacy, major media agencies, or tourism. In the field of science, English is used as the sole language at almost all international meetings, and also all major scientific journals are also published in English.

This thesis aims to translate a technical text from Czech to English language and comment on the aspects of the translation and its problems. The source text is educational material called Design of Analogue Integrated Circuits written by Ing. Vilém Kledrowetz, Ph.D. and doc. Ing. Jiří Háze. Ph.D. (who is also a supervisor of the same-named course), in Brno University of Technology, Faculty of Electrical Engineering and Communication.

I chose the topic "Commented translation of a text on science and technology" for my bachelor thesis because I have always been interested in the translation issues and electrical engineering. By studying the materials needed to elaborate this bachelor thesis. Hopefully, I will gain theoretical knowledge and extend my practical skills and abilities, mainly concerning the translation of professional texts.

Another reason why this electronic textbook was chosen is that the text should provide enough content for the thesis as it contains several professional terms and abbreviations. Furthermore, the translated electronic textbook could be used for the education of foreign students of this course, which might be useful for the university. The students are supposed to have basic knowledge about electronic components (especially transistors, resistors and capacitors) which means that most of the terms are not explained.

The first part of the thesis is dedicated to the translation theory, presenting the processes, procedures and types. Special attention is given to the topic of functional styles, especially to the style of science and technology. Following with the practical part – the translation of the first two chapters - *Introduction* and the *CMOS technology*. The final – analytical part contains the commentary on various issues from different linguistic perspectives.

1 Theoretical part

1.1 Translation theory

The difference between the translator and the author of an artistic or professional text is determined by the ultimate goal of their work. Levý (1998) says that the aim of the translator's work is to preserve, capture, communicate the original work, not to create a new piece of work which had no predecessor. The aim of the translation is reproductive, according to him. The translator translates the author's work only stylistically, not contently. If the translator changes the content of the translated text, either due to inadequate knowledge of the language or cultural background of the country where the language is spoken or for some other reason, it is an incorrect translation.

As stated above, specific requirements are demanded from translators. The translator must have a good understanding of the text; in other words, he must know the language from which he translates. Furthermore, he must know the language in which he translates and substantive content of the text, i.e. local cultural background. The translator should also be familiar with the translation methods and procedures and should be able to apply them in practice.

According to Grygová (2009), quality translation must meet at least **three basic requirements:**

a) language expression acts naturally in the target language,

b) the resulting communication has the same meaning in the target language (or meaning as close as possible to the identical state) as its original in the source language, and acts on the recipient in the same way as the original text acted on the native speaker of the source language (in other words, the entropy is low as possible),

c) language expression in the target language preserves the dynamics of the original expression formulated in the default language - the translation should cause the same reaction as it caused in the default language

1.2 Translation process

The first precondition for achieving good translation is a good understanding of the initial text of the source language. Overall understanding of the text can prevent wrong translation of more complex parts. The translated text of the target language must be understandable; therefore, in case of professional style, the translator is often forced to add various comments and additions (Levý, 1998).

Today's linguists agree on dividing the translation process into three parts, but the individual parts differ from one linguist to another. For example, one of our most famous linguists, Jiří Levý, divides the translation phases in his book *Umění překladu* as:

1. **Understanding of translating text**

   The translator must first understand the origins of the translated text. This understanding is not only about the language in which the original text is written, but also about the aesthetic tuning of the original and the facts expressed in it. This phase is crucial, especially in the translation of professional texts, considering their sometimes very complicated sentence structure. Hence, it means that the translator must primarily be a good reader.

2. **Interpretation of translating text**

   The task of the translator is to identify the objective ideas of the translated text. On the other hand, his task is not to translate ideas and qualities that are not in the original. Then it would not be a translation, but a modification of the work.

3. **Transcription of the original text**

   The final phase of translating is the transcription of the original text in SL (source language) to TL (translation language) so that the original idea is understandable to the recipient of the translated work. The translator must, first of all, be aware of the semantic differences between SL and TL. Furthermore, a good translator should not allow the stylistic features typical for SL, if these features are not present in TL, or are present, but at a much lesser extent, to be reflected in the translation.

The translation should begin with a translator's analysis of the text. At this phase, the translator tries to find all possible pitfalls of the text in order to be able to translate the entire text correctly and comprehensible for the reader. Based on the interpretation, the translator formulates a concept that forms the basis of his / her further process and determines the methods used to reproduce the original. The last phase of the translator's work is the creation of a new text. The purpose of translation is not just putting the word behind the word, but the idea behind the ideas (Levý, 1998).

1.3 Translation procedures

The translation process uses different methods, paths, procedures, and different naming of these methods, although they are essentially all leading to the solution of the same problem (Knittlová a kol., 2010). If there is no suitable target language translation for the term of the source language, the translator must choose such procedures to compensate for the missing term. It cannot be avoided because the information or part of it can disappear in the professional text, which can cause the loss of its precision.

Vinay and Darbelnet have distinguished seven basic procedures to solve the lack of a target language equivalent (Knittlová, 2010). Sorting them from the simplest to the most complex:

1) Transcription – also transliteration, transforming a term using a different language system
2) Calque – literal translation
3) Substitution – replacing a term by its equivalent (noun/pronoun)
4) Transposition – grammatical modification due to a different language system
5) Modulation – change of viewpoint (e.g. *elbow of the pipe: koleno potrubí*)
6) Equivalence – expressing a term by different structural or stylistic means (*my sweet girl: děvenka*)
7) Adaptation – the substitution of an event not present in a culture of the target language using an equivalent event (idiom translation)

Assuming that there is no direct equivalent (equality between the expression in the source language and the equivalent in the target language), Joseph L. Malone states the following steps (Knittlová, 2000):

1) Equality (A = E)
2) Substitution (A : S)
3) Divergence (A : B/C)
4) Convergence (B/C : A)
5) Amplification (A : AB)
6) Reduction (AB : A)
7) Diffusion (AB : A/B)
8) Condensation (A/B : AB)
9) Reordering (AB : BA)

1.4 Translation types

Jakobson (1959) divides the translation according to the reproduction of word signs into three types:

1) **Intralingual** (or rewording) – word signs are reproduced by other signs in the same language (e.g. dictionaries, reformulations of sentences, paraphrases).
2) **Interlingual** (or proper translation) – word signs are reproduced by means of another language (translation between languages).
3) **Intersemiotic** (or transmutation) – word signs are reproduced by means of other sign systems (e.g. verbal to nonverbal sign system - movie translated into a book) (Levý, 1998).

M. Hrdlička distinguishes in his work *Literární překlad a komunikace* three types of approaches to interpreting the translations according to their relation to the original text:

1) **The literal (faithful) translation** aims to reproduce the original text mechanically. The creativity is missing. The translator is limited by the source text. The text is divided according to the original structure regardless of the word order. Every detail matters. Nowadays, it is almost never used anymore.

2) **Free (adaptation) translation** is the opposite of literal translation. The free translation tries to translate the original text sometimes in a too creative way. The author often aims to achieve the beauty and likeness of the translated work. This translation has been applied in the past, where, thanks to excessive freedom and creativity in translation creation, translations have become challenging to understand nowadays.

   These two different ways of translation are the critical moments in the development of the translation method and the concept of interpreting the original text.

3) **Adequate translation**, on the one hand, aims to remain faithful to the original, but on the other hand, tries to adopt expressive tools to contemporary readers. Reader's objective qualities and identity are respected, but they are rather perceived as people living nowadays. The reproductive and creative components should be applied in translation in the way of not distorting the values of the original text in a new communication context (Hrdlička, 1997).

1.5 Functional styles

This chapter is focused on the functional styles of written language. These functional styles include administrative style, style of science and technology (or professional style), newspaper style (journalistic), style of literature/arts (belles-lettres) and publicistic style. A distinction is made in the purpose and manner of communication - the main task is to convert invariant information. It is not only about factual information, but also about aesthetic information. In the administrative, professional and publicistic style - factual information plays a significant role, so the content of the message is the most important. On the contrary, in the journalistic and artistic style, the emphasis is on aesthetic information. When translating into a target language, the translator must select language tools that have the same function in the default text (Knittlová, 2000).

The practical part of this bachelor thesis is focused on the translation of the text, which belongs to the style of science and technology, specifically to didactic substyle.

1.6 Didactic style

The didactic style is intended not only to convey certain necessary information but also to activate interest in it, to control the process of acquiring information, etc. Intentional action on the recipient (in addition to the professionally informative feature) is an important factor shaping the style. It is also influenced by the fact that textbooks, especially school textbooks, form a system that must meet both professional and didactic content requirements. Traditionally, these texts were designed to assume the mediating role of the teacher who led the perception. Furthermore, the teacher supplemented the information according to the current situation and directed knowledge acquisition during practice, etc. The link between the student and the teacher written textbook is now partly disseminated by various e-learning courses that are used by the teacher for the necessary interaction between them in the internet environment (Hausenblas, 1972).

The text should be logically structured to explain the topic step by step and helps to orientate in it. The didactic style extensively uses professional terminology, in this case from the field of electrical engineering (Hausenblas, 1972).

1.7 Style of science and technology

English professional language has its typical features and specifics. Its task is to convey the information from the scientific or technical field as concisely and accurately as possible. In the professional style, great emphasis is placed on the nature of things dealt with in the text. The agent/executor of the action is not essential in this case, and therefore, it is not usually mentioned in the texts. The brevity, accuracy and impersonality of communicating certain information also affect the language of the professional style (Knittlová, 2010).

In the professional style, a high emphasis is placed on the accuracy of expression. Above all, impersonal forms are extensively used in the professional language, such as the verbal nouns – infinitive and gerund, which are translated into the Czech language using a subordinate clause, or a participle, and very often also usage of a passive voice is particularly typical. Almost no pronouns appear in the texts in the 1st person of the singular form (Knittlová, 2010).

The main component of each professional text is professional terms with high information content, such as very often used compounds. Furthermore, adverbs (*again, however*) are an integral part of such text, as well as prepositions and conjunctions that determine the relationships between words in a sentence (*after, upon, moreover, aside from, besides, after*). Author's attitude in the text is expressed mainly by phrases *"to be sure", "beyond doubt"* or *"of course"*, etc. To express probability in the English professional texts, there are widely used connections like *"probably", "perhaps", "possible", "apparently"*, and many more. Sentences are often introduced by *"in the first place", "basically", "more specifically", "to be more exact"* or *"with the exception of"*. Other typical phrases of professional English are, for example *"to a certain degree"***,** *"in general"* and *"take in account"*. For such connections, it is essential in translation to follow the meaning of the whole phrase, since the meaning of the connection may be very different from the meaning of its individual parts (Janata, 1999).

Compounds are frequently used in professional English texts. English, often referred to as "business English" or "international English", is today the modern *lingua franca* - the world's main international language of communication. That is why many new technical terms (very often in the form of compounds) are formed in it, which are then used by the whole world. However, there is also a powerful tendency in English to shorten these terms. Therefore, a large number of acronyms and abbreviations in English texts could be found (Krhutová, 2009).

Compounds in English are made up of at least two words, the basic word, and the word that specifies the basic word. These compounds are divided into compound terms with left or right attributes, also known as closed and open. In the first case, the compound expression arises by the gradual expansion of the word (*pocket-sized gadget* –kapesní zařízení, *family-run business* – rodinná firma, etc.). In the second case, the attribute stands behind the noun (*water tank* – vodní nádrž, *machine under-test* – testovaný stroj). Compounds can be almost indefinitely long. The opposite of long compound terms is short one-syllable words, which are also part of professional texts (Janata, 1999).

Another very typical part of professional texts is the use of Latin terms; the most typical are *ad verbum* - literally, *et cetera* - and so on, or *ex-post* - additionally. The gerund has to be mentioned, as it is used very frequently in English professional texts, perhaps

because they can perform the function of almost any member of the sentence. For translators, it is necessary not only to know these forms but also to be able to create them (Knittlová, 2010).

The "saving" form of English also includes the omission of words whose preservation is not essential for the meaning of the sentence, for example, "Doufá, *že* on dodrží slovo." – "She hopes he will keep his word." (where *že - that* is omitted) or "To je ta nejlepší věc, *co* jsem kdy viděl" – "That is the best thing I have ever seen" (where *co – what* is omitted).

There are also many "inconsistencies" in professional English, which are mainly related to vocabulary. There are several closely related terms between which the difference is not sufficiently defined (e.g. *plate – sheet*). Also, a dash/hyphen usage between individual parts of a phrase is not clearly defined. Other incomprehensibility could be caused by some differences between British and American English. Very often, the differences are factual and therefore significant for the professional text, there are also formal differences concerning mainly different word writing (Janata, 1999).

Tab. 1.1: Differences between British and American English

Czech equivalent	**British English**	**American English**
země, uzemnění	*earth*	*ground*
řídící páka	*gear lever*	*gearshift*
benzín	*petrol*	*gasoline*

2 TRANSLATION

2.1 Introduction

Dear students, you get to your hands an electronic textbook for the subject BNAO - Design of Analog Integrated Circuits. In this course, students are acquainted with CMOS technology and design of basic analogue integrated circuits. The subject requires basic knowledge of electronic components - especially MOS transistors and operational amplifiers. The introductory part of the script deals with the process of producing semiconductor chips and describes the various process steps, including illustrative images. This is followed by a detailed description of the MOS transistor principle, a malignant model, modes of operation, and important mathematical relationships needed for circuit design. Another part of the textbook is already devoted to the design of specific analogue circuits. It starts with current mirrors, which are virtually part of most complex circuits. Following are the current and voltage references, the differential pair. After a detailed introduction to the design and function of these basic circuits, there is a chapter dealing with operational amplifiers. The chapter describes the design principles of the operational amplifier to achieve the required parameters. The problem of their stability is described in detail. The last chapter describes the design of a chip layout.

2.1.1 Classification of the course in the study program

Course The design of analog integrated circuits is included in the bachelor study program in subjects of optional specializations of studies Microelectronics and Technology (summer semester of the 3rd year) and Electronics and Communication Technology (summer semester of the 2nd year) and also as an optional interdisciplinary course in summer semester of the 2nd year of the bachelor's degree program in Teleinformatics.

2.1.2 Entry test

Ex. 1: Determine the output voltage $\boldsymbol{U}_{\mathbf{OUT}}$ of the following circuits. Assume the ideal parameters of the components. $R = 100\ \Omega$. Calculate the current $\boldsymbol{I}_{\mathbf{D}}$ in the circuit b) and the current $\boldsymbol{I}_{\mathbf{R}}$ in circuits c) and d).

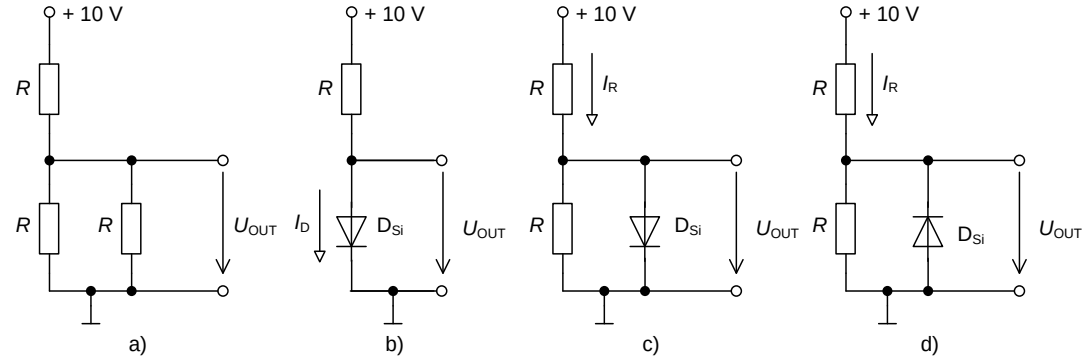


Fig. 1.1: Wiring diagrams for example 1

Ex. 2: Determine the amplitude $\boldsymbol{U_{OUT}}$ – **Fig. 1.2a.** C = 10 pF.

Ex. 3: Determine the frequency of the pole $\boldsymbol{f_P}$ in the circuit – **Fig. 1.2b**

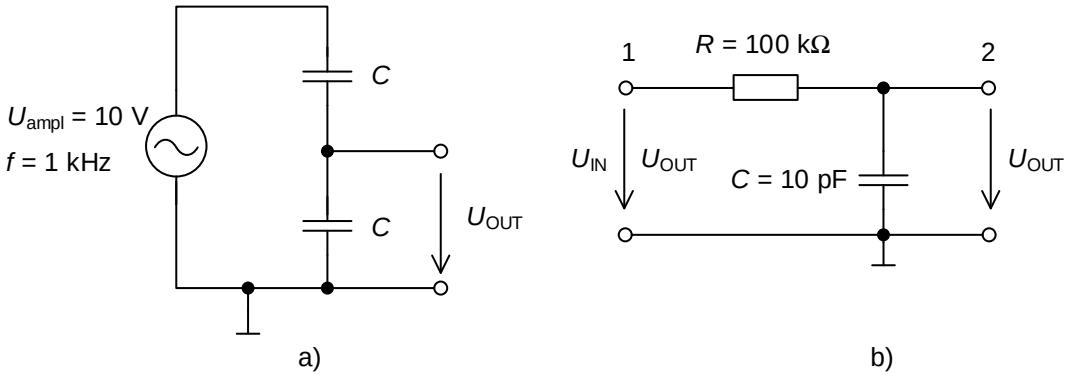


Fig. 1.2: Wiring diagrams for examples 2 and 3

Ex. 4: Calculate the output voltage U_{OUT1} and U_{OUT2}. Assume ideal transistors.

R = 100 Ω

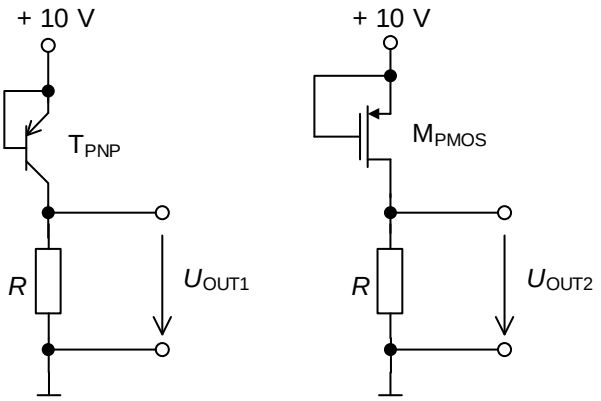


Fig. 1.3: Connection with transistors for example 4

Ex. 5: Calculate the output voltage U_{OUT} for each connection. Assume the ideal operational amplifiers.

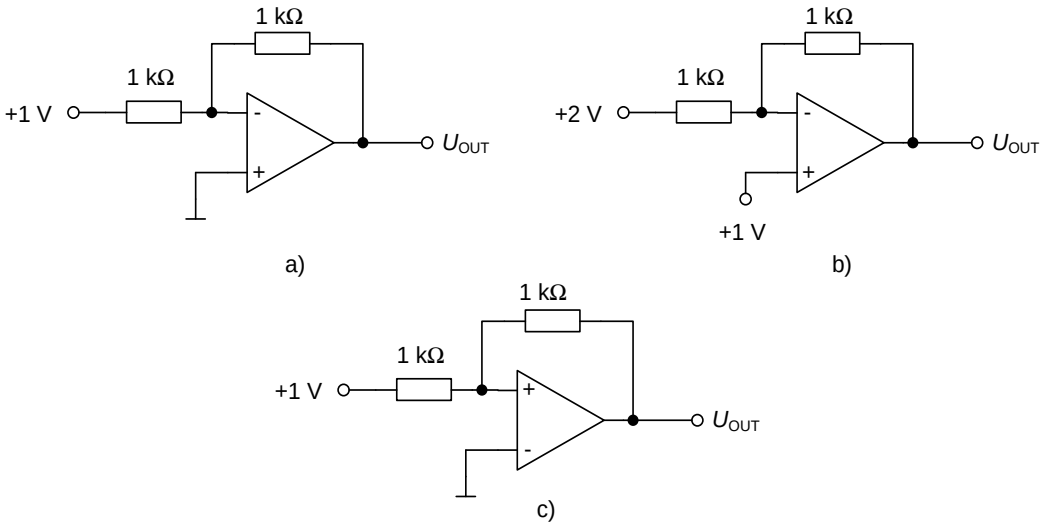


Fig. 1.4: Connection with operational amplifiers for example 5

2.2 CMOS technology

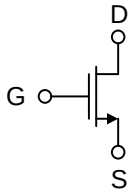
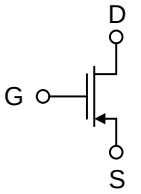
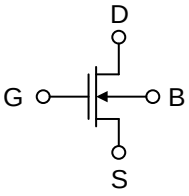
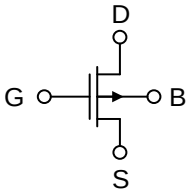
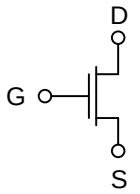
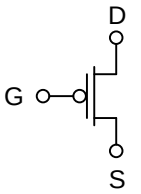
Nowadays, bipolar technology and CMOS (Complementary Metal Oxide Semiconductor) are the most widely used. In history, bipolar technology (operational amplifiers, TTL circuits) have dominated the field of silicon integrated circuits (IC)

In the 1970s, a number of circuits have been demonstrated in MOS technology – DRAM memories, microprocessors, and logic circuits series 4000. At the end of the 1970s, it was clear that MOS technology is the right direction for achieving high-density integration on the chip. Firstly, it was used for NMOS analogue and digital circuits. Then in the 1980s for CMOS technology. This technology, in addition to the high density of integration, also enabled low power consumption in digital IC. In contrast, bipolar technology provides many benefits in purely analogue IC. For example, many times higher transconductance at the same current. Therefore, bipolar technology is mainly used to design purely analogue ICs and CMOS technology is used to design purely digital ICs. However, integrated circuits often contain both parts – analogue and digital. For these cases, BiCMOS technology can be used, where it is possible to use bipolar and MOS transistors. However, in terms of the price of these ICs, it is better to use pure CMOS technology. These scripts are focused on CMOS technology only.

2.2.1 MOSFET transistor

Transistor MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is an electric field-controlled transistor. The conductivity of the channel between the source and drain electrodes is controlled by the potential connected between the gate and source terminals. The gate is isolated from the channel by a layer of silicon oxide (SiO2) - hence the name of the transistor type. The source and drain electrodes can be of type N and P, but both must be of the same type. If they are of type N, they are an NMOS transistor. Otherwise, if they are type P, it is a PMOS transistor.

Tab. 2.1: Symbols used for NMOS and PMOS transistors

	Transistor NMOS	Transistor PMOS
Bulk is connected to U_{SS} (NMOS), and to U_{DD} (PMOS)		
Bulk is not connected		
Digital model		

U_{DD} voltage is positive and U_{SS} negative supply voltage.

The name of the source electrode is derived from operating as the source of the charge carriers (N-type channel electrons and P-type channel holes) that pass through the channel. Similarly, the drain is called as the place where the carriers flow out from the channel.

When the MOS transistor is type N, the drain and source areas are of the N+ type ("+" signify a high dopant concentration) and the area under the gate is type P. If a positive voltage U_{GS} is connected between the gate and the source, an inverse layer of the N-type called channel is created under the gate. The channel connects the source-drain areas and allows the passage of electric charge carriers (electric current) between these areas. If the gate-to-source low voltage (less than the threshold) or negative is connected, the channel disappears and the charge carriers cannot pass between source-drain areas (the transistor is closed, the electrical current is not passing).

When the MOS transistor is type P, the drain and source areas are of the P+ type and the area under the gate is type N. If a negative voltage U_{GS} is connected between the gate and

the source, an inverse layer of the P-type called channel is created under the gate. The channel connects the source-drain areas and allows the passage of electric charge carriers (electric current) between these areas. If the gate-to-source higher voltage (higher than the threshold) or positive is connected, the channel disappears and the charge carriers cannot pass between source-drain areas (the transistor is closed, the electrical current is not passing).

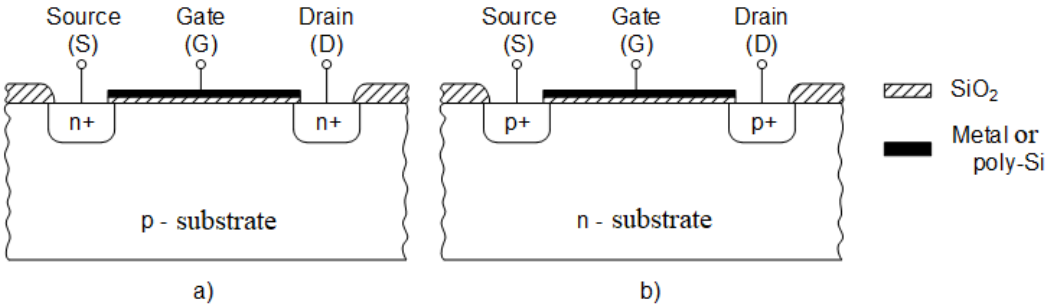


Fig. 2.1: a) NMOS b) PMOS Transistor structure

A condition for the amplification of the electrical signal is the power gain (this condition basically says that an element can amplify, only when it is able to amplify a voltage or current, or both). A component that can amplify current and voltage is, of course, highly desirable. The MOSFET transistor is such a component.

The current gain of the MOS transistor can be explained simply by the fact that MOS does not need any input current (and no current flows through the input terminal). Thus, the structure has a theoretically infinite DC current gain. Current gain is inversely proportional to the signal frequency and achieves unit gain at the transit frequency.

The voltage gain of the MOS transistor is due to current saturation in the area of higher drain-source voltage, so a small change in current will cause a large voltage change.

2.2.1.1 Structure and principle of the MOS transistor

The structure of the NMOS and PMOS transistor on one substrate (type P) is shown in Figure 2.2, where the length of the channel L is identical to the width of the channel W. The actual length of gate L is not the same with the required length of the gate, but closer to the distance of drain and source areas under the gate. The overlap between the gate area and the drain/source is important for providing a conductive path (channel) between

the drain-source. Usually, the aim is to make this overlap as small as possible - to minimize parasitic capacities.

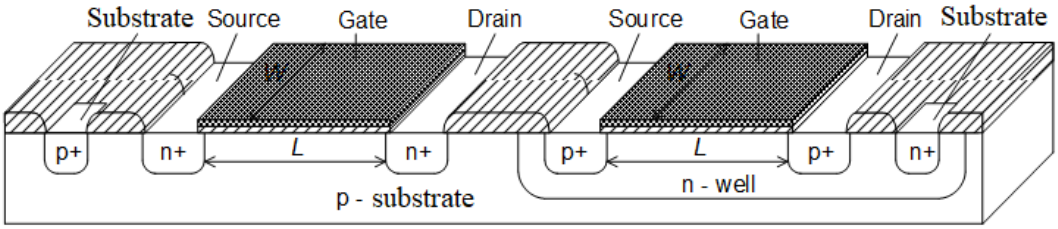


Fig. 2.2: The structure of the NMOS and PMOS transistors on a single substrate

The substrate contact is added to the structure shown in Fig 2.3. This must be connected so that the PN junction is always poled in the reverse bias configuration. Thus, the substrate contact to P+ to the lowest potential in the circuit (U_{NAP-}) and the substrate contact to N+ to the highest potential in the circuit (U_{NAP+}).

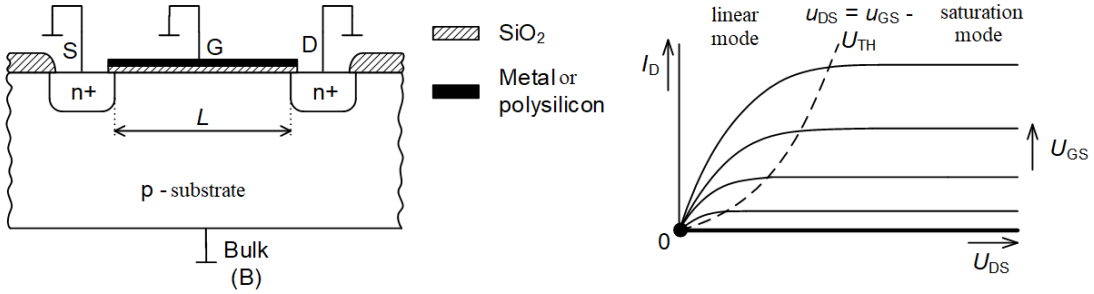


Fig. 2.3: NMOS transistor in the closed state

Figure 2.3 is the state where the gate, source, and drain are connected to the ground. There is no inverse layer beneath the gate - a conductive channel that allows the passage of electrical charge carriers between the drain and the source. The transistor is closed.

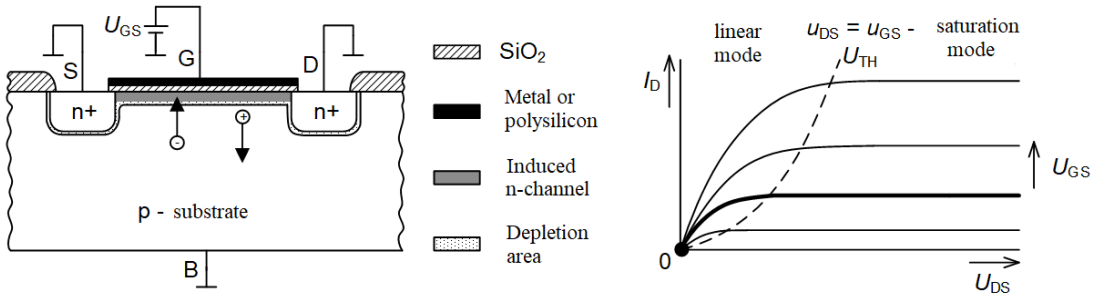


Fig. 2.4: Creating the inverse layer in the NMOS transistor

After connecting the positive voltage U_{GS}, the minority carriers (electrons) in the P-substrate are attracted, and majority carriers (holes) are expelled from the area under the gate (Fig. 2.4). Therefore, the N-type inversion layer, which connects the drain and source areas with the conductive channel, is formed below the gate. At the same time, under the dielectric-semiconductor interface, a depletion area is created.

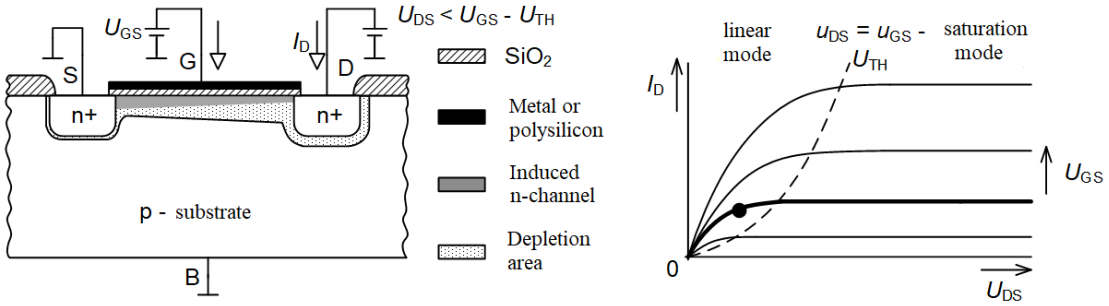


Fig. 2.5: NMOS transistor in linear mode

After the connection of the voltage U_{DS}, a current I_D starts to flow between the drain and the source areas (Figure 2.5). As the voltage U_{DS} increases, the potential difference between the drain and the gate decreases, and the channel narrows down on the drain electrode side and the depletion area is increased around the drain area. For small $U_{DS} < U_{GS} - U_{TH}$,

the current I_D increases linearly with the voltage U_{DS}. The transistor is in linear mode.

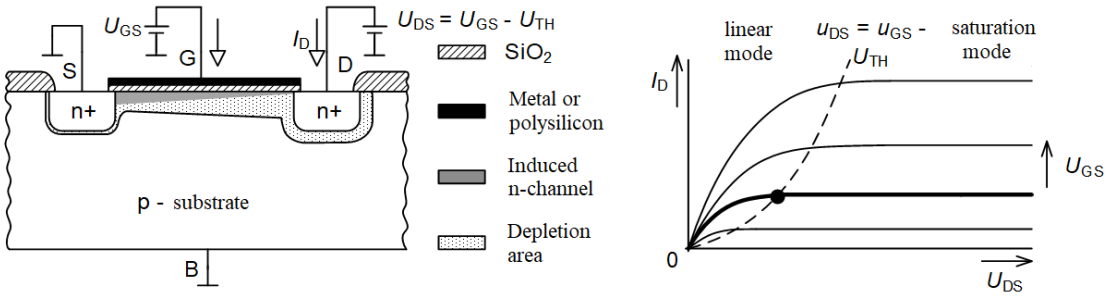


Fig. 2.6: NMOS transistor, the transition to saturation mode

If the voltage $U_{DS} = U_{GS} - U_{TH}$, then the channel closes on the drain side (pinched-off channel) and saturation of the current I_D occurs. However, the current flowing does not disappear but remains constant when the U_{DS} increases (Figure 2.6).

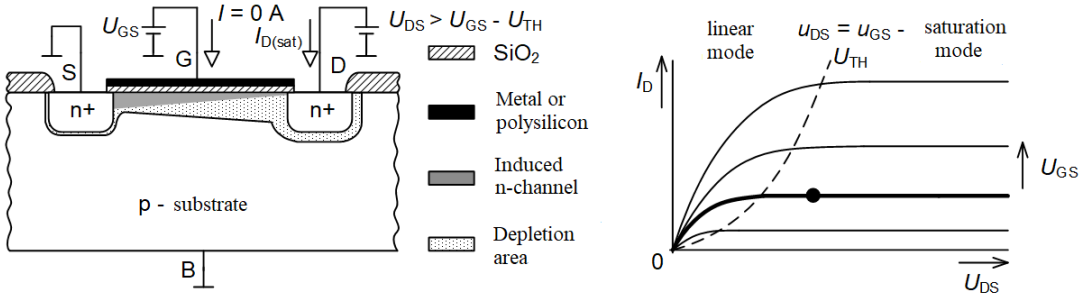


Fig. 2.7: NMOS transistor in saturation mode

With the increasing voltage U_{DS}, the current I_D is no longer changing. The transistor is in saturation mode (Figure 2.7).

2.2.2 Passive components

This chapter deals with the passive components used in the design of ICs that are compatible with CMOS manufacturing process technology. These components include resistors and capacitors.

2.2.2.1 Capacitors

Capacitors are used in analogue circuits such as filters, A/D and D/A converters, sampling circuits, compensation elements in the operational amplifiers, etc. The switching capacitor (SC) technology is also popular with the IC design. The characteristic features of the capacitors used in the above applications are

a) good matching,

b) high capacity per unit area,

c) low-temperature dependence,

d) good ratio of reached capacity and parasitic capacity.

The capacitor is implemented in the CMOS technology by the structure of two parallel (mostly superimposed) electrodes. The electrodes should be implemented as conductive layers that are available in the given technology (metal, polySi, diffusion). The insulating dielectric between the electrodes is usually made of silicon oxide (SiO2), silicon nitride (Si3N4) or polySiO2. In IC technologies, mostly occurred capacitors are formed between metallic layers (for example, metal3-metal2 at ONSemi I3T, metal6-metal5 at TSMC 180

nm, etc.), poly-poly or metal1(M1) – poly. Ideally, the capacity value should not be dependent on the ambient temperature and the applied voltage. Practically, it depends. This dependency is expressed by the parameters t_c (temperature) and v_c (voltage). Table 2.2 lists the parameters of capacitors from ONSemi I2T100 and I3T25 technologies.

Tab. 2.2: Overview of typical capacitors parameters in ONSemi technologies

Type	Technology	Capacitance [fF/µm^2]	Temperature dependence [ppm/°C]	Voltage dependence [ppm/V]
M1-poly	I2T100	0,75	-	25
poly-poly	I3T25	0,94	25	15
M3-M2 (MIMC)	I3T25	1,5	45,5	-32,03

The implementation of the on-chip capacitor itself has a considerable inaccuracy due to the technological deviations of the production process. For example, for I3T25 technology, the datasheet shows a typical capacity value of 1.5 fF / µm^2. However, the extreme values of the manufacturing process are 1.3 fF / µm^2 and 1.7 fF / µm^2, making the error up to ± 15%. In integrated circuits, the ratio of two or more capacitors is often used. This ratio can be realized with an accuracy of around 0.1%. The resulting accuracy of the ratio depends on the size of the capacitor surface ($W \cdot L$), the concurrency coefficient A [%·µm] and the chip topology. It holds that

$$\sigma^2\left(\frac{\Delta C}{C}\right) = \frac{A^2}{W \cdot L}.$$

In I3T25 technology, the capacitor has between M3-M2 a concurrency coefficient A = 1.48%·µm. For two capacitors, each of 1.5 pF (W·L = 1000 µm^2) is concurrence 0.04%.

This value assumes a well-designed topology (Chapter 8).

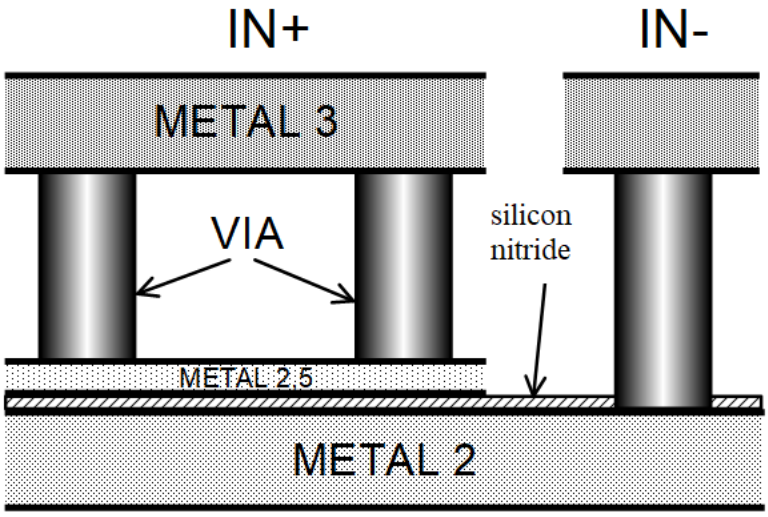


Fig. 2.8: Structure of the MIMC capacitor

Figure 2.8 shows the structure of the M3-M2 capacitor – MIMC (Metal – Insulator – Metal capacitor). Between the M3 and M1 layer, it is connected to the M2.5 over the VIA M3. In modern technologies, there are also structures of two capacitors superimposed connected in parallel. This will double the capacity per unit area.

2.2.2.2 Resistors

The main components used in the IC design are MOS transistors and capacitors. In some circuits, resistors are also used. These circuits include, for example, A/D and D/A converters, voltage dividers, and so on. In general, the resistor is formed by a layer (rectangle or stripe) of resistive material which at its ends is contacted with the layer of metal 1. The actual body of the resistor is electrically insulated from the substrate (washer) using an oxide semiconductor layer or transition in the reverse direction/bias. When the so-called square resistance - R □ is introduced as a parameter, then the total resistance of the resistor will be determined as

$$R = R \quad \frac{L}{W} + 2R_{kont},$$

where R_{kont} is the contact resistance, which is in units of Ω and can be neglected.

The most widely used resistor that efficiently utilizes space in the IC design is a PolySi-based resistor. The value of its resistance per square is in the range of hundreds of Ω to kΩ units - for resistor HIPOR (Hi-Ohmic polySi - without salicidation)

and in the order of Ω units for resistor LOPOR (Low-Ohmic polySi - with salicidation).

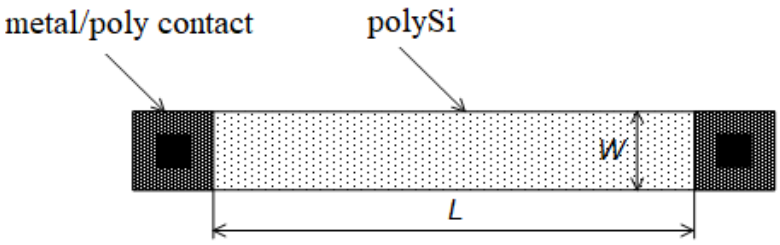


Fig. 2.9: Resistor made by a polySi layer

Another type of resistors are resistors formed by diffusion - N+ or P+. These resistors achieve less square resistance than HIPOR ones.

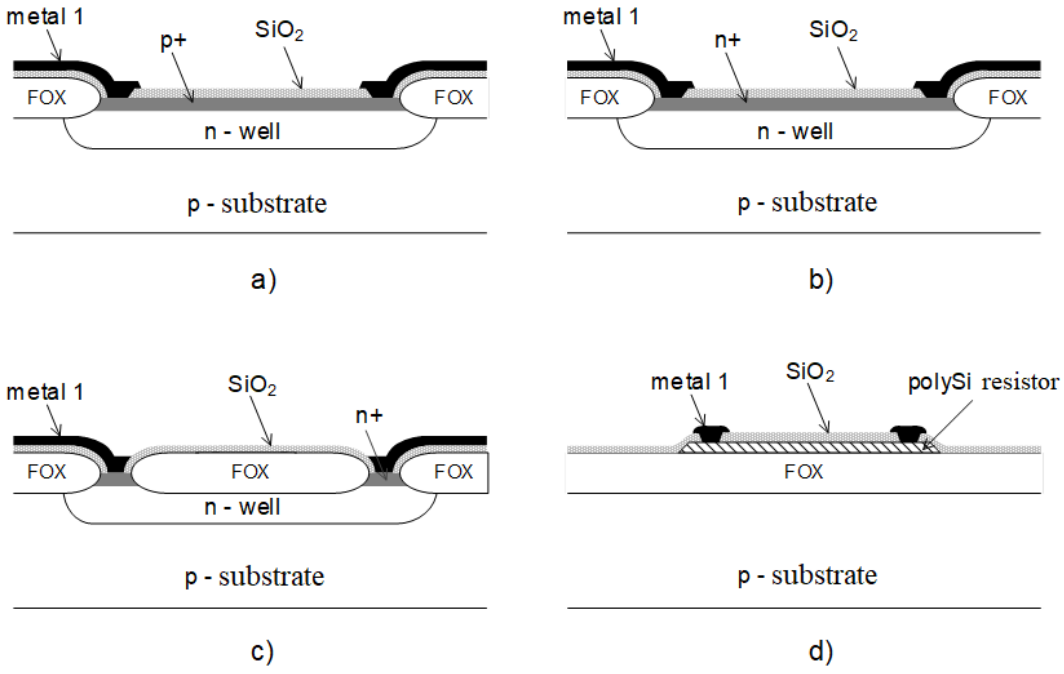


Fig 2.10: Resistor formed by a) P+ diffusion, b) N+ diffusion,

c) the n-well, d) the PolySi layer

Structures using polySi can better cope with shielding problems. PolySi is not sunk directly in the substrate, and so these parasitic capacities are much smaller than in the case of a resistor made by a diffusion. A pit can be used for shielding (need to be polarized properly). Even better shielding is achieved if the resistor is formed from the polySi 2 layer and the polySi 1 layer is used to shield together with the pit.

Tab. 2.3: Overview of typical parameters of some resistors in ONSemi technologies

Type	ONSemi technology	Resistance [Ω/□]	Temperature dependence [ppm/°C]
Nwell	I2T100	1300	4900
P+	I2T100	96	1300
N+	I2T100	67,5	1400
HIPOR	I2T100	1825	-2100
HIPOR	I2T25	975	-1420
LOPOR	I2T25	2,4	3470

As with capacitors, the inaccuracy of the resistors with respect to the nominal value due to technological deviations from the manufacturing process is considerable. For example, for I3T25, the datasheet shows a typical HIPOR resistance value of 975 Ω/□. However, the extreme manufacturing process values are 775 Ω/□ and 1175 Ω/□, which means an error of up to ± 20%. Also, the ratio of two or more resistors is often used. This ratio can be realized with an accuracy of around 0.1%. The resulting accuracy of the ratio depends on the size of the resistor surface ($W \cdot L$), the concurrency coefficient A [%·µm] and the chip topology. As with capacitors, equation (1) holds for concurrency.

2.2.3 CMOS manufacturing process

The production of semiconductor chips consists of several process steps. To understand the entire manufacturing process of semiconductor chips, it is necessary to know the following procedural steps. These include oxidation, diffusion, deposition, ion implementation, and etching. An important process is photolithography, which is used to prepare topologically defined structures by curing the exposed photoresist on a prepared sample and delimits areas that will be in the next technological step, subject to local operations.

The basis for semiconductor chips production is a single-crystal semiconductor (Si, Ge or GaAs) with high purity. The most common monocrystalline semiconductors are

produced using the Czochralski process (which was discovered in 1917). The input of polycrystalline silicon with the addition of a small amount of dopant which determines the electrical properties of the resulting product is melted in a quartz crucible, and a monocrystalline seed is immersed in the melt. By regulating the drawing speed, the melt temperature, the revolutions, and a number of other technological parameters, the silicon atoms are gradually built into precisely defined positions in the crystal lattice (100 or 111) and form a monocrystal of the required diameter (75 mm - 450 mm) and properties. The resultant product is a silicon monocrystal (ingot), which is then cut into 300 μm thick slices (160 μm is planned in the future). Silicon wafers are alloyed with boron, phosphorus, arsenic or antimony. According to the cut parts of the wafer, it is possible to recognize its crystallographic orientation and type (Fig. 2.11).

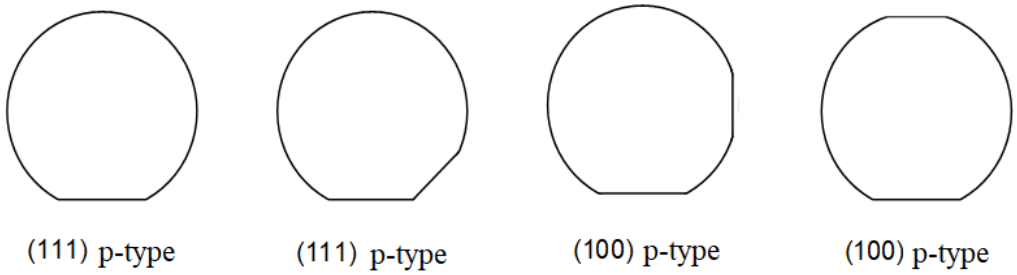


Fig. 2.11: Wafer types and their crystallographic orientation

The five basic procedural steps are described in the following sections (oxidation, diffusion, ion implementation, deposition, and etching).

2.2.3.1 Oxidation

The first basic process step is oxide growth or oxidation. Oxidation is the process of forming the SiO_2 layer on the silicon wafer surface. Oxide increases not only on the surface of the wafer but also partly below the surface of the silicon wafer.

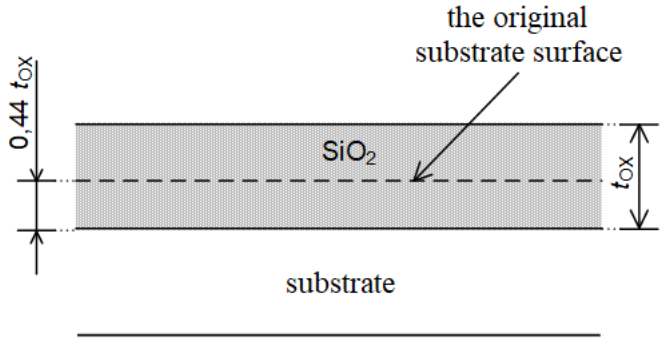


Fig. 2.12: Increase in oxide on the wafer surface

Typically, 56% of the oxide is above the original surface and 44% under the original surface. Oxide thickness, referred to as t_{OX}, can grow by dry (equation 2.3) or wet oxidation in water vapour (equation 2.4) to achieve a minimum defect density.

$$Si + O_2 \longrightarrow SiO_2, \tag{2.1}$$

$$Si + H_2O \longrightarrow SiO_2 + H_2. \tag{2.2}$$

The oxide thickness ranges from the nm units of gate oxides (for example, I2T100 t_{OX} = 17.5 nm) to hundreds of nm of insulation oxides (FOX). The oxidation takes place at temperatures of 700-1100 ° C and is proportional to the thickness of the oxidation layer - provided that it is always done for the same period.

2.2.3.2 Diffusion

The second process step is diffusion. Diffusion is a chemical process that occurs when the wafer is heated to 800-1400 ° C (melting point of Si is 1415 ° C) and when exposed to the vapour of the dopant. The dopant atoms in this process move to an area of lower concentration - the doping gas is allowed to act as long as the doping molecules penetrate to the required depth. To achieve greater depth after diffusion, the distribution of the doped atoms to the depth and to the width follows. The total depth of diffusion varies from 0.1 μm to 10 μm or more. Figure 2.13 shows two graphs of admixture concentrations depending on the penetration depth for different times of exposure. The first Fig. 2.13a shows a diffusion graph from a source with an infinite number of dopants and Fig. 2.13b with a limited amount of dopants. Concentration N_0 is the concentration on the substrate surface. With increasing depth, the concentration decreases.

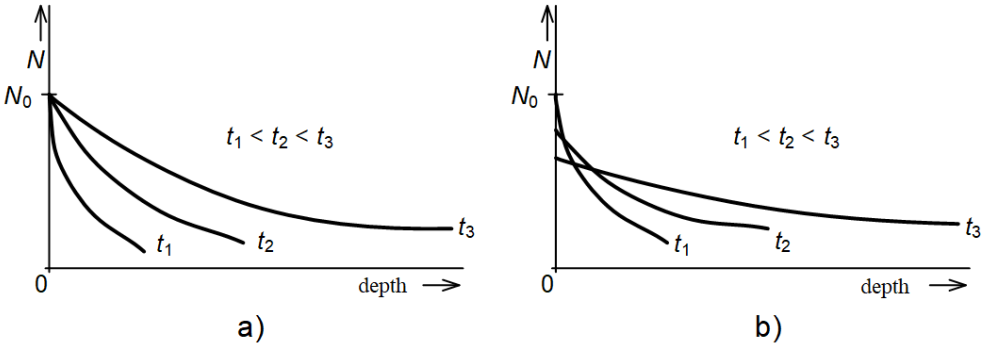


Fig. 2.13: Dependence of admixture concentration on the depth of penetration for different times a) source with infinite quantity b) limited amount of dopants

The concentration N_0 in Fig. 2.13a is constant (infinite source of dopants). In Fig 2.13b, due to the finite number of dopants with increasing time and depth, the concentration N_0 is decreasing.

For diffusion, it is necessary to ensure high concentration, respectively the rate of concentration of the diffusion additive (P, As, Sb - donor-type admixtures in silicon, B, Al, Ga - acceptor type admixtures) and supply the necessary energy - the diffusion of the admixtures takes place in the reactors at high temperatures.

2.2.3.3 Ion implantation

Another process step is ion implantation, which is very often used in the production of MOS components. In ion implantation, the ions of the dopant are accelerated by the electric field and implemented into the substrate in order to alter the electrical properties. This process is being done at low pressure. The average depth of penetration is from 0.1 to 0.6 μm, depending on the speed and angle of ion impinging on the substrate. The impinging angle is chosen outside the substrate grid axis to collide with the substrate crystal lattice atoms to prevent the unwanted channel effect. The disadvantage is that the impinging angle is too acute (less than 90°) and the mask applied shades to some substrate locations. Another way to prevent the channel effect is to use a thick layer of SiO_2 through which the dopant ions are fired. The SiO2 layer changes the dopant penetration direction randomly before penetrating into the substrate. The ion implantation process causes disruption of the crystal lattice of the substrate, and many implanted ions are thus electrically inactive. This damage can be corrected by annealing at about 800 ° C. The

concentration profile of the implanted admixture is shown in Fig. 2.14. Unlike diffusion, the highest concentration of admixture is not present at the surface, respectively at the point where the diffusion takes place, but at a certain depth below the surface, which can be controlled by the energy of impinged ions.

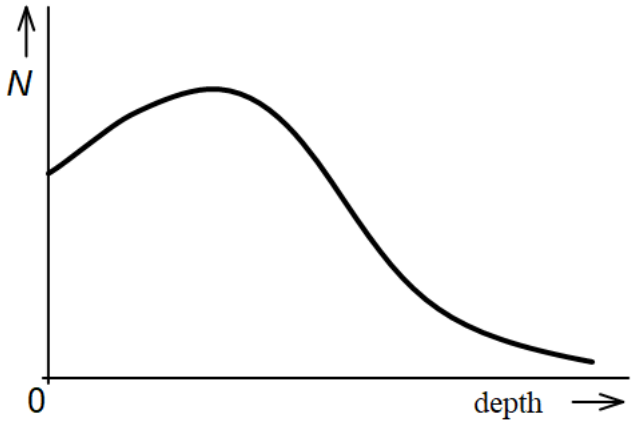


Fig. 2.14: The concentration profile of implanted dopants depending on the depth of penetration

The advantage of ion implantation compared to diffusion is precise dopant dose control (± 5%), excellent reproducibility and accurate depth control. Thus, it is possible to adjust the threshold voltage of the transistor or to create precise resistors. Another advantage is that ion implantation takes place at room temperature. It is only necessary to use a high temperature during the subsequent repair of the crystal lattice of the substrate by annealing.

2.2.3.4 Deposition

A deposition is a chemical process used to prepare thin films of various materials on a silicon wafer. Thin films can be prepared by various techniques – for example, by vapouring, sputtering or chemical vapour deposition (CVD).

During the deposition by vapouring, the solid material is placed in a vacuum and heated (high-frequency, ionic heating) until it starts to evaporate. The evaporated molecules hit the cold wafer and condense on the surface of the wafer in a thin film. The thickness of the applied film depends on the temperature and the time of vapouring. This technique requires a vacuum. Sputtering can be accomplished, for example, by a magnetron, ion, or

cathode. In general, it is the application of atoms of material (Al, Cu) to the contacts of the chip (anode) of energy that emit these atoms from the target (cathode). These atoms are carried on the substrate due to the electric field between the material and the plate. This technology does not place high demands on temperature and pressure, as in the case of vapour deposition. It is controlled by the voltage and pressure (not need such a high vacuum as in vapour deposition).

Chemical Vapor Deposition (CVD) is the technological process of forming thin layers, which utilizes a chemical reaction in the gas phase. These may be reactions between multiple precursors or a decomposition reaction of one substance. The reaction product subsequently forms a thin layer on the substrate. The CVD method takes place at elevated temperature, and the by-products of the chemical processes are vacuum aspirated or removed by a gas stream. However, it usually takes place at atmospheric pressure, but can also at low vacuum (referred to as LPCVD - Low-Pressure CVD). This type of deposition is mainly used to form layers of polySi, SiO2 or Si3N4.

2.2.3.5 Etching

The etching is the process of removing exposed material. The photolithography technique described in the next chapter is used to determine which parts of the material will be removed and which parts will stay. In Fig. 2.15a there are three layers of material - top protective layer (mask), then below there is a thin film of the deposited material. The bottom layer is a substrate. The goal of etching is to remove only a film unprotected by the mask. The etching process must have two essential properties. First, the selectivity (S) - the etching process must act only on the desired layer (thin film) and must not affect the mask or substrate. The selectivity can be evaluated as the ratio of the etching rate of the desired layer and the undesired layer

$$S_{A-B} = \frac{desired\ layer\ etching\ rate}{undesired\ layer\ etching\ rate}. \tag{2.3}$$

The second important feature is anisotropy (A). Maximum anisotropy - one direction of rapid etching (value 1), is required. Anisotropy can be categorized as

$$A = 1 - \frac{side\ etching\ rate}{vertical\ etching\ rate}. \tag{2.4}$$

In practice, neither perfect selectivity nor anisotropy can be achieved, resulting in the etching of a part of the mask and the bottom layer part (Fig. 2.15b). The dimension x_a shows what part of the mask was etched and x_b what part of the bottom layer was etched (non-ideal selectivity). The y_c dimension shows the underetched part under the mask layer - related to non-ideal anisotropy. Thin film etched materials (Figure 2.15) include polySi, SiO_2, Si_3N_4 and aluminium.

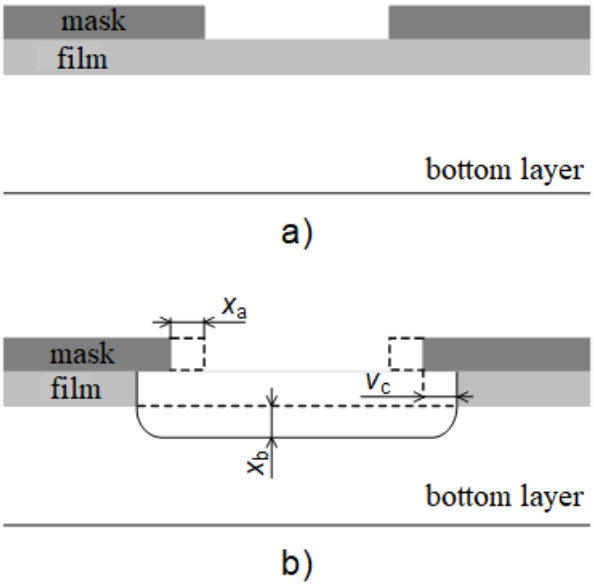


Fig. 2.15: Etching process

There are two basic types of etching - wet and dry etching. Wet etching uses chemicals that etch the desired material. Hydrofluoric acid (HF) is used for etching SiO_2, phosphoric acid for etching Si_3N_4. Nitric, acetic or hydrofluoric acid is used to remove polySi, potassium hydroxide for silicon, and phosphoric acid mixtures to remove metallic layers. The wet etching process is heavily dependent on exposure time and temperature.

Dry etching uses ionized gases. The emergence and development of dry etching processes required increasing miniaturization in microtechnologies (as well as nanotechnologies) because wet etching processes do not meet submicron dimensions (selectivity, anisotropy). Dry etching is characterized by excellent anisotropy (no overetching) and is therefore used for submicron technology.

2.2.3.6 Photolithography

Most of the basic process steps in semiconductor chip manufacturing are applied only to the selected wafer, except for oxidation and deposition. Selected parts can be defined using photolithography. The essential component of photolithography is a photoresist and a photomask that covers some parts from UV radiation. All ICs consist of different layers, which together form part structures. Each layer must be geometrically defined. These layers are formed on a large scale and then optically adjusted to the desired size on the wafer.

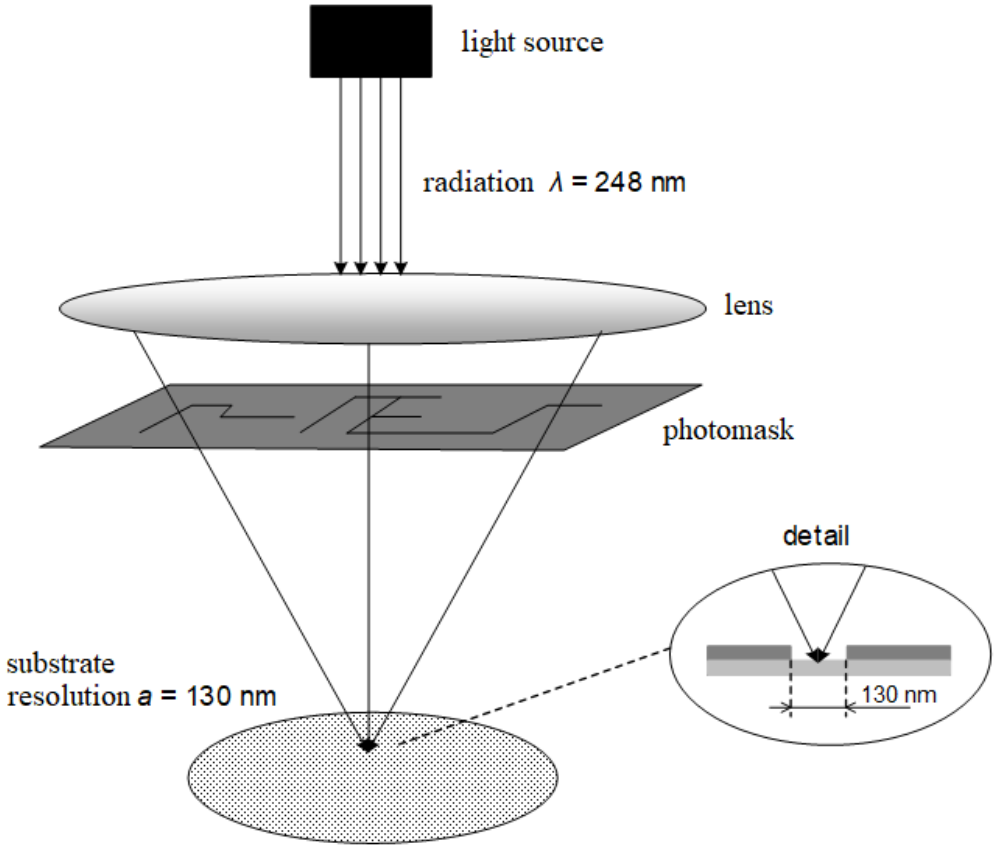


Fig. 2.16: Principle of photolithography

The minimum size (resolution) that can be implemented using the principle shown in Figure 2.16 is defined

$$M = \frac{c_1 \cdot \lambda}{NA}, \tag{2.5}$$

where M is the resolution, λ is the wavelength of the emitted UV radiation, c_1 is the index dependent on the particular photolithography device (values ranges from 0.5 to 1) and *NA* (numerical aperture). Numerical aperture expresses the effective aperture of the lens. It is a dimensionless number that can be expressed as

$$NA = n \cdot \sin(\theta), \tag{2.6}$$

where *n* is the refractive index in the space between the lens and the wafer (through which the radiation passes), Θ is the maximum angle of incidence of light (Fig. 2.17). The higher the numerical aperture, the higher the resolution of the lens and the greater the magnification (equation 2.7)

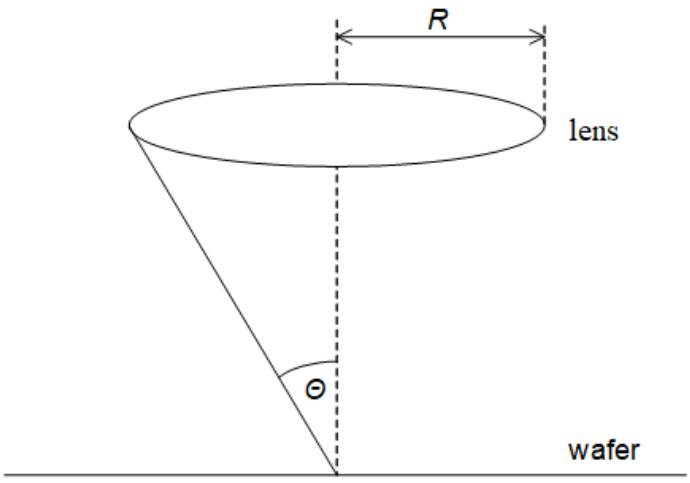


Fig. 2.17: The refractive index in the space between the lens and the wafer

The photoresist is an organic polymer that reacts by changing its structure when exposed to UV radiation. The photoresist may be positive or negative. The positive photoresist exposed parts are etched (irradiation breaks the polymer chains). The negative photoresist exposed parts remain (cross-linking and curing occurs by photochemical reaction).

The first step in photolithography is to apply a drop of photoresist to the surface of the layer, which has to be selected. When applying a photoresist, the wafer is rotated at a thousand revolutions per minute, thereby achieving a uniform stratification photoresist. Then the photoresist is cured at 85 to 90 ° C for about 3 minutes (soft-bake). The next

step is exposure - irradiation (by UV radiation) of the photoresist through the mask. The process of exposure and subsequent selective etching of the photoresist is referred to as induction. The remaining photoresist is cured at 110 ° C (hard-bake).

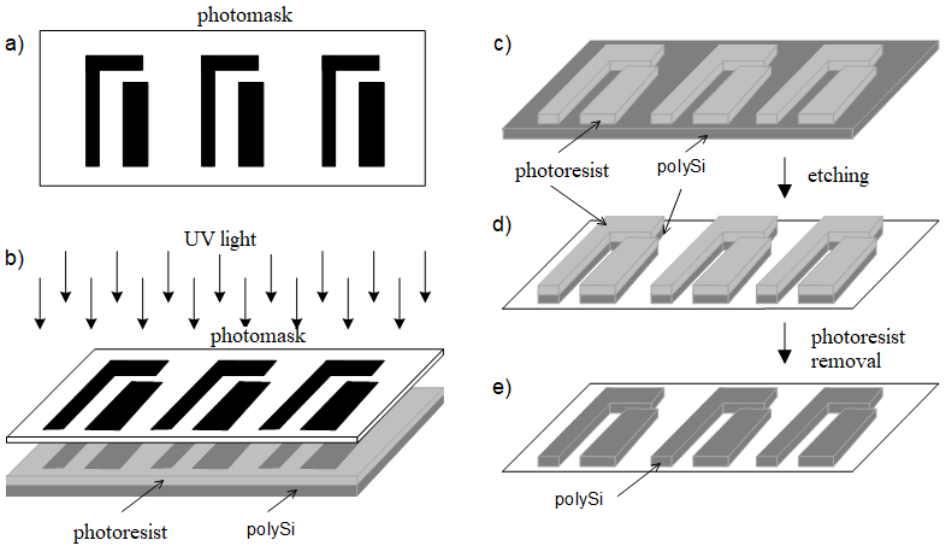


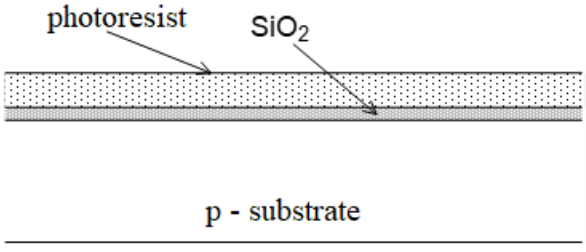
Fig. 2.18: Basic steps of photolithography to create polySi geometry: a) photomask, b) enlightenment, c) invocation, d) etching, e) photoresist removal

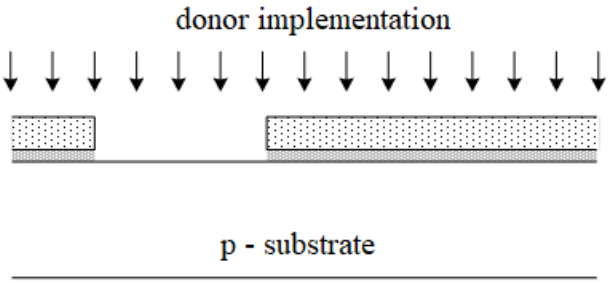
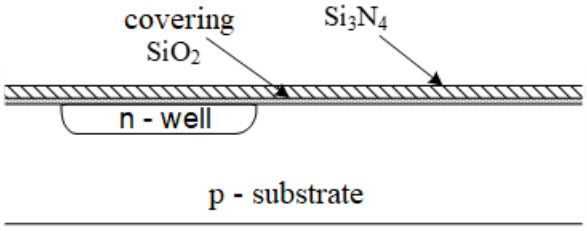
The above Fig. 2.18 illustrates the basic steps of photolithography, where the geometric shapes are formed in the layer of polySi.

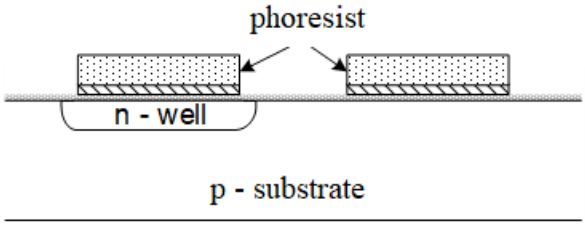
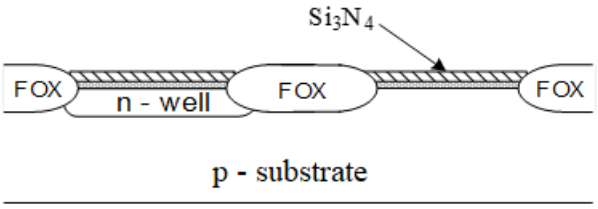
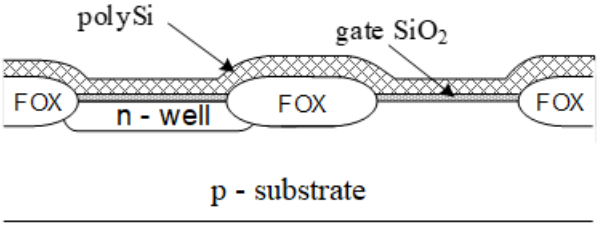
2.2.3.7 The manufacturing process of MOS transistor in n-well technology

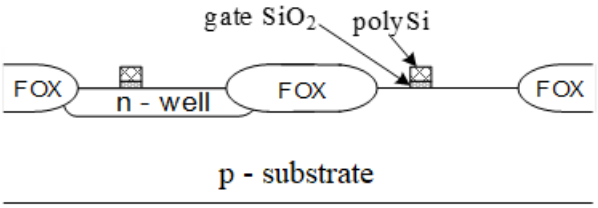
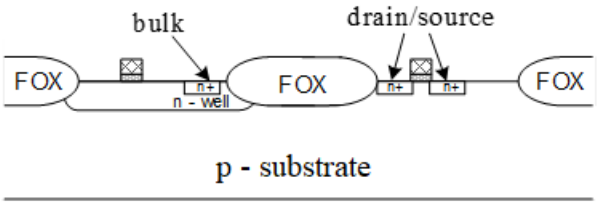
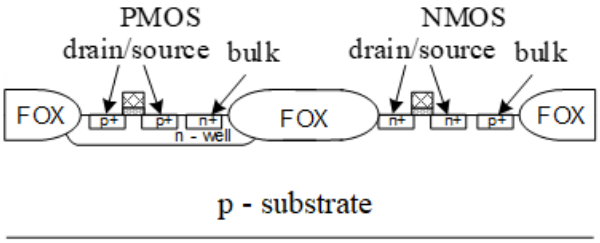
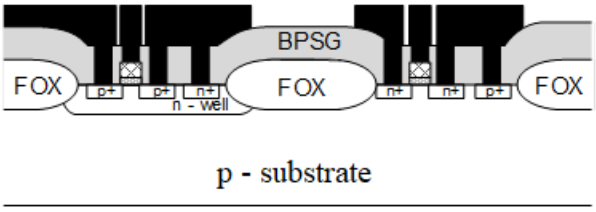
The manufacturing process of PMOS and NMOS will be shown in this chapter. Individual process steps such as oxidation, diffusion, etc. have been described in the previous chapters. An example of the technological process is simplified [2].

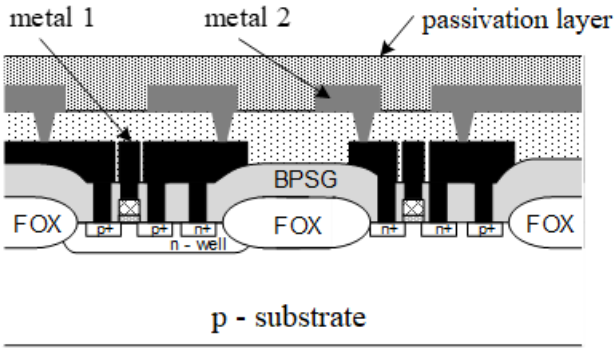
Fig. 2.4: Manufacturing process of NMOS transistor in n-well technology

1.	The first step is the growth of a thin layer of SiO_2 (by oxidation) on the surface of the p-substrate (wafer). A	

	photoresist is deposited on the SiO_2 layer by deposition.	
2.	The lithographic process of the first mask and etching over the areas of the next transistors with the P channel removes the photoresist and subsequently SiO_2 (using an n-well mask), and by ion implantation, a donor (five valence electron element – phosphorus, arsenic, antimony) is implanted on the wafer surface.	
3.	N-well is created for the PMOS transistor. In the next step, both the photoresist and SiO_2 are removed, and the thermal diffusion at high temperatures causes the donors to distribute into p-substrate. After that, the original SiO_2 is removed, followed by a thin layer of SiO_2 (protects the substrate from the stress caused by differential thermal expansion of the silicon substrate and silicon nitride Si_3N_4) and the Si_3N_4 layer is	

	deposited throughout the wafer.	
4.	Subsequently, a photoresist is deposited and removed by means of a lithographic process at the locations where the active regions (MOS transistors) will be located. Then, Si_3N_4 and the rest of the photoresist are also selectively removed.	
5.	Due to the isolation of the active moieties, a relatively thick layer of insulating oxide (FOX) grows in the next step by oxidation in places that are not covered by Si_3N_4 (which prevents oxide growth). FOX growth extends below the Si_3N_4 boundary and the active region narrows.	
6.	The remaining Si3N4 is removed, and the thin SiO2 layer will form a gate oxide. A polySi is applied throughout the wafer layer by deposition, which is needed to form the transistor gate. The applied polySi is heavily	

	doped to achieve good conductivity.	
7.	Using a photolithographic process, polySi and gate oxide are removed. It is left only where the gate electrodes will be located.	
8.	Subsequently, the entire wafer is covered with a photoresist. Then, using photolithography results in uncovering places where the n+ regions (source, drain, bulk) are created by means of diffusion or ion implementation.	
9.	Again, the entire wafer is covered with a photoresist. Then, using photolithography results in uncovering places where the p+ regions (source, drain, bulk) are created by means of diffusion or ion implementation.	
10.	The entire chip is covered with a thick oxide layer. This layer is usually borophosphosilicate glass (BPSG), which has a low melting point. In places	

	where contacts are to be found, holes in the BPSG are created using the photolithography process and etching. Subsequently, the remaining photoresist is etched, and a metal 1 layer (aluminium or aluminium/ copper compound) is deposited throughout the chip by deposition. Again, using the photolithographic process and etching, only the required metal paths remain on the wafer.	
11.	For the preparation of the second metal layer, another layer of dielectric material is applied - most commonly sandwich structure SiO2 + glass (SOG) + SiO2. Through the photolithography process and etching, holes are created in the sandwich structure for inter-metallic jumpers (via). As with the metal 1 layer, metal 2 is deposited and by using the same followed process, only required metal 2 connection will remain. If no metallic layer follows, a	

	protective passivation layer is applied - SiO_2 or SiN_3.	

3 Analytical part

3.1 Source text analysis

The translated text is called *Design of Analog Integrated Circuits* and was written by Ing. Vilém Kledrowetz, Ph.D. and doc. Ing. Jiří Háze. Ph.D, who is also a supervisor of this course. They are experts in this particular electrotechnical field, which is reflected in the vocabulary used and the style in which the textbook is written. The text matches the properties of professional discourse. It is characterized by using a codified language and vocabulary from a particular field of science or engineering. The discourse focuses on various methods of delivering scientific ideas and thoughts to a diverse range of audiences. The author's opinion is practically omitted in contrary to the Czech professional discourse, where the author's opinion on the given issue is expressed significantly.

The text is written mainly for educational purposes. Therefore, the recipients are university students of the course named Design of Analog Integrated Circuits. The primary purpose of this text is to inform and educate the students in the field of microelectronics.

3.1.1 Horizontal dividing of text

A typical horizontal division is a division into main chapters as an introduction, main part (there can be more main parts), and conclusion. These main chapters are divided into subchapters, and these subchapters can be divided into their own subchapters. The number of chapter levels depends on the total size of the text.

The *Design of Analog Integrated Circuits* is following this typical horizontal structure. The translated text consists of three levels of chapters. The whole textbook starts with a short introduction explaining the content briefly and the requirements of the course, followed by an entry test. Then, every chapter is dedicated to any course problem developed further by subchapters explaining more details.

3.1.2 Vertical dividing of text

A vertical dividing of text is represented by specific tools. The text is usually accompanied by footnotes, explanatory notes or critical apparatus. A font size, crossover, italics, underline, different line spacing, parentheses, etc. are used to distinguish relevant and less important information in the text.

Examples of usage in this text are graphs, schemes and text division using the numbers (or letters).

3.2 Translated text analysis

This chapter will analyse the differences between source text (ST) and translated text (TT) and used devices in the style of science and technology.

3.2.1 Used translation procedures analysis

The translation procedures were presented in the practical part of this thesis and are further analysed in this part.

1) **Equivalence** - expressing a term by different structural or stylistic means. Some SL words are culturally very specific, and it would be misunderstood in TL's cultural context. In such cases, the use of a functional equivalent, i.e. a term that is culturally non-specific, is used.

   V 70-tých letech – In 1970s: The 1970s form of expressing time period is culturally specific to English speaking countries only. There is no such short form in the Czech language. In Czech, it is necessary to proceed to a definitive version of the expression of the time period, which is also the most accurate translation.

   návrh - design

   subject - předmět

   voltage – napětí

   circuit – obvod

   component – součástka

2) **Transposition** - when transposing, grammatical changes are necessary due to a different language system.

Následuje kapitola – There is a chapter: a situation where a literal translation is possible, but in a given case, it is not in accordance with TL.

3) **Modulation** - is a variation by changing perspective (point of view). It is used when a literal translation is not appropriate.

   zesíťování – cross-linking: refers to a chemical bond of one polymer chain to another. Czech word probably refers to the graphical representation of a polymer chain, as it looks like a *web – síť*, but something as *dewebbing* would not be appropriate.

4) **Borrowing** – words adopted by one language from another language and normally used.

   amplituda – amplitude

   frekvence – frequency

   tranzistor – transistor

   rezistor – resistor

   depozice – deposition

   wafer – wafer

   substrát - substrate

5) **Calque** – literal translation word (word-for-word).

   zesilovač – amplifier

   vlnová délka – wavelength

   krystalová mřížka – crystal lattice

6) **Reordering** – change of word order or sentence structure.

   Realizace samotného kapacitoru na čipu - The implementation of the on-chip capacitor

7) **Reduction** – omitting the redundant element

   výrobní process technologie CMOS – CMOS manufacturing process: the word *technologie – technology* was omitted as it does not need to be specified. The word order is changed so it can be considered as reordering as well.

3.2.2 Lexical analysis

This part will deal with analysis from a lexical point of view.

3.2.2.1 Transition words

The use of a large number of transition words contributes to the logical continuity of individual statements and to the organized structure and hierarchy of the text. Thanks to them, the text is coherent and clear.

ST: *"Často však je na IO jak analogová tak digitální část."*

TT: *"However, integrated circuits often contain both parts – analogue and digital."*

This transition word "*However"* reinforces ideas, and express agreement with preceding material.

ST: *"Naopak bipolární technologie poskytuje mnoho výhod v čistě analogových IO."*

TT: *"In contrast, bipolar technology provides many benefits in purely analog IC."*

In this case, the transition phrase "in contrast" express that there is evidence to the contrary or point out alternatives.

ST: *"Oxidace probíhá při teplotách 700 až 1100 °C a je úměrná tloušťce oxidační vrstvy – za předpokladu, že vždy probíhá po stejnou dobu."*

TT: *"The oxidation takes place at temperatures of 700-1100 ° C and is proportional to the thickness of the oxidation layer - provided that it is always done for the same period."*

This transitional phrase present specific condition.

ST: *"Obecně se jedná o nanášení atomů…"*

TT: *"In general, it is the application of atoms…"*

This transitional device is used to introduce an example, supporting the information stated in the previous sentence.

ST: "Struktura má tedy teoreticky nekonečné velké stejnosměrné proudové zesílení."

TT: "*Thus*, the structure has a theoretically infinite DC current gain."

"Thus" in this case serves the purpose of showing that there is a consequence or an effect after what was stated in the previous sentence. It has infinite DC current gain, because MOS does not require any input current.

3.2.2.2 Terminology

Terminology is an integral part of any scientific discipline, and special attention needs to be paid to translating it. The science and technology style records exact science information. Therefore, it is vital to ensure that the terms used are exact - to be clear and accurate. The book "*O české terminologii*" states that terms are usually context-independent and can, therefore, be also used separately. The terminology of each field is closely related to the history of the industry. The terms are continually being updated, usually by linguists, who are also experts in the field and theory. The terms may be completely new, or the meaning in the field may be reduced. (Poštolková, 1983)

As this text written in the style of science and technology contains a large number of general technical terms from the field of electrical engineering, it also contains few branch-specific terms related to the microelectronic field of study.

Krhutová (2009) classified terms used in electrical engineering into three groups:

1) General scientific terms (analyze, classify, research)
2) General technical terms (semiconductor, operational system)
3) Branch-specific electrotechnical terms (cache, output stage, Fortran)

Few of these terms are shown in the following figures.

Tab. 3.1: General technical terms

Czech	**English**
tranzistor	*transistor*
napětí	*voltage*
odpor, rezistor	*resistor*
obvod	*circuit*
kondenzátor	*capacitor*
zesilovač	*amplifier*
usměrňovač	*rectifier*

Tab. 3.2: Branch-specific terms used in microelectronics

Czech	English
wafer	*wafer*
fotomaska	*photomask*
fotolitografie	*photolithography*
difůze	*diffusion*
depozice	*deposition*

Most of these terms are loanwords, as they were adopted from English and incorporated into the Czech language without translation. These new words are very often taken into Czech and used as the only way to express some things or are used as synonyms of Czech equivalents. Typical loanwords here could be *transistor* (translated as a *transistor*) or *resistor* (translated as *rezistor* or sometimes as *odpor* – but it refers rather to the word *resistance* – it's use in the communication can be specified as a professional slang). Another example is word *capacitor* – in czech *kondenzátor*, but also *kapacitor* as well. In fact, *kondenzátor* is a passive electrotechnical component, but it also represents the heat exchanger used for cooling and converting steam (condensation) in the different scientific field, so it has context-based multiple meanings.

The branch-specific terms include more specific information. Therefore, these are used in the texts for experts in individual disciplines and can be understood by highly instructed readers. Illustrated examples in Fig. 4-2, such as *diffusion* or *deposition*, are referring to the chemistry field of study, but are also used in microelectronics when describing the manufacturing process of the integrated circuits.

Terms occurrence of translated text has also been analysed, with the following results:

Tab. 3.3: Most occurred terms in the translated text

Term	Occurrences
layer	*47*
process	*41*
transistor	*33*

etching	*31*
source	*28*

The repetition index tends to be high, as only narrow vocabulary is used in individual disciplines.

3.2.2.3 Acronyms and abbreviations

The abbreviation is a steady way to shorten a word or phrase. Most often, abbreviations are used to write frequently used words or, in the case of science and technology – to shorten long terms. The acronym is a type of abbreviation that, unlike standard abbreviations, is not spelt out and can be read as one word. For example, MOS (Metal Oxide Semiconductor) is usually pronounced in Czech as [m-o-s] – as one word, but in English, it is usually spelt out with single letters [em-ou-es]. This acronym is then extended with another information, such as CMOS (Complementary Metal Oxide Semiconductor), PMOS/NMOS (P-type or N-type MOS) or even MOSFET (Metal Oxide Semiconductor Field Effect Transistor) pronounced in English as a single word [m-ou-s-f-e-t] and in Czech as well [m-o-s-f-e-t]. Some of these abbreviations are not even specified as the author relies on the fact that the reader is already acquainted with the meaning, such as TTL (Transistor-Transistor Logic) or DRAM (Dynamic Random Access Memory). In this type of text, the abbreviations represent mostly the electronic components (IC – Integrated Circuit) or manufacturing processes (CVD – Chemical Vapor Deposition).

3.2.3 Grammatical analysis

This part will deal with analysis from a grammatical point of view.

3.2.3.1 Passive voice

The author's opinion is practically omitted, and the message is centred on describing facts and phenomena. This is very typical for technical texts in both languages, as it is one of the approaches of expressing impersonality, thus being objective. (Krhutová, 2009)

Examples from the text:

…have been demonstrated – byla demonstrována, …is controlled by - …je řízena potencionálem, …can be explained – …lze vysvětlit, …which has to be selected - …která má být vyselektována, ..the wafer is rotated - ..je wafer otáčen, ...the ions of the dopants are accelerated by - Při iontové implantaci jsou ionty daného dopantu urychlovány…

Active voice in Czech technical texts or in English exact science texts are quite common and accepted by using pronoun "we" (for example: *"we deduced", "we assume", "we consider"*), but this case was not found in the source text as the whole textbook aims to be impersonal. According to the Dušková's statistic (Knittlová, 2010), the English scientific text contains in average of 20% of the passive voice from all sentences. Using the passive voice detector tool on the internet, 18% has been concluded from analysing the translated text, proving the nature of given style (from https://datayze.com/passive-voice-detector.php).

3.2.4 Stylistic analysis

As mentioned before, the style of science and technology uses many examples, graphs or tables to support the facts. The didactic style also uses imperative sentences in order to instruct the student/reader to calculate the examples. The entry test is a part of this textbook, serving as a measurement of student's knowledge for teachers, or can represent what is needed to know for further understanding of given topics (Knittlová, 2010).

Examples from the text:
determine - určete,
assume - předpokládejte,
calculate - vypočítejte
Because the author cannot rely on the reader's feedback, or use intonation, gestures or mimics, the message/content has to be formal and complete. To achieve this, the text has to be stylistically clear, allowing the communication process to be smooth, without any complex parts and most importantly, to be understandable. This is facilitated by the arrangement of expressions, the division of text and the continuity of sentences. The well-organised structure is using transition words, auxiliary conjunctions and referencing and denoting terms (Knittlová, 2010).

However, the syntax is relatively simple. Similarly to administrative style, sentences are relatively closed units with a logically consistent structure with a concentrated composition that is stereotyped to some extent. Strict objectivity is achieved by passive voice and impersonality. The author of the text is only objectively and impartially passing facts, providing a view of a certain verifiable fact (Krhutová, 2009).

The uncertainty is not present in this type of text, as the Czech experts in the field of electrical engineering tend to express rather a high degree of certainty and the original text is written in the Czech language. Hence, the certainty has been transferred to the translated text. All the information stated is proved and certain. (Krhutová, 2009)

Examples from the text:

"The reaction product subsequently forms a thin layer on the substrate.", "The basis for semiconductor chips production is a single-crystal semiconductor (Si, Ge or GaAs) with high purity."

Defining in the style of science and technology is done by using formal lexis and other semiotic signs, such as presenting figures and tables, together with specific fonts (e.g. Greek letters) (Krhutová, 2009).

Examples from the text:

"The structure of the NMOS and PMOS transistor on one substrate (type P) is shown in Figure 2.2,..", "Table 2.2 lists the parameters of capacitors from ONSemi I2T100 and I3T25 technologies.", "*The first Fig. 2.13a shows a diffusion graph from a source with an infinite number of dopants and Fig. 2.13b with a limited amount of dopants."*

The formality has a significant role in texts on electrical engineering. Increasing the specificity of the information causes increasing of its wording formality. Krhutová (2009) states that "the more objective the statements, the more formal is the language". The translated text show signs of strict word order, without slang, taboo or colloquial forms. Therefore, it can be categorized as a formal text. Additionally, the author has no intention to impact the reader emotionally.

Objective word order is the word order that proceeds from the theme (known) to the rheme (new information). For this reason, the new information is always listed at the end of the sentence.

Examples from the text:

"At the end of the 1970s, it was clear that MOS technology is the right direction for achieving high-density integration on the chip (R). Firstly, it was used for NMOS analogue and digital circuits."

"To understand the entire manufacturing process of semiconductor chips, it is necessary to know the following procedural steps (R). These include oxidation, diffusion, deposition, ion implementation, and etching."

As mentioned above, the impersonality can be achieved by using a passive voice. The facts are conducted on real experiments and real facts, which means that the author is expressing general idea impersonally. Personality and impersonality can be determined from the author's personal approach to the readers. This translated text can be considered as highly impersonal, but still, a few examples of personality can be found (Krhutová, 2009).

For example:

"Dear students, you get to your hands.." – the author is interacting with readers in the introduction part

"Calculate", "Determinate", and *"Assume"* – can be considered as a personal approach to the readers/students in the *Entry test* part, instructing them to do a particular activity.

These examples are the only ones representing the personality in the text.

3.2.5 Pragmatic analysis

This part will deal with analysis from a pragmatic point of view.

3.2.5.1 Implicitness and explicitness

Another distinctive feature of the style of science and technology is the degree of explicitness and implicitness. As the translated text is written using the didactic style, it is supposed that everything should be clearly described - explicitly. However, this given textbook is intended for the further education of the university students of the second year in the particular field of electrotechnics. Therefore, it can be somewhat considered with its signs closer to scientific prose and categorize it as a scientific book. With that in mind,

the author relies on the professional knowledge of the readers, allowing him to omit some definitions of specific terms. For example, fundamental laws of electrotechnics or description of basic electrotechnics components (Krhutová, 2009).

It is also mentioned in the introductory part: *"The subject requires basic knowledge of electronic components - especially MOS transistors and operational amplifiers."*

Examples of implicitness in the translated text:

"Nowadays, bipolar technology and CMOS (Complementary Metal Oxide Semiconductor) are the most widely used. In history, bipolar technology (operational amplifiers, TTL circuits) have dominated the field of silicon integrated circuits (IC). In the 1970s, a number of circuits have been demonstrated in MOS technology – DRAM memories, microprocessors, and logic circuits series 4000."

Definitions:

"An operational amplifier (or an op-amp) is an integrated circuit (IC) that operates as a voltage amplifier" (https://www.chegg.com), *"Transistor-transistor logic (TTL) is a class of integrated circuits which maintain logic states and achieve switching with the help of bipolar transistors."* (https://www.techopedia.com), *"Dynamic random access memory (DRAM) is a type of random-access memory used in computing devices (primarily PCs). DRAM stores each bit of data in a separate passive electronic component that is inside an integrated circuit board."* (https://www.techopedia.com), *"A microprocessor is a component that performs the instructions and tasks involved in computer processing. In a computer system, the microprocessor is the central unit that executes and manages the logical instructions passed to it."* (https://www.techopedia.com).

Examples of explicitness in the translated text:

"A condition for the amplification of the electrical signal is the power gain (this condition basically says that an element can amplify, only when it is able to amplify a voltage or current, or both)." – This *condition* is explicitly described by added information in the parentheses.

"However, the current flowing does not disappear but remains constant when the U_{DS} increases (Figure 2.6)." – This fact is supported by the graphical content, where it can be easily seen and understood in the graph.

Conclusion

The aim of this bachelor thesis was to translate the science and technology text and comment on its problems on the theoretical and practical level. For this purpose, the electronic textbook *Design of Analog Integrated Circuits* was chosen, as it might prove useful for the university for further education of foreign students of this same-named course. Another reason was that electrical engineering is also a significant part of my studies, therefore extending the technical knowledge of microelectronics field is considered as a positive outcome. The thesis was divided into three main parts.

The theoretical part presented the proper ways and tools used for creating the functional and quality translation from a source language to a target language. This can be achieved by following the procedural steps, according to Malone, and Vinay and Darbelnelt. Additionally, the types of translations described by Jakobson and Hrdlička were introduced. The final chapter of the theoretical part deals with the features of the professional, functional style. Hence, the acquired knowledge could be applied in the practical part of this thesis.

The practical part is represented by the translation of two chapters - *Introduction* and the *CMOS technology*.

The analytical part presented a translation commentary created on the basis of the problematic phenomena in the translation process. These problems were commented from the lexical, grammatical, stylistic and pragmatical perspective, such as the extensive use of passive voice and specific terms in the style of science and technology.

This bachelor thesis has expanded my knowledge of translation theory and enriched me with valuable practical experience, which could be useful for the upcoming state exams and in my future career. I was reassured that a good translator must have not only an excellent knowledge of the source language but also excellent knowledge of the target language. In translating professional texts, at least a basic knowledge of the field is an essential part of the translator's arsenal, without which it would be difficult to understand the text itself, which is the first prerequisite for translation. Nowadays, the internet can be beneficial in searching for a particular information or specific term. As I can tell myself, the translation activity is very demanding, lengthy and sometimes very exhausting.

Bibliography

HAUSENBLAS, Karel, 1972. *Učební styl v soustavě stylů funkčních*. [online]. [cit. 2019-05-15]. Available from: http://naserec.ujc.cas.cz/archiv.php?art=5628.

HRDLIČKA, Milan, 1997. *Literární překlad a komunikace*., Praha: Filosofická fakulta Univerzity Karlovy Praha, 81 s. ISBN 80-85899-22-1.

JANATA, Petr, 1999. *Překládáme do angličtiny*., Plzeň: Fraus, 185 s. ISBN 80-7238-052-4.

KNITTLOVÁ, Dagmar, 2000. *K teorii i praxi překladu*. 2nd ed., Olomouc: Univerzita Palackého v Olomouci, 215 s. ISBN 8024401436.

KNITTLOVÁ, Dagmar a kol., 2010, *Překlad a překládání.* 1st ed., Olomouc: Univerzita Palackého v Olomouci, Filozofická fakulta, 291 s. ISBN 978-80-244-2428-6.

KRHUTOVÁ, Milena, 2009. *Parameters of professional discourse:* English for electrical engineering. 1st ed. in Tribun EU. Brno: Tribun EU, 197 s. ISBN 978-80-7399-867-7.

LEVÝ, Jiří, 2013. *Umění překladu*., 4th ed., Praha: Apostrof, 368 s. ISBN 978-80-87561-15-7.

POŠTOLKOVÁ, Běla, 1983. *O české terminologii*., 1st ed., Praha: Academia, 120 s.

List of tables

Source text

4 Úvod

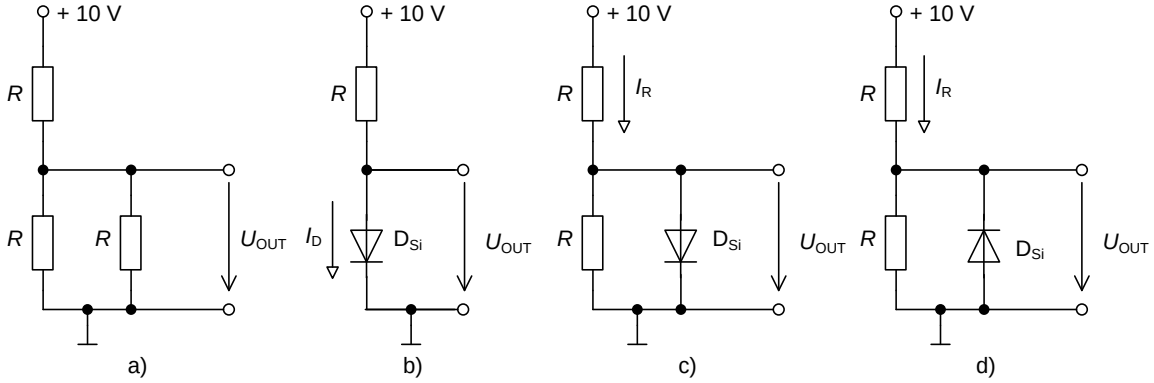
Vážení studenti, dostává se vám do rukou elektronický text skript pro předmět BNAO - Návrh analogových integrovaných obvodů. V rámci tohoto předmětu jsou studenti seznámeni s technologií CMOS a návrhem základních analogových integrovaných obvodů. Předmět vyžaduje základní znalosti z oblasti elektronických součástek – zejména tranzistorů MOS a operačních zesilovačů. Úvodní část skript se věnuje procesu výroby polovodičových čipů, jsou zde popsány jednotlivé procesní kroky včetně názorných obrázků. Následuje detailní popis principu činnosti tranzistoru MOS, malosignálový model, režimy činnosti a důležité matematické vztahy potřebné pro návrh obvodů. Další část skript se již věnuje návrhu konkrétních analogových obvodů. Začíná se proudovými zrcadly, které jsou prakticky součástí většiny složitějších obvodů. Následují proudové a napěťové reference, diferenční pár. Po detailním seznámení s návrhem a funkcí těchto základních obvodů následuje kapitola zabývající se operačními zesilovači. V kapitole jsou popsány zásady návrhu operačního zesilovače pro dosažení požadovaných parametrů. Detailně je popsána i problematika jejich stability. Poslední kapitole popisuje návrh topologie (layout) čipu.

4.1 Zařazení předmětu ve studijním programu

Předmět Návrh analogových integrovaných obvodů je zařazen v bakalářském studijním programu do předmětů volitelných oborových oboru Mikroelektronika a technologie (letní semestr 3. ročníku) a oboru Elektronika a sdělovací technika (letní semestr 2. ročníku) a dále také jako volitelný mimooborový v letním semestru 2. ročníku bakalářského studijního programu pro obor Teleinformatika.

4.2 Vstupní test

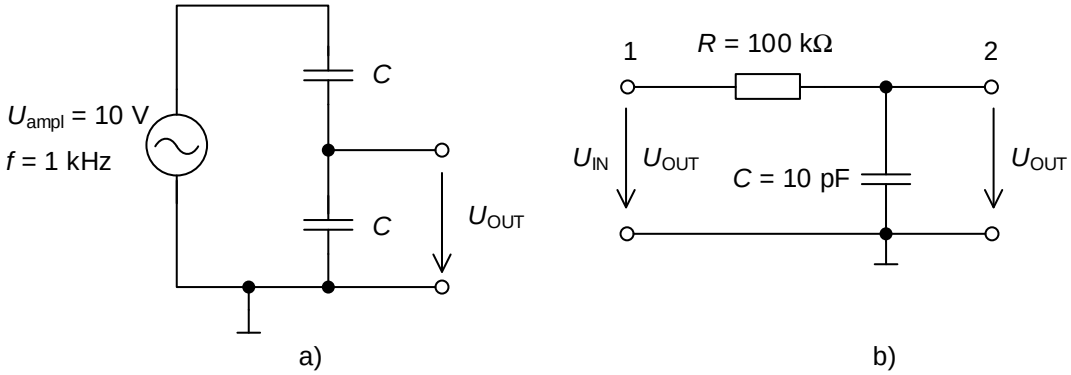
Př. 1: Určete výstupní napětí U_{OUT} následujících obvodů. Předpokládejte ideální parametry součástek. R = 100 Ω. U obvodu b) vypočítejte proud I_D a u obvodu c) a d) proud I_R.



Obr. 4.1: Schémata zapojení k příkladu 1

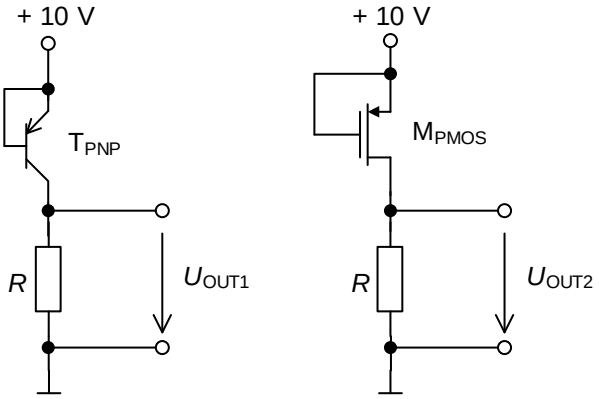
Př. 2: Určete amplitudu U_{OUT} – **obr. 1.2a**. C = 10 pF.

Př. 3: Určete kmitočet pólu f_P obvodu na **obr. 1.2b**.



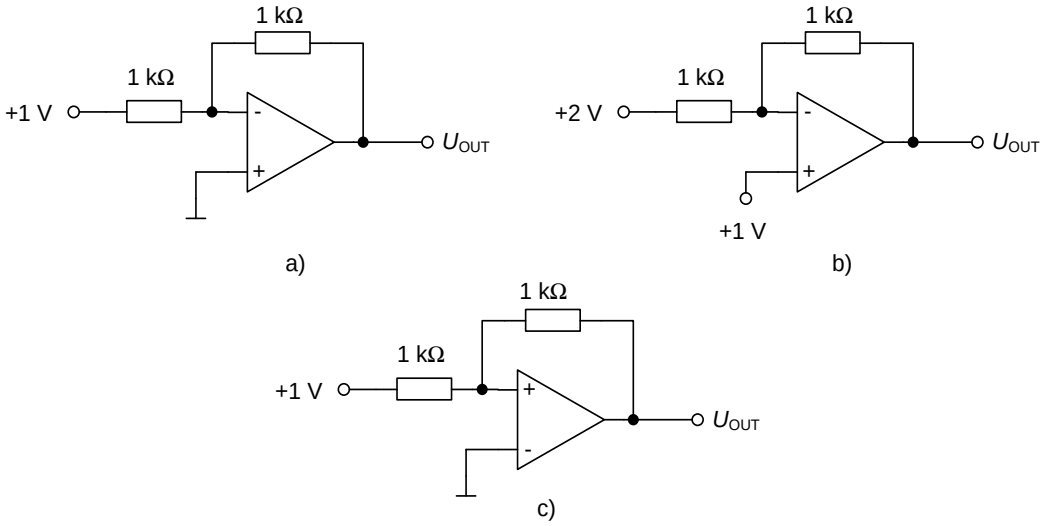
Obr. 4.2: Schémata zapojení k příkladu 2 a 3

Př. 4: Vypočítejte výstupní napětí U_{OUT1} a U_{OUT2}. Předpokládejte ideální tranzistory. $R = 100\ \Omega$.



Obr. 4.3: Zapojení s tranzistory k příkladu 4

Př. 5: Vypočítejte výstupní napětí U_{OUT} u jednotlivých zapojení. Předpokládejte ideální operační zesilovače.



Obr. 4.4: Zapojení s operačními zesilovači k příkladu 5

5 Technologie CMOS

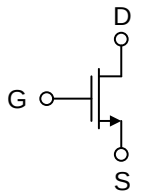
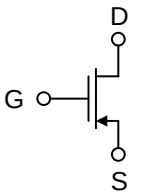
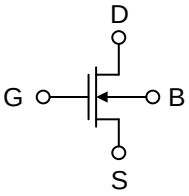
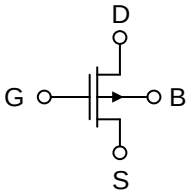
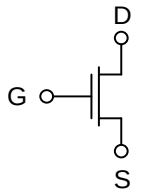
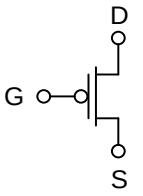
V současné době jsou nejvíce rozšířené technologie bipolární a CMOS (Complementary Metal Oxid Semiconductor). V historii mnoho let dominovala v oblasti křemíkových integrovaných obvodů (IO) bipolární technologie (operační zesilovače, obvody TTL). V 70-tých letech byla demonstrována v technologii MOS řada obvodů – paměti DRAM, mikroprocesory a logické obvody série 4000. Na konci 70-tých let bylo zřejmé, že technologie MOS je správným směrem pro dosažení vysoké hustoty integrace na čipu. Nejdříve byla používána pro analogové a digitální obvody technologie NMOS. V 80-tých letech to byla již technologie CMOS. Tato technologie umožňuje v oblasti digitálních IO kromě možnosti vysoké hustoty integrace také nízkou spotřebu. Naopak bipolární technologie poskytuje mnoho výhod v čistě analogových IO. Například mnohonásobně vyšší transkonduktanci při stejném proudu. Proto je tedy pro návrh čistě analogových IO používána především bipolární technologie a pro návrh čistě digitálních IO technologie CMOS. Často však je na IO jak analogová tak digitální část. Pro tyto případy lze použít technologii BiCMOS, kde je možné používat bipolární tranzistory i tranzistory MOS [1]. Avšak pro tyto kombinované IO je z hlediska ceny vhodné použít čistě technologii CMOS. Tato skripta jsou zaměřena jen na technologii CMOS.

5.1 Tranzistor MOSFET

Tranzistor MOSFET (Metal Oxide Semiconductor Field Effect Transistor) je tranzistor řízený elektrickým polem. Vodivost kanálu mezi elektrodami source a drain je řízena potenciálem připojeným mezi terminály hradlo (gate) a source. Gate je izolován od kanálu vrstvou oxidu křemíku (SiO_2) – odtud pochází v názvu typu tranzistoru oxid. Elektrody source a drain mohou být typu N i P, ale obě musí být stejného typu. Pokud jsou typu N, jedná se o tranzistor NMOS. V opačném případě, pokud jsou typu P, jedná se o tranzistor PMOS.

Tab. 5.1: Používané symboly pro tranzistory NMOS a PMOS

	Tranzistor NMOS	Tranzistor PMOS

Bulk je spojen s U_{SS} (NMOS), resp. s U_{DD} (PMOS)		
Bulk není připojen		
Digitální model		

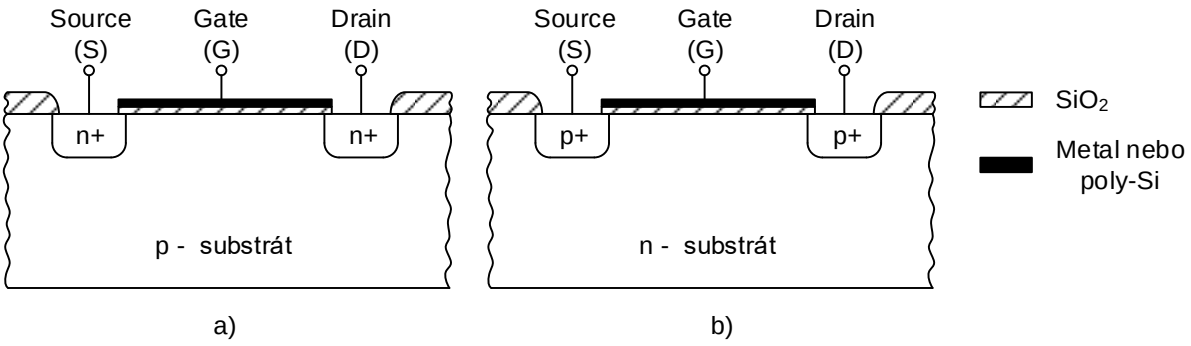
Napětí U_{DD} je kladné a U_{SS} záporné napájecí napětí.

Název elektrody source je odvozen od toho, že slouží jako zdroj (source) nosičů náboje (elektronů pro kanál typu N a děr pro kanál typu P), které procházejí kanálem. Podobně je nazván drain jako místo, kde nosiče z kanálu odtékají.

Pokud je MOS tranzistor typu N jsou oblasti drain a source typu N+ („+“ značí vysokou koncentraci dopantu) a oblast pod hradlem je typu P. Pokud je připojeno mezi gate a source kladné napětí U_{GS}, vytvoří se pod hradlem inverzní vrstvička typu N nazývaná kanál. Kanál spojuje oblasti source-drain a umožňuje průchod nosičů elektrického náboje (elektrický proud) mezi těmito oblastmi. Pokud je připojeno mezi gate a source nízké napětí (menší než prahové) nebo záporné, kanál mizí a nosiče náboje nemohou mezi oblastmi source-drain procházet (tranzistor je uzavřen, elektrický proud neprochází).

Pokud je MOS tranzistor typu P jsou oblasti drain a source typu P+ a oblast pod hradlem je typu N. Pokud je připojeno mezi gate a source záporné napětí U_{GS} vytvoří se pod ním inverzní vrstvička typu P nazývaná kanál. Kanál spojuje oblasti source-drain a umožňuje průchod nosičů elektrického náboje (elektrický proud) mezi těmito oblastmi. Pokud je připojeno mezi gate a source vyšší napětí (vyšší než prahové) nebo kladné, kanál

mizí a nosiče náboje nemohou mezi oblastmi source-drain procházet (tranzistor je uzavřen, elektrický proud neprochází).



Obr. 5.1: Struktura tranzistoru a) NMOS b) PMOS

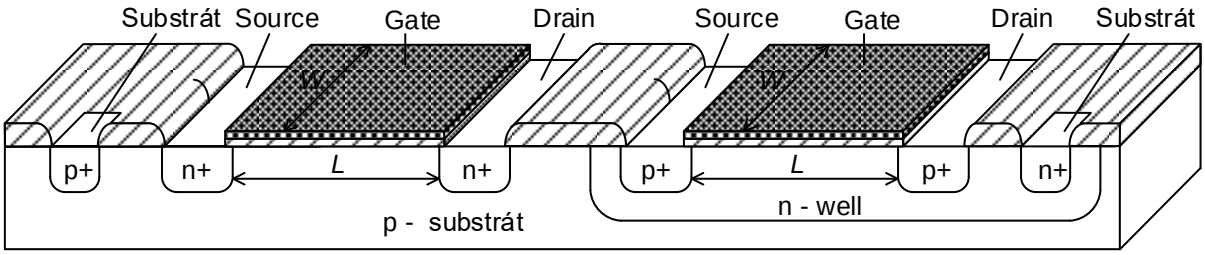
Podmínkou pro proces zesilování elektrického signálu je výkonové zesílení (tato podmínka v podstatě říká, že zesilovat může prvek, který umí zesílit napětí nebo proud, případně obojí). Součástka, která umí zesilovat proud i napětí je samozřejmě velmi žádaná. Tranzistor MOSFET takovou součástkou je.

Proudové zesílení MOS tranzistoru lze vysvětlit jednoduše tím, že MOS žádný vstupní proud nepotřebuje (a ani žádný proud vstupní svorkou neteče). Struktura má tedy teoreticky nekonečné velké stejnosměrné proudové zesílení. Proudové zesílení je nepřímo úměrné kmitočtu signálu a dosahuje jednotkového zesílení na tranzitním kmitočtu.

Napěťové zesílení MOS tranzistoru je způsobeno proudovou saturací v oblasti vyšších hodnot drain-source napětí, takže malá změna proudu způsobí velkou změnu napětí.

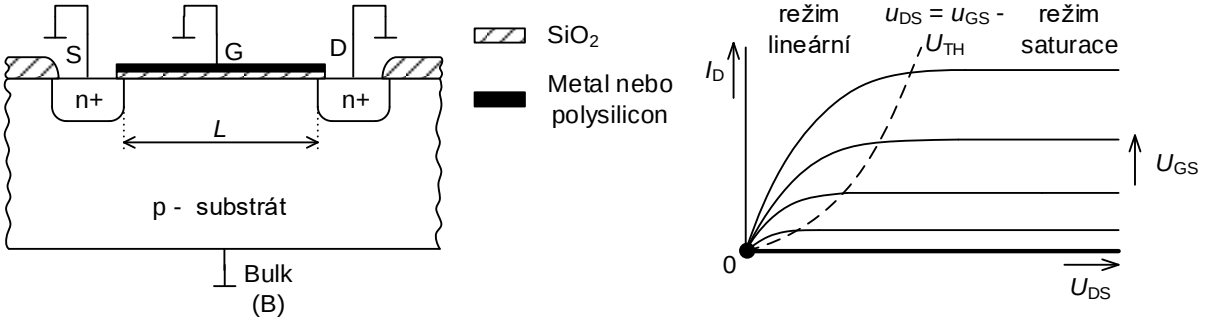
5.1.1 Struktura a princip tranzistoru MOS

Struktura tranzistoru NMOS a PMOS na jednom substrátu (typu P) je na obr. 2.2, kde délka kanálu *L* je identická s šířkou kanálu *W*. Skutečná délka hradla *L* není shodná s požadovanou délkou hradla, ale spíše se blíží vzdálenosti oblastí drain a source pod hradlem. Překryv mezi oblastí hradla a drain/source je důležitý pro zajištění vodivé cesty (kanálu) mezi drain-source. Obvykle je snahou, aby tento překryv byl co možná nejmenší – z důvodu minimalizace parazitních kapacit.



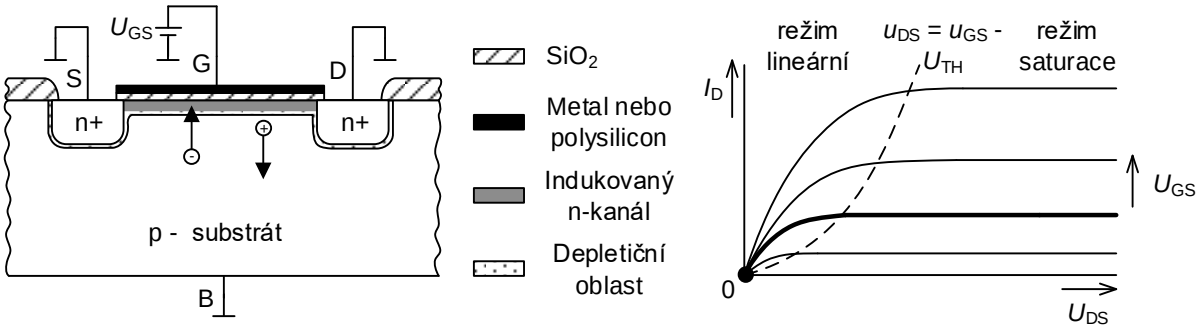
Obr. 5.2: Struktura tranzistoru NMOS a PMOS na jednom substrátu

Na struktuře uvedené na obr. 2.3. je přidán kontakt na substrát. Ten musí být zapojen tak, aby byl přechod PN vždy pólován v závěrném směru. Tedy substrátový kontakt na P+ na nejnižší potenciál v obvodu (U_{NAP-}) a substrátový kontakt na N+ na nejvyšší potenciál v obvodu (U_{NAP+}).



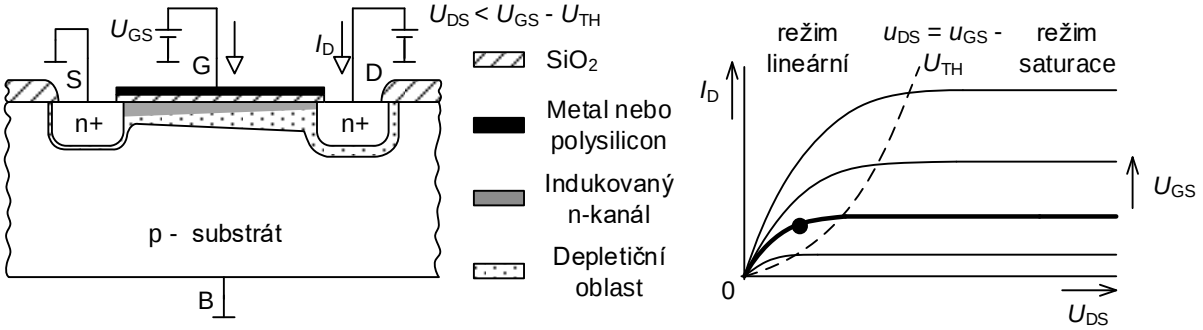
Obr. 5.3: Tranzistor NMOS v zavřeném stavu

Na obr. 2.3 je stav, kdy je gate, source a drain připojen na zem. Pod hradlem se nevytvoří inverzní vrstvička – vodivý kanál, který by umožňoval průchod nosičů elektrického náboje mezi drain a source. Tranzistor je uzavřen.



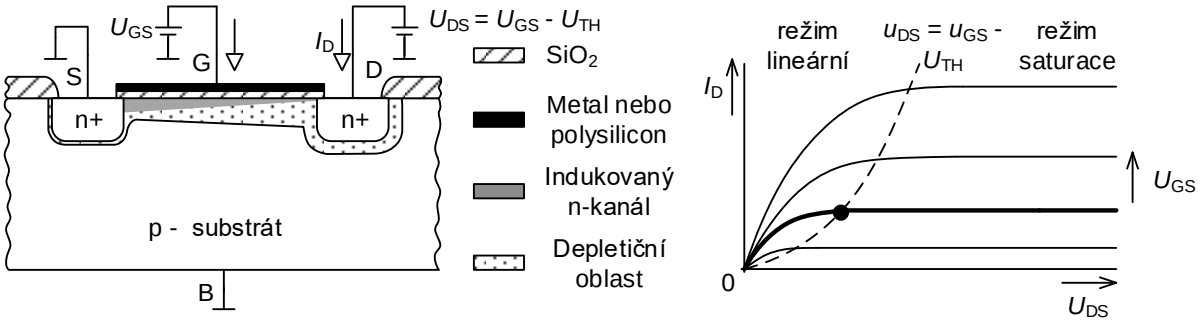
Obr. 5.4: Vytvoření inverzní vrstvičky v tranzistoru NMOS

Po připojení kladného napětí U_{GS} jsou minoritní nosiče (elektrony) v P-substrátu přitaženy a majoritní nosiče (díry) odpuzeny z oblasti pod hradlem (obr. 2.4). Pod hradlem je tedy vytvořena inverzní vrstvička typu N, která spojuje oblasti drain a source vodivým kanálem. Zároveň se pod rozhraním dielektrikum - polovodič vytvoří depletiční oblast.



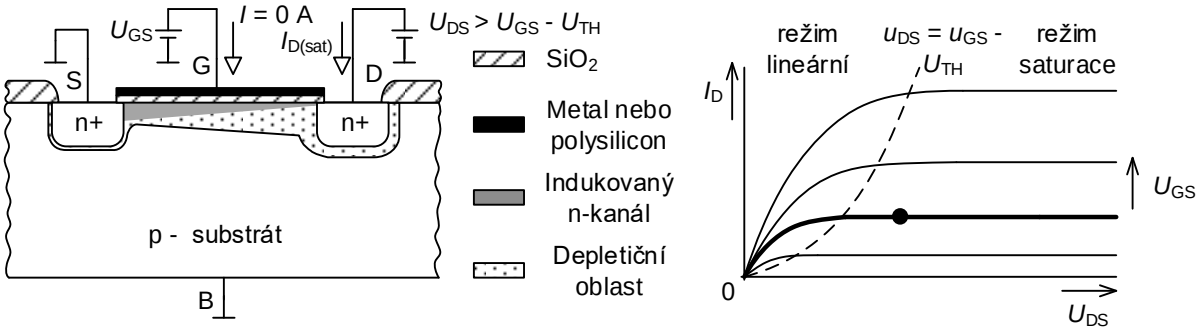
Obr. 5.5: Tranzistor NMOS v lineárním režimu

Po připojení napětí U_{DS} začne mezi oblastmi drain a source protékat proud I_D (obr. 2.5). Při zvyšování U_{DS} zároveň klesá rozdíl potenciálů mezi drain a hradlem a zužuje se kanál na straně elektrody drain a zvětšuje se depletiční oblast kolem oblasti drain. Pro malá $U_{DS} < U_{GS} - U_{TH}$ proud I_D roste lineárně s napětím U_{DS}. Tranzistor se nachází v lineárním režimu.



Obr. 5.6: Tranzistor NMOS, přechod do režimu saturace

Pokud je napětí $U_{DS} = U_{GS} – U_{TH}$ dojde na straně drainu k uzavření kanálu („zaškrcení“)
a k saturaci proudu I_D, procházející proud ovšem nezanikne a zůstává konstantní při dalším zvyšování U_{DS} (obr. 2.6).



Obr. 5.7: Tranzistor NMOS v režimu saturace

Se zvyšujícím se napětím U_{DS} se proud I_D již nemění. Tranzistor se nachází v režimu saturace (obr. 2.7).

5.2 Pasivní součástky

Tato kapitola se věnuje pasivním součástkám, používaných při návrhu IO, jež jsou kompatibilní s výrobním procesem technologie CMOS. Mezi tyto součástky patří

rezistory
a kapacitory.

5.2.1 Kapacitory

Kapacitory se používají v analogových obvodech, jako jsou filtry, převodníky DA a AD, vzorkovací obvody, kompenzační prvky v operačních zesilovačích apod. Oblíbená je při návrhu IO také technika spínaných kapacitorů (SC). Charakteristickými rysy kapacitorů používaných ve výše uvedených aplikacích jsou

- dobrý souběh (matching),
- vysoká kapacita na jednotku plochy,
- nízká teplotní závislost,
- dobrý poměr dosažené kapacity a parazitní kapacity.

Kapacitor je v technologii CMOS realizován strukturou dvou paralelně (ve velké většině nad sebou) umístěných elektrod. Elektrody by měly být realizovány vodivými vrstvami, které jsou v dané technologii k dispozici (metal, polySi, difúze). Izolační dielektrikum mezi elektrodami je většinou z oxidu křemíku (SiO_2), nitridu křemíku (Si_3N_4) nebo polySiO_2. V technologiích IO se vyskytují nejčastěji kapacitory vytvořené mezi metalickými vrstvami (např. metal3-metal2 u ONSemi I3T, metal6-metal5 u TSMC 180 nm, atd.), poly-poly nebo metal1(M1) - poly. V ideálním případě by hodnota kapacity neměla být závislá na teplotě okolí a přiloženém napětí. Ve skutečnosti závislá je. Tato závislost je vyjádřena parametry t_c (teplotní) a v_c (napěťová). V tab. 1 jsou uvedeny parametry kapacitorů z technologií ONSemi I2T100 a I3T25.

Tab. 5.2: Přehled typických parametrů kapacitorů v technologiích ONSemi

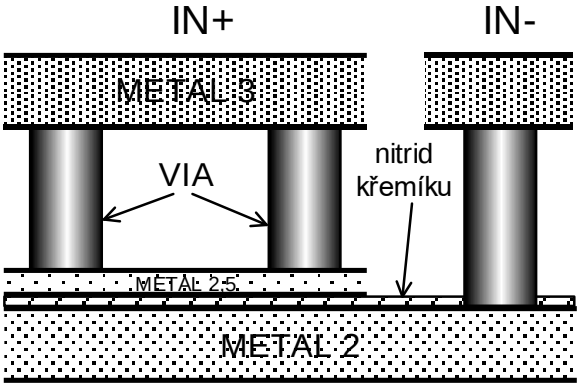
Typ	Technologie	Kapacita [fF/μm^2]	Teplotní závislost [ppm/°C]	Napěťová závislost [ppm/V]
M1-poly	I2T100	0,75	-	25
poly-poly	I3T25	0,94	25	15

M3-M2 (MIMC)	I3T25	1,5	45,5	-32,03

Realizace samotného kapacitoru na čipu má vlivem technologických odchylek výrobního procesu značnou nepřesnost. Např. u technologie I3T25 uvádí katalogový list typickou hodnotu kapacity 1,5 fF/μm^2. Krajní hodnoty výrobního procesu však jsou 1,3 fF/μm^2 a 1,7 fF/μm^2, což dělá chybu až ±15 %. V IO se často využívá poměru dvou a více kapacitorů. Tento poměr lze realizovat s přesností kolem 0,1 %. Výsledná přesnost poměru závisí na velikosti plochy kapacitoru ($W \cdot L$), koeficientu souběhu A [%·μm] a na provedení topologie čipu. Platí

$$\sigma^2\left(\frac{\Delta C}{C}\right) = \frac{A^2}{W \cdot L}. \tag{5.1}$$

V technologii I3T25 má kapacitor mezi M3-M2 koeficient souběhu A = 1,48 %·μm. Pro dva kapacitory, každý o velikosti 1,5 pF ($W \cdot L$ = 1000 μm^2) je souběh 0,04 %. Tato hodnota předpokládá kvalitně navrženou topologii (kapitola 8).



Obr. 5.8: Struktura kapacitoru MIMC

Na obr.2.8 je ukázána struktura kapacitoru M3-M2 – MIMC (Metal – Insulator – Metal capacitor). Mezi vrstvou M3 a M1 je přes via M3 připojen na vrstvu M2,5. V moderních technologiích existují také struktury dvou kapacitorů nad sebou zapojených paralelně. Dojde tak k dvojnásobnému zvýšení kapacity na jednotku plochy.

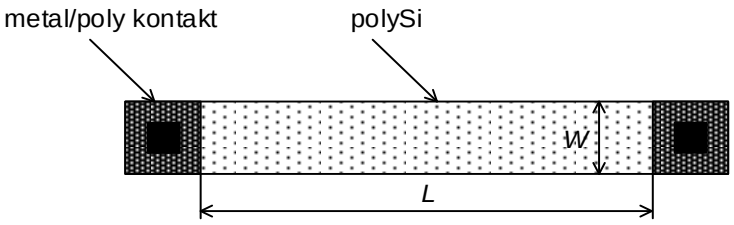
5.2.2 Rezistory

Hlavními součástkami používanými v návrhu IO jsou tranzistory MOS a kapacitory. V některých obvodech nacházejí uplatnění i rezistory. Mezi tyto obvody patří např. převodníky AD a DA, děliče napětí apod. Obecně je rezistor tvořen vrstvou (obdélníkem či proužkem) rezistivního materiálu, který je na svých koncích kontaktován s vrstvou metal 1. Samotné tělo rezistoru je elektricky izolováno od substrátu (podložky) pomocí oxidové vrstvy nebo polovodičovým přechodem v závěrném směru. Pokud je zaveden jako parametr tzv. odpor na čtverec - $R_{\square}$, pak celkový odpor rezistoru bude určen jako

$$R = R_{\square}\frac{L}{W} + 2R_{kont}, \tag{5.2}$$

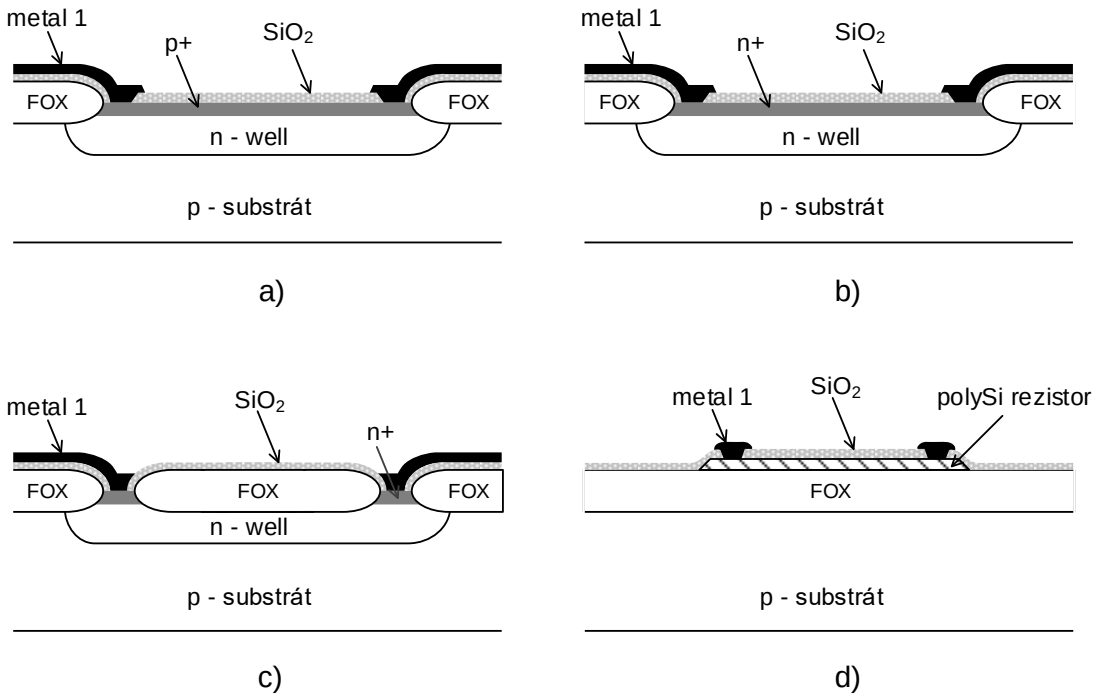
kde R_{kont} je odpor kontaktů, který se pohybuje v jednotkách Ω a lze jej zanedbat.

Nejpoužívanějším rezistorem, který nejefektivněji využívá plochu, používaným při návrhu IO je rezistor tvořený vrstvou PolySi. Hodnota jeho odporu na čtverec se pohybuje v rozmezí stovek Ω až jednotky kΩ - pro odpor HIPOR (Hi-Ohmic polySi - bez salicidace)
a v řádu jednotek Ω pro odpor LOPOR (Low-Ohmic polySi – se salicidací).



Obr. 5.9: Rezistor vytvořený vrstvou polySi

Dalším typem rezistorů jsou rezistory vytvořené pomocí difúze – N+ nebo P+. Tyto rezistory dosahují menšího odporu na čtverec než rezistory typu HIPOR.



Obr. 5.10: Rezistor vytvořený a) difúzí P+, b) difúzí N+, c) v nwell, d) vrstvou polySi

Struktury využívající polySi můžou lépe čelit problémům s odstíněním. PolySi není potopena přímo v substrátu a tak jsou i tyto parazitní kapacity mnohem menší než v případě rezistoru vytvořeného pomocí difúze. Ke stínění je možno využít jámu (nutno vhodně polarizovat). Ještě lepší odstínění je dosaženo, pokud se rezistor vytvoří z vrstvy polySi 2
a vrstvy polySi 1 je využita ke stínění spolu s jámou.

Tab. 5.3: Přehled typických parametrů některých rezistorů v technologiích ONSemi

Typ	Technologie ONSemi	Odpor [Ω/□]	Teplotní závislost [ppm/°C]
Nwell	I2T100	1300	4900
P+	I2T100	96	1300
N+	I2T100	67,5	1400

HIPOR	I2T100	1825	-2100
HIPOR	I2T25	975	-1420
LOPOR	I2T25	2,4	3470

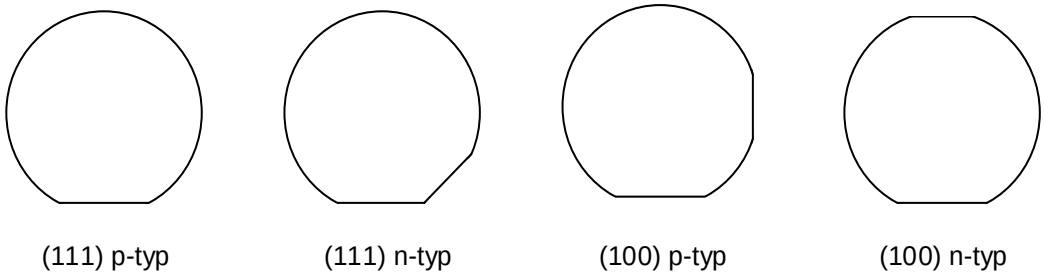
Stejně jako u kapacitorů, i rezistory mají vlivem technologických odchylek výrobního procesu značnou nepřesnost vzhledem ke jmenovité hodnotě. Například u technologie I3T25 uvádí katalogový list typickou hodnotu odporu HIPOR 975 Ω/□. Krajní hodnoty výrobního procesu však jsou 775 Ω/□ a 1175 Ω/□, což znamená chybu až ± 20 %. Rovněž se často využívá poměru dvou a více rezistorů. Tento poměr lze realizovat s přesností kolem 0,1 %. Výsledná přesnost poměru závisí na velikosti plochy rezistoru ($W \cdot L$), koeficientu souběhu A [%·µm] a na provedení topologie čipu. Stejně jako u kapacitorů platí pro souběh rovnice (1).

5.3 Výrobní proces technologie CMOS

Výroba polovodičových čipů se skládá z několika procesních kroků. K pochopení celého výrobního procesu polovodičových čipů je nutné znát tyto procesní kroky. Mezi ně patří oxidace, difuze, depozice, iontová implementace a leptání. Důležitým procesem je také fotolitografie, která slouží pro přípravu topologicky přesně definovaných struktur vytvrzením exponovaného fotorezistu na připraveném vzorku a ohraničuje oblasti, které budou
v následujícím technologickém kroku předmětem lokálních operací.

Základem pro výrobu polovodičových čipů je monokrystal polovodiče (Si, Ge nebo GaAs) s vysokou čistotou. Nejčastěji se monokrystaly polovodiče vyrábějí pomocí Czochralského metody (ten ji objevil v roce 1917). Vstupní polykrystalický křemík s přídavkem malého množství dopantu, který určuje elektrické vlastnosti výsledného produktu, je roztaven v křemenném kelímku a do taveniny je ponořen monokrystalický zárodek. Regulací rychlosti tažení, teploty taveniny, otáček a řady dalších technologických parametrů se docílí toho, že atomy křemíku se postupně zabudovávají do přesně definovaných poloh v krystalové mřížce (100 nebo 111) a tvoří monokrystal o požadovaném průměru (75 mm – 450 mm) a vlastnostech. Výsledným produktem je

monokrystal křemíku (ingot), který se po té nařeže na plátky tloušťky 300 μm (v budoucnu se plánuje 160 μm). Křemíkové desky (wafery) jsou legovány bórem, fosforem, arzenem nebo antimonem. Podle odřezaných částí waferu lze poznat jeho krystalografickou orientaci a typ (obr. 2.11).

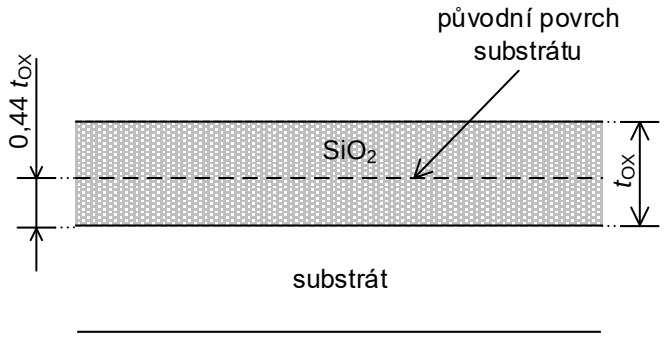


Obr. 5.11: Typy waferů a jejich krystalografická orientace

Základních pět procesních kroků je popsáno v následujících kapitolách (oxidace, difuze, iontová implementace, depozice a leptání).

5.3.1 Oxidace

První základní procesní krok je růst oxidu nebo oxidace. Oxidace je proces, kdy dochází k vytváření vrstvičky SiO_2 na povrchu křemíkového waferu. Oxid narůstá nejen na povrchu waferu, ale také částečně pod povrch křemíkového waferu.



Obr. 5.12: Nárůst oxidu na povrchu waferu

Typicky 56 % oxidu se nachází nad původním povrchem a 44% pod původním povrchem. Tloušťka oxidu, označovaná t_{OX}, může růst pomocí suché (rovnice 2.3) nebo mokré oxidace ve vodní páře (rovnice 2.4) a dosáhnout tak minimální hustoty poruch

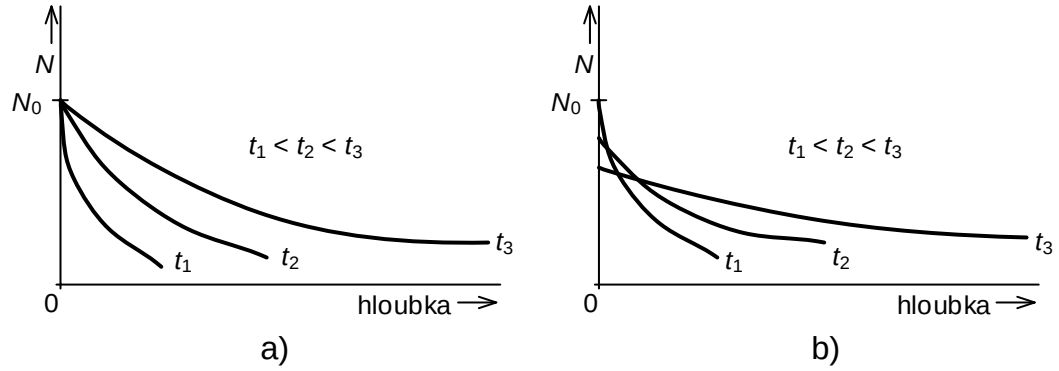
$$Si + O_2 \longrightarrow SiO_2, \tag{5.3}$$

$$Si + H_2O \longrightarrow SiO_2 + H_2. \tag{5.4}$$

Tloušťka oxidu se pohybuje od jednotek nm u gate oxidů (např. u I2T100 t_{OX} = 17,5 nm) po stovky nm u izolačních oxidů (FOX). Oxidace probíhá při teplotách 700 až 1100 °C a je úměrná tloušťce oxidační vrstvy – za předpokladu, že vždy probíhá po stejnou dobu.

5.3.2 Difúze

Druhým procesním krokem je difúze. Difúze je chemický proces, který probíhá, je-li wafer zahřátý na 800-1400 °C (teplota tavení Si je 1415 °C) a je-li vystaven parám dopantu. Atomy dopantu se v tomto procesu pohybují do oblasti s nižší koncentrací - nechá se působit dotující plyn tak dlouho, až dotující molekuly proniknou do požadované hloubky. Pro dosažení větší hloubky po difúzi následuje rozdifundování atomů příměsových atomů do hloubky i do šířky. Celková hloubka difúze se pohybuje od 0,1 μm do 10 μm i více. Na obr. 2.13 jsou dva grafy koncentrace příměsí v závislosti na hloubce proniknutí pro různé časy působení. První obr.2.13a znázorňuje graf difuze ze zdroje s nekonečným množstvím dopantů a obr. 2.13b zdroje s omezeným množstvím dopantů. Koncentrace N_0 je koncentrace na povrchu substrátu. S rostoucí hloubkou koncentrace klesá.



Obr. 5.13: Závislost koncentrace příměsí na hloubce proniknutí pro různé časy a) zdroj s nekonečným množstvím b) omezeným množstvím dopantů

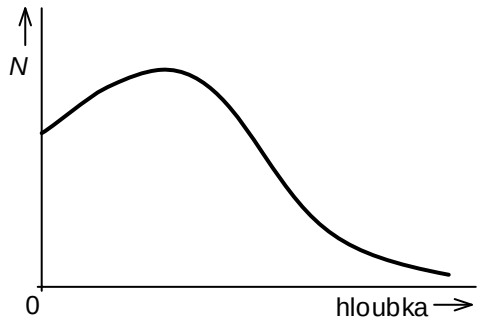
Koncentrace N_0 u obr. 2.13a je konstantní (nekonečný zdroj dopantů). U obr 2.13b vlivem konečného počtu dopantů s rostoucím časem a hloubkou klesá koncentrace N_0.

Pro difúzi je potřebné zajistit vysokou koncentraci, resp. spád koncentrace difundující příměsi (P, As, Sb – příměsi donorového typu v křemíku, B, Al, Ga – příměsi akceptorového typu) a dodat potřebnou energii – difúze příměsí probíhá v reaktorech při vysokých teplotách.

5.3.3 Iontová implantace

Dalším procesním krokem je iontová implantace, která je velmi často používaná při výrobě komponentů MOS. Při iontové implantaci jsou ionty daného dopantu urychlovány elektrickým polem a zaváděny do substrátu s cílem změnit elektrické vlastnosti. Tento proces probíhá při nízkém tlaku. Průměrná hloubka proniknutí je 0,1 až 0,6 μm a závisí na rychlosti a úhlu nastřelování iontů do substrátu. Úhel nastřelování je volen mimo osu mřížky substrátu, aby docházelo ke kolizím s atomy krystalové mřížky substrátu a zabránilo se tak nežádoucímu kanálovému efektu. Nevýhodou je, že úhel nastřelování je příliš ostrý a použitá maska stíní některým místům na substrátu. Jinou možností jak zabránit kanálovému efektu je použití tlusté vrstvy SiO_2, přes kterou jsou nastřelovány ionty dopantu. Vrstva SiO_2 mění náhodně směr proniknutí dopantu než pronikne do substrátu. Proces iontové implantace způsobuje narušení krystalické mřížky substrátu a mnoho implantovaných iontů je tak elektricky neaktivních. Toto poškození může být napraveno

žíháním při teplotě cca 800 °C. Koncentrační profil implantované příměsi je znázorněn na obr. 2.14. Na rozdíl od difúze není největší koncentrace příměsi na povrchu, resp. v místě odkud difúze probíhá, ale v jisté hloubce pod povrchem, kterou lze řídit energií dopadajících iontů.



Obr. 5.14: Koncentrační profil implantované příměsi v závislosti na hloubce proniknutí

Výhodou iontové implantace ve srovnání s difuzí je precizní kontrola dávky dopantu
(± 5 %), velmi dobrá reprodukovatelnost a přesné řízení hloubky. Je tak možné upravit prahové napětí tranzistoru nebo vytvářet precizní rezistory. Další výhodou je, že iontová implantace probíhá při pokojové teplotě. Je pouze nutné při následné opravně krystalické mřížky substrátu žíháním použít vysokou teplotu.

5.3.4 Depozice

Depozice je chemický proces využívaný pro přípravu tenkých filmů různých materiálů na křemíkovou destičku. Tenké filmy můžou být připravovány různými technikami - např. napařováním, naprašováním nebo chemickou depozicí z plynné fáze (CVD - Chemical Vapour Deposition).

Při depozici napařováním je materiál v pevném skupenství umístěn ve vakuu a zahříván (vysokofrekvenční, iontový ohřev), dokud se nezačne vypařovat. Vypařované molekuly zasáhnou chladný wafer a kondenzují na povrchu waferu v tenký film. Tloušťka naneseného filmu závisí na teplotě a na času, po který probíhá napařování. Tato technika vyžaduje vakuum.

Naprašování lze zrealizovat např. magnetronovým, iontovým nebo katodovým způsobem. Obecně se jedná o nanášení atomů materiálu (Al, Cu) na kontakty čipu (anoda) energií, která vyráží tyto atomy z terče (katoda). Tyto atomy jsou unášeny na substrát vlivem elektrického pole mezi materiálem a destičkou. Tato technologie neklade velké nároky na teplotu a tlak, jako tomu je u napařování, je řízena napětím a tlakem (není třeba tak vysoké vakuum jako při napařování).

Chemická depozice z plynné fáze (Chemical Vapour Deposition - CVD), je technologický postup tvorby tenkých vrstev, který využívá chemické reakce v plynné fázi. Může se jednat o reakce mezi více prekurzory nebo rozkladnou reakci jedné látky. Reakční produkt vytváří následně na substrátu tenkou vrstvu. Metoda CVD probíhá za zvýšené teploty a vedlejší produkty chemických procesů jsou odsáty vakuem nebo odstraněny proudem plynu. Obvykle však probíhá při atmosférickém tlaku, ale může i při nízkém vakuu (označuje se LPCVD - Low Pressure CCD). Tento typ depozice se používá především pro vytváření vrstev polySi, SiO_2 nebo Si_3N_4.

5.3.5 Leptání

Leptání je proces odstranění exponovaného materiálu. Která část materiálu bude odstraněna a která ne je dáno technikou fotolitografie, která je popsána v další kapitole. Na
obr. 2.15a jsou tři vrstvy materiálu - vrchní ochranná vrstva (maska), pod ní se nachází tenký film naneseného materiálu depozicí. Spodní vrstva je substrát.

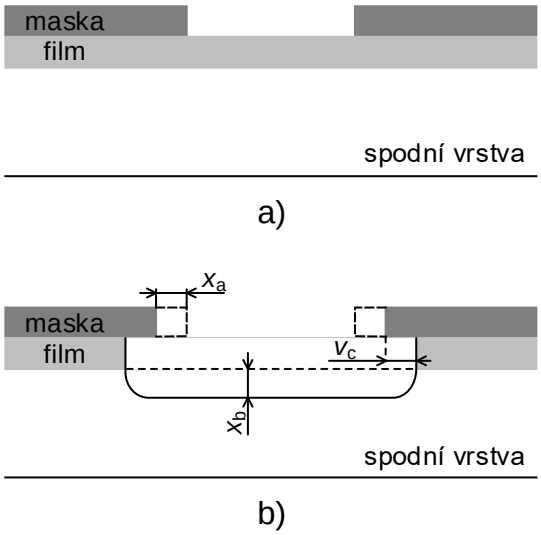
Cílem leptání je odstranit pouze maskou nechráněný film. Leptací proces musí mít dvě důležité vlastnosti. Zaprvé selektivitu (S) - leptací proces musí působit pouze na požadovanou vrstvu - tenký film a nesmí působit na masku ani na substrát. Selektivita může být vyhodnocena jako poměr rychlosti leptání požadované vrstvy a nepožadované vrstvy

$$S_{A-B} = \frac{rychlost\ leptání\ požadované\ vrstvy}{rychlost\ leptání\ nepožadované\ vrstvy}. \tag{5.5}$$

Druhou důležitou vlastností je anizotropie (A). Požadována je maximální anizotropie, tj. jeden směr rychlého leptání (hodnota 1). Anizotropie může být kvalifikována jako

$$A = 1 - \frac{boční\ rychlost\ leptání}{vertikální\ rychlost\ leptání}. \tag{5.6}$$

Ve skutečnosti nelze dosáhnout perfektní selektivity ani anizotropie, výsledkem čehož je odleptání i části masky a spodní vrstvy (obr. 2.15b). Rozměr x_a ukazuje, jaká část masky byla odleptána a x_b jaká část spodní vrstvy (neideální selektivita). Rozměr y_c ukazuje podleptání pod maskou - souvisí s neideální anizotropií. Mezi materiály (na obr. 2.15 tenký film), které jsou leptány, patří polySi, SiO_2, Si_3N_4 a hliník.



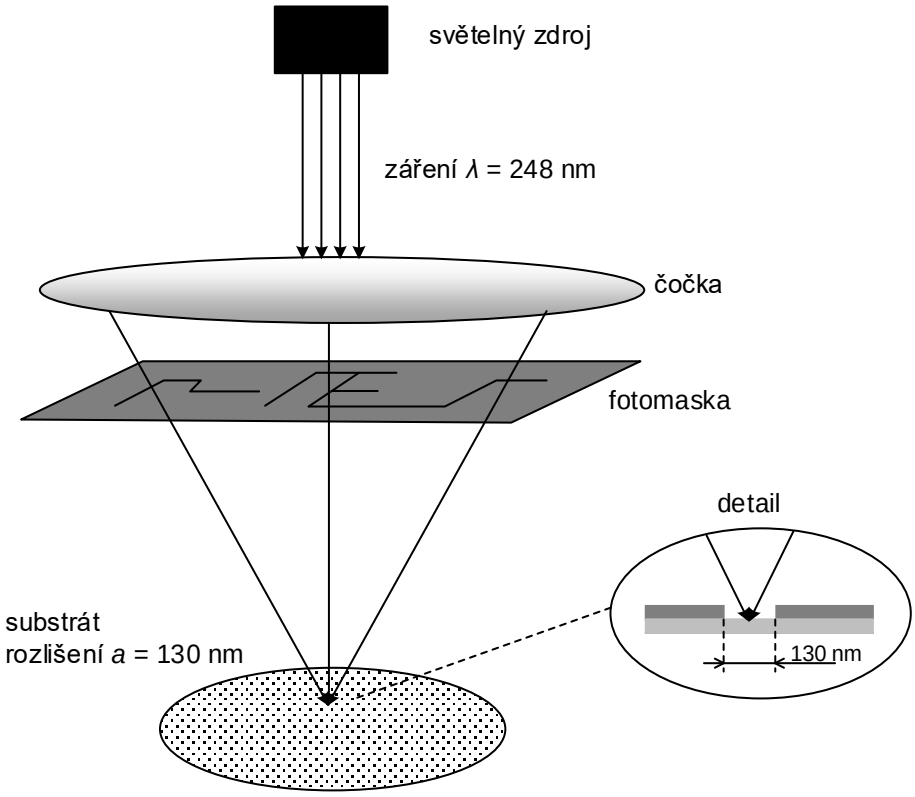
Obr. 5.15: Proces leptání a) struktura před leptáním b) po leptání

Existují dva základní typy leptání - mokré a suché leptání. Mokré leptání využívá chemikálie, které odleptávají požadovaný materiál. Kyselina fluorovodíková (HF) se používá při leptání SiO_2, kyselina fosforečná při leptání Si_3N_4. Kyselina dusičná, octová nebo fluorovodíková se používá pro odstranění polySi, hydroxid draselný pro křemík a směsi kyseliny fosforečné pro odstranění metalických vrstev. Mokrý leptací proces je silně závislý na čase působení a teplotě.

Suché leptání využívá ionizované plyny. Vznik a rozvoj suchých leptacích procesů si vyžádala stále větší miniaturizace v mikrotechnologiích (a také nanotechnologiích), protože mokré leptací procesy nevyhovují submikronovým rozměrům (selektivita, anizotropie). Suché leptání se vyznačuje výbornou anizotropií (nedochází k podleptání), a proto se používá pro submikronové technologie.

5.3.6 Fotolitografie

Většina základních procesních kroků při výrobě polovodičových čipů je aplikována pouze na vybranou část waferu s výjimkou oxidace a depozice. Vybrané části lze definovat pomocí fotolitografie. Základní komponentou fotolitografie je fotorezist a fotomaska, která zakrývá některé části před působením UV záření. Všechny IO se skládají z různých vrstev, které dohromady vytvářejí struktury součástek. Každá vrstva musí být geometricky definována. Tyto vrstvy jsou vytvořeny ve velkém měřítku a po té jsou opticky upraveny do požadované velikosti na waferu.



Obr. 5.16: Princip fotolitografie

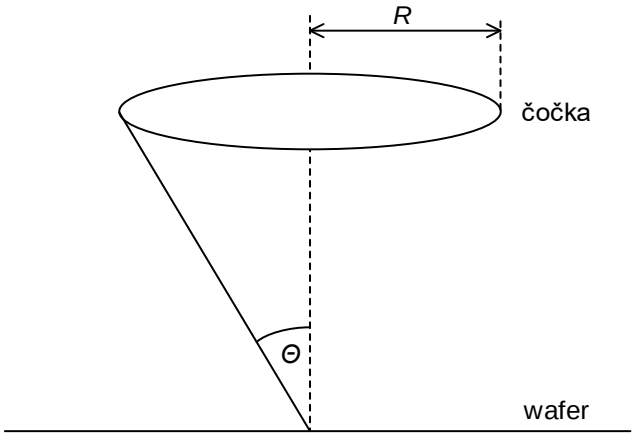
Minimální rozměr (rozlišení), realizovatelný pomocí principu uvedeného na obr. 2.16, je definován

$$M = \frac{c_1 \cdot \lambda}{NA}, \tag{5.7}$$

kde M je rozlišení, λ je vlnová délka emitovaného UV záření, c_1 je index závislý na konkrétním zařízení pro fotolitografii (nabývá hodnot od 0,5 do 1) a NA (numerická apertura). Numerická apertura vyjadřuje účinnou světelnost objektivu. Je to bezrozměrné číslo, které lze vyjádřit jako

$$NA = n \cdot \sin(\theta), \tag{5.8}$$

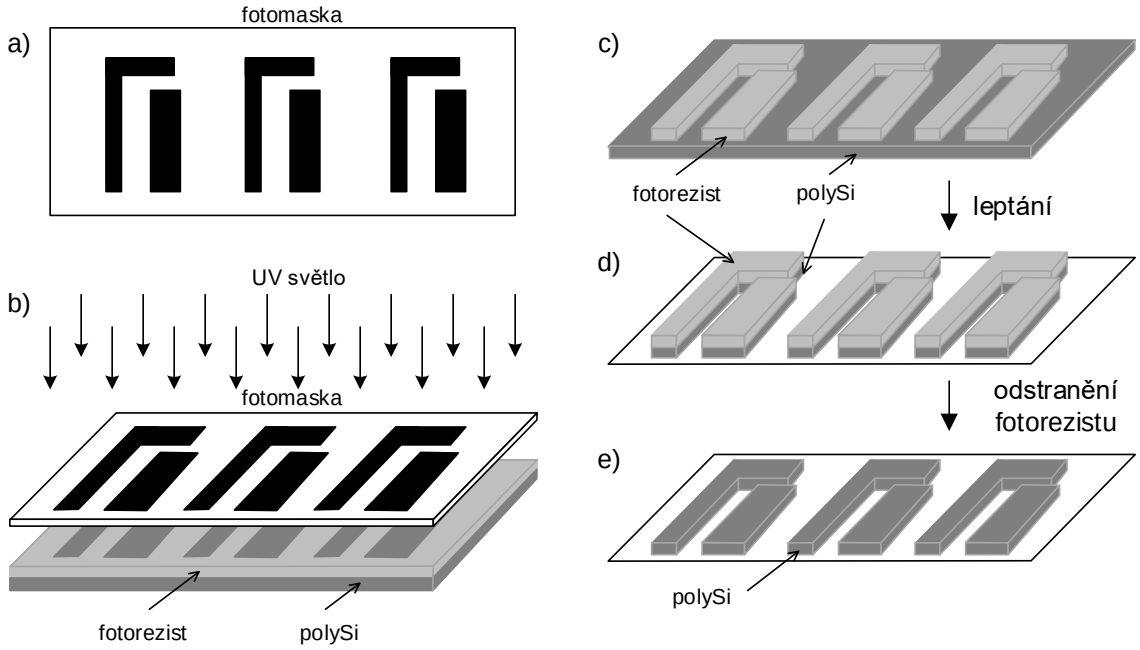
kde n je index lomu v prostoru mezi čočkou a waferem (kterým prochází záření), Θ je maximální úhel dopadu světla (viz. obr. 2.17). Platí čím vyšší numerická apertura, tím vyšší rozlišovací schopnost objektivu a větší zvětšení (viz. rovnice 2.7)



Obr. 5.17: Index lomu v prostoru mezi čočkou a waferem

Fotorezist je organický polymer, který reaguje změnou struktury při vystavení na UV záření. Fotorezist může být pozitivní nebo negativní. U pozitivního fotorezistu exponované části se odleptají (ozářením dochází k porušení vazeb polymerních řetězců). U negativního fotorezistu exponované části zůstávají (fotochemickou reakcí dochází k zesíťování a vytvrzení).

Prvním krokem fotolitografie je nanesení kapky fotorezistu na povrch vrstvy, která má být vyselektována. Při aplikaci fotorezistu je wafer otáčen rychlostí tisíce otáček za minutu, čímž je dosaženo rovnoměrného rozvrstvení fotorezistu. Tloušťka fotorezistu závisí pouze na úhlové rychlosti otáčejícího se waferu. Poté je fotorezist vytvrzen při teplotě 85 až 90 °C po dobu cca 3 minut (tzv. soft-bake). V dalším kroku probíhá expozice - ozáření (UV zářením) fotorezistu přes masku. Proces expozice a následného selektivní odleptání fotorezistu se označuje jako vyvolání. Zbývající fotorezist je vytvrzen při teplotě 110 °C (tzv. hard-bake).



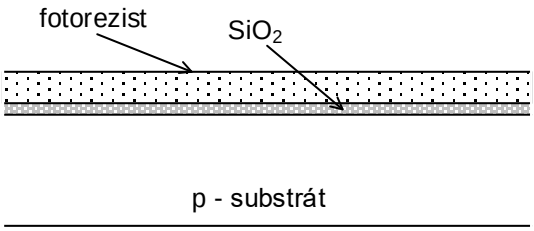
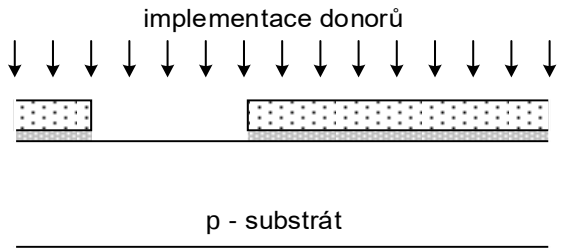
Obr. 5.18: Základní kroky fotolitografie pro vytvoření polySi geometrie: a) fotomaska, b) osvícení, c) vyvolání, d) leptání, e) odstranění fotorezistu

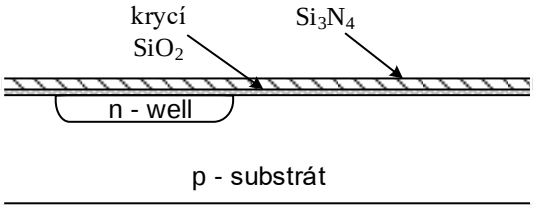
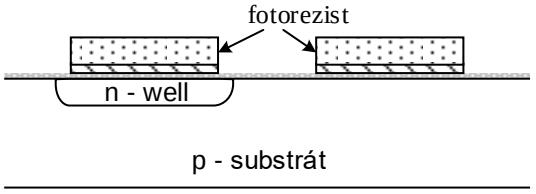
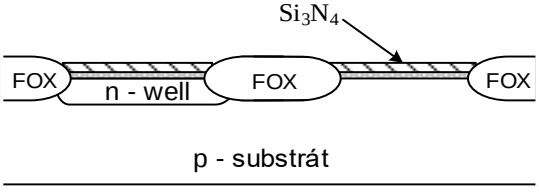
Výše uvedený obr. 2.18 názorně ukazuje základní kroky fotolitografie, kdy jsou vytvořeny geometrické tvary ve vrstvě polySi.

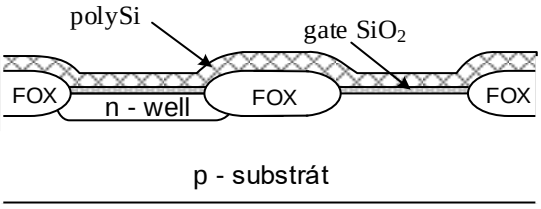
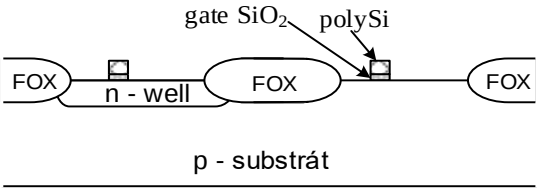
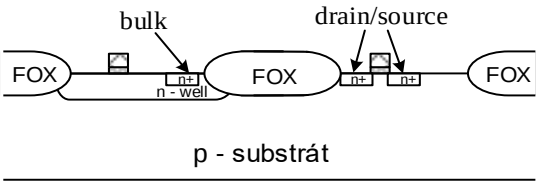
5.3.7 Proces výroby tranzistoru MOS v n-well technologii

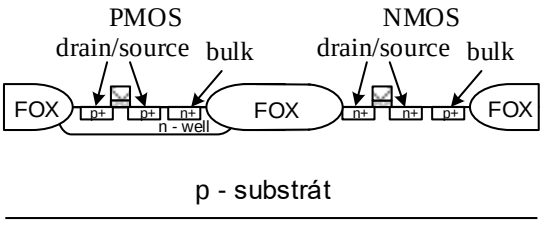
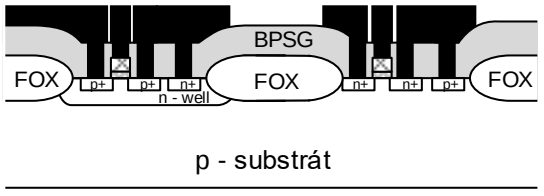
Proces výroby tranzistoru PMOS a NMOS bude ukázán v této kapitole. Jednotlivé procesní kroky, jako jsou oxidace, difúze atd., byly popsány v předchozích kapitolách. Ukázka technologického postupu je zjednodušena [2].

Tab. 5.4: Proces výroby tranzistoru NMOS v N-well technologii

1.	Prvním krokem je růst tenké vrstvy SiO_2 (pomocí oxidace) na povrchu p-substrátu (waferu). Na vrstvu SiO_2 je pomocí depozice nanesen fotorezist.	
2.	Litografickým procesem první masky a leptáním se nad oblastmi příštích tranzistorů s kanálem P odstraní fotorezist a následně SiO_2 (za využití nwell masky) a iontovou implantací se na povrch waferu implantuje donor (prvek s pěti valenčními elektrony - fosfor, arsen, antimon).	

3.	Je vytvořen nwell pro tranzistor PMOS. V dalším kroku se odstraní fotorezist i SiO_2 a termickou difúzí za vysokých teplot dochází k rozdifundování donorů do p-substrátu. Po té je odstraněn původní SiO_2, následně nanesená tenká vrstvy krycího SiO_2 (chrání substrát před stresem způsobeným rozdílnou teplotní roztažností křemíkového substrátu a nitridu křemíku Si_3N_4) a nanesena depozicí po celém waferu vrstva Si_3N_4.	
4.	Následně je nanesen fotorezist a pomocí litografického procesu se odstraní v místech, kde se budou nacházet aktivní oblasti (tranzistory MOS). Po té se selektivně odstraní i Si_3N_4 a zbytek fotorezistu.	
5.	Kvůli izolaci aktivních částí dochází v dalším kroku za pomocí oxidace k růstu relativně tlusté vrstvy izolačního oxidu (FOX) v místech, které nejsou	

	pokryty Si_3N_4 (ten zabraňuje růstu oxidu). Růst FOX zasahuje i pod hranice Si_3N_4 a dochází k zúžení aktivní oblasti.	
6.	Je odstraněn zbývající Si_3N_4 a tenká vrstva SiO_2 bude tvořit gate oxid. Pomocí depozice je po celé vrstvě waferu nanesen polySi, který je potřebný pro vytvoření gate tranzistorů. Nanesený polySi je silně dotován kvůli dosažení dobré vodivosti.	
7.	Využitím fotolitografického procesu je odstraněn polySi a gate oxid. Je ponechán pouze v místech, kde se budou nacházet elektrody gate. Následně se celý wafer pokryje fotorezistem a pomocí fotolitografie jsou odkryta místa, kde pomocí difúze popř. iontové implementace jsou vytvořeny oblasti n+ (source, drain, bulk).	
8.	Následně se celý wafer pokryje fotorezistem a pomocí fotolitografie jsou odkryta místa, kde pomocí	

	difúze popř. iontové implementace jsou vytvořeny oblasti n+ (source, drain, bulk).	
9.	Opět se celý wafer pokryje fotorezistem a pomocí fotolitografie jsou odkryta místa, kde pomocí difúze popř. iontové implementace jsou vytvořeny oblasti p+ (source, drain, bulk).	
10.	Celý čip je pokryt tlustou vrstvou oxidu. Tato vrstva bývá obvykle boro-fosfo-silikátové sklo (BPSG), které má nízkou teplotu přetavení. V místech, kde se mají nacházet kontakty, jsou využitím fotolitografického procesu a leptání vytvořeny díry v BPSG. Následně je zbývající fotorezist odleptán a pomocí depozice je nanesena po celém čipu vrstva metal 1 (hliník popř. sloučenina hliníku a mědi). Opět pomocí fotolitografického procesu a leptání zůstanou na waferu pouze požadované metalové cesty.	

11.	Pro přípravu depozice druhé vrstvy metalu je nanesena další vrstva dielektrického materiálu – nejčastěji sendvičová struktura SiO_2 + sklo (SOG) + SiO_2. Pomocí fotolitografického procesu a leptání jsou vytvořeny v sendvičové struktuře díry pro mezi-metalické propojky (via). Stejně jako u vrstvy metal 1 je metal 2 nanesen depozicí a stejným následným procesem zůstanou pouze požadované spojení metalem 2. Pokud již nebude následovat žádná metalická vrstva, je nanesena ochranná pasivační vrstva – SiO_2 nebo SiN_3.