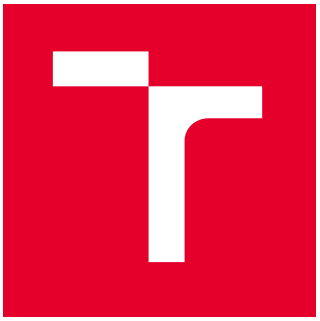
BRNO UNIVERSITY OF TECHNOLOGY

Faculty of Electrical Engineering
and Communication

MASTER'S THESIS

Brno, 2024 Bc. Dominik Klement



BRNO UNIVERSITY OF TECHNOLOGY

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY
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ÚSTAV RADIOELEKTRONIKY

MULTILEVEL CONVERTER WITH ACTIVE GATE DRIVERS FOR FAULT RIDE-THROUGH

VÍCEÚROVŇOVÝ MĚNIČ S AKTIVNÍMI HRADLOVÝMI BUDIČI PRO FAULT RIDE-THROUGH

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

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BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

Master's Thesis

Master's study program **Space Applications**

Department of Radio Electronics

Student: Bc. Dominik Klement ***ID:*** 211152

Year of study: 2 ***Academic year:*** 2023/24

TITLE OF THESIS:

Multilevel Converter with Active Gate Drivers for Fault Ride-Through

INSTRUCTION:

This thesis aims to make a significant contribution to the advancement of fault tolerance in power electronics converters, specifically focusing on the Nested Neutral Point Piloted (NNPP) multilevel converter. Rooted in a thorough review of state-of-the-art literature, the research aims to identify gaps, limitations, and challenges in existing approaches. The goals encompass a comprehensive description of the NNPP converter and other multilevel topologies. The thesis will propose and implement a fault-tolerant algorithm utilizing active gate driving technology, including space vector modulation and active capacitor voltage balancing control. This algorithm is to be implemented in simulation software, and the converter's hardware is to be designed for further real-world testing. The thesis will conclude with a comparative analysis of existing fault-tolerant methods, highlighting their respective advantages and disadvantages. In its final section, the thesis will summarize key findings, discuss potential applications, and propose topics for future research.

Goals

1. Conduct an in-depth analysis and comparison of various multilevel converter topologies, exploring their applications, use cases, functional principles, and differences to provide a broader understanding of their utilization in power electronics.
2. Develop an algorithm that addresses identified limitations in existing nested neutral point piloted converter designs and validate the proposed algorithm through simulation software implementation.
3. Design the converter's hardware and active gate driver to enable future real-world testing, ensuring it aligns with the algorithm's specifications for compatibility with control and measurement signals.
4. Perform a comparative analysis of existing fault-tolerant methods and the proposed method, outlining specific advantages and disadvantages and potential topics for future development of multilevel converters.

RECOMMENDED LITERATURE:

1. CHEN, Jiangui, Yan LI a Mei LIANG, 2019. A Gate Driver Based on Variable Voltage and Resistance for Suppressing Overcurrent and Overvoltage of SiC MOSFETs. Energies [online]. 12(9), 1640. ISSN 1996-1073. Dostupné z: doi:10.3390/en12091640

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4. YU, Jianghui, Rolando BURGOS, Qiong WANG a Ismail AGIRMAN, 2019. Design of a SiC-based Five-Level Stacked Multicell Converter for High-Speed Motor Drives. In: 2019 IEEE Energy Conversion Congress and Exposition (ECCE): 2019 IEEE Energy Conversion Congress and Exposition (ECCE) [online]. s. 4063–4068. ISSN 2329-3748. Dostupné z: doi:10.1109/ECCE.2019.8912728

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Supervisor: doc. Ing. Tomáš Götthans, Ph.D.

Consultant: Dr. Jun Wang, University of Nebraska–Lincoln

doc. Ing. Tomáš Götthans, Ph.D.
Chair of study program board

Abstract

This thesis explores multilevel converters, highlighting their benefits and current/potential future applications. It focuses on the Nested Neutral Point Piloted (NNPP) topology and develops a fault ride-through control algorithm with active capacitor voltage balancing and space vector modulation. The algorithm is validated through simulation. A prototype is designed for experimental validation. The thesis concludes by comparing the proposed fault-tolerant algorithm with existing methods.

Keywords

Nested Neutral Point Piloted Converter, Fault Ride-through, Active gate driver, Multilevel converters, SiC MOSFET, Power Electronics, Stacked Multicell Topology, High reliability

Abstrakt

Tato práce se zabývá víceúrovňovými měniči, popisuje jejich výhody a současné/potenciální budoucí aplikace. Zaměřuje se na „Nested Neutral Point Piloted (NNPP)“ topologii a vývoj algoritmu řízení s aktivním vyrovnáváním napětí kondenzátoru a pokročilou vektorovou modulací pro tuto topologii. Tento algoritmus je ověřen pomocí simulací. Součástí práce je i návrh prototypu pro experimentální ověření. Práce je uzavřena porovnáním vyvinutého algoritmu s již existujícími metodami.

Klíčová slova

Nested Neutral Point Piloted měnič, Fault Ride-through, Aktivný hradlový budič, Víceúrovňový měnič, SiC MOSFET, Výkonová elektronika, Stacked Multicell topologie, Vysoká spolehlivost

Rozšířený abstrakt

Tato práce zkoumá aplikace a výhody víceúrovňových měničů, od trakčních měničů a HVDC přenosových vedení až po potenciální vesmírné aplikace, přičemž zdůrazňuje jejich schopnost snižovat elektromagnetické rušení a zvyšovat spolehlivost. Popisuje pět specifických topologií vhodných pro integraci do HFPP SiC FET modulů. Zaměřuje se na NNPP topologii, zdůrazňuje její výhody a popisuje její princip. Analýza identifikuje potenciální chyby v této topologii, tato analýza vede k vývoji řídicího algoritmu schopného jim odolávat. Algoritmus integruje základní části řízení měniče, včetně aktivního vyrovnávání napětí kondenzátoru a pokročilé vektorové modulace, a je ověřen pomocí simulace. Je navržen prototyp měniče pro experimentální měření a aktivní hradlový budič, který je navržen podle požadavků algoritmu. Práce je uzavřena porovnáním navrženého algoritmu s již existujícími metodami.

Bibliographic citation

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Author's Declaration

Author:	*Bc. Dominik Klement*
Author's ID:	*211152*
Paper type:	*Master's Thesis*
Academic year:	*2023/24*
Topic:	*Multilevel Converter with Active Gate Drivers for Fault Ride-Through*

I declare that I have written this paper independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the project and listed in the comprehensive bibliography at the end of the project.

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Brno, May 16, 2024 ----------

author's signature

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I extend my gratitude to my supervisor, doc. Ing. Tomáš Götthans Ph.D., for his guidance and support throughout this thesis. I also thank Dr. Jun Wang for his professional consultations, which have greatly contributed to the development of this work. His expertise has been invaluable in shaping the direction of my research. Furthermore, I acknowledge the University of Nebraska-Lincoln and Brno University of Technology for their support and resources, without which this thesis would not have been possible. Additionally, I acknowledge the use of AI for text formatting assistance.

Brno, May 16, 2024 ----------

Author's signature

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INTRODUCTION

The focus of this work is to develop a general algorithm for controlling a three-phase multilevel power converter. The algorithm aims to maintain functionality when a fault occurs with reduced output waveform quality until the converter is serviced resulting in fault ride-through capability. This solution is particularly valuable for high-reliability applications in extreme environments. The converter will be simulated and additionally, a physical prototype meeting the algorithm's requirements will be designed for future experimental validation.

Power converters are instrumental in transforming electrical power from one form to another in various applications. These range from low-power, low-voltage systems such as electric bikes to high-power, high-voltage applications such as HVDC grids, wind farms, and heavy industrial machinery as well as the automotive sector, where multilevel converters are a rising trend [1]. In addition, power converters are critical in space applications, enabling efficient power management and distribution aboard spacecraft and satellites [2].

The multilevel converter addresses several shortcomings of a more traditional two-level topology, as low-order harmonics in the output waveform [3] or high overvoltage on the output terminals caused by reflections [4]. However, the improvements in output waveform quality comes at a cost of control complexity [5] and additional components that can lead to fault susceptibility [6].

The current state-of-the-art control solutions mainly focus on the open circuit fault [5], [6], [7], the short circuit fault of multilevel converters is studied, however the proposed solution requires additional components in the current carrying path [8]. The design of the converter and the focus is given on the short circuit failure mode of the switching device as it is the main failure mode [9] of a novel Press-pack type SiC IGBT [10] that was developed in parallel and that is to be used as a switching device in the future versions of this power converter, as well as the fail-to-short behavior being the preferred failure mode for HVDC and FACTS applications [11], [12].

The thesis consists of four chapters. The first chapter provides an overview of multilevel converters, including a comparison with two-level converters and an exploration of current and potential future applications. Various converter topologies are compared to select one for the prototype and control algorithm design. The second chapter delves deeper into the chosen converter topology, analyzing switching subintervals, voltage stresses on main components, and conducting fault state analysis. The third chapter focuses on the detailed development of a specific fault ride-through capable control algorithm tailored to the chosen topology. Hardware control and measurement interface requirements are outlined, and simulation results of the control algorithm are presented. Finally, the last chapter centers on the hardware design of the power converter, selecting components compatible with the control algorithm's requirements.

1. MULTILEVEL CONVERTERS

Multilevel converters are converters where the output voltage waveform is synthesized as a combination of several DC voltages, thus they have the ability to generate a high-quality output with lower total harmonic distortion, with a zero harmonic distortion of the output waveform being obtained with an infinite number of output levels. More levels mean higher voltages can be spanned by series devices without device voltage sharing problems [7].

Depending on the topology, a multilevel converter is usually comprised of identical sub-modules whose series and parallel combinations give the convert the ability to staircase the output voltage waveform and more accurately represent the requested waveform, the difference in the output waveforms can be seen in Figure 1.1.

With the increase of power requirements of many applications a higher voltage is required, for example in the case of HVDC and UHVDC transmission lines, where the voltages can reach levels upwards of 800 kV [8], however the current commercially available semiconductor technology tops up at 6.5 kV [9], [10]. Multilevel converters allow the use of lower voltage switching devices in high voltage applications [11], [12], [13].

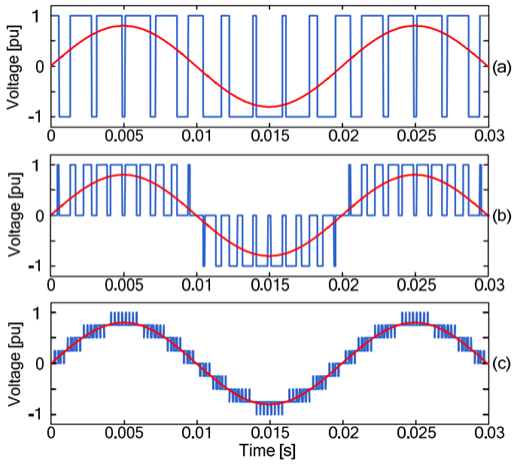


Fig. 1.1 Comparison of output phase voltage waveforms (a) two level converter, (b) three level converter, (c) nine level converter [14].

The advantages of multilevel converters include:

- High-quality output waveform,
- use of lower voltage switching devices for high voltage applications,
- modularity and expandability,
- depending on topology: switch combination redundancy,
- improved efficiency due to switching at fundamental frequency.

Multilevel converters have a number of advantages over traditional two-level converters;

however, they also present some disadvantages. The use of series connection of lower voltage switching devices as opposed to use of switching devices rated for operation at the voltage level of the system leads to increase part count, which inherently decreases the reliability due to potential manufacturing defects or faulty components, this has been mostly solved in the current days [15], but still needs to be taken into account during the failure rate assessment.

When implementing a multi-level converter in a low voltage application, the increase in cost of the components may offset the advantages of increased output waveform quality, that is why multi-level topologies are still a domain of high-voltage converters.

As opposed to a traditional three phase two-level topology, where only six switching devices are controlled, multi-level converters usually have a much greater number of switches with different switching combinations that have different effect on the output voltage as well as in the case of some multi-level topologies the current and its direction flowing through the DC-link capacitors, the voltage balance of them as well as the neutral point current. This results in the need for complex control algorithms that may require significant computational power for the converter to operate at high switching frequencies, which is the case of control of a high-speed electric motor with a high pole pair count resulting in high fundamental frequency.

If care is not taken in the hardware design of a multi-level converter, big commutation loops may occur, which may result in high EMI of the converter, which can in turn affect the performance of sensitive voltage and current sensors used for control, rendering the converter inoperable as well as affect the surrounding subsystems onboard the device.

The disadvantages of multilevel converters include:

- Increased part count,
- control complexity when compared to two-level converters,
- improper design may result in EMI issues,
- depending on topology and number of levels: higher switching losses.

1.1 Applications

Multilevel converters have found successful industrial applications in various fields, including renewable energy integration, high-voltage DC transmission, motor drives, and more. Recent advances in multilevel converter technology have led to new commercial topologies and modulation and control techniques that have improved their performance and efficiency [16].

An example of a use of a multilevel converter may be an MM7 modular multilevel converter from GE Vernova shown in Figure 1.2, such a converter may be used in many applications ranging from MVDC transmission with voltages of up to 100 kV all the way to STATCOM applications with power ranging from 30 to 150 MW. The main advantages of using a multilevel converter topology include the containment of a single

failure at a local submodule level and a transform-less design for applications of up to 36 kV [17].

Fig. 1.2 GE Vernova MM7 modular multilevel converter [18].

Another example of the use of multilevel converters is a Multilevel Highspeed Inverter from BorgWarner shown in Figure 1.3. This converter can, thanks to the multilevel technology operate high-speed electric motors at speeds of up to 180 000 rpm [19]. Such speeds would be very difficult to achieve with traditional topologies due to the extremely high dV/dt on the output terminal.

Fig. 1.3 BorgWarner 850-Volt Multi Level High Speed Converter [20].

High dv/dt can cause voltage spikes and ringing on the leading edge of the voltage pulse, which can lead to high-frequency EMI and damage to the motor windings if the peak voltage is too high. The main problems associated with high dV/dt are motor insulation failure, motor bearing failure and increased levels of RFI [21].

A filter may be introduced at the output of the converter, which will decrease the high dV/dt, but will lead to losses, which can in certain cases be as high as 11.7% [22]. The inclusion of a filter also lowers the volumetric and gravimetric density of the converter,

which can in some applications be highly undesired, such applications may include an extraterrestrial mining machinery, whose cost to launch from earth would be increased and payload capacity reduced.

Application of multi-level converter in motor controllers can due to the lower overvoltage values on the output terminals [4], increase the lifespan of electric motors, reducing their potential downtime and increasing the servicing interval. This can in both terrestrial and space applications mean cost savings.

Multi-level converters are currently being developed for a more potential use in the aerospace industry [23], the number of redundant switching states, when implemented correctly offer added redundancy and can result in fault tolerant systems [24]. With future space developments, including the potential permanent habitations of extraterrestrial objects such as Mars or the Moon, the comfort of the crew needs to be taken into account, the power demand will increase [25], where it will be necessary to increase the voltage of the systems beyond the current norms [26], by using multi-level converters in such applications, redundancy can be achieved with low EMI and RFI.

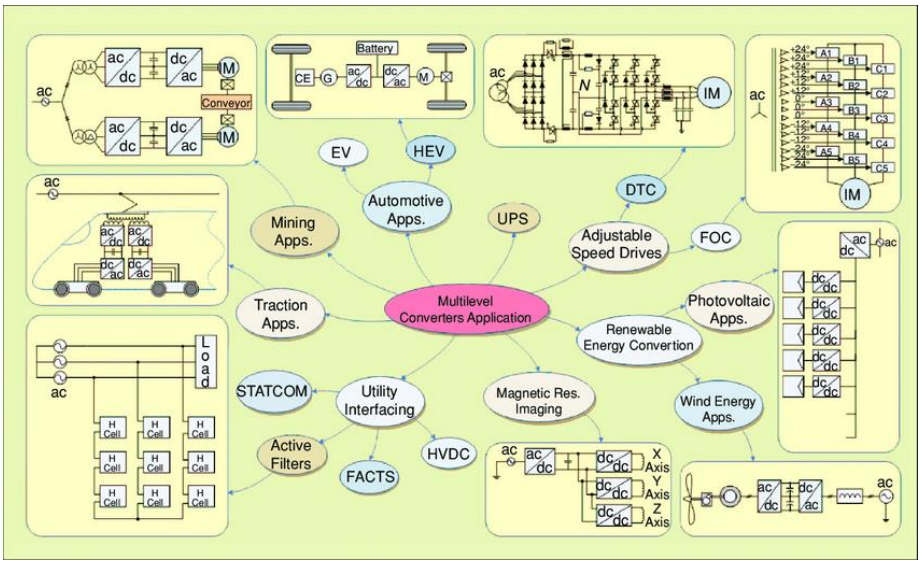


Fig. 1.4 Overview of multilevel converter-driven applications [27].

The use of multilevel converters is extremely broad, an overview is shown in Figure 1.4. Their utilization is only growing, where the advantages in many applications outweigh the disadvantages.

1.2 Converter topologies

Multilevel converter topologies have been widely studied and developed for various applications. A review of existing topologies of multilevel inverters is presented in the following chapters.

This is not a comprehensive comparison as the number of topologies is constantly growing as can be seen in [28], [29], [30] and in the Figure 1.5, where the most popular power converter topologies are shown. Only the five major multi-level converters are considered in this comparison as there is sufficient information available regarding their functional principle and inherent properties.

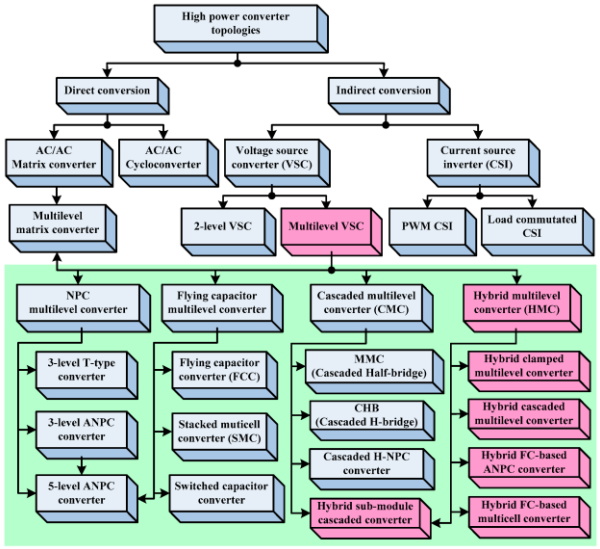


Fig. 1.5 Overview of power converter topologies [31].

This comparison is conducted to gain a better understanding of the underlying concepts of achieving a multi-level output, for most of the topologies compared, the individual switching states are not described as that is not the focus of this thesis, only their functional principle is shown.

Individual topologies have distinctive features, which have their advantages and disadvantages and the choice between them must be made according to the system requirements such as the efficiency target, total harmonic distortion, fundamental frequency, system voltage etc. For the development of the control algorithm a Nested Neutral Point Piloted topology was chosen, the choice is described in more detail in chapter 2 of this thesis.

1.2.1 Neutral Point Clamped

Neutral Point Clamped (NPC) converter is the most commonly used multilevel converter topology [32]. And is widely used in medium voltage applications [33]. The topology is characterized by the use diodes to clamp the output voltage and is shown in Figure 1.6.

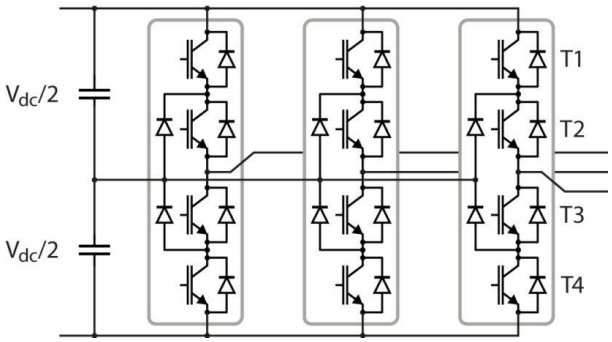


Fig. 1.6 Three-phase Neutral Point Clamped Multilevel converter topology [33].

Care needs to be taken to keep the DC midpoint balanced as at high modulation indices a low frequency ripple occurs on the neutral-point voltage and steady-state unbalance in the neutral-point voltage may arise due to a variety of factors such as component imperfections, transients and other nonidealities and imbalances [34].

The Neutral point clamped converter has three output levels per phase and varies between three states *"Positive", "Zero"* and *"Negative"* as shown in Figure 1.7, where the current flow for one leg of the converter can also be seen [35].

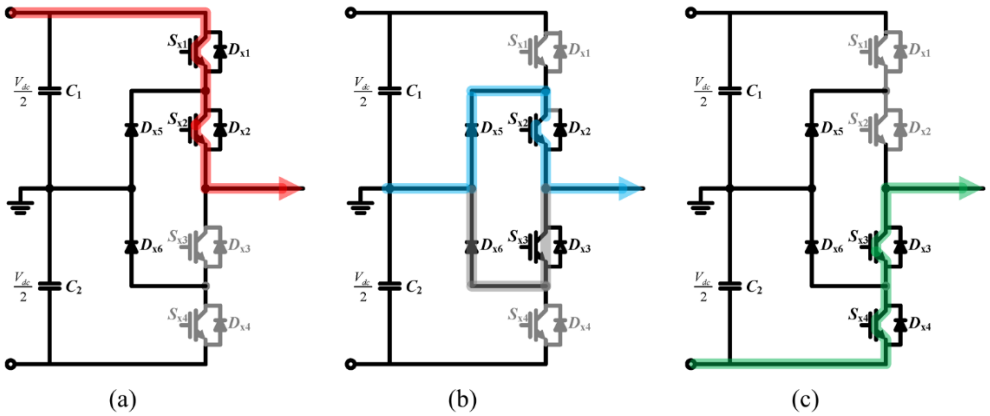


Fig. 1.7 Neutral Point Clamped converter single leg states (a) state "Positive", (b) state "Zero", (c) state "Negative" [35].

The resulting output then is *+E*, *0* and *-E*, respectively. Whereas the two-level converter only switches between *+E* and *-E*. The output waveforms of the converter are shown in Figure 1.8.

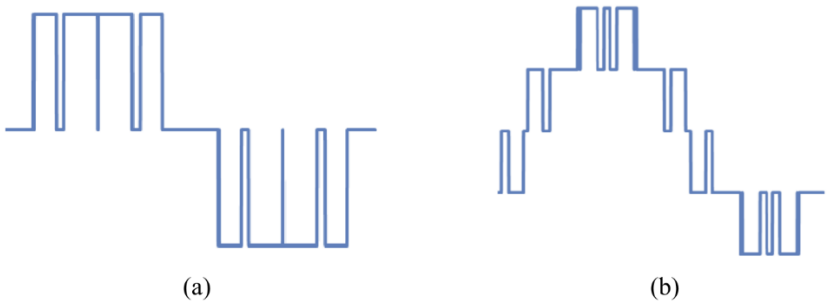


Fig. 1.8 Neutral Point Clamped converter output waveforms a) leg output b) phase-to-phase [36].

Table 1.1 contains an overview of the basic switching states of a single leg of the neutral point clamped converter topology from Figure 1.7. For each of the three switching states the conduction state of each of the switching devices is presented as well.

Table 1.1 Neutral Point Clamped converter switching states

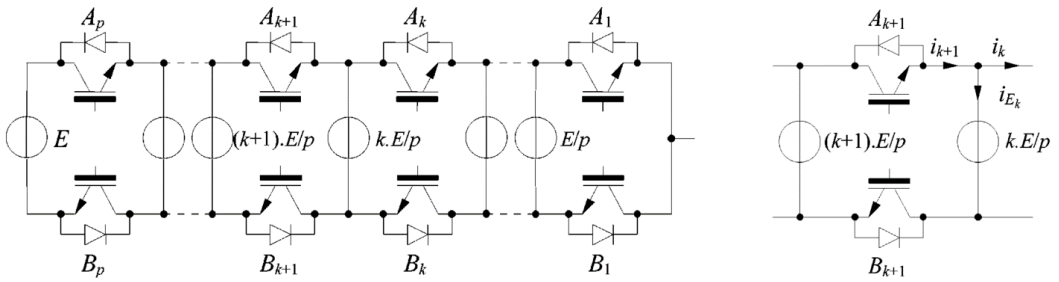
Switching device state				**Output voltage**	**Switching state**
Sx1	**Sx2**	**Sx3**	**Sx4**		
ON	ON	OFF	OFF	+E	Positive
OFF	ON	ON	OFF	0	Zero
OFF	OFF	ON	ON	-E	Negative

Overall, the three-level output of the neutral point clamped has clear advantages over the traditional two-level converter, such as reduced switching losses due to only half of the voltage being switched, this also gives the topology an advantage of for lower voltage rating of switching devices such as MOSFETS or IGBTs, which may result in lower cost and lower conduction losses due to more mature technology.

The output will also only have lower current ripple and half of the voltage transient [37]. These advantages come at a cost of more complex control, the unequal loss distribution among switching devices and the need for DC link capacitor voltage balancing [38].

1.2.2 Flying Capacitor

The flying capacitor topology, often referred to as the multicell topology, is a type of multilevel converter that consists of a series of elementary cells. The general converter topology is shown in Figure 1.9a. The topology is comprised of *p* pairs of three quadrant switches, separated by *p-1* flying voltage sources [39] shown in Figure 1.9b.



(a) (b)

Fig. 1.9 Flying Capacitor topology (a) general converter, (b) single cell [39].

The number of output levels N_{output_lvls} is directly proportional to the number of cells in series and can theoretically be infinite and can be expressed by an equation [40]

$$N_{output\_lvls} = p + 1, \tag{1.1}$$

where p is the number of single cells in the converter leg. Figure 1.10 shows connection of three elementary cells and two flying capacitors per phase with a shared DC link capacitor C_3.

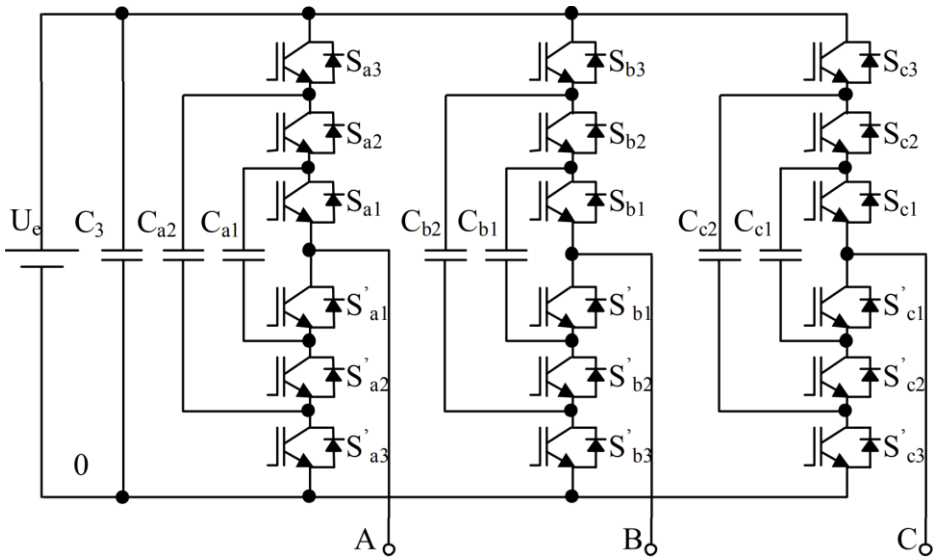


Fig. 1.10 Three-phase four level Flying Capacitor Converter [41].

The voltage on the flying capacitors may become unbalanced, in the past an open-loop balance booster was used [39], that however adds additional components to the circuit and may introduce losses, the solution for active closed-loop control was proposed in [42].

In summary, flying capacitor converters consist of multiple cells connected in series to distribute the voltage constraints amongst them and to improve the output waveform. They have been shown to be suitable for various applications such as for example the

input converter of GEC/ACEC T13 Locomotives and three-phase Alstom electric motor inverters [43].

1.2.3 Modular Multilevel Converter

The modular multilevel converters consist of submodules that can be of different types, Although the most commonly used submodules are the half- and full-bridge topologies [44], several alternative submodules topologies to fulfill different objectives have been proposed, such as a modified active neutral point clamped submodule proposed in [45]. Several submodule configurations are shown in Figure 1.11

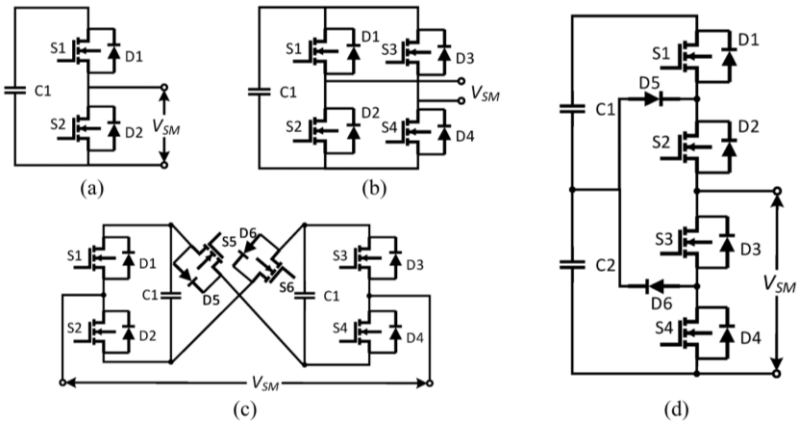


Fig. 1.11 Modular Multilevel Converter submodules (a) half-bridge, (b) full-bridge, (c) CCSM, (d) NPCSM [46].

Modular multilevel converter is a cascaded connection of a large number of the described submodules, they are arranged in groups called arms, which can be connected in several configurations as shown in Figure 1.12.

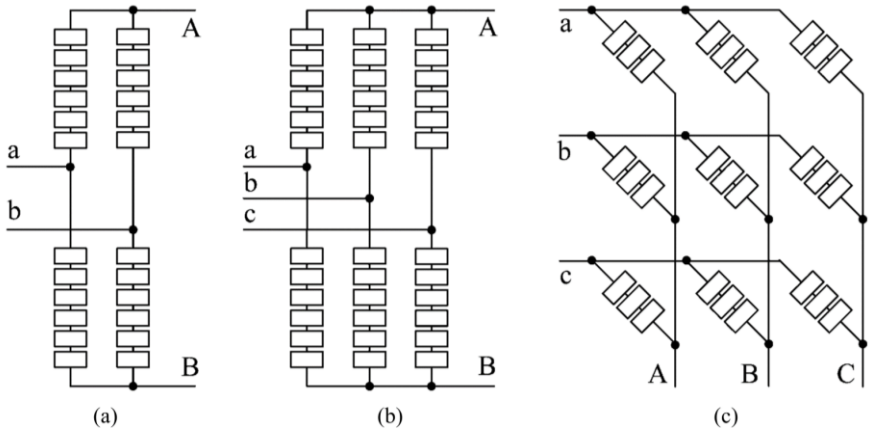


Fig. 1.12 Modular Multilevel Converter submodule arm arrangements (a) single-phase, (b) three-phase/(DC/single-phase), (c) B2B [47].

A five level output can be achieved in a three layer stack of the HFPP module design proposed in [48]. The half-bridge based multilevel converter is a highly customizable

converter with modular and transformer-less construction, half-bridge cell is essentially a DC-chopper, where the voltage is either equal to the voltage of the intermediate capacitor or it is zero, the states of the switching devices are complementary [49].

The advantages and disadvantages are similar to other topologies, the output waveform has a better quality, but over the two-level converter, there is need for more power semiconductor switches and their gate driving circuitry, which in turn increases the footprint as well as costs of the converter [50]. This topology also requires an inductor on each side of a single leg of the converter [51].

1.2.4 Nested Neutral Point Piloted

Nested Neutral Point Piloted sometimes also called Stacked Multicell topology [31] is a hybrid multilevel topology . The topology is inherently modular and exhibits a natural flying capacitor voltage balancing properties, however input variations can occur, which can influence the balancing property and can negatively influence the performance of the converter [52], this can be solved by an external balance booster circuit as in [53], [54], [55] or an active voltage balancing can be implemented, which will be described in further detail in the chapter 3.1.

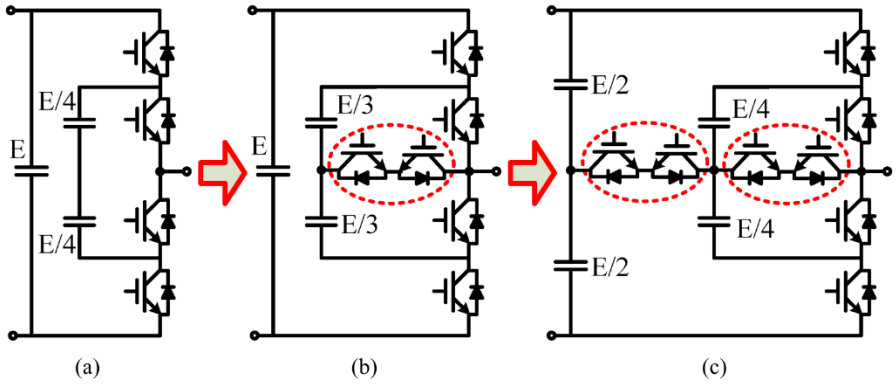


Fig. 1.13 Nested Neutral Point Piloted topology derivation (a) three level FC cell, (b) 4L NNPC converter, (c) NNPP converter [31].

The topology for a single leg of a five-level three-phase stacked multicell is shown in Figure 1.13c, the topology is derived as a combination of a Flying Capacitor cell and an Nested Neutral Point Clamped converter topology [31].

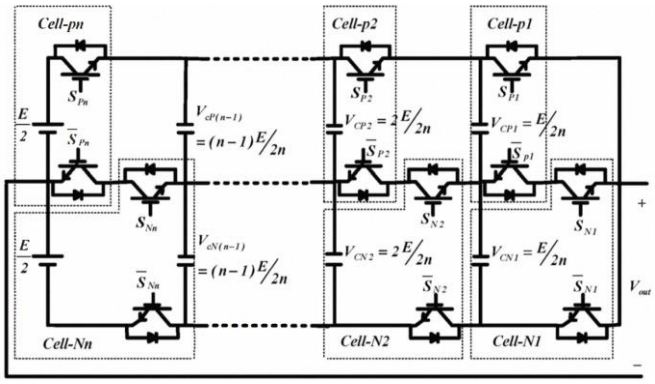


Fig. 1.14 Nested Neutral Point Piloted Converter general single leg topology [56].

A general topology for a nested neutral point piloted leg is shown in Figure 1.14. The circuit is made up of elementary commutation cells connected in n stages with p cells connected in a $n \times p$ structure, where the number of output levels N_{output_lvls} can be calculated by the following equation [57]

$$N_{output\_lvls} = (n \cdot p) + 1. \tag{1.2}$$

For this thesis, only *2x2* (two cells in series and two stacks) configuration is considered as five-level output waveform can be achieved using three layers of the HFPP Press-pack design. As the implementation of a NNPP topology with fault ride-through is the focus of this thesis the switching states as well as the potential faults are described in more detail in chapter **X**. The voltage $V_{C_{ij}}$ across the flying capacitors is [57]

$$V_{C_{ij}} = \frac{i \cdot E}{n \cdot p}, \tag{1.3}$$

where i is the index of the capacitor in a circuit, E is the input voltage, n is the number of stages and p is the number of cells in series [53]. The voltage constraint V_{sw} on the switching devices is the same across all switches and is equal to [57]

$$V_{sw} = \frac{E}{n \cdot p}, \tag{1.4}$$

where E is the input voltage, n is the number of stages and p is the number of cells in series [54]. The main advantage of this topology over a classical multilevel converter is the possibility to share the voltage constrains across the circuit, therefore the voltage rating of the flying capacitors and switching devices are reduced. The disadvantages are similar to the majority of the multilevel converter topologies, a large number of power semiconductor switches are needed, which inherently reduces the reliability of the converter. Although low-voltage-rated switches can be utilized in a multilevel converter, each switch requires a gate driver and protection circuits [55].

1.2.5 Active Neutral Point Clamped

The initial proposed concept is shown in Figure 1.15, but the topology was due to the three floating capacitors excessive in terms of costs as well as the volumetric density, to reduce the number of floating capacitors, capacitors C2 and C3 can be eliminated resulting in a simplified topology shown in Figure 1.16.

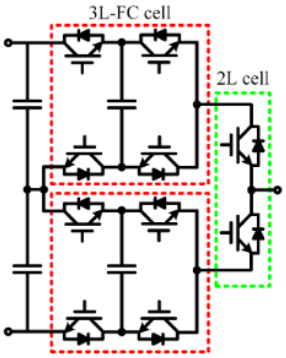


Fig. 1.15 Initial Active Neutral Point Clamped Converter topology [58].

Active Neutral-point-clamped converter is a hybrid multilevel converter based on a cascade of a three-level Flying capacitor topology and a traditional two-level topology. The switches of 3L FC cells operate in low (fundamental) frequency while switches of the two-level cell operate in high (switching) frequency [49].

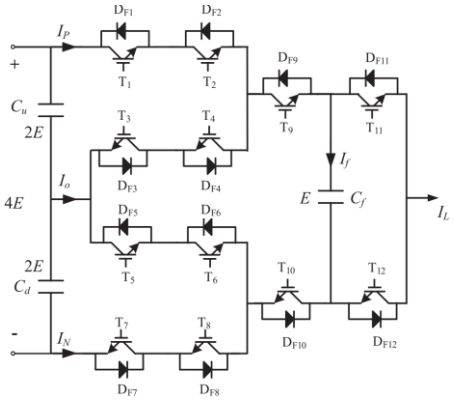


Fig. 1.16 Simplified Active Neutral Point Clamped Converter topology.

The removal of capacitors C2 and C3 however resulted in the elimination of the natural balancing aspect of the converter, this was solved in [59], [60] by the implementation of active capacitor voltage control.

The advantage of this topology is that it requires only one more capacitor per phase than a NPC three-level converter [59] to achieve a five level output waveform, but the disadvantage is the unequal distribution of the switching device losses, this is however potentially solvable by the use of different optimization strategies as shown in [60].

2. NESTED NEUTRAL POINT PILOTED CONVERTER

The selection of the multilevel converter topology was based on a paper, where a novel high-frequency press-pack (HFPP) SiC FET module was proposed. This paper was a part of development from the same laboratory as this thesis is. The nested neutral point piloted topology is easily scalable and has switching state redundancy properties, which allows for a fault tolerant/ride-through capabilities, where a fail-to-short behavior of the switching device is expected, a five-level circuit can be achieved within a three layer structure of the HFPP module and can be seen in Figure 2.1a allowing for operation under medium voltage, high current and fast switching transients [10], in Figure 2.1 other multilevel topologies achievable within the three layer HFPP structure can be seen.

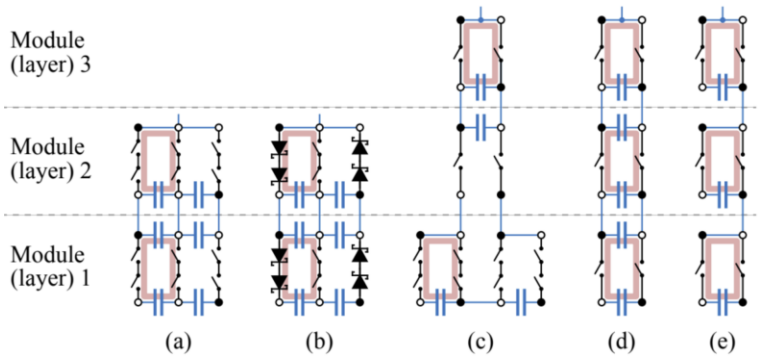


Fig. 2.1 HFPP SiC Module topologies: (a) 5L-NNPP, (b) 5L-Vienna-NNPP, (c) 5L-ANPC, (d) 5L-FC, (e) 5L-MMC [48].

The aim of this thesis is to develop a prototype that uses components available off the shelf, to evaluate and gain experience with the control of such a converter topology at a lower voltage and lower power. The control algorithm that is to be developed is then to be used during the experimental phase of the implementation of the HFPP module, the focus of current state of the art papers in this field are on the open circuit fault, where the short-circuit fault is only studied briefly and for fault tolerance capability external devices are used in [61].

In this chapter the nested neutral point piloted topology is to be analyzed further with focus on its subinterval analysis, the effect of the switching states on the capacitor voltages and neutral point current as well as the types of faults which can occur.

2.1 Subinterval analysis

For this chapter only a five-level topology is considered as that is the focus of this work and the limitation of the HFPP SiC module. A general single phase five-level nested neutral point piloted converter circuit is shown in Figure 2.2.

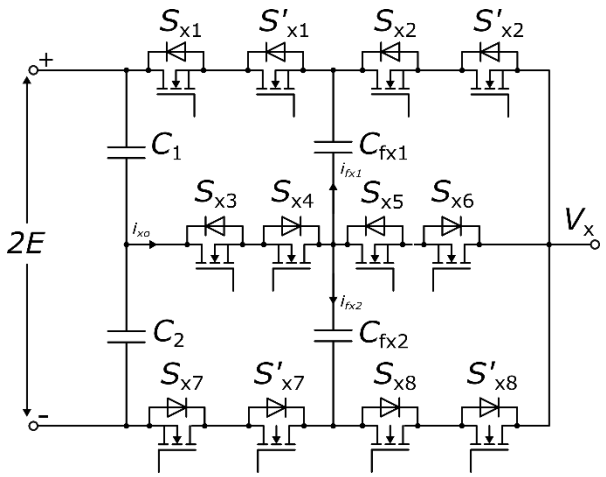


Fig. 2.2 General five level single phase NNPP Topology.

The five-level output can be achieved using nine combinations, each with different effects on the flying capacitors and neutral point current, which is important for achieving a balanced capacitor voltage and the effect is used in the active capacitor voltage balancing algorithm, which is described in chapter 3.1, this balance is important for acquiring a high-quality output waveform. Table 2.1 shows the state of the switching devices for each of the nine combinations as well as the effect on the currents in the circuit [62].

Table 2.1 NNPP Converter Switching states overview

V_N	S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	S_{X7}	S_{X8}	V_{OX}	I_{FX1}	I_{FX2}	I_{X0}
V_1	1	1	1	0	1	0	0	0	E	0	0	0
V_2	1	0	1	0	1	1	0	0	E/2	I_{ox}	0	0
V_3	0	1	1	1	1	0	0	0	E/2	$-I_{ox}$	0	I_{ox}
V_4	1	0	1	0	0	1	0	1	0	I_{ox}	I_{ox}	0
V_5	0	0	1	1	1	1	0	0	0	0	0	I_{ox}
V_6	0	1	0	1	1	0	1	0	0	$-I_{ox}$	$-I_{ox}$	0
V_7	0	0	0	1	1	1	1	0	-E/2	0	I_{ox}	I_{ox}
V_8	0	0	1	1	0	1	0	1	-E/2	0	$-I_{ox}$	0
V_9	0	0	0	1	0	1	1	1	-E	0	0	0

In Figure 2.3 two of the nine combinations are shown, the rest is in appendix A. These combinations are shown for a single leg of a three-phase converter, where the neutral point is referred to as ground point for the output voltage measurement. The switching devices were replaced by SPST switches to better animate the conductive path.

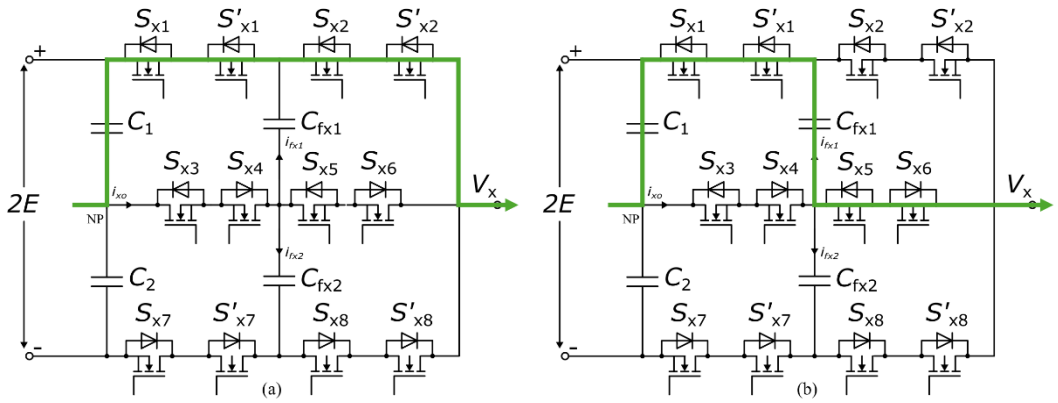


Fig. 2.3 NNPP Topology subintervals (a) V_9, (b) V_8.

2.2 Types of faults

According to [63], approximately 51% of faults in power converters is caused by semiconductors and capacitors. In a survey from [64] power device was selected by 31% of the respondents as the most fragile component, making it the most selected option as can be seen in Figure 2.4.

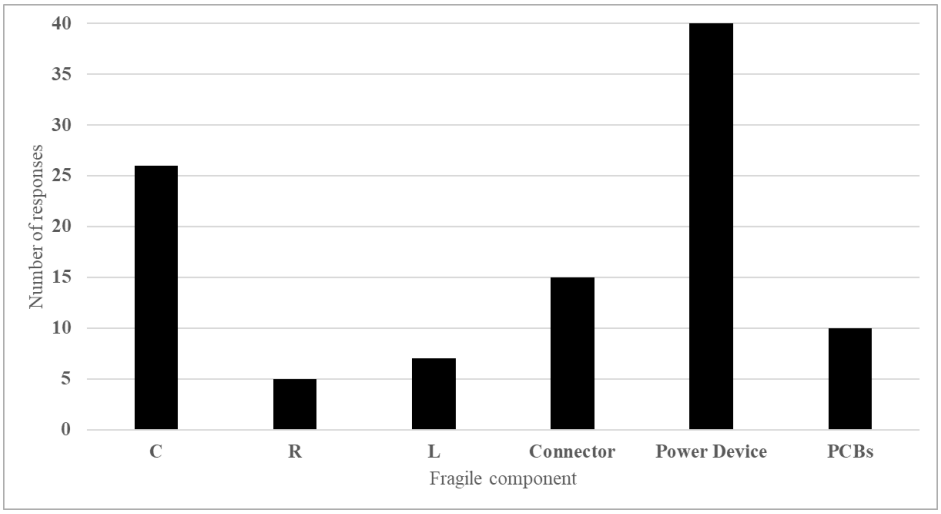


Fig. 2.4 Results of survey on power converter fault causes.

Based on these sources, the focus is put on the fault analysis of the switching devices and fault of other devices such as capacitors, gate drivers etc... is not considered. The failure rate of the switching devices and the converter configuration itself is also not described as it was already sufficiently described in [65] as well as other literature.

Two common fault modes of a traditional switching device are open- and short-circuit faults, but considering the use of HFPP Press-pack switching module, where the aim is to have a fail-to-short behavior the open-circuit fault is less prevalent then in case of a wire-

bond, where a bond wire fusing leads to an open circuit [66], only short-circuit faults are to be analyzed and considered in the development of the control algorithm.

A short-circuit fault is the inability of a switch to stop conducting when a turn on signal is no longer present. This can due to the amount of energy present in power electronics converters cause severe consequences not only on the switch, but also on the connected components, such as the capacitors or the PCB of the converter and can, if present for longer than the short-circuit withstand capability guarantee of the manufacturer lead to thermal runaway [67].

According to [61], where a short-circuit analysis of the nested neutral point piloted circuit topology was conducted, the fault of the converter can be grouped into two groups; the outer cell fault and the inner cell fault in figure 2.5 the group division is shown.

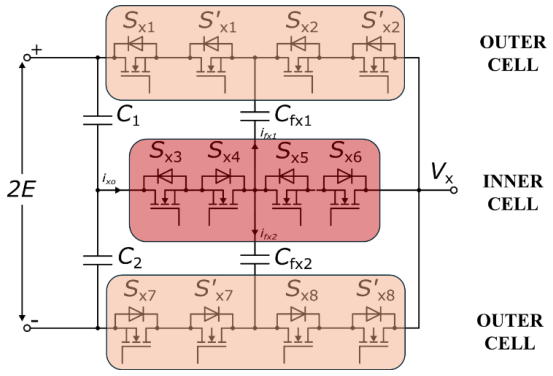


Fig. 2.5 NNPP Converter fault type division.

2.2.1 Outer cell fault

The outer cell fault is fault of the switching devices S_{x1}, S'_{x1}, S_{x2}, S'_{x2}, S_{x7}, S'_{x7}, S_{x8} and S'_{x8}, where x is the phase leg marking of the converter. As each of the switches is redundant, and when failure occurs, on for example S_{x1}, the switch S'_{x1} can still be used to control the circuit, however the switch would have to withstand a bigger voltage that it may be rated to, therefore the solution would be to either use another pair of switching devices in series or to increase the voltage rating of the switching device used. Due to this reason and the simplicity of solving this fault, it is not considered during the development of the proposed control algorithm but should be considered for commercial applications.

2.2.2 Inner cell fault

The inner cell fault is defined as the short circuit failure of the switching devices S_{x3}, S_{x4}, S_{x5} and S_{x6}. When, for example, the switching device S_{x3} fails, the effect on the circuit is during the subintervals V_6, V_7 and V_9, during which a current loop would be formed by switching devices S_{x3}, S_{x7}, S'_{x7} and S_{x4}. This current loop would force the energy from the DC link capacitor C_2 to flow to the flying capacitor C_{fx2}, this current would be extremely high as the capacitors used in power converters have low ESR and ESL and could cause damage to the components in the circuit.

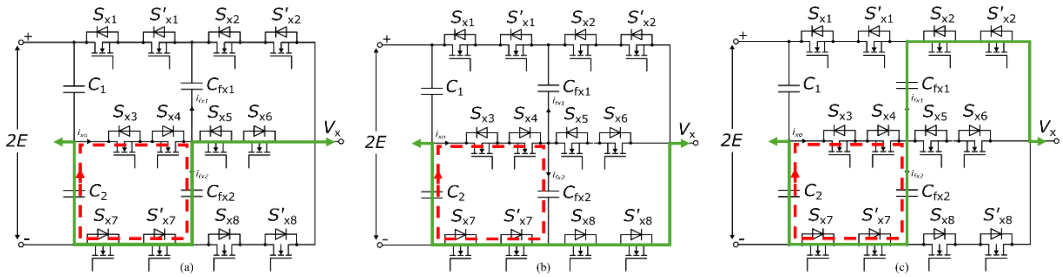


Fig. 2.6 NNPP Converter inner cell fault current loops during (a) subinterval V_6, (b) subinterval V_7, (c) subinterval V_9.

The resulting current loops for this example are shown in Figure 2.6. Where the effect of the short-circuit failure of the switch S_{x3} can be seen. Similar procedure was taken during the evaluation of the rest of the switching devices in the inner cell group. The conclusion is summarized in table 2.2**.**

Table 2.2 NNPP Converter inner cell fault current loop overview

Switch at fault	**Current loop formed in subinterval**
S_{x3}	V_6, V_7, V_9
S_{x4}	V_1, V_2, V_4
S_{x5}	V_4, V_8, V_9
S_{x6}	V_1, V_3, V_6

The inner cell fault has the potential to be destructive and influence the functionality of the converter. Therefore, an algorithm is to be proposed in this thesis to deal with the issue of current loops forming when a short-circuit fault occurs in one of the described switches. In [61] external devices such as mechanical switches and fuses are used to achieve this, but this requires additional components in the high current path, which is undesirable. An active gate control is to be implemented to mitigate the external components in the high current path and instead, use the active region of the switch utilizing gate-source voltage manipulation of the switching device to detect and to resolve a short-circuit fault, this is described in detail in the chapter 4.4.

3. CONTROL ALGORITHM

The control algorithm is the main part of this thesis, the goal is to develop an algorithm to control a three-phase nested neutral point piloted converter with a fault ride-through capability as well as advanced features such as active capacitor voltage balancing, space vector modulation of the output voltage for an optimal performance when operating with AC motors as well as third harmonic injection to improve the performance of the converter. Feedback loop to control the direct axis and the quadrature axis current is also to be implemented to allow Field-Oriented Control of the connected motor. High switching frequency is to be used to allow the use of motors with a high number of pole pairs. Additional features such as Flux-weakening, MTPA and other high-performance motor specific features shown to have the ability to improve the overall system performance are not considered in the design of the control algorithm nor the converter as they have been previously implemented as shown in [68], [69], [70], [71].

Most of the features listed have been previously implemented and are mostly commercially available, except for the method for fault ride-through, which is described in the chapter 3.5. At the time of writing, no paper has been presented to use the proposed method.

3.1 Active capacitor voltage balancing

In order to achieve an optimal performance of a nested neutral point piloted converter, it is crucial to achieve balance of the voltages of the capacitors [72], [73]. This balance can be in many multicell converter cases be achieved naturally [74], [75], [76], however such balancing property is usually dependent on the properties of the connected load and on the use of Phase Shifted Pulse Width Modulation control scheme as shown in [77] and [78]. A balance booster is proposed in [79], it is a resonant RLC circuit, that accelerates the natural balancing property of the converter [80], this however introduces power losses. As fault ride-through capability is the main requirement for the control algorithm, a reliance on the natural balancing property either with or without the use of a balance booster is not sufficient as the load condition in a three-phase circuit may change dynamically depending on the motor/grid load as described in [81], [82] and [83]. Therefore, an active capacitor voltage balancing algorithm needs to be implemented, many solutions have already been presented such as [84], [85] and [86]. These algorithms use the properties of the different subintervals and their effect on the current flowing through the neutral point and the two flying capacitors.

A balance of the capacitors voltages was in the first version of the algorithm achieved by slightly modifying the ACVB solution described in [87], where a dynamic model of the neutral-point voltage of the nested neutral point piloted topology is established. This model is then used to calculate the zero-sequence voltage component. Such a solution has

been previously used in different topologies such as ANPC in [88] and NPC in [89]. A zero-sequence component is zero in case of symmetrical load, however due to conditions described previously an asymmetrical load may be formed on the output of the converter, therefore between the neutral points, there is a voltage difference, which is referred to as the zero sequence voltage [90], which in turn influences the DC-link capacitor balance.

From the measured voltages V_{c1} and V_{c2} of the DC-link capacitors, we can calculate the voltage imbalance and using the known capacitance C of the DC-link capacitor we can calculate the neutral point current $I_{balance}$ which is required to achieve their balance

$$I_{balance} = \frac{C \cdot \frac{(V_{c2} - V_{c1})}{K}}{T_s}, \tag{3.1}$$

where $I_{balance}$ is the neutral point current, C is the capacitance, V_{c1} and V_{c2} are the voltages of the DC-link capacitors, K is the number of switching cycles that are used to achieve the neutral-point voltage-balance and T_s the switching cycle.

By applying $I_{balance}$ for K switching cycles a balanced state of the DC-link capacitors is achieved. To achieve the $I_{balance}$ current a zero-sequence voltage component is calculated from the geometric relationship and is summed together with the reference signals for the three phases of the converter. The actual reference voltage signals u_x for each of the phases then are

$$u_x \begin{cases} u_a = u_{a0} + u_z \\ u_b = u_{b0} + u_z \\ u_c = u_{c0} + u_z \end{cases}, \tag{3.2}$$

where u_{a0}, u_{b0} and u_{c0} are the reference voltages of the three phases before adjustment and u_z is the zero-sequence voltage, to also achieve the regulation of the flying capacitors an optimal zero-sequence voltage selection method is proposed in [73].

This method results in a stable and fast balancing of both of the DC-link capacitors as well as the flying capacitors, however due to the requirements to control a high-speed motor resulting in high switching frequency as well as the additional computational burden of the fault ride-through capability and space vector modulation a simpler method was used. Slightly sacrificing the balancing accuracy of the converter but giving greater flexibility in the development of the fault ride-through capability by simplifying the subinterval selection procedure.

The method used in the final control algorithm is described in detail in [91]. First based on a space vector modulation algorithm that is described in Chapter 3.3 target vector is determined, from the target vector and the sector of the voltage space vector diagram in which the target vector lies, the three basic vectors with the lowest resulting common mode voltage can then be calculated

$$U_{com} = \frac{E \cdot [(V_a - 2) + (V_b - 2) + (V_c - 2)]}{12}, \tag{3.3}$$

where V_a, V_b, V_c are the phase voltage outputs. Based on their distance d_i of to the target refence vector $\boldsymbol{V_{ref}}(V_g^*, V_h^*)$ in the *gh* coordinate system the two nearest vectors are selected; the distance is calculated as

$$d_i = \sqrt{\left(V_g^* - V_{gi} + \frac{1}{2}V_h^* - \frac{1}{2}V_{hi}\right)^2 + \frac{3}{4}(V_h^* - V_{hi})^2}\,, \tag{3.4}$$

where (V_{gi}, V_{hi}) is the coordinate of $\mathbf{V}_i$ (i = 1, 2, 3), from the two vectors then based on the state of the flying capacitor voltages V_{fx11} and V_{fx12} subintervals are chosen, which minimize the voltage deviation of their voltages, the flowchart of the selection process is then shown in Figure 3.1.

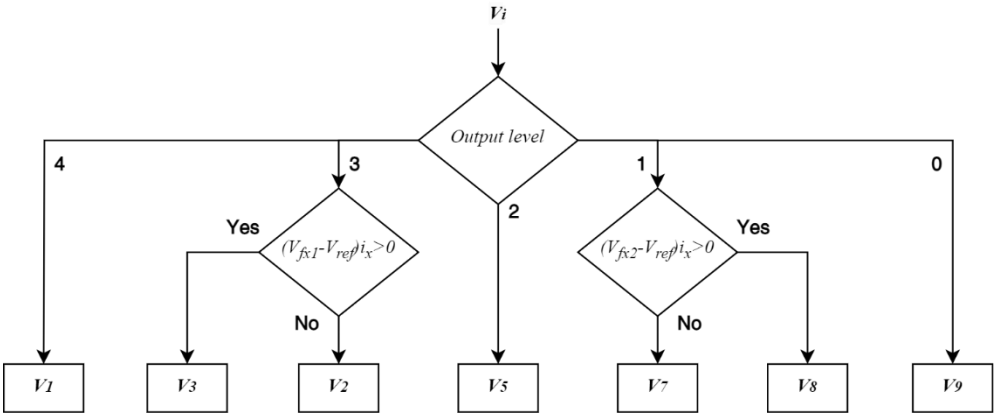


Fig. 3.1 Flying capacitor selection process flowchart [91].

After choosing the two subinterval candidates the average value of the neutral point current I_{on} can be calculated for each of them

$$I_{on} = \sum_{x=a,b,c}(S'_{x1} + S_{x4} - 1)I_x, \tag{3.5}$$

where x represents each of the three phases and S'_{x1} the negation of the state of the switching device S_{x1} and I_x the output current. Subinterval with the minimal result of the following equation is selected as the final one to be used

$$\Delta v'_{on} = \Delta v_C + \Delta v_0 = \frac{v_{fC1} - v_{fC2}}{2} - \frac{I_{on}T_s}{2C}, \tag{3.6}$$

Where v_{fC1} and v_{fC2} are the voltages of the capacitors, I_{on} the neutral point current, C their capacitance and T_s the switching cycle. This algorithm is then implemented in the simulation as a block shown in Figure 3.2 and the results of the balancing properties are shown in Figure 3.16 as a part of the simulation chapter 3.6.1.

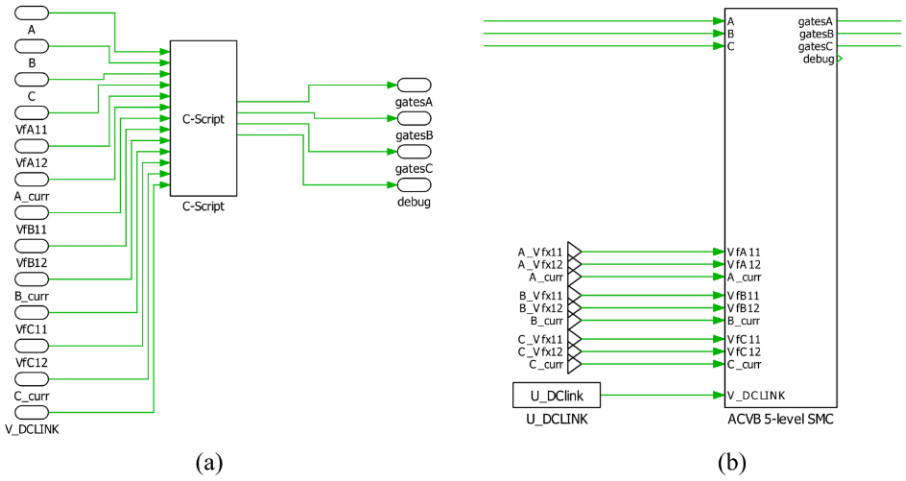


Fig. 3.2 Active Capacitor Voltage Balancing block in simulation software (a) internal structure, (b) block in schematic.

3.2 Coordinate transformations

Coordinate transformations play a crucial role in advanced control of three-phase circuits, particularly in motor control applications. These transformations enable the conversion of three-phase AC values from and into *αβ* reference frame or to the *dq* reference frame, allowing for more straightforward implementation of control algorithms and improved regulation of speed and torque of an electric motor. Coordinate transformations are an integral part of three-phase circuit control as shown in [92], [93] and [94]. Figure 3.3 shows the layout of the transformation implementation for a three-phase motor.

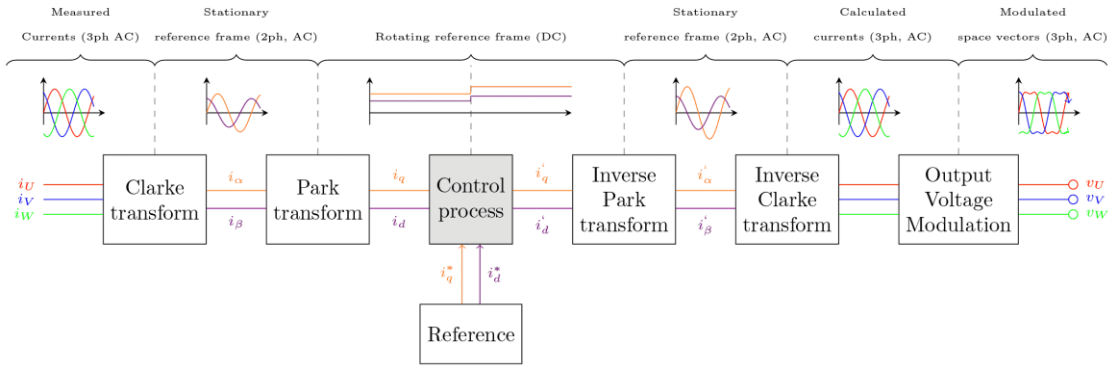


Fig. 3.3 Three-phase control block diagram [95].

3.2.1 Clarke transformation

Clarke transformation also known as *alpha-beta (αβ)* [96] transformation is utilized to simplify the analysis and control for example of three-phase electric motors, where the measured current from each of the three phases on the output in case of a balanced load

into two axis in a stationary reference frame allowing for simpler processing. Together with Park transform and their inverse transformations it is commonly used in Field Oriented Control employed in motor drives for example [97], [98] and [99].

The following equation [100] shows how the components are calculated for a general three-phase system in a matrix form:

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \frac{2}{3} \times \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}, \tag{3.7}$$

where V_a, V_b, V_c are the three-phase components, in this case the output voltage and V_α, V_β the alpha and beta components respectively and V_0 the zero component, which is in case of a balanced system equal to zero [100]. The individual components can then be calculated

$$\begin{cases} V_\alpha = \frac{1}{3}(2 \cdot V_a - V_b - V_c) \\ V_\beta = \frac{1}{\sqrt{3}}(V_b - V_c) \\ V_0 = \frac{1}{3}(V_a + V_b + V_c) \end{cases}. \tag{3.8}$$

These calculations are implemented in the simulation as a subsystem block with two functions shown in Figure 3.4.

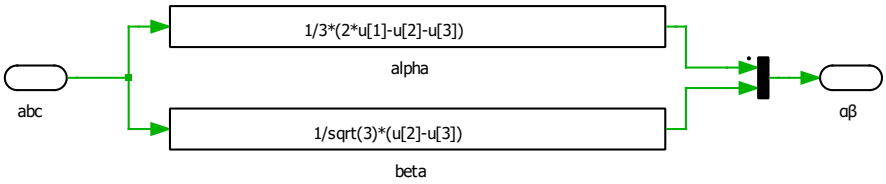


Fig. 3.4 Clarke transformation implementation in simulation.

Figure 3.5 shows the output of the subsystem block in simulation. This output is generated based on the current measurement obtained from a three-phase symmetrical load.

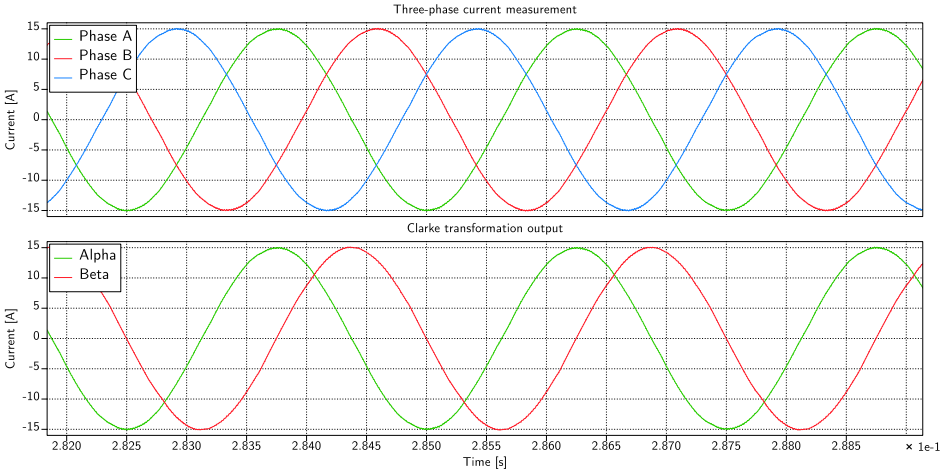


Fig. 3.5 Input and output of the Clarke transformation.

3.2.2 Park transformation

The previously described Clarke transformation is often used in conjunction with a Park transformation [101], [102]. The input of a Park transformation is in the case of motor control an output of a Clarke transformation, where the two components *Alpha* and *Beta* are converted from a stationary reference frame into a rotating reference frame, using *Theta*, in this case, the output of the motor position sensor with offset to obtain the electrical angle. The general equation for Park transformation is [103]

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}, \tag{3.9}$$

where V_d, V_q are the direct and quadrate axis components, θ is the reference of the rotating frame, in case of motor control it is the electrical angle when the rotor flux is aligned with the stator phase A [104] and V_α, V_β are the outputs of the Clarke transformation. Each component of the transformation can be calculated

$$\begin{cases} V_d = \cos\theta \cdot V_\alpha - \sin\theta \cdot V_\beta \\ V_q = -\sin\theta \cdot V_\alpha + \cos\theta \cdot V_\beta \end{cases}. \tag{3.10}$$

The Park transformation enables us to obtain a steady-state DC representation that reflects the currents within an AC three-phase system. This steady-state value can be effectively utilized for controlling the converter. Additionally, conventional control techniques like PI and PID controllers can be applied using this transformed representation for precise control and regulation of the system.

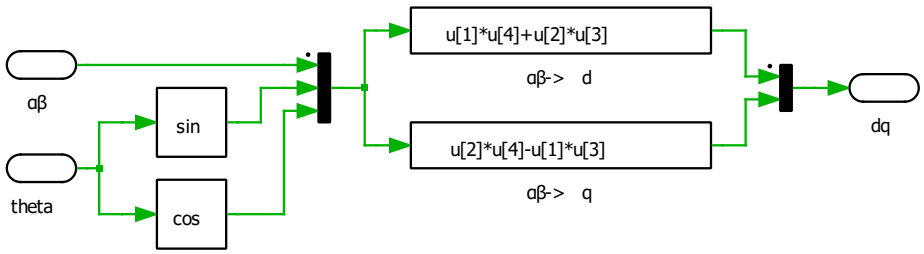


Fig. 3.6 Park transformation implementation in simulation.

The implementation of the Park transformation is similar to the Clarke transformation but involves the use of trigonometric functions applied to the *Theta* input. This addition simplifies the computation of the *d* and *q* functions and reduces the overall number of calculations required. Figure 3.6 shows the internal structure of the Park transformation and in Figure 3.7 the input and output of the transformation are shown.

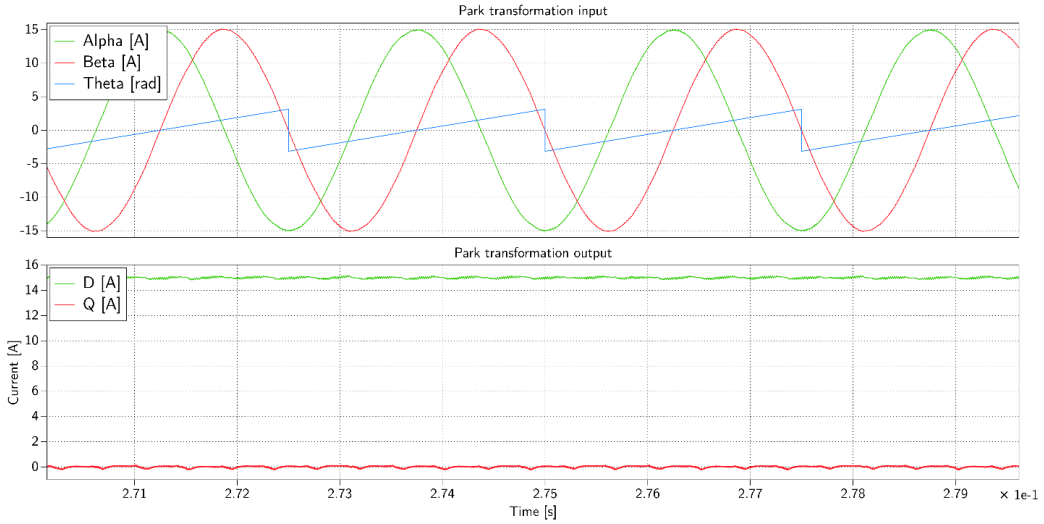


Fig. 3.7 Input and output of the Park transformation.

3.3 Space vector modulation

Space vector pulse width modulation (SVPWM) is a technique for synthesizing a desired reference voltage vector to a three phase PWM pattern at the output of the inverter without the use of a carrier as explained in [105] and [106] and as shown in Figure 3.8. Space vector modulation offers improved DC bus voltage utilization by up to 15.5%, simple implementation in a DSP and improved harmonic performance [107], [108].

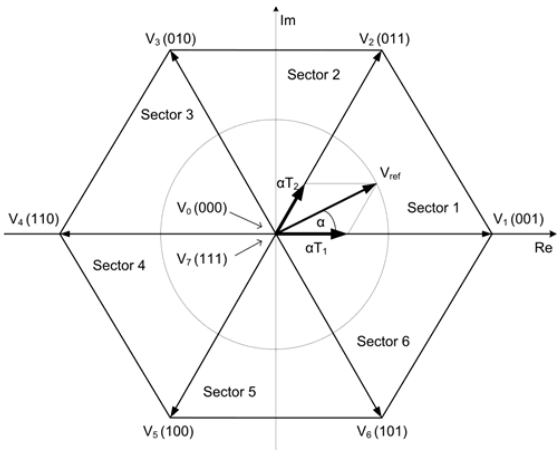


Fig. 3.8 Reference voltage vector in the alpha-beta plane [109].

As field-oriented control is to be used, the space vector modulation is to be implemented, the inputs for the modulation algorithm are the output of an inverse park transformation, the *d* and *q* axis values can be converted to the *gh* coordinate system using the equation from [110]

$$\begin{bmatrix} V_g \\ V_h \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix}, \tag{3.11}$$

where V_d and V_q are the outputs of the PI controllers, θ the angle of rotation as shown in [111]. Figure 3.9 shows the voltage space and switching state for a five-level converter in the *gh* coordinate system, the voltage levels are normalized to the DC-link voltage.

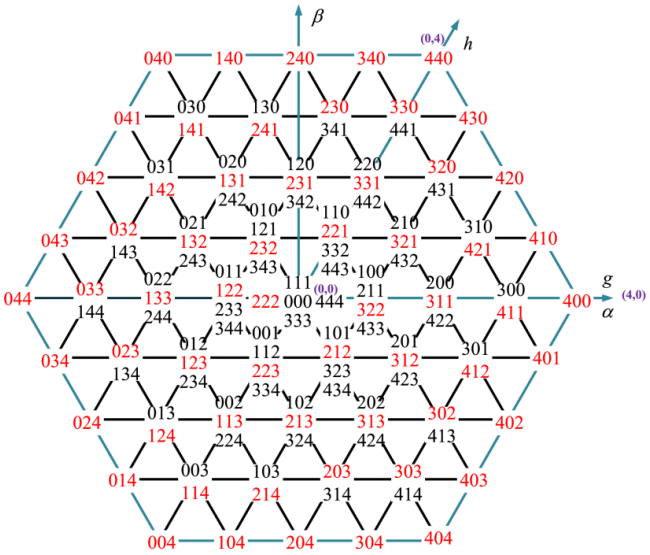


Fig. 3.9 Five level converter voltage space [91].

The closed interval sector for a reference vector $\boldsymbol{V_{ref}}(V_g^*, V_h^*)$ is a triangle consisting of three space points V_1, V_2, V_3

$$\begin{cases} V_1 = (V_{gf} + 1, V_{hf}) \\ V_2 = (V_{gf}, V_{hf} + 1), \\ V_3 = (V_{gf}, V_{hf}) \end{cases} \tag{3.12}$$

where V_{gf} and V_{hf} are the outputs of a floor function of V_g^* and V_h^* respectively. As per the subinterval analysis, there are multiple redundant states for some of the output levels. If a reference vector $\boldsymbol{V_{ref}}(V_g^*, V_h^*)$ is synthesized to one of such levels an active capacitor voltage balancing, and common mode voltage reduction algorithm described in chapter 3.1 is used to determine the final switching state combination, the duty cycle is then calculated to synthesize the reference vector accurately as described in [91].

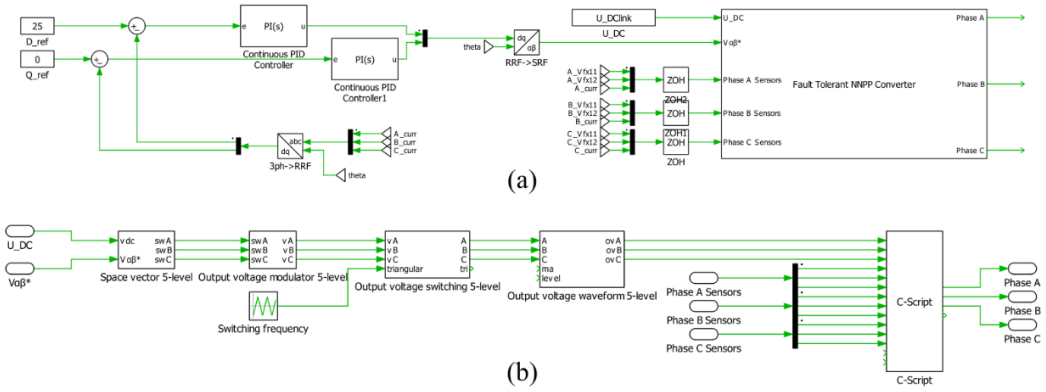


Fig. 3.10 Simulation block schematic (a) control part, (b) modulation part.

The Figure 3.10b shows the block layout of the space vector modulation part of the control algorithm, Figure 3.10a shows the output of the PI controllers for the *d* and *q* are fed into an inverse part transformation block RRF->SRF together with the sensor data, the output of which is then fed into a Fault Tolerant NNPP Converter in which.

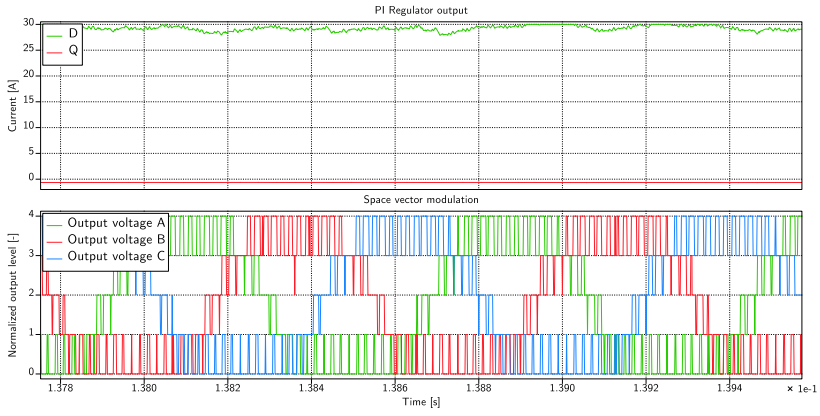


Fig. 3.11 Input and output of the Space Vector Modulation block.

The input data as well as the space vector output is shown in Figure 3.11. The output is then used by the active capacitor balancing block to determine the actual states of the switching devices based on other sensor data.

3.4 Fault detection

In order for the algorithm to be able to have a fault ride-through capability, the fault first needs to be detected, there are many options available such as desaturation detection as described in [112] and [113], which is challenging to implement due to the fast switching properties of the wide bandgap semiconductor switches used in the design. Another option is to use a senseFET technology as shown in [114], where a scaled down current is measured across a shunt resistor usually integrated in the switching device itself, this increases the costs and reduces the selection due to the availability of such devices. The last considered option was the use of a shunt resistor or other form of current measurement of the current carrying path, this method can in some real world applications be less suitable due to the increased losses as described in [115], [116] and [117], but use of hall effect and new current sensors such as TLI4791 from Infineon may help with the loss problem as they offer high accuracy measurement with sufficiently fast overcurrent detection [118], the choice of the current sensor as well as the actual hardware configuration for fault detection is described in chapter 4.3.1.

For the sake of the simulation the fault of the switching device is controlled, an external switch is used to bridge the switching device and act as a short circuit. The algorithm uses the measured current as a form of detection of the state of the switching device and compares it to the desired current through the path in a particular subinterval. In case the two values do not match, the fault is evaluated, and a switch failure mode is determined. Based on that information and the desired output subinterval the control algorithm acts accordingly. This behavior is described in the next section and is the main contribution of this thesis to the topic of nested neutral point piloted converter development as it allows for a smooth fault ride-through operation, be it with minor performance degradation.

3.5 Fault ride-through

Based on the desired subinterval a strategy for the control of the actual switches is determined, the control-flow graph for the strategy is shown in Figure 3.12, the control-flow graph is also inserted as an Appendix B. As per the subinterval and types of fault analysis, only the subinterval faults for which the failure may be destructive are considered. At the time of writing no method without inserting additional devices in the high current path for fault ride-through has been presented.

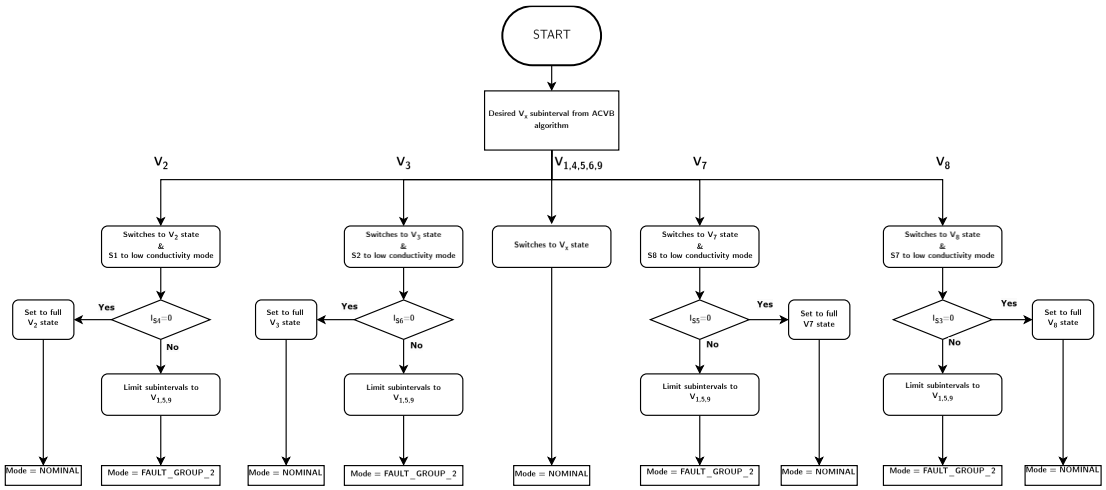


Fig. 3.12 Propose fault ride-through control-flow graph.

The destructive failure of controller may occur when the desired subintervals are $V_{2,3,7,8}$ as in these subintervals a high-current loop may be formed between the capacitors. Such a fault is shown in Figure 3.13, where a switch configuration for a subinterval V_8 is presented. In this subinterval, in case of a failure of the switch S_3 a short circuit is formed through the switches S_7, S_3, the capacitors C_2 and C_{fx2} and the diode in the switch S_4. This current will be extremely high and can reach thousands of amperes [119] due to the low resistance path formed between the two capacitors and the low ESR and ESL of the capacitors. Such high current can almost instantly damage the converter assembly and even cause an electrocution and fire [120].

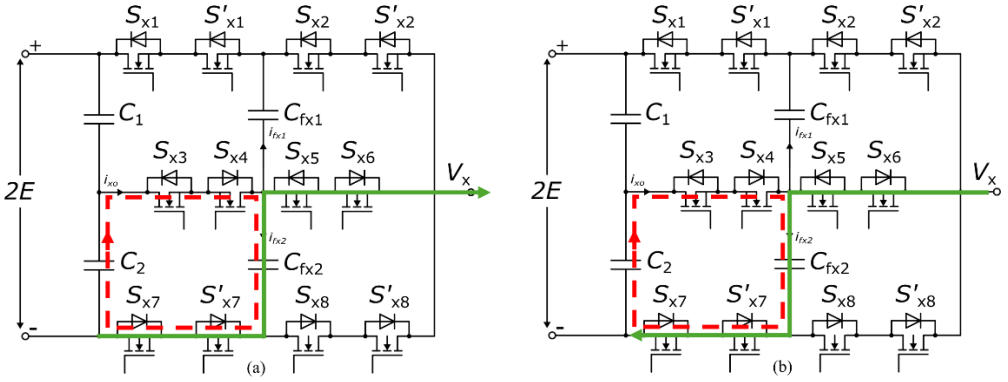


Fig. 3.13 Fault of switch S_3 during V_8 subinterval (a) $i_x > 0$, (b) $i_x < 0$.

To prevent this risk the switching device, in the case of the prototype, where a SiC MOSFET is used an active gate control is implemented. In some instances of the subintervals the switches are operated in a region, where the drain current I_D is a function of the V_{GS} voltage and V_{DS}, which can be considered constant and MOSFET is therefore operated in the active region as shown in Figure 3.14.

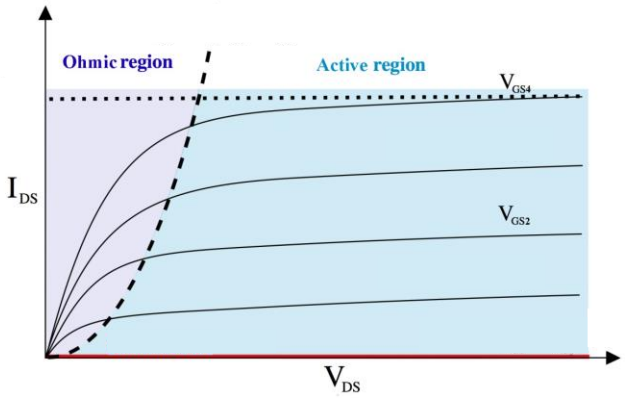


Fig. 3.14 MOSFET Drain current vs. Gate-source voltage dependance [121].

By adjusting the V_{GS} voltage, the drain current I_D can be limited to a known value. This current is then measured by a fast current sensor and based on it either the full V_{GS} is applied, or the converter switches into a "*fault mode*" to prevent damage from occurring.

Such a fault tolerant method has its shortcomings, one of which is the need for a more advanced gate driver to be used as well as the increased number of control signals, these shortcomings are described in more detail in the chapter 4.4.

3.6 Simulation

Simulation of the control algorithm as well as the entire power converter was done in PLECS by Plexim. This software is designed for power electronics simulation [122] and was initially developed as a piece-wise linear electrical circuit toolbox under Simulink [123]. It also includes tools for thermal simulation allowing the estimation of switching and conduction losses [124] as well as code generation for implementation and execution of the algorithms developed in PLECS on real-world targets [125] such as the Texas Instruments C2000 [126], STMicroelectronics STM32 MCUs [127] and the RT Box HiL Platform [128]. The ability to generate code directly from the simulation model will in future testing allow for rapid changes to be made to optimize the algorithm.

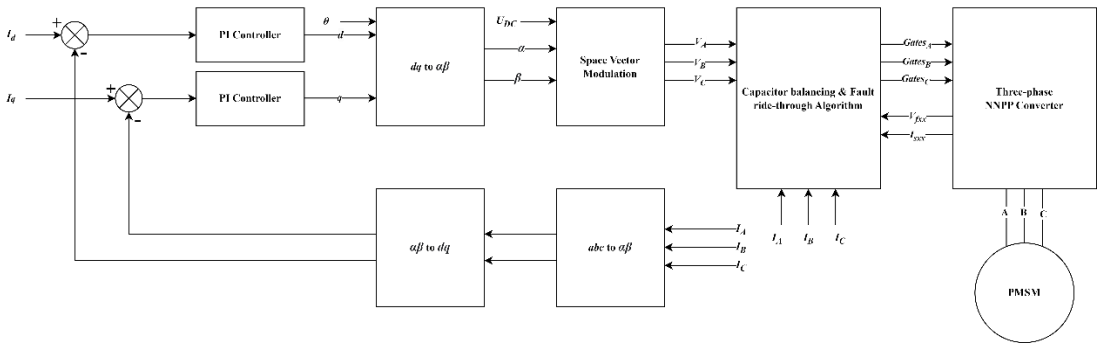


Fig. 3.15 Converter block diagram.

A block diagram of the converter for the evaluation purposes of the proposed algorithm is presented in Figure 3.15. The simulation is carried out under ideal conditions, where disturbances, non-linearities and other external conditions which may influence the actual result in the real world such as gate driver dead-times etc. are not considered as the simulation model would be too complicated for the purpose of evaluating the proof of concept of the developed algorithm and would be beyond the scope of this thesis.

3.6.1 Normal operation

First a simulation of the basic control of the converter is conducted to ensure correct operation under normal conditions, in this simulation the active capacitor voltage balancing algorithm, the space vector modulation as well as the current regulation components are evaluated. The initially requested current changes at time t_{change} to check the stability of the current control loop and resilience to abrupt changes in load conditions. Parameters of the simulation are concluded in Table 3.1.

Table 3.1 Overview of simulation parameters for normal operation

Parameter	Symbol	Value	Unit
Simulation time	t_{sim}	0.5	s
Maximum step size	t_{step}	0.1	µs
Reference frequency	f_{ref}	900	Hz
Switching frequency	f_{sw}	50	kHz
DC bus voltage	U_{DC}	600	V
Load resistance	R_{load}	130	mΩ
Load inductance	L_{load}	0.4	mH
Initial requested current	I_{req1}	10	A
Time of step change	t_{change}	0.25	s
Requested current since t_{change}	I_{req2}	25	A

In figure 3.16 the voltage measurement of the flying capacitors C_{f11} and C_{f12} are shown. Their voltage is balanced, and the algorithm is working as proposed. The deviation from the requested voltage of 150 Volts is only caused by the discharging of the capacitors during the individual subintervals.

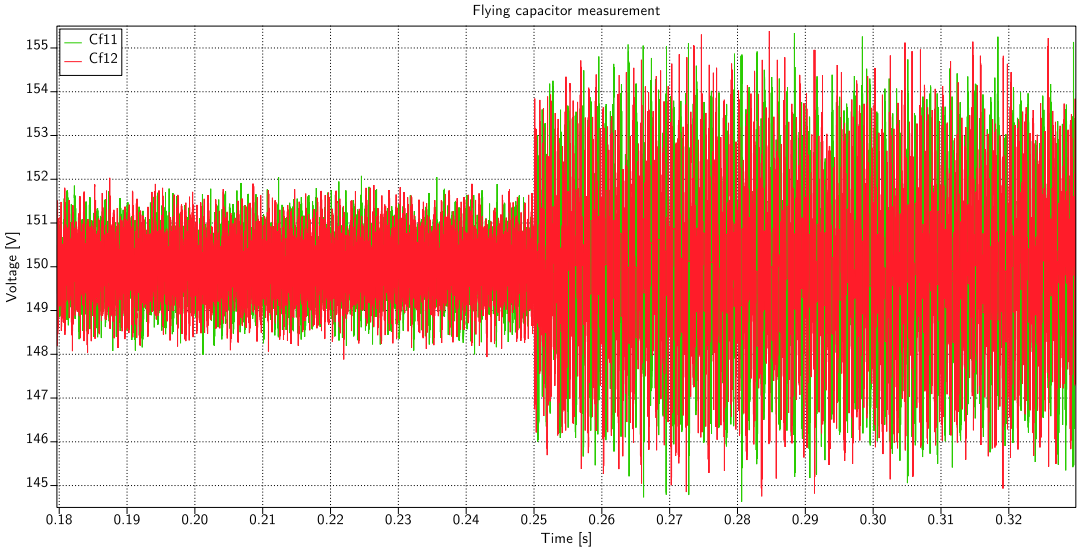


Fig. 3.16 Flying capacitor voltage measurement.

Figure 3.17 shows a detail of the simulation results for the line-to-line voltage measurement of each of the phases and requested current I_{req2}.

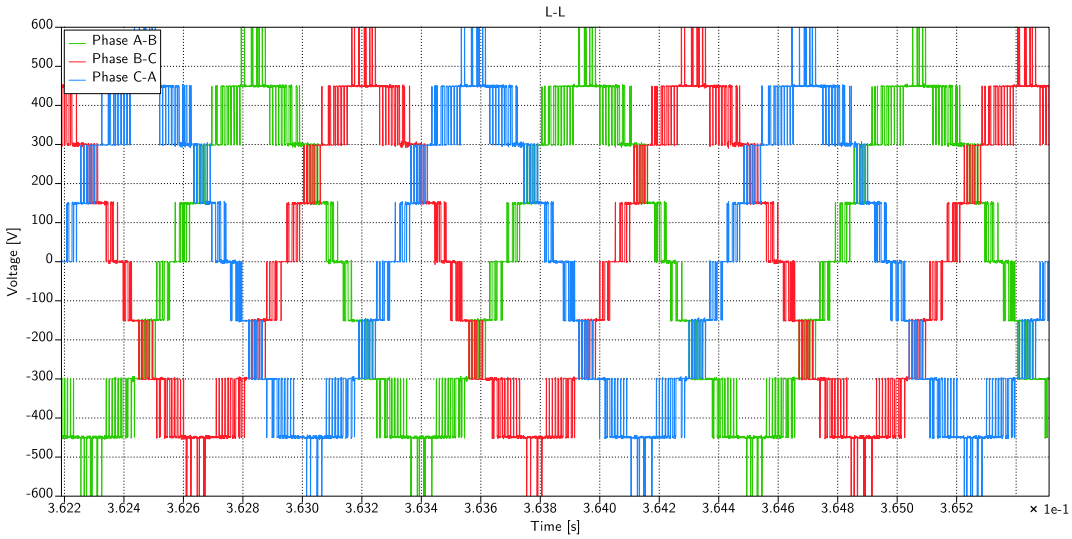


Fig. 3.17 Phase to phase voltage measurement of the converter.

Figure 3.18 shows a detail of the simulation results for the requested current I_{req2}. The line-to-neutral-point voltage measurement of each of the phases is presented.

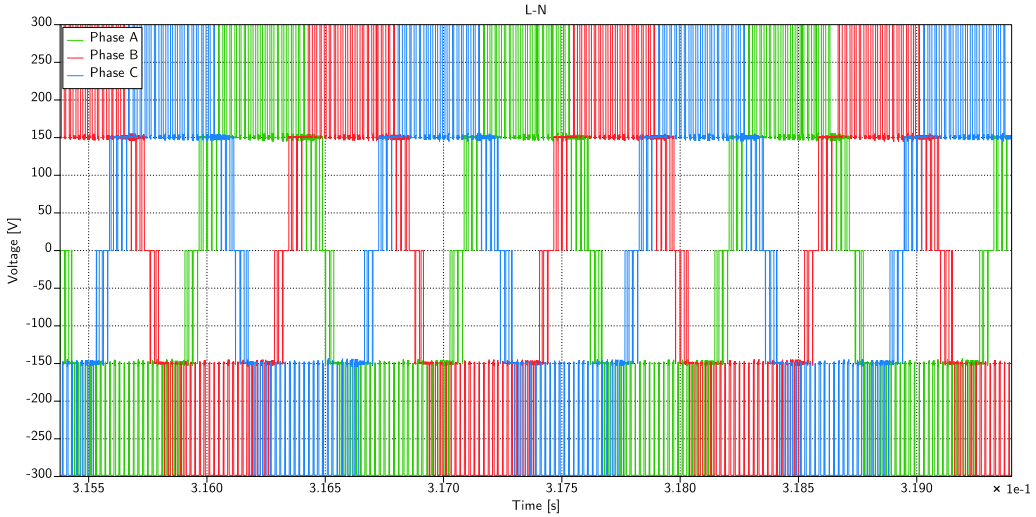


Fig. 3.18 Phase to neutral voltage measurement of the converter.

Figure 3.19 shows the phase current output waveform for the requested current I_{req2} in detail.

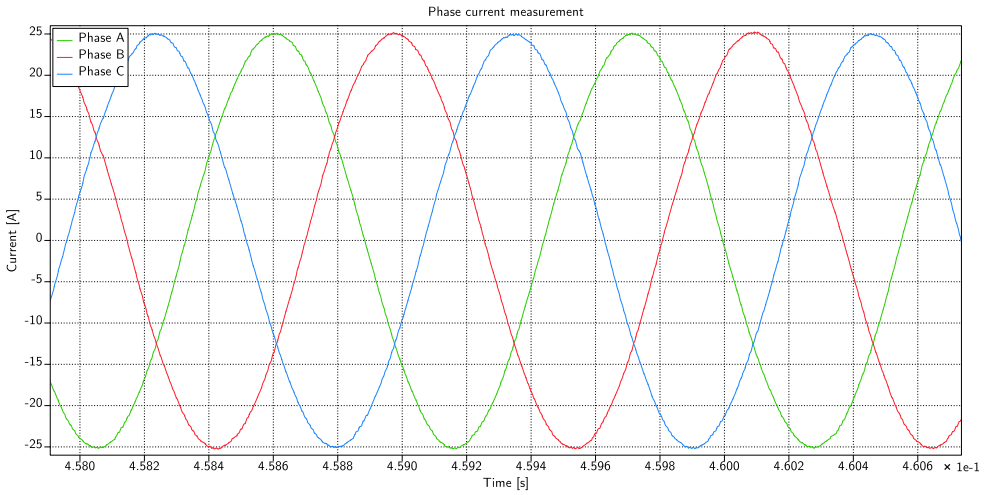


Fig. 3.19 Phase current measurement of the converter.

In Figure 3.20, the response of the converter to the change from I_{req1} to I_{req2} is presented.

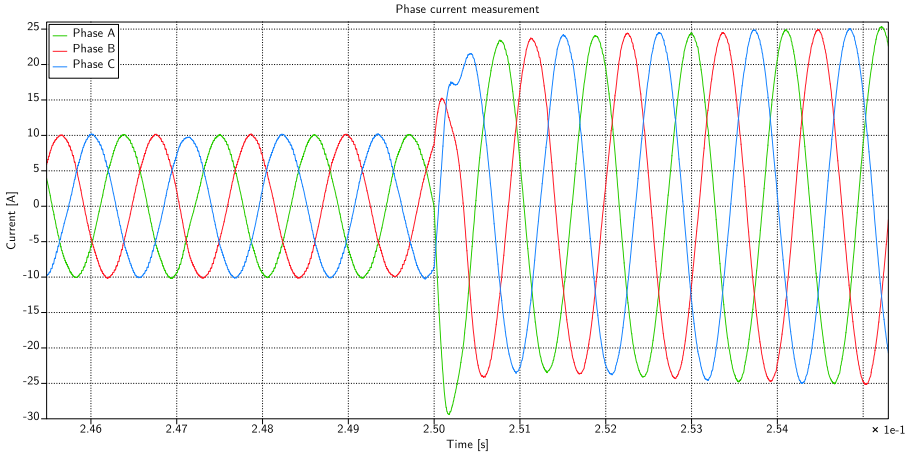


Fig. 3.20 Phase current measurement of the converter during transient.

In conclusion, the simulation successfully validated the converter's control algorithm under nominal and dynamic load conditions. The evaluation encompassed key components such as active capacitor voltage balancing, space vector modulation, and current regulation, with stability and resilience tested through abrupt current request changes at t_{change}.

3.6.2 Fault condition

Secondly the simulation of fault at the MOSFET S_{13} is conducted. According to the proposed fault-tolerant algorithm the fault should be detected during the low conductivity state of the S_{17} as short circuit condition is formed through these switched and capacitors C_1 and C_{f12}. As the utilized simulation software PLECS does not allow dependency of the MOSFET conductivity on the gate-source voltage, but instead uses a simplified behavioral model [129], to overcome this limitation a subsystem to replace the MOSFET part in the converter simulation as shown in Figure 3.21a. Instead of a gate-source voltage input a two-dimensional gate signal is used to switch between the states of the MOSFET, which can be seen in the internal structure presented in Figure 3.21b. The low conductivity mode is established by a simple series resistor to represent the impedance of the MOSFET when low gate-source voltage is applied. Such a simplification is only sufficient for the basic evaluation of the algorithm's functionality, a more accurate representation of the MOSFET behavior should be considered for future work on the simulation of the converter, however for the purposes of this thesis this simplification is not a limitation.

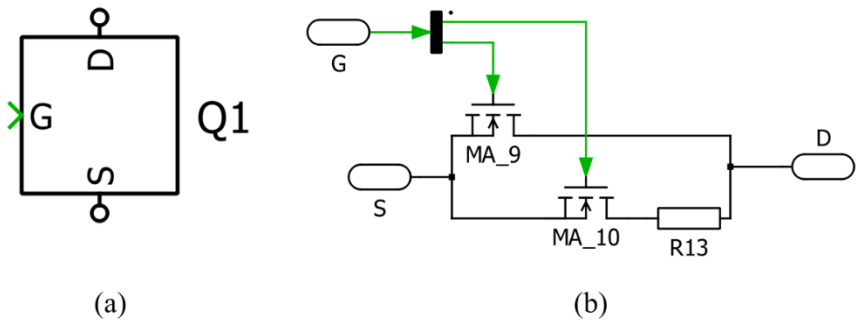


Fig. 3.21 Simplified MOSFET model (a) subsystem, (b) internal structure.

Compared to the simulation of the normal operation, the simulation time for the fault condition was reduced, and a smaller step size was used to gain a more accurate look at the operation of the algorithm. The requested current I_{req} does not change during the fault condition simulation. The fault of the converter occurs at the time t_{fault}.

Table 3.2 Overview of simulation parameters for fault condition

Parameter	Symbol	Value	Unit
Simulation time	t_{sim}	0.05	s
Maximum step size	t_{step}	0.01	µs
Reference frequency	f_{ref}	900	Hz
Switching frequency	f_{sw}	50	kHz
DC bus voltage	U_{DC}	600	V
Load resistance	R_{load}	130	mΩ
Load inductance	L_{load}	0.4	mH
Time of fault occurrence	t_{fault}	0.025	s
Requested current	I_{req}	25	A

To simulate a short circuit fault, a basic ideal switch is used to bridge the MOSFET S_3 at time t_{fault}. The output of an ammeter is then used to compare this measurement with overcurrent limit thresholds described in the chapter 4.3.1, thereby simulating the behavior of the TLI4791 current sensor. A transport delay is incorporated to emulate the delay of the sensor's output. The configuration of the individual blocks is shown in Figure 3.22.

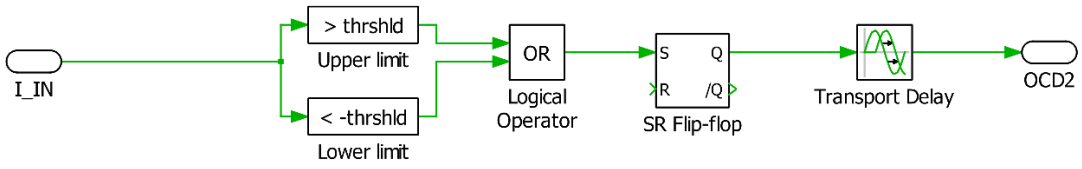


Fig. 3.22 Model of the OCD2 output of the TLI4791 current sensor in simulation.

The simulated OCD2 output is then routed to a C-Script block, where the proposed algorithm is running and based on the desired subinterval and the state of the OCD2

outputs action is taken. In this case at the time of t_{fault} the allowed subintervals are limited to $V_{1,5,9}$ resulting in a three-level modulation. Figure 3.23 presents a detailed view of the simulation results depicting the line-to-line voltage measurements for each phase during the fault transition.

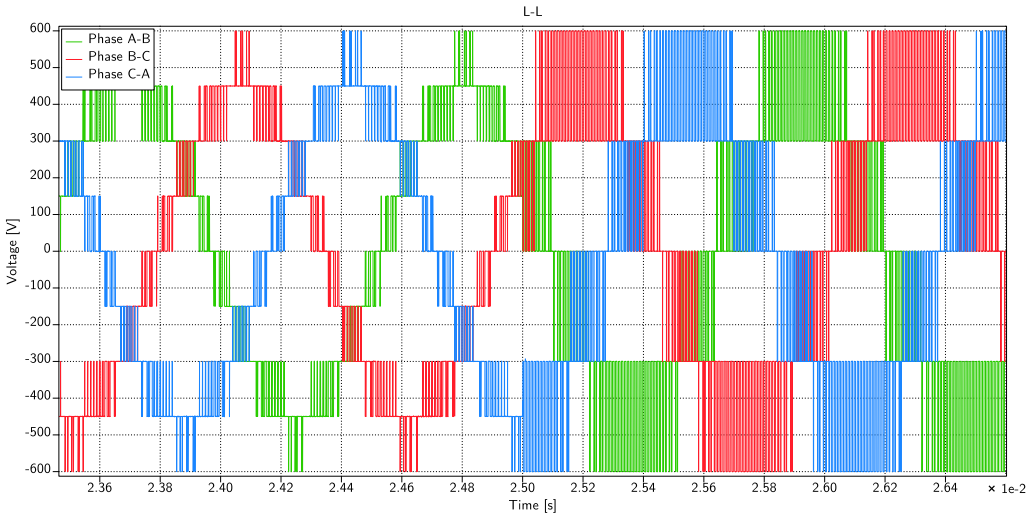


Fig. 3.23 Phase to phase voltage measurement of the converter for fault transition.

In Figure 3.24 the line-to-neutral voltage measurements of the fault transition are presented. The voltage THD in respect to the reference frequency f_{ref} increases from approximately 17.5 % to 39.8 %. High THD can lead to issues related to voltage stability, electromagnetic interference as described in [130], [131].

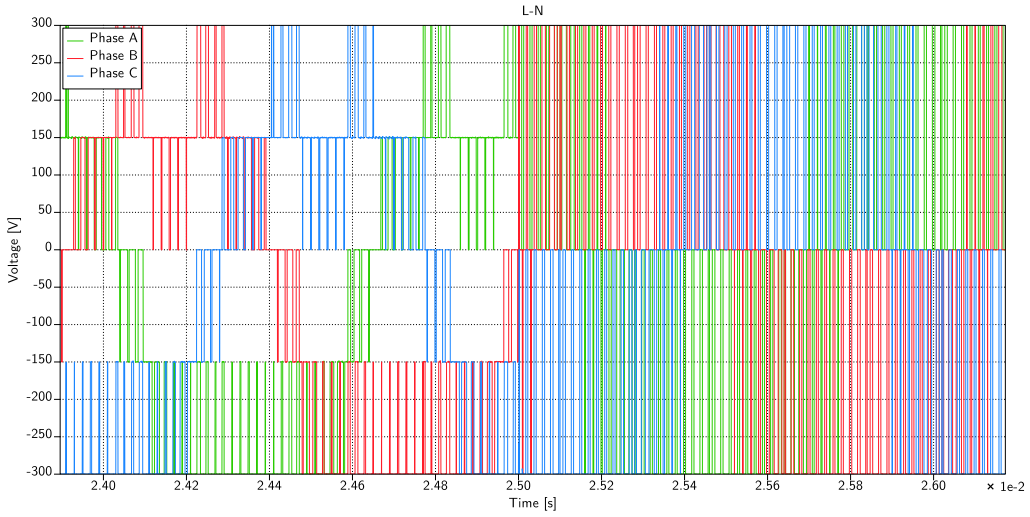


Fig. 3.24 Phase to neutral voltage measurement of the converter for fault transition.

The transition also influences the phase current waveform and reduces the quality of the output. The current THD in respect to the reference frequency f_{ref} increases from

approximately 0.34 % to 0.57 %. The reduction in the output quality can be seen in Figure 3.25.

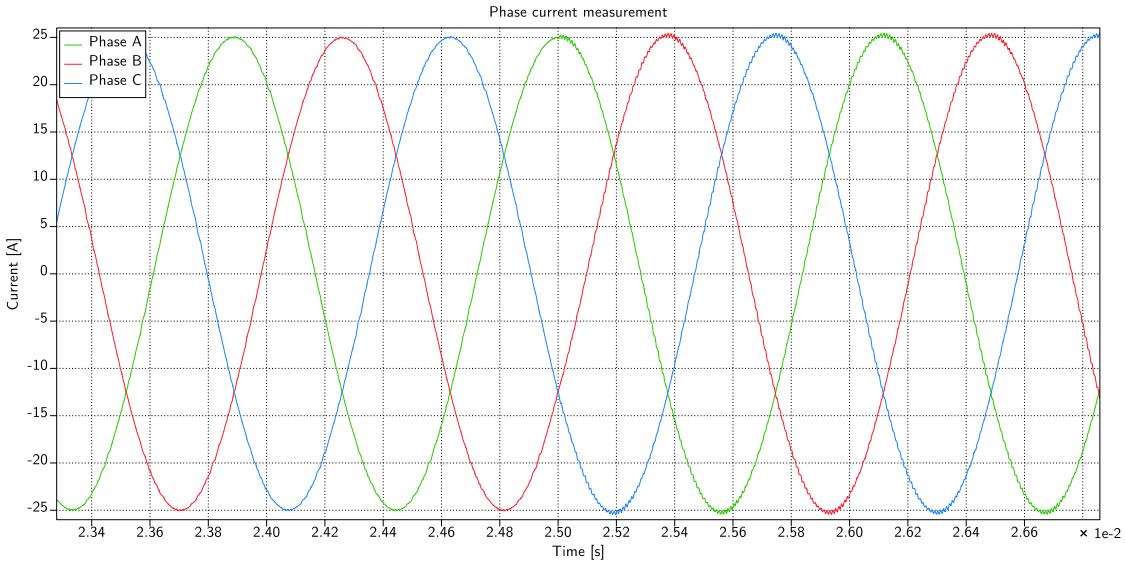


Fig. 3.25 Phase current measurement of the converter for fault transition.

The simulation of a fault of the S_3 in the inner cell group was conducted, as per the description of the proposed algorithm the fault is detected during the low conductivity mode of the S_7 MOSFET, therefore action can be taken before potentially damaging current is allowed to flow. Due to limitations in the simulation software regarding MOSFET behavior, a subsystem was created to replace the MOSFET part in the converter simulation, using a simplified two-dimensional gate signal approach to mimic a real MOSFET gate-source voltage dependance. This simplification, while adequate for evaluating the algorithm's functionality, more accurate representation of MOSFET behavior may be needed for more accurate converter simulation work.

4. CONVERTER PROTOTYPE

The simulation as well as the converter hardware prototype is based on a high-speed three-phase IPMSM TI085-052-070-04B7S-07S04BE2 from Fischer Elektromotoren GmbH shown in Figure 4.1 as this motor is available for testing at the university. Medium voltage (1 kV+) [132], for which the novel high-frequency press-pack (HFPP) switching device is designed can be dangerous and the availability of both the power supply as well as sufficient load are scarce, for the sake of the development and evaluation of the control algorithm a lower power, lower voltage prototype is sufficient.

Fig. 4.1 Fischer Elektromotoren TI085-052-070-04B7S-07S04BE2.

The most important parameters of the chosen motor important for the development of the converter, on which much of the prototype and the simulation are based are shown in Table 4.1.

Table 4.1 Overview of the motor parameters [133]

Parameter	Symbol	Value	Unit
DC bus voltage	U_{DC}	600	V
Resistance per phase	R_{ph}	0,126	Ω
Inductance per phase	L_{ph}	0,393	mH
Number of pole pairs	N_{ppairs}	4	-
BEMF constant	k_e	0,031	$V/rmin^{-1}$
No load current	I_{eff}	16	A_{RMS}
Rated power	P_{nennWk}	15 404	W
Rated speed	n_{nennWk}	13 250	$rmin^{-1}$

Based on this data we can calculate the maximum reference frequency for the maximum rated speed and the number of poles using following equation [134]

$$f_{ref} = \frac{N_{ppairs} \cdot 2 \cdot n_{nennWk}}{120} = \frac{8 \cdot 2 \cdot 13250\ \text{rmin} - 1}{120} \approx 883\ Hz. \quad (4.1)$$

From these parameters we can establish the basic requirements for the design of the converter, these requirements are concluded in Table 4.2.

Table 4.2 Overview of the converter parameters.

Parameter	Symbol	Value	Unit
Number of phases	N_{ph}	3	-
Number of levels	N_{lvl}	5	-
Topology	T	NNPP	-
Rated power	P_{conv}	30 000	W
Rated current	I_{conv}	30	A
DC bus voltage	U_{DC}	600	V
Reference frequency	$f_{refconv}$	900	Hz

Parameters such as the switching frequency, choice of capacitors, switching device as well as measurement devices are explained in the following chapters, due to the inherent complexity of the converter, the costs associated with the development of such converter as well as the limitations of the equipment available at the university facilities, some compromises are made in terms of the converter efficiency, the power rating as well as accuracy of the measurement. These compromises are explained in further detail in each of the following chapters. The final three-phase five level NNPP converter topology is shown in Figure 4.2.

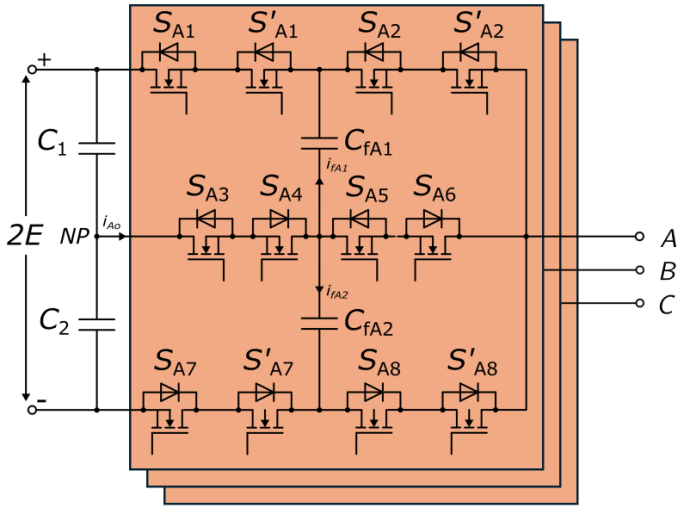


Fig. 4.2 Three-phase five level NNPP Converter.

4.1 Switching device

A choice of switching device is based on the maximum voltage that may occur the switch terminals, the current requirements and the aim is to reduce the heat generated by the switch as well as to have a low gate charge capacitance to lower the switching losses and to allow for higher switching frequencies [135], which are beneficial for achieving a lower THD as shown in [136] and [137]. As previously discussed, Flux-weakening is not implemented, therefore the voltage at the output terminals shall not be higher than back

electromotive force at the maximum rated speed, as can be calculated [138]

$$V_{max} = k_e \cdot n_{nennWk} \cdot \sqrt{2} = 0{,}031 \frac{\mathrm{V}}{\mathrm{rmin}^{-1}} \cdot 13\,250\ \mathrm{rmin}^{-1} \cdot \sqrt{2} \approx 581\ V. \quad (4.2)$$

Therefore, we can consider U_{DC} as the maximum voltage that may occur, without considering the motor cable reflections, which can for a five-level converter based on comparison to a two- and three-level in [4] be neglected. The voltage constraint U_{sw} is the same on all of the used switching devices and can be based on the *2 x 2* NNPP topology explained in chapter 1.2.4 and can be calculated [57]

$$U_{sw} = \frac{U_{DC}}{n \cdot p} = \frac{600\ V}{2 \cdot 2} = 150\ V \quad (4.3)$$

As it is possible for some imperfections during either the design or operation of the converter (such as malfunctioning power supply, electrical noise etc.…) to occur, it is good practice to derate the voltage rating [139], therefore the voltage that the switching device shall withstand is

$$U_{sw\_derated} = U_{sw} \cdot 1{,}3 = 150\ V \cdot 1{,}3 = \ 195\ V. \quad (4.4)$$

The rated current I_{conv} is based on the no load current I_{eff} of the motor as well as the losses that may occur in the system and derating of the converter to ensure smooth control of the motor in the entire range. The requirement for the switch constant current is then calculated

$$I_{sw\_derated} = \mathrm{Iconv} \cdot 1{,}5 = 30\ A \cdot 1{,}5 = \ 45\ A. \quad (4.5)$$

Based on the parameters $U_{sw\_derated}$ and $I_{sw\_derated}$ a list of possible candidates was compiled and can be seen in Table 4.3, only switching devices in the TO-247-4 package were considered to streamline the design as surface mount switches are more difficult to replace in case of an accident during testing.

Table 4.3 Comparison of the switching device candidates

Parameter	**TW015Z65C,S1F**	**STW65N023M9-4**	**MSC035SMA070B4**
Manufacturer	Toshiba	STMicroelectronics	Microchip
Technology	SiC MOSFET	SiC MOSFET	SiC MOSFET
Drain-source voltage	650 V	650 V	**700 V**
Continuous drain current	**100 A**	95 A	77 A
Drain-source resistance	**15 mΩ**	23 mΩ	35 mΩ
Gate charge	128 nC	230 nC	**99 nC**
Price (3/2024)	45,39 €	19,98 €	**14,42 €**
Note	Kelvin terminal	Kelvin terminal	Kelvin terminal
Datasheet	[140]	[141]	[142]

From these three candidates MSC035SMA070B4 was selected. It was chosen based on the price to performance ratio, where compared to the TW015Z65C,S1F it is more than three times cheaper and the continuous drain current is only lower by 23 A, it also has a

much lower gate charge when compared to the STW65N023M9-4, resulting in lower switching losses as show in in [143] and [144].

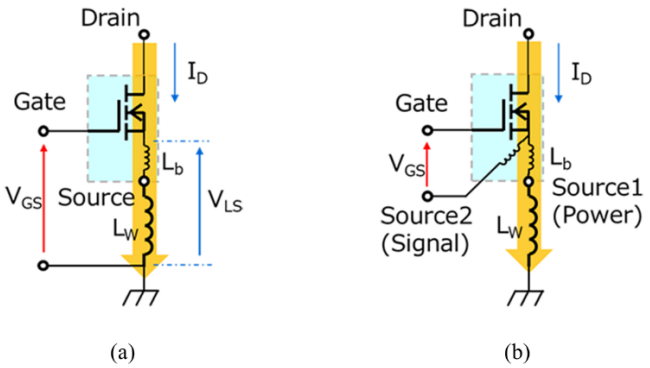


Fig. 4.3 MOSFET Packages (a) 3 pin – no kelvin connection, (b) 4 pin – kelvin connection [145].

The chosen MOSFET also has a kelvin connection, which allows for the V_{GS} to be applied directly to the substrate, without being affected by the inductance and resistance of the bond wire of the source terminal [146] resulting in a smaller gate-drive loop as show in Figure 4.3b in comparison to a three terminal version in Figure 4.3a, this allows for an increase in the switching speed [147].

Manufacturer Microchip also released a PLECS model of the MSC035SMA070B4 SiC MOSFET [148], this allows for much more accurate estimation of the turn-on and turn-off losses based on lookup table data and equation shown in Figure 4.4.

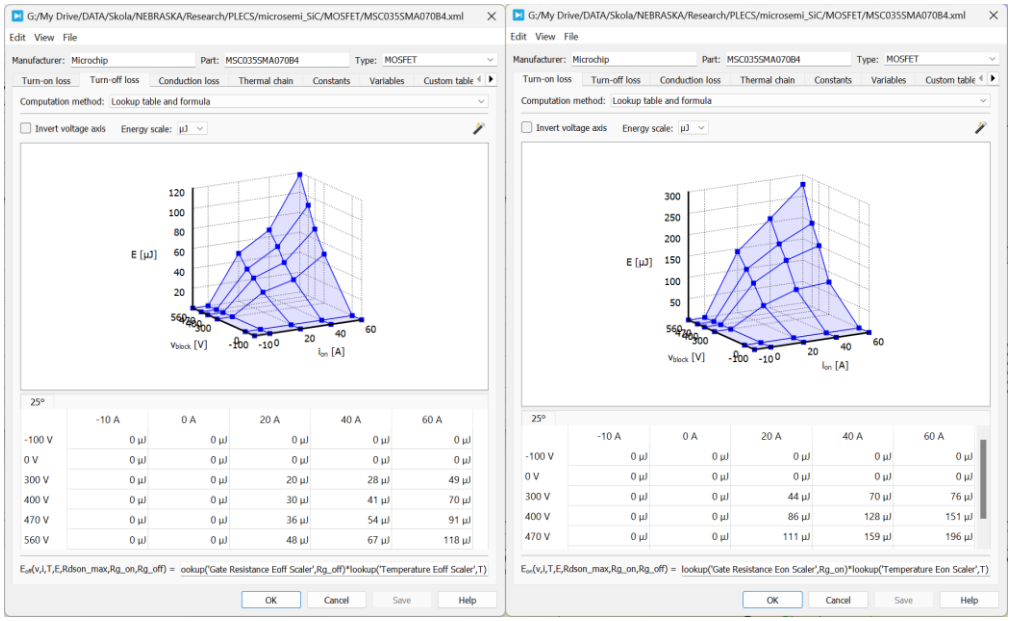


Fig. 4.4 Turn-off/on loss lookup table of the MSC035SMA070B4 model.

Based on these the switching loss of the entire converter at the switching frequency of 50

kHz was estimated to be 13 Watts. Using higher switching frequency would lead to higher switching losses as well as the need for a faster computing unit and higher bandwidth for the voltage and current sensors.

4.2 Capacitors

The purpose of a DC-link capacitor is to allow for high frequency components of the switching process to have a low impedance path to mitigate the effect of parasitic inductances caused by wiring [149]. As the converter prototype is not designed to operate in extreme environments and continuous operation as well as high efficiency operation are not required, the choice of both the DC-link and flying capacitors is mostly based on the size and availability, parameters such as capacitance drift are not considered. One of the most important parameters when choosing capacitors is their voltage rating, due to the nested neutral topology the voltage of the capacitors in the circuit can be calculated using the following equation [57]

$$U_{cap} = \frac{i \cdot U_{DC}}{n \cdot p} \tag{4.6}$$

where U_{DC} is the input voltage of the converter, n and p the configuration of the converter as described in chapter 1.2.4, and i the index of the cell in the circuit. Therefore, in case of the DC-link capacitors the voltage U_{DCcap} is calculated

$$U_{DCcap} = \frac{i \cdot V_{DC}}{n \cdot p} = \frac{2 \cdot 600\,V}{2 \cdot 2} = 300\,V. \tag{4.7}$$

To achieve close to datasheet values an aggressive derating of the capacitor is applied, therefore the actual required rating of the DC-link capacitor can be calculated

$$U_{DCcap\_derated} = U_{DCcap} \cdot 1{,}5 = 300\,V \cdot 1{,}5 = 450\,V. \tag{4.8}$$

Such high derating was chosen to prevent accidents in case the capacitor voltage balancing algorithm does not perform as intended and the voltages on all the capacitors are not in their intended operating window.

Fig. 4.5 Chosen DC-link capacitor package [150].

Low ESR is an important parameter for capacitor selection as it together with the ripple current creates self-heating of the capacitor [151], which may be a limiting factor when selecting a capacitor. For a traditional two level three phase inverter topology with a space vector modulation PWM strategy the ripple current can by calculated analytically [152], however for the selected inverter topology and control strategy such a calculation would be complicated. Therefore, an estimate was taken from the simulation of the converter. A C4AU capacitor series from Kemet was selected as it is designed for use in DC-link applications [150], specifically the C4AULBW5700M3PK capacitor show in Figure 4.5 was used as it offers a voltage rating of 500 VDC, while maintaining a compact package with a four lead output to reduce the ESR and ESL. Based on the capacitor and converter parameters self-heating can then be calculated [153]

$$\Delta T = (I_{RMS})^2 \cdot ESR \cdot R_{TH} = (8.9\ A)^2 \cdot 2.1 \cdot 10^{-3}\ \Omega \cdot 14 \frac{°C}{W} \approx 2.3\ °C, \tag{4.9}$$

where I_{RMS} is the RMS current through the capacitor from simulation, R_{TH} is the thermal resistance and ESR is the equivalent series resistance of the chosen capacitor. As can be seen the temperature of the capacitor only increases by approximately 2.3 °C, therefore the selected capacitor is suitable for the converter. A similar approach was taken for the flying capacitor voltage $V_{Flyingcap}$ calculation, where the voltage is lower due to the position of the flying capacitors in the circuit

$$U_{Flyingcap} = \frac{i \cdot V_{DC}}{n \cdot p} = \frac{1 \cdot 600\ V}{2 \cdot 2} = 150\ V. \tag{4.10}$$

When derating is applied

$$U_{Flyingcap\_derated} = U_{Flyingcap} \cdot 1{,}5 = 150\ V \cdot 1{,}5 = \ 225\ V. \tag{4.11}$$

An R71H capacitor series from KEMET was selected, specifically the 71XR5150H0 due to the small package size, sufficient voltage rating, availability as well as high ripple current rating as can be seen in the parameters listed in [154], the selected capacitor is show in Figure 4.6.

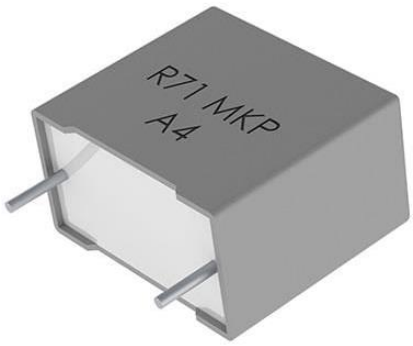


Fig. 4.6 Chosen flying capacitor package [154].

Based on the capacitor parameters and the circuit simulation the self-heating can be calculated [153]

$$\Delta T = (I_{RMS})^2 \cdot ESR \cdot R_{TH} = (7.1\ A)^2 \cdot 7 \cdot 10^{-3}\ \Omega \cdot 23 \frac{°C}{W} \approx 8.1\ °C, \quad (4.12)$$

where I_{RMS} is the RMS current through the capacitor from simulation, R_{TH} is the thermal resistance and ESR is the equivalent series resistance of the chosen capacitor. The flying capacitor only heats up approximately 8.1 °C over the ambient temperature, this will however be lower in real application due to the heat dissipation into the printed circuit board copper.

4.3 Measurement

For the algorithm to function properly several variables and signals on the converter need to be measured, due to the nature of working with dangerous voltages as well as the different floating potentials these measurements need to be sufficiently isolated. As the prototype is to be used in a controlled environments with trained personnel taking necessary safety precautions a basic insulation rating to withstand the full input voltage of 600 Volts is adequate [155]. The use of high switching frequency also limits the choice of sensors to be used as transition times, ringing and phase error need to be taken into account when choosing a measurement method [156], [157]. To reduce noise coupling from the high-power switching events and ground impedance the use of differential signaling, or digital communication is also preferred over single-ended analog signals [158], [159].

4.3.1 Current

Measuring the phase current in the circuit is crucial for the correct operation of the converter as it is used by the control algorithm as well as by the PI regulators in the process of selection of the correct subinterval state and to ensure accurate control of the motor torque and speed [160]. As the switching frequency of 50 kHz is quite high compared to traditional 10 – 20 kHz used by Si IGBT based motor controllers [161], other things apart from measurement range and accuracy need to be considered, such as the current sensor bandwidth, high dV/dt immunity as well as the phase-shift over frequency. Based on these requirements a current transducer LESR 15-NP from the manufacturer LEM was selected. Table 4.4 concludes the main parameters of the sensor.

Table 4.4 LESR 15-NP Parameters [162].

Parameter	Symbol	Value	Unit
Measuring range	I_{PM}	± 51	A
Sensitivity error	ε_s	± 0.2	%
Total error	ε_{tot}	0.7	% of I_{PM}
Frequency bandwidth (± 3dB)	BW	300	kHz

The sensor has a single-ended analog voltage output and due to the location of the sensor on the converter routing the signal through the high-power switching area would result in noise coupling and would potentially greatly reduce the accuracy of the measurement and may even result in an unusable reading [163], [164]. To maintain the signal integrity of the current measurement, the single-ended output is converted to a differential output, which greatly reduces the sensitivity of the signal to induced or coupled noise [165]. The complete schematic for the phase current measurement is shown in Figure 4.7.

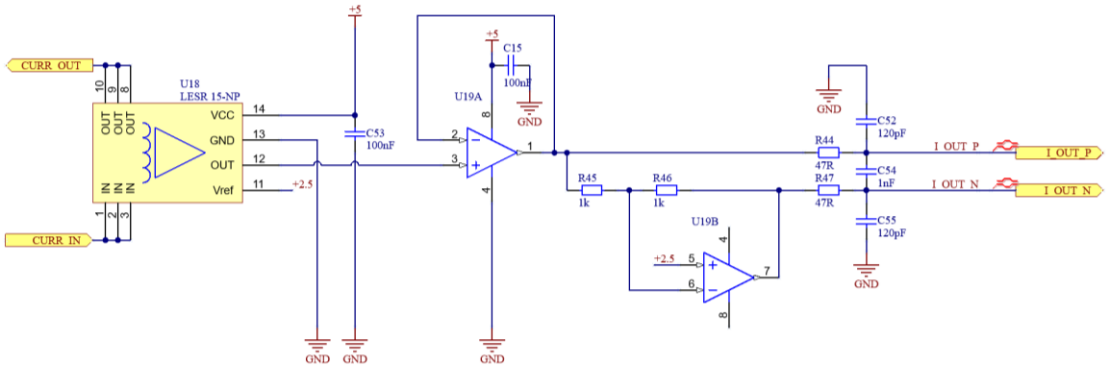


Fig. 4.7 Phase current measurement schematic.

Current also needs to be measured for each of the transistors, this measurement is used by the fault detection system, and it therefore needs to be fast, also due to the number of transistors used it needs to be small enough to fit on the converter without needing to enlarge the commutation loop. For this reason, an SMD current sensor TLI4791 from Infineon was selected. The small PG-TISON-8 package shown in Figure 4.8 allows for placement of the sensor close to the actual transistors, ensuring that the commutation loop stays minimal.

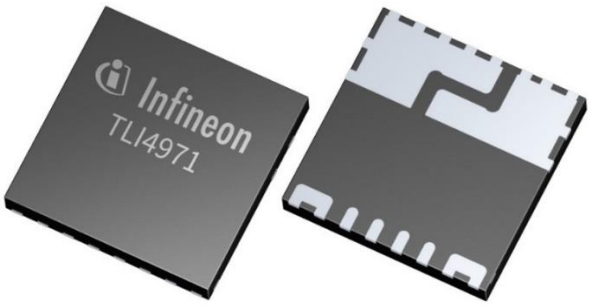


Fig. 4.8 TLI4791 Current sensor package.

The sensor also features a differential output, galvanic isolation up to 1150 V and a fast over-current detection output [166]. The over-current output threshold is user programmable and is set to threshold level 1, where the output is trigged at half of the full-scale current, which in the case of the selected variant TLI4971-A025T5-E0001 is 12.5 Amps. The typical response time of the detection is 0.7 microseconds, which is faster than the MSC035SMA070B4 transistor's short circuit current withstand time of 3

microseconds after which damage may occur.

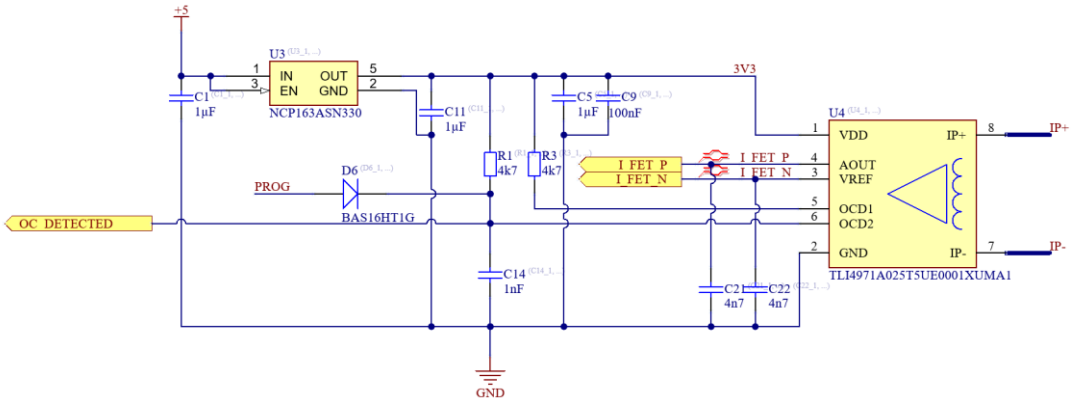


Fig. 4.9 MOSFET Current measurement schematic.

Complete schematic for the transistor over-current protection and measurement is shown in Figure 4.9. The differential outputs *I_FET_P and I_FET_N* are routed to the controller output connector, where based on the configuration of the DSP they are read. An OCD2 output is used as the threshold level 1 allows for the lowest current detection value. The PROG net is used to program the sensor and set the output mode to differential as well as configure the over-current detection.

4.3.2 Voltage

For the active capacitor voltage balancing algorithm to function, the voltages of the DC-link as well as the flying capacitors must be measured, the DC bus voltage is also measured and is partially used to determine the output voltage state. The voltage measurement has similar requirements to the current measurement in regard to the bandwidth, isolation as well as high dV/dt immunity.

A voltage divider made up of a number of lower voltage rated resistors in series is used to distribute the total voltage across them to reduce the necessary working voltage of each of the resistors [167] is used as an input into an isolated single-ended input, differential output amplifier AMC1311 from Texas Instruments, whose maximum input voltage is 2 V. This amplifier is specifically designed for high-impedance voltage measurement as to be optimized for use with high-impedance voltage divider circuits, the amplifier also features a high output bandwidth of 220 kHz [168] , which is sufficient for the proposed algorithm described in the previous chapters.

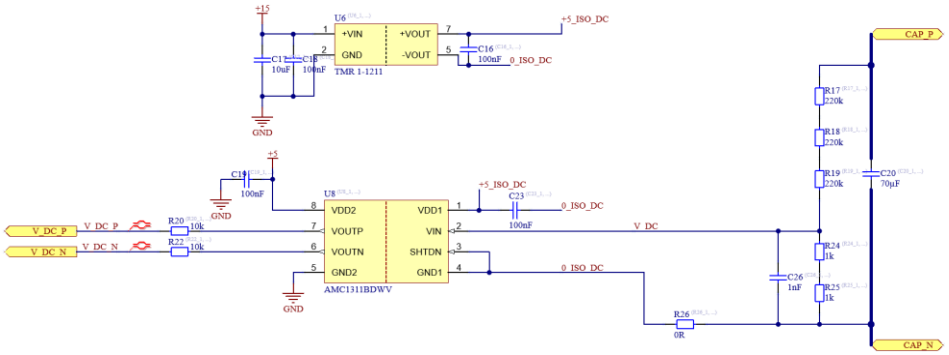


Fig. 4.10 DC-link capacitor voltage measurement schematic.

Figure 4.10 shows the complete schematic of the voltage measurement of the DC-link capacitor, where R_{17}, R_{18} and R_{19}, together with R_{24} and R_{25} form a voltage divider whose gain G_{div} can be calculated

$$G_{div} = \frac{R_{24} + R_{25}}{(R_{24} + R_{25}) + (R_{17} + R_{18} + R_{19})} = \frac{2000\ \Omega}{2000\ \Omega + 660\ 000\ \Omega} = 3.021 \cdot 10^{-3}. \tag{4.13}$$

As the maximum input voltage U_{maxamp} of the AMC1311 amplifier is 2 V, we can calculate the maximum voltage $U_{maxmeas}$ that can be measured by the circuit

$$U_{maxmeas} = \frac{U_{maxamp}}{G_{div}} = \frac{2\ V}{3.021 \cdot 10^{-3}} = 662\ V. \tag{4.14}$$

The maximum voltage that can be measured is higher than the maximum DC bus voltage, such a voltage divider configuration was chosen to have the ability to use the identical circuit in all voltage measurement points in the converter. By adjusting the voltage divider ratio, a more accurate measurement could be achieved on for example the flying capacitor terminals, where the maximum voltage that should occur during normal operation is around 150 V, but for the prototype functionality and demonstration the measurement is sufficient, and it also reduces the costs associated with a more complex bill of materials and it also simplifies the assembly process. Additionally, an isolated regulated DC-DC converter TMR 1-1211 from Traco Power [169] is used to power the high-voltage side of the amplifier.

4.4 Active gate driver

MOSFET is a non-linear electrical component, whose drain current is a function of the drain-source voltage, and the gate-source voltage. The drain-source voltage can be considered static due to the minimum voltage to occur at the switch being the flying capacitor voltage of 150 volts resulting in drain saturation condition. The MSC035SMA070B4 MOSFET is operated in the saturation region, where the drain-

source current can be controlled by applying precise voltage to the gate terminal [170] and [171]. This property is exploited by the control algorithm, where first a low gate voltage is applied for a brief period to lower the short circuit current and to determine the fault state of the converter after which if no fault is present, the full gate voltage is applied to lower the conduction losses. Such control is achieved by use of active gate drivers [172], which can be classified into several categories shown in Figure 4.11.

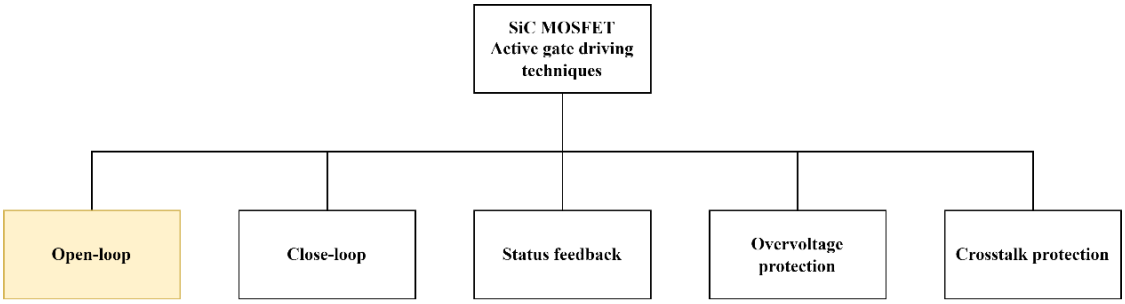


Fig. 4.11 Active gate driving methods overview [173].

An open-loop gate driver is developed as a part of this thesis, which is sufficient for the use in an experimental environment, where operational conditions, such as load, voltage and temperature are controlled, however it may not be sufficient in a real-world application as these parameters may vary. For such applications closed-loop active drivers such as the circuits developed in [174] and [175] are more sufficient as they generally employ drain-source voltage measurement signal as a part of the switching process, resulting in reduced sensitivity to external disturbances [176]. These circuits are generally more complicated than open-loop circuits as they require additional measurement circuitry and feedback logic.

4.4.1 Requirements

The active gate driver is required to switch between three output voltage levels to achieve three conductivity states of the MOSFET required by the fault ride-through capable algorithm. Additionally, to ensure safety during the operation a “ready” signal is used to disable the gate driver and prevent accidental turn-on of the MOSFET.

The MOSFET driving states are described in the following list:

- **OFF**

Where the MOSFET is in no conductivity state, therefore no significant drain current is flowing, and the gate-source voltage is lower than the gate-source threshold voltage of the specific MOSFET. In high-speed and SiC MOSFET applications it is beneficial to use a negative gate-source voltage bias as these devices tend to have low gate-source threshold voltage, which may lead to false turn-on of the device if noise is present in the

circuit [177], [178].

- **LOW CONDUCTIVITY**

To achieve the fault ride-through capability of the converter an additional conductivity state is required to be implemented by the active gate driver. The conductivity in this state is to be high enough to trigger the over current protection output OCD2 on the TLI4791, but low enough to not cause damage to the converter itself. A similar approach as in [179] is to be used, where an adjustable LDO voltage regulator supplies the gate-source voltage for the low conductivity mode.

- **ON**

In the ON state the MOSFET is in or close to full conductivity of the channel and the resistance of the device is close to the drain-source on resistance parameter of the used MOSFET. As SiC MOSFET was selected, the gate-source voltage needs to be higher than if a traditional Si MOSFET was used [180].

The gate driver should also on the isolated side output the state of the voltage of the adjustable voltage regulator as well as the overcurrent output of the TLI4791 current sensor for use as an input for the fault ride-through algorithm. The gate driver should also be modular to allow for simple reconfiguration of the circuit and in future testing also the possibility to be replaced by a more advanced closed-loop gate driver. By employing a modular design, the design of the main converter power board is simplified as it is not dependent on the design of the gate driver.

4.4.2 Implementation

An active gate driver is to be designed based on the requirements specified in the previous chapter. Based on the parameters of the selected MOSFET described in chapter 4.1, the OFF and ON state voltages are selected. To achieve the required isolation and the necessary output voltages an isolated DC/DC Converter MGJ1D151505MPC from Murata Power Solutions was chosen. This converter is specifically designed for driving SiC MOSFETs as it has dual output voltages of +15 V and -5 V [181]. The high Common Mode Transient Immunity (CMTI) of the DC/DC converter also allows for high switching frequencies [182], [183]. The DC/DC converter is shown in Figure 4.12, thanks to the SMD packaging and small dimensions it can be mounted on one side of the converter with the other being used for the driving circuitry and voltage regulation.

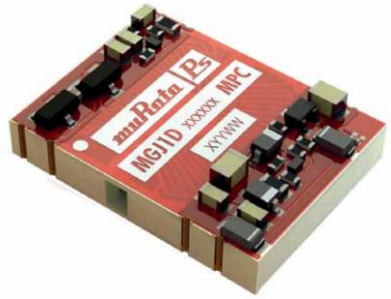


Fig. 4.12 Isolated DC/DC Converter MGJ1D151505MPC [181].

To calculate the voltage of the adjustable voltage regulator for the low conductivity mode, first the overcurrent trigger point of the OCD2 output of the TLI4791 current sensor needs to be calculated, the threshold level is selectable from 8 options, to minimize the current flow in case of failure the lowest level was selected, the current $I_{TRIGGER}$ at which the protection is triggered can then be calculated

$$I_{TRIGGER} = I_{THR2.1} \cdot I_{FSR}, \tag{4.15}$$

where $I_{THR2.1}$ is the threshold level 1 of the OCD2 output and I_{FSR} the full scale current output, based on the selected model of the current sensor and its programming, in this case the TLI4971-A025T5-E0001, which features ±25A full scale range [184]. The current $I_{TRIGGER}$ then is

$$I_{TRIGGER} = I_{THR2.1} \cdot I_{FSR} = 0.5 \cdot 25\ A = 12.5\ A. \tag{4.16}$$

Therefore, the current flow during the low conductivity mode should be slightly higher than 12.5 A to ensure correct trigger under all conditions. Based on this, the gate-source voltage can be estimated, for this a model of the MSC035SMA070 was used in a MPLAB Mindi Analog simulator, a SIMetrix simulation environment, this simulator allows for the use of Microchip proprietary component models [185]. The initial voltage for the low conductivity mode was estimated based on the MOSFET datasheet values and tuned for the drain-source current to be approximately 15 A. The schematic of circuit used for the simulation is shown in Figure 4.13.

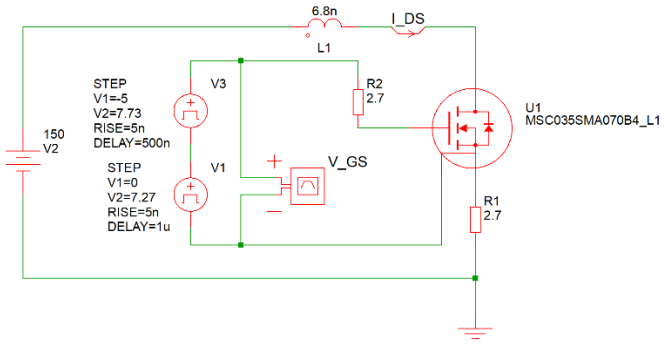


Fig. 4.13 SIMetrix simulation model of the MSC035SMA070 MOSFET.

Where V_2 is the drain-source voltage source worst case scenario voltage for the trigger

current as the channel may not be fully saturated. Waveform generators V_1, V_3 and resistor R_2 generate the two-step gate-source voltage waveform to transition the MOSFET U_1 through all conduction states with rough estimate of the real-world circuit. L_1 is an estimate of the PCB inductance and R_1 a low resistance of a near short-circuit fault.

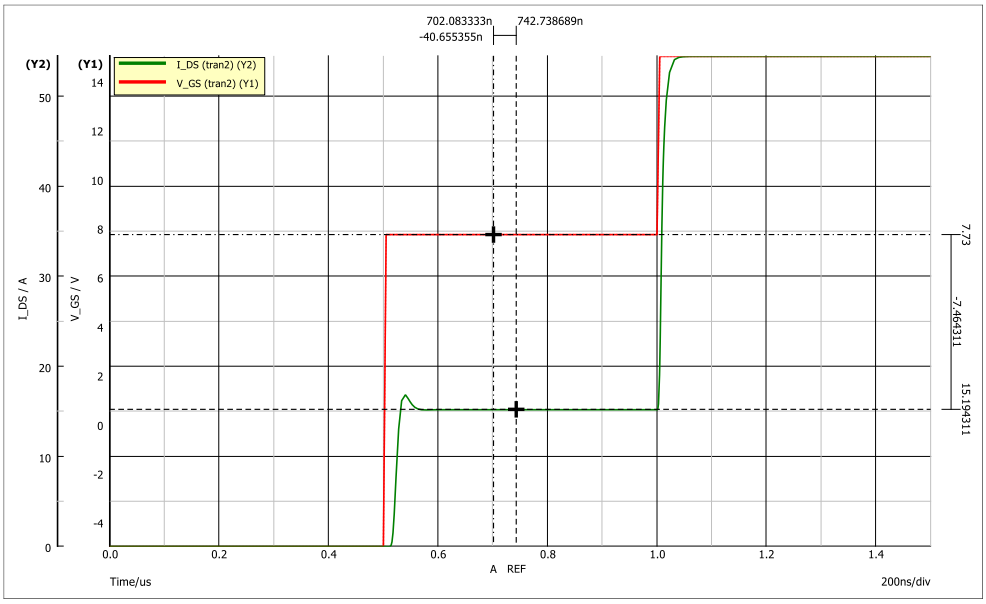


Fig. 4.14 Output of the SIMetrix simulation of the MSC035SMA070 MOSFET.

In Figure 4.14 the result of the simulation is shown, the green curve represents the drain-source current I_{DS} as can be seen the current reaches approximately 15 Amperes in the simulation time between 0.5 µs and 1 µs, where the gate-source voltage of 7.73 Volts is applied. As many factors such as the junction temperature or manufacturing differences between each of the MOSFETs were not taken into account and will influence the drain-source current, the gate-source voltage shall be adjustable.

To achieve this an adjustable LDO regulator TLV709A01DBVR from Texas Instruments was selected as it has a high enough input voltage range of 30 volts and is available in a small SOT-23-5 package [186]. The feedback resistor network was calculated to output approximately 6.7 Volts and an additional 10 turn potentiometer was then used to achieve an output voltage range of 6.7 to 8.2 Volts. This voltage is to be tuned based on the circuit parameters once the converter is assembled.

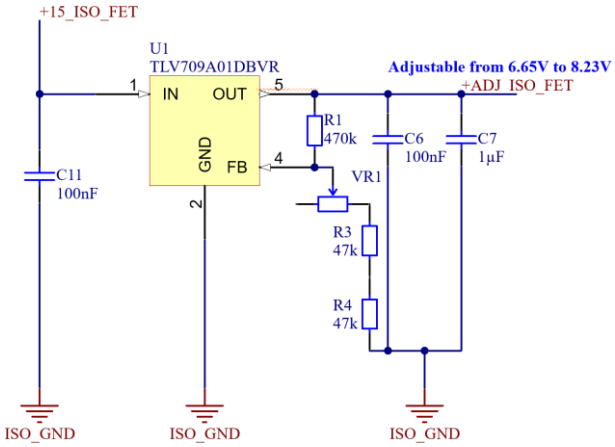


Fig. 4.15 Low conductivity mode power supply schematic.

The final schematic of the adjustable gate-source voltage regulator can be seen in Figure 4.15. Capacitors C_{11}, C_6 and C_7 were added for stability of the regulator and output voltage waveform. Additionally, a comparator is used to check that the voltage is in the correct window, the output of the comparator is then together with the TLI 4791 OCD2 overcurrent output signal routed through an ADuM342 Quad digital isolator to the control signal side, the signal can then be used to check if all gate drivers are operating as expected. From the control side two signals for the control of the MOSFET are routed through the same isolator. The entire active gate driver schematic can be seen in appendix C.

4.5 Prototype design

Based on the converter parameters and proposed algorithm requirements, a hardware prototype is to be designed to allow for experimental testing and validation. A modular design is to be utilized to enable expansion of the converter, increasing the number of output levels, phases, and allowing for swapping of the active gate driver modules for different versions based on the experiment to be conducted. This modular design will enhance versatility and scalability, supporting various experiments and validation scenarios effectively. As described in the simulation chapter, PLECS allows for code generation for multiple control platforms. Therefore, the main converter board is to have a universal control interface, allowing for simple connection to these platforms for added experimental flexibility. To achieve this Altium Designer 24 software package was used as is allows for advanced PCB design features such as hierarchical schematic design as well as 3D modelling and visualization of the PCB [187].

4.5.1 Schematic

A system of hierarchically interconnected functional schematic blocks is used to simplify the design of the main converter board. The top-level schematic sheet of the main system is shown in Figure 4.16. Each of the green blocks is then made up of other blocks in which

the actual components are interconnected.

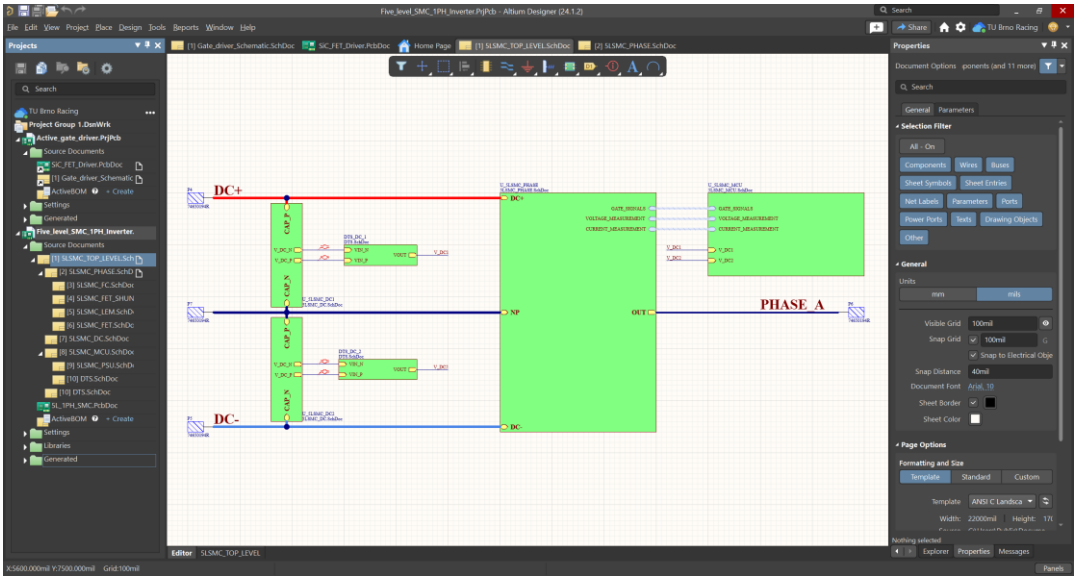


Fig. 4.16 Hierarchical schematic of the converter system.

To ensure that safe clearance between the low and high voltage side is maintained the IPC-2221B standard was used. This standard, apart from many other PCB design requirements, also specifies the required minimum conductor spacing based on the voltage between the two signals [188]. The spacing requirements are concluded in Figure 4.17.

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]
B3 - External Conductors, uncoated, over 3050 m [10,007 feet]
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]
A7 - External Component lead termination, with conformal coating (any elevation)

Fig. 4.17 IPC-2221B Electrical conductor spacing [188].

In Altium Designer, automatic clearance requirement control can be set up based on rule

definition. This involves specifying a distance to be maintained based on object properties, and the rule is checked during the design of the converter to ensure compliance [189]. Such rule definition is shown in Figure 4.18.

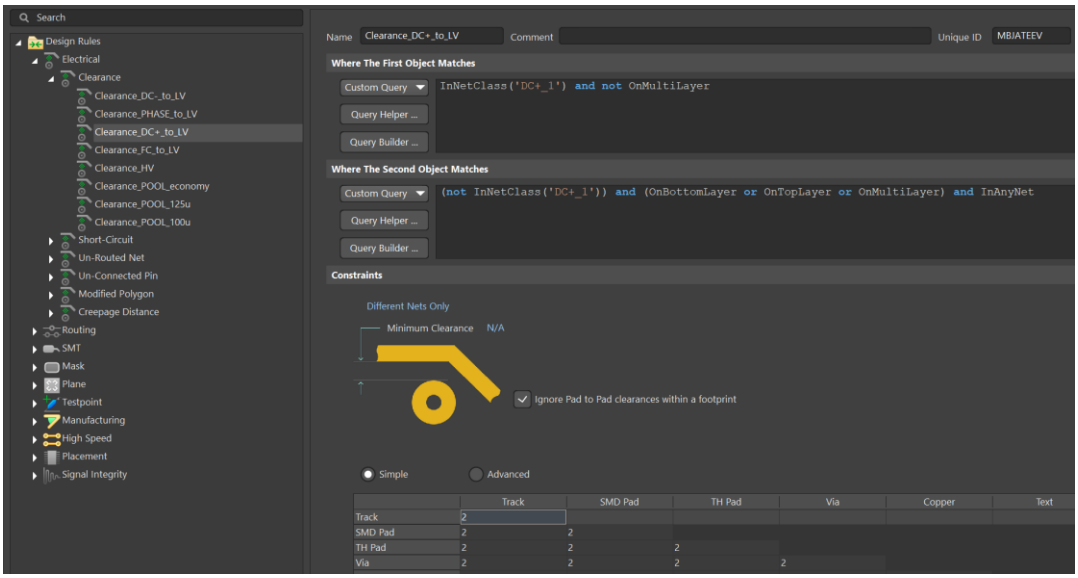


Fig. 4.18 Altium designer clearance rule definition.

First the active gate driver board was designed as a separate module following the previously described rules. The schematic of the active gate driver board is shown in Appendix C. Care was taken during the schematic layout to clearly distinguish the isolated and non-isolated sides. A component was then created based on the designed module, this allowed for simple placement of the driver in the main converter design.

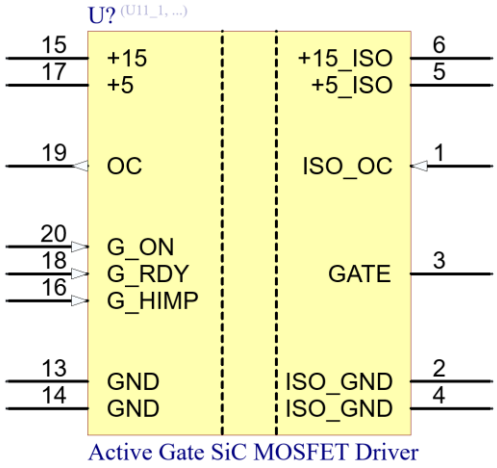


Fig. 4.19 Active gate driver schematic symbol.

In Figure 4.19 the schematic symbol of the active gate driver module can be seen. Such a part can then be used in other projects as well without the need to reference the original design file for pinout information etc. In Figure 4.20 the component can be seen used in the main converter schematic in the sheet for MOSFET control without current sensor.

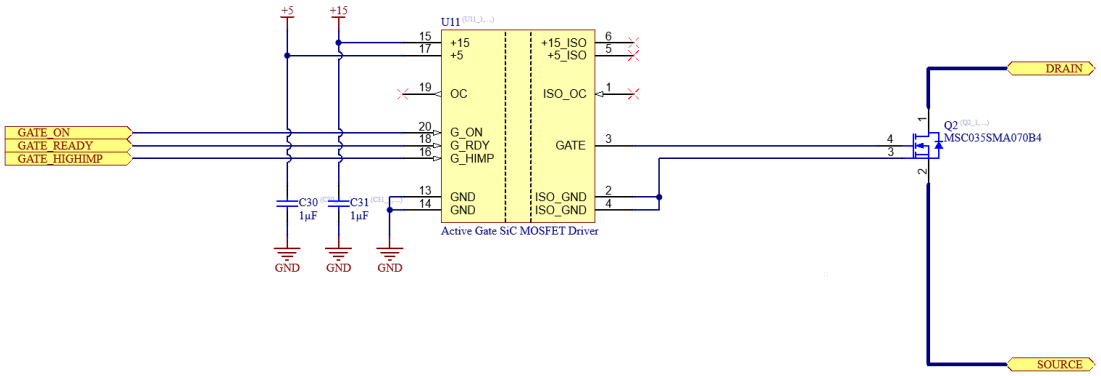


Fig. 4.20 MOSFET Control schematic sheet.

In the previous chapters the methods for current and voltage measurement are described, these methods are then used in the main converter board design. Due to the number of differential channels for each of the measurements signal harnesses are used, this allows for grouping of different signals into a singular stream [190]. Such grouping then allows for easier routing between the schematic blocks in the hierarchical design. In Figure 4.21a the grouping of gate signals for each of the MOSFETs is shown and in 4.21b the advantage in routing and simplification of the schematic can be seen.

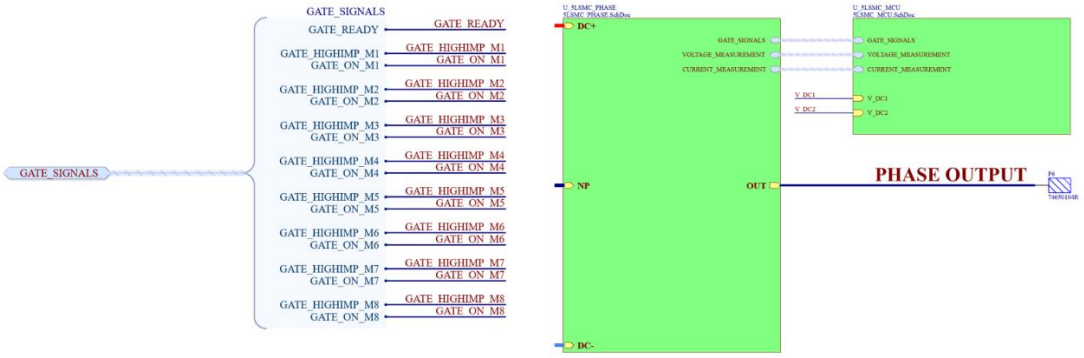


Fig. 4.21 Signal harness (a) group creation, (b) usage in hierarchical design.

All the control and measurement signals are then routed into a pair of 24 pin IDC connectors, these are then connected to a control board, depending on the control system that is to be used. Such design as chosen to allow for versatility and compatibility with different platforms. The entire schematic of the main converter board including the connector pinout is shown in Appendix D. The converter board is a single-phase leg of the entire converter, therefore, to achieve the three-phase capability, three of the converter boards are needed.

4.5.2 Printed circuit board

Based on the schematic design the printed circuit boards for both the main converter and the active gate driver were designed. Based on the best practices for PCB layout such as

ones described in [191], [192] and [193] care was taken to minimize the size of the commutation loops to reduce the EMI by placing the high power components close to each other. This also allowed for a reduction in the inductance of the traces by shortening them. Sensitive measurement components were placed as far away from the sources of noise as possible. The control and measurement signals are routed away from the high current path and are shielded by a ground plane. As previously described the IPC-2221B standard was followed during the design of the PCBs, in Figure 4.22 the minimum distance on the active gate driver board is shown on the PCB layout.

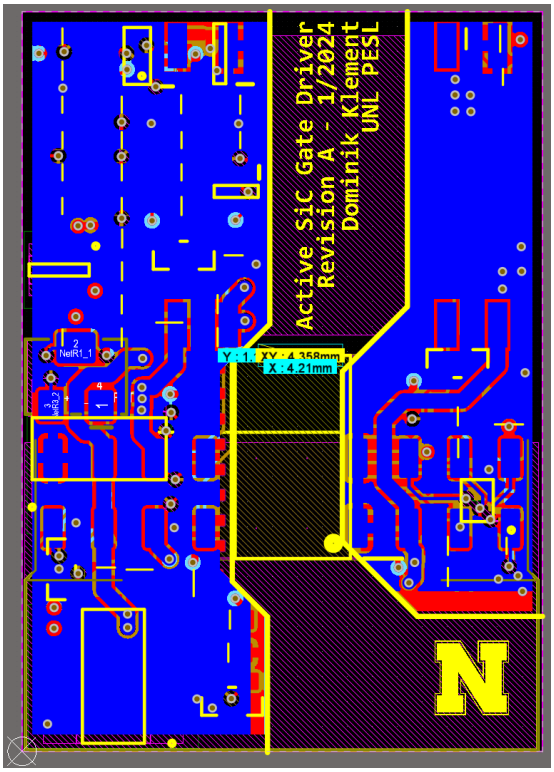


Fig. 4.22 Active gate driver PCB layout.

The active gate driver was designed on four-layer PCB, even though a two-layer board would have been sufficient for routing all the signals. This was done to improve the signal integrity and reduce crosstalk. The gate driving signal is a pulsed signal that carries significant power and may cause electromagnetic interference on the control signals; therefore, it was routed to be as short as possible and away from them. The additional layers were used to distribute power to the components and to also improve the integrity of the ground plane. Saturn PCB design Toolkit was used to ensure that conductor width is sufficient for the current to be carried. This tool also allows for calculation of the minimum conductor spacing and many different useful calculations for the PCB design [194]. In Figure 4.23 an example of a calculation for the current carrying capacity of a PCB trace can is shown.

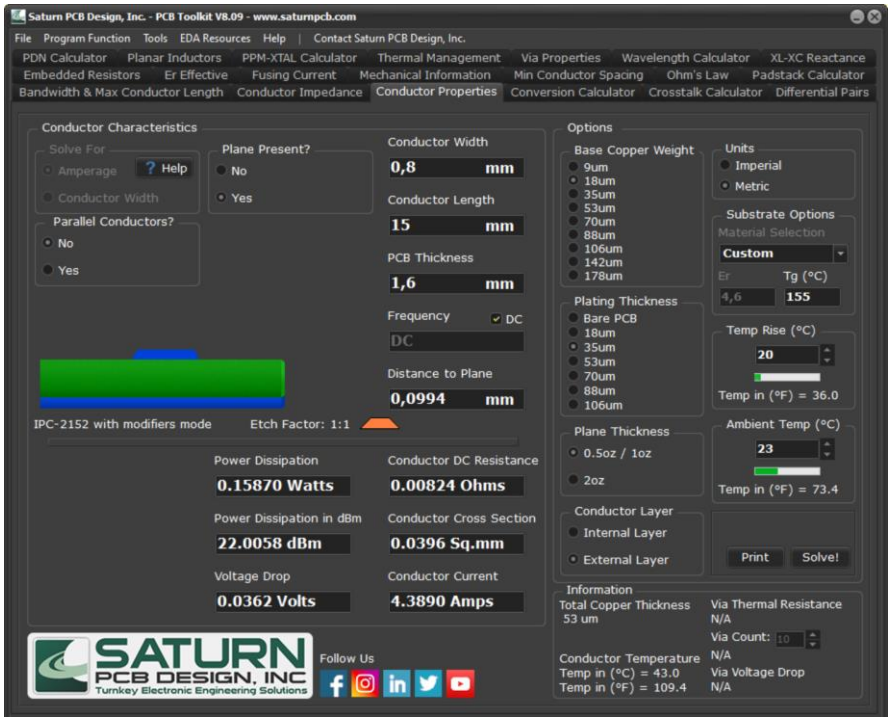


Fig. 4.23 Saturn PCB Design tool example calculation.

The active gate driver board is designed to be plugged into the main converter board vertically, this was done to minimize the footprint of the converter and in turn improve the EMI properties. In Figure 4.24, the rendering of the final design of the active gate driver board is shown.

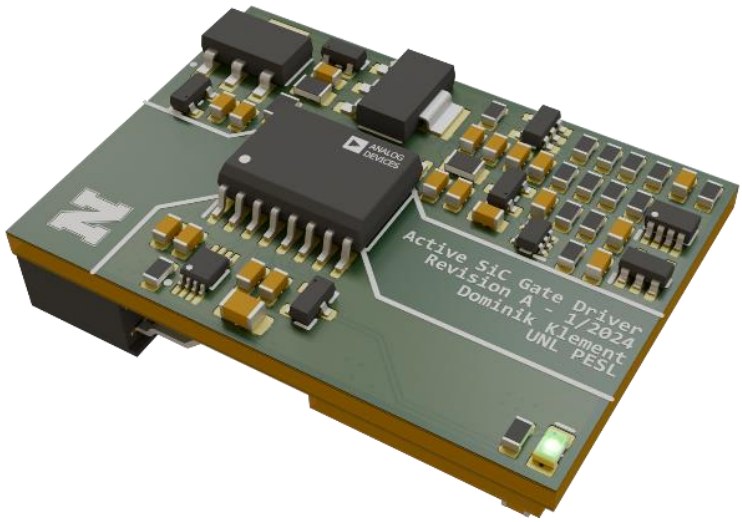


Fig. 4.24 Rendering of the active gate driver PCB.

A similar approach was taken in the design of the main converter board. The final size of the single-phase main converter board is 185 by 124 millimeters. To reduce flex of the board when mounting components of connecting the connectors a stack up with thicker core was chosen, the main converter board is two millimeters thick. As the design utilizes

several circuits, which are identical to each other a room object is used to duplicate the PCB layout of these parts, rooms allow for repeated circuits to be routed once and then copied onto the other identical circuits [195]. In Figure 4.25 rooms that are used to copy the MOSFET with current measurement blocks can be seen.

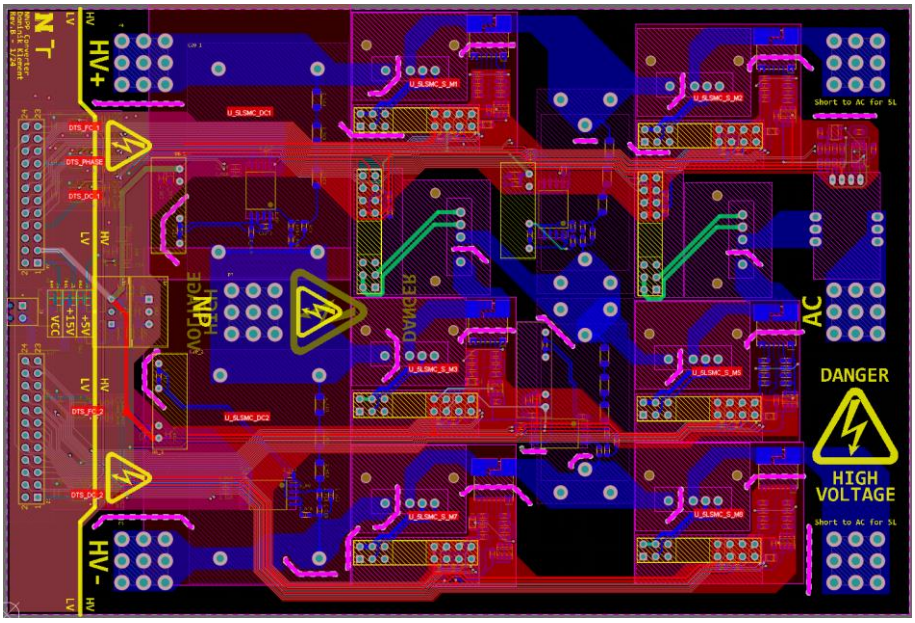


Fig. 4.25 Single phase of the converter PCB layout.

All distances between the isolated low-voltage control side and the high-voltage side are maintained according to the IPC-2221B standard. Additionally, isolation slots are added to the board to add an extra layer of protection in places where the isolation distance is borderline sufficient.

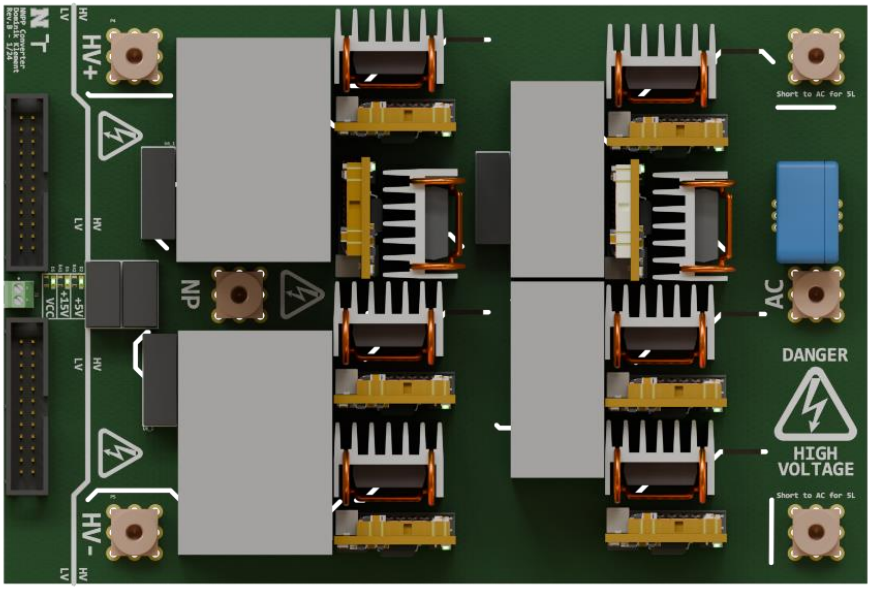


Fig. 4.26 Rendering of the top side of the converter PCB.

Figure 4.26 shows the final design of the main converter board, the two 24-pin IDC

connectors can be seen as well as the high voltage input terminals. The vertical mounting of the active gate driver modules is also visible. As the top layer is occupied with the DC-link and flying capacitors as well as the MOSFETs and their respective heatsinks, most of the other components on the main board are placed on the bottom layer, this was done so that automated single sided PCB assembly can be utilized to save time assembling the boards. The bottom view is shown in Figure 4.27.

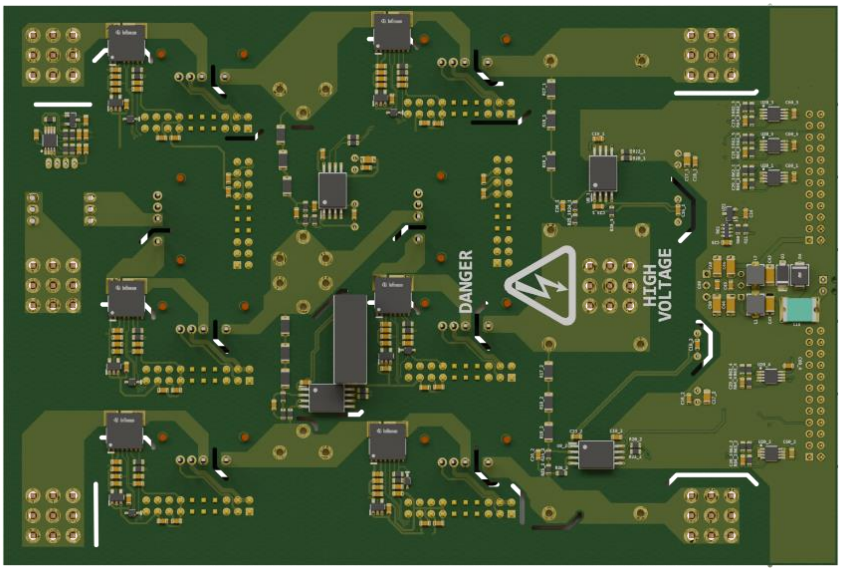


Fig. 4.27 Rendering of the bottom side of the converter PCB.

The designed active gate driver board and the main converter board are to be manufactured and assembled in the future; however, evaluation of their functionality is not a part of this thesis and is to be performed as a part of further work.

5. CONCLUSION

This thesis provides a comprehensive study of multilevel converters, their applications, and their potential for future use in various fields such as energy, defense, automotive, medical, and aerospace. It dives into the unique properties of five different multilevel topologies. The nested neutral point piloted converter topology is highlighted due to its advantageous properties in terms of voltage stress distribution and redundant switching states.

A subinterval analysis of a five-level three-phase circuit is performed to identify potential faults during operation. The thesis proposes a control algorithm to achieve a fault ride-through capability, particularly for short circuit faults occurring in the inner cell group, which can cause disruptive currents and potential damage to the converter.

Further research could be aimed at developing other fault detection and mitigation methods to improve the detection speed and to reduce the number of additional sensors for the algorithm to operate sufficiently. Other topics could be focused on improving the efficiency of the control algorithm during normal operation by optimizing the time spent in the high impedance mode. The use of similar fault detection and ride-through capability could be explored in other multilevel converter topologies.

5.1 Comparative analysis

The proposed fault ride-through method has the potential to improve the reliability of the nested neutral point piloted topology using active gate control ensuring fault detection and subsequent control strategy change. Other algorithms aiming to achieve a similar task have been a focus of many research institutions with most papers being published in the last five years as the topology offers many advantages, an overview of methods that were compared in this thesis can be seen in Table 5.1.

A number of different fault detection methods were proposed, such as the method proposed in [196], where measurement of either the output voltage of the converter or the floating capacitor voltages is used to compare them to the predicted values with a KNN algorithm being utilized to distinguish between real and false-positive faults.

Another software based method is proposed in [61], where a deep learning method together with a long short-term memory is proposed to locate and detect a fault in the converter circuit. The proposed method allows for detection of both the open- and short-circuit faults. Additional components in the high-current path are used to prevent the formation of a short-circuit loop, the algorithm then switches to a three-level modulation scheme.

In [197] an open-circuit fault detection method is proposed based on analyzing the circuit signals and extraction of their time domain characteristics, an unsupervised feature learning algorithm combining DGUFS filter and RFFS wrapper is then used for fault

detection. The method is validated by simulations as well as experiments and is not limited to a specific topology.

The paper [198] proposes a simple method for open-circuit fault detection, window comparators are used to track the output voltage levels and in combination with the current direction the fault is detected and localized. Bypass circuits are proposed to reroute the output for the converter to continue to operate with a reduced number of output levels.

Table 5.1 Fault-tolerant method comparison overview

	Proposed method	**Method A**	**Method B**	**Method C**	**Method D**
Fault type detection	Short and open circuit	Open circuit	Short and open circuit	Open circuit	Open circuit
Detection method	Fast current sensing and active gate driving	KNN classification	Wavelet packet transform and LSTM network	DGUFS filter and RFFS wrapper	Voltage sensing and fast window detectors
Fault ride-through	Yes	No	Yes	No	No
Computation intensity	Low	Medium	High	Medium	Low
Additional hardware	Yes	No	Yes	No	Yes
Simulation validation	Yes	Yes	Yes	Yes	Yes
Experimental validation	No	No	Yes	Yes	Yes
Disadvantages	Need for active gate drivers and additional current sensing	Only open circuit fault detection	Additional components required for fault ride-through	Only open circuit fault detection	Additional hardware and open circuit fault detection
Proposed in	-	[196]	[8]	[197]	[198]

5.2 Summary

As a part of this thesis first the multilevel converters were described, explaining their applications, ranging from traction inverters to HVDC transmission converters also discussing their potential for future use in space applications, where their discussed properties pose great advantages if implemented correctly and if the fault-tolerant algorithm is used.

Multilevel converters are a broad topic, with many different topologies, which each have unique properties, work on different principles and may be suitable for different applications. Five topologies were discussed, their working principles as well as their schematic were described. These topologies were selected as they are capable of being

implement in the novel high-frequency press-pack (HFPP) SiC FET module proposed in [48].

The nested neutral point piloted converter topology is discussed in detail in the next chapter, this topology was selected as the main focus of this thesis as it offers interesting properties in terms of distribution of voltage stress amongst the components in the circuit as well as redundant switching states, which have the potential to be used as the backbone of a fault ride-through capable converter suitable for high-reliability application such as defense, automotive, medical and aerospace. A subinterval analysis of a five-level three-phase circuit is performed to determine the potential faults that may occur during operation. The types of faults were grouped into two groups. The outer cell type of fault is not considered during the development of the control algorithm as the switches are redundant and the fault was concluded to be detectable and solvable using traditional MOSFET protection methods. When a fault occurs in the switch in the inner cell group, a current loop may be formed by the DC-link and flying capacitors. This current is disruptive to the functionality of the converter and may cause irreversible damage. A control algorithm developed as a part of this thesis aims to mitigate this type of fault by use of active gate driver to manipulate the conductivity of specific switches and use this property to check that current is not flowing through disabled switches.

The control algorithm consists of a number of parts, some dedicated to the basic control of the converter itself during normal operation, such as the active capacitor voltage balancing algorithm, coordinate transformations and space vector modulation, which are components to be implemented in a converter to achieve an efficient three-phase control of a motor. These parts and their implementation in the simulation are discussed in chapter 3, together also with the part dedicated to the fault ride-through capabilities. Available fault detection methods are discussed and suitable ones for the prototype and simulation is chosen, the fault ride-through strategy is also described and block diagram for the fault ride-through part of the control algorithm is shown.

Design of the prototype to perform real-world experimental tests of the control algorithm is described in chapter 4.5. The main component choice is described in Chapter 4 and is based on the availability of the components as well as the equipment of the testing laboratory and the available motor. Requirements of the algorithm for control and measurement signals of the converter are considered in chapter 4.3, where the choice of current and voltage measurement techniques are described in detail. The voltage is measured using a high-voltage voltage divider and a high-bandwidth isolated amplifier to convert the signal to the low voltage control side. Two different sensors are used for the current sensing, the phase current is measured using an off-the-shelf current transducer, where the current measurement of the switches, which is a necessary input to the fault ride-through algorithm is using a coreless current sensor due to size constrains.

An active gate driver is developed to control the impedance of the switches used in the converter. The requirements and subsequent implementation are described in chapter

4.4, the gate driver is a modular board which is slotted into the main converter board. Such a design was chosen to simplify the design of the main converter board and to allow modifications to the gate driver module. The main converter board design is described in chapter 4.5.2, the board is a single-phase leg of the three-phase converter, such a design was chosen mainly for manufacturing reasons. Topics for potential future work and research are presented.

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ABBREVIATIONS

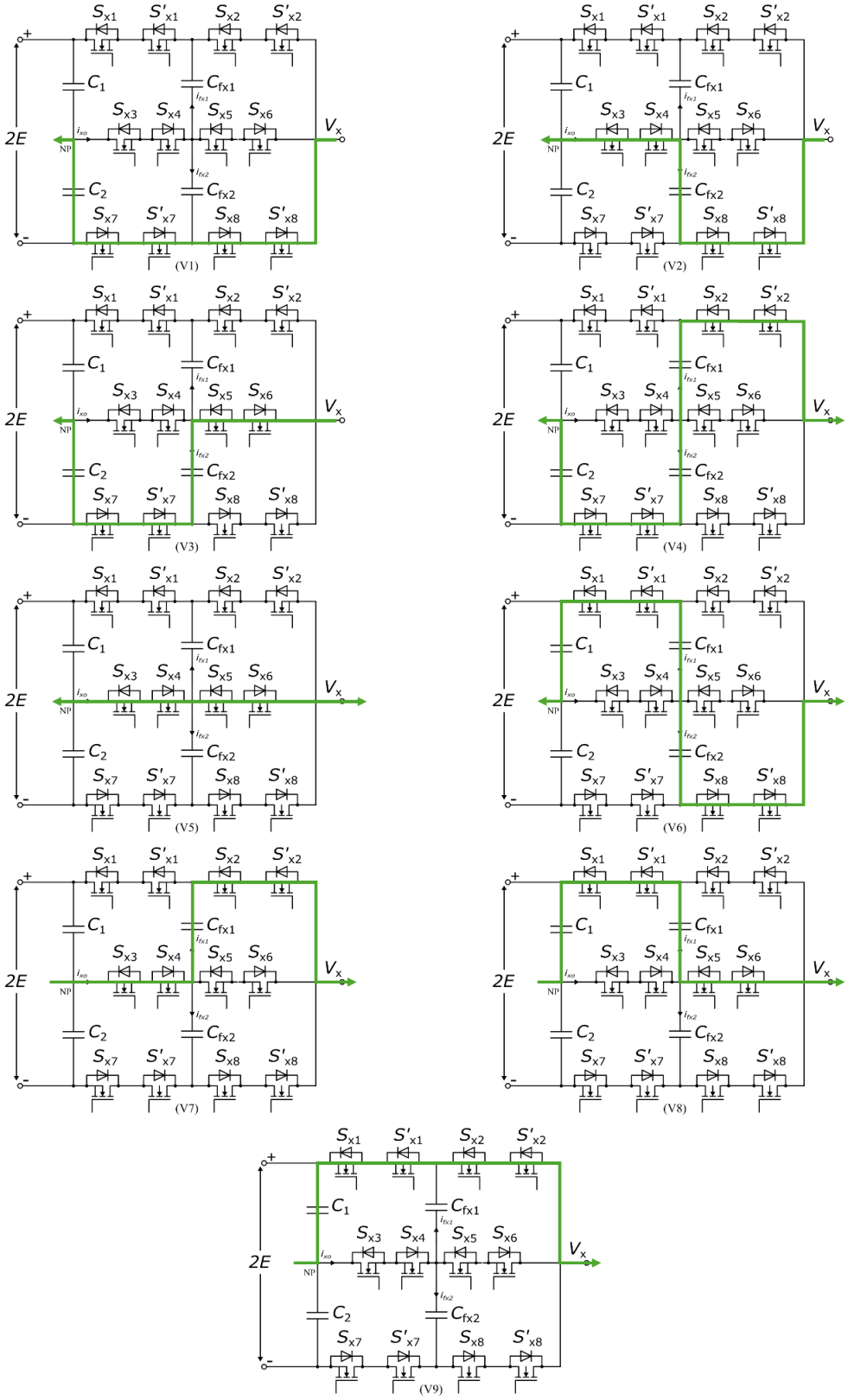
Abbreviations:

HVDC	High-Voltage Direct Current
FACTS	Flexible Alternating Current Transmission Systems
SiC	Silicone Carbide
IGBT	Insulated-Gate Bipolar Transistor
UHVDC	Ultra High-voltage Direct Current
STATCOM	Static Synchronous Compensator
DC	Direct Current
EMI	Electromagnetic Interference
RFI	Radio Frequency Interference
FOC	Field Oriented Control
DTC	Direct Torque Control
EV	Electric Vehicle
HEV	Hybrid Electric Vehicle
IM	Induction Motor
AC	Alternating Current
UPS	Uninterruptible Power Source
NPC	Neutral Point Clamped
VSC	Voltage Source Converter
CSI	Current Source Inverter
HFPP	High-Frequency Press-Pack
NNPP	Nested Neutral Point Piloted
ANPC	Active Neutral Point Clamped
CCSM	Cross-Connected Submodule
NPCSM	Neutral Point Clamped Submodule
B2B	Back-to-Back
FC	Flying Capacitor
ACVB	Active Capacitor Voltage Balancing
MTPA	Maximum Torque Per Ampere
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
SVPWM	Space Vector Pulse Width Modulation
PWM	Pulse Width Modulation
HiL	Hardware in Loop
IPMSM	Interior Permanent Magnet Synchronous Motor
THD	Total Harmonic Distortion
ESR	Equivalent Series Resistance

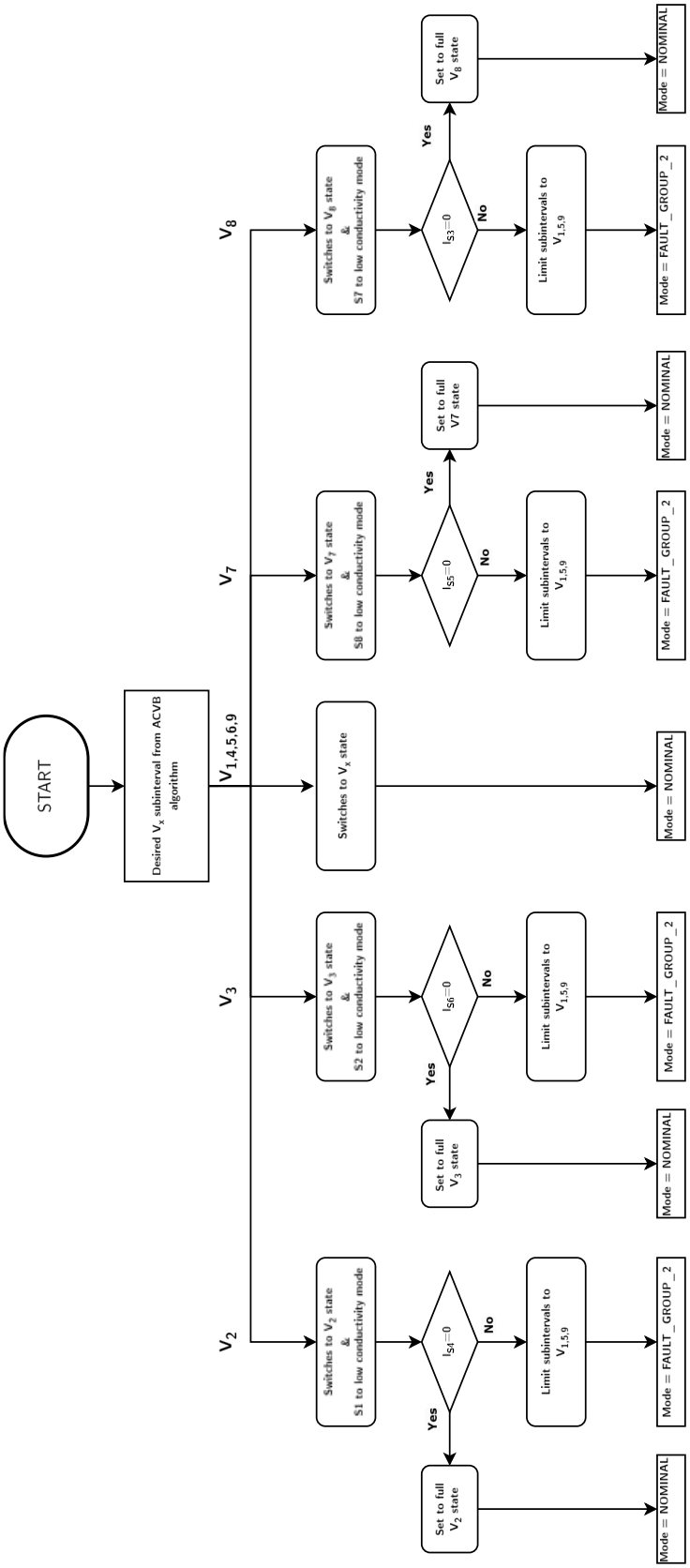
ESL	Equivalent Series Inductance
LDO	Low-dropout
RMS	Root Mean Square
DSP	Digital Signal Processor
PCB	Printed Circuit Board
AI	Artificial Intelligence
DGUFS	Dependence-Guided Unsupervised Feature Selection
RFFS	Random Forest Feature Selection
KNN	K-Nearest Neighbor
LSTM	Long Short-Term Memory
SMD	Surface Mount Device

LIST OF APPENDICES

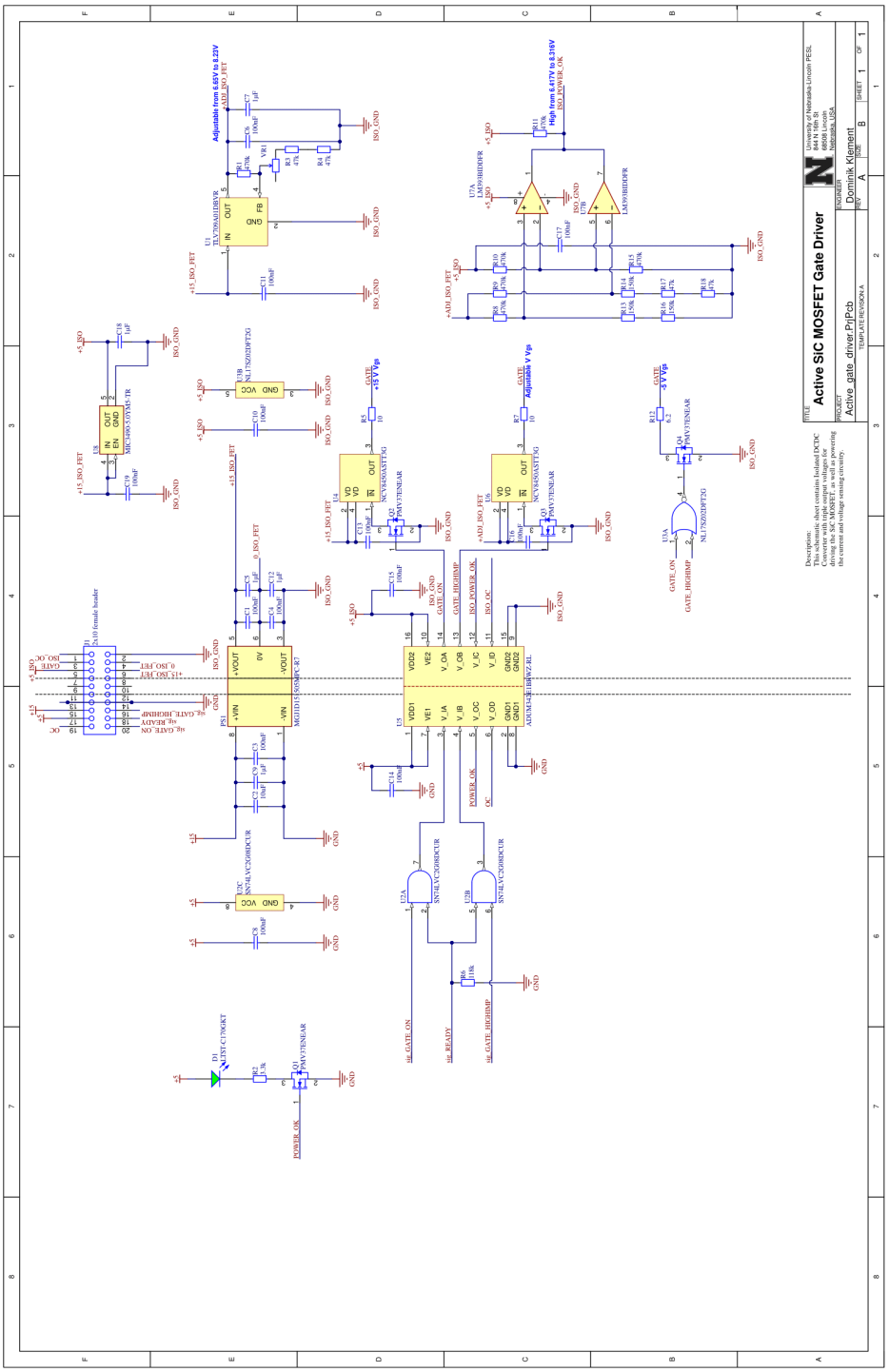
Appendix A - Subinterval analysis



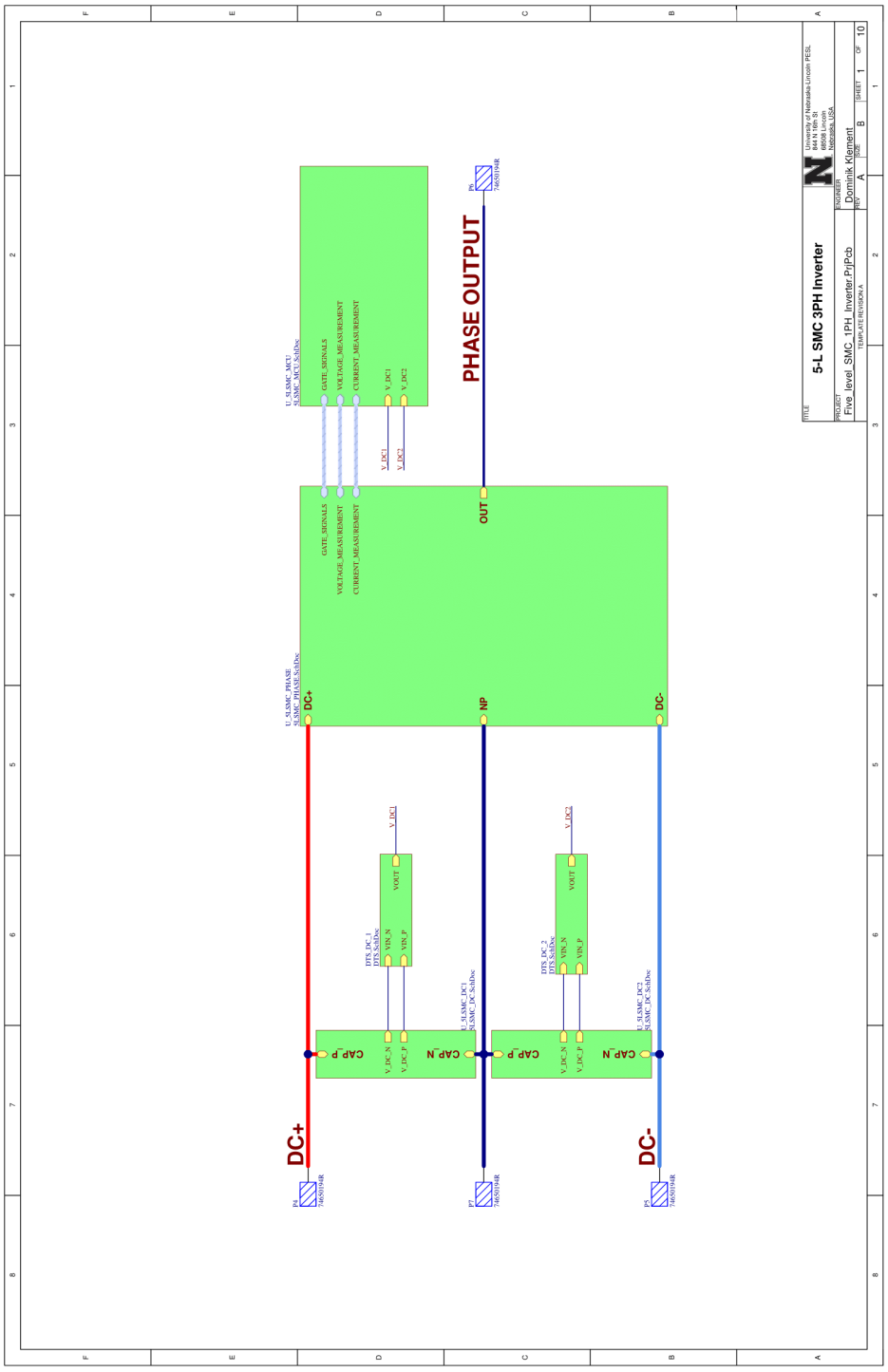
Appendix B - Fault ride-through control-flow

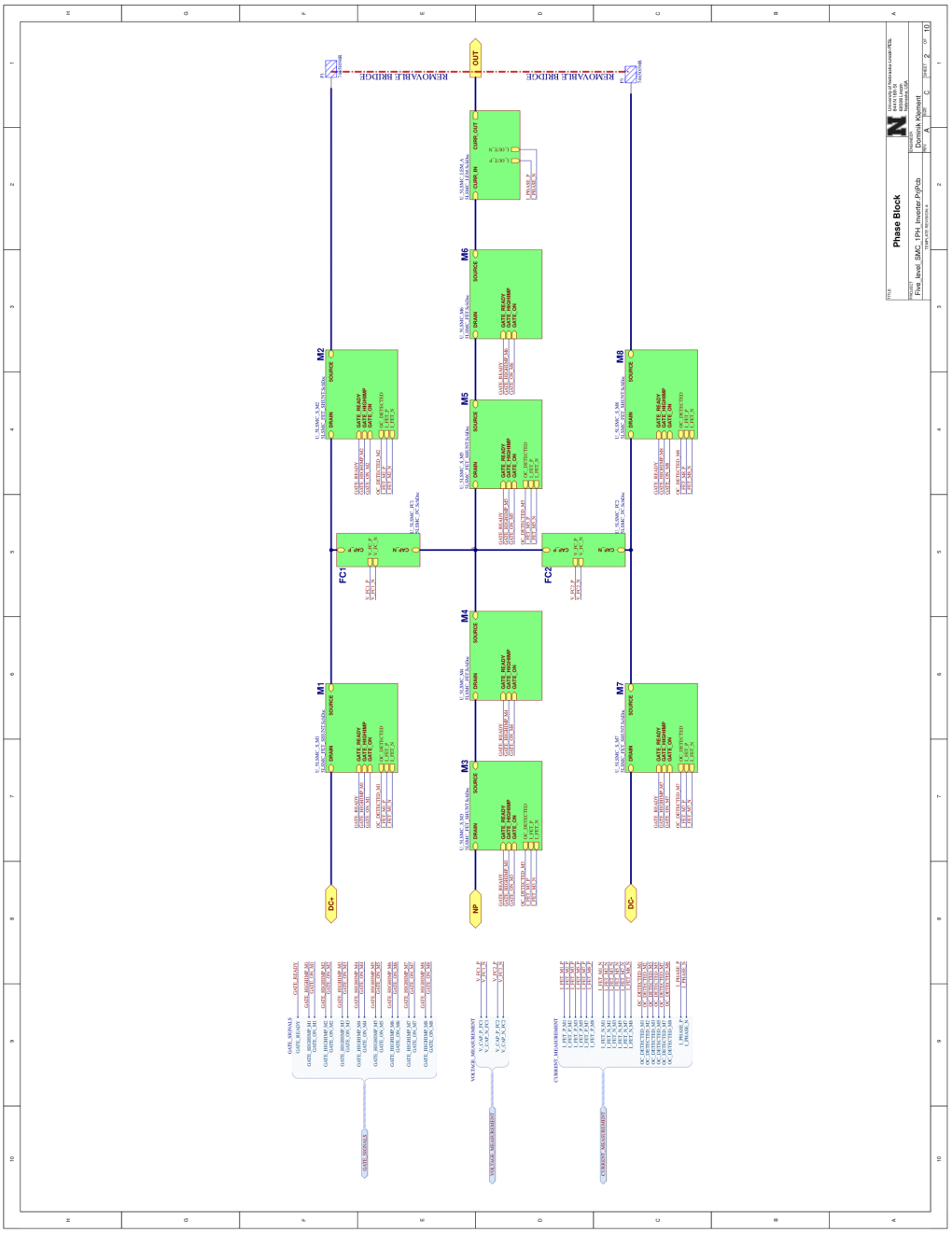


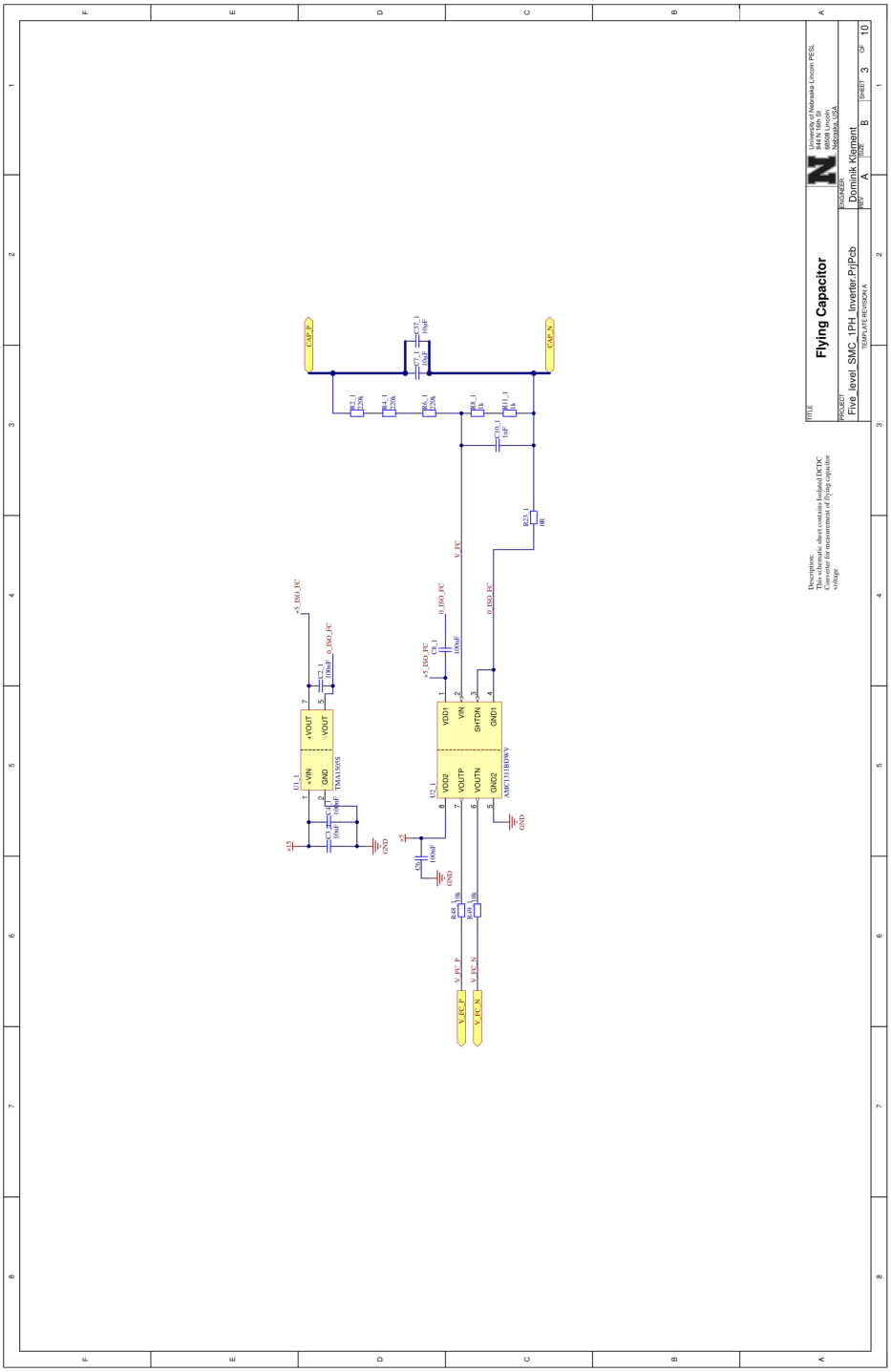
Appendix C - Active gate driver schematics



Appendix D - Main converter schematics




REMOVABLE BRIDGE
REMOVABLE BRIDGE
OUT
M1
M2
M3
M4
M5
M6
M7
M8
FC1
FC2
DC+
NP
DC-
Phase Block
Five_level_SMC_IPH_Inverter.PrjDsn
Dominik Kliment


TITLE
Flying Capacitor
PROJECT
Five level_SMC_1PH_Inverter.PrjPcb
ENGINEER
Dominik Klement
SHEET 3 OF 10
Description:
This schematic sheet contains Isolated DCDC
Converter for measurement of flying capacitor
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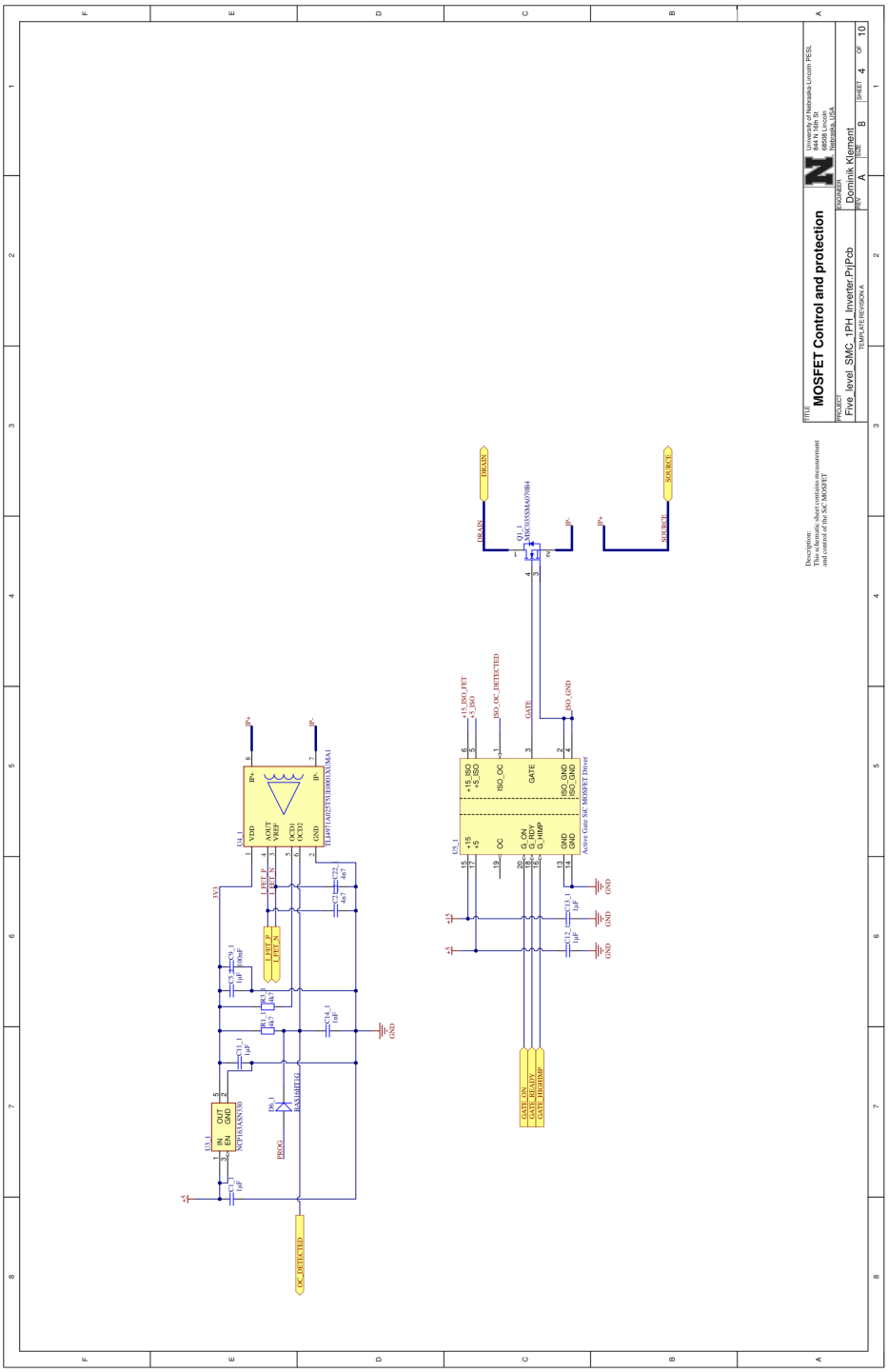
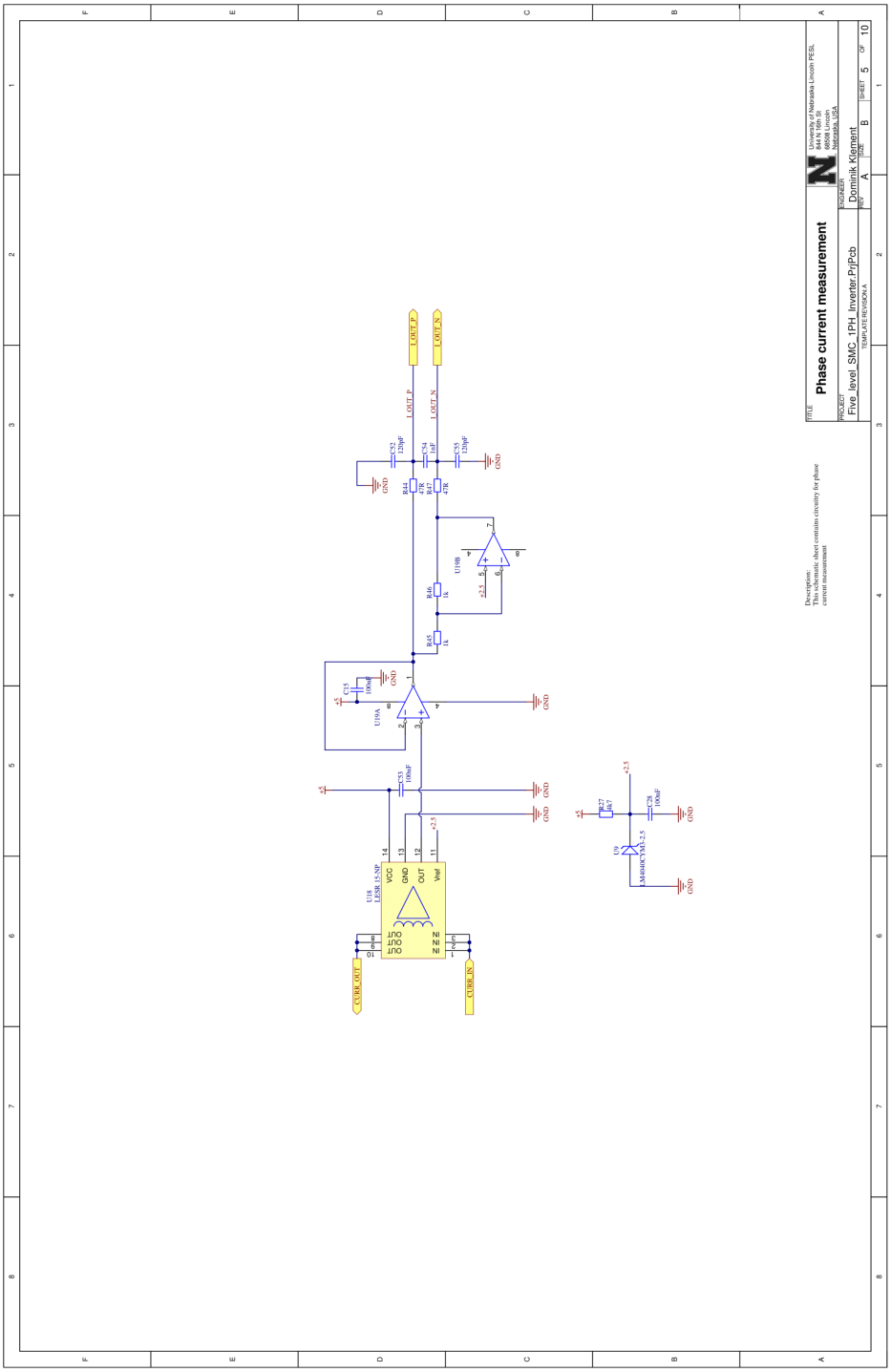
C4P_N
V_FC
0_ISO_FC
+5_ISO_FC
+15
GND
V_FC_P
V_FC_N


MOSFET Control and protection
Five_level_SMC_1PH_Inverter.PrjPcb
Dominik Klement
DRAIN
SOURCE
GATE
Active Gate SiC MOSFET Driver
ISO_OC_DETECTED
OC_DETECTED
GATE_ON
GATE_READY
GATE_FAULT
PROG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Phase current measurement
PROJECT
Five_level_SMC_1PH_Inverter.PrjPcb
ENGINEER
Dominik Klement
SHEET 5 OF 10
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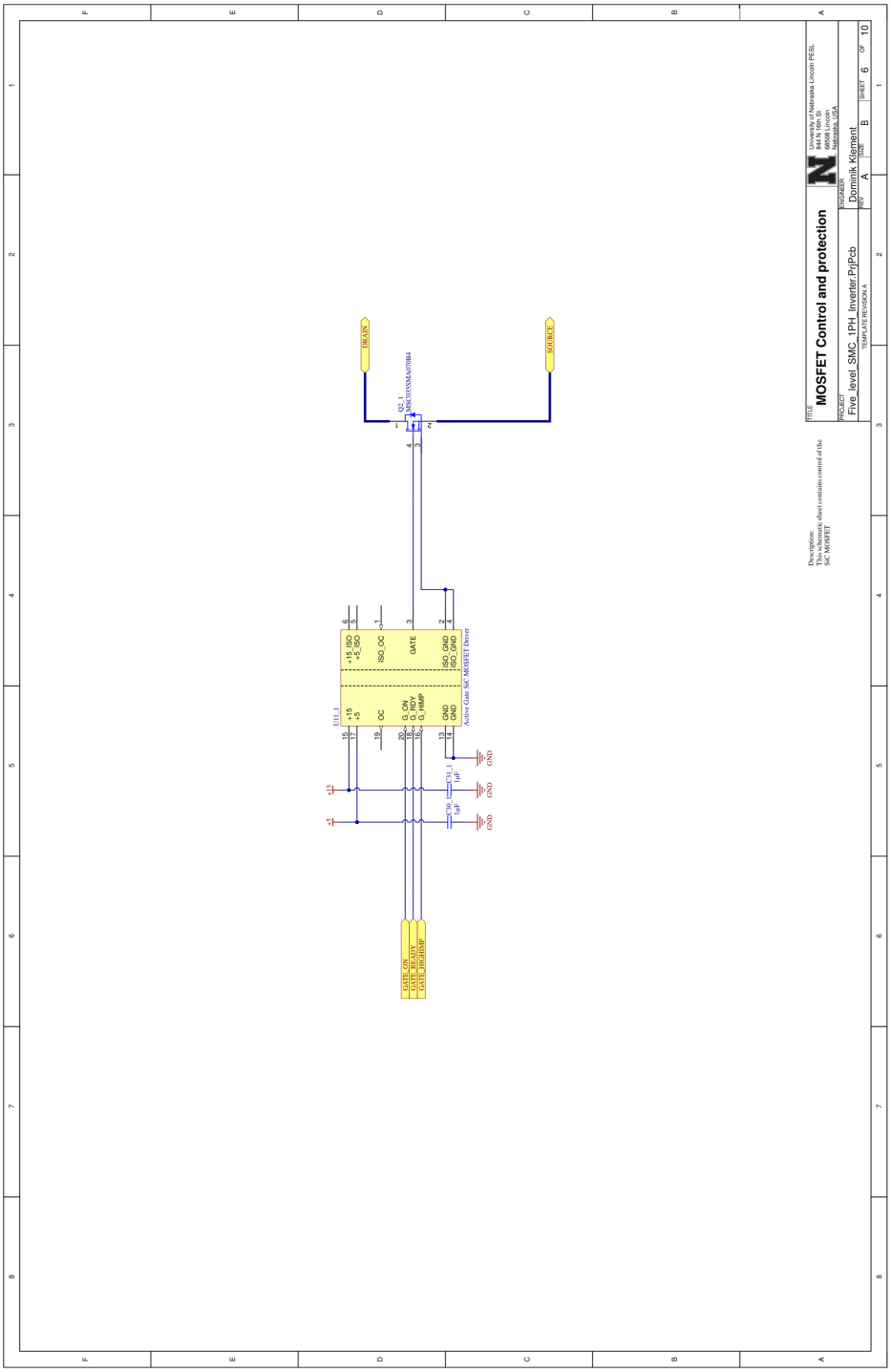
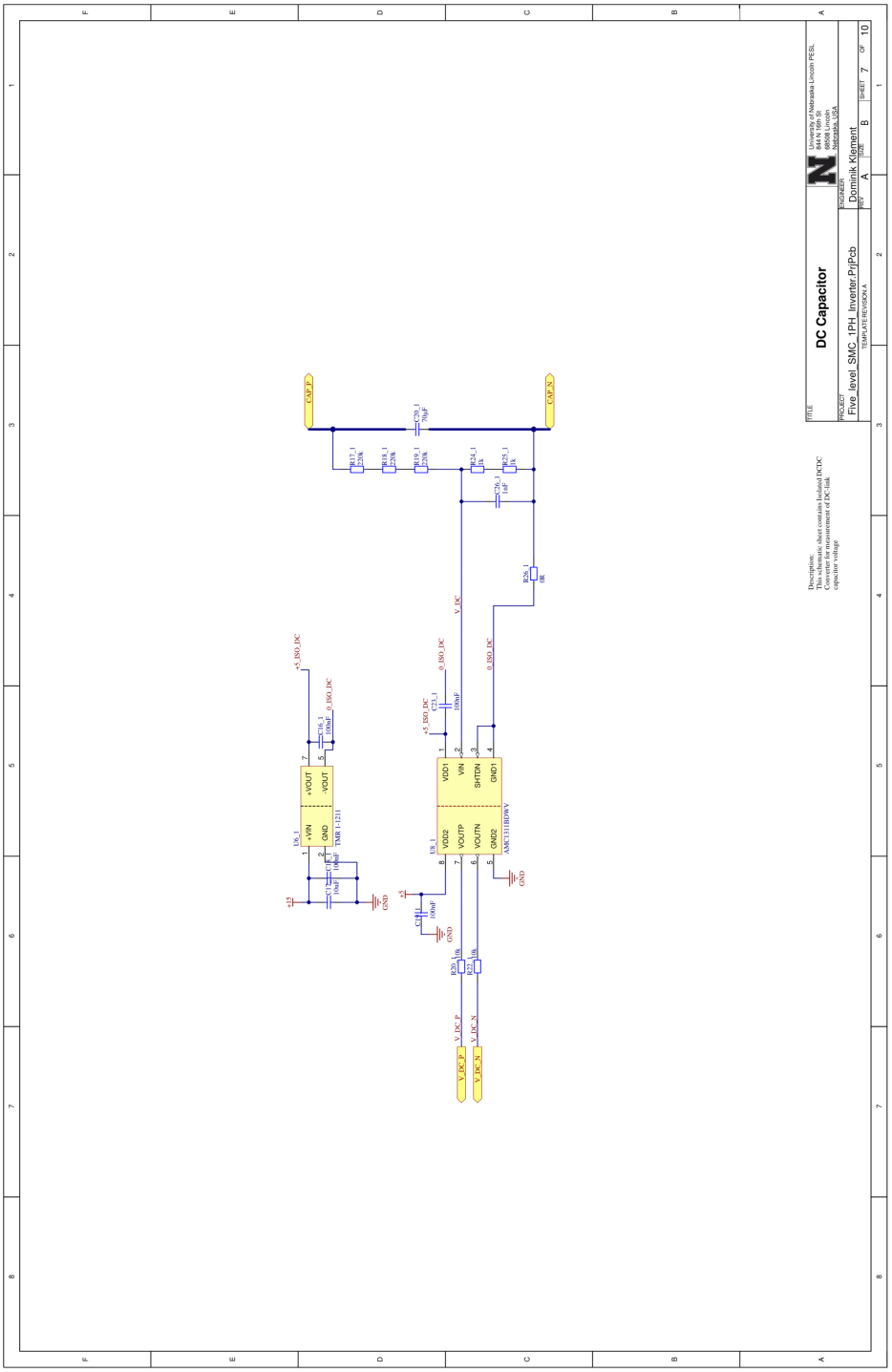

MOSFET Control and protection
Five_level_SMC_1PH_Inverter.PrjPcb
Dominik Klement
University of Nebraska Lincoln PESL
Active Gate SiC MOSFET Driver
DRAIN
SOURCE
GATE_ON
GATE_OUT
GATE_RAMP


DC Capacitor
Five level SMC 1PH Inverter.PrjPcb
Dominik Klement
CAP_P
CAP_N
V_DC
0_ISO_DC
+5_ISO_DC
V_DC_P
V_DC_N
VDD1
VIN
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GND1
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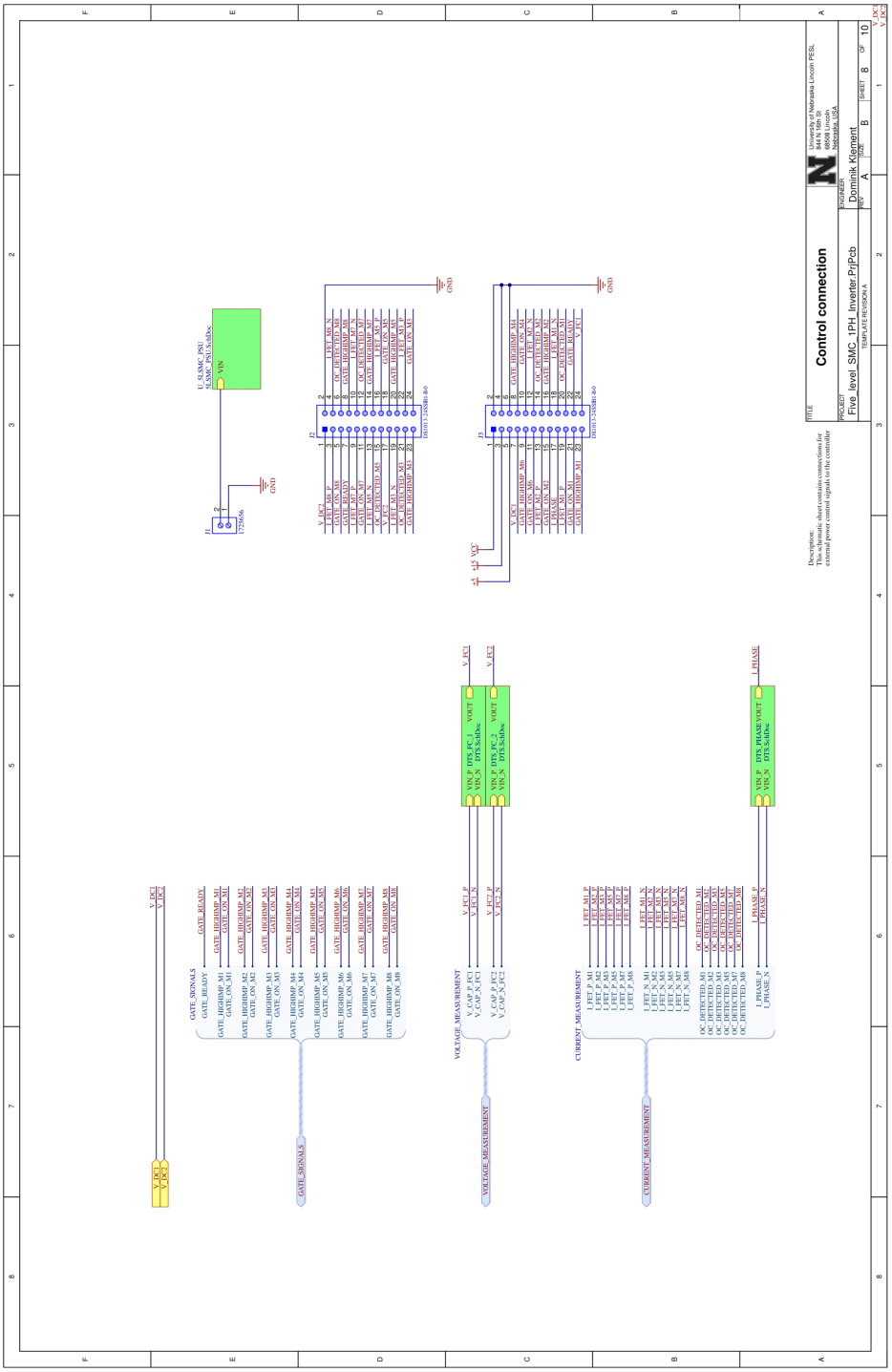
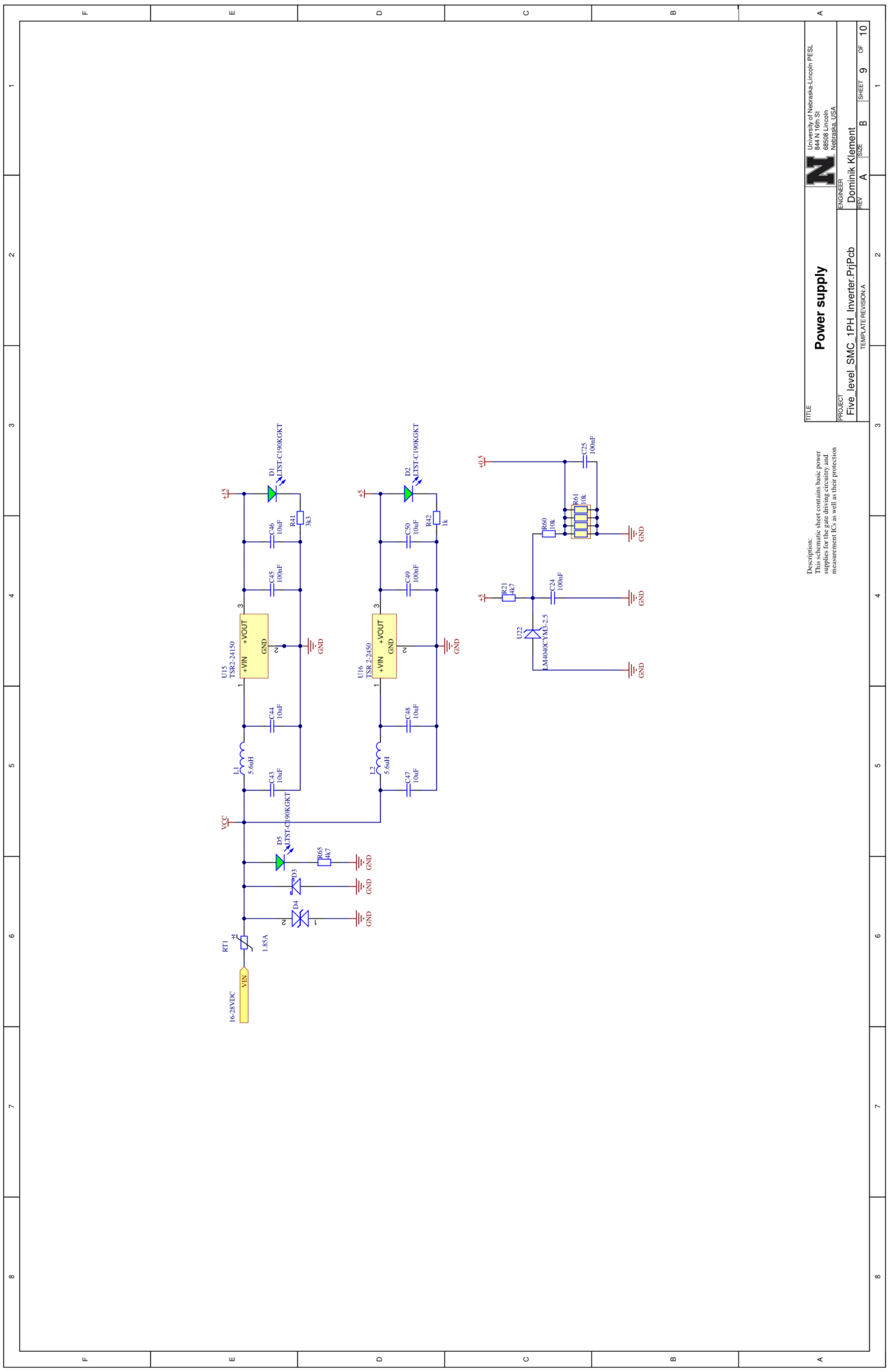
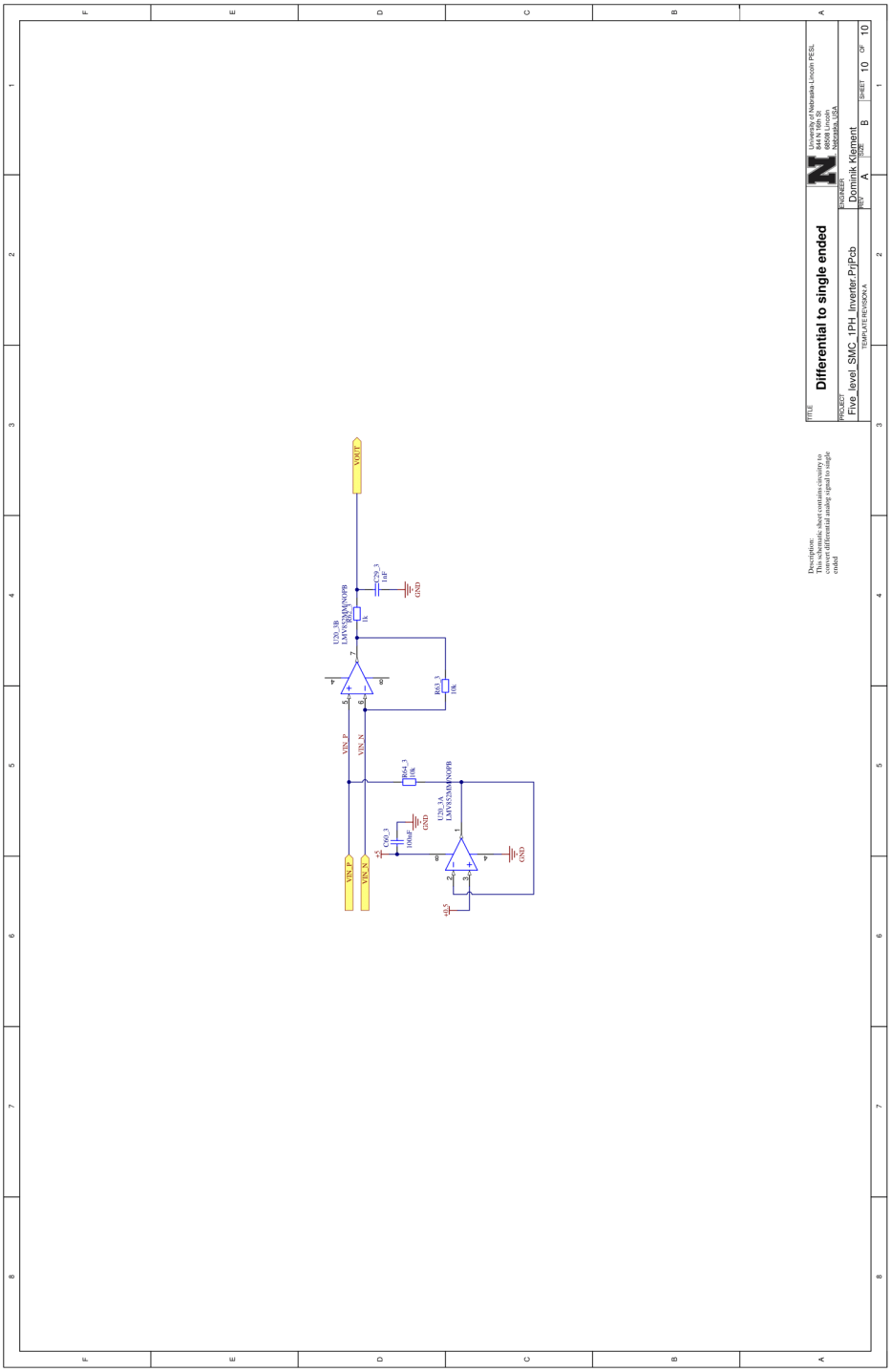
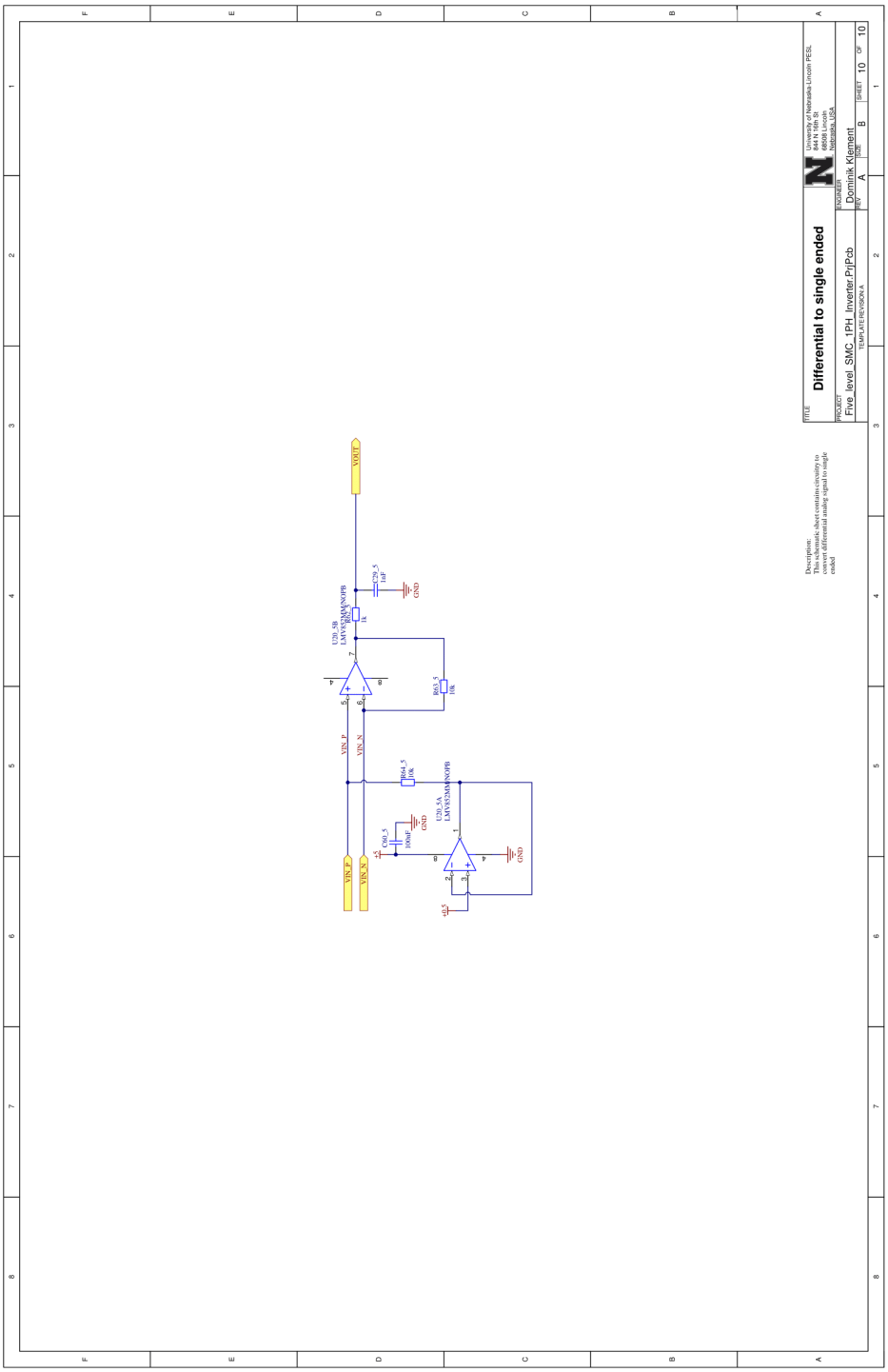
VOUTP
VOUTN
GND2
+VIN
GND
+VOUT
-VOUT
GND

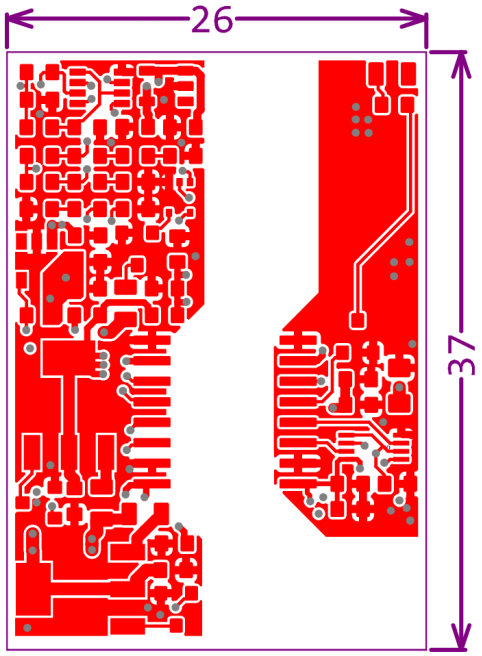

Control connection
Five level SMC 1PH Inverter.PrjPcb
Dominik Klement
University of Nebraska Lincoln PESL
Description:
This schematic sheet contains connections for external power control signals to the controller

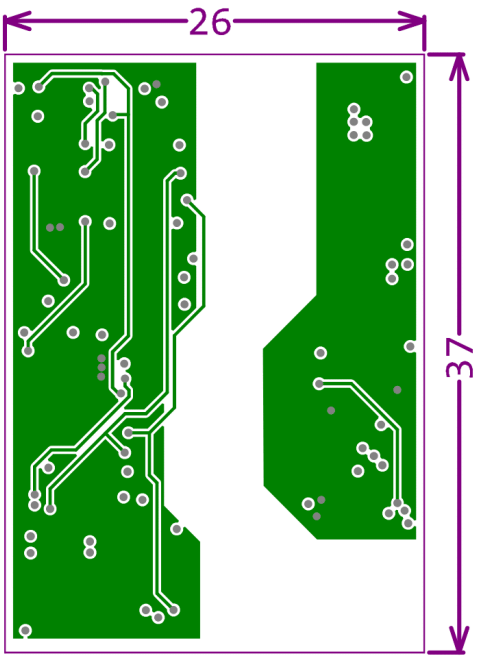

Description:
This schematic sheet contains basic power supplies for the gate driving circuitry and measurement ICs as well as their protection
TITLE
Power supply
University of Nebraska-Lincoln PESL
844 N 16th St
68508 Lincoln
Nebraska, USA
PROJECT
Five_level_SMC_1PH_Inverter.PrjPcb
TEMPLATE REVISION:A
ENGINEER
Dominik Klement
REV A
SIZE B
SHEET 9 OF 10

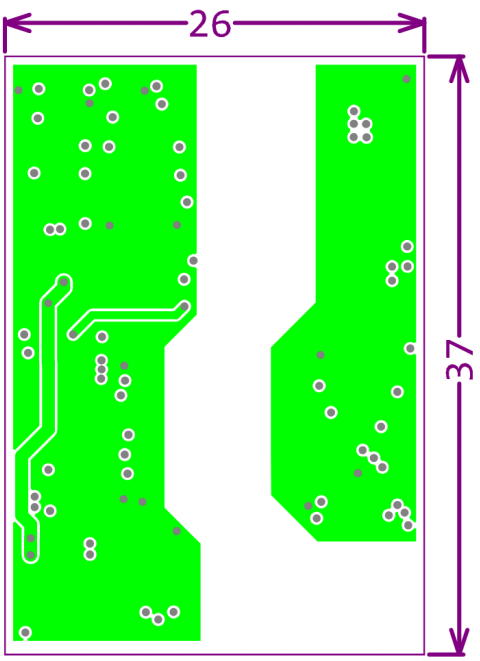

Differential to single ended
Five_level_SMC_1PH_Inverter.PrjPcb
Dominik Klement
University of Nebraska-Lincoln PESL
844 N 16th St
Lincoln NE 68588-0511
Nebraska, USA
Description:
This schematic sheet contains circuitry to convert differential analog signal to single ended
VOUT
VIN_P
VIN_N
GND
+5
+15

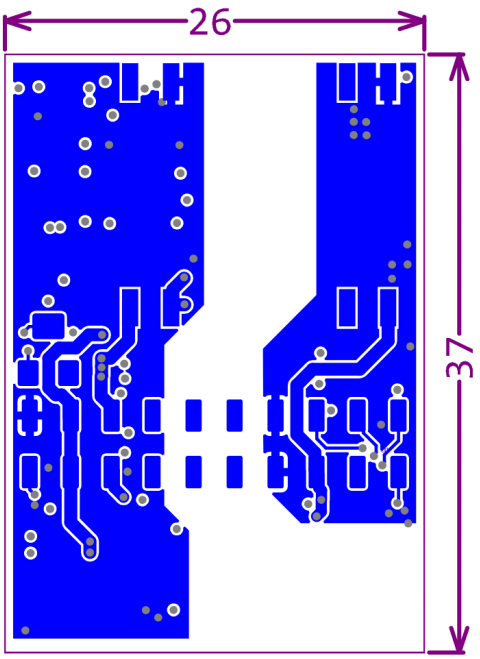

Differential to single ended
Five_level_SMC_1PH_Inverter.PrjPcb
Dominik Klement
University of Nebraska-Lincoln PESL
844 N 16th St
68588 Lincoln
NEBRASKA
Description:
This schematic sheet contains circuitry to convert differential analog signal to single ended
VOUT
VIN_P
VIN_N
VIN_P
VIN_N
GND
GND
GND
+5
+5
-5

Appendix E - Active gate driver PCB

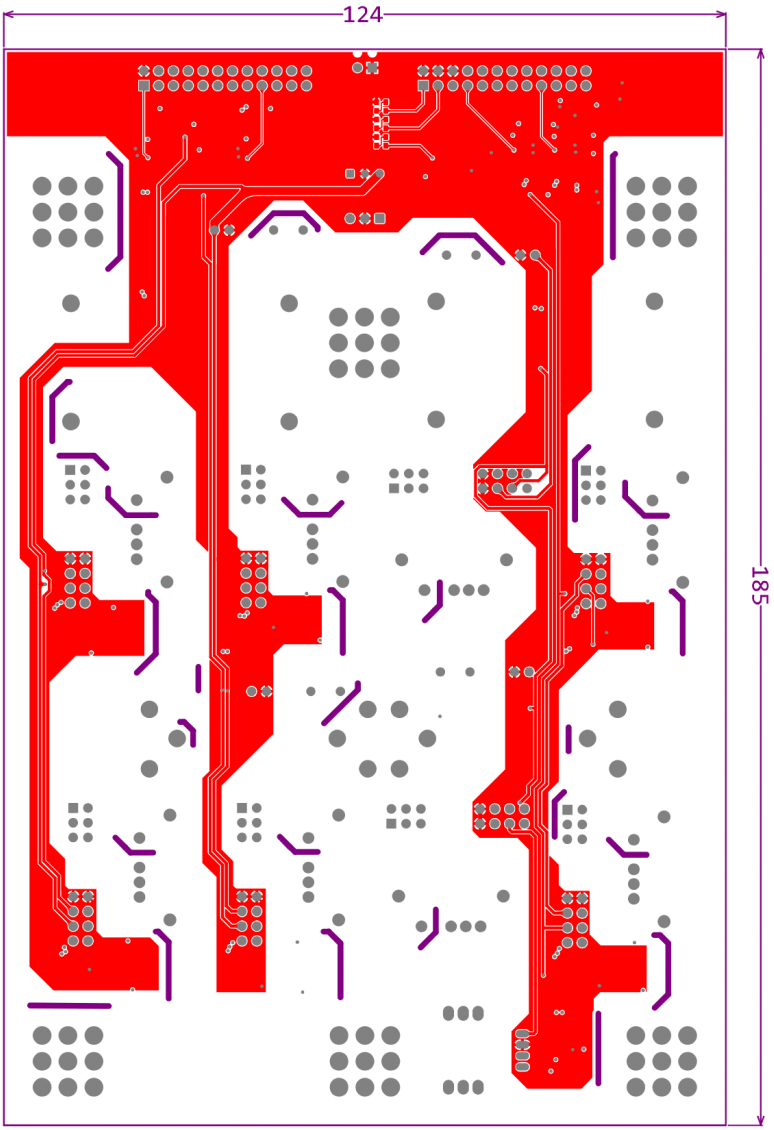


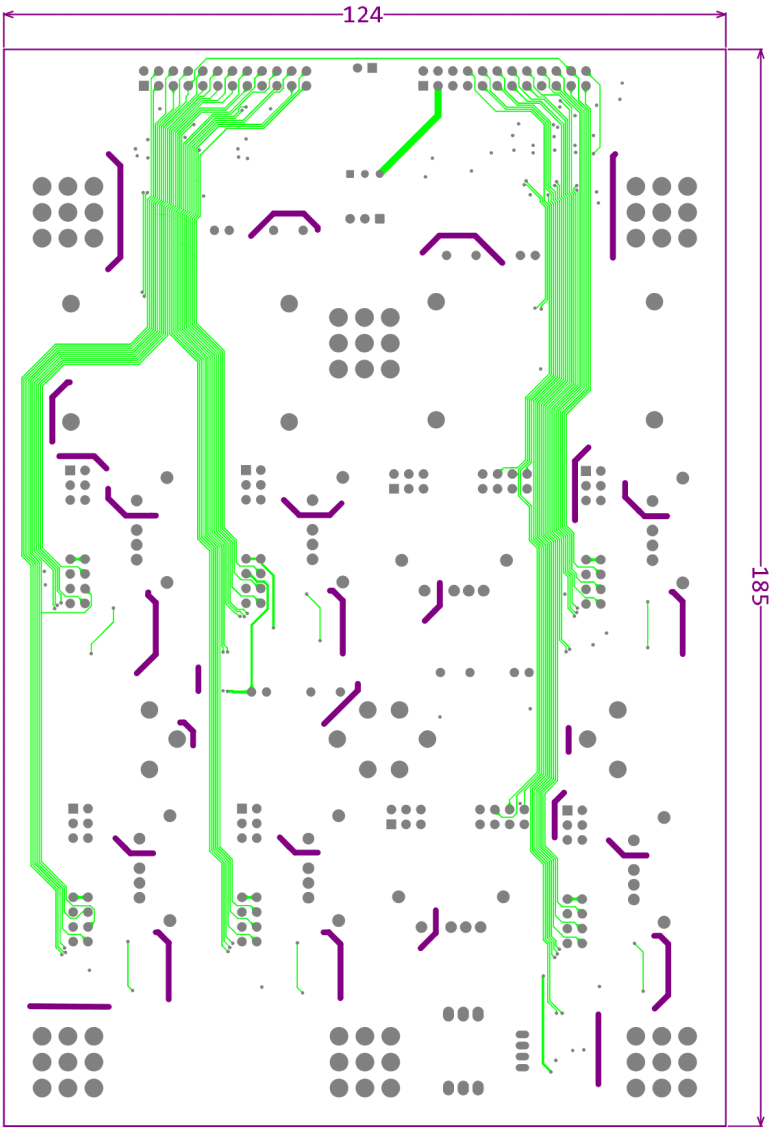

26
37

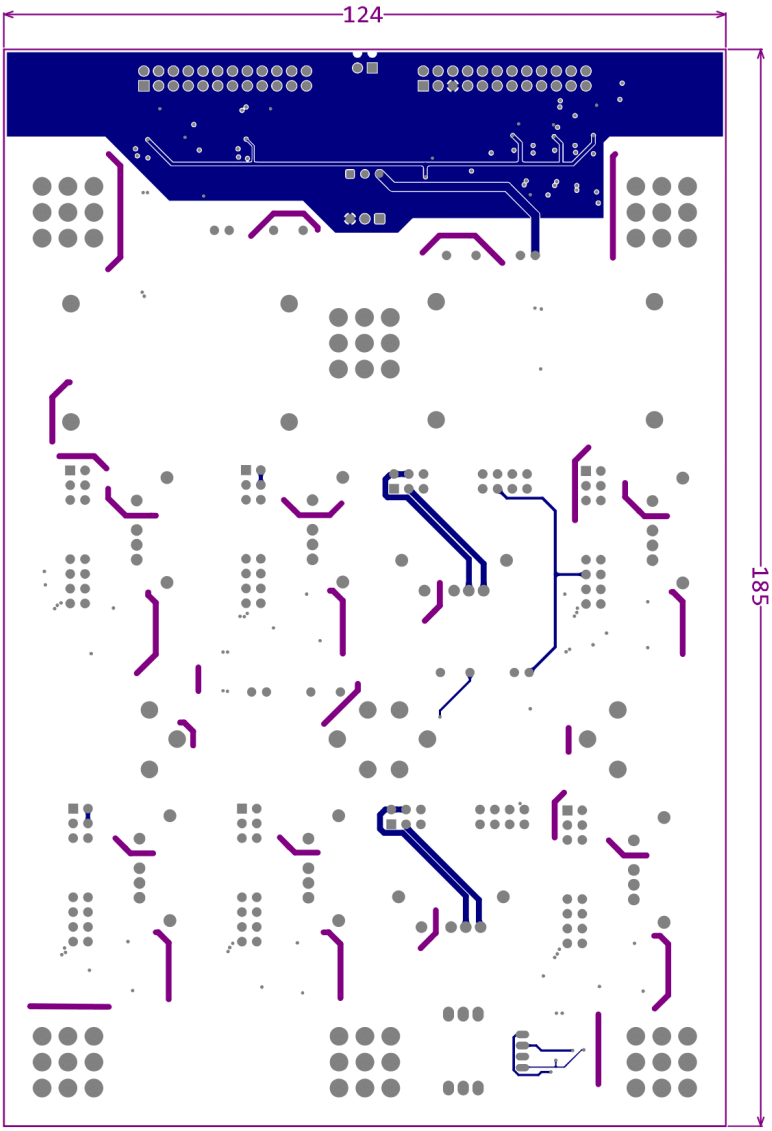

26
37

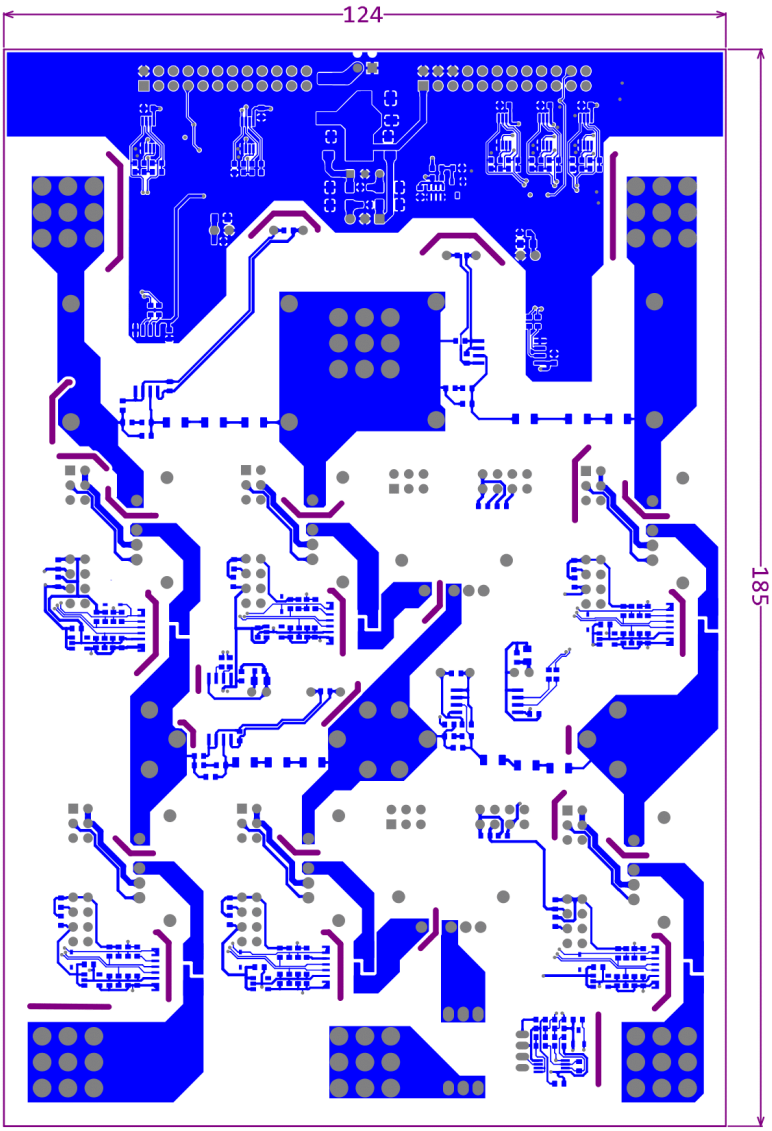

26
37

Appendix F - Main converter PCB

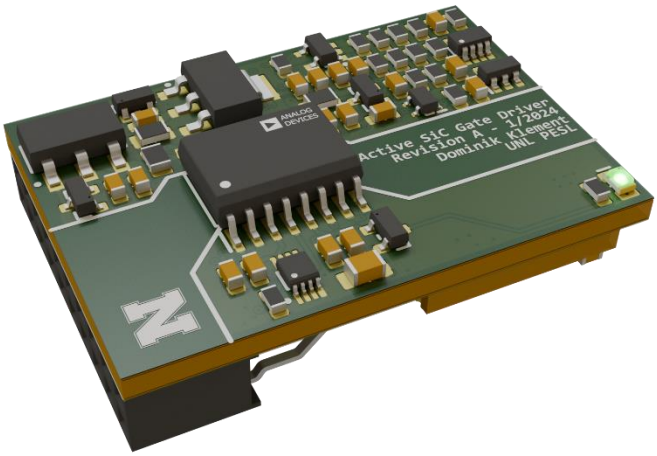


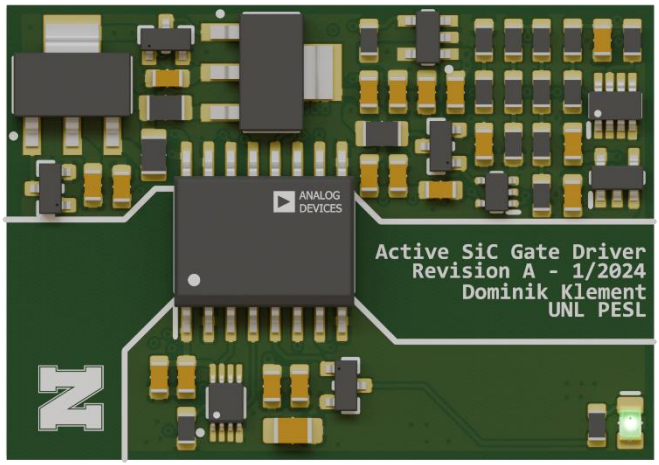

124
185

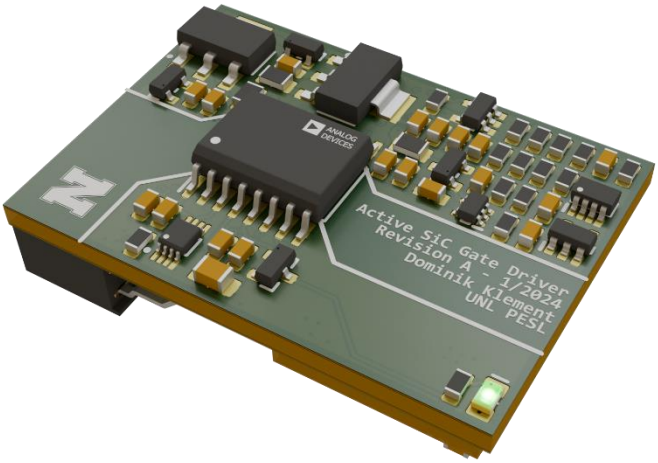

124
185


124
185

Appendix G - Active gate driver visualization







Appendix H - Main converter visualization