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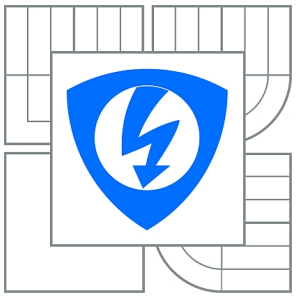

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FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

DEPARTMENT OF POWER ELECTRICAL AND ELECTRONIC ENGINEERING

FIELD PROGRAMMABLE GATE ARRAYS USAGE IN INDUSTRIAL AUTOMATION SYSTEMS

UŽITÍ PROGRAMOVATELNÝCH HRADLOVÝCH POLÍ V SYSTÉMECH PRŮMYSLOVÉ AUTOMATIZACE

DIZERTAČNÍ PRÁCE

DOCTORAL THESIS

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Abstract

This doctoral thesis deals with the usage of Field Programmable Gate Arrays (FPGAs) in a diagnosis of power inverters which use the IGBTs transistors as switching devices. It is focused on the IGBT gate drives and their structures. As long as the transient phenomena and other quantities such as I_G, V_{GE}, V_{CE} shows the IGBT degradation during the switching process (turn-on, turn-off), a new IGBT gate driver architecture is proposed for measuring and monitoring these quantities. Quick measurements and monitoring during the IGBT switching process require high sampling frequencies. Therefore, high speed parallel ADC converters ($> 50\,\mathrm{MSPS}$) are proposed.

The thesis is focused on the FPGA design (hardware, software). A new FPGA board is designed for desired functions implementation such as IGBT driving using multiple stages, IGBT monitoring and diagnosis, and interfacing to inverter controller.

Keywords

Fault detection and diagnosis (FDD), Fault Tolerant Control (FTC), Field Programmable Gate Arrays (FPGA), Insulated-Gate Bipolar Transistor (IGBT), gate drive, ADC, monitoring, PC board, redundancy, Very High Speed Integrated Circuit Hardware Description Language(VHDL), Verilog, Fast Fourier Transform (FFT), DDR2SDRAM, Industrial automation.

Abstrakt

Tato disertační práce se zabývá využitím programovatelných hradlových polí (FPGA) v diagnostice měničů, využívajících spínaných IGBT tranzistorů. Je zaměřena na budiče těchto výkonových tranzistorů a jejich struktury. Přechodné jevy veličin, jako jsou I_G, V_{GE}, V_{CE} během procesu přepínání (zapnutí, vypnutí), mohou poukazovat na degradaci IGBT. Pro měření a monitorování těchto veličin byla navržena nová architektura budiče IGBT. Rychlé měření a monitorování během přepínacího děje vyžaduje vysokou vzorkovací frekvenci. Proto jsou navrhovány paralelní vysokorychlostní AD převodníky ($> 50\,\mathrm{MSPS}$).

Práce je zaměřena převážně na návrh zařízení s FPGA včetně hardware a software. Byla navržena nová deska plošných spojů s FPGA, která plní požadované funkce, jako je řízení IGBT pomocí vícenásobných paralelních koncových stupňů, monitorování a diagnostiku, a propojení s řídicí jednotkou měniče.

Klíčová slova

Detekce poruch a diagnostika (FDD), Řízení odolné vůči poruchám (FTC), Programovatelné hradlové pole (FPGA), Tranzistor IGBT, Budič, Analogově-digitální převodník, monitoring, PC deska, redundance, Jazyk VHDL, Verilog, Rychlá Fourierova transformace (FFT), DDR2-SDRAM, Průmyslová automatizace.

DECLARATION

I declare that I have elaborated my doctoral thesis on the theme of Field Programmable Gate Arrays Usage in Industrial Automation Systems, under the supervision of doc. Ing. Bohumil Klíma, Ph.D. and with the use of technical literature and other sources of information which are all quoted in the thesis and detailed in the list of literature at the end of the thesis.

_____

Ziad Nouman
Brno, 2015

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First of all, I would like to express my gratitude to my supervisor doc. Ing. Bohumil Klíma, Ph.D. for creating the preconditions for the work guiding me through the process. His comments and support especially during the finalizing period of the work are greatly appreciated. I also wish to thank my colleagues in the department of Power Electrical and Electronic Engineering at Brno University of Technology for their comments, ideas, and suggestions during the work. I would like to express my thanks to Tishreen University in Syria for help and support.

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Abbreviations

Mathematical Terminology

E_{on}	Loss of Energy
f_{CCLK}	Configuration Clock Frequency
f_{CLK}	Clock Frequency
F_{RSELF}	Self Resonant Frequency
F_{RIS}	Effective Resonant Frequency
f_{sw}	Switching Frequency
G_{FE}	Forward Transconductance
I_C	Collector Current
I_L	Load Current
L_G	Stray Inductance in the Gate Path
L_{via}	Via Inductance
L_{trace}	Trace Inductance
L_{mount}	Mounting Parasitic Inductance
L_{self}	Self Inductance
L_{IS}	Effective Parasitic Inductance
L_C	Main Collector Terminal Connection Parasitic Inductance
L_{SC}	Sensor Collector Terminal Connection Parasitic Inductance
L_E	Main Emitter Terminal Connection Parasitic Inductance
L_e	Kelvin Emitter Terminal Connection Parasitic Inductance
L_g	Gate Terminal Connection Parasitic Inductance
N_{cc}	Clock Cycles Number
R_g	Internal Gate Resistor
R_{on}	On State Resistance
R_{thJC}	Thermal Resistance of Junction to Case
T_{CH}	Case-Heat-Sink Temperature
t_{fv}	Voltage Fall Time
$TMCCKTOL$	Configuration Clock Tolerance
T_{SPITCO}	SPI clock to out
T_{SPIDDC}	FPGA data setup time
T_{stg}	Storage Temperature
$T_{vj,op}$	Junction Temperature

$t_{sc,MAX}$	Maximum Short Circuit Time
$t_{d(on)}$	Turn on Delay Time
t_{on}	Turn on Time
t_p	Time Period
t_{ri}	Current Rise Time
U_{DC}	DC-Bus Voltage
V_G	Gate Drive Voltage
V_{CE}	Collector-Emitter Voltage
V_{GE}	Gate-Emitter Voltage
V_{th}	Threshold Voltage
$V_{CE(sat)}$	On-State Voltage Drop
Z_{thJC}	Transient Thermal Impedance

Miscellaneous Abbreviations

AAF	Anti-Aliasing Filter
AC	Alternative Current
ADC	Analog Digital Converter
AFTC	Active Fault-Tolerant Control
AGD	Active Gate Drive
ASIC	Application Specific Integrated Circuit
BGA	Ball Grid Array
BJT	Bipolar Junction Transistor
BLVDS	Bus Low Differential Signaling
BUFG	Global Clock Buffer
BUFH	Horizontal Clock Buffer
BUFIO	Input/Output Buffer
BUFMR	Multi-region Clock Buffers
BUFR	Regional clock Buffers
C	Collector Terminal
C_S	Collector Sensor Terminal
CCLs	CMOS configuration latches
CFGBVS	Configuration Bank Voltage Select
CLB	Configurable Logic Blocks
CPLDs	Complex Programmable Logic Devices
CMT	Clock Management Tile
DAC	Digital Analog Converter
DC	Direct Current
DCI	Digitally Controlled Impedance
DDR2 SDRAM	double data rate synchronous dynamic random-access memory

DFT	Discrete Fourier Transform
DIN	Data In
DIP	Dual In-line Package
DOUT	Data Out
DRP	Dynamic Reconfiguration Port
DSP	Digital Signal Processing
E	Emitter Terminal
e	Kelvin Emitter Terminal
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMCCLK	External Master Configuration Clock
EMI	Electro-Magnetic Interference
EPROM	Erasable Programmable Read Only Memory
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FDD	Fault Detection and Diagnosis
FDI	Fault Detection and Isolation
FFT	Fast Fourier Transform
FPGA	Field-Programmable Gate Array
FPLA	Field-Programmable Logic Array
FTC	Fault-Tolerant Control
FUL	Fault Under Load
G	Gate Terminal
GPIO	General Purpose Input/Output
HDL	Hardware Description Language
HP	High-Performance
HR	High-Range
HROW	Horizontal Clock Row
HSTL	High-Speed Transceiver Logic
HSF	Hard Switch Fault
IDELAY	Programmable Input Delay
IGBT	Insulated Gate Bipolar Transistor
I/O	Input/Output
INIT_B	Initialization Bar
JTAG	Joint Test Action Group
LSB	Least Significant Bit
LUT	Look Up Table
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor Transistor Logic
LVDS	Low Voltage Differential Signaling
MC	Memory Controller
MF	Multi-Functional
MIG	Memory Interface Generator
MMCM	Mixed-Mode Clock Manager

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSI	Master-Output, Slave-Input
MPGAs	Mask-Programmable Gate Arrays
MRCC	Multi-Region Clock Capable
MSPS	Mega Sample Per Second
NA	Not Available
NC	No Connected
NPT	Non-Punch-Through
NU	Not Used
ODELAY	Programmable Output Delay
ODT	On-Die Termination
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PDS	Power Distribution System
PFTC	Passive Fault-Tolerant Control
PHY	Physical Layer
PI	Proportional Integral Controller
PLL	Phase-Locked Loop
PPDS	Point-to-Point Differential Signaling)
PROGRAM_B	Program Bar
PROM	Programmable Read Only Memory
PT	Punch-Through
PTH	Plated Through Hole
PUDC_B	Pull-Up During Configuration Bar
RCCM	RC Component Model
RSDS	Reduced Swing Differential Signaling
RVM	Relevance Vector Machine
SAFST	Shorted Anode Field Stop Trench
SC	Short Circuit
SCR	Silicon Controlled Rectifier
SCS	Stages Control Signals
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SRCC	Single-Region Clock-Capable
SSN	Simultaneous Switching Noise
SSTL	Stub-Series Terminated Logic
TCK	Test Clock
TDI	Test Data Input
TDO	Test Data Output
TIM	Thermal Interface Material
TMS	Test Mode Select
UART	Universal Asynchronous Receiver/Transmitter

UCF	User Constraints File
USB	Universal Serial Bus
VCP	Virtual COM Port
VFD	Variable Frequency Drive
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VLD	Variation of lateral doping
VR	Voltage Regulator
VSI	Voltage Source Inverter
VTF	Verilog Test Fixture
XADC	Xilinx Analog to Digital Converter
XDTs	Xilinx Design Tools

Chapter 1

Introduction

Today's, industrial automation systems are highly complex networks of embedded systems consisting of many sensors, drives, controllers, and intelligent I/O devices. Recently, Field Programmable Gate Arrays (FPGAs) are used throughout industrial automation systems to add intelligence, flexibility, and high precision control. Their applications include motion control, machine to machine communications, motor drives, diagnosis and fault-tolerant control, smart energy and smart grid, big data analytic, etc.

Generally, when the FPGAs are used in motor drives, they implement complex control algorithms and modulation switching. Additionally, they can provide functions for fault protection of motor such open circuit and short circuit. In other words, the FPGAs usage is limited to motor control and modulation switching, but they are not used to detect the problems of inverter components during the switching process. For example, the monitoring of the IGBT switching process (turn-on, turn-off) in a power inverter may lead to predict and diagnose the faults before the complete degradation occurrence in the drive system.

Mostly, no methods exist for continuous monitoring of inverter switching transistor condition or other parts of power inverter such as DC link capacitance, leakage resistance, or terminals contact resistances etc. Diagnostic methods based on continuous condition monitoring, which were developed for mechanical vibration monitoring or for many other fields - for example ball bearing condition monitoring or partial discharges in motor winding, do not exist for IGBT transistors proper operation. The quality of switching process is possible to observe only on transients, when the transistor switches on or off. Based on the study presented in chapter 2, it could be noted that several factors affect the switching transient in the transistor: transistor switching speed, gate resistance, gate current, gate voltage, DC link capacitance, snubbers capacitance, etc. Among these quantities, which can be measured, are collector-emitter voltage V_{CE}, gate-emitter voltage V_{GE} and gate current I_G. These quantities are only measurable in the IGBT gate driver in the inverter. Based on the quantities measurements and their quantitative evaluation, the degree of degradation in the power components (IGBT transistors, diodes, capacitors, etc.) may be predicted, where the characteristic of these components change during the degradation. Therefore, the diagnostic methods, which depend on measuring and monitoring the IGBT

quantities during the switching process in the gate drive circuits, should lead to predict the critical degree of the components degradation. Accordingly, the maintenance can be scheduled to avoid the failure of the components during the operation.

As long as the IGBT gate driver is used to measure and monitor the required quantities for the diagnosis, a new hardware for the gate driver is required. In addition to its basic functions (turn-on, turn-off), the gate driver should be able to perform measurements, recording, and mathematical analysis during the IGBT switching process. The digital signal processing for the analysis and recording is required. Generally, Fast Fourier Transform (FFT) or Wavelet transform are used for this purpose. Therefore, the implementation of programmable devices, which are placed directly on the gate driver, are required. The programmable devices may be Field Programmable Gate Arrays (FPGAs) or microprocessors.

1.1 Motivation and Objectives

The idea is to integrate the diagnostic functions into the IGBT gate driver circuits. These functions should allow analysis of the required quantities in the IGBT transistor and its gate driver. The purpose is to measure and monitor these signals during the IGBT switching process. The quantitative evaluation of the measured parameters, which are recorded and analyzed using programmable devices, can indicate the degree of the degradation. As a result, the IGBT failure can be predicted and it would be able to plan the targeted service (replacement of specific IGBT, driver, capacitor).

The aim is to design a hardware of the IGBT gate driver, which would allow achieving the previous properties.
The structure of the proposed IGBT gate driver can be summarized as follows:

1. Multiple gate stages outputs for realization of variable gate resistance by sequential switching. It allows realization of liner charging of gate capacitance delayed sequential switching signals are generated in the FPGA and are programmed in HDL language.

2. Programmable devices (FPGAs) for recording and analysis of the digital signals.

3. Multiple power supplies for IGBT gate stages and for FPGA feeding.

4. Driver interface to inverter control system with data exchange capability except standard PWM signal. The insulated SPI interface is used for this purpose.

1.2 Structure of the Thesis

The thesis is structured as follows:

1. *Introduction*: This chapter includes the usage of Field Programmable Gate Arrays (FPGAs) in the applications of industrial automation. It also describes the capability of their usage in the control and diagnosis of inverter faults during the switching

process. Additionally, this chapter describes the motivation and the objective of the thesis.

2. *Background and State of the Art*: This chapter is dedicated to IGBT transistor description and its applications. This chapter also reviews the current state of the art of the IGBT transistor faults, fault detection and diagnosis and the fault-tolerant control.

3. *Proposed IGBT Gate Drive Architecture*: This chapter is concerned with the IGBT Gate driver design. A new IGBT gate driver architecture with integrated diagnostic functions is provided.

4. *FPGA Board Design for IGBT Control and Diagnosis*: This chapter focuses on the FPGA board design and the required components for implementation the diagnostic functions and the IGBT switching process control.

5. *Stages Control Signals Generator Design*: This chapter deals with the design steps of stages control signals generator which provides the signals that control the IGBT gate driver stages during the IGBT turn-on/turn-off.

6. *Conclusions*: This chapter summarizes the the results of the dissertation. This chapter also discuses the future work which can be the continuous of FPGA usage in the applications of the diagnosis and the fault-tolerant control.

7. *Appendix A*: Includes the connections between the conectors pins (J11, J10,J20) and The FPGA device.

8. *Appendix B*: Provides the User Constraint File (UCF) of the FPGA device for interfacing to the external devices.

9. *Appendix C*: Is the PCB layout of the FPGA board design.

10. *Appendix C*: The Verilog Top Level (VTL) and Verilog Test Fixture (VTF) designed for the simulation and experimental results.

Chapter 2

Background and State of the Art

The drive system can be divided into:

- Power semiconductor devices.
- Gate drive circuit.
- Control circuits.
- Sensors.
- Communication interfaces.
- Software.

A general motor control system can be illustrated as follows:

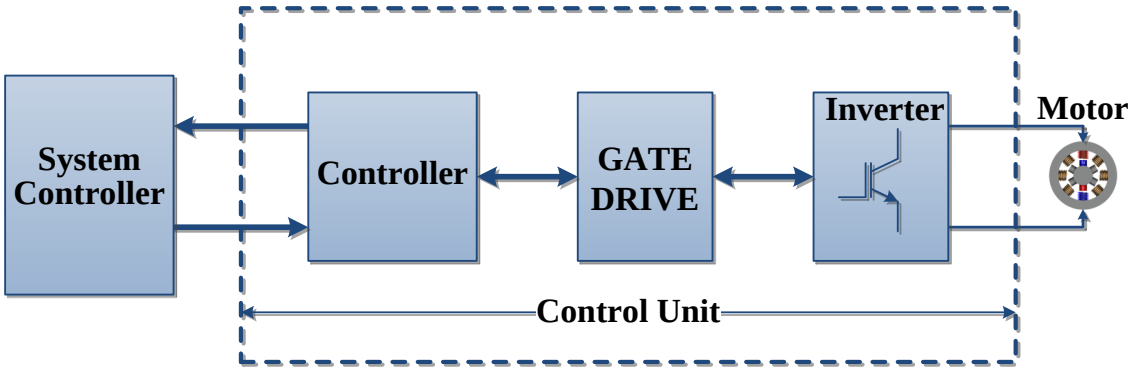


Figure 2.1: General motor control system

As can be seen from Figure 2.1, the control unit, which is composed of inverter, gate

driver, and controller, is the key of control system and if this part and all its functions are understood, all the faults and their causes can be diagnosed.

When the drive system works for a long time, it could go out of the service due to the fault occurrence. Therefore, the faults must be predicted. The fault may occur in the control unit (power semiconductor, gate driver, controller) or inside the electrical machine. Sometimes, the fault occurs in the area between the control unit and the electrical machine. Therefore, the system must be protected to prevent its failure and damage during the operation.

The scope of this chapter is focused on the detection of optimization operating state of the drive system. It presents diagnosis methods which are designed to predict drive system faults, where the robust and reliability are usually increased using the fault detection and fault tolerant solutions.

2.1 IGBT Basics

Nowadays, the full controlled power semiconductors (IGBTs and MOSFETs) are widely used in most power inverters of drive systems. The advantage of MOSFET is that it requires a little current to turn on, but its disadvantage is that it requires a high voltage to turn on. IGBT is developed to combine a high efficiency and a fast switching. IGBT is a cross between the bipolar junction transistor (BJT) and the MOSFET transistor, and it has the characteristics of the BJT (collector-emitter) and the drive characteristics of the MOSFET. Hence, the focus would be placed on IGBT power switches.

2.1.1 Basic Structure and Operation

There are several structures for the IGBT transistors. Figure 2.2 illustrates one of these structures. The N^+ layer at the top is the emitter, the P^+ layer at the bottom forms the collector [44], with n^+ buffer layer the IGBT is called a Punch-Through (PT) IGBT, the buffer layer improves the performance of the device (low on-state voltage drop, fast in switching). The IGBT without buffer layer is called a Non-Punch-Through (NPT) IGBT. The NPT IGBT improved the switching speed but it is unsuitable for the high power application due to its high $V_{ce(sat)}$. The equivalent circuit can be to simplify the structure, see drawn Figure 2.3a.

The equivalent circuit contains MOSFET, NPN, JFET and PNP transistors. Figure 2.3b shows the IGBT circuit symbol, which has three terminals called collector (C), emitter (E), and gate (G).

Improved characteristics of IGBTs have resulted in a higher switching speed and lower switching power losses. New generations of IGBTs have adopted the trench technology to reduce the losses of IGBTs [65]. The gate structure of IGBTs, which is dependent on the trench technologies differs from the conventional structure illustrated in Figure 2.2, where the gate electrode is built in deep narrow trench. The structure of trench IGBT is shown in Figure 2.4, where the trench gate structure reduces the on state voltage drop $V_{CE(sat)}$

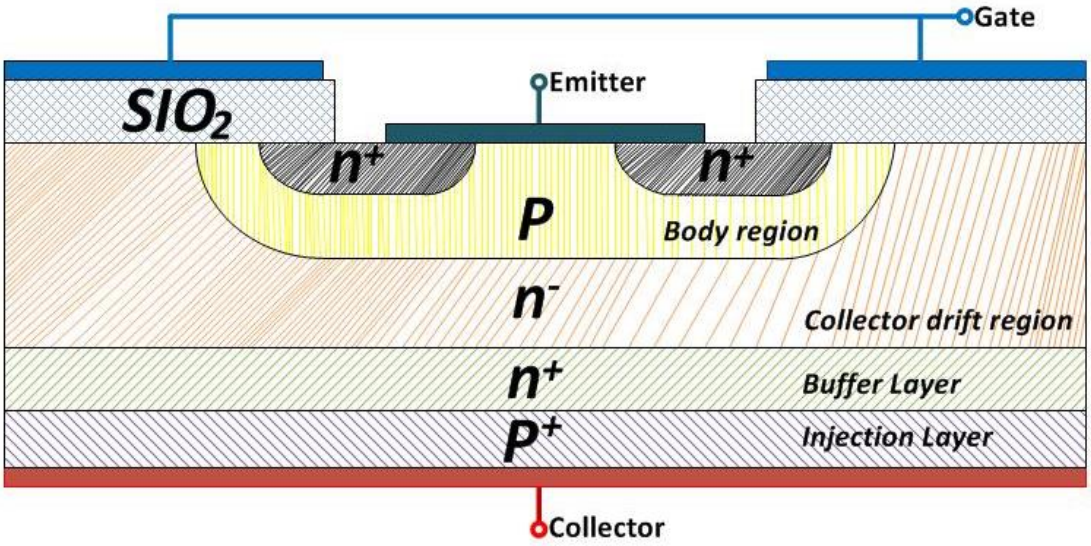
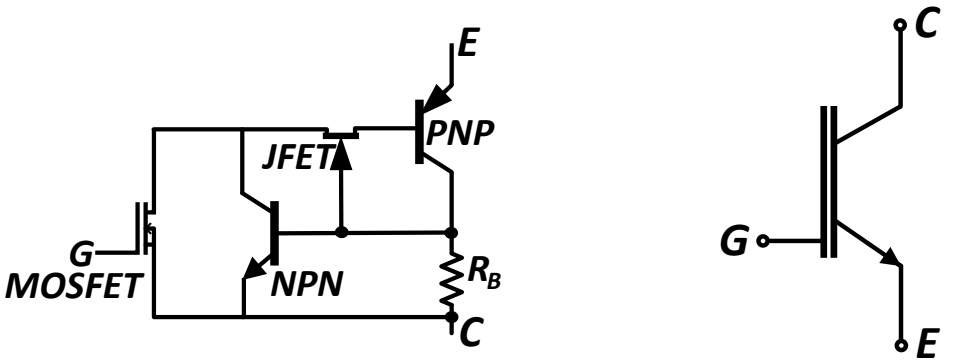


Figure 2.2: Cross Section of IGBT Structure [44].



(a) Equivalent circuit. (b) Circuit symbol of an IGBT.

Figure 2.3: Equivalent circuit of an IGBT structure and its symbol [44].

and the field stop layer reduces the turn off losses [116].

The trench concept with variation of lateral doping (VLD) technology have been introduced for 4.5 kV/1.2 kA and 6.5 kV/750 A IGBT modules [25] [6], this new generation of IGBTs (IGBT3) reduced the complexity of inverter designs that use previous IGBT modules (IGBT2) or GTOs. As a result, lower system costs and better reliability.

IGBT is robust but it suffers failures because of the electrical and thermal stress. However, thanks to its advantages, IGBT became the main component in the power electronic applications (transport, energy conversion, manufacturing, mining and petrochemical) and it can be used for application up to 6.5 kV and 1.2 kA.

The power IGBT module is build up from parallel IGBT chips, T_1 through T_n and par-

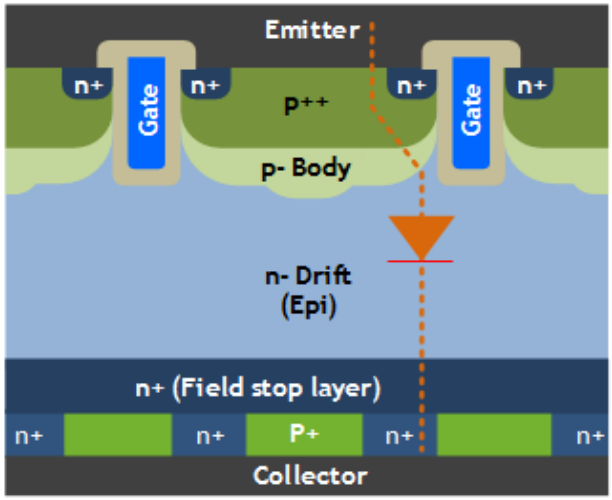
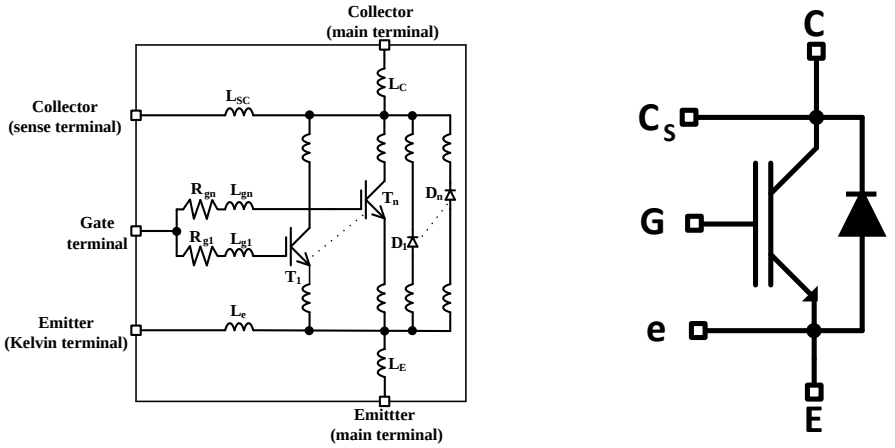


Figure 2.4: Cross section of FS SA T IGBT structure [116].



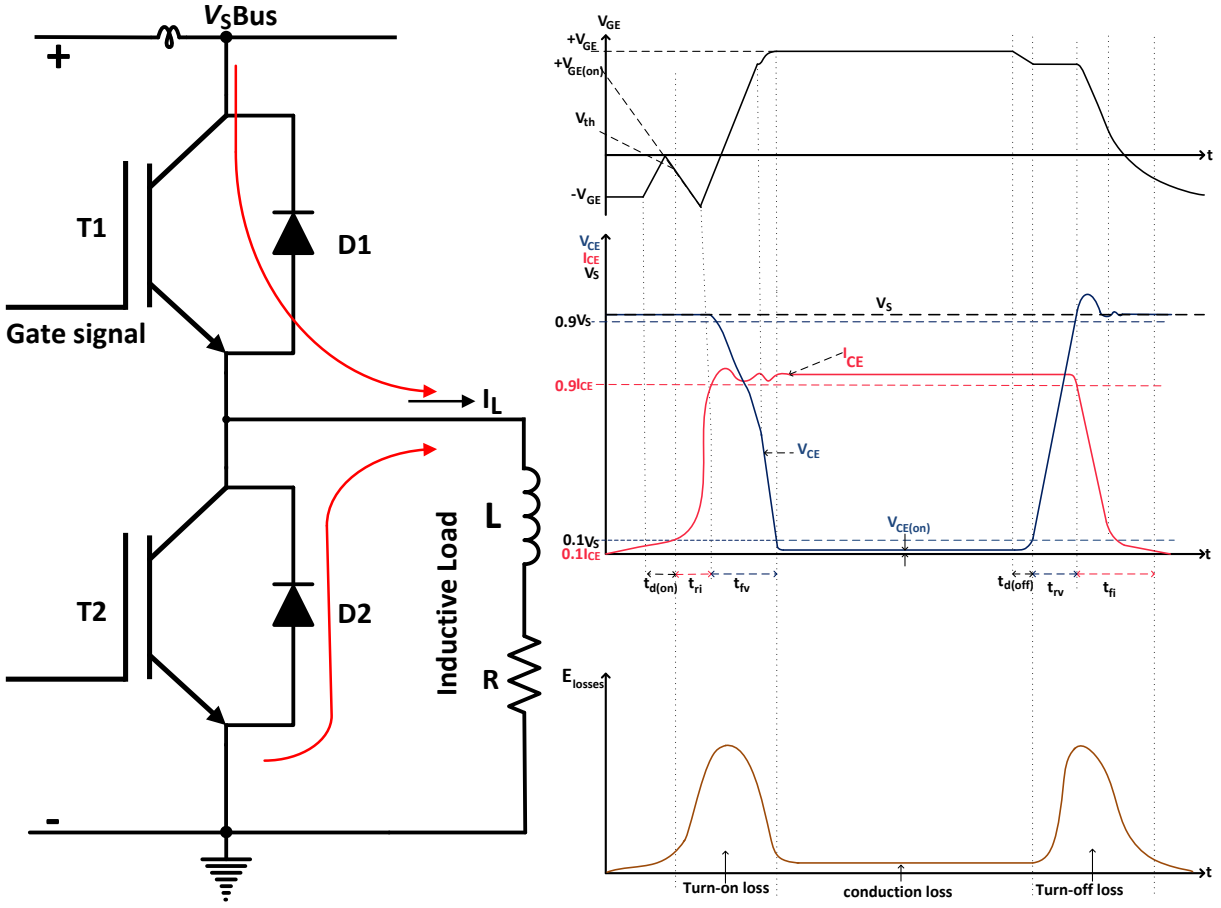
(a) Equivalent circuit of IGBT module. (b) Symbol of IGBT module.

Figure 2.5: Schematic of IGBT module with its symbol [14].

allel diode chips, D_1 through D_n, as shown in Figure 2.5a, where (L_C,L_{SC}, $L_{g1..gn}$,L_E) are the parasitic inductances applied to the wire connections [14]. R_{g1} and R_{gn} are the internal gate resisters. Due to these resistors, the oscillations between the parasitic capacitance of IGBT chips and the parasitic inductance of the internal gate wires are prevented. Figure 2.5b depicts the symbol of the IGBT module where it has five terminals. The external terminal e is called Kelvin emitter. Kelvin emitter is used for the IGBT gate driver. This feature improves the noise immunity during the IGBT switching operation. The collector sensor terminal C_{SC} is used for measurement.

2.1.2 Switching Characteristics of IGBT

IGBT transistor is a controlled device. Therefore, a voltage between the gate and emitter V_{GE} is applied to turn it on or off, this voltage is fed from a circuit called gate drive circuit. This circuit acts as an interface between logic signals of controller (FPGA) and the gate signals of IGBT. Figure 2.6a shows an IGBT half bridge inverter with an inductive load,



(a) IGBT half bridge converter.

(b) Turn on and turn off waves of IGBT (T1).

Figure 2.6: Switching characteristics of an IGBT (T_1) in half-bridge inverter with inductive load [11].

and Figure 2.6b illustrates the switching characteristics (turn-on and turn-off) wave-forms of one transistor T_1 with an inductive load without using snubbers. Suppose that the $\frac{L}{R}$ time constant of the load is greater than used IGBT switching frequency. Therefore, the load current I_L can be considered constant.

When a positive gate voltage is applied to the gate IGBT, the input capacitance between the gate and emitter C_{GE} charges during the turn-on delay time $t_{d(on)}$ to a voltage V_{GE} greater than the threshold voltage V_{th}, then the IGBT begins to turn on. The current and voltage waves as a function of time are shown in Figure 2.6. When $V_{GE} > V_{th}$ the load

current is transferred from the diode into the device and it increases to the steady on-state value during the rise time t_{ri}, where the current rise time t_{ri} is the time interval for the current to increase from $0.1\,I_L$ to $0.9\,I_L$.

As soon as the gate voltage V_{GE} reaches the value $V_{GE(on)}$, the collector-emitter voltage begins to fall until reaches the value $V_{CE(sat)}$ during the time t_{fv}, where the voltage fall time t_{fv} is the time needed for the voltage V_{CE} to decrease from $0.9\,V_s$ to $0.1\,V_s$.

2.1.3 IGBT Switching Losses

The loss of energy E_{on} during the turn-on of the IGBT can be written as the following:

$$E_{on} = \int_0^{t_{on}} V_{CE} \cdot i_{CE} \cdot dt \tag{2.1}$$

where t_{on} is the IGBT turn-on time. If the delay time is ignored, then the turn-on time equals $t_{ri} + t_{fv}$, and the loss of energy during the turn-on can be stated in the following equation form

$$E_{on} = \frac{V_s \cdot I_{CE}}{2} \cdot (t_{ri} + t_{fv}) = \frac{V_s \cdot I_{CE}}{2} \cdot t_{on}. \tag{2.2}$$

The average power dissipation $P_{loss(on)}$ is given by

$$P_{loss(on)} = E_{on} \cdot f_{sw} = \frac{V_s \cdot I_{CE}}{2} \cdot t_{on} \cdot f_{sw} \tag{2.3}$$

where f_{sw} is the switching frequency of the IGBT.

As shown in Figure 2.6b, the IGBT turn-off begins by removing the gate-emitter voltage, where the gate-emitter capacitance C_{GE} begins to discharge, the time interval needed for the capacitance to discharge to the value $V_{GE(on)}$ is called a turn-off delay time $t_{d(off)}$. When the V_{GE} reaches the value $V_{GE(on)}$, then the collector-emitter voltage V_{CE} begins to rise, whereas the collector-emitter current I_{CE} remains constant. The voltage V_{CE} increases during the time t_{rv} until the value equals V_s, and the collector-emitter current I_{CE} begins to decrease during the time t_{fi}. The voltage V_{GE} continues to decrease until it reaches the value less than the V_{th}, at this value of the V_{GE} the MOS channel in IGBT is turned off but the collector current is slowly decreasing because of the high minority carrier concentration stored in the n^- drift region. Since the voltage V_{CE} has reached the bus voltage V_S, with this current tail the loss of energy will be high and the power loss will increase with the frequency increasing.

The loss of energy E_{off} during the IGBT turn-off time can be written as follows

$$E_{off} = \int_0^{t_{off}} V_{CE} \cdot I_{CE} \cdot dt \tag{2.4}$$

suppose $t_{off} \cong t_{rv} + t_{fi}$, then Equation 2.4 can be written as the following

$$E_{off} = \frac{V_s \cdot I_{CE}}{2} \cdot (t_{rv} + t_{fi}) = \frac{V_s \cdot I_{CE}}{2} \cdot t_{off}. \tag{2.5}$$

The average power dissipation $P_{loss(off)}$ is given by

$$P_{loss(off)} = E_{off} \cdot f_{sw} = \frac{V_s \cdot I_{CE}}{2} \cdot t_{off} \cdot f_{sw}. \tag{2.6}$$

The total losses of energy $E_{SWlosses}$ during the IGBT turn on and turn off is the sum of Equation 2.2 and Equation 2.5

$$E_{SWlosses} = E_{on} + E_{off} \tag{2.7}$$

$$= \frac{V_s \cdot I_{CE}}{2} \cdot (t_{on} + t_{off}). \tag{2.8}$$

The total power dissipation $P_{SWlosses}$ during the switching is the sum of Equation 2.3 and Equation 2.6:

$$P_{SWlosses} = P_{loss(on)} + P_{loss(off)} \tag{2.9}$$

$$= \frac{V_s \cdot I_{CE} \cdot f_{sw}}{2} .(t_{on} + t_{off}). \tag{2.10}$$

2.1.4 IGBT Conduction Losses

Figure 2.6b illustrates the conduction losses during the on-state of IGBT, where these losses occur between the end of the turn-on time and the beginning of the turn-off time of the IGBT. The conduction energy losses $E_{loss(con)}$ can be deduced using Equation 2.11

$$E_{loss(con)} = \int_{t_{con}} V_{CE(sat)} \cdot I_C \cdot dt \tag{2.11}$$

where t_{con} is the interval between the end of the turn-on time and the beginning of the turn-off time, $V_{CE(sat)}$ is the voltage drop across the IGBT during the conduction, and I_C is the collector current that is equal the load current I_L. The losses during the off-state is negligible.

The total energy loss for IGBT E_{IGBT} is the sum of energy losses E_{on}, E_{off} and $E_{loss(con)}$

$$E_{IGBT} = E_{on} + E_{off} + E_{loss(con)}. \tag{2.12}$$

And the total power loss P_{IGBT} is the product of total energy loss E_{IGBT} and the switching frequency f_{sw}

$$P_{IGBT} = \{E_{on} + E_{off} + E_{loss(con)}\} \cdot f_{sw} = E_{IGBT} \cdot f_{sw}. \tag{2.13}$$

2.1.5 Free Wheeling Diode (FWD)

IGBT modules are sometimes composed of multiple IGBTs and freewheeling diodes which connect in anti-parallel with the IGBT, as shown in Figure 2.6a. The function of this diode is to handle the current of the inductive loads such as inductive motors or transformers. Therefore, the reverse recovery process of the diode will produce undesired stress on the IGBT during the operation. Therefore, the reverse recovery losses of the diode must be taken into account, because they will be rated to the switching losses of the IGBT. The switching and conduction waveforms of the diode (FWD) can be seen in Figure 2.7.

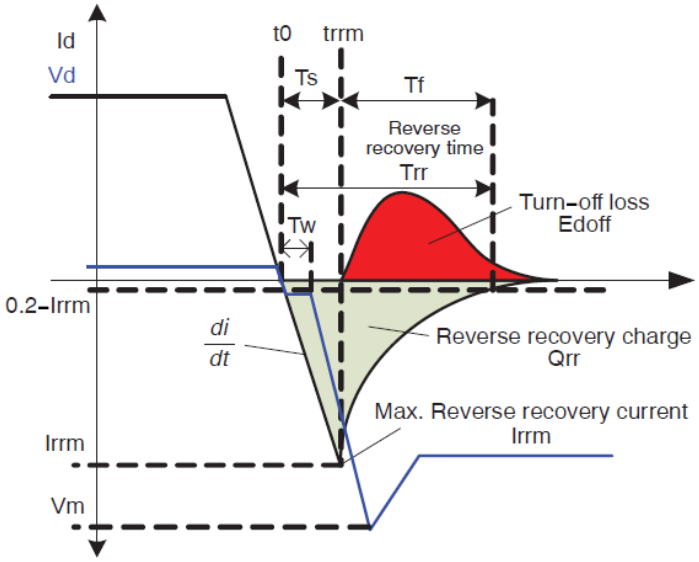


Figure 2.7: Switching waveforms of freewheeling diode in IGBT module [87].

When the diode conducts the current I_d, a voltage drop V_d will be across the diode. This condition will lead to turn-on and turn-off losses in the complementary switching. The conduction loss $P_{conduction}(t)$ can be calculated as follows

$$P_{conduction}(t) = i_d(t) \cdot v_d(t). \tag{2.14}$$

The peak reverse recovery current I_{rrm} and recovered charge Q_{rr}, as shown in Figure 2.7, depend on the initial forward current I_0 and the rate di/dt at which this current decreases. The turn-on loss E_{don} can be neglected, because the turn-on time is short and fast. Whereas the turn-off loss E_{doff} is determined by the reverse recovery charge of the diode [95]. The loss of energy E_{doff} can be calculated from Equation 2.15.

$$E_{doff} = \int_{t_w}^{t_f} V_m \cdot I_{rrm} \cdot dt. \tag{2.15}$$

Then the diode losses can be calculated as follows

$$P_{Dtotal} = (E_{conduction} + E_{doff}) \cdot f_{sw}. \tag{2.16}$$

2.1.6 Thermal Characteristics of IGBT Modules

The IGBT temperature must be maintained below the critical level to avoid the device destruction during its operation. Generally, a significant amount of power is produced and it must be dissipated to the surroundings to prevent the temperature from rising to a level at which the device performance is unsatisfactory. A heat is generally removed to the surroundings by connecting the IGBT to a cooling surface or a heat-sink.

When a thermal design is achieved for an IGBT module, temperatures must be taken into consideration. The temperatures include the storage temperature T_{stg}, the virtual junction temperature T_{vj}, the junction-case temperature T_{JC} and the case heat-sink temperature T_{CH}. The thermal behavior of an IGBT module at the steady state is specified by the thermal resistance, whereas the thermal impedance Z_{thJC} characterizes the IGBT thermal behavior at transient conditions. The thermal resistance of junction to case R_{thJC} and case to heat-sink R_{thCH} are specified by manufacturers in a datasheet, whereas the transient thermal impedance Z_{thJC} is specified as a function of the time [1]. Figure 2.8

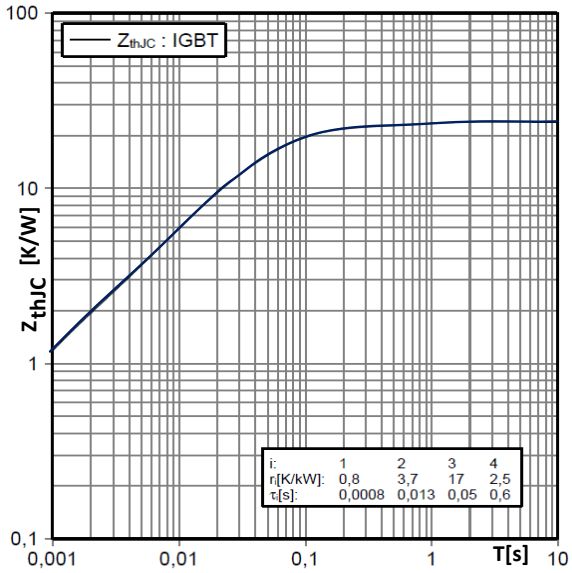


Figure 2.8: The transient thermal impedance Z_{thJC} as a function of the time $Z_{thJC} = f(t)$ [95].

depicts the transient thermal impedance Z_{thJC} as a function of the time t, and it includes the partial fraction coefficient used for calculating the values of the capacitances as the

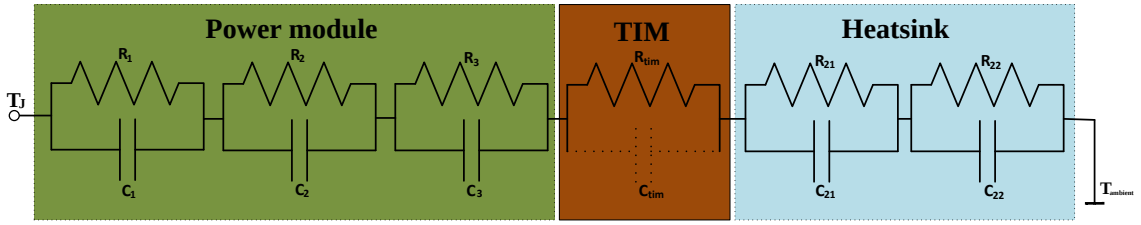


Figure 2.9: R/C Foster thermal model description [80].

following

$$C_i = \frac{\tau_i}{r_i} \tag{2.17}$$

where τ_i is the time constant, and r_i is the thermal component resistance.

Knowing the thermal parameters R_{th} and Z_{thJC} of the device and the dissipated losses during the operation allow calculating the junction temperature. When the junction temperature is calculated, it must stay between the minimum and maximum specified values of the operating junction temperature $T_{vj(op)}$ even in the case of hard conditions (overload,short circuit). There are various possibilities for measuring the device temperatures such as infrared cameras or using temperature sensors [13].
Every IGBT module has a thermal equivalent circuit which describes its thermal behavior during the switching operation. Figure 2.9 shows the thermal equivalent network using foster model, where the IGBT module is connected in series with the water cooled heat-sink via thermal interface material (TIM) [80].

The temperature changes can lead to mechanical stress which can result in a failure. Therefore, the thermal behavior analysis of IGBT modules mounted on heat-sinks was the issue of numerous articles. An RC component model (RCCM) is proposed in [117] for analysis the static and dynamic thermal behavior of the IGBT module mounted on water cooled heat-sink. It is important to have accurate thermal models for high power IGBT modules in order to predict its thermal behavior and calculate the junction temperature in the real time application [50].

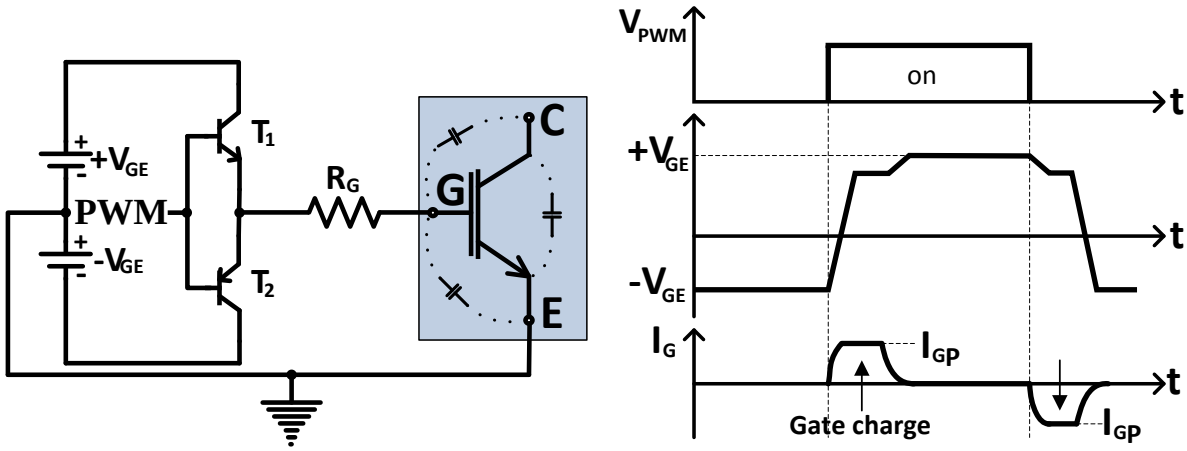
2.1.7 IGBT Gate Drive Circuit

As previously mentioned, the IGBT turn-on and turn-off are controlled by the gate voltage, and the speed of switching is determined by the gate current. The gate drive circuit feeds the IGBT gate signals. Therefore, it is considered as an interface between the logic signals generated from the controller and the signals of the IGBT gate.

Recently, the gate drive circuits have grown rapidly [74], to adapt with the development of switching devices which have special advantages, such as high currents, high voltages, high switching frequencies, and simple control [77] [8]. There are two types of gate drive

circuits, namely, voltage drive and current drive. The main function of the gate drive circuit is to convert the logic signals to power signals which control the IGBT switching. The gate drive circuit generates a positive voltage $+V_{GE}$ during the turn-on, and a negative voltage $-V_{GE}$ during the turn-off. Moreover, the gate drive circuit should control the time change rate di/dt of the IGBT collector current to avoid excessive Electro-Magnetic Interference (EMI), and it should control the time change rate dV_{CE}/dt of the IGBT collector-emitter voltage to avoid the IGBT latch up [53] [55].

A simple gate drive circuit for IGBT module is shown in Figure 2.10a. The NPN and



(a) IGBT gate drive circuit.

(b) Voltage and current waveforms of gate driver.

Figure 2.10: IGBT gate drive circuit diagram and waveforms of current and voltage [29].

PNP transistors are used to convert the logic signal to the power signal. When the logic signal is high, the T_1 is turned on and T_2 is turned off. Accordingly, the IGBT gate is pulled up to $+V_{GE}$, and the IGBT module is turned on. When the logic signal is low, the switch T_1 is turned off, and the switch T_2 is turned on. As a consequence, the IGBT gate is pulled down to $-V_{GE}$, and the IGBT is turned off. A reverse bias must be used to ensure that the IGBT stays in its off-state when dv/dt noise is present in the collector-emitter voltage. The low reverse bias voltage does not only reduce the drive circuit power, but also improve the switching off time. In addition, the low reverse bias voltage can speed up the switching on time and the delay switching off time. A series gate resistor is used to limit the current flow through the gate. Equation 2.18 is used to calculate the peak value of the current flowed to charge and discharge the gate during the IGBT switching.

$$I_{GP} = \frac{+V_{GE} + \left|-V_{GE}\right|}{R_G + R_g} \tag{2.18}$$

where R_G is the external gate resistor and R_g is the internal gate resistor.

A small gate resistor reduces the switching times and switching losses, but this may cause a high surge voltage. The value of the gate resistor has a significant impact on the turn-on speed of IGBTs, while it barely affects the turn off speed.

The average value of the drive current I_G can be calculated by Equation 2.19, using the gate charge characteristics shown in Figure 2.11

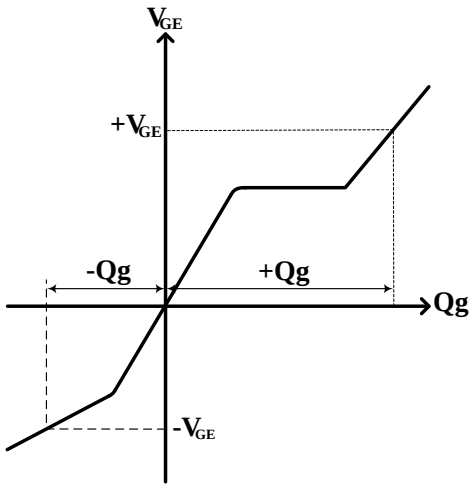


Figure 2.11: Waveform of IGBT gate charge characteristics [29].

$$+I_G = -I_G = f_{sw} \times \left(|+Q_g|+|-Q_g|\right) \tag{2.19}$$

where $+Q_g$ is the gate charge from 0 V to $+V_{GE}$ and $-Q_g$ is the gate charge from $-V_{GE}$ to 0 V. The gate drive power $P_{d(on)}$ required to turn on the IGBT is given by

$$P_{d(on)} = f_{sw} \times \left[\frac{1}{2} \times \left(|+Q_g|+|-Q_g|\right) \times \left(|+V_{GE}|+|-V_{GE}|\right)\right] \tag{2.20}$$

supposing that the gate drive power $P_{d(off)}$ required to turn off the IGBT is equal to the power $P_{d(on)}$, then the gate drive power P_d required to drive the IGBT switching is written as follows

$$P_d = P_{d(on)} + P_{d(off)} = f_{sw} \times \left[\left(|+Q_g|+|-Q_g|\right) \times \left(|+V_{GE}|+|-V_{GE}|\right)\right]. \tag{2.21}$$

Power circuit and gate drive circuit must be located as close as possible to the gate emitter control terminals of the IGBT module to minimize the stray inductance L_G in the gate path, which increases the switching losses. For high power applications, opto-couplers are used to avoid coupling of noise between the power circuits and the control circuits.

2.2 Present State in Inverter Diagnosis

The components of a drive system depend on their function and the place of use. Therefore, the faults and their causes may differ from system to another. The two components most prone to failure in the drive system are electrolytic filtering capacitors [51] [15] and power

devices, but 38 % of faults in the drive systems occur due to the failure of power devices during the switching operation [57] [58].
This section deals with the IGBT fault diagnosis in power inverter, where the IGBT is taken as a working part or a failed part.

The IGBT transistor is a controlled device, where the gate drive circuit controls the IGBT switching. The literature includes a number of articles describing the fault diagnosis for IGBT transistor. The IGBT failure during the switching operation can lead to the failure of entire drive system. Therefore, it is important to protect the IGBT devices against the faults. The IGBT faults can occur due to external or internal causes. The external causes are environmental influences such as humidity, dust, electromagnetic radiation, and high temperature. The internal causes can be classified into open circuit faults and short circuit faults. In addition, IGBT gate driver faults can lead to the IGBT device failure.

The causes of failure in the drive system have been briefly discussed in [2]. This paper presented the fault causes in the variable frequency drives. Based on the results of failure analysis, the causes of the failure were electrical and non-electrical causes, but the most causes are non-electrical.

The IGBT open circuit faults, which are defined as electrical causes, may be caused by the lifting of bonding wires [4] [60], or by the gate driver failure [82] [75]. The open circuit fault is not considered a fatal fault, but it can lead to another fault in healthy parts. Therefore, it is necessary to get rid of these faults to protect the system from the complete failure. Several detection methods for open circuit faults have been developed. An open circuit fault diagnostic technique in IGBTs for the AC to DC converters has been achieved in [40]. Since the current value in the faulty leg will change during the open switch fault in the PWM rectifier, the absolute normalized DC current method is proposed. This fault detection method improved the reliability of the drive system, where any false alarm will be avoided. The fault detection is achieved during one cycle of the current waveform. The open circuit fault diagnostic technique presented in [66] is based on the line to line voltage measurement in voltage source inverters (VSI) which uses IGBT switches. This measured voltage value is combined with the gate driver signals using a simple circuit. This circuit is composed of some resistors, comparators, and logic gates "AND". However, this study is uncompleted, because it does not take into consideration the possibility of freewheeling diode fault and it supposes that this diode is always healthy during the IGBT open circuit fault. The same problematic is discussed in [97], where the proposed open circuit faults diagnosis method is achieved for multiple IGBTs faults in VSI fed an induction motor. This technique uses the slope method which was modified based on the proposed slope method in [76]. The algorithm of this modified method is achieved by the analysis of the current space vector trajectory diameter to detect and locate the fault occurrence in two IGBTs simultaneously. This method has some defects such as long detection times. In addition, this technique faces problems under the light loads.

The IGBT fault diagnosis based on the Park's vector method was achieved in [62]. A new diagnostic method is suggested in [28]. This technique can detect and locate a multiple open circuit fault in the VSI. The algorithm of this method is achieved using the combination of the current Park's vector phase and the currents polarity. Nevertheless, all

the methods, which use the Park's vector transformation in their algorithms, are complex and they require more efforts to achieve.

The short-circuit (SC) is considered the usual fault mode of semiconductors, because the short-circuit faults are very destructive. Therefore, the protection and diagnosis system requires special measures to turn off the drive system immediately.

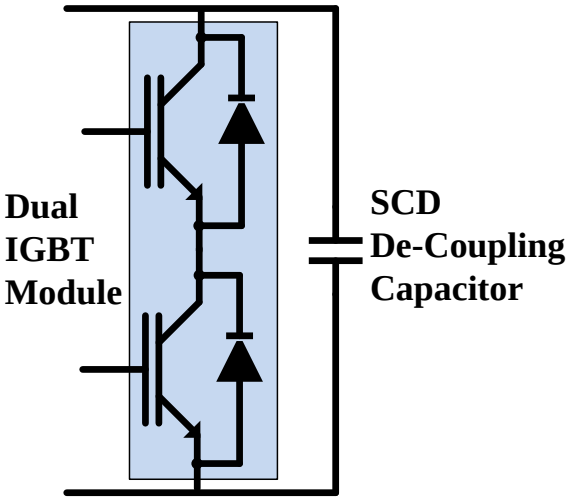
The short circuit faults are based on a variety of conditions which differ from drive system to another. The IGBT SC fault can happen, if two transistors in the same inverter leg are turned on simultaneously. The driver circuit malfunction can lead to this fault [58].

The SC fault diagnosis is difficult to achieve because this event has a short time. During the SC fault, the current increases quickly, and it results in the destruction of the IGBT. Therefore, it is important to understand the IGBT behavior during the SC faults to design the suitable protection circuits that turn off the IGBT safely. Since the SC event is very fast, few mathematical algorithms are capable to record it. Therefore, the SC detection and protection are achieved by hardware circuits. Thus, most SC detection and protection for IGBTs are based on the gate driver design mechanism. The IGBTs SC withstand time, which can be in the range of 6 μs to 10 μs, is dependent on their type and structure. If the protection circuit failed to turn off the IGBT during the withstand time, the IGBT will be destroyed. The IGBT SC destruction modes may happen during the following periods:

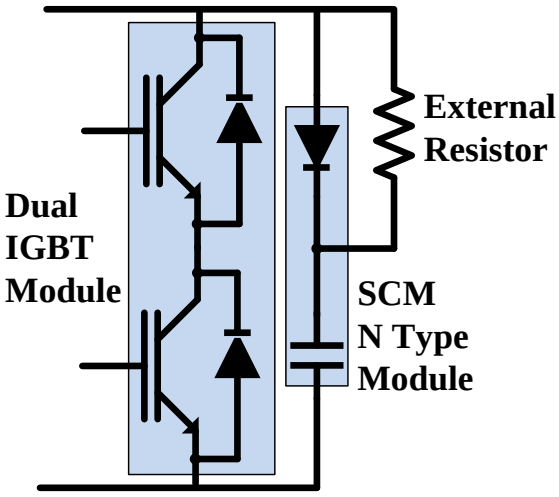
1. Destruction during the IGBT turn-on due to a current spike.
2. Destruction during the IGBT turn-off due to a voltage spike.
3. Destruction after the IGBT conduction due to an abnormal current.
4. Destruction after the IGBT turn-off due to a thermal runaway.

The voltage and current spikes on the IGBT can be reduced using a resistor capacitor (RC) damping network and a resistor-capacitor-diode (RCD) turn-off snubber. In addition, these circuits reduce the EMI by damping the voltage and current ringing. They also improve the reliability and the robustness against the SC conditions, but they increase the cost, size and losses in the drive system [10]. However, the efficiency does not increase. Moreover, the snubber circuits increase the commutation time. Accordingly, the dead time between the switching devices in the inverter has to be increased. The snubbers circuits used in IGBT applications depend on the power level, switching frequency, and circuit layout [89]. The snubber voltage will be at least equal to the maximum DC-bus voltage.

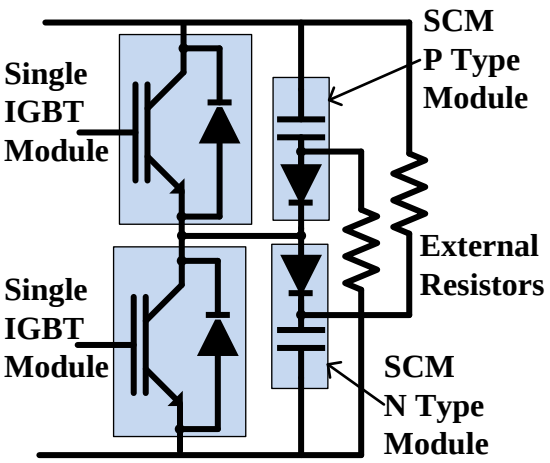
Figure 2.12 illustrates the snubbers circuits and their connections to the half bridge inverter. The C snubber circuit, shown in Figure 2.12a, is the simplest circuit used in medium current applications where it provides a low inductance path during the switching operation. Therefore, it reduces the transients. In high current applications, the C snubber produces a ripple current that can result in a capacitor failure. The RCD snubber, shown in Figure 2.12b, is used in medium and high current applications. In the higher current applications, the P type and N type SCM snubbers, illustrated in Figure 2.12c, may be used to protect the IGBT module against the over-voltage. This type of snubbers is suitable for



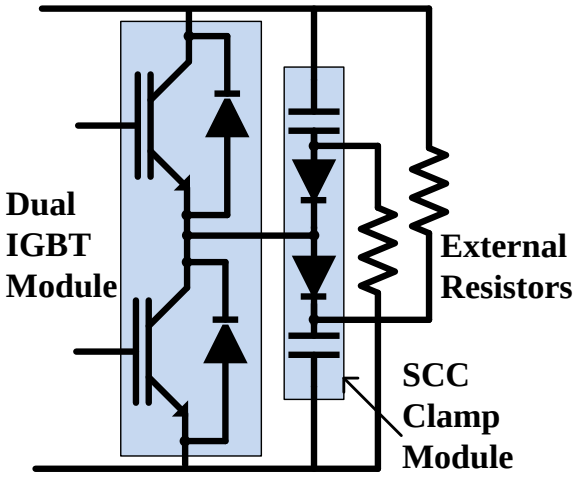
(a) C Snubber circuit.



(b) RCD Snubber circuit.



(c) SCM N&P Type module.



(d) SCC Clamp module.

Figure 2.12: Types of snubber circuits used in IGBT applications [89].

high switching frequencies. It causes a small power dissipation loss. The power dissipation loss caused by the resistance of the snubber is calculated by Equation 2.22

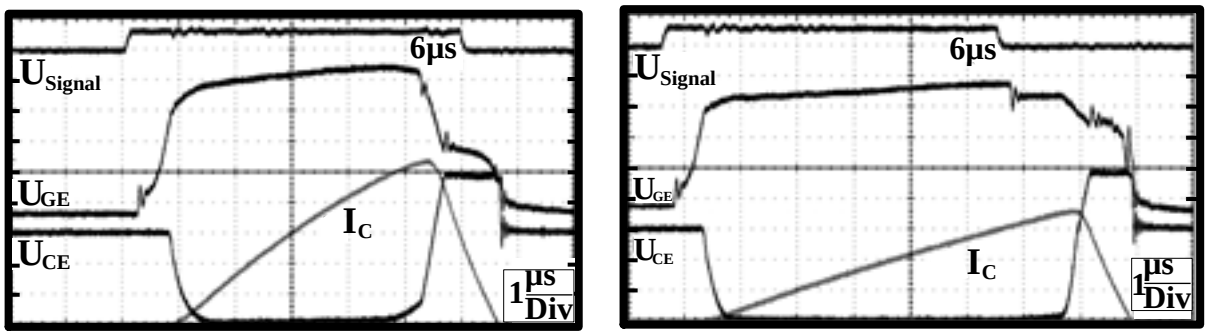
$$P_{snub} = \frac{L.I_0^2.f_{sw}}{2} \tag{2.22}$$

where L is the wiring inductance of the main circuit, I_0 is the collector current at the IGBT turn-off, and f_{sw} is the switching frequency.
The dual IGBT module can be protected by the SCC snubber circuit, as shown in Figure 2.12d. This circuit reduces a reverse recovery voltage transient.

As mentioned before, the effective protection design requires understanding the IGBT behavior under the short circuit conditions, where the short circuit current may be 10 times the normal current. Based on the fact that the withstand time of most IGBT modules for SC is 10 μs, the SC duration from the beginning to its turn-off must not last beyond 10 μs. Nevertheless, the SC time is affected by various circuits parameters and fault conditions. The maximum SC duration $t_{sc,MAX}$ greatly depends on the junction temperature $T_{vj,op}$ and the DC-bus voltage U_{DC}, where the higher $T_{vj,op}$ or U_{DC} will result in a shorter maximum permissible short circuit duration.

$$t_{sc} = f(T_{vj,op} \uparrow\downarrow, U_{DC} \uparrow\downarrow)$$

Moreover, the SC current and power dissipation are based on the inductance of the SC path. If the inductance is low, the di/dt at turn-on will be high, and the IGBT will be pushed into the desaturation state, as shown in Figure 2.13a, where The IGBT module enters the desaturation phase during a pulse time of 6 μs. This fast change can lead to excessive power dissipation which generates a high temperature. Accordingly, the IGBT is destroyed, if the short circuit is sustained. If the inductance is high, the di/dt at turn-on



(a) Low short circuit inductance.

(b) High short circuit inductance.

Figure 2.13: Effect of short circuit inductance on IGBT module behavior [100].

is low and the IGBT module doesn't enter the desaturation region quickly, as depicted in Figure 2.13b, where the IGBT doesn't go to the desaturation within the pulse of 6 μs.

Generally, when the short circuit is turned off rapidly, the IGBT goes from the saturation mode to the desaturation mode but if the short circuit occurs before the IGBT reaches the saturated operation and when the SC is turned off due to the protection, a high du/dt occurs. This problem may happen, if the turn on process is slow. Therefore, the driver stage must turn on the IGBT as much as possible in a short time to attenuate the negative effects of such critical situation [100]. The short circuit inductance also plays a key role in the short circuit during the turn on, where a very low inductance increases du/dt and charges the gate beyond the nominal gate voltage via Miller capacitor. As a result, the IGBT can be destructed in spit of the protection devices. Another parameter called the forward transconductance G_{FE} influences the short circuit current. The G_{FE}

is defined as a transfer characteristic which depicts how the gate voltage V_{GE} affects the collector current I_C with a constant collector-emitter voltage V_{CE}, where the rise of V_{GE} will result in the rise of I_C, as shown in Figure 2.14. Equation 2.23 defines the relationship between I_C, V_{GE}, and G_{FE} as

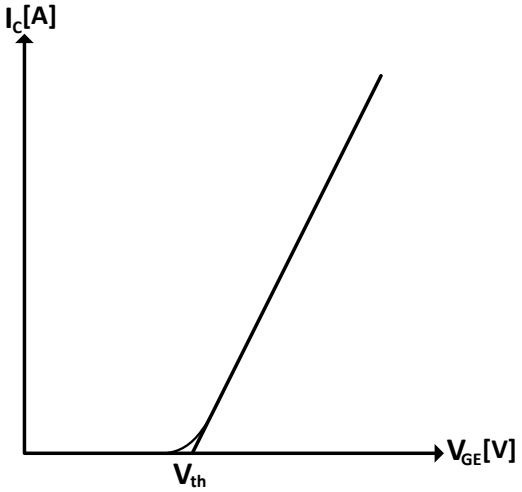


Figure 2.14: Gate voltage effects on the collector current [14].

$$I_C = G_{FE}(V_{GE} - V_{th}) \tag{2.23}$$

where V_{th} is the threshold voltage of the IGBT module.
The IGBT G_{FE} has a negative temperature coefficient. Therefore, it can protect the IGBT under the short circuit conditions [10].

The short circuit protection for the IGBTs and other power switch devices is an essential topic in the industrial applications, because the short circuit faults are destructive, and they can immediately destroy the switching devices and result in the entire drive system failure. Several approaches to the SC protection of IGBTs have been proposed and studied. Since the rise of the gate voltage V_{GE} is followed by the increase of the collector current due to the IGBT forward transconductance G_{FE}, several proposed SC protection methods were based on this function, where the short circuit current can be limited by the limitation of the maximum IGBT V_{GE}. The use of an external capacitor between the gate and the emitter can reduce the gate voltage after the fault. In addition, this capacitor reduces the Miller effect. But this technique affects the IGBT turn on time and it will delay the IGBT to reach its saturation mode. Another proposed method to reduce the V_{GE} during the SC fault is the use of a low gate resistor [18], where the fast change from the saturation to the desaturation causes a voltage swing which generates a negative current I_{GC}. This current causes the charge of the IGBT gate to values which are higher than nominal values provided by the gate driver. Therefore, due to I_{GC}, a low voltage will be created across the gate resistor which keeps the gate voltage within the nominal values. The increase

of the gate resistor value will result in the increase of the turn on time t_{on} and switching losses (E_{on}, E_{off}). Moreover, the use of a very small gate resistor causes EMI noises, and it can lead to higher di/dt or dv/dt values. Therefore, the care must be taken when the gate resistor is chosen.

Generally, all the output stages of the proposed gate drive circuits have a gate resistor that is split into two resistors $R_{G(on)}$ for switching turn-on, and $R_{G(off)}$ for switching turn-off. This allows controlling and optimizing the switching turn-on and switching turn-off separately [18] [17] [83]. Sometimes, series diodes are placed to the gate resistors, as shown in Figure 2.15. However, the disadvantages of this method are the increase of the voltage

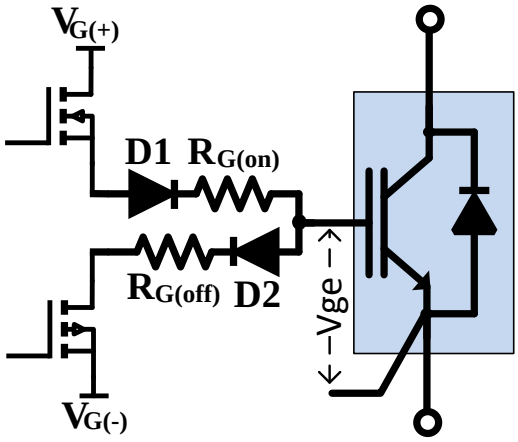


Figure 2.15: Gate resistors with series diodes.

drop at the output stage of the gate driver due to the diode forward bias, switching losses rise, increase of turn-on and off time, and increase of the PCB size.

As previously explained, when the IGBT transistor is turned on into a short circuit condition, a high current rises very quickly through it. After the occurrence of the short circuit detection, the IGBT is forced to turn off until it desaturates. In other words, due to the short circuit detection, the IGBT device goes from saturated operation to desaturated operation rapidly causing a high du/dt. Based on these conditions, several SC detection and protection circuits were suggested. The goal of these protection devices is to minimize the short circuit current and to decrease the high changes du_{ce}/dt. Therefore, the power dissipation is reduced and the system reliability increases. The fault current limiting circuit presented in [16] has the function of sensing the fault and lowering the gate voltage. The voltage V_{CE} is used to detect the short circuit fault. The advantage of this circuit is the reduction of the fault current and power dissipation during the short circuit. As a result, the short circuit withstand time increases. This circuit has several disadvantages: The first is that it cannot reduce the initial peak current because of its delay time during the normal turn-off transient conditions. The second is the disability of turning off the IGBT during the short circuit fault, and if the fault continues, the IGBT device will be destroyed. The last problem is that this circuit cannot detect the faults of light loads. Therefore, it is

necessary to use additional means to this protection circuit to build a complete protection system, but this will lead to a more complex design and more cost. A new active protection method is proposed in [39]. This technique can limit the fault currents to acceptable level and safely shut down the IGBT. This method includes the desaturation technique. The protection circuit is able to suppress the initial peak current value. However, since it uses a resistors and diodes to sense the fault occurrence, the response time delay prevents its usage in high speed switching devices.

The desaturation technique is a common method for detection of the fault occurrence in the IGBT device [16] [39] [32]. The detection of SC fault is achieved, if the collector emitter voltage V_{CE} rises above 5-8 V during the on-state operation. The SC condition indicates that the collector current I_C has exceeded the normal value. This method is simple because it uses only a diode for sensing the fault.

A new IGBT protection circuits are proposed in [33] [98] [102] to accelerate the fault detection time. The method technique is dependent on di/dt feedback control. The induced voltage across the stray inductance between Kelvin emitter and the power emitter is measured for the fault sensing. The induced voltage measured is investigated to extract the magnitude and the duration of di/dt signal which is used to control the IGBT shutdown during the SC fault. The advantage of this technique is its speed which allows it to be used with the high performance devices.

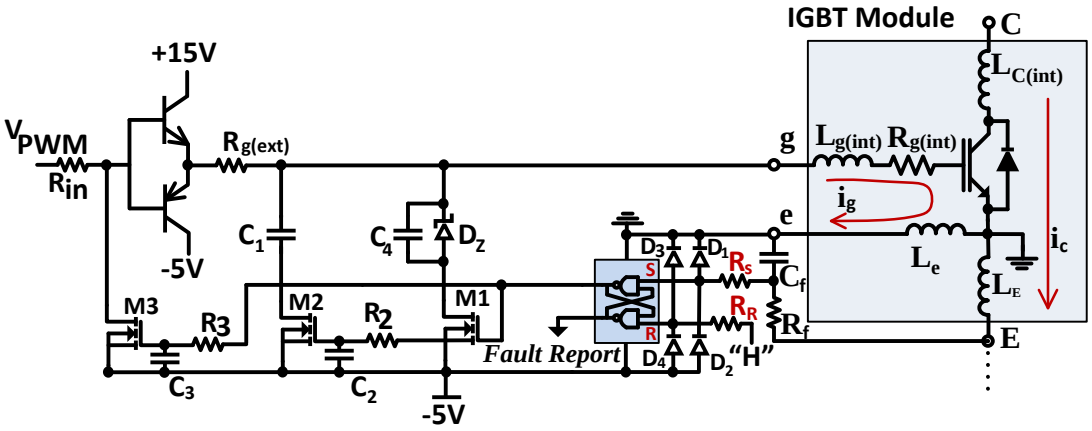


Figure 2.16: IGBT SC Protection circuit based on di/dt feedback control [102].

Figure 2.16 shows a SC protection scheme based on the voltage induced in the stray inductance between Kelvin emitter and the power emitter of the IGBT device. The induced voltage is given by Equation 2.24.

$$V_{Ee} = -L_{Ee} \cdot (di_c/dt) + L_{e(int)} \cdot (di_g/dt) \tag{2.24}$$

where V_{Ee} is the voltage drop between Kelvin and power emitter terminals in mV, L_{Ee} is the stray inductance between the power and Kelvin emitter terminals in nH. The di_g/dt

is very small and it can be neglected. Then the L_{Ee} is expressed as

$$L_{Ee} \approx -V_{Ee}/(di_c/dt). \tag{2.25}$$

The SC fault is detected by the RS NAND Latch circuit, while the gate voltage clamping is achieved by the zener diode D_Z and capacitor C_4. After the clamping of gate voltage, the IGBT is softly turned off by adding the M_2 and C_2 to the operation.

The similar approach has been discussed in [54], but in this proposed technique, the required measurements are achieved by a digital method. The digital method is an FPGA algorithm which can detect the SC occurrence.

All proposed SC protection circuits include a soft turn off technique to reduce the voltage spike caused by the high current falling rate, where the soft shutdown method increases the system reliability under the SC conditions [10].

Recently, SC protection circuits based on the gate voltage monitoring have been proposed. As early mentioned, the gate voltage changes during the fault period. Therefore, the analyzing of this change can lead to detect the fault condition. The approach suggested in [52] [72] [45] used the gate voltage sensing technique. The gate voltage signal is analyzed during the operation. Two comparators, SR latch and some logic components are used to analyze the gate voltage samples. The fault condition is decided based on the results of analyzing. This technique is capable to distinguish between the hard switch fault (HSF) and the fault under load (FUL). Figure 2.17 shows the block diagram of the proposed protection circuit for the IGBT device which depends on the gate voltage sensing, where the gate voltage is clamped after the detection of fault. Then, the IGBT device is softly turned off.

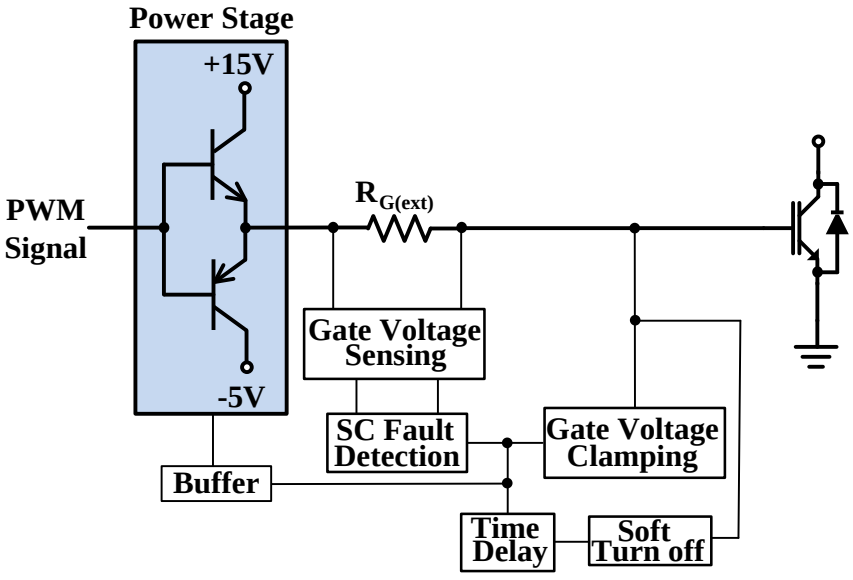


Figure 2.17: Block diagram of the SC protection circuit based on gate voltage sensing [72].

This proposed SC protection circuit based on the gate voltage sensing is simple, but it

requires a lot of components which increase the circuit complexity. In addition, the implementation of this scheme is not in the real time.

A new digital short-circuit protection method for the IGBT was proposed in [94]. The gate charge is the indicator of the SC condition, where it changes under the SC fault. The gate charge is reduced from the value of the normal condition. The protection circuit means are generally composed of a gate charge sense, a reference voltage generator and a comparator. The reference voltage generator and comparator are designed digitally using digital logic circuits in an field programmable gate arrays (FPGA). In addition, the digital circuit includes an analog digital converter (ADC) and a digital analog converter (DAC). The advantage of the digital SC protection is its high speed. However, the FPGA usage may increase the design cost. The proposed technique in [31] investigated the gate charge and the gate voltage to detect the SC condition for IGBT device. This method requires a real time monitoring for the gate charge and gate voltage using an FPGA, ADC, and a DAC. Figure 2.18 shows the block diagram of this technique based on the gate voltage V_{GE} and gate charge Q_G sensing.

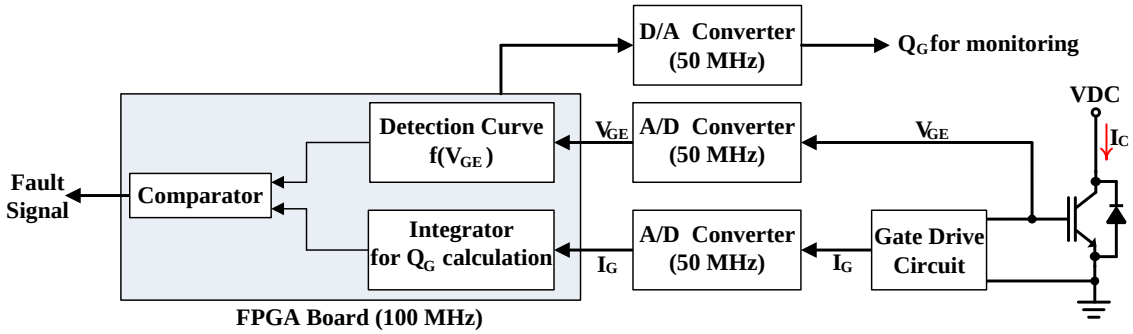


Figure 2.18: Block diagram of the SC protection circuit based on V_{GE} and Q_G sensing [31].

The measured characteristic of Q_G and V_{GE} in a normal condition is used to deduce the detection curve $f(V_{GE})$, as shown in Figure 2.19. Therefore, the experimental measurement is necessary for the IGBT device. The SC protection time of this method is shorter than the protection time of the previous methods, but the disadvantage of this method is the need of experimental measurement for the IGBT device.

The IGBT turn-on and turn-off are treated as transient phenomena. The IGBT transient phenomena, which are related to the charge profile of the parasitic input capacitance, can directly show the damage of the IGBT or other parts in a drive system. During the switching transient of the IGBT devices, the power dissipation and switching stress increase. Therefore, the switching speed is required to reduce the effect of these phenomena on the IGBT performance. In other words, the IGBT protection against the transient surge is required. As mentioned before, using the snubbers and clamps optimizes the IGBT protection against voltage transients during the normal switching operation.

Generally, the transient phenomena in the IGBT devices during the normal switching operation include the turn-on di/dt and turn-off dv/dt. The gate driver design plays the

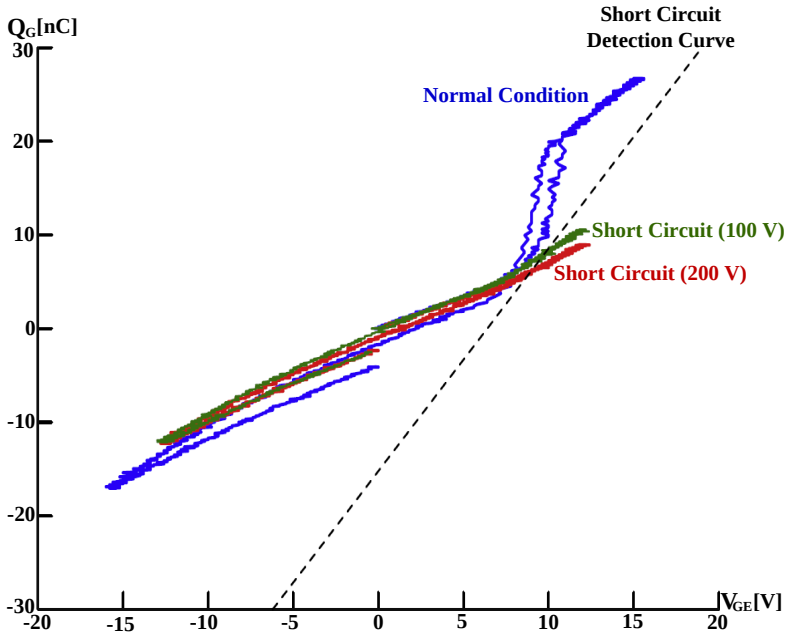


Figure 2.19: Characteristic of Q_G vs V_{GE} [31].

key role in the control of the IGBT switching operation and its transient phenomena [79]. The proposed technique in [34] offered the possibility of controlling di/dt and dv/dt in the IGBT, where the gate drive circuit is used to achieve this method. This method is based on the introduction an intermediate voltage level between $0 - 15\,\mathrm{V}$ in the square pulse voltage generator, during the turn-on and turn-off of the IGBT device. This method has the advantages of short switching time and low losses compared to the conventional methods which include the gate resistors. However, if this method is compared with the modern methods, the delay and switching losses will be higher. The similar method has been adopted in [71] [12] [101]. This method uses the feedback loop coming from collector voltage to control the gate voltage during the switching operation. The controlling di_C/dt and dv_{CE}/dt during the IGBT switching operation was also achieved using the active gate driver (AGD) investigated in [56]. This technique is also based on the closed loop feedback, as shown in Figure 2.20. The PI controller used in the AGD is composed of a high bandwidth operational amplifier to provide the required output current. The di_C/dt and dv_{CE}/dt feedback loops are used to keep the system in the stable state, where the dv_{CE}/dt feedback provides a positive signal for the voltage slope, and the di_C/dt feedback provides a negative signal for current slope. The advantages of this method are the direction control of V_{CE} and i_C, and the compensation of non-linearity, but the complexity of this method limits its usage in drive systems. In addition, the need of sensors increases the losses and cost. Moreover, this method does not have any mean for IGBT fault for protections. In order to minimize the number of sensors used in the feedback loop, [27] proposed a gate drive unit with closed-loop feedback for the control of collector current slope di_C/dt. But the complexity, cost, fault protection circuit, and additional losses stay the problematic of

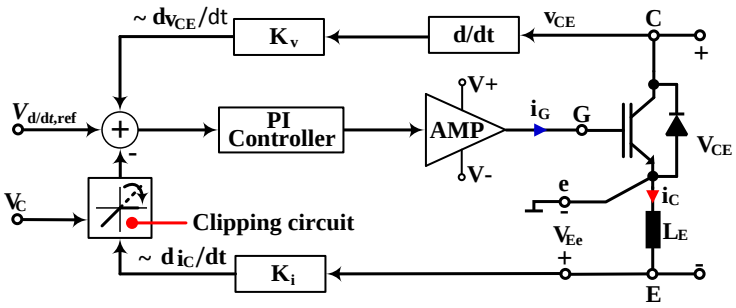


Figure 2.20: Block diagram of the basic proposed closed loop active gate driver [56].

these methods which adopt the feedback loop control.

Recently, the fault detection and diagnosis in drive systems depend on the online monitoring and measurement [64] [115], where the extracted online information can be used for the design of fault tolerant control system (FTCS). Based on the relationship between the healthy switching device and its parameters (V_{CE}, V_{GE}, I_G, I_C, transient time during turn-on/turn-off, etc.), any change in these parameters during the fault conditions will affect the IGBT device performance. Therefore, the online fault detection and diagnosis (FDD) is implemented based on the preset values of device parameters during normal operation.

Few works described the ability of online fault detection and diagnosis. The proposed online fault detection algorithm, which was discussed in [3], is able to detect multiple early stage faults in IGBTs, where this algorithm depends on the preset parameters of healthy IGBT device. The advanced gate driver architecture is designed to acquire the required quantities for online monitoring and detection the failure. But this approach provided the experimental results based on the analog measurements and offline processing. The FPGA can be used to implement these online measurements and monitoring for the fault detection and diagnosis.

Generally, the monitoring and measurement of all healthy device parameters require very complex circuits, difficult algorithms, and high budget. Therefore, only one critical quantity is chosen to be monitor and measured. Based on this quantity, the other quantities can be estimated. Then, the fault detection and diagnosis may be implemented. The online measurement of the collector emitter voltage V_{CE} is a common method for the fault detection and diagnosis. In addition to use a protection against the short-circuit and overload currents, the V_{CE} is used for the IGBT junction temperature online monitoring.

The IGBT devices and any power devices used in the drive system are prone to high temperatures during the operation, where the high temperatures may result in the IGBT rupture [58]. Therefore, the protection of IGBT against degradation, which occurs gradually due to the high temperature, is important. There are several parameters in IGBT modules which are affected by the temperature such as on state voltage drop, threshold voltage, saturation current, leakage current, electrical resistance, and turn on or turn off energy loss [9]. There are variety of methods used for measuring the temperature of the IGBT device [9]. Several methods based on the electrical parameters have been presented

in literature. Online estimation technique for IGBT junction temperature $T_{vj,op}$ has been presented in [46]. The proposed method uses the on state voltage drop $V_{CE(sat)}$ for the estimation of $T_{vj,op}$, where $V_{CE(sat)}$ is the function of $T_{vj,op}$, collector current I_C, and gate driver voltage V_G. Figure 2.21 shows the circuit used for measuring the $V_{CE(sat)}$. The dis-

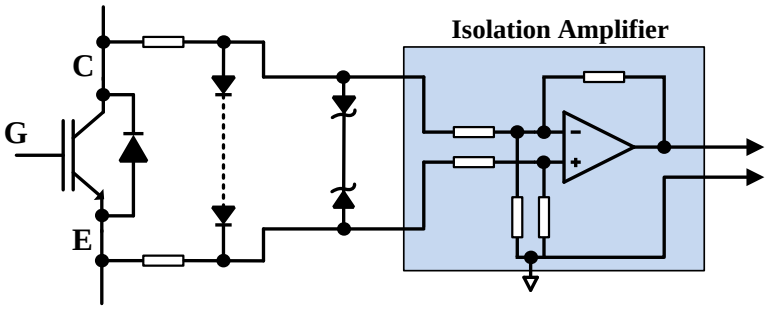


Figure 2.21: On state voltage drop sensing circuit [46].

advantage of this method is that it is difficult to guarantee the accuracy due to the small value of $V_{CE(sat)}$, and the change of $V_{CE(sat)}$ during the switching transient is very high. In addition, the components, which are used for measuring and sensing, require a high isolation if high voltages are used. The $V_{CE(sat)}$ based monitoring was also used for bond wire lift off detection [92], while the proposed monitoring method, which has been presented in [64], depended on the measuring on state resistance R_{on}. The developed technique discussed in [114] adopted a new system for early detecting the solder joint degradation and wire-bond lift off in IGBT devices. This system is composed of hardware and software architecture. The adoption of this method on the $V_{CE(sat)}$ for predicting would make it face difficulties related to the measurement accuracy. The technique presented in [7] is based on online V_{CE} measurement for prediction the case of IGBT modules before the complete degradation due to the high temperature. The proposed circuit, which is similar to desaturation protection technique, uses two serial diodes for the V_{CE} sense, and a differential operational amplifier is used for the V_{CE} calculation, as shown in Figure 2.22. The output

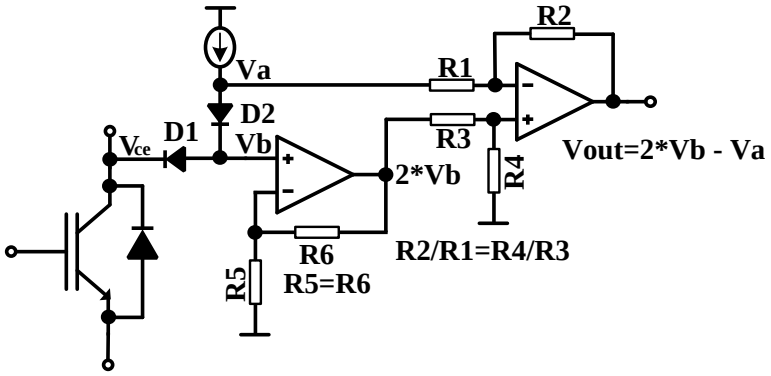


Figure 2.22: Online V_{CE} measurement circuit for the IGBT wear out monitoring [7].

of this circuit can be connected to parallel analog digital converter (ADC) which connects to the FPGA board. The extracted information from the AD converter can also be used for FTCS design.

As previously mentioned, the degradation of IGBT device occurs gradually. Therefore, the monitoring of defects inside the IGBT module during the operation may avoid it from the complete catastrophic failure that can affect the other drive system parts. Moreover, the maintenance can be regulated to decrease its high cost. Based on this importance, the researches still continue to invent more accurate methods for monitoring and predicting the IGBT module faults that lead to a catastrophic failure. Based on the fact that the changes of gate current I_G is caused by the change of some parasitic elements inside the IGBT module, the proposed technique in [120] used the changes of the I_G for monitoring the defects of IGBT module. This method depends on the RVM algorithm [96] for monitoring defects in an IGBT module using the gate current at beginning state. The accuracy of this method may be higher than the accuracy in the previous methods, but the complexity of programming the algorithm limits its use in drive systems.

Generally, the gate voltage monitoring is used for fault detection and diagnosis, where the change of V_{GE} can indicate the fault mechanism in the IGBT module. The technique proposed in [81] is based on the V_{GE} monitoring. But so far, this method was applied on the resistive load under low voltages.

The fault detection and isolation (FDI), fault detection and diagnosis (FDD), and fault-tolerant control (FTC) and the interaction between them are considered a suitable way for improving reliability and flexibility of drive systems. In addition, the cost of repair and maintenance decreases highly.

In general, the behavior of system changes suddenly and quickly during the abrupt faults, whereas, it changes gradually and slowly during the incipient faults. The abrupt faults are diagnosed based on tested methods, while the incipient faults are diagnosed based on the estimated methods. Based on the previous study, the types of faults, which can be taken into account in semiconductor power devices, are short and open circuits. Generally, the faults are detected, confirmed, and diagnosed. The FDD analysis is important for the fault-tolerant technique. The fault tolerant control system (FTCS) is designed to achieve stability, reliability, flexibility, and satisfactory performance, not only when all the system is working normally, but also in cases when there are malfunctions in some components of the control system. The FTC can be classified into two types: passive (PFTC) and active (AFTC) [119]. The PFTC does not require FDD schemes or controller reconfiguration, where the controllers are robust against several of preset faults. Therefore, the PFTC limits the fault tolerant capabilities. In contrast to PFTC, the AFTC requires FDD information for control reconfiguration [38].

The FTCS used in IGBT inverters depends on the redundant components, to keep the process in the operation when the faults are detected and diagnosed. The FTCS improves both the reliability and the safety of technical systems. Additionally, the FTCS reduces the maintenance costs, which are very expensive, and it improves the life time of the drive system. Figure 2.23 illustrates the scheme of FTCS based on redundancy. The function modules can include hardware components or software, and the redundant components

can be identical or diverse. The redundant modules are usually connected in parallel. The reconfiguration system is achieved after the fault detection and diagnosis, where this mechanism switches off the failed components and switches on the auxiliary components.

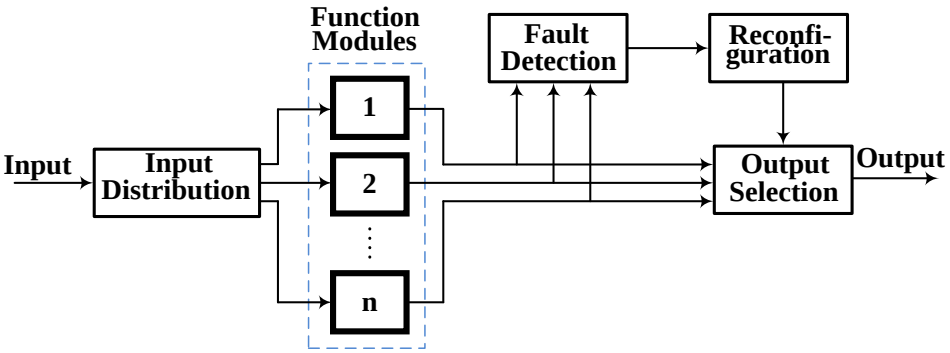
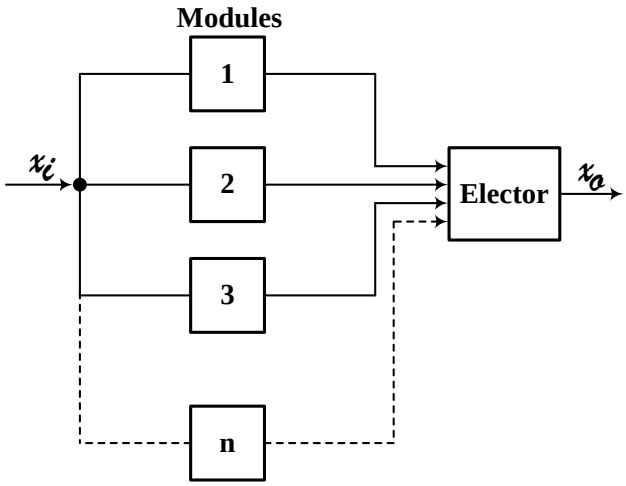
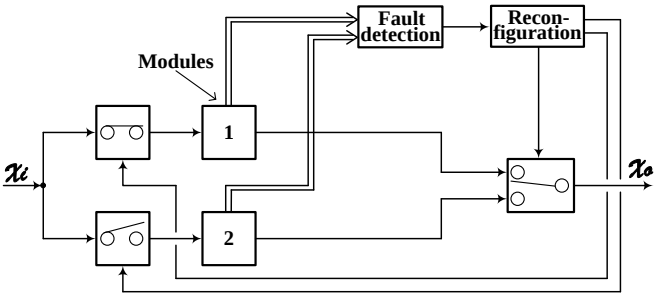


Figure 2.23: Scheme of a fault tolerant system with redundant function modules [36].



(a) Static redundancy scheme with active parallel modules.



(b) Dynamic redundancy with two modules (Active and Inactive).

Figure 2.24: The schemes of FTC types [36].

Generally, the fault tolerant control based on redundancy has two types: a static redundancy and a dynamic redundancy. The static redundancy is composed of several parallel modules which have the same input signal, whereas their outputs are connected to an elector. The elector chooses which signal is correct for the control. Figure 2.24a depicts this type of the FTC. The disadvantage of this FTC type is that the parallel modules are always active and this increases the power losses. Additionally, the input signal fault, which can force entire system to stop, is not taken into account. The dynamic redundancy is more complex, as shown in Figure 2.24b, where it includes two modules, the first module is active, and the second is inactive. If the fault is detected by the fault detection module, the system is reconfigured to activate the standby module, which is normally inactive. The disadvantages of this FTC type are the complexity and the higher cost. In order to overcome the disadvantages of FTC types, a hybrid redundant system is combined from both types of FTC.

In the literature, several approaches deal with the fault tolerant control (FTC) in drive systems which are fed by IGBT inverters. An overview of many fault-tolerant frequency inverter topologies is presented in [103], where this overview concentrated on the features, requirements, costs, and performance limitations of these proposed fault tolerant methods. Moreover, a comparison between the suggested techniques in the literature were achieved. It was noted that all fault tolerant control techniques in drive systems depend on the redundancy. The proposed techniques in [21] uses four legs for the inverter. Upon the fault occurrence, the faulty leg is isolated and the spare leg is switched on by the configuration module. The isolation of faulty leg is achieved using fast active fuses and back to back connected switches (SCRs). This method is able to protect against the short circuit and open circuit, which occur in the same inverter leg, but the cost of this method is very high and it needs an efforts to design the algorithm that is used to detect and isolate the faulty switch in one inverter leg. The similar technique for fault tolerance in drive system was discussed in [61] [26], where additional components (hardware, software) are used to increase the reliability and flexibility, but this, on the other hand, led to a higher cost and complexity.

When the power system feeds important loads which require nonstop source, the fault tolerance can play a key role in the voltage source continuity. For example, the fault tolerant control applied in the wind turbines, can temporarily guarantee the voltage source continuity, upon the fault occurrence, until the failure is repaired by the operator, this implies that the reliability and flexibility would be improved. The proposed technique in [42] and [43] adopted the fault tolerant design for inverter used in wind energy conversion systems (WECS). This proposed method is able to detect and diagnosis the faulty switch in the inverter leg. Then, the faulty switch is isolated and the redundant components are switched on. In order to accelerate the time of fault detection and diagnosis, an FPGA is used. It is noted that inverters based on fault tolerance used , in addition to three legs, one auxiliary leg. This redundant leg replaces the faulty switch when the fault is detected and diagnosis.

Recently, the proposed techniques depend on using more than one auxiliary leg in inverter to protect against the faults, which may occur in different legs at the same time. For

example, the proposed method in [37] discussed the fault tolerant inverter with three spare legs, but the complexity and costs of this technique limited its use and it was replaced by fault tolerant five leg inveter method [90]. This technique uses two spare legs instead of three legs, which leads to reduce the complexity and costs. If the faults occur in two legs simultaneously, the system is reconfigured to isolate the faulty legs and switch on the redundant legs. The speed of fault detection and diagnosis is based on a single FPGA controller, where the reconfiguration is required after the FDD. Accordingly, the reliability and flexibility are improved. The importance of the fault tolerance in the industrial application also leads the researchers to study the multilevel inverters based on FTC [93] [59]. However, in spite of their capability in the service continuity after the fault occurrence, the higher costs and the complexity of algorithm control, which require fast software and hardware for FDD and reconfiguration, may also prevent the adoption of these methods.

Based on the previous review, it is noted that the control units used in the drive systems play the key role in FDD and FTC. Generally, the control unit is composed of hardware and software. The hardware includes the gate driver, protection and diagnosis circuits, controller, whereas the software includes all algorithms for FDD and FTC. In order to minimize the time between the fault detection and diagnosis, using the field programmable gate arrays (FPGAs) is the new solution for the FTCSs, power electronics, and drive applications [63]. FPGAs can perform networking and control support simultaneously. A single FPGA can do the work of dozens of microcontrollers. Therefore, the microcontroller is going to disappear with the FPGA appearance. The industrial control systems based on the FPGAs design proved their flexibility, reliability, capacity, and fast response in difficult conditions. Nowadays, complex functions for power electronic systems are implemented using the FPGA controller design. The FPGA controller was used in the application of switching power converters [30], where the designed digital circuit generates 16 signals for controlling 32 transistors in DC-DC back bidirectional converter. Using this digital control implemented in the FPGA provides a very high accuracy. The usage of FPGAs in voltage source inverters fed induction machines was discussed in the literature. The proposed digital control circuit for multilevel multipulse source voltage converter, which is presented in [68] [73], is based on the FPGA design, where it implements the pulse width modulation signals (PWMs) for the switching of the power electronics used in the proposed drive system. Additionally, a lot of researches discussed the design and implementation of PID controllers using FPGA. For example, the article presented in [118] proposed a digital anti-windup controllers PI to regular the speed of induction motor, the design is implemented using FPGA chip-Spartan3 in VHDL language. Also the research developed in [78] introduces ALTERA FPGA to implement an intelligent PID controller.

As mentioned before, the gate drive circuit is the key part in the control unit of any drive system, and it behaves as a power amplifier, where it amplifies the digital signals coming from the digital controller. Moreover, it can play a key role in the fault detection and diagnosis of power electronic devices used in drive systems. Nowadays, in industrial applications, there are very advanced digital gate drivers for high power IGBT modules up to 6500 V, the main features of these drivers are variable gate ON/OFF resistors, advanced desaturation and di/dt protection, active feedback clamping, high peak output current and

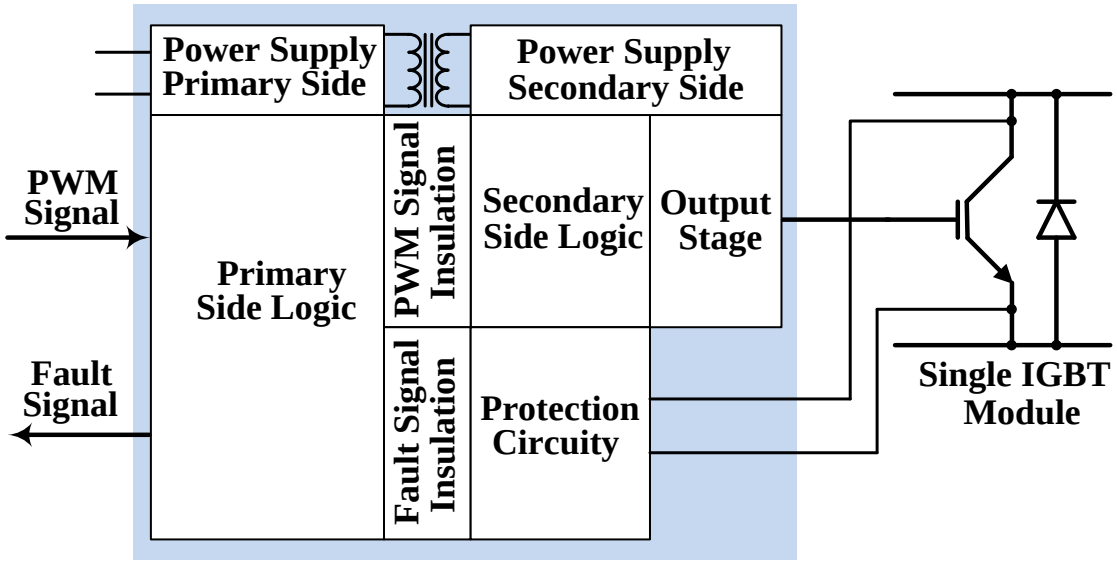


Figure 2.25: Standard driver architecture [47].

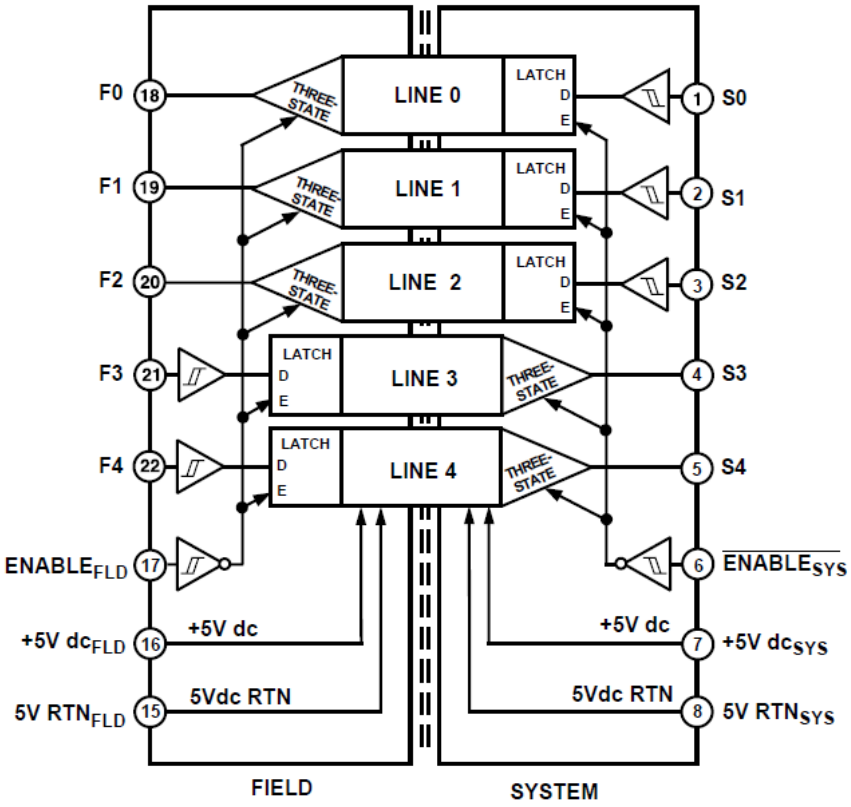


Figure 2.26: Functional block diagram of the logic isolator "AD261" [22].

output power, short signal transition times, and soft shut down [32]. These drivers have a programmable control unit as a driver core and the software defines all functions including digital filtering or digital timing and contains several algorithms for the protection of IGBT.

Generally, standard drivers are built according to the architecture shown in Figure 2.25. They include usually an output stage, secondary logic, protection circuits and secondary part of insulated power source on the secondary side (side of power transistor). Whereas on the primary side, there are primary parts of power source and primary logic. The control PWM signals and power supply are transferred through the insulation barrier to the secondary side and transistor/driver error signals are transferred to the primary side.

The Insulation barrier must have high du/dt immunity, low parasitic capacity and static insulating capability according to the application field of the driver. The insulation barriers are usually realized using opto-couplers or signal transformers. The main function of an opto-coupler is to block the high voltage which can destroy the components of electronic circuits. The opto-coupler is usually designed to withstand a very high voltage (500 V to 10 kV) between its input and output. The main disadvantage of opto-coupler is the propagation delay and propagation delay skew during the transfer of logic signal from its input to output. Accordingly, the digital signal may be distorted. Therefore, the designers are continuing to develop new techniques, which reduce the delay time and eliminate the distortion during the signal transmission. There are now high speed logic isolators. Figure 2.26 illustrates a block diagram of a high speed logic isolator which can be used to isolate digital control signals from microcontroller. Additionally, it can isolate the signals related fault detection and data transfer. The propagation delay of this isolator is only 14 ns. Since the problem of isolation is still the main issue for designers and researchers, other techniques for isolation barriers were presented in the literature, for example the proposed method in [5] discussed the implementation of an IGBT control signal by wireless transmission, while the proposed method in [84] used a printed transformer which can insulate a voltage of 10 kV.

Chapter 3

Proposed IGBT Gate Driver Architecture

From Figure 2.25 in section 2.2, the development of the gate driver architecture is necessary for purposes of the proposed diagnosis in the developed gate driver. The proposed gate drive circuit architecture is shown in Figure 3.1, where the analog measurements of required quantities are implemented on the secondary side of the proposed gate driver.

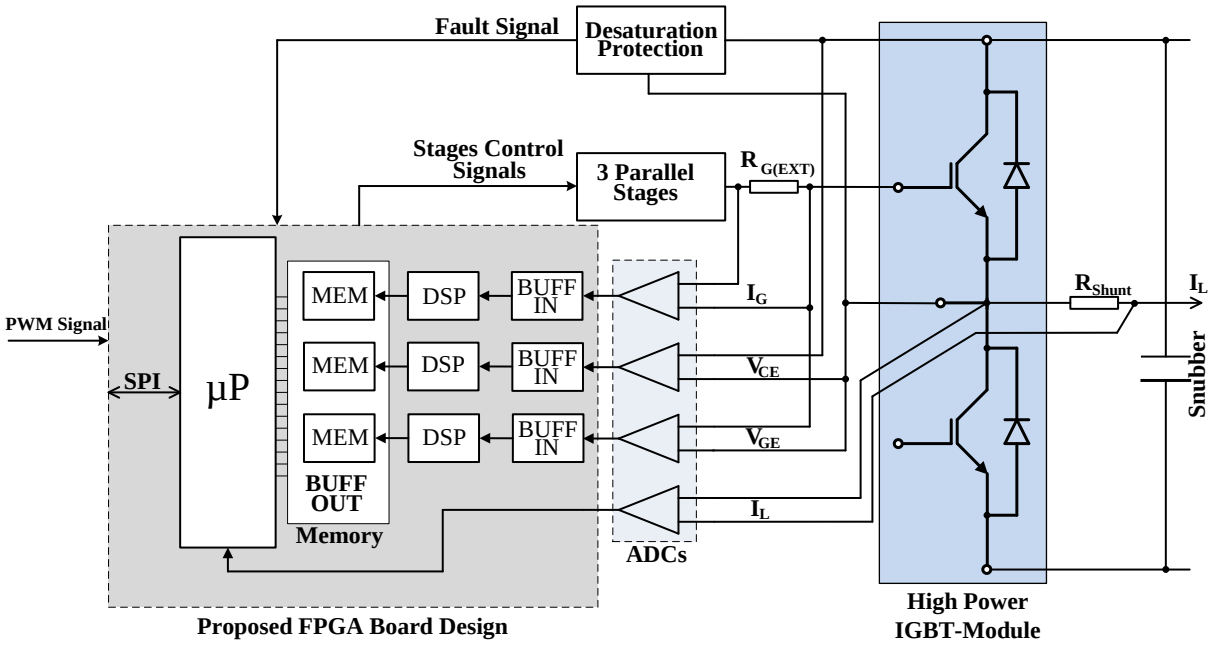


Figure 3.1: The Architecture of Proposed Gate Driver with ADCs Devices for Monitoring and diagnosis [70].

The measured quantities are V_{CE}, V_{GE}, and I_G. Additionally, the load current I_L can also

be measured. The transients of these quantities can be evaluated. Then, the quality of switching process can be monitored.

The analog measurements of the required quantities can be realized using dedicated electronic circuits such as peak detectors, differentiators [48]. Then, the characteristics of measured quantities can be observed using ADCs. Accordingly, any change in the particular characteristics of any measured quantity can point on the switching device degradation. The quantitative evaluation of the measured quantities is implemented after continuously sampling their signals at a rate equal to a sampling frequency f_s of ADC converters. The transient states in the high power IGBTs occur within 2-5 μs typically. Therefore, high speed ADCs must be used for obtaining sufficient number of samples. We assume at least 100 samples for the switching process. It means 50 MHz sampling frequency is necessary. The ADC converters outputs represent the digital data of the measured quantities, which will be taken into input buffers synchronously with rising and falling edges of input PWM signal, as shown in Figure 3.1. Mathematical methods are used to analysis and process the sampled data. Since the sampling interval is $1/f_s$, the mathematical algorithm must sufficiently be fast to maintain the analog signal characteristics. The Discrete Fourier Transform (DFT) and its fast implementation, the Fast Fourier Transform (FFT) are usually used for the calculation. The wavelet transform can also be used for digital signal processing (DSP). Field Programmable Gate Arrays (FPGAs) hardware provides these algorithms cores with maximum speed and high flexibility for DSP [99]. Moreover, one FPGA includes more functions, such as multipliers, adders, multiplexer, barrel-shifters, counters, logic blocks, memory banks, etc.

The outputs spectrum of the DSP is the magnitude of signal (unit of signal) as a function of frequency. The particular faults are analyzed and quantitatively evaluated as a function of selected spectral lines generally. These fault indicators are compared with preset thresholds and their time courses are recorded for time extrapolation. If the fault indicator value exceeded the threshold value, a fault signal is sent to avoid the failure propagation in the particular IGBT or any part of the inverter. The time to reach the critical value of particular fault indicator can be computed using exponential extrapolation methods. RAM and FLASH memory are necessary for measured data storage.

On the other hand, monitored parameters which aren't important for the gate driver control and which serve for long-time monitoring as I_L can be transferred in longer intervals, as shown in Figure 3.1.

3.1 Gate Driver Interface

The data transfer of PWM control signal and back transfer of fault signal are assumed using separate insulated channels, as shown in Figure 3.2. Separate fault signal is not necessary, because the error information is also transferred through the data interface. However, in the case of requirement for switching-off other transistors of inverter simultaneously, it is necessary to separate the fault signals.

The bi-direction data synchronized with the inverter control unit (main controller)

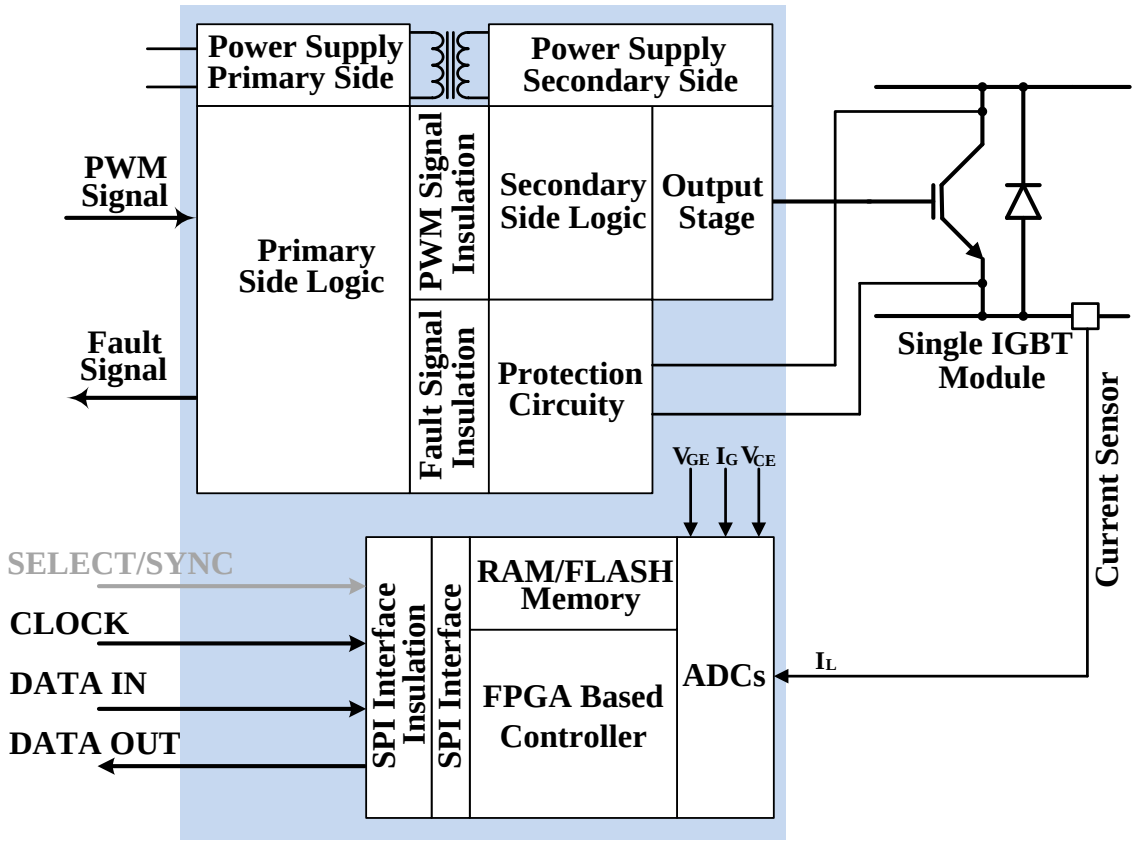


Figure 3.2: Interface Between One IGBT Gate Driver and Main FPGA Controller.

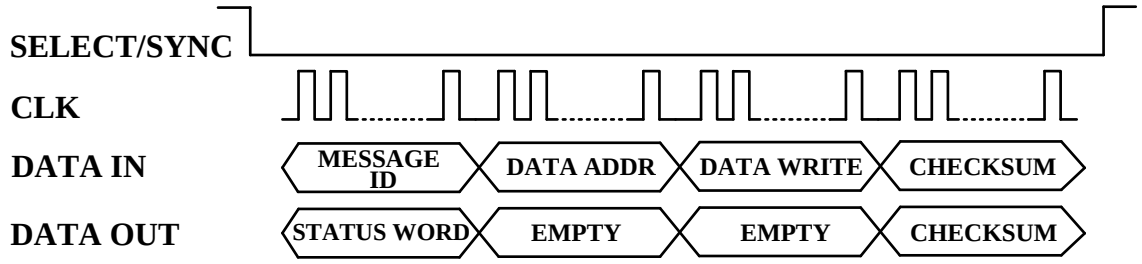
require a high communication speed, reliability, and simplicity of implementation. There are many types of serial communication interface, which can be used for this purpose. A Synchronous Peripheral Interface (SPI) is used in the drive system, as shown in Figure 3.2. In this type of communication interface, at least four isolated signals are required. These signals are:

1. Serial clock (CLK).
2. Data coming from the main controller (master) to the single gate driver FPGA based DSP (DATAIN).
3. Data read from the single gate driver FPGA based DSP (DATAOUT).
4. Control signal (SELECT/SYNC).

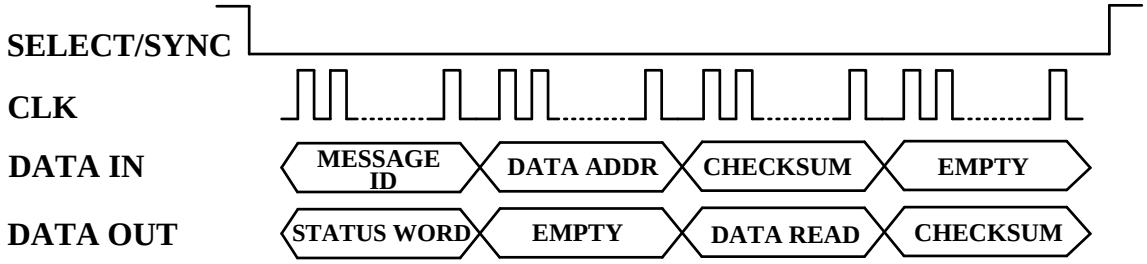
The control signal (SELECT/SYNC) is used to define the beginning and the end of data transfer. This signal is not used when the data transfer in one master-one slave communication, but if this signal is used, the communication will be more reliable and simple. Using SPI with SELECT/SYNC creates a synchronous space between the feedback quantities and

the modulation cycle period, especially in relation to inverter output currents measured in the gate driver. Falling edge of SELECT/SYNC signal can be used as a command for sampling of relevant ADC channel. The inverter control unit can use one common signal for simultaneous sampling of all output currents of the inverter or six of these signals can be used for sampling data in each gate driver in individual time.

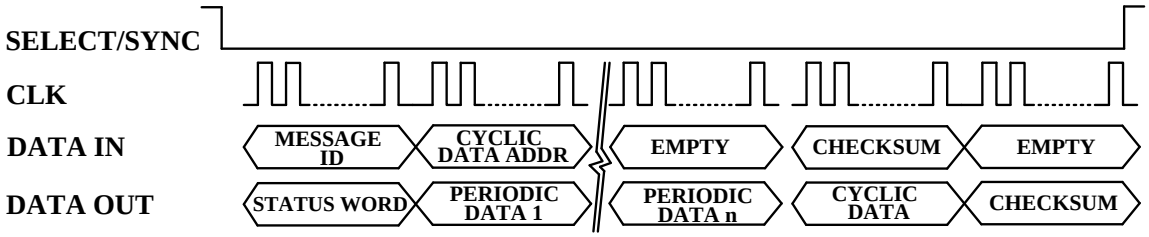
3.2 Data Exchange SPI Protocol



(a) Data frame for writing parameter into one gate driver memory.



(b) Data frame back reading of parameter or an individual variable.



(c) Data frame for periodic data exchange between driver and inverter controller.

Figure 3.3: Proposed SPI data transfer protocol.

Data exchange is realized between the main controller of the inverter and the gate driver FPGA by a simple communication protocol for SPI.
There are several services required in the data transfer: driver parameters settings and periodic data reading from the driver at each modulation period. Read data can be divided

into two groups: Feedback data used for control process (PERIODIC DATA) and data used long time for power transistor and driver secondary side monitoring. These data are called CYCLIC DATA, because they are mixed to periodic frame. Each message contains one issue of cyclic data addressed by the inverter control unit. At least two message types are necessary:
The first one is constant writing into gate driver FLASH memory. The data frame is shown in Figure 3.3a. The message, which is sent into the gate driver, contains data field $MESSAGE\_ID = WRITE\_CONSTANT$. The following data field (DATA ADDRESS) contains address (negotiated index) of written data. The third field contains value of written parameter. Checksum is unavoidable. Driver status (STATUS WORD) is sent back in each type of message. Status word contains status flags of individual protection circuits and limit values over passing.
The second message type is data exchange $MESSAGE\_ID = DATA\_EXCHANGE$, as shown in Figure 3.3c. For periodic data exchange in each modulation period, there are fields in outgoing data ($PERIODIC\_DATA1 to PERIODIC\_DATAn$) reserved. Only the inverter output current is assumed to be a periodic data. It means that the data packet length is only four words including checksum. The incoming data contains the address (index) of desired cyclic data, where its value is sent back in outgoing data in next word. Therefore, when the incoming checksum is invalid, it is possible to make also invalid outgoing checksum in the last data field of outgoing data frame. Due to this feature the validity result of complete data transfer in the inverter controller is immediately known.
For written data validation, it is important to have possibility of backward data reading. For this purpose, the next message type parameter/variable reading (MESSAGE_ID = READ_DATA) is designed, as shown in Figure 3.3b.

3.3 The proposed IGBT Gate Driver

Figure 3.4 shows the detail of the proposed IGBT gate driver for one channel. The IGBT gate driver for one channel, whether the upper or the bottom, includes the following components:

- FPGA based controller: It receives the measured digital signals, such as I_C, VGE, I_G and V_{CE}, from high speed parallel ADCs across buffer functions using a Verilog program.
- High speed parallel analog digital converters: High speed (105 MSPS), high resolution (10 bit) ADCs are used in the design. Their analog inputs are the outputs of the dedicated circuits for the quantities which are going to be measured. The ADCs are operated with the internal reference of 1 V or 0.5 V, this depends the configuration. The ADCs clocks are generated by the gate driver FPGA using Verilog code and another tools. The clock frequency range must be from 50 MHz to 105 MHz, this is based on the required sampling rate.

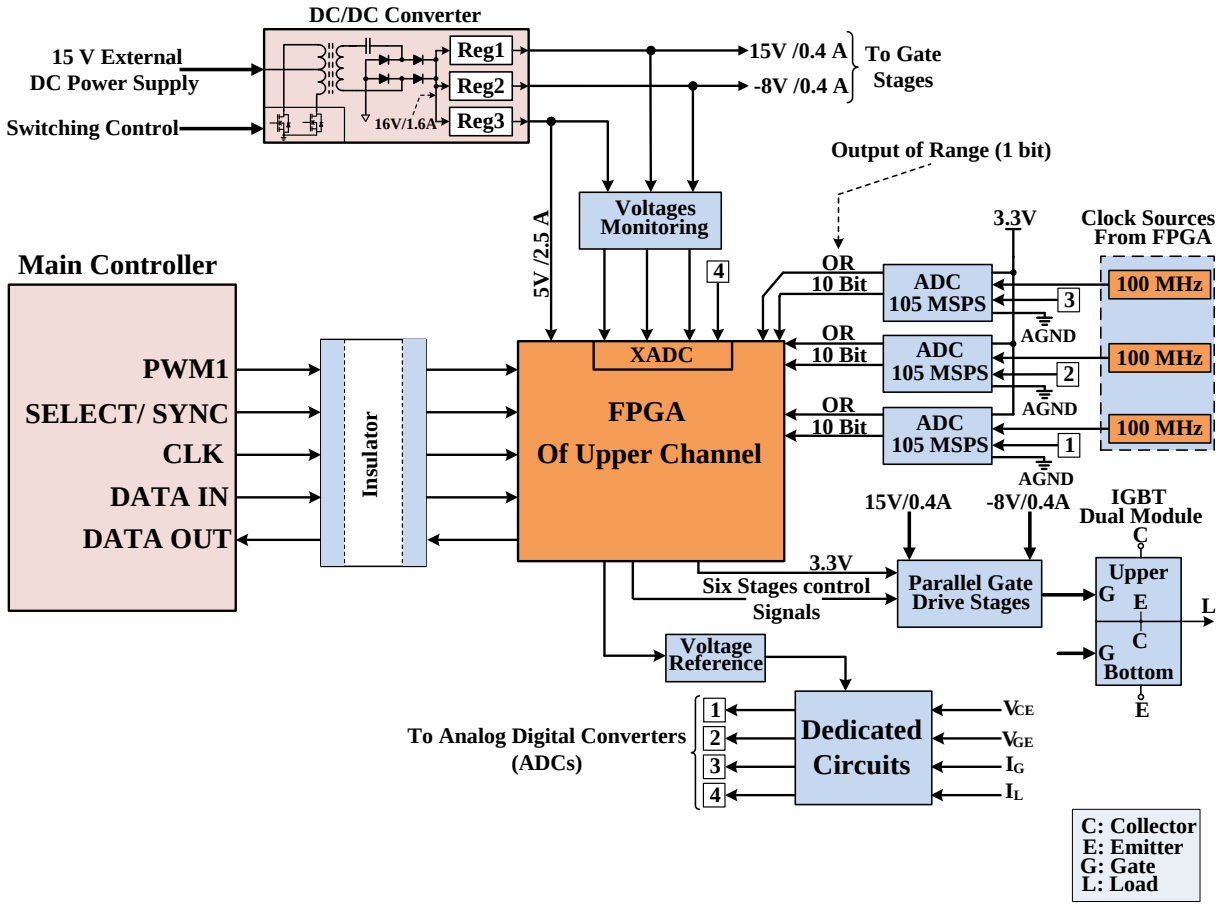


Figure 3.4: IGBT gate driver detail for one channel in IGBT module.

- Voltage references.
- Parallel gate drive stages: They are used to control the external gate resistors during the turn-on/turn-off.
- Stages control signals: They are used for controlling the parallel stages inputs. A Verilog code can be written for generating these control signals which assert delay times between the gate stages during the IGBT switching.
- Insulator: A high speed logic isolator could be used to isolate digital control signals from the main controller, see Figure 2.26 in section 2.2.
- High speed communication: An SPI interface can be used to achieve the exchange data between the main controller and the used FPGAs based controller which are used to analysis the measured digital signals in the gate drivers.
- Dedicated circuits: They can be voltage dividers,operational amplifiers, anti-aliasing filters, etc.

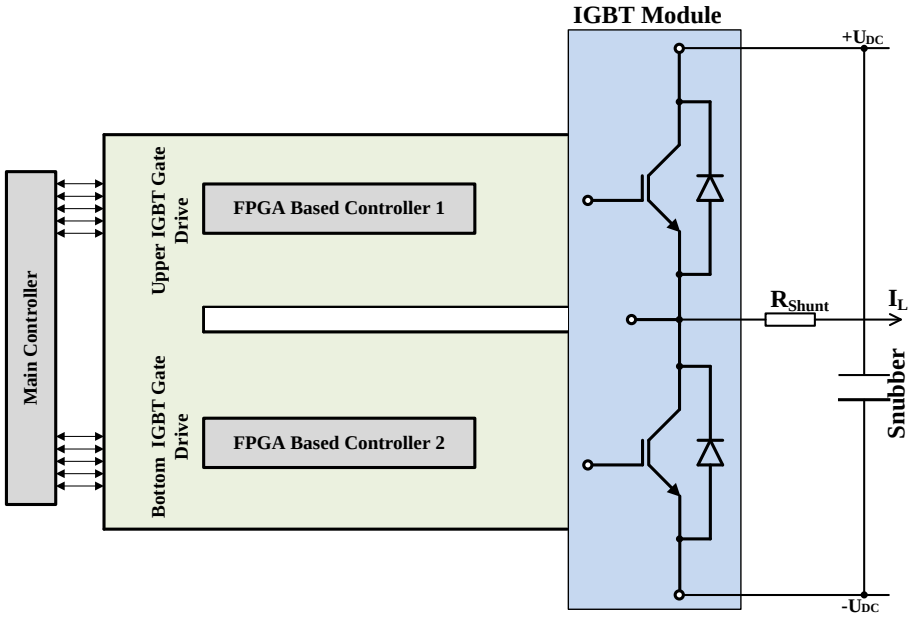


Figure 3.5: Physical configuration of the proposed IGBT gate drivers based FPGA controller.

- Insulated DC/DC converter: The zero voltage zero current (ZVSZCS) push-pull resonant topology and regulators are designed for this purpose.

Figure 3.5 illustrates the physical configuration of FPGAs on one inverter leg, where each IGBT gate driver has its own FPGA board. The main controller, which can be a microcontroller or an FPGA based controller, implements exchange data with each gate driver FPGA in the drive system.

3.4 Design of the Proposed IGBT Gate Driver

Based on the previous study, the IGBT gate driver can perform the following functions:

1. Convert the logic signals to power signals.
2. Charge the gate capacitance during the IGBT turn-on and discharge it during the turn-off.
3. Protection functions such as short circuit and over-voltage protection and control of di/dt and dv/dt during the switching operation.
4. Affect the dynamic behavior of the IGBT and the freewheeling diode.
5. Separate the low voltage side connected to the controller from the high voltage side connected to the IGBT.

Therefore, the gate driver must be designed carefully.

Generally, the logic signals level used for gate drive circuits is 5 V. In the FPGA controller, the maximum level of the logic signal is between (1.8 V − 3.3 V), this value is based on the FPGA bank used to generate the logic signals. In the proposed FPGA design, the level of logic signal, which will be generated, is 3.3 V, this point must be taken into account. The power supplies, which are provided by DC/DC converters or bootstrap circuits, are required for the gate driver. The short circuit and over-voltage protection circuits must be added into the gate drive circuit. Additionally, the soft shutdown functionality must be also implemented to shut down the IGBT transistor safely during the fault occurrence. The gate driver, which is going to be designed, is a dual channel, for upper and bottom transistor in IGBT dual module. The gate driver will be compatible with the IGBT module parameters provided in [95].

3.4.1 Design of the Driver Stages of Proposed IGBT Gate Driver

Figure 3.6 depicts the block diagram of the driver stages for the upper and bottom transistor of dual IGBT module. These stages are divided into two channels: Upper channel for the upper transistor, and bottom channel for the bottom transistor. Each channel is composed

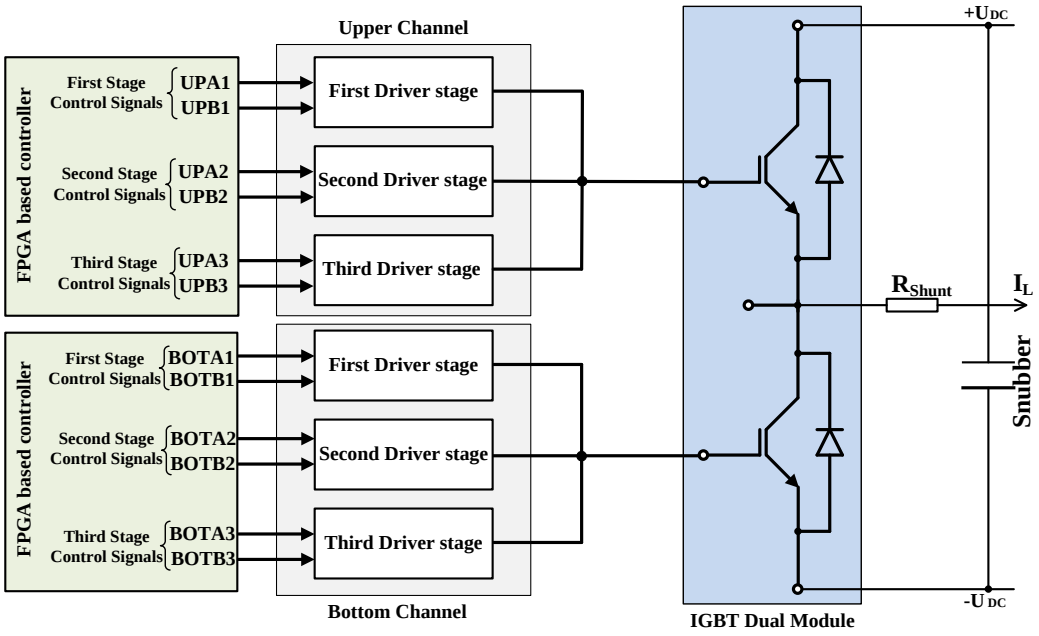


Figure 3.6: Block diagram of the parallel driver stages used in the proposed gate drive circuit.

of three parallel driver stages. The stages output of each channel feeds its own transistor in the dual IGBT module. These stages are responsible for the IGBT switching (turn-on, turn-off) during the operation. Figure 3.7 shows the driver stage structure in each channel where X indicates the stage number. The transistor P-channel MOSFET Q1X is used for

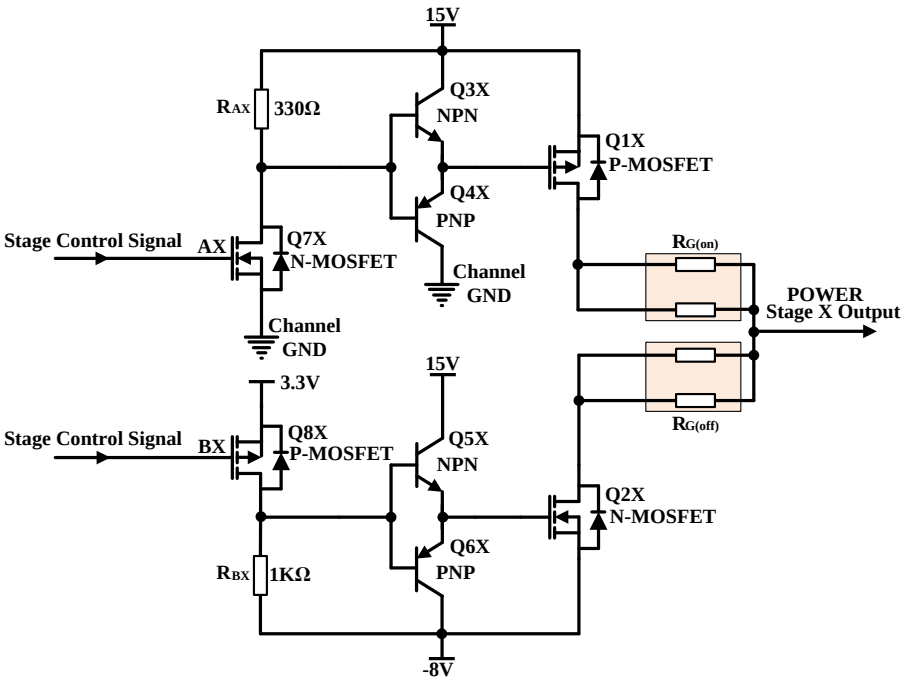


Figure 3.7: Schematic diagram of single driver stage in one channel.

the IGBT turning on, while the transistor N-channel MOSFET Q2X is used for the IGBT turning off. The turn-on voltage of the IGBT is approximately +15 V, and the turn-off voltage is about −8 V. Accordingly, the voltage drop along the charging/discharging path can be calculated as follows

$$\triangle V_{GE} = +\,15\,\mathrm{V} - (-8\,\mathrm{V}) = 23\,\mathrm{V}$$

The source pin of the transistor Q1X is connected to the positive supply of 15 V. Therefore, the Q1X is turned on, when its gate becomes more negative than the source voltage. On the other hand, the source pin of the transistor Q2X is connected to the negative supply −8 V. Therefore the Q2X is turned off, if its source becomes more negative than the gate voltage. Based on the simulation results[1], the output signal fed by the transistors Q1X and Q2X is shown in Figure 3.8, where the signal frequency is 5 kHz.

The maximum IGBT gate current I_G is determined according to the external resistors, where the external gate resistors $R_{G(on)}$ limit the gate current $I_{G(on)}$ during the turning on, and the resistors $R_{G(off)}$ limit the gate current $I_{G(off)}$ during the turning off. Moreover, the gate driver with this structure can control the du/dt and di/dt.

The Q1X switching (turn-on, turn-off) is controlled by the emitter follower (Q3X, Q4X) with single power supply. This follower consists of a complementary pair of bipolar transistors. Figure 3.9 depicts the gate signal used for Q1X switching, where the Q1X is turned on when the gate signal level is less than the source voltage ≈ 0 V, whereas it

[1]OrCAD Capture CIS is used for these simulation results

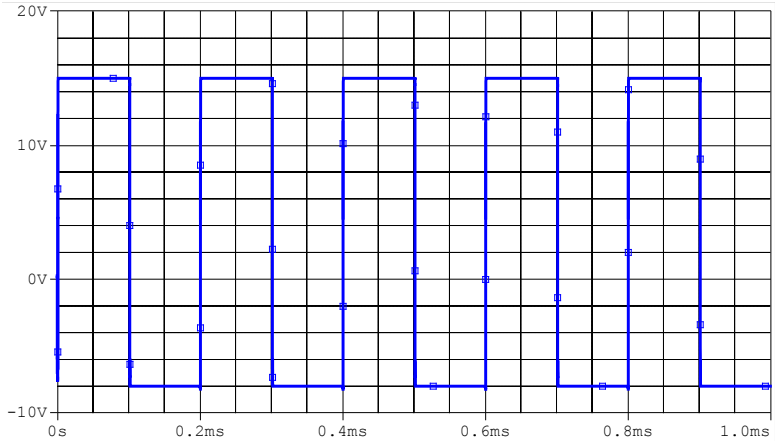


Figure 3.8: The output signal of one stage for the proposed IGBT gate driver.

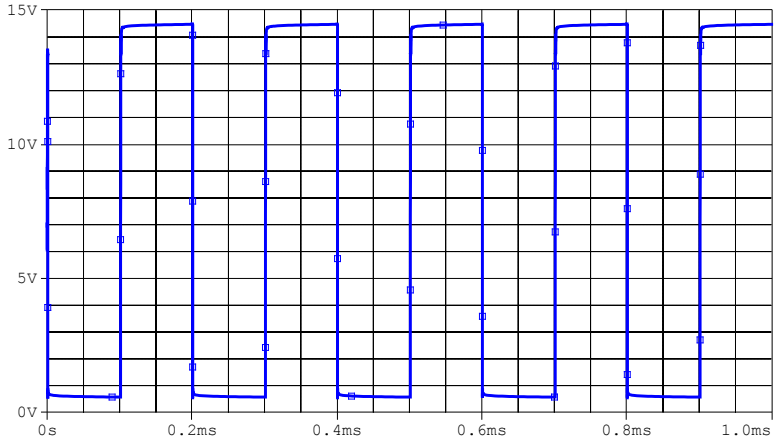


Figure 3.9: The gate signal of P-MOSFET Q1X.

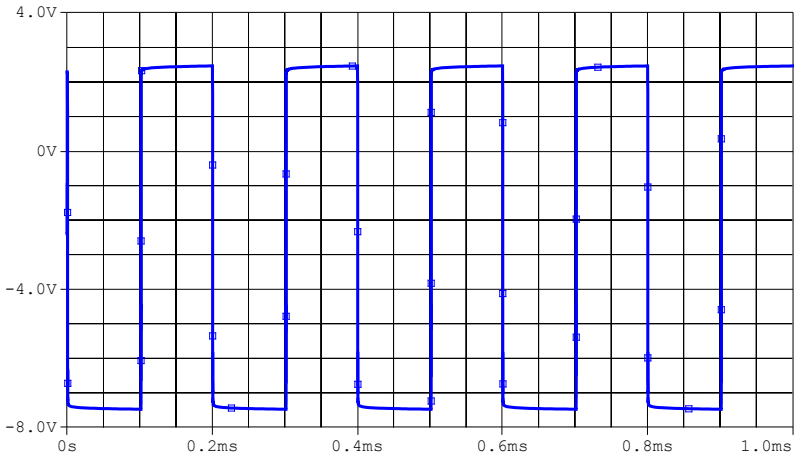


Figure 3.10: The gate signal of N-MOSFET Q2X.

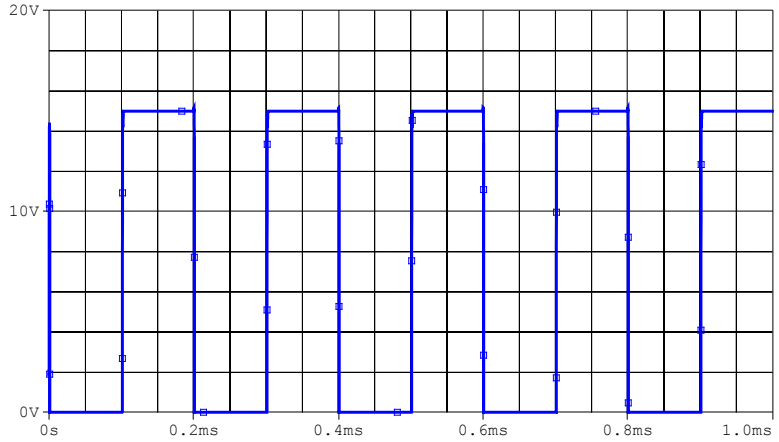


Figure 3.11: The base signal of the emitter follower (Q3X, Q4X).

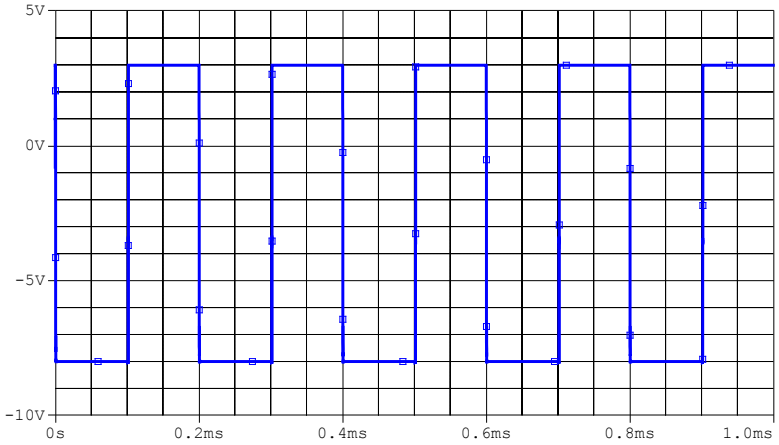


Figure 3.12: The base signal of the emitter follower (Q5X, Q6X).

is turned off when the gate signal level is equal to the source voltage ($15\,\mathrm{V} - V_{BE}$). In addition to control the Q1X gate, the emitter follower acts as a buffer between the input stage and the output stage. The base of emitter follower is controlled using the small signal N-channel MOSFET Q7X, as shown in Figure 3.7. When the Q7X is turned on, the base of the follower is connected to ground. Accordingly, the follower output signal is equal to the voltage between the emitter and base V_{EB}. The V_{EB} is typically equal to 0.7 V. On the other hand, if the Q7X is turned off, the base of the follower will be connected to the power supply $\approx 15\,\mathrm{V}$, and the follower output signal will be equal to $15\,\mathrm{V} - V_{BE}$. The base signal of this follower is shown in Figure 3.11.

The emitter follower, which controls the Q2X switching, is also composed of a complementary pair of bipolar transistors Q5X and Q6X. This follower is fed from the positive voltage +15 V for the collector of the NPN transistor Q5X and from the negative voltage −8 V for the collector of the PNP transistor Q6X. The output signal of the follower, which controls the Q2X gate, is shown in Figure 3.10. The small signal P-channel MOSFET Q8X

controls the base of the emitter follower, as illustrated in Figure 3.7. When the Q8X is turned on, the voltage applied on the follower base is approximately 3.3 V, and when it is turned off, the voltage applied on the follower base is −8 V. Then, the output signal of this stage is according to Figure 3.12.

The small signal transistors N-MOSFET Q7X, and P-MOSFET Q8X are considered as an input stage. They are controlled digitally by the FPGA controller. Each stage consists of two transistors controlled by different signals in the FPGA controller, as shown in Figure 3.13. This implies that the channel whether upper or bottom in the proposed gate driver is composed of six small signal transistors and each channel requires six signals coming from the FPGA for controlling the switching of these transistors. The structure of this gate driver allows controlling the gate resistors $R_{G(on)}$ and $R_{G(off)}$. As can be seen from Figure 3.13, the digital signals used for controlling the driver stages[2]have a delay time t_d. The delay time is not used for the first driver stage, while a delay time t_d is inserted for the other driver stages. Accordingly, the transistor $Q7_2$ is turned on after the t_{d1}, and the transistor $Q7_3$ is turned on after the t_{d2}, for controlling the $R_{G(on)}$ value during the IGBT turn-on. On the other hand, the transistor $Q8_2$ is turned off after the t_{d3}, and $Q8_2$ is turned off after the t_{d4}, for controlling the $R_{G(off)}$ values during the IGBT turn-off.

According to the datasheet of the IGBT module FF1000R17IE4 [95], and based on the Equation 2.18 in section 2.1.7, the peak value of current, which has to be provided by the first gate stage in each channel, for charging and discharging the gate during the IGBT switching, is

$$I_{GP(stage)} = \frac{15 + |-8|}{5 + 1.5} \approx 3.54\,\text{A}$$

Table 3.1 presents the complementary transistors used in the gate drive stages.

Complementary Transistor		**Voltage** (V_{DS}/V_{CE})	**Current** (I_{CM})
Si4564DY [91]	Q1X	40 V	40 A
	Q2X	−40 V	−40 A
PBSS4240DPN [88]	Q3,5X	40 V	3 A
	Q4,6X	−40 V	−3 A
DMG6602SVT [24]	Q7X	30 V	25 A
	Q8X	−30 V	−20 A

Table 3.1: The complementary transistors used in the proposed gate drive stages.

3.4.2 Design of the Power Supply System for the Proposed IGBT Gate Driver

As previously mentioned, the proposed gate driver turns on the IGBT with a positive voltage of 15 V to reduce the conduction losses, and it turns off the IGBT with a negative

[2]The transistors $Q7_1, Q7_2$ and $Q7_3$ are turned on, if the digital signal is high, and the transistors $Q8_1, Q8_2$ and $Q8_3$ are turned on when the digital signal is low.

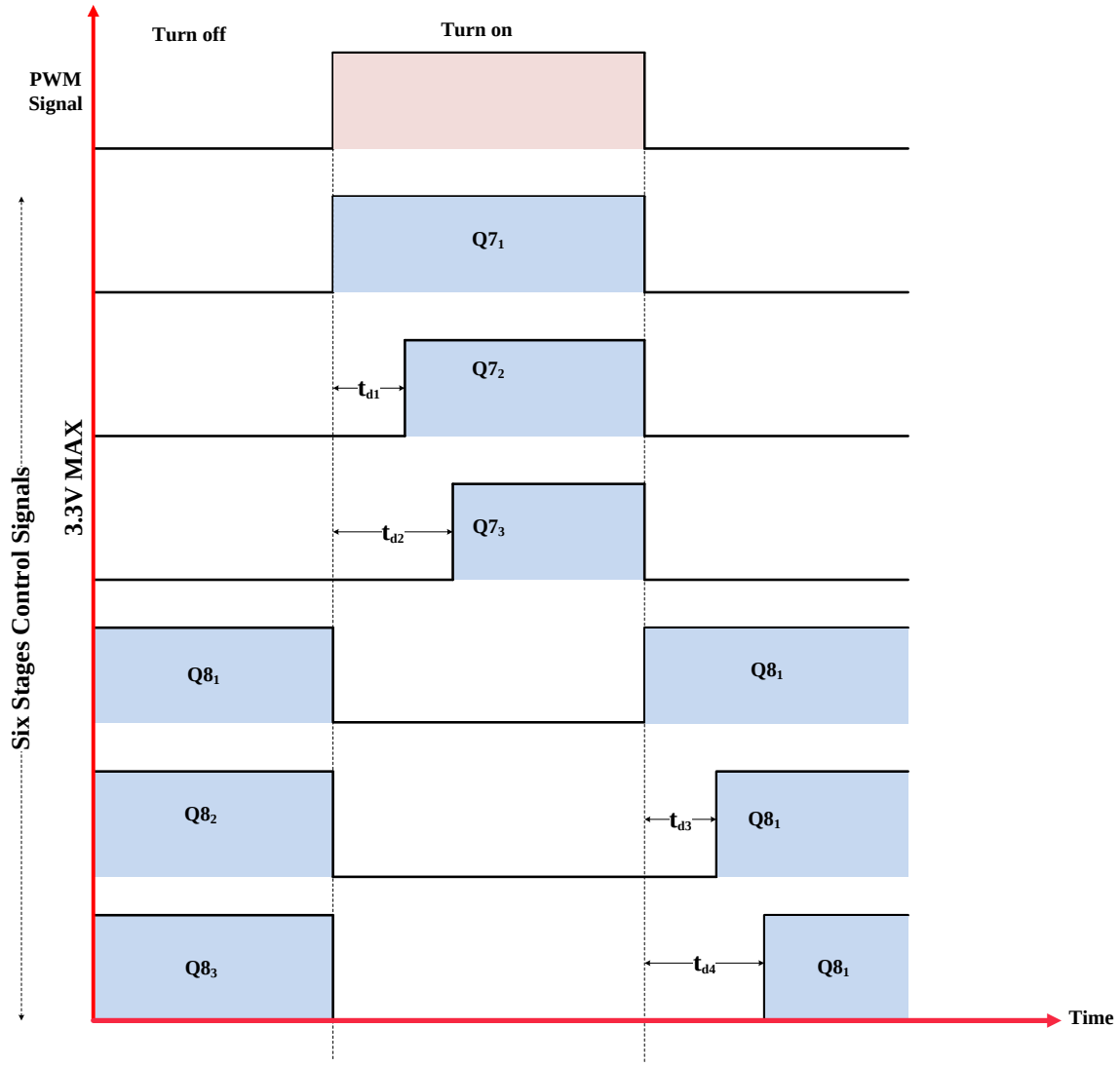


Figure 3.13: The digital signals used for controlling the input stages.

voltage of $-8\,\mathrm{V}$ for decreasing the turn-off losses which are caused by the tail current. Moreover, the negative voltage decreases the turn-off time.
Based on Equation 2.19 in section 2.1.7, the average value of the drive current I_G is calculated as follows

$$\begin{aligned} I_G &= 5 \cdot 10^3 \cdot 10 \cdot 10^{-6} \\ &= 50\,\mathrm{mA}. \end{aligned}$$

According to Equation 2.21 in section 2.1.7, it can be noted that the transmitted power P_d required to drive the IGBT switching is based on the gate voltage drop and gate charge as well as the switching frequency of the IGBT device. Using Equation 2.21, the required

DC/DC converter power can be calculated as follows

$$\begin{aligned} P_d &= 23 \cdot 5 \cdot 10^3 \cdot 10 \cdot 10^{-6} \\ &= 1.15\,\mathrm{W}. \end{aligned}$$

This value must be provided by the power supply system during the IGBT turn-on/turn-off. If an external gate emitter capacitor C_{GE} is added, an additional power $P_{C_{GE}}$ has to be provided by the power supply system. The $P_{C_{GE}}$ is calculated using Equation 3.1 as

$$P_{C_{GE}} = f_{sw} \cdot C_{GE} \cdot \triangle U_{GE}^2. \tag{3.1}$$

Generally, the values of C_{GE} are between 1 nF and 20 nF. Then according to Equation 3.1, the value ranges of the $P_{C_{GE}}$ are between 2.645 mW and 52.9 mW. Additionally, the power dissipation P_{dRs} in the resistors R_{AX} and R_{BX} must be provided by the power supply system, where each channel includes three resistors R_{AX} and three resistors R_{BX}. The P_{dRs} is calculated using Equation 3.2 as

$$P_{dRs} = 3 \cdot P_{dRAX} + 3 \cdot P_{dRBX} \tag{3.2}$$

$$= 3 \cdot \frac{\triangle V^2}{R_{AX}} + 3 \cdot \frac{\triangle V^2}{R_{BX}} \tag{3.3}$$

$$= 3 \cdot \frac{15^2}{330} + 3 \cdot \frac{(3.3 - (-8))^2}{1 \cdot 10^3}$$

$$= 2.045 + 0.38307 \approx 2.43\,\mathrm{W}.$$

Accordingly, the total power dissipation is calculated by Equation 3.4

$$\begin{aligned} P_{d(tot)} &= P_d + P_{C_{GE}} + P_{dRs} \\ &= 1.15 + 0.053 + 2.43 \\ &= 3.633\,\mathrm{W}. \end{aligned} \tag{3.4}$$

Figure 3.14 illustrates the block diagram of the power supply system used for the proposed IGBT gate driver, where two insulated DC/DC converters are used. Each one provides isolated output 16 V/1.6 A. The output of each converter feeds the following regulators:

- Positive regulator with output 15 V/0.4 A.
- Negative regulator with output −8 V/0.4 A.
- Positive regulator with output 5 V/2.5 A for the FPGA controller.

3.4.2.1 Design of the Positive and Negative Regulators for the Required Output voltages

The required output voltages (positive and negative outputs) are provided from the output of DC/DC converter using the step down regulator LM2596 [86]. The schematic circuit

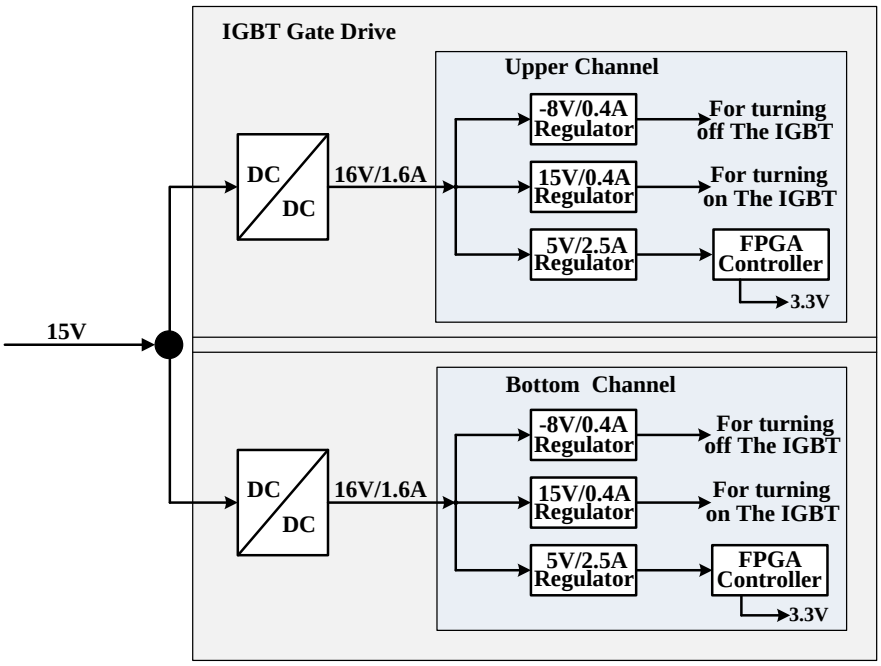


Figure 3.14: Block diagram of power supply in the proposed gate drive.

of the regulator LM2596, which is used for the positive outputs 5 V/2.5 A and 15 V/0.4 A, can be seen in Figure 3.15, and the schematic circuit of the negative outputs is shown in Figure 3.16 where the inverting mode is used for implementing the negative output voltage. According to the datasheet of the regulator LM2596 [86], Equation 3.5 is used to calculate the value of the resistor R_2.

$$R_2 = R_1(\frac{V_{out}}{V_{ref}} - 1) \tag{3.5}$$

where $V_{ref} = 1.235\,\mathrm{V}$ is the reference voltage. Equation 3.6 is used to choose the value of inductor L.

$$E \times T = (V_{in} - V_{out} - V_{sat}) \cdot \frac{V_{out} + V_D}{V_{in} - V_{sat} + V_D} \cdot \frac{1000}{150\,\mathrm{kHz}} \tag{3.6}$$

where $E \times T$ is a constant in $(\mathrm{V} \times \mu\mathrm{s})$, $V_{sat} = 1.16\,\mathrm{V}$ is the internal switch saturation voltage, and $V_D = 0.5\,\mathrm{V}$ is the diode forward voltage drop.

The value of $E \times T$ and the maximum load current value are used to identify the required inductor value (L). The peak current I_{peak} of the chosen inductor for the positive output voltage must be greater than the value($1.5\mathrm{I_{load}}$), whereas for the negative output voltage, the I_{peak} is calculated using Equation 3.7.

$$I_{peak} \approx \frac{I_{load} \cdot (V_{in} + |V_o|)}{V_{in}} + \frac{V_{in} \cdot t_{on}}{2L} \tag{3.7}$$

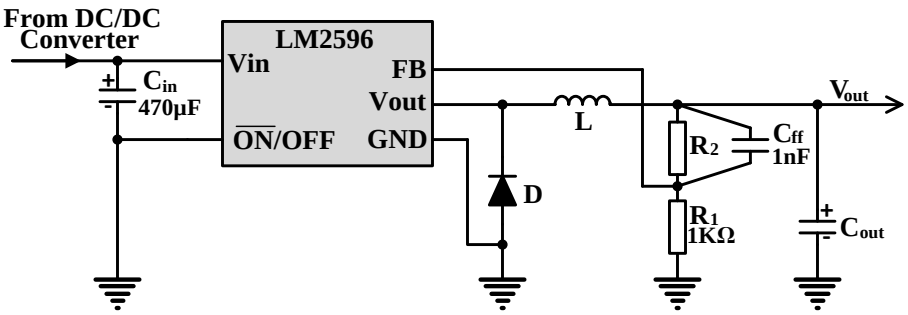


Figure 3.15: The schematic circuit of the positive regulators.

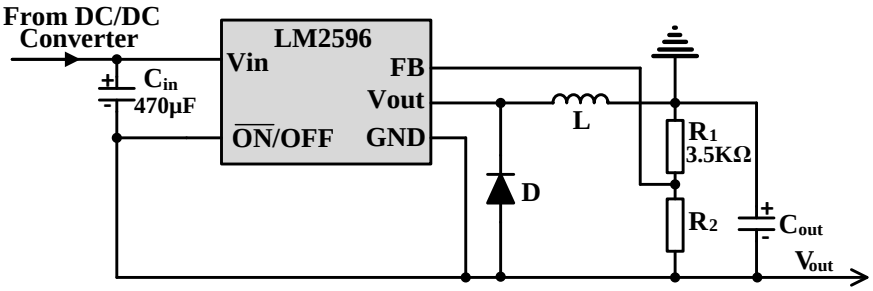


Figure 3.16: The schematic circuit of the negative regulators.

where t_{on} is the on time of the power switch which can be calculated by Equation 3.8

$$t_{on} = \frac{|V_o|}{V_{in} + |V_o|} \cdot \frac{1}{52\,\text{kHz}}. \tag{3.8}$$

The power dissipated $P_{D(reg)}$ by each regulator in the proposed power supply system can be calculated by Equation 3.9

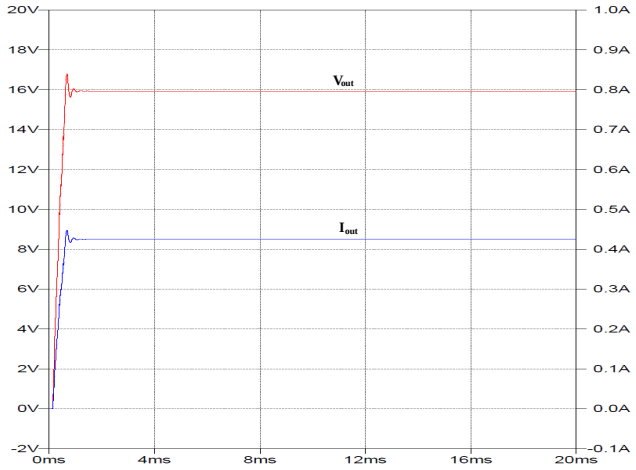
$$P_{D_{reg}} = (V_{in} \cdot I_Q) + \frac{I_{load} \cdot V_{sat} \cdot |V_o|}{V_{in}} \tag{3.9}$$

where I_Q is quiescent current which can be obtained from datasheet.

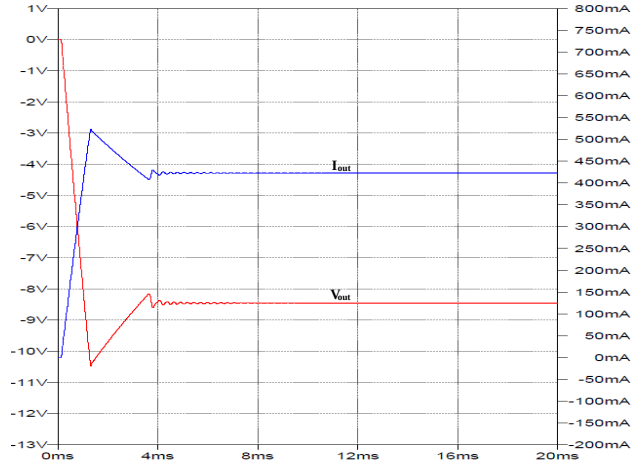
According to Equation 3.9:

- The dissipated power $P_{D_{reg1}}$ by regulator $15\,\text{V}/0.4\,\text{A}$ is $0.551\,\text{W}$.
- The dissipated power $P_{D_{reg2}}$ by regulator $-8\,\text{V}/0.4\,\text{A}$ is $0.348\,\text{W}$.
- The dissipated power $P_{D_{reg3}}$ by regulator $5\,\text{V}/2.5\,\text{A}$ is $1\,\text{W}$.

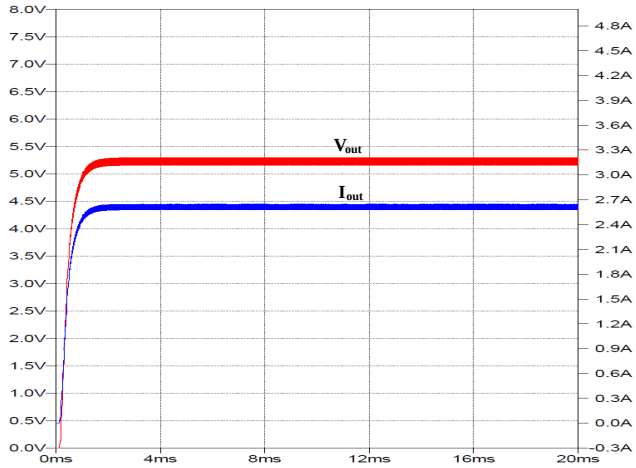
According to the above study, the total output power, which must be fed from the



(a) Output waveforms of regulator with 15 V.



(b) Output waveforms of regulator with −8 V.



(c) Output waveforms of regulator with 5 V.

Figure 3.17: Output waveforms of the regulators in the power supply system.

DC/DC converter, can be calculated by Equation 3.10:

$$P_{O(tot)} = \langle P_{D_{reg1}} + P_{reg1} \rangle + \langle P_{D_{reg2}} + P_{reg2} \rangle + \langle P_{D_{reg3}} + P_{reg3} \rangle \tag{3.10}$$

$$= 6.551 + 3.548 + 13.5 \tag{3.11}$$

$$\approx 23.6\,\text{W}.$$

Table 3.2 presents the values of components used in the design of regulators to obtain the required outputs.

V_{out}	I_{out}	C_{out}	R_2	L	D
15 V	0.4 A	47 μF	12 kΩ	HSRP1038A-150M(15 μH)	MBRS540T3G
5 V	2.5 A	200 μF	3 kΩ	SRP1038A-330M(33 μH)	MBRS540T3G
-8 V	0.4 A	470 μF	3 kΩ	MCSDRH125B-151MHF (150 μH)	MBRS540T3G

Table 3.2: The values of components required for positive and negative outputs of power supply system.

Based on the simulation results[3], the output waveforms of the regulators for the proposed IGBT gate driver can be seen in Figure 3.17.

In addition, the proposed gate driver requires a power supply with output voltage 3.3 V, which can be fed from the FPGA controller.

3.4.2.2 Design of the Insulated DC/DC Converters

The zero voltage zero current (ZVSZCS) push-pull resonant topology is used in the proposed power supply system for the gate drive circuit. Two ZVSZCS push pull resonant converters are provided in the design, where each converter feeds its own channel in the IGBT gate drive circuit with an output power 25.6 W and a current 1.6 A. As previously mentioned, the output voltage of each converter is applied to the inputs of the regulators used in each channel of the gate driver. Figure 3.18 depicts the schematic circuit of the push pull resonant converters with bridge rectifiers used for the proposed design.

The transformer used in the design is a toroidal transformer with a center taped primary winding and a single secondary winding. The resonant capacitor is placed on the secondary side of the transformer. The DC voltage is applied through the center taped primary of the transformer and two N-channel MOSFET transistors Q_1 and Q_2 convert the DC voltage into a pulsing voltage. The switches Q_1 and Q_2 are driven alternately by a control circuit with a high switching frequency $f_{sw} = 100\,\text{kHz}$ and a duty cycle $D = 45\,\%$. The Q_1 and Q_2 are turned on at zero voltage and turned off at zero current due to the resonant capacitor C_r and leakage inductance L_σ at the secondary side. The resonant frequency (f_r), at which the switching devices are operated, is given by Equation 3.12

$$f_r = f_{sw} = \frac{1}{2\pi\sqrt{L_\sigma C_r}}. \tag{3.12}$$

[3]LT Spice IV has been used for these simulation results

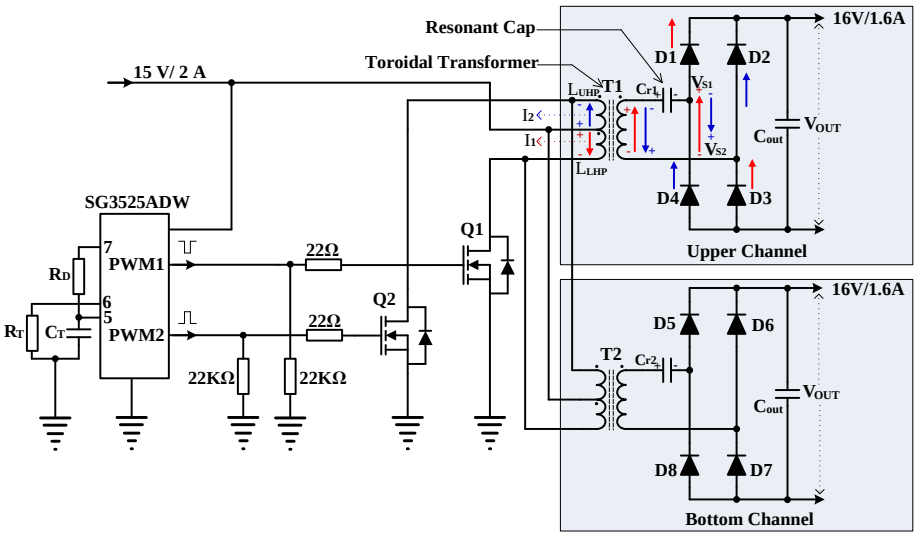


Figure 3.18: The schematic circuit of the push pull DC/DC converters used in power supply system.

When the Q_1 is turned on, a negative current flows through the lower half of the primary winding to ground, where the dot end will be more positive than the non-dot end. As a consequence, the generated magnetic field is converted into an electrical power by the secondary winding. Because of the voltage polarity on the primary winding, the dot end of the secondary winding is also more positive than the non dot end. As a result, the diodes D_1 and D_3 are forward-biased and the current flows through them. The transistor Q_1 is turned off, when the current through the resonant capacitor is equal to zero. During the time interval $D/f_{sw} < t \leq 0.5/f_{sw}$, both Q_1 and Q_2 are turned off and the stored energy in the lower half of the primary is discharged through the Q_1 freewheeling diode. On the other hand, the Q_2 is turned on, when the voltage across the resonant capacitor is equal to zero. Accordingly, a positive current flows through the upper half of the primary to ground. In this case, the non-dot end of the primary winding is more positive than the dot end. Similarly, the non dot end of secondary side will be more positive than the dot end. Therefore, the diodes D_2 and D_4 are forward-biased and the current flows through them.

As mentioned above, the switching frequency of the Q_1 and Q_2 is 100 kHz and the duty cycle is 0.45 %. Equation 3.13 calculates the switching period

$$\begin{aligned} T &= \frac{1}{f_{sw}} \\ &= \frac{1}{100} = 10\,\mu\text{s}. \end{aligned} \tag{3.13}$$

While the maximum on time T_{on} for each transistor can be calculated by Equation 3.14

$$\begin{aligned} T_{on} &= D \cdot T \\ &= 0.45 \cdot 10 = 4.5\,\mu\text{s}. \end{aligned} \tag{3.14}$$

Equation 3.15 allows calculating the number of primary turns in one part

$$N_{p(X)} = \frac{U_1 \cdot T_{on}}{2 \cdot B_{max} \cdot A_e} \tag{3.15}$$

where X indicates the part number of primary winding, A_e is the cross sectional area of the core in mm^2, and $B_{max} = 0.15\,T$ is the maximum operating flux density in Tesla. According to the datasheet of used core LJT 1606 C-CF 138, $A_e = 20\,mm^2$. Then, the number of primary turns in one part is

$$N_{p(X)} \approx 11\,\text{turns}.$$

Then, the number of the secondary turns can be calculated by Equation 3.16

$$\begin{aligned} N_s &= \frac{V_{out} + 2V_d}{V_{in}} \cdot N_{p(X)} \\ &\approx 13\,\text{turns} \end{aligned} \tag{3.16}$$

where $V_d = 0.7\,V$ is the rectifier on voltage.
The diameter of used wire can be calculated using Equation 3.17

$$\begin{aligned} D_W &= 2 \cdot \delta \\ &= 0.0418\,\text{cm} \end{aligned} \tag{3.17}$$

where δ is the skin depth in cm, and it can be calculated using Equation 3.18

$$\begin{aligned} \delta &= \frac{6.62}{\sqrt{f_{sw}}} \\ &\approx 0.0209\,\text{cm}. \end{aligned} \tag{3.18}$$

Then, the bare wire area A_W can be calculated by Equation 3.19

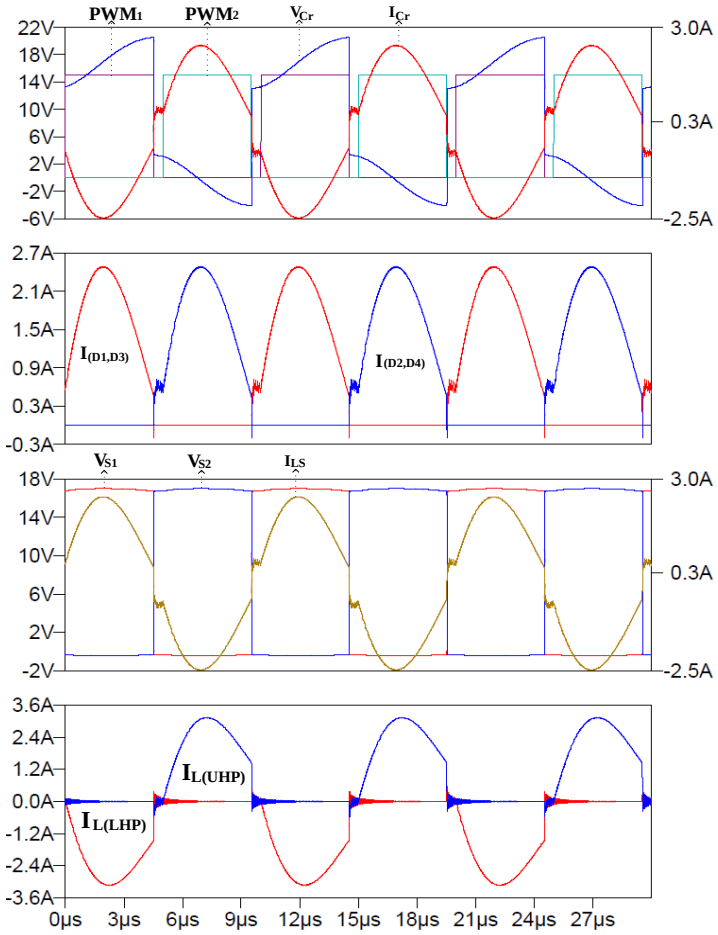
$$\begin{aligned} A_W &= \frac{\pi \cdot D_W^2}{4} \\ &\approx 0.00137\,cm^2. \end{aligned} \tag{3.19}$$

Based on the simulation results, the waveforms of the DC/DC converter are shown in Figure 3.20, Figure 3.19a depicts the waveforms during the DC/DC converter operation and the output waveforms (I_{out}, V_{out}) are shown in Figure 3.19b.

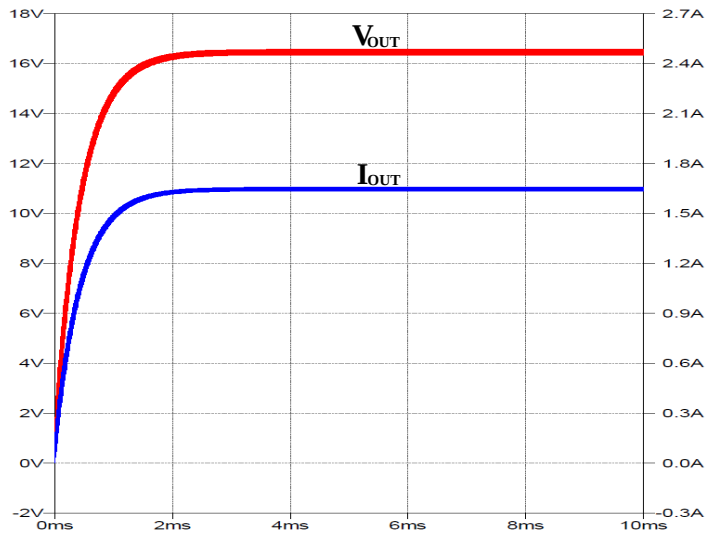
3.4.2.3 Design of the PWM Controller

The PWM controller used in the design is SG3525ADW [85], as shown in Figure 3.18. This controller contains an internal oscillator. The relationship between the PWM output frequency and the oscillator is defined by Equation 3.20

$$\begin{aligned} f_{osc} &= 2 \cdot f_{sw} \\ &= 200\,\text{kHz} \end{aligned} \tag{3.20}$$



(a) Waveforms of one push pull resonant converter during the operation.



(b) Output waveforms of one push pull resonant converter.

Figure 3.19: Waveforms of one push pull resonant converter.

where the f_{osc} is related to R_T, C_T and R_D by Equation 3.21

$$f_{osc} = \frac{1}{C_T(0.7 \cdot R_T + 3 \cdot R_D)} \tag{3.21}$$

where C_T is the timing capacitance in nF, R_T is the timing resistance in kΩ and R_D is the discharge resistance in Ω.
If $C_T = 1.5\,\text{nF}$ and $R_D = 0\,\Omega$, the f_{osc} can be set by R_T which is calculated by Equation 3.22

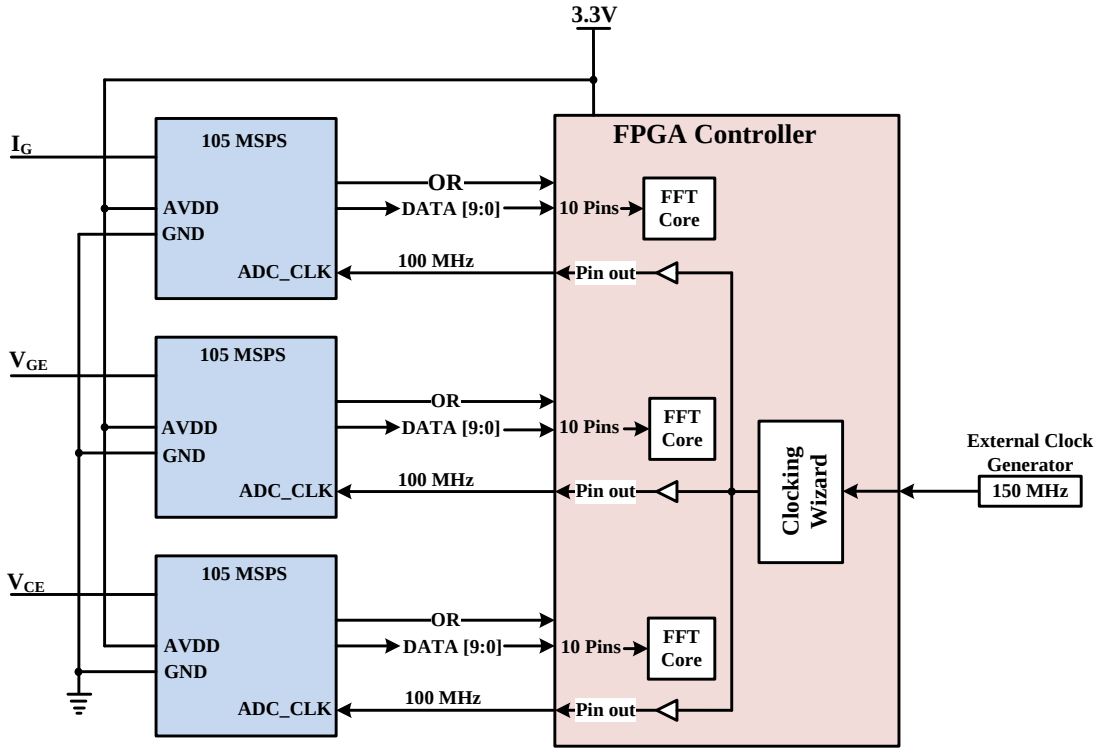
$$\begin{aligned} R_T &= \frac{1}{0.7 \cdot C_T \cdot f_{osc}} \\ &\approx 4.7\,\text{k}\Omega. \end{aligned} \tag{3.22}$$

3.4.3 The Proposed Analog to Digital Converters Design

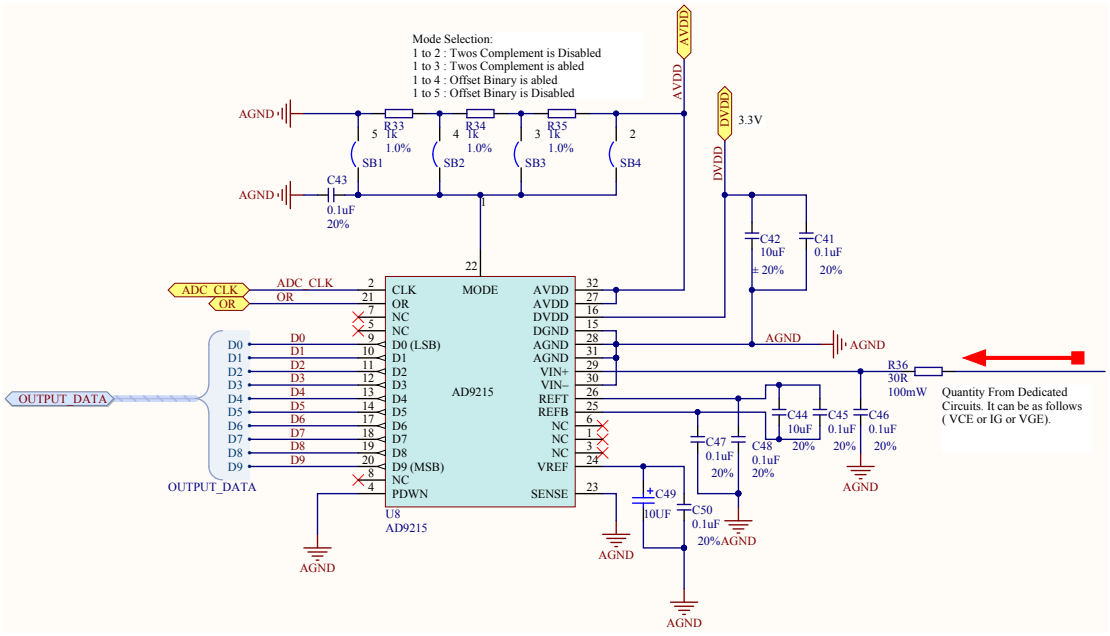
As previously mentioned, the important quantities, which are measured during the IGBT switching process (turn-on, turn-off), are I_G, V_{GE} and V_{CE}. The ADC devices convert the analog signals of the measured quantities to digital signals for analysis and processing. The quantitative evaluation determines the IGBT degree of degradation. Generally, the IGBT switching process is between $2 - 4\,\mu$s. Therefore, the ADC converters must be fast for digitizing the input signals during the switching process within this period. Assuming that the number of required samples for analysis and processing of the input signal is at least 100 samples[4], an ADC converter with 100 MSPS will be sufficient for this function. According to datasheet of the ADC converter AD9215 [23], it can be used for the proposed purpose. Figure 3.20a represents the block diagram of the ADC converters (AD9215) interface to the FPGA controller. The converted parallel data of each converter D[0:9] are wired to 10 pins in the FPGA. Additionally, the out of range (OR) is wired to one pin in the FPGA, this output bit indicates when the signal is beyond the selected input range. Figure 3.20b illustrates the schematic circuit of one ADC converter for one analog signal which is measured during the switching process. The ADC converter is operated from a single 3.3 V power supply which is provided by the FPGA controller. The clock input (ADC_CLK), which is used to control all internal conversion cycles, is generated by the FPGA using the clock wizard and buffers. The clock frequency must be at least 50 MHz.

A simple HDL code can be used to sample ADCs data at FPGA inputs. In addition to HDL code, the User Constraints File (UCF) is required to specify the pins location in the FPGA controller.

[4]These samples are acquired during the period between 2-5 μs which represents the transient phenomenon of the IGBT switching process.



(a) The Schematic blocks of the proposed analog to digital converters (ADCs).



(b) The schematic circuit of one ADC.

Figure 3.20: ADC Devices interface to the FPGA controller.

Chapter 4

FPGA Board Design for IGBT Control and Diagnosis

4.1 Introduction

The Field Programmable Gate Arrays (FPGA) devices share a common history with most Programmable Logic Devices(PLD). The first of this kind of devices was the Programmable Read Only Memory (PROM). Philips invented the Field-Programmable Logic Array (FPLA) in the 1970s. This consisted of two planes, a programmable wired AND-plane and the other plane as wired OR. Another class of electronic devices, Mask-Programmable Gate Arrays (MPGAs). These devices, which consist of transistor arrays, motivated the design of the FPGAs. The first FPGA goes to XILINX. The XC2064 was invented in 1985 consisting of 64 Configurable Logic Blocks with 3 Look Up Tables (LUTs), and now it has more than 10 million gates. There are two basic types of FPGAs, the first type could be reprogrammed such as SRAM, EPROM, and EEPROM, the second type is One-Time Programmable (OTP) such as anti-fuses, fuses, and PROM [41].

The software of FPGA is typically described in a Hardware Description Language (HDL). Two HDLs are used for describing the hardware based FPGA VHDL and Verilog. VHDL is dedicated to VHSIC Hardware Description Language. VHDL is used for circuit synthesis as well as circuit simulation. The main applications of VHDL are in the field of Programmable Logic Devices CPLDs and FPGAs and in the field of ASIC.

4.2 Proposed FPGA Board Design

Figure 4.1 shows the block diagram of the FPGA board used for the control and the diagnosis during the switching of the IGBT transistor.

As can be seen from Figure 4.1 the hardware features are:

- Kintex-7 XC7K70T-FBG484.

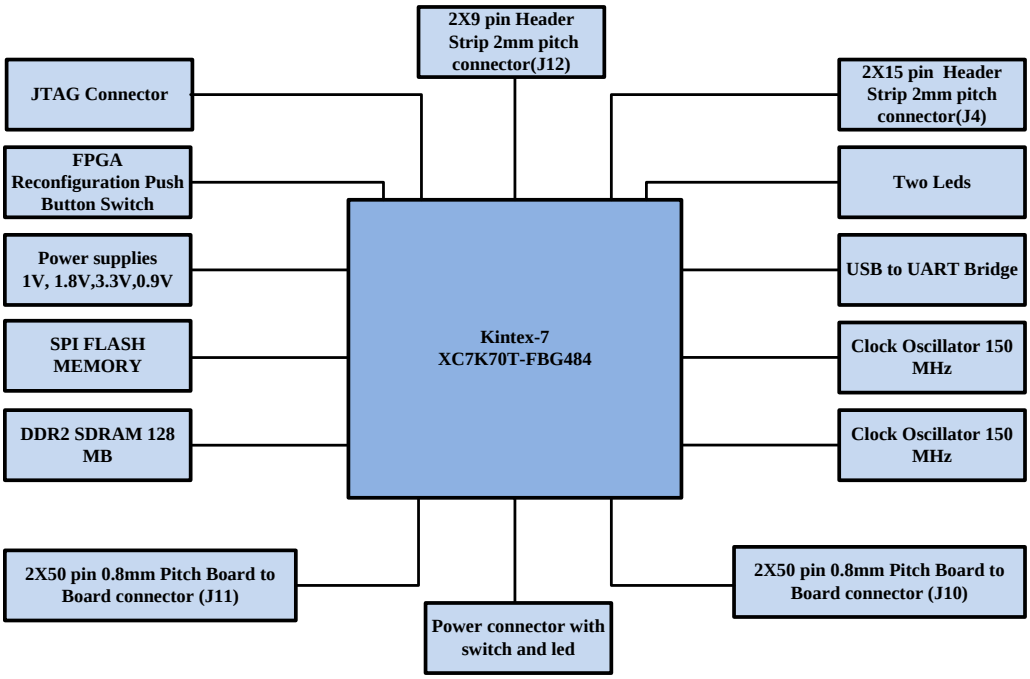


Figure 4.1: Block diagram of proposed FPGA design.

- DDR2 SDRAM (Micron MT47H128M8CF-25).
- SPI PROM (N25Q128 1.8/3.3 V).
- USB to UART Bridge (CP2103).
- Two clock crystal oscillators 150 MHz, 3.3 V (TXC 7W-150.000MBB-T OSC).
- Power Supplies 1 V/2.5 A, 1.8 V/1 A, 0.9 V/2.5 A, 3.3 V/1.5 A.
- JTAG.
- Two 2X50 pin 0.8 mm pitch board to board connectors (FX18-100S-0.8SH).
- Two leds.
- 2X9 pin header strip 2 mm pitch connector.
- 2X15 pin header strip 2 mm pitch connector.
- FPGA Reconfiguration push button switch.
- Power connector with switch and status led.

4.2.1 Description of Hardware Components

4.2.1.1 Kintex-7 XC7K70T-FBG484 Structures

Each FPGA device is split into I/O Banks to allow for flexibility in the choice of I/O standards.

Figure 4.2 shows the I/O and transceiver Banks for the XC7K70T. This FPGA device is one of 7 series FPGA families, it has two types of I/O Banks, high-performance (HP) and high-range (HR) I/O Banks. The HP I/O Banks are designed for achieving the requirements of high-speed memory and other chip-to-chip interfaces with voltages from 1.2 V to 1.8 V. The HR I/O Banks are designed to support a range of I/O standards with voltages from 1.2 V to 3.3 V.

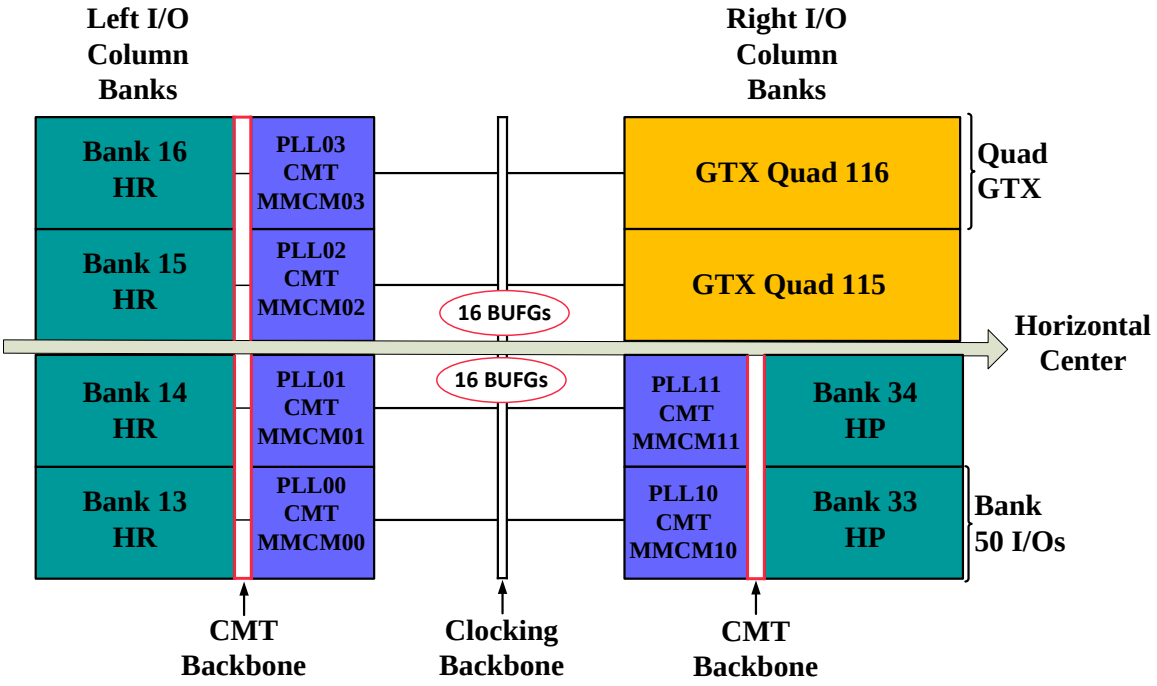


Figure 4.2: IO and Transceiver banks for XC7K70T [108].

Each Bank contains 50 I/O pins. These pins can be configured to both single-ended and differential I/O standards. The two pins at the ends of each Bank can only be used with single-ended I/O standards. The remaining pins could be used with either single-ended or differential standards. The single ended I/O standards can be used with integrated circuits such as LVCMOS, LVTTL, HSTL, PCI, and SSTL. Whereas the differential standards are used to interface with LVDS, Mini LVDS, RSDS, PPDS, BLVDS, and differential HSTL and SSTL.

Table 4.1 shows the features of the FPGA device Kintex-7 XC7K70t-3fbg484 which is used in the design. The FPGA slice contains four look-up tables (LUTs) and eight flip-flops. Digital Signal processing slice (DSP) contains a pre-adder, a 25X18 multiplier, an

device	Kintex-7 XC7K70t-3fbg484	
Size(mm)	23X23	
Ball Pitch	1	
Logic cells	65600	
Configurable Logic Blocks (CLBs)	slices	10250
	Max Distributed RAM(kb)	838
Block RAM Blocks	18Kb	270
	36kb	135
	Max(kb)	4860
I/O	HR	185
	HP	100
DSP Slices	240	
CMT	6	
PCIe	1	
GTXs	8	
XADC Blocks	1	
Total I/O Banks	6	
Max User I/O	300	

Table 4.1: Features of 7 series FPGA device (Kintex-7 XC7K70t-3fbg484).

adder, and an accumulator.

The Clock Management Tile (CMT) contains one mixed-mode clock manager (MMCM) and one phase-locked loop (PLL). The MMCM and PLL are used as a frequency synthesizer and a jitter filter for either external or internal clocks. MMCM and PLL usage was described in [112].

Figure 4.3 illustrates the architecture of clock resources in a clock region. As can be seen from Figure 4.3, the 7 series devices are divided into clock regions, the number of clock regions varies from eight to 24 clock regions. A clock region contains 50 CLBs per column, ten 36 k block RAMs per column, 20 DSP slices per column, and 12 BUFHs. The clock region requires 25 CLBs up and 25 CLBs down from the HROW. The horizontal clock row (HROW) is used for access to the global clock lines via the horizontal clock buffer (BUFH) in a single clock region. The BUFH can also be used as a clock enable circuit (BUFHCE) to enable or disable the clocks of single clock region. In addition, there are global clock buffers (BUFGs). BUFGs are driven indirectly by clock- capable inputs, then all BUFGs can drive all clock regions in 7 series devices. There are also I/O buffers (BUFIO) and regional clock buffers (BUFR). The BUFIO drives I/O clocking resources, whereas the BUFR drives I/O resources and logic resources. Moreover, 7 series FPGA device has a multi-region clock buffer (BUFMR). There are two BUFMRs in each Bank. The clock region spans one I/O Bank in the FPGA device. Every Bank contains Multi-region Clock Capable pin pairs (MRCC) and Single-region Clock Capable pin pairs (SRCC). MRCC and SRCC are directly driven by an external clock. This clock can be differential or single-

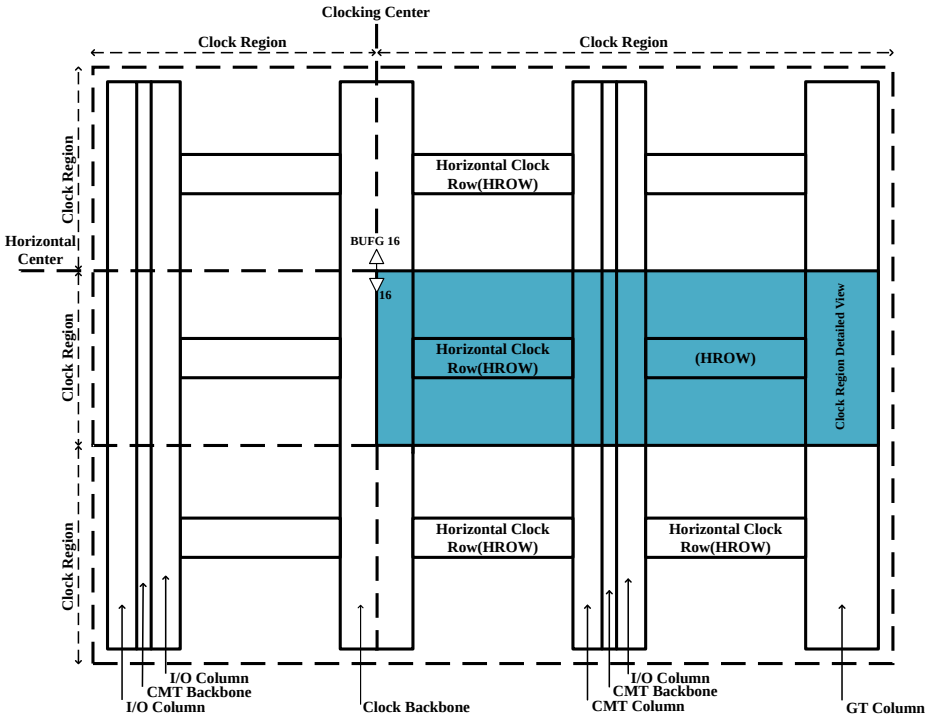


Figure 4.3: Architecture of clock resources in a clock region [112].

ended clock. This is dependent upon the application requirements. Then, MRCC and SRCC can drive BUFIOs, BUFRs, BUFMRs, and CMT. This depends on the location each of MRCC and SRCC in the FPGA device. Figure 4.4 shows in detail a diagram of the I/O clocking resources with buffers.
It can be seen from Figure 4.4 that every clock region has two MRCC pin pairs and two SRCC pin pairs. The pin pair is P side (master) and N side (slave). When an external single-ended clock is connected to SRCC or MRCC, it is connected to the P-side, whereas the N-side cannot be used as another single-ended clock pin, but it can be used as a user I/O. If MRCC and SRCC are not connected to an external clock, they are configured as I/O standards.

The VHDL and Verilog code is used for all clocking resource primitives. LogiCORE IP Clocking Wizard in ISE design tools helps to set up the clocking resource in the FPGA devices [105].

4.2.1.2 Power Supply Structure

The speed grades of kintex-7 FPGA devices are -3, -2, -1, and -2L. The FPGA device with speed grade (-3) has the highest performance. Table 4.2 shows the power supply voltages ratings on which it is depended to design the power supply system for the proposed FPGA board. When the power supply system of the FPGA device is turned on, the power on

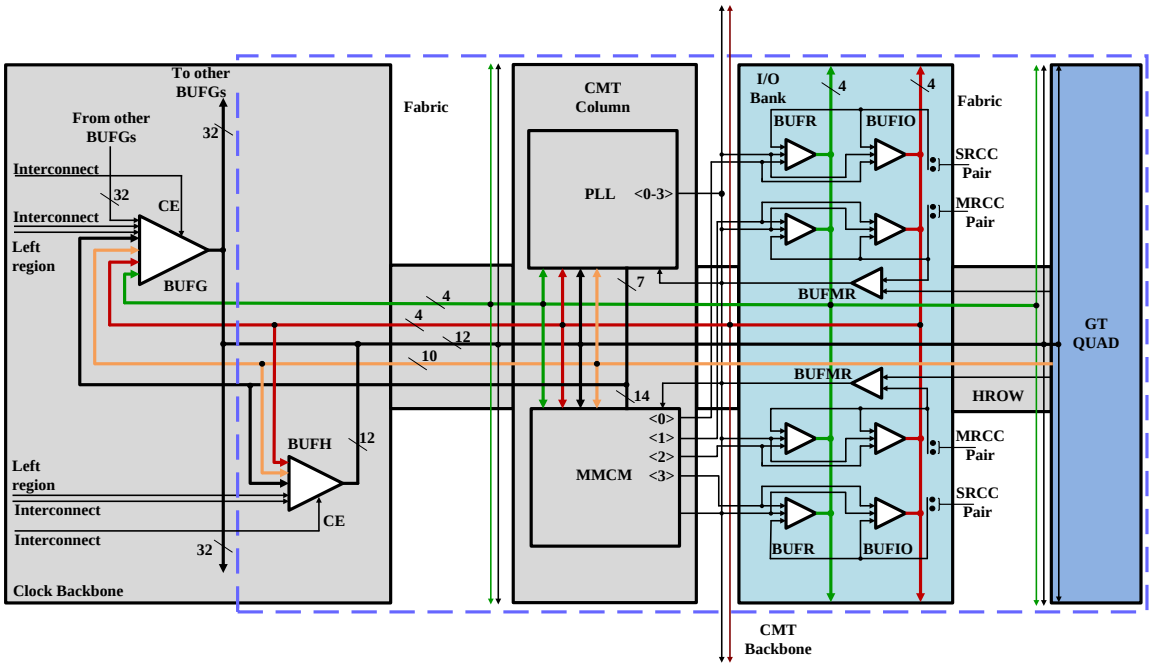


Figure 4.4: BUFG/BUFH/CMT/BUFR/BUFMR/BUFIO Clock region detail [112].

Symbol	Description	Min	Type	Max	Units
VCCINT	internal supply voltage	0.97	1.00	1.03	V
VCCBRAM	block RAM supply voltage	0.97	1.00	1.03	V
VCCAUX	Auxiliary supply voltage	1.71	1.8	1.89	V
VCCO	Supply voltage for HR I/O Banks	1.14	-	3.465	V
	Supply voltage for HP I/O Banks	1.14	-	1.89	V
XADC					
VCCADC	XADC supply relative to GNDADC	1.71	1.8	1.89	V
VREFP	Externally supplied reference voltage	1.20	1.25	1.3	V

Table 4.2: Power supply voltage ratings for proposed FPGA board.

sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to draw a minimum current, whereas the power off sequence is the reverse of the power on sequence [113]. Therefore, the supplies V_{CCINT} and V_{CCBRAM} are designed with soft-start 1 ms, V_{CCAUX} with soft-start 1.5 ms and V_{CCO} with soft-start 2 ms. Figure 4.5 shows the power supplies structure of FPGA device Kintex-7 XC7K70t-3fbg484. V_{CCINT} and V_{CCBRAM} are powered by the same supply, because they have the same voltage levels 1 V/2.5 A. The high range I/O Banks are powered by the supply with 3.3 V/1.5 A and they have the same voltage levels. The high performance I/O Banks are powered by a supply with 1.8 V/1 A.

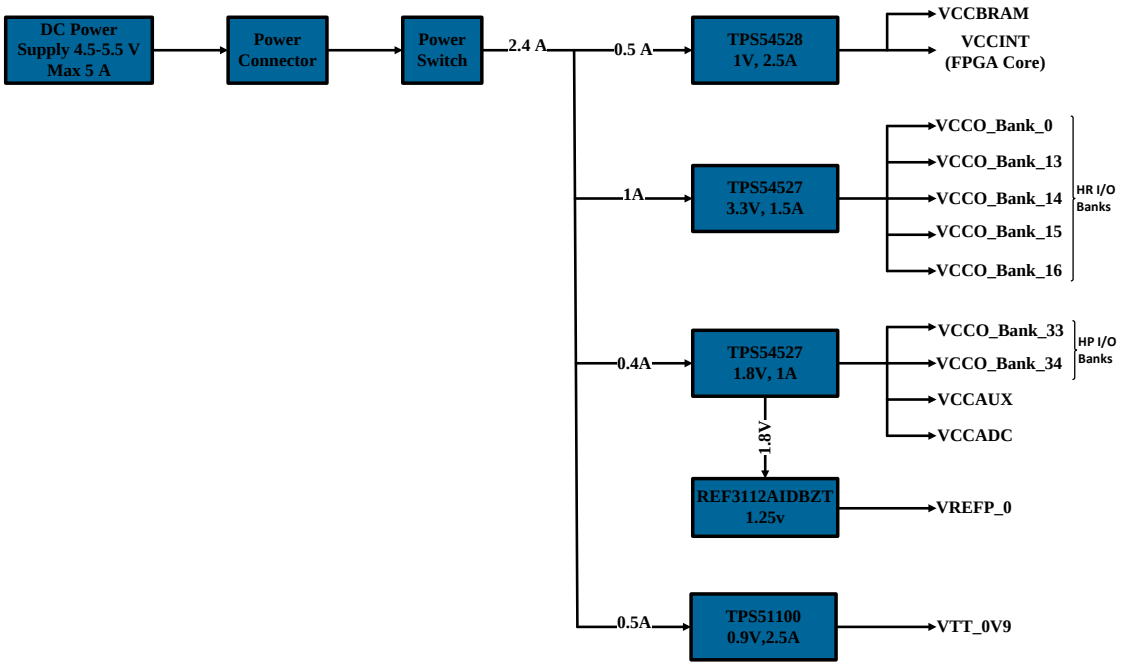


Figure 4.5: Power supplies block diagram of Kintex-7 XC7K70t-3fbg484.

4.2.1.3 System Clock Sources

Figure 4.6 shows the system clock circuit which is used for clocking the FPGA device. Two 150 MHz single-ended clocks are used, the first one is connected to the FPGA MRCC

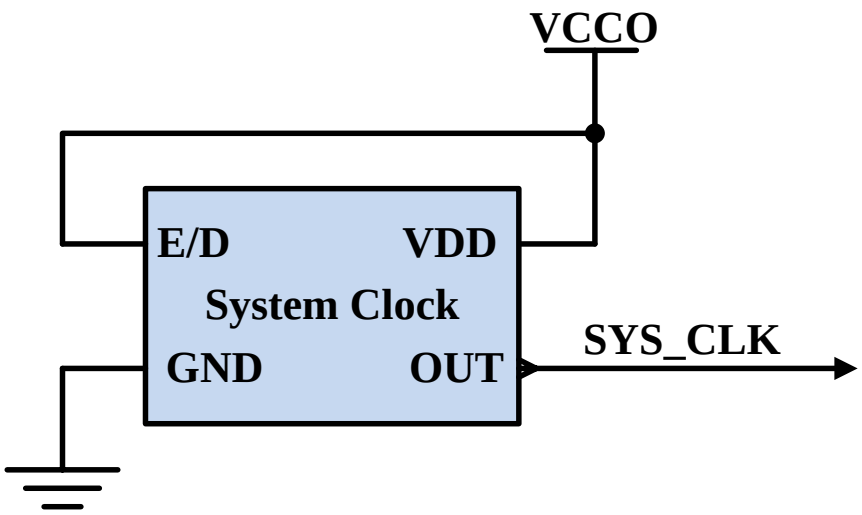


Figure 4.6: Schematic circuit of the clock crystal oscillator.

clock input on Bank 14 and it is named SYS_CLK2, and the second one is connected to the FPGA MRCC clock input on Bank 34 and it is named SYS_CLK1. Table 4.3 shows the FPGA pins to which the clock sources are wired and the output type of signals.

Clock Input Name and Frequency	FPGA Pin	FPGA Bank	I/O Standard
SYS_CLK1 /150 MHz	T4	Bank 34	CMOS_18
SYS_CLK2 /150 MHz	N18	Bank 14	CMOS_33

Table 4.3: Clock sources table.

4.2.1.4 FPGA Configuration

Xilinx 7 series FPGA devices can be configured by loading the bitstream file into an internal memory. The configuration data (bitstream) can be loaded either by an external nonvolatile memory device or via an external intelligent source, such as a microprocessor, DSP processor, or microcontroller. In addition, the configuration data can be downloaded from a PC through a cable to the JTAG port of the FPGA device. The FPGA devices must be reconfigured after it is turned off because the configuration data is stored in CMOS configuration latches (CCLs). There are special configuration pins that are used to load the configuration data into the FPGA device.

7 series FPGA devices have five configuration modes [107]. The proposed FPGA board supports two configuration modes:

- JTAG/boundary-scan configuration mode: this mode is always available, regardless of the mode pin settings.
- Master Serial Peripheral Interface (SPI) flash configuration mode (x4): this mode supports reading from an SPI flash using a data bus up to four bits wide.

The specific configuration mode is selected by input pins M[2:0], which are available in Bank 0. The $M2$, $M1$, and $M0$ mode pins are wired either to the ground or to the $VCCO\_0$. Bank 0 is always a part of each configuration interface, whereas Bank 14 and Bank 15 contain multi-function pins, which are used in a few of the configuration modes.

Table 4.4 presents the pins which are involved in the configuration interfaces of proposed FPGA board. Configuration Bank Voltage Select (CFGBVS) determines the I/O voltage operating range and the voltage tolerance for the dedicated configuration bank 0. Program Bar (PROGRAM_B) is used to reset the FPGA configuration.

Figure 4.7 shows the configuration pins schematic of Bank 0 used in the configuration modes of the design. PROGRAM_B is connected to 4.7 kΩ pull-up resistor to VCCO_3.3V to ensure a stable high input. In addition, this dedicated pin is wired to ground through a push-bottom switch to achieve manual configuration reset. Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI), and Test Data Output (TDO) are connected to JTAG chain. Initialization pin (INIT_B) is connected to a 4.7 kΩ pull-up resistor to VCCO_3.3V to ensure clean Low-to-High transitions. Done pin (DONE) is wired to VCCO_3.3V through a 330 Ω.

Pin Name		I/O Pin	JTAG Mode	Master SPI Mode (X4)
	BANK 0	H7	M0_0=1	M0_0=1
		H6	M1_0=0	M1_0=0
		J5	M2_0=1	M2_0=0
		G7	CCLK_0	CCLK_0
		K7	TCK_0	TCK_0
		L6	TMS_0	TMS_0
		J6	TDO_0	TDO_0
		K6	TDI_0	TDI_0
		K6	TDI_0	TDI_0
		M6	PROGRAM_B_0	PROGRAM_B_0
		M7	CFGBVS_0	CFGBVS_0
		P6	DONE_0	DONE_0
	BANK 14	K18	PUDC_B_14	PUDC_B_14
		H18	-	D00_MOSI_14
		H19	-	D01_DIN_14
		G18	-	D02_14
		L16	-	D03_14
		F19	-	FCS_B_14

Table 4.4: Configuration mode Pins used in proposed FPGA board.

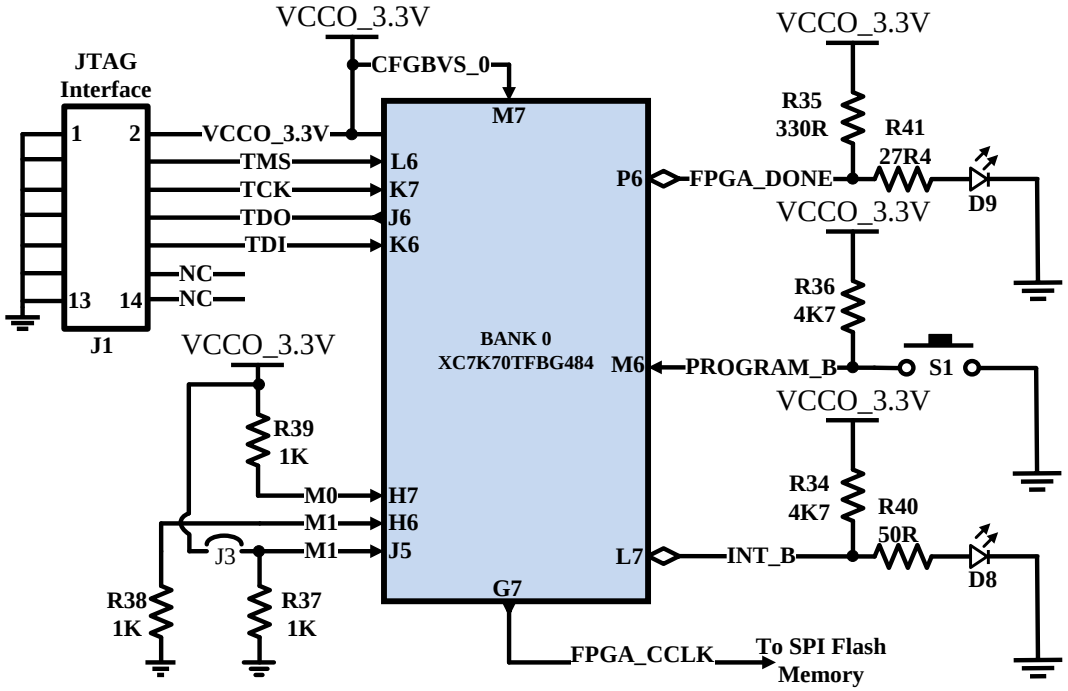


Figure 4.7: Configuration mode pins circuit of bank 0 in proposed FPGA board.

4.2.1.5 Quad SPI Flash Memory 128 Mb

The proposed FPGA board has a 128 Mbit quad SPI Flash Memory used for the configuration and for the data storage. QSPI flash has six lines to enable 4-bit data width. Accordingly, the configuration time is decreased. Figure 4.8 shows the QSPI flash circuit. The pin C is the input clock that provides the timing of the serial interface. This clock signal is driven by the configuration clock (CCLK) illustrated in Figure 4.7. DQ[0:3] are bidirectional input and output data signals between the FPGA device and the SPI flash memory. Series resistors with value 15 Ω are added through path of DQ[0:3] to eliminate reflections and overshoot which could damage the FPGA device. The chip select pin S# is driven by FCS_B. When S# is HIGH, the device is deselected and DQ[0:3] are at High-Z.

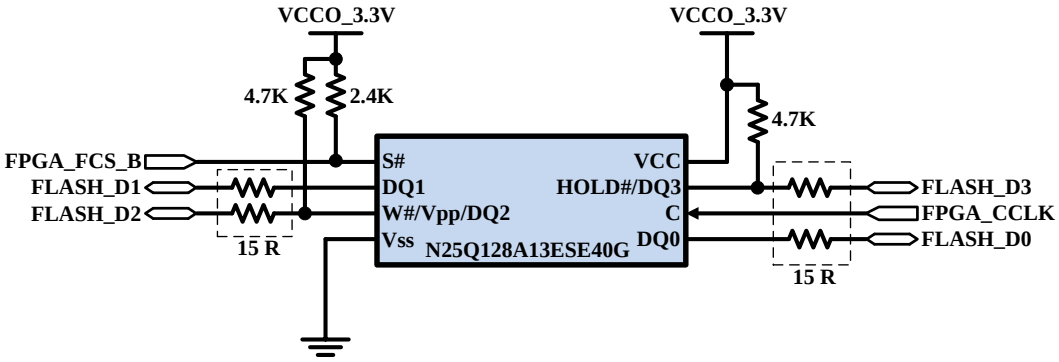


Figure 4.8: QSPI flash memory circuit.

When S# is low, the SPI flash is enabled, placing it in active mode. The source voltage V_{CC} is fed from the voltage VCCO_3.3V. The SPI flash is placed on the back side of the proposed FPGA board. Table 4.5 shows the connections between the SPI device and the FPGA device.

SPI FLASH Pin	NET Name	FPGA Pin	I/O Standard
DQ0	FLASH_D0	H18	LVCMOS33
DQ1	FLASH_D1	H19	LVCMOS33
DQ2	FLASH_D2	G18	LVCMOS33
DQ3	FLASH_D3	YF19	LVCMOS33
C	FPGA_CCLK	G7	LVCMOS33
S#	FPGA_FCS_B	L16	LVCMOS33
VCC	VCCO_3.3V	NA	–
VSS	GND	NA	–

Table 4.5: Quad SPI flash memory connections to FPGA pins.

The bitstream is stored in the SPI flash memory using an indirect programming method.

IMPACT programming software is used to program the SPI flash devices.
As mentioned above, M[2:0] determines the FPGA configuration mode. When $M[2:0] = 001$, the FPGA device is configured from the SPI flash memory and it begins to generate clocks on CCLK at the configuration clock frequency (f_{CCLK}). When the SPI flash device clocks data-out on the falling edge and the FPGA device clocks data-in on the rising edge, a half cycle will be lost. As a result, the maximum configuration clock frequency is decreased. In order to improve the data transfer, the FPGA device can be modified for clocking data-in on the falling edge. The maximum configuration clock frequency can be determined using Equation 4.1

$$f_{MCCLK} = \frac{1}{T_{SPITCO} + T_{SPIDDC}} \tag{4.1}$$

where f_{MCCLK} is maximum configuration clock in MHz, T_{SPITCO} is SPI clock to out in ns, and T_{SPIDDC} is FPGA data setup time in ns.
If f_{MCCLK} is required, it must be checked due to the wide of configuration clock tolerance (TMCCKTOL) that can be equal to $\pm 50\,\%$. Equation 4.2 is used to check the maximum configuration clock at the maximum configuration rate.

$$f_{M\_CCLK\_Checked} = MaxConfigRate \times (1 + TMCCKTOL_{MAX}) > f_{MCCLK} \tag{4.2}$$

where $MaxConfigRate$ is the maximum configuration rate in MHz, and $TMCCKTOL_{MAX}$ is the maximum configuration clock tolerance in %. If $f_{M\_CCLK\_Checked}$ is less than f_{MCCLK}, it is recommended use External Master Configuration Clock (EMCCLK) that is available in Bank 14. Table 4.6 summarizes the configuration switching characteristics which are used for f_{MCCLK} calculations.
Using Equation 4.1 and Table 4.6, the f_{MCCLK} can be calculated

Config_Parameter	**MAX Value**	**Unite**
T_{SPITCO}	7 under 30 pF	ns
	5 under 10 pF	ns
T_{SPIDDC}	3	ns
MaxConfigRate	66	MHz
$TMCCKTOL_{MAX}$	± 50	%

Table 4.6: Configuration parameters for f_{MCCLK} calculation.

$$f_{MCCLK} = \frac{1}{7+3} = 100\,\text{MHz}$$

From Equation 4.2, $f_{M\_CCLK\_Checked}$ can be calculated:

$$f_{M\_CCLK\_Checked} = 66 \times 1 + 50\,\% = 99\,\text{MHz} < 100\,\text{MHz}.$$

Accordingly, if the maximum configuration clock is required, an external master configuration clock must be used. The EMCCK pin in Bank 14 isn't wired on the proposed

FPGA board. Therefore, the FPGA's internal oscillator is used for the configuration. The configuration bitstream length of the proposed FPGA device is 24,090,592 bits [107]. If the configuration rate 40 MHz is chosen, the needed time for the configuration is calculated from Equation 4.3.

$$T_{config} = \frac{L_{ConfigBits}}{ConfigRate \times data_{width}} \tag{4.3}$$
$$T_{config} = \frac{24,090,592}{40,000,000 \times 4} \approx 150.6\,\text{ms}.$$

4.2.1.6 XADC Design

The Xilinx analog to digital converter (XADC) is an integrated block that is available in 7 series FPGA devices. The XADC is composed of a dual 12 bit, 1 Mega sample per second (1MSPS) ADCs, on-chip voltage, and temperature sensors. Figure 4.9 depicts the structure of the ADC in the FPGA device which is used in the design. The single dedicated

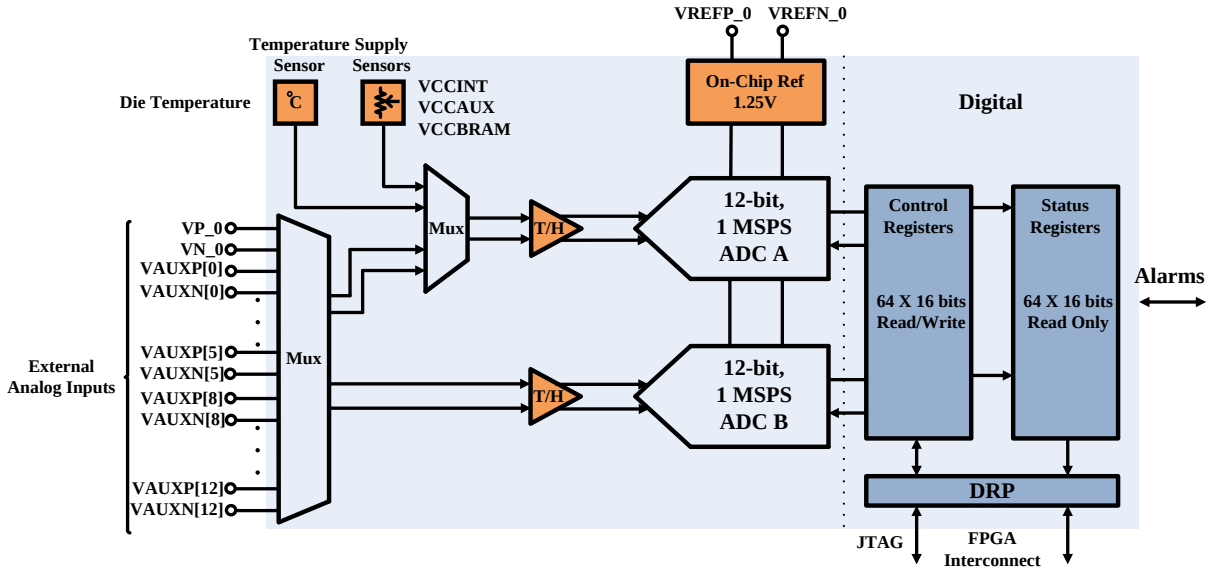


Figure 4.9: XADC block diagram in Kintex 7 [111].

analog input pair (VP/VN) is available in the Bank 0, and the other analog input channels are distributed in the Bank 15. The on-chip sensors and the external analog inputs are multiplexed and connected to two ADCs through a track and hold amplifier (T/H). These ADCs can be configured to sample in continuous or event driven modes. The status registers store the conversion data. These registers are accessible via the FPGA interconnect using a 16-bit synchronous read and write port called the dynamic reconfiguration port (DRP). The ADC conversion data is also accessible via the JTAG interface. The JTAG is directly accessed using the ChipScpoe Pro tool. Alarm signals can be generated by the

XADC on the logic outputs when an internal sensor measurement exceeds some defined thresholds.
Figure 4.10 shows the required circuit for XADC in the proposed FPGA board. The external voltage reference with 1.25 V is used to increase the measurement accuracy and thermal drift. The ferrite bead L3 is used for filtering the voltage reference input VIN, and L4 is used to isolate the analog ground GND_ADC and system ground GND.

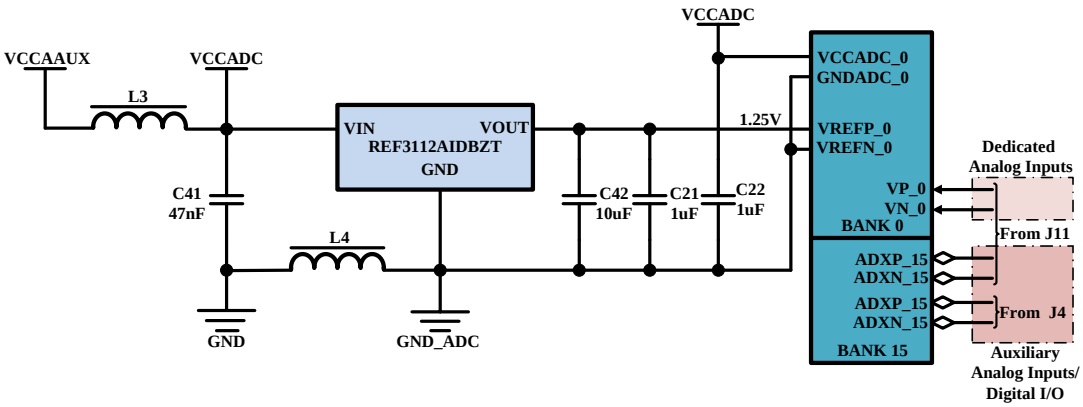


Figure 4.10: XADC external voltage reference circuit with analog inputs.

The dedicated analog input pair (VP_0/VN_0) provides a differential analog input. This analog input channel is very flexible and support multiple analog input signal types. The auxiliary analog inputs (ADxP_15/ADxN_15) are a multi-function pins witch can be used as analog inputs or as digital I/O. These analog input channels are also very flexible and support multiple analog input signal types. The auxiliary analog input channels do not require any User Constraint File (UCF) or pin locations.

The proposed FPGA board supports both the internal sensor measurements and the external measurement capabilities of the XADC. From Figure 4.9, the Internal measurements are die temperature, VCCINT, VCCAUX, and VCCBRAM. For external measurements, the XADC header (J4) shown in Figure 4.11 is used. This header can be used to connect analog inputs to the auxiliary analog input channels VAUXP[2]/VAUXN[2], VAUXP[3]/VAUXN[3], VAUXP[4]/VAUXN[4], VAUXP[8]/VAUXN[8], VAUXP[9]/VAUXN[9], VAUXP[10]/VAUXN[10], VAUXP[11]/VAUXN[11]. The header also provides four digital general purpose input/output (GPIO) which can be used to generate control signals from the FPGA device. In addition, the external measurements can be achieved using the board to board connector (J11). The header J11 can be used to connect analog inputs to the FPGA dedicated channel VP_0/VN_0, and to the auxiliary analog input channels VAUXP[0]/ VAUXN[0], VAUXP[1]/VAUXN[1], VAUXP[12]/VAUXN[12]. Figure 4.12 illustrates the pins connection of J11 to the FPGA dedicated channel and the auxiliary analog input channels.

The analog anti-aliasing filter (AAF) is used to provide a cutoff frequency which removes unwanted signals from the XADC inputs. To prevent aliasing and maximize bandwidth

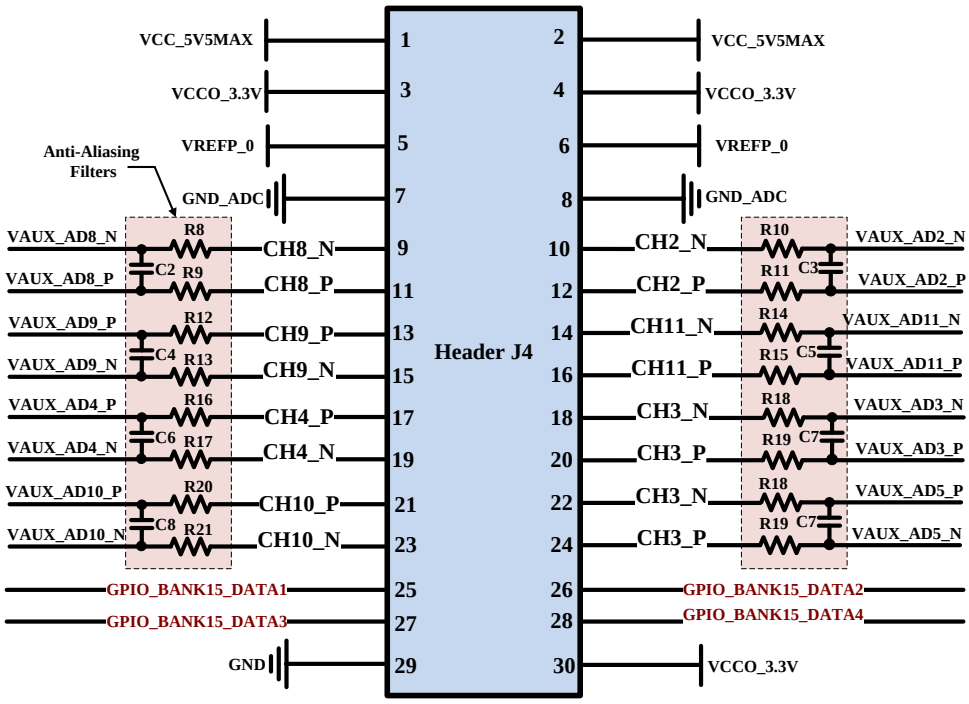


Figure 4.11: XADC Header (J4).

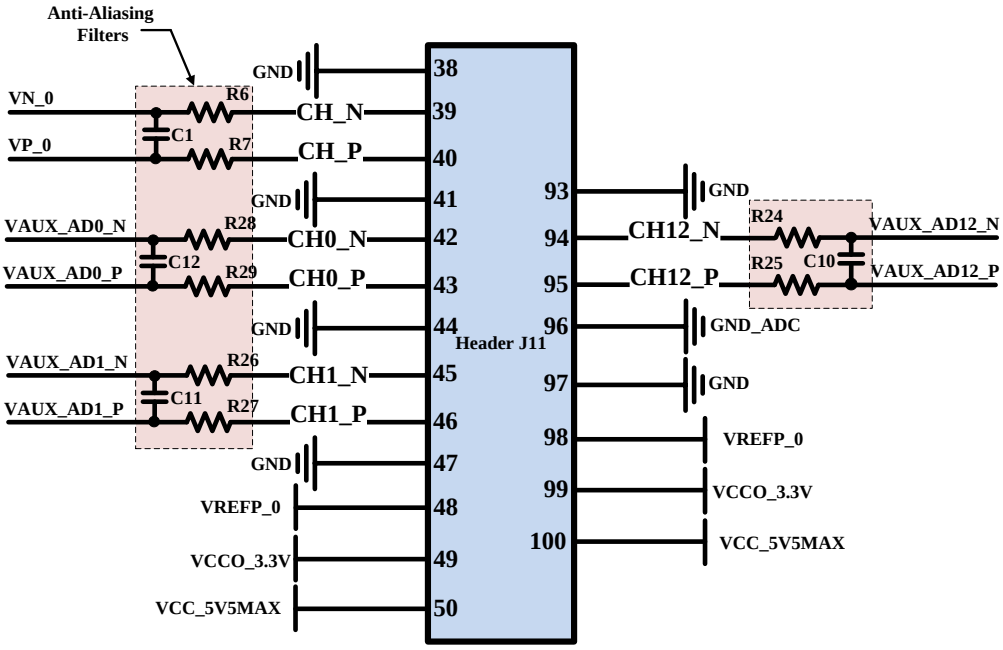


Figure 4.12: Pins of Header (J11) used to provide analog inputs to FPGA.

with a Nyquist rate (non-oversampling), the AAF typically must have a flat response up to about $(0.45 \cdot f_S)$ and it has to attenuate all frequencies above $(0.5 \cdot f_S)$ to level bellow the noise floor. In general, it is not possible to design an AAF with such features [67], because the design will be more difficult and expensive, requiring precision components and additional board space.

As can be seen in Figure 4.11 and Figure 4.12, the AAF is composed of resistors and capacitors. The values of AAF components are dependent on the use cases:

- Voltage monitoring.
- Measuring a current.
- Measuring the output from a sensor.
- External multiplexer mode.

The XADC can be operated in an unipolar mode or in a bipolar mode. The nominal analog input range is $1\,V_{P-P}$. In the unipolar mode, the analog inputs produce a full scale code of FFFh when the input signal value is equal to 1 V. In this mode, the voltage on VP_0 must always be positive and VN_0 is connected to GND_ADC. A common mode voltage can be used on VN_0 and its value can vary from 0 V to +0.5 V. In the bipolar mode, a two's complement coding is used and a full scale code of 7FFh with +0.5 V input and 800h with –0.5 V input is produced. In this mode, the analog input signals can be positive or negative with respect to the common mode voltage.

Equation 4.4 determines the smallest change which can be measured in the FPGA device. This change is usually represented by the ADC's least significant bit (LSB).

$$Resolution = \frac{1\,\mathrm{V}}{2^{12}} = \frac{1\,\mathrm{V}}{4096} = 244\,\mu\mathrm{V}. \tag{4.4}$$

From this design, the temperature and the power supplies of the IGBT gate driver can be measured. Moreover, the load current I_L can be measured. This depends on the structure of drive system.

As mentioned above, the auxiliary inputs can be used as analog inputs or digital I/O. When these auxiliary inputs are used as analog inputs, they don't require the UCF, but the UCF is required when the auxiliary inputs are used as digital I/O. On the other side, it is possible to use any number of auxiliary inputs as analog input and the other inputs can be used as digital I/O.
When the auxiliary inputs are used as digital I/O, the user constraint file (UCF) must be written using Table 4.7. Appendix B, section B.1 represents the UCF for auxiliary inputs used as digital I/O.

Header pin		Channel	Net Name	FPGA Pin	Standard I/O
Header (J4)	9	Channel 8	VAUX_AD8_N	B12	LVCMOS33
	11		VAUX_AD8_P	C12	LVCMOS33
	10	Channel 2	VAUX_AD2_N	B13	LVCMOS33
	12		VAUX_AD2_P	C13	LVCMOS33
	13	Channel 9	VAUX_AD9_P	A13	LVCMOS33
	15		VAUX_AD9_N	A14	LVCMOS33
	14	Channel 11	VAUX_AD11_N	A15	LVCMOS33
	16		VAUX_AD11_P	B15	LVCMOS33
	17	Channel 4	VAUX_AD4_P	B17	LVCMOS33
	19		VAUX_AD4_N	A18	LVCMOS33
	18	Channel 3	VAUX_AD3_N	A16	LVCMOS33
	20		VAUX_AD3_P	B16	LVCMOS33
	21	Channel 10	VAUX_AD10_P	C14	LVCMOS33
	23		VAUX_AD10_N	C15	LVCMOS33
	22	Channel 5	VAUX_AD5_P	C17	LVCMOS33
	24		VAUX_AD5_N	C18	LVCMOS33
Header (J11)	42	Channel 0	VAUX_AD0_N	G16	LVCMOS33
	43		VAUX_AD0_P	G15	LVCMOS33
	45	Channel 1	VAUX_AD1_N	F16	LVCMOS33
	46		VAUX_AD1_P	F15	LVCMOS33
	94	Channel 12	VAUX_AD12_N	D16	LVCMOS33
	95		VAUX_AD12_P	D15	LVCMOS33

Table 4.7: Auxiliary inputs connected to Headers (J11) and (J4).

4.2.1.7 DDR2 SDRAM Memory Design

The proposed FPGA board includes a 128 MB DDR2 SDRAM memory (16Meg x8). This device has eight internal banks. The double data rate architecture is used by DDR2 SDRAM to achieve a high speed operation. The DDR2 architecture uses a 4n-prefetch architecture in which the internal data bus is four times the width of the external data bus. Figure 4.13 illustrates the DDR2 circuit and its nets connected to the FPGA.

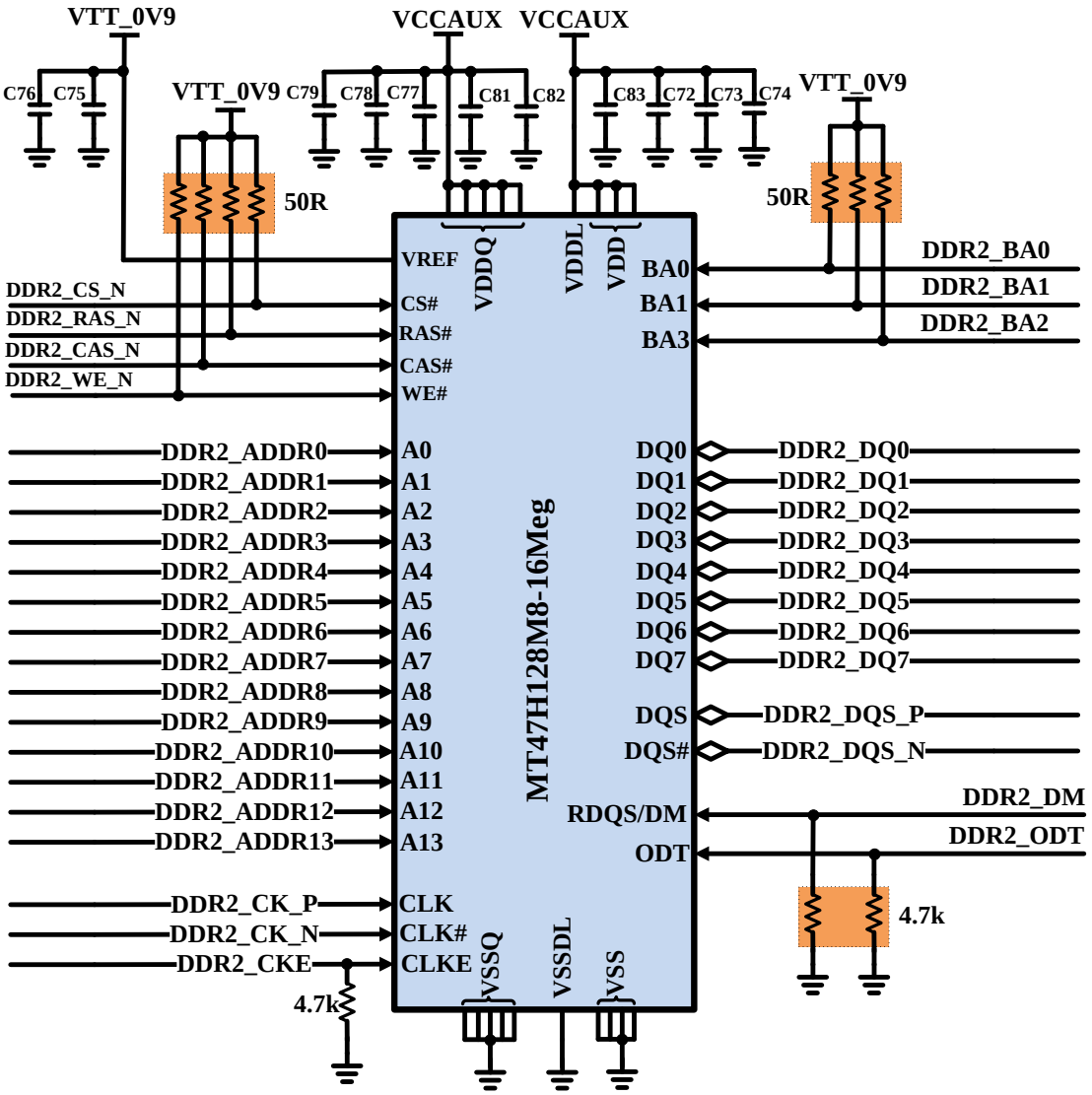
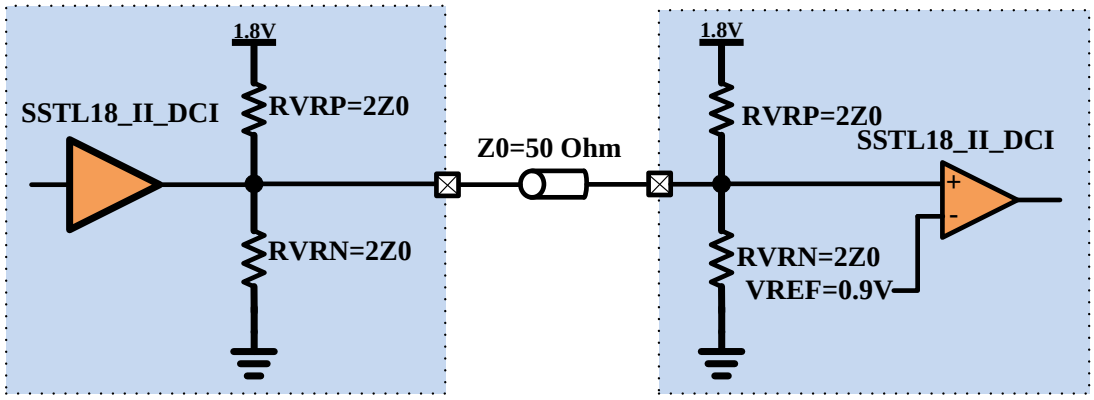


Figure 4.13: DDR2 SDRAM memory schematic circuit.

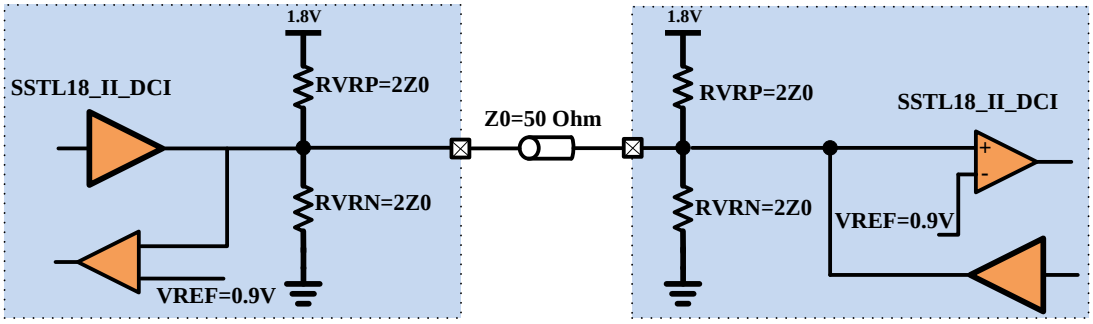
Table 4.8 lists the connection between the DDR2 and the FPGA. The bidirectional data bus DQ[7:0] is used as input for data reads and as output for data writes. The address

DDR2 PIN			Net Name	FPGA PIN	I/O Standard
ADRESSES OF DDR2	1	A0	DDR2_ADDR0	R2	SSTL18_II
	2	A1	DDR2_ADDR1	N3	SSTL18_II
	3	A2	DDR2_ADDR2	P1	SSTL18_II
	4	A3	DDR2_ADDR3	M5	SSTL18_II
	5	A4	DDR2_ADDR4	K3	SSTL18_II
	6	A5	DDR2_ADDR5	R1	SSTL18_II
	7	A6	DDR2_ADDR6	L1	SSTL18_II
	8	A7	DDR2_ADDR7	M3	SSTL18_II
	9	A8	DDR2_ADDR8	K2	SSTL18_II
	10	A9	DDR2_ADDR9	N2	SSTL18_II
	11	A10	DDR2_ADDR10	P2	SSTL18_II
	12	A11	DDR2_ADDR11	L3	SSTL18_II
	13	A12	DDR2_ADDR12	L5	SSTL18_II
	14	A13	DDR2_ADDR13	K1	SSTL18_II
DA I/O OF DDR2	15	DQ0	DDR2_DQ0	AB2	SSTL18_II_T_DCI
	16	DQ1	DDR2_DQ1	AA3	SSTL18_II_T_DCI
	17	DQ2	DDR2_DQ2	W1	SSTL18_II_T_DCI
	18	DQ3	DDR2_DQ3	AB1	SSTL18_II_T_DCI
	19	DQ4	DDR2_DQ4	Y1	SSTL18_II_T_DCI
	20	DQ5	DDR2_DQ5	AA1	SSTL18_II_T_DCI
	21	DQ6	DDR2_DQ6	AB3	SSTL18_II_T_DCI
	22	DQ7	DDR2_DQ7	AA4	SSTL18_II_T_DCI
CONTROL	23	DQS	DDR2_DQS_P	Y3	DIFF_SSTL18_II_T_DCI
	24	DQS#	DDR2_DQS_N	Y2	DIFF_SSTL18_II_T_DCI
	25	CLKE	DDR2_CKE	U2	SSTL18_II
	26	ODT	DDR2_ODT	V2	SSTL18_II
	27	CLK	DDR2_CK_P	M2	DIFF_SSTL18_II
	28	CLK#	DDR2_CK_N	M1	DIFF_SSTL18_II
Banks	29	BA0	DDR2_BA0	U1	SSTL18_II
	30	BA1	DDR2_BA1	T1	SSTL18_II
	31	BA2	DDR2_BA2	N4	SSTL18_II
	32	DM	DDR2_DM	W5	SSTL18_II
	33	RAS#	DDR2_RAS_N	P4	SSTL18_II
	34	CAS#	DDR2_CAS_N	R4	SSTL18_II
	35	WE#	DDR2_WE_N	R3	SSTL18_II
	36	CS#	DDR2_CS_N	T3	SSTL18_II

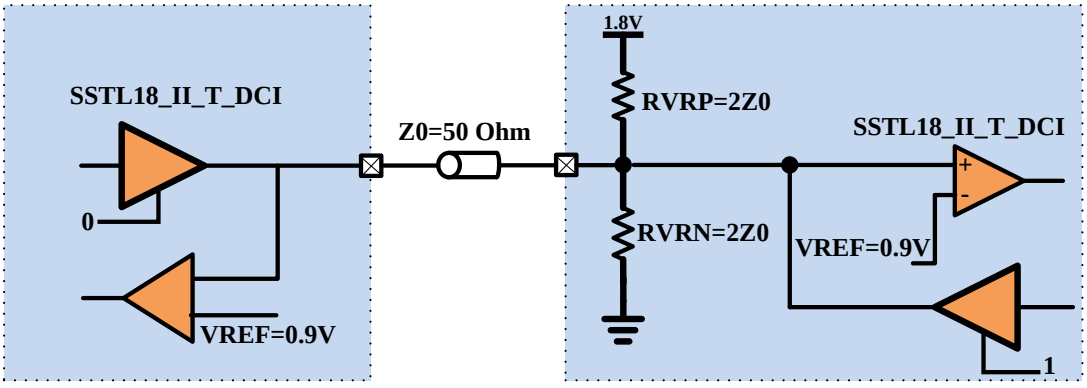
Table 4.8: The connections between the DDR2 SDRAM memory and the FPGA.



(a) SSTL18 class II with unidirectional termination.

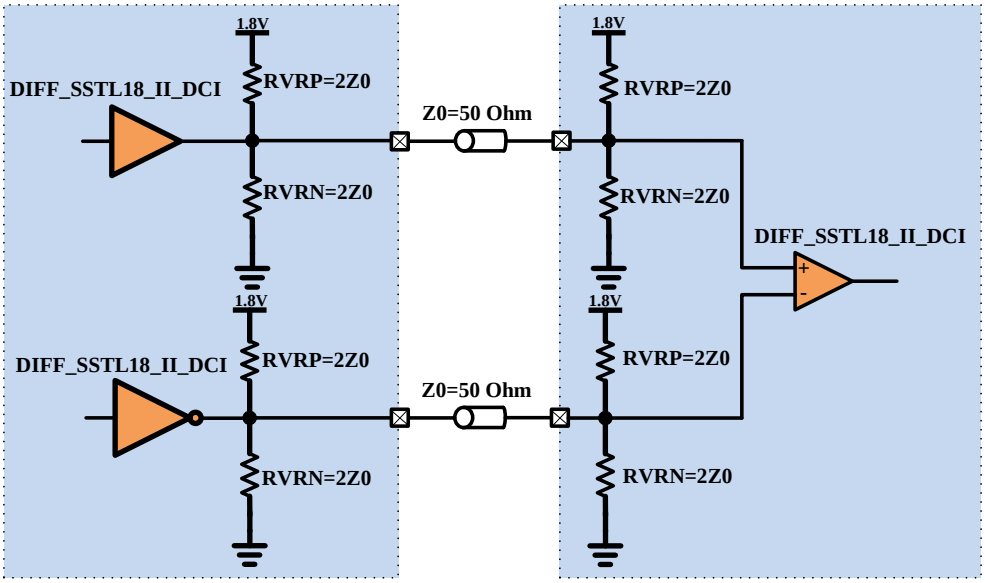


(b) SSTL18 class II with bidirectional termination.

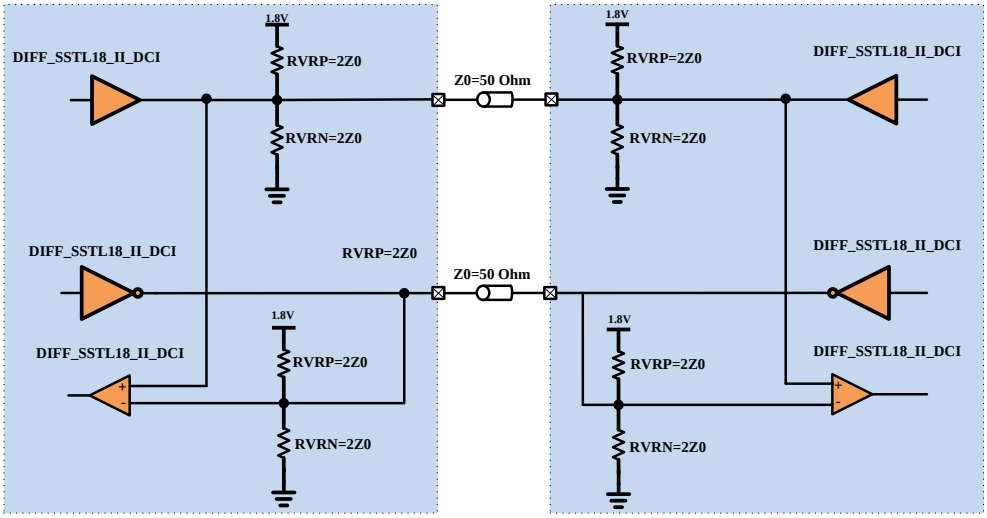


(c) SSTL18 class II with T-DCI termination.

Figure 4.14: SSTL18 class II sample circuits [110].



(a) Differential SSTL18 class II with unidirectional DCI termination.



(b) Differential SSTL18 class II with DCI bidirectional termination.

Figure 4.15: Differential SSTL18 class II sample circuits [110].

inputs A[13:0] provide the row address for ACTIVATE commands, and the column address for READ/WRITE commands. The data mask signal (DM) is used for write data. The command inputs RAS#, CAS#, WE#, and CS# are used for control commands. The differential clock (CLK, CLK#) is provided by the FPGA device, where all address and control signals are sampled on the positive edge of CLK and the negative edge of CLK#. The differential data strobe (DQS, DQS#) is bidirectional signal, where it is an output with read data and an input with write data. The on-die termination (ODT) is the input signal which activates the termination resistance internal to the DDR2 device.

The SDRAM devices use the SSTL 1.8 V I/O standard. This SSTL18 (class-I, class-II) can be provided by the 7 series FPGAs. The class-I driver is only used in unidirectional, whereas class-II driver is used for both bidirectional and unidirectional signals. In the proposed FPGA board, the DDR2 interface is implemented across the high performance (HP) bank (Bank 34). Therefore, the supply voltage of this bank is 1.8 V provided by VCCAUX. Table 4.8 provides the I/O standards used at the connection between the FPGA device and The DDR2. The address and command signals are unidirectional signals driven by the FPGA (SSTL18_II) shown in Figure 4.14a. While The DQ[7:0] bus is bidirectional signals (SSTL18_II_T_DCI) shown in Figure 4.14c. The DQS is bidirectional differential signal (DIFF_SSTL18_II_T_DCI). The CLK is unidirectional differential signal (DIFF_SSTL18_II) illustrated in Figure 4.15a.

An external reference voltage is provided for the data interface. This voltage is equal to $VDD/2 = 0.9\,\text{V}$. Accordingly, the reference voltage of DDR2 is 0.9 V. The bank 34 has also a dedicated DCI VRP/VRN resistor connection. Figure 4.16 depicts these connections.

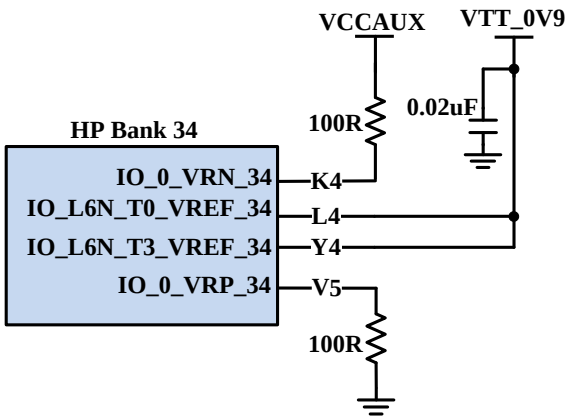


Figure 4.16: Dedicated DCI VRP/VRN resistor and reference voltage schematic circuit.

The Memory Interface Generator (MIG) tool is used to generate HDL and pin placement constraints [104]. Appendix B, section B.2 provides these necessary constraints. The MIG generates the memory controller (MC) which implements the interface between the FPGA device and the DDR2. The physical interface between the external DDR2 and the MC is achieved via the physical layer (PHY). The PHY controls all DDR2 signals sequencing

and timing. Various clocks are required for DDR2 SDRAM interface. Using the clocking wizard, the required frequencies, which are listed in Table 4.9, can be generated.

Clock Name	Frequency (Hz)	Required Phase	Required Group	Buffer
Clk_ref	200,000,000	0	PLLE0	True
Mem_refclk	400,000,000	0	PLLE0	False
Freq_refclk	400,000,000	337.5	PLLE0	False
Sync_pulse	25,000,000	9.84375	PLLE0	False
SYS_Freq=150 MHz				

Table 4.9: The required frequencies for The DDR2 SDRAM interface.

4.2.1.8 USB to UART Bridge

The proposed FPGA board contains a USB to UART bridge device (CP2103-GM) which allows a connection to a host computer with a USB port. This connection is achieved via a mini-B USB cable. Figure 4.17 depicts the USB to UART Bridge circuit that is connected to the FPGA device. The CP2103 includes an on-chip 5 to 3 V voltage regulator, it is configured as a USB bus-powered device where it is powered by the USB 5 V which provided by the host PC when the mini-USB cable is plugged into the USB port on the proposed FPGA board. Accordingly, a (3 V/100 mA) voltage regulator output is provided on the VDD pin, and it can be used to power an external devices with 3 V. The I/O voltage (VIO) is powered by an external voltage supply 3.3 V provided by the VCCO_3.3V.

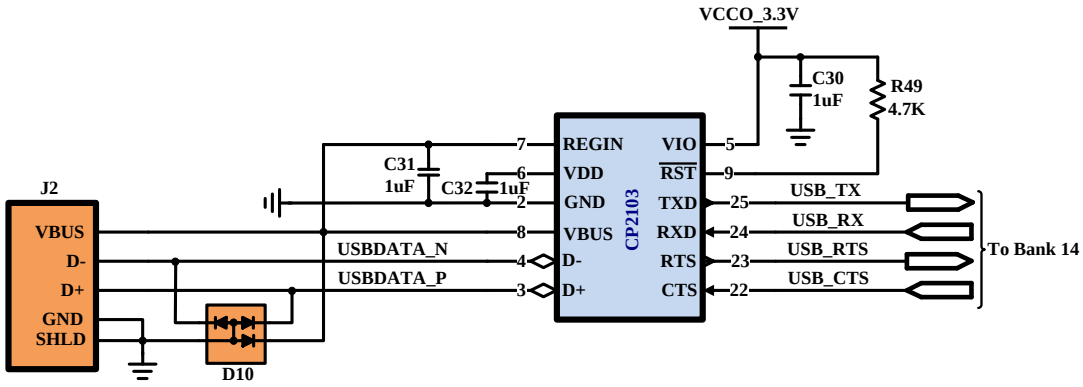


Figure 4.17: USB TO UART bridge schematic circuit.

Four signals are used to connect the CP2103 UART to the FPGA. These signals are wired to HR Bank 14 as listed in Table 4.10.

Silicon Laboratories provides royalty-free Virtual COM Port (VCP) device drivers which permit the CP2103 to appear as a COM port to PC applications (Tera Term,

CP2103 Pin	Direction	Net Name	FPGA Pin	I/O Standard
TXD	Output	USB_TX	R22	LVCMOS33
RXD	Input	USB_RX	R21	LVCMOS33
RTS	Output	USB_RTS	R18	LVCMOS33
CTS	Input	USB_CTS	R19	LVCMOS33

Table 4.10: The connection of UART to FPGA pins (HR Bank 14).

HyperTerm). The UART supports a variety of data formats and baud rates. The UCF constraints for the UART port must be added to the design which includes the USB to UART bridge. Appendix B, section B.3 provides the UCF constraints for the UART port.

4.2.1.9 User GPIO LEDs

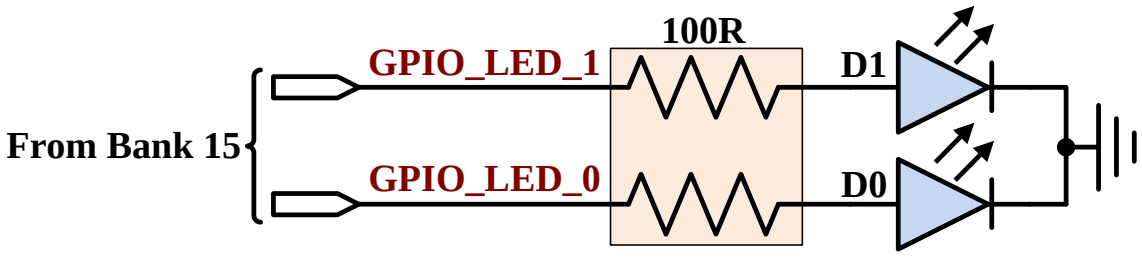


Figure 4.18: Schematic circuit of the User GPIO LEDs.

The proposed FPGA board includes two GPIO LEDs which are used to test the board and the design on the proposed FPGA board. Figure 4.18 shows the GPIO LEDs circuit and Table 4.11 lists the GPIO LEDs connection to the FPGA pins.

Led Name	Net Name	FPGA Pin	I/O Standard
D0	GPIO_LED_0	C22	LVCMOS33
D1	GPIO_LED_1	D22	LVCMOS33

Table 4.11: GPIO LEDs connection to the FPGA pins (HR Bank 15).

When the GPIO LEDs are used to test HDL functions such as (counters, PWM signals, gate logic), the UCF constraints must be added to this design. Appendix B, section B.4 provides the UCF location constraints for the GPIO LEDs.

4.2.1.10 Board to Board Connector J11

This connector J11 is used to connect the FPGA board to the gate drive. The J11 provides up to 73 single-ended signals. In addition, the J11 provides analog inputs, as shown in

Figure 4.12. The J11 can also power the external devices that are available onto the gate drive board by the following voltages:

1. Power supply voltage 5 V/0.5 A (VCC_5V5MAX).
2. Power supply voltage 3.3 V/0.5 A (VCC_3.3V).
3. Power supply 1.25 V/100 mA (VREF_0).

Moreover, the J11 includes multi-functional contacts (MF contact) which are used to provide a power supply with 5 V/2.5 A and system ground (GND). An analog ground (GND_ADC) is also provided by the J11.

All pins of J11 are connected to HR banks: Bank 13, Bank 14, and Bank 15. Appendix A, section A.1 lists the J11 connections to the FPGA. The FPGA receives or transmits data via the J11 connector using LVCMOS33 level. The UCF constraints for J11 contacts are provided in Appendix B, section B.5.
The I/O standard LVTTL can also be used, where the LVTTL is a general standard for 3.3 V applications which use a single-ended CMOS input buffer and a push-pull output buffer.

4.2.1.11 Board to Board Connector J10

The proposed FPGA board also includes another board to board connector J10. The J10 connects to the HP Bank 33 and the HR Bank 16. Therefore, I/O standards use 1.8 V level provided by the HP Bank 33 and 3.3 V level provided by the HR Bank 16. Appendix A, section A.2 provides the J10 connections to the FPGA device. Up to 20 differential signal pairs or 40 single-ended signals are provided by the J10. If a differential signal pair is used to interface an external device, the differential high speed transceiver logic (DIFF_HSTL_18) is used. Two DIFF_HSTL_18 classes with DCI are available in the proposed FPGA design [112]. If a single-ended signal is used for data, LVCMOS18 or HSLV18 can be used. Appendix B,subsection B.6.1 provides the UCF constraints for the differential signal pairs when they are used in the design.
Up to 19 single-ended signals with 3.3 V level are also provided by the J10. The I/O standard LVCMOS33 or LVTTL can be used to interface an external device. The UCF constraints of these signals are provided in Appendix B, subsection B.6.2.
The power supplies provided by the J10 are:

1. Power supply voltage 5 V/0.5 A (VCC_5V5MAX).
2. Power supply voltage 3.3 V/0.5 A (VCC_3.3V).
3. Power supply voltage 1.8 V/0.5 A (VCCAUX).

The J10 also includes multi-functional contacts (MF contact) which are used to provide a power supply with 5 V/2.5 A and a system ground (GND) . In addition, it connects to the analog ground (GND_ADC) for the external analog signals.

4.2.1.12 Board to Board Connector J12

This 2 mm pitch SMD connector J12 provides up to 14 single-ended signals with 3.3 V level. The J12 connects to the HR Bank 15. Appendix A, section A.3 lists these J12 connections to the FPGA device. The J12 can be used to interface various external devices such as LCD display, an external clock oscillator, or SPI ADC devices. The I/O standard used for data is LVCMOS33. Appendix B, section B.7 provides the UCF constraints for the J12.

The J12 also provides a power supply with voltage 3.3 V which can be used to power the external devices that connect to the FPGA via the J12.

4.2.2 PC Layout of the Proposed FPGA Board

Figure 4.19 shows the printed circuit of the FPGA board (PCB). The number of layers used in the design is six. The structure of layer stack is shown in Figure 4.20, and the

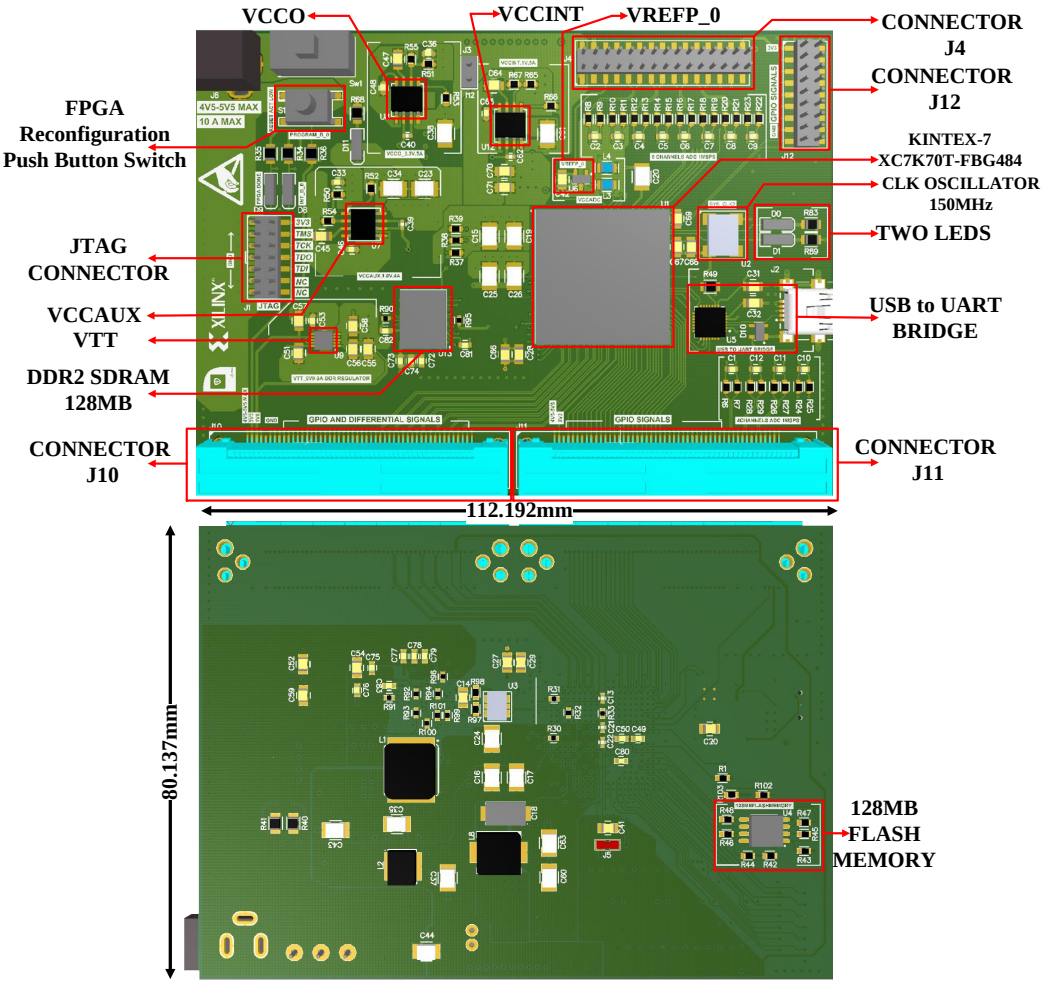


Figure 4.19: Top and bottom view of the proposed FPGA board.

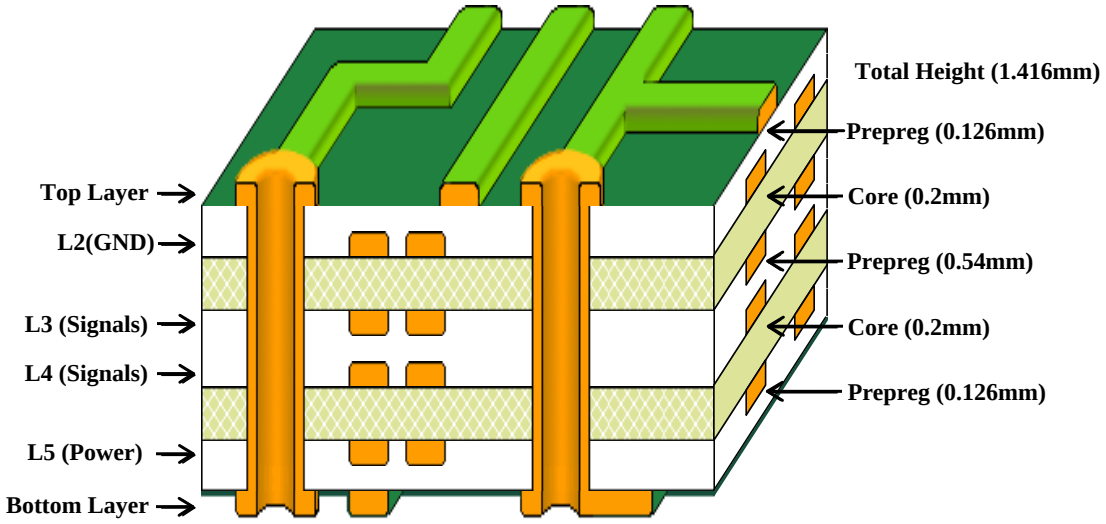


Figure 4.20: The layer stack-up for 6 layers used in the FPGA board.

Layer Name	Copper Thickness	Dielectric Height	Dielectric Material	Dielectric Constant	Dielectric Type
Top Solder Mask	–	0.0102 mm	Solder Resist	3.50	–
Top Layer	0.0356 mm	–	–	–	–
–	–	0.126 mm	FR-4	4.70	PrePreg
L2(GND)	0.0356 mm	–	–	–	–
–	–	0.2 mm	FR-4	4.70	Core
L3(Signals)	0.0305 mm	–	–	–	–
–	–	0.54 mm	FR-4	4.70	PrePreg
L4(Signals)	0.0305 mm	–	–	–	–
–	–	0.2 mm	FR-4	4.70	Core
L5(Power)	0.0356 mm	–	–	–	–
–	–	0.126 mm	FR-4	4.70	PrePreg
Bottom Layer	0.0356 mm	–	–	–	–
Bottom Solder Mask	–	0.0102 mm	Solder Resist	3.50	–

Table 4.12: Layer stack-up detail for the FPGA board (PCB).

materials of layer stack-up are listed in Table 4.12, where the PCB dielectric material is FR4 with a dielectric constant of 4.70. The components are placed on the top and bottom sides. Plated Through Hole (PTH) are used to connect between the layers. The inner layers L3 and L4 are signal layers. They include the DDR2 signals (ADDR(0:13), DQ, DQS, control signals). Single-ended signals and differential pairs were also routed onto these inner layers.

In addition, polygon GND was used for shielding. The layers L3 and L4 are shown in Appendix C, Figure C.2. The outer layer L2 is used as a reference plane (GND system), and it plays a significant role for EMI shielding. The outer layer L5 is used for the power distribution system (PDS). The L5 is split to four power nets, as shown in Appendix C, Figure C.2e. The polygon planes were used to achieve the required power nets which allow carrying heavy power supply currents for the FPGA device.

The power supplies of the FPGA device must not vary more than ±5 % [109]. The voltage regulators VRs keep the power supplies constant. These VRs were placed onto the top side. They are placed near the FPGA device to reduce the losses. The polygon planes are provided. This design allows drawing a heavy current between layers into the FPGA device.

In addition, the bypass filters were used to reduce the noise in the current which can be supplied into the FPGA device. The capacitors have characteristics of low ESR and ESL, where every capacitor with the parasitic ESR and ESL behaves as a RLC circuit, which its resonant frequency is defined by Equation 4.5.

$$f_{RSELF}(\text{MHz}) = \frac{1}{2\pi\sqrt{L_{self}C}} \tag{4.5}$$

where f_{RSELF} is the capacitor's self resonant frequency, C is the nominal capacitance, and L_{self} is the parasitic inductance (ESL) of the capacitor.

However, there is a difference between the capacitor's self resonant F_{RSELF}, and the capacitor's effective resonant frequency f_{RIS}, where the effective parasitic inductance L_{IS} will be the sum of capacitor's parasitic inductance L_{self}, and the mounting's parasitic inductance L_{mount}, that is formed when the capacitor is mounted on the PC board. The L_{mount} is the inductance of PCB lands, connecting traces, vias, and power planes:

$$L_{mount}(nH) = L_{trace} + L_{via} + L_{PCBland} + L_{Powerplane}. \tag{4.6}$$

The inductance of a connecting trace ,L_{trace}, can be calculated approximated by Equation 4.7 [35]

$$L_{trace}(nH) = 2X \cdot \left(ln\langle\frac{2X}{W+h}\rangle + 02235\langle\frac{W+h}{X}\rangle + 0.5 \right) \tag{4.7}$$

where X is the length of the trace in cm, W is the width of the trace in (cm) and h is the height of the trace in cm.
The $L_{PCBland}$ and the $L_{Powerplane}$ can be calculated using special software such as "Saturn PCB Toolkit".
The approximate inductance of the via L_{via}, is given by Equation 4.8 [35]

$$L_{via}(nH) \approx \frac{h}{5} \cdot \left(1 + ln\langle\frac{4h}{d}\rangle \right) \tag{4.8}$$

where h is the height of the via in mm, and d is the diameter of the via in mm.
The total parasitic inductance of capacitor is described by Equation 4.9

$$L_{IS}(nH) = L_{self} + L_{mount}. \tag{4.9}$$

Then, the mounted capacitor resonant frequency, f_{RIS} is determined by Equation 4.10 [109]

$$f_{RIS}(\text{MHz}) = \frac{1}{2\pi \cdot \sqrt{L_{IS}C}}. \tag{4.10}$$

From Equation 4.10, it can be seen that as the parasitic inductance L_{IS} increases the resonant frequency f_{RIS} decreases.

The power distribution system decoupling capacitor networks were also designed to prevent the spike containing harmonic current. This spike generated by the FPGA device during the operation flows into the power supply line. Using decoupling capacitor networks, the harmonic current is forced to flow in a short loop created between the decoupled capacitor and the FPGA device. The decoupling capacitors must place as close as possible to the FPGA device. If the decoupling capacitors are placed farther from the FPGA device, they don't effectively help with simultaneous switching noise (SSN).

As previously mentioned, the connecting trace has an inductance given by Equation 4.7. In addition, the trace has a capacitance, this capacitance can be coupled to nearby conductors. These conductors can be vias, pads, connectors, planes, and other traces. The combination of the inductance and the capacitance forms the trace impedance Z_0. Without taking into account the trace characteristic impedance, the I/O standards with controlled impedance drivers (DCI) can't be used for the high speed transceivers such as DDR2, where the DCI is provided by the 7 series FPGAs HP I/O banks.

The stack-up geometry and the trace geometry affect the characteristic impedance [49]. The DDR2 signals in the proposed FPGA board were routed onto the inner layers L3 and L4, and they were shielded by the outer layer L2 (GND) and the outer layer L5 (PDS). Together, these layers form asymmetric stripline models, whereas the L2 with the top layer forms a microstrip model. This model is also formed by the L5 with the bottom layer.
Accordingly, the single-ended traces of DDR2, which require controlled impedance drivers (DCI), were designed to have a 50 Ω characteristic impedance Z_0, as shown in Figure 4.21.
In addition, the differential traces of DDR2 were designed to have the odd mode impedance, where the differential impedance Z_{diff} is equal to 100 Ω, as shown in Figure 4.22.
The traces of differential pair need to be kept at equal length. This ensures that there is no skew between the signals of the pair, and the flight times will be identical.
As a result, this design leads to minimize the PCB area and the cost, because the external source-termination resistor networks are not required. Moreover, this design eliminates the reflections which may cause several problems such as modifying frequency responses, overload, and over-voltage.

The DDR2 address traces were also routed to have a 50-60 Ω characteristic impedance. All address traces have the same length, they were matched to less than 1 mm. Figure 4.23 illustrates the DDR2 address traces, where they were tuned to 30 mm in order to match to within 1 mm.

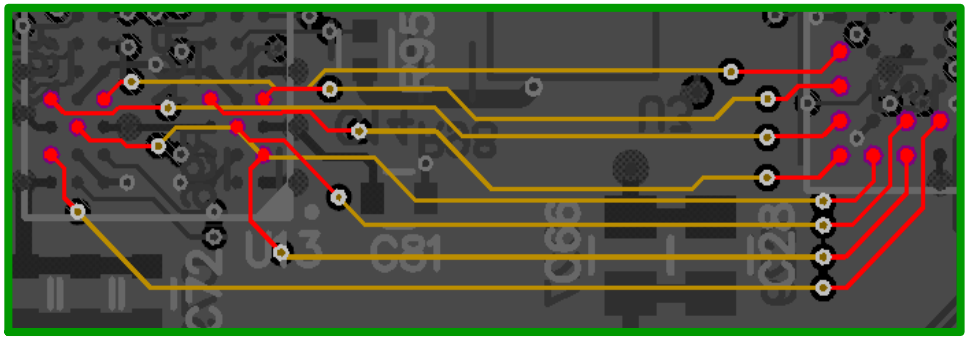


Figure 4.21: The single-ended traces of DDR2 (DQ) with 50 Ω characteristic impedance.

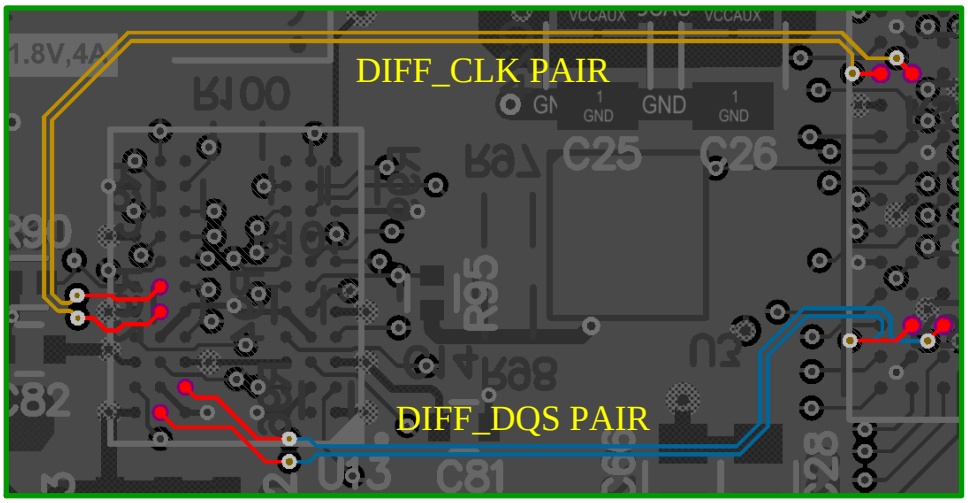


Figure 4.22: The differential traces of DDR2 with 100 Ω differential impedance.

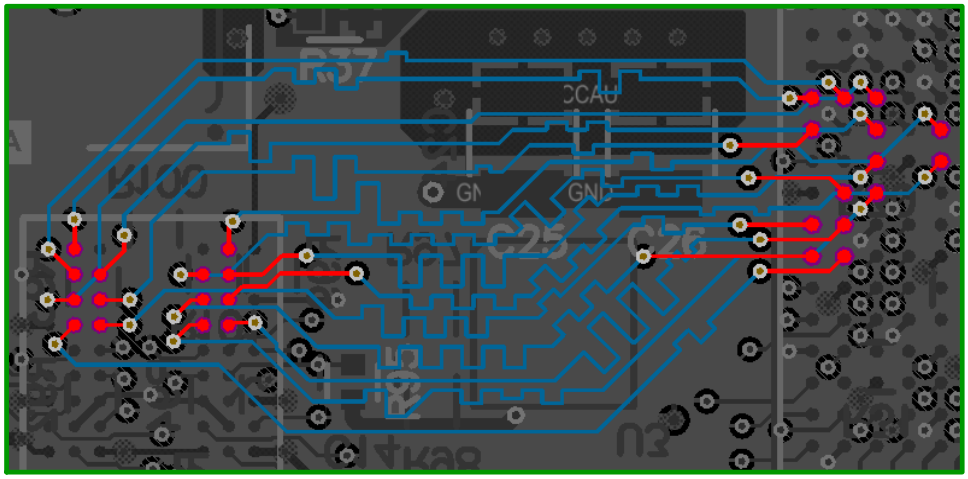


Figure 4.23: The addresses traces of DDR2 with $50 - 60\,\Omega$ impedance.

As indicated in section 4.2.1.6, the 7 series FPGAs provide an integrated analog to digital converter block XADC. The requirements for the XADC were routed, as shown in Figure 4.24. The traces of power supply VCCADC and analog ground GNDADC were routed into the center of FPGA device. The GNDADC trace was tied to the island GND_ADC. The GND_ADC is available onto the top side and the bottom side. The GND_ADC is connected to the system ground GND through the ferrite bead L4, where, the L4 will play an important role in the isolation from the high frequency noise on the system ground and also provides a path for the return current to GND. The trace of the reference voltage VREFP_0, which is connected to the external reference voltage 1.25 V, was also routed to the center. The external reference voltage was placed as close as to the FPGA device.The VREFN_0 pin was tied to the GNDADC pin. The traces of analog differential pair were routed together and were tightly coupled.

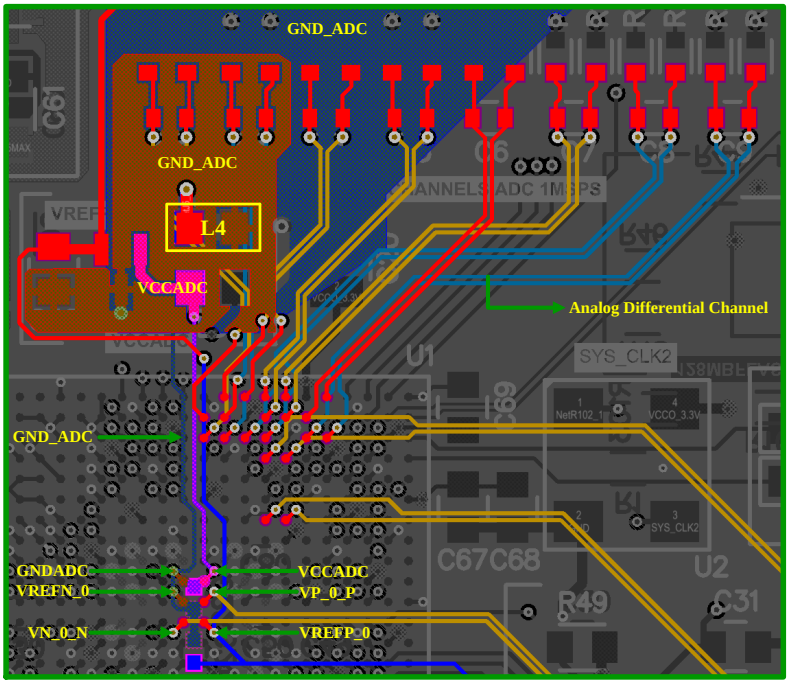


Figure 4.24: The PCB layout of XILINX ADC block (XADC).

4.2.3 Testing the Proposed FPGA Board

Using programs written in VHDL, we tested all the signals on the proposed FPGA board. We used the software "ISE Design Suite 14.4" that includes the following programs:

1. ChipScope pro.
2. Embedded Development Kit (EDK).
   (a) Xilinx Platform Studio (XPS).

(b) Xilinx Software Development Kit (SDK).

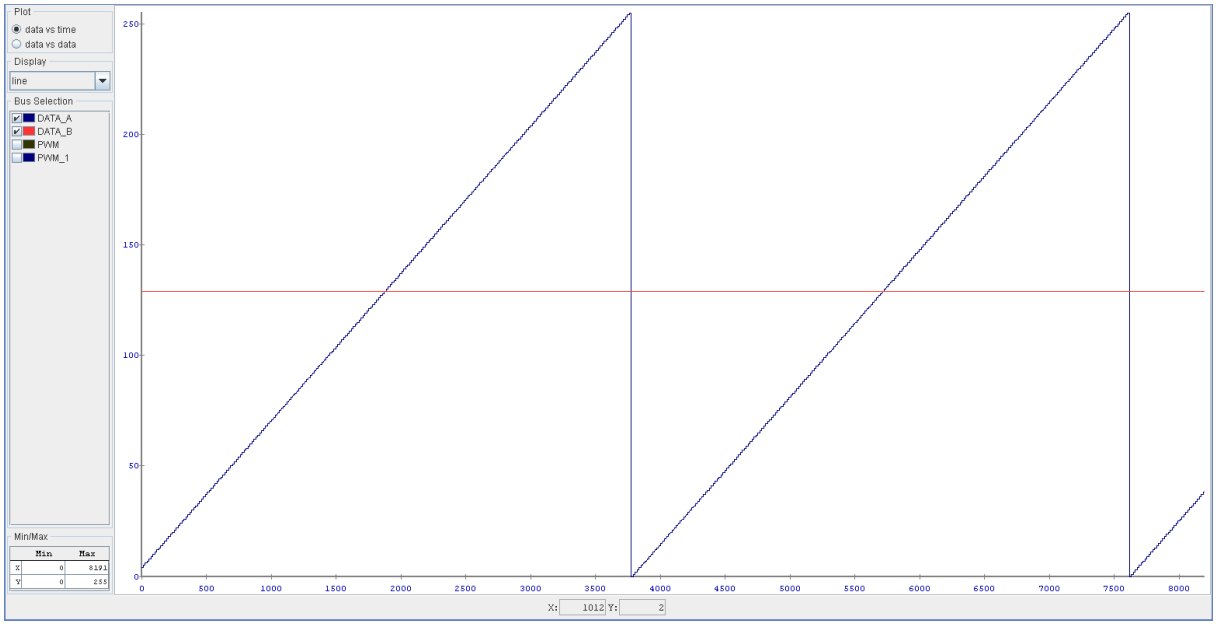
3. ISE Design Tools.
   (a) Project Navigator.
   (b) Tools.
      i. Constraints Editor.
      ii. Core Generator.
      iii. FPGA Editor.
      iv. iMPACT.
      v. Simulation Library Compilation Wizard.
      vi. Timing Analyzer.
      vii. XPower Analyzer.
4. PlanAhead.
5. System Generator (Matlab).

Using The program "ISE Navigator 14.4", we designed a processor, which can generates the PWM waveform, as shown in Figure 4.25. The processor includes an eight bit up counter which generates the sawtooth wave, and data input which is controlled by two push button switches, as shown in Figure 4.25a. The PWM signal is generated when the value of data in is greater than the value of up counter signal. Figure 4.25b illustrates the PWM signal generated by the processor. These signals can be used to control gate drivers and other application in control systems [69], [20].

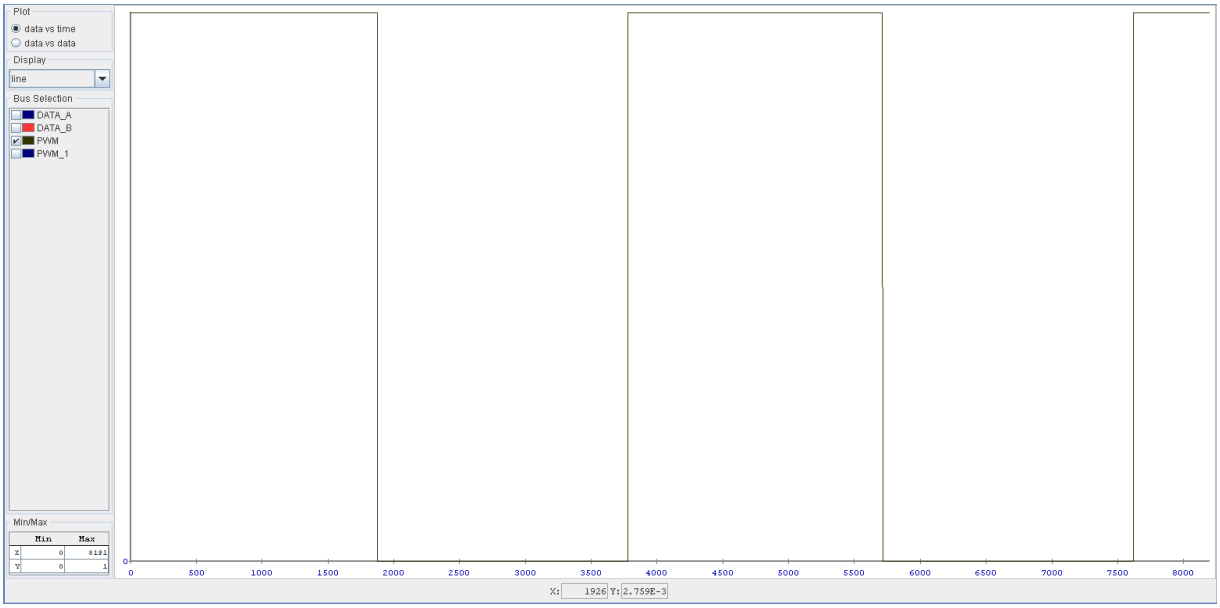
Using the XADC Block, we monitored the FPGA device power supplies waves, where all the values of voltages were between the allowed values, as shown in Figure 4.26.

Using Xilinx XPS and SDK, we implemented the design shown in Figure 4.27. The key of this design is the MicroBlaze processor [106]. The function of this design is to read data from 7 bit dip switch and write data on 7 bit led. The status of the switches is send to PC using USB to UART bridge.

In addition, using the circuits shown in Figure 4.28 and VHDL codes [19], we tested the I/O provided by the connector (J11). As a result, all the J11 I/O can be used to receive data from ADC devices which are used to digitize the required signals of the IGBT gate driver.



(a) The sawtooth waveform with the carried signal.



(b) The PWM waveform.

Figure 4.25: Analyzing data using bus plot in ChipScope core.

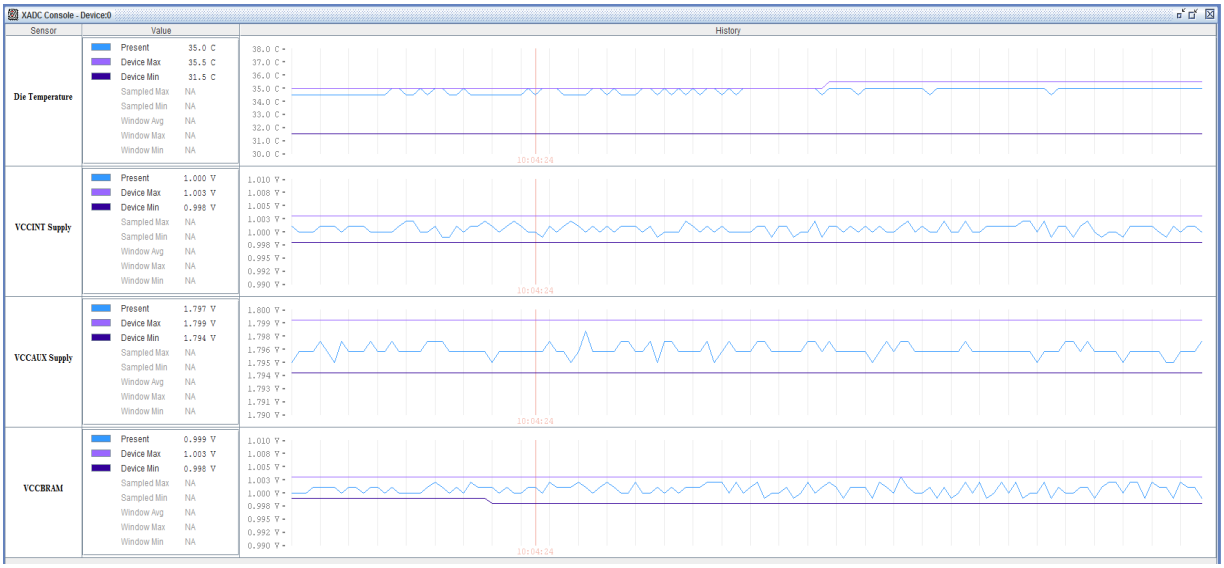


Figure 4.26: Monitoring the power supplies of FPGA device using XADC Block.

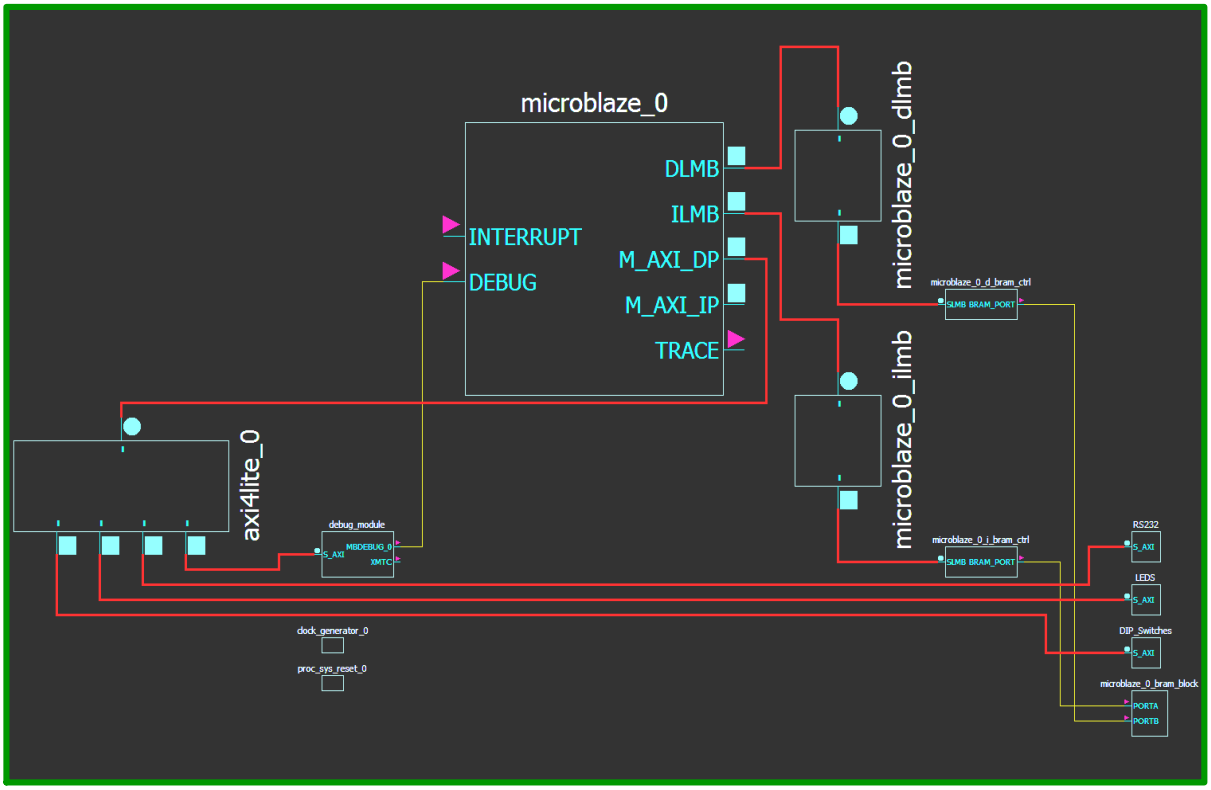
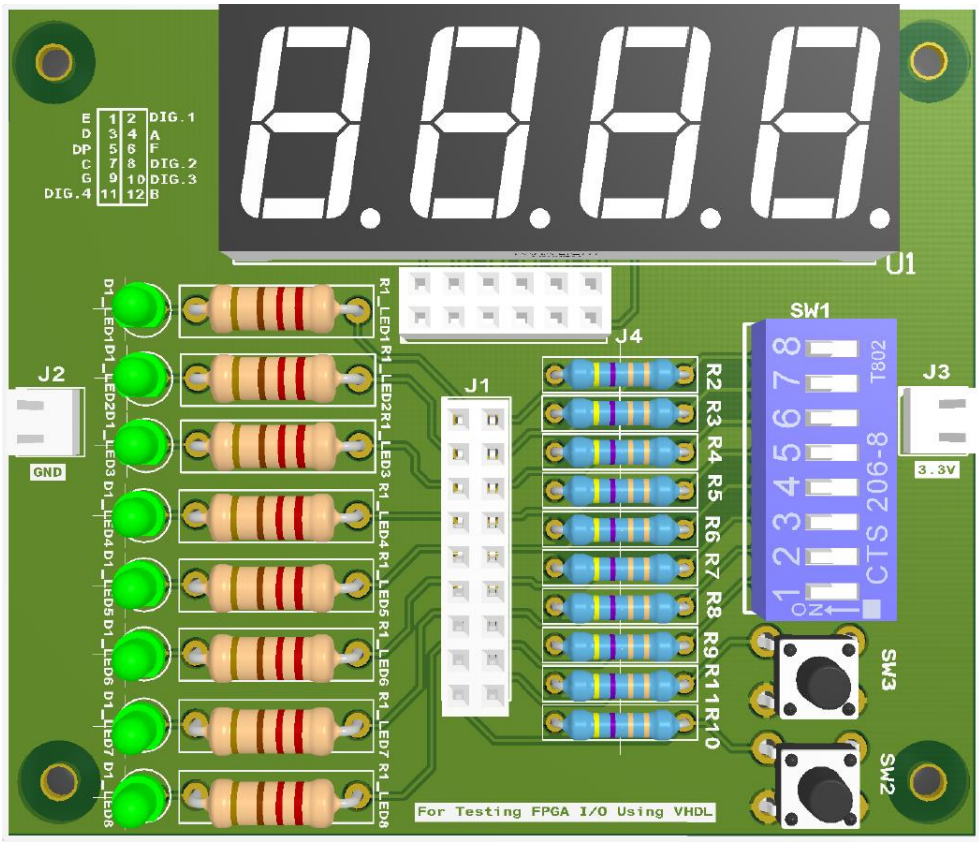
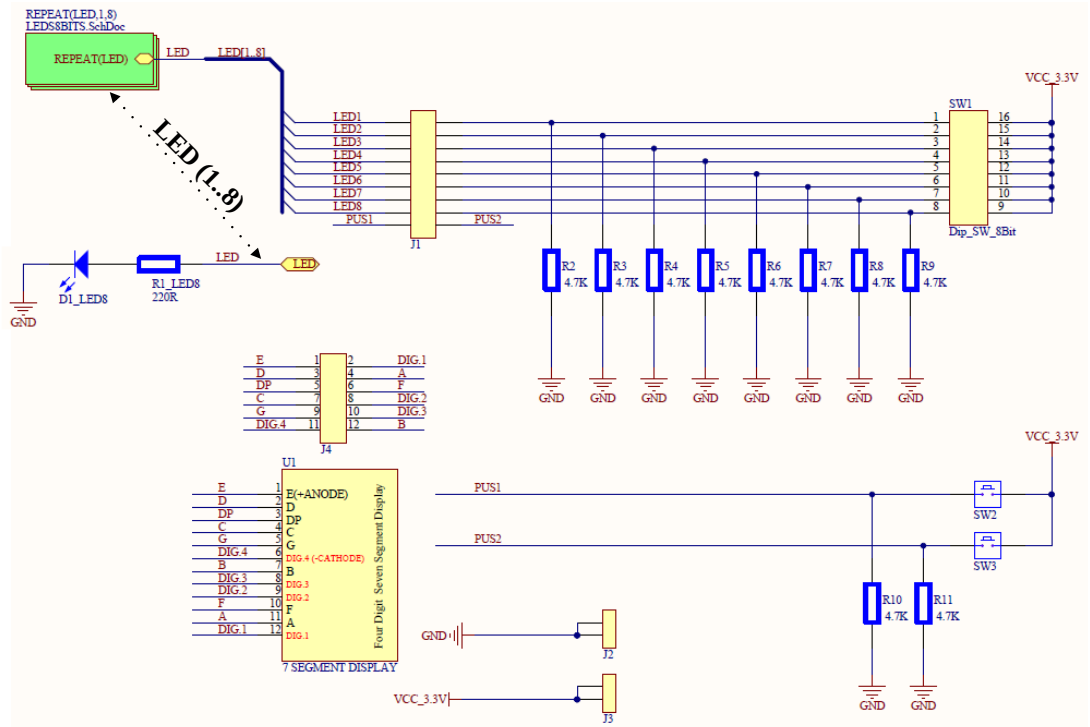


Figure 4.27: Read and write data using MicroBlaze.



(a) The PC of board for testing FPGA I/O.



(b) The schematic circuit of the testing board.

Figure 4.28: PC of testing board with schematic circuit.

Chapter 5

Stages Control Signals Generator Design

From Figure 3.13 in section 3.4.1, six stages control signals for each channel in the proposed IGBT gate driver are required to control the external gate resistors during the IGBT turn-on/turn-off. All the functions of the stages control signals (SCS) generator are activated using a DIP switch (SW). A global reset (RST) is also used to reconfigure the program when an error occurs during the operation. The RST is used to reset and reconfigure the entire software in the main controller and other IGBT gate driver FPGAs, but this also depends on the hardware design. Figure 5.1 depicts the schematic block of the Verilog top level[1](see appendix D, section D.1) for the proposed SCS generator which as-

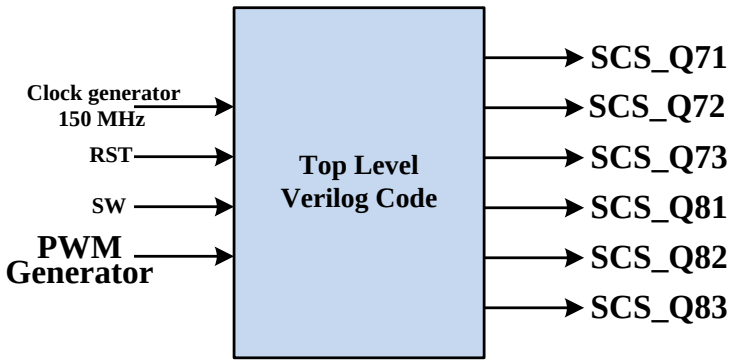


Figure 5.1: Schematic block of Verilog top level in the proposed gate driver FPGA.

serts the stages control signals according to the PWM signals edges of the main controller. The schematic block of the Verilog top level is composed of the following schematic blocks:

- Clocking wizard.
- Switch debouncer.

[1]Top level is created hierarchically from several modules using HDL Verilog, VHDL, and schematic.

- Stages control signals generator.
- PWM input.

5.1 Clocking Wizard

The clocking wizard is used to generate the required output clock frequency. Figure 5.2 illustrates the schematic block of the clocking wizard which is used in the design. The

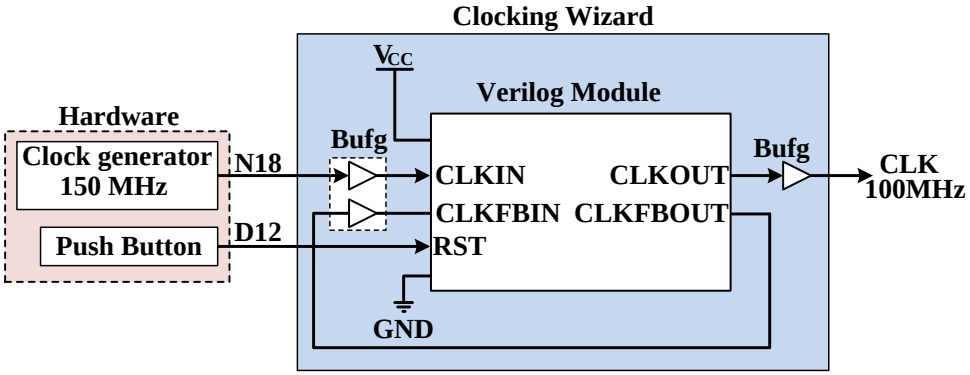


Figure 5.2: Schematic block of the clocking wizard.

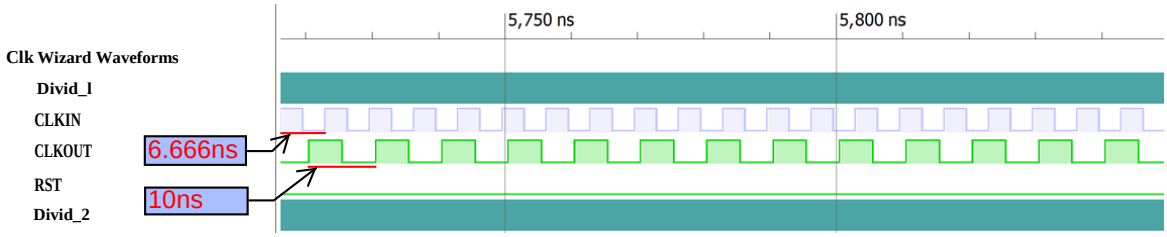


Figure 5.3: The digital signals of the clocking wizard.

input clock frequency f_{clkin} of the clock wizard is 150 MHz across the N18[2]. The f_{clkin} is generated by the system clock shown in Figure 4.6, section 4.2.1.3. The clock output frequency f_{clkout} of the clocking wizard is 100 MHz. Depending on the f_{clkout}, the required signals are generated and sampled. A push button (SW1) is used to reset[3]the system signals. The SW1 is wired to the FPGA across D12[4]. Figure 5.3 shows the simulation digital signals of the clocking wizard, where a Verilog Test Fixture (VTF) has been written using the ISE Design Tools[5].

[2]N18 is the pin to which the system clock was wired, and it is available in the FPGA bank 14. T4 in the bank 34 can also be used for this design.

[3]RST is high, when it is inserted by the SW1.

[4]D12 is optional and any pin can be used to perform the RST function.

[5]ISE Simulator is used to simulate the inputs and outputs signals of the top level design.

5.2 Stages Control Signals Generator

As mentioned before, the system frequency f_{clkout}, which is an output of the clocking wizard, is 100 MHz. Accordingly, the clock input (CLK) of the SCS generator is 100 MHz. Figure 5.4 represents the schematic block of the SCS generator for one channel in the proposed IGBT gate driver. A Verilog code is created for this purpose. Six stages control signals are generated for one channel[6]. Two up counters and two comparators are used

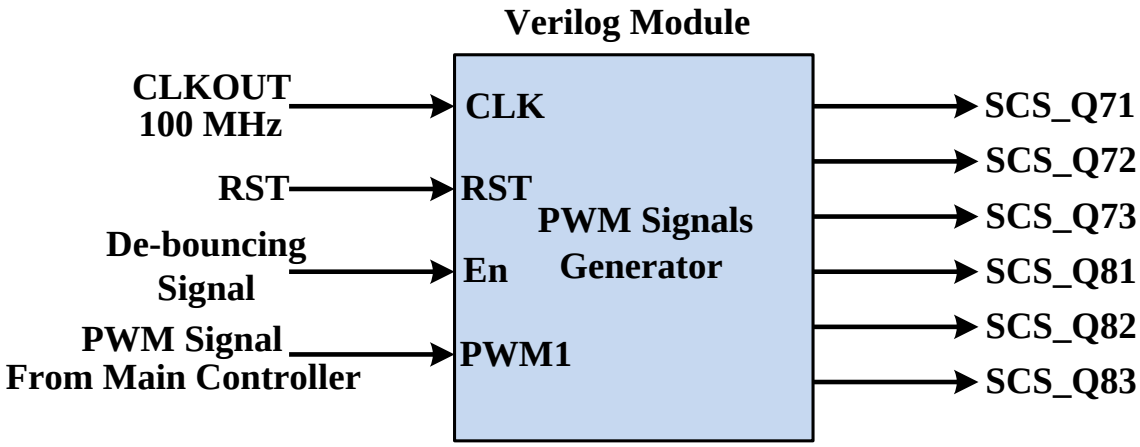


Figure 5.4: Schematic block of the SCS generator.

to generate the required signals, as shown in Figure 5.5. The maximum count value of the counters is determined by the duty cycle of the PWM wave which is generated by the main controller. As can be seen in the Figure 5.5, when the PWM signal of the main controller has rising edge, the stage control signal SCS_Q71 is asserted by the SCS generator and the first counter begins to count. The count value of the counter1 is compared with the delay time t_{d1}. When the count value is greater than the value of t_{d1}, the stage control signal SCS_Q72 is confirmed, and the stage control signal SCS_Q73 is asserted when the value of the counter1 is greater than the delay time t_{d2}. Accordingly, the external gate resistors are controlled by switching the stages transistors $Q7_1$, $Q7_2$ and $Q7_3$ in sequence with delay times t_{d1} and t_{d2}.
On the other hand, the stage control signal SCS_Q81 is asserted and the counter2 begins to increase, when the PWM signal of the main controller has falling edge. As a consequence, the stage control signal SCS_Q82 is asserted when the count value of the counter2 is greater than the t_{d3} and the stage control signal SCS_Q83 is confirmed when the count value of the counter2 is greater than the t_{d4}. This allows controlling the external gate resistors during the IGBT turn-off.

As long as the clock frequency of the SCS generator f_{clk} is 100 MHz, the time period

[6]This channel can be upper or bottom channel for the proposed IGBT gate driver.

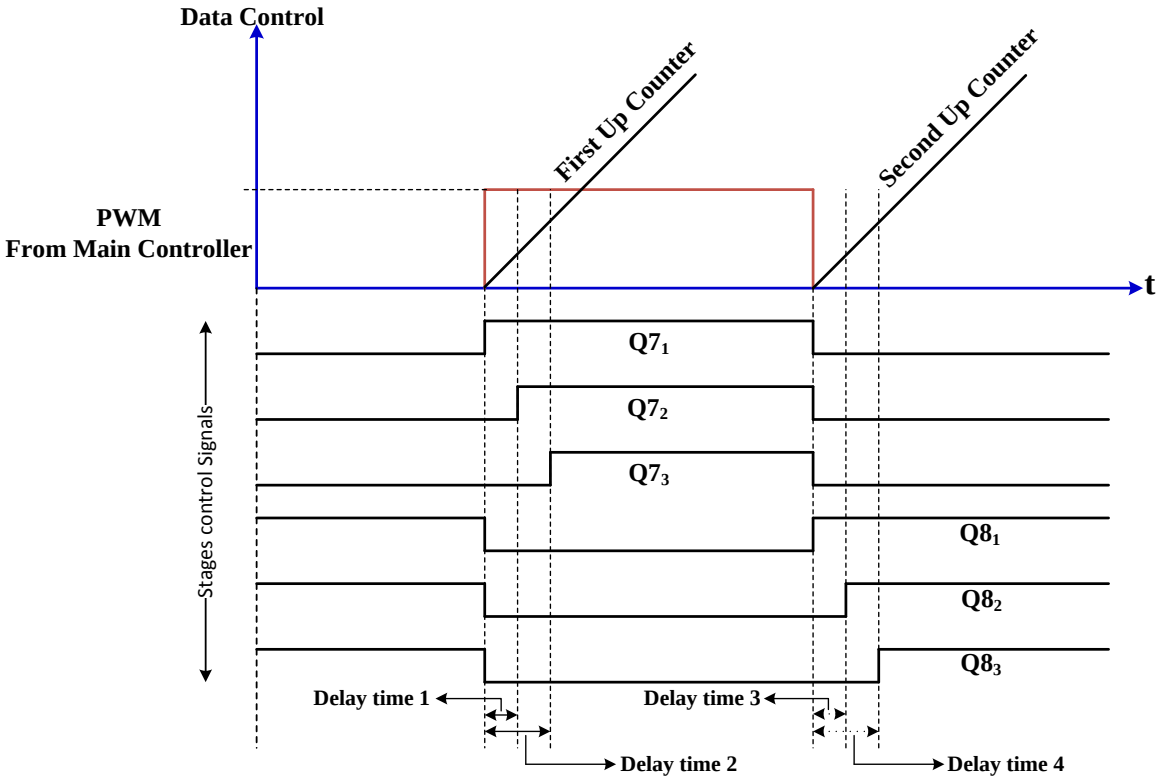


Figure 5.5: Up counters operation with SCS generator outputs and PWM edges.

t_{clk} is

$$t_{clk} = \frac{1}{fclk} = \frac{1}{100} = 10\,\text{ns}. \tag{5.1}$$

Accordingly, the number of clock cycles, which is required to implement a delay time, could be calculated as follows

$$N_{CC} = \frac{delay\,time}{t_{clk}}. \tag{5.2}$$

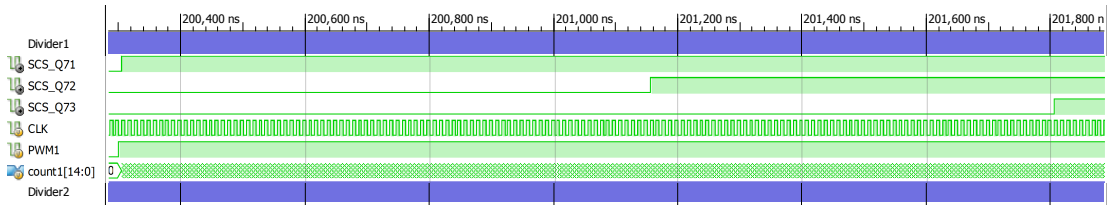
Assuming that the IGBT switching frequency f_{sw} is 5 kHz, $t_{d1} = t_{d3} = 0.85\,\mu$s, and $t_{d2} = t_{d4} = 1.5\,\mu$s[7]. The number of clock cycles can be calculated as follows

$$N_{CC_{td1}} = \frac{0.85{\cdot}10^{-6}}{10{\cdot}10^{-9}} = 85\,\text{cycles}.$$

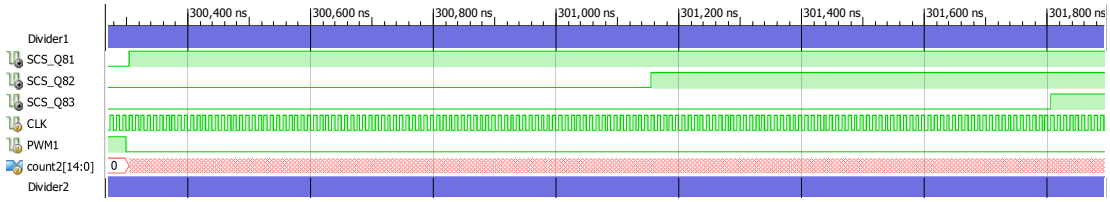
$$N_{CC_{td2}} = \frac{1.5{\cdot}10^{-6}}{10{\cdot}10^{-9}} = 150\,\text{cycles}.$$

[7]This is only an example

Figure 5.6 illustrates the stages of assertion of the stages control signals during the operation. The stages control signals of the transistors $Q7_1$, $Q7_2$ and $Q7_3$ are asserted when the PWM signal is high, where the SCS_Q72 is asserted after 85 cycles, and the SCS_Q73 is confirmed after 150 cycles, as shown in Figure 5.6a. On the other hand, the stages control signals of the transistors $Q8_1$, $Q8_2$ and $Q8_3$ are confirmed when the PWM signal is low, as shown in Figure 5.6b.



(a) Digital signals of the transistors $Q7_{1..3}$ during their switching process.



(b) Digital signals of the transistors $Q8_{1..3}$ during their switching process.

Figure 5.6: Digital signals of the stages transistors with the delay times.

The En signal is inserted using an external switch which is de-bounced using digital circuits.

5.3 The Switch De-bouncer Circuit

As long as an external switch is used to confirm the enable signal EN, the switch signal requires to be debounced using a digital circuit.

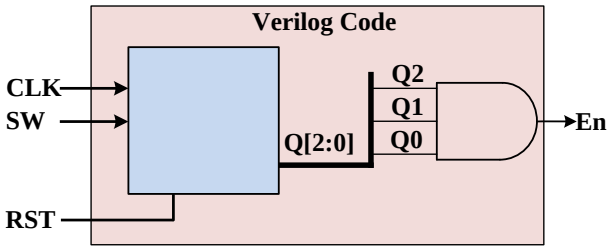


Figure 5.7: Schematic block of the digital de-bouncer circuit.

Figure 5.7 illustrates the schematic block of the switch de-bouncer, which is designed using a Verilog code. When the switch is turned on, its signal is sampled based on the clock signal. As can be seen from Figure 5.8, the En signal is asserted after 3 clock cycles

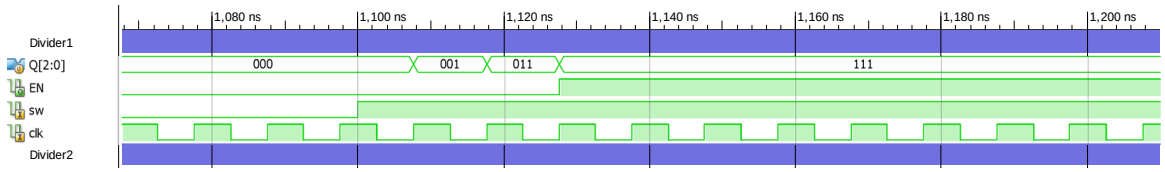


Figure 5.8: Digital signals of the digital de-bouncer circuit.

when the switch SW is turned on. This implies that a delay time, which is equal to 30 ns, is added before the En signal assertion. The design increases the SCS generator outputs accuracy during the operation.

Figure 5.9 shows all signals of the SCS generator and other parts during the operation.

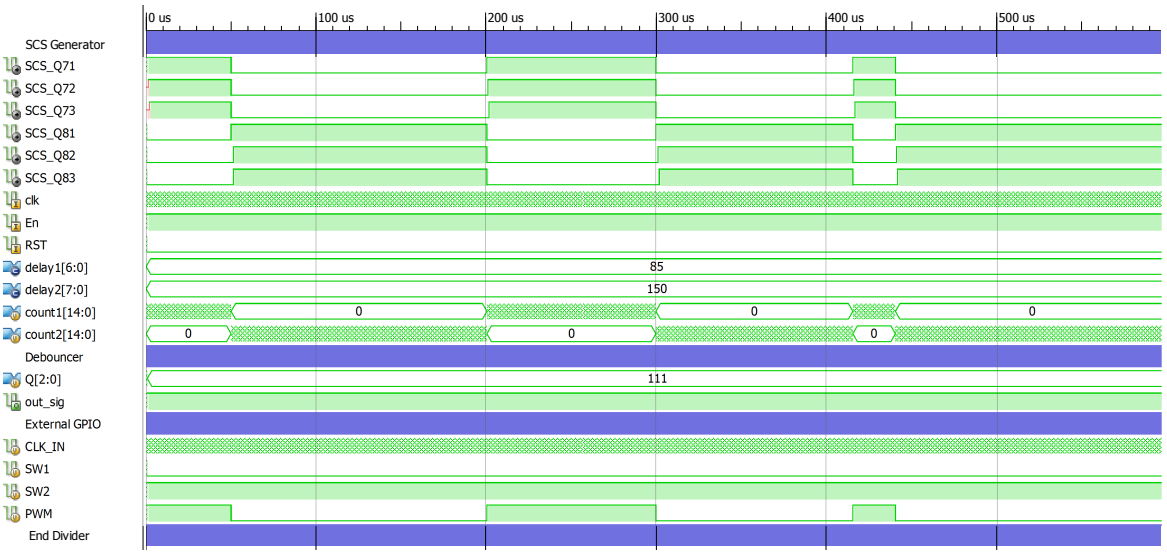


Figure 5.9: Digital signals of SCS generator during the operation.

5.4 Experimental Results

The schematic block shown in Figure 5.10 is an assembly of several designs which were tested on the proposed FPGA board. Verilog top level is used to interface to the blocks. This design is used to test the SCS generator. All the components of the design are built using the Verilog language. The structure of SCS generator was mentioned before. The other components are used to generate the PWM signal for testing. The main frequency is 150 MHz, it is the input frequency of the clock wizard. The clock wizard generates two frequencies 100 MHz and 5 MHz. The first one is used by all components whereas the second one is used to control data by two external push buttons. As can be seen from Figure 5.10, the design is composed of inputs and outputs signals. The User Constraint File (UCF)

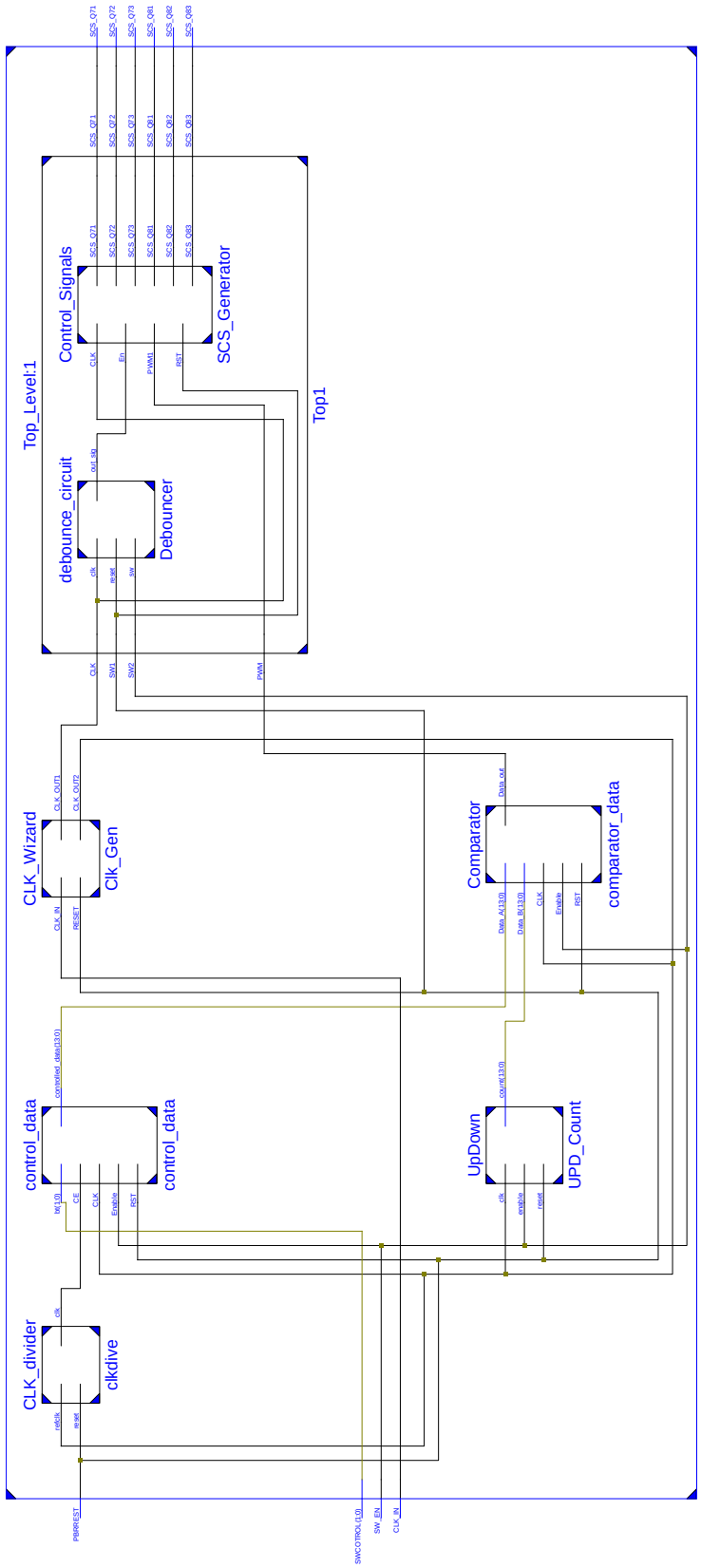


Figure 5.10: Schematic block of the Verilog top level for testing

is used to select the location of these signals[8]. Generally, ChipScope core is added to the design for monitoring the signals. Figure 5.11 illustrates the digital signals of the SCS generator which are monitored using ChipScope core. As can be seen from Figure 5.11, when the PWM signal has rising edge, the signals SCS_Q71, SCS_Q72, and SCS_Q73 are confirmed sequentially, for controlling the IGBT gate resistors during the turn-on. On the other hand, when the PWM signal has falling edge, the signals SCS_Q81, SCS_Q82 and SCS_Q83 are also asserted sequentially, for controlling the IGBT gate resistors during the turn-off. The FPGA output waveforms which control the driver stages transistors $Q7_1$, $Q7_2$ and $Q7_3$ are shown in Figure 5.13, and the FPGA output waveforms which control the driver stages transistors $Q8_1$, $Q8_2$ and $Q8_3$ are shown in Figure 5.14.

Additionally, the power supplies of the IGBT gate driver FPGA and the internal temperature of the FPGA device can be monitored during the SCS generator operation. As can be seen from Figure 5.15, the current Die temperature of the FPGA device is always 37.5 °C, the current value of VCCIN and VCCBRAM are 0.996 V, and the present value of VCCAUX is 1.796 V. This means that all the values are in the acceptable range.

[8]Xilinx PlanAhead software is used for this purpose, see appendix D.3.

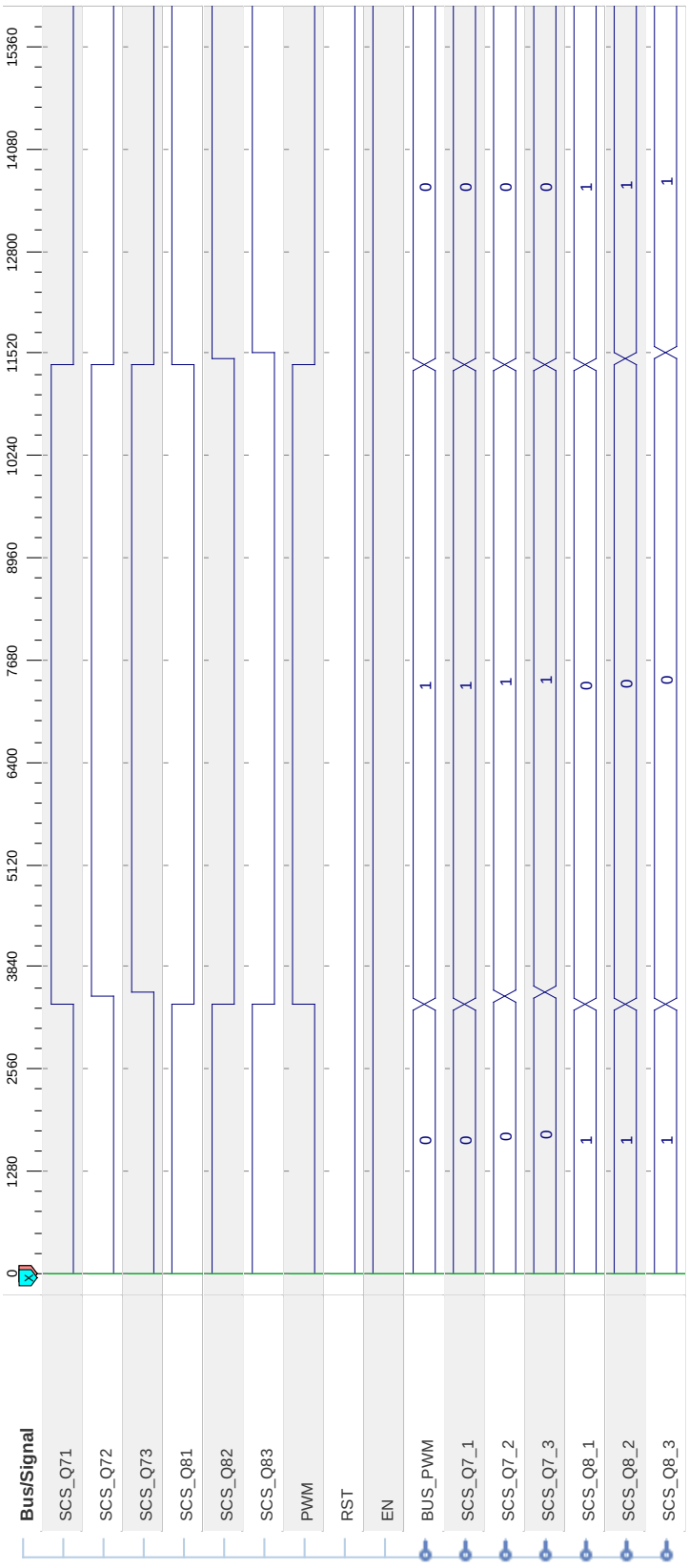


Figure 5.11: Monitoring of internal digital signals in the FPGA board using ChipScop core

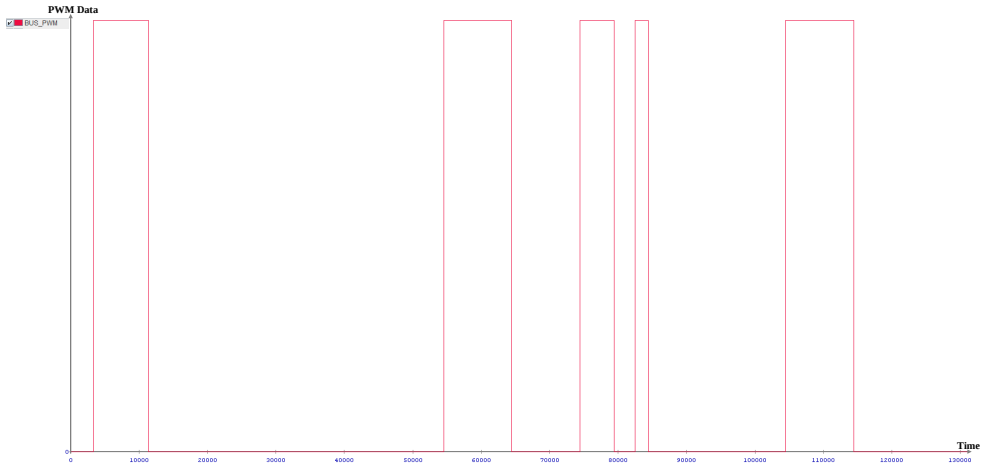


Figure 5.12: Waveform of the generated PWM based on FPGA controller.

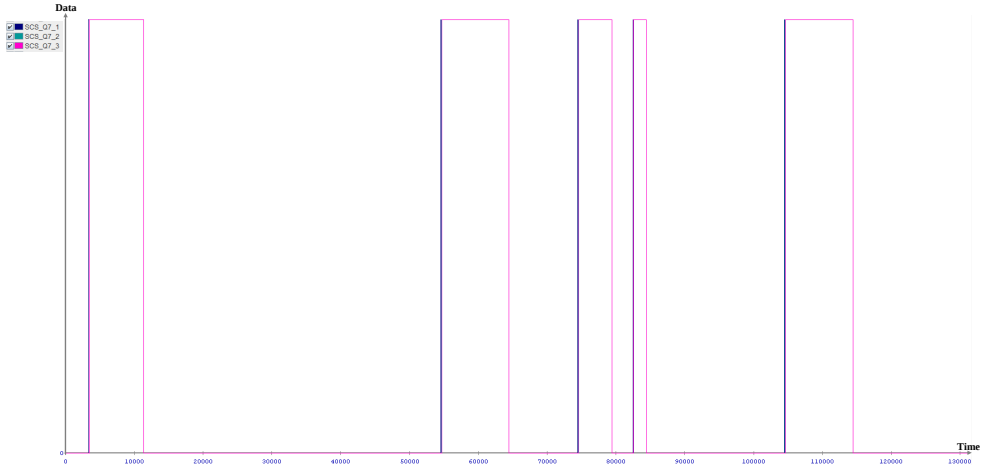


Figure 5.13: Waveforms of the transistors $Q7_{1..3}$ during their switching operation

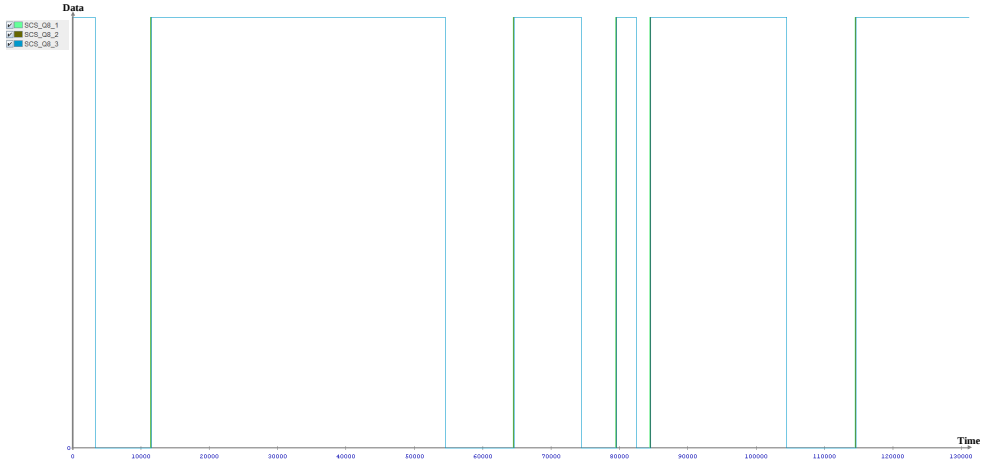


Figure 5.14: Waveforms of the transistors $Q8_{1..3}$ during their switching operation.

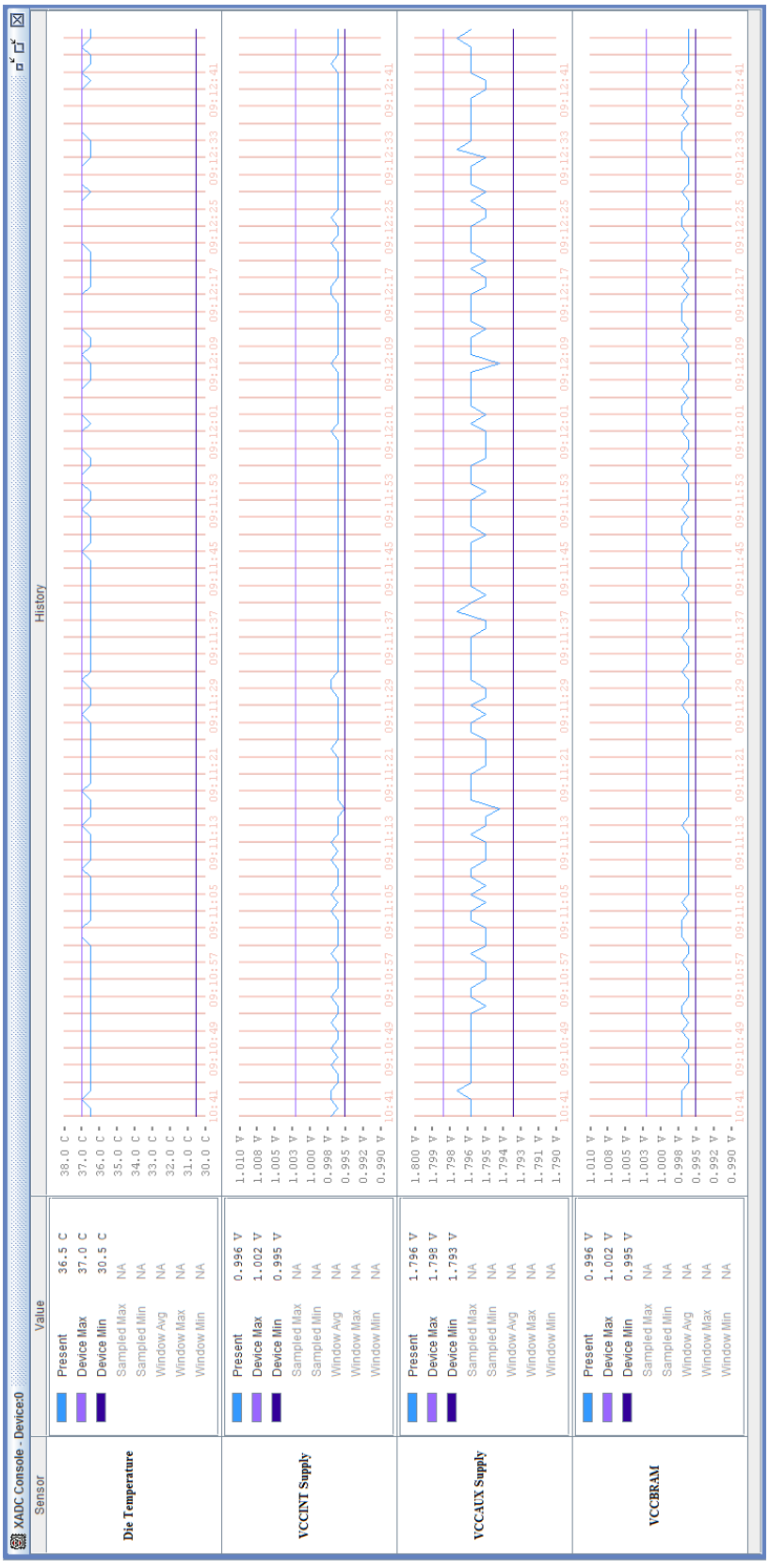


Figure 5.15: Monitoring of powers supplies and Die temperature in the FPGA board during the SCS generator operation using ChipScop core

Chapter 6

Conclusion

The usage of Field Programmable Gate arrays (FPGAs) in industrial automation systems of factories are very wide. However, their usage are limited in the control applications and drive systems, and few research are concerned withe the FPGAs usage in the diagnosis and fault detection. Therefore, the thesis is focused on the FPGAs usage in the fault diagnosis of inverter IGBT transistors during the switching process.

A new IGBT gate driver architecture is developed to integrate the diagnostic functions. These functions allow analyzing the IGBT quantities I_G, V_{GE} and V_{CE} during the switching process. For this purpose, high speed parallel ADC converters are proposed. Multiple gate stages are designed for realization of variable gate resistance by sequential switching. Three parallel gate driver stages are used for one transistor in the power inverter. The usage of these parallel driver stages allows controlling the external IGBT gate resistors during the IGBT switching process. Driver interface to inverter control system with data exchange is designed, where the insulated SPI interface is used for this purpose.

FPGA board was designed and integrated to the IGBT gate driver. The FPGA device used in the design has two types of I/O Banks, high-performance (HP) and high-range (HR) I/O Banks. One of HP I/O Banks is used to interface a DDR2SDRAM memory to the FPGA device with a voltage 1.8 V. The HR I/O Banks are designed to support a range of I/O standards with voltages from 1.2 V to 3.3 V. These Banks are used to interface the high speed parallel ADCs of the IGBT gate driver to the FPGA device. The FPGA board includes differential signals and single signals which can be provided from board to board connectors. The proposed FPGA board supports two configuration modes: JTAG/boundary-scan configuration mode and Master Serial Peripheral Interface (SPI) flash configuration mode (x4). These modes are used to download the designed software on the FPGA device. Two clock sources are used to clocking the FPGA device. The clocks frequency is 150 MHz. The FPGA device has also an integrated XADC which is composed of a dual 12 bit,1MSPS, ADCs. These ADCs can be configured to sample in continuous or event driven modes. Additionally, the XADC is used to monitor the power sources of FPGA banks and it can also be used to monitor the power system of the IGBT gate driver stages. An USB to UART bridge device is used to interface the PC to the FPGA device. The FPGA board was tested and the signals outputs were proper.

In addition to control the IGBT transistor switching, the FPGA board acquires the data from the ADCs converters during the switching event, where the FPGA device contains all the DSP tools for analyzing and quantitative evaluation.

Multiple power supplies for IGBT gate driver stages and for FPGA feeding were designed. Two insulated DC/DC converters are used to feed the drive system, where regulators are used to adjust the DC/DC converters outputs.

The Stages Control Signals (SCS) were generated using Verilog code. The designed generator generates six signals which are synchronized with the PWM signal which is generated by the main controller of the drive system. The input frequency of the generator is 100 MHz. The clocking wizard which is provided by the IP cores of FPGA devices is used to generate the generator frequency from the external clock source. Global reset is used to reconfigure the entire software when an error occurs. Additionally, an enable signal is used to activate the generator. When the PWM signal has rising edge, three signals are generated sequentially with predefined delays[1], for controlling the gate driver stages during the IGBT transistor turn-on, and when the PWM signal has falling edge, three signals are also generated sequentially with predefined delays, for controlling the gate driver stages during the IGBT transistor turn-off.
The SCS generator is designed to generate six signals for three gate driver stages. This gate driver can control one IGBT transistor switching during turn-on/turn-off, but the capability of HDL language (Verilog, VHDL) allows building at least 12 SCS generators which can be used in the fault-tolerant applications or in another applications of industrial automation.

6.1 Future Work

The author of the doctoral thesis suggests to explore the following:

- It would be interesting to develop the IGBT gate driver with integrated diagnostic functions to include three phase inverter with diagnosis and fault-tolerant control.
- It would be important to develop the FPGA board to include differential clock source which accelerates the speed of analyzing during the process.
- The implementation of mentioned steps above, requires the development of software to interface the inverter with drivers FPGAs to the main controller.

6.2 Contributions of the Thesis

The present state on power IGBT inverters diagnosis methods is summarized in this thesis, where the current diagnosis methods can be divided into the following categories:

1. The absolute normalized DC current method for open circuit protection.

[1]These delays can be set in accordance to the requirements of used IGBT.

2. The line to line voltage measurement for open circuit protection.
3. IGBT fault diagnosis based on the Park's vector method.
4. Using the gate charge and gate voltage as an indicator of the SC condition.
5. Using the V_{CE} to detect the SC fault.
6. Using stray inductance between Kelvin emitter and the power emitter for the fault sensing.
7. RS NAND Latch circuit for SC fault detection.
8. Measuring the temperature for fault detection and diagnosis in the drive system.
9. Using the fault tolerant control in the drive systems.

The thesis contributes to power inverter diagnosis field. The hardware architecture of the IGBT driver was developed. The architecture allows implementation of diagnosis methods based on IGBT switching process analysis. The aim of the methods is evaluation of power inverter components degradation during regular life. The methods can predict the oncoming failures and maintenance schedule. Many works deal with the diagnosis of power inverters, and fault tolerant inverter systems development. These techniques usually detect the inverter correct function or failing state and some inverter reconfiguration can be performed based on this diagnosis. The quantitative diagnosis methods development effort can be found in few recent works. The thesis results provide a base for future development of diagnosis methods using FPGAs at the Department of Power Electrical and Electronic Engineering.

The author personal benefits of the thesis can be seen as follows:

- Increasing his knowledge on power inverters, power inverters control.
- Increasing his knowledge of power transistors switching phenomena, driving techniques and drivers functionality.
- Becoming familiar with FPGAs programming.
- Becoming familiar with high speed Multilayer PCB design.

The new knowledge will be transferred to Syrian Universities at which the author will work in near future.

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Appendix A

The Connections Between (J11, J10, J20) and the FPGA

A.1 The J11 Connections to the FPGA

J11	Net Name	FPGA I/O	Pad Function
1	VCC_5V5MAX	NA	NA
2	VCC_3.3V	NA	NA
3	GND	NA	NA
4	GPIO_BANK13_DATA1	AA14	IO_L18P_T2_13
5	GPIO_BANK13_DATA2	AB15	IO_L16P_T2_13
6	GPIO_BANK13_DATA3	AA15	IO_L18N_T2_13
7	GPIO_BANK13_DATA4	AB16	IO_L16N_T2_13
8	GPIO_BANK13_DATA5	AA16	IO_L17P_T2_13
9	GPIO_BANK13_DATA6	AB17	IO_L17N_T2_13
10	GPIO_BANK13_DATA7	AB18	IO_L15N_T2_DQS_13
11	GPIO_BANK13_DATA8	AA18	IO_L15P_T2_DQS_13
12	GPIO_BANK13_DATA9	AA19	IO_L10P_T1_13
13	GPIO_BANK13_DATA10	AB20	IO_L10N_T1_13
14	GPIO_BANK13_DATA11	AA20	IO_L8P_T1_13
15	GPIO_BANK13_DATA12	AB21	IO_L8N_T1_13
16	GPIO_BANK13_DATA13	AA21	IO_L9P_T1_DQS_13
17	GPIO_BANK13_DATA14	AB22	IO_L9N_T1_DQS_13
18	GPIO_BANK13_DATA15	Y21	IO_L7P_T1_13
19	GPIO_BANK13_DATA16	Y22	IO_L7N_T1_13
20	GPIO_BANK13_DATA17	W21	IO_L4P_T0_13
21	GPIO_BANK13_DATA18	W22	IO_L4N_T0_13
22	GPIO_BANK13_DATA19	V22	IO_L2N_T0_13

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Table A.1 – continued from previous page

J11	Net Name	FPGA I/O	Pad Function
23	GPIO_BANK13_DATA20	U22	IO_L2P_T0_13
24	GPIO_BANK13_DATA21	U21	IO_L1N_T0_13
25	GPIO_BANK14_DATA3	N20	IO_L17P_T2_A14_D30_14
26	GPIO_BANK14_DATA4	M20	IO_L18P_T2_A12_D28_14
27	GPIO_BANK14_DATA14	L20	IO_L12N_T1_MRCC_14
28	GPIO_BANK14_DATA15	K19	IO_L5N_T0_D07_14
29	GPIO_BANK14_DATA16	L18	IO_L5P_T0_D06_14
30	GPIO_BANK14_DATA17	K17	IO_L6N_T0_D08_VREF_14
31	GPIO_BANK14_DATA18	G20	IO_L4P_T0_D04_14
32	GPIO_BANK14_DATA19	F20	IO_L4N_T0_D05_14
33	GPIO_BANK14_DATA20	P21	IO_L22P_T3_A05_D21_14
34	GPIO_BANK14_DATA21	M21	IO_L17N_T2_A13_D29_14
35	GPIO_BANK14_DATA22	P22	IO_L22N_T3_A04_D20_14
36	GPIO_BANK14_DATA23	L19	IO_L12P_T1_MRCC_14
37	GPIO_BANK14_DATA13	J20	IO_L11P_T1_SRCC_14
38	GND	NA	NA
39	VN_0_N	M11	VN_0
40	VP_0_P	L12	VP_0
41	GND	NA	NA
42	VAUX_AD0_N	G16	IO_L1N_T0_AD0N_15
43	VAUX_AD0_P	G15	IO_L1P_T0_AD0P_15
44	GND	NA	NA
45	VAUX_AD1_N	F16	IO_L3N_T0_DQS_AD1N_15
46	VAUX_AD1_P	F15	IO_L3P_T0_DQS_AD1P_15
47	GND	NA	NA
48	VREFP_0	NA	NA
49	VCCO_3.3V	NA	NA
50	VCC_5V5MAX	NA	NA
51	VCC_5V5MAX	NA	NA
52	VCCO_3.3V	NA	NA
53	GND	NA	NA
54	GPIO_BANK13_DATA22	Y14	IO_L22N_T3_13
55	GPIO_BANK13_DATA23	W14	IO_L22P_T3_13
56	GPIO_BANK13_DATA24	W15	IO_L23N_T3_13
57	GPIO_BANK13_DATA25	Y16	IO_L21N_T3_DQS_13
58	GPIO_BANK13_DATA26	W16	IO_L21P_T3_DQS_13
59	GPIO_BANK13_DATA27	Y17	IO_L14N_T2_SRCC_13
60	GPIO_BANK13_DATA28	Y18	IO_L13P_T2_MRCC_13

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Table A.1 – continued from previous page

J11	Net Name	FPGA I/O	Pad Function
61	GPIO_BANK13_DATA29	W17	IO_L14P_T2_SRCC_13
62	GPIO_BANK13_DATA30	Y19	IO_L13N_T2_MRCC_13
63	GPIO_BANK13_DATA31	W19	IO_L12N_T1_MRCC_13
64	GPIO_BANK13_DATA32	W20	IO_L11N_T1_SRCC_13
65	GPIO_BANK13_DATA33	V19	IO_L12P_T1_MRCC_13
66	GPIO_BANK13_DATA34	V20	IO_L11P_T1_SRCC_13
67	GPIO_BANK13_DATA35	U20	IO_L6N_T0_VREF_13
68	GPIO_BANK13_DATA36	T20	IO_L6P_T0_13
69	GPIO_BANK13_DATA37	V14	IO_25_13
70	GPIO_BANK13_DATA38	U15	IO_L24N_T3_13
71	GPIO_BANK13_DATA39	T15	IO_L24P_T3_13
72	GPIO_BANK13_DATA40	U16	IO_L19P_T3_13
73	GPIO_BANK13_DATA41	V17	IO_L19N_T3_VREF_13
74	GPIO_BANK13_DATA42	V18	IO_L5N_T0_13
75	GPIO_BANK13_DATA43	U18	IO_L3N_T0_DQS_13
76	GPIO_BANK13_DATA44	U17	IO_L5P_T0_13
77	GPIO_BANK13_DATA45	T19	IO_0_13
78	GPIO_BANK13_DATA46	T21	IO_L1P_T0_13
79	GPIO_BANK13_DATA47	V15	IO_L23P_T3_13
80	GPIO_BANK13_DATA48	T16	IO_L20N_T3_13
81	GPIO_BANK13_DATA49	R16	IO_L20P_T3_13
82	GPIO_BANK13_DATA50	T18	IO_L3P_T0_DQS_13
83	GPIO_BANK14_DATA1	P19	IO_L20P_T3_A08_D24_14
84	GPIO_BANK14_DATA2	P20	IO_L20N_T3_A07_D23_14
85	GPIO_BANK14_DATA5	R17	IO_L21P_T3_DQS_14
86	GPIO_BANK14_DATA6	P16	IO_L23P_T3_A03_D19_14
87	GPIO_BANK14_DATA7	P17	IO_L21N_T3_DQS_A06_D22_14
88	GPIO_BANK14_DATA8	N19	IO_L13N_T2_MRCC_14
89	GPIO_BANK14_DATA9	M18	IO_L14N_T2_SRCC_14
90	GPIO_BANK14_DATA10	M17	IO_L14P_T2_SRCC_14
91	GPIO_BANK14_DATA11	N17	IO_L23N_T3_A02_D18_14
92	GPIO_BANK14_DATA12	H20	IO_L11N_T1_SRCC_14
93	GND	NA	NA
94	VAUX_AD12_N	D16	IO_L11N_T1_SRCC_AD12N_15
95	VAUX_AD12_P	D15	IO_L11P_T1_SRCC_AD12P_15
96	GND_ADC	NA	NA
97	GND	NA	NA
98	VREFP_0	NA	NA

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Table A.1 – continued from previous page

J11	Net Name	FPGA I/O	Pad Function
99	VCCO_3.3V	NA	NA
100	VCC_5V5MAX	NA	NA

Table A.1: The Connection Between board to board connector (J10) and the FPGA

A.2 The J10 Connections to the FPGA

J10	Net Name	FPGA Pin	Pad Function
1	VCC_5V5MAX	NA	NA
2	VCC_3.3V	NA	NA
3	VCCAUX	NA	NA
4	GND	NA	NA
5	NC	NA	NA
6	GND	NA	NA
7	GND	NA	NA
8	NC	NA	NA
9	GPIO_BANK16_DATA19	F11	IO_L11P_T1_SRCC_16
10	GPIO_BANK16_DATA18	F10	IO_L11N_T1_SRCC_16
11	GPIO_BANK16_DATA17	E11	IO_L12P_T1_MRCC_16
12	GPIO_BANK16_DATA16	D10	IO_L7P_T1_16
13	GPIO_BANK16_DATA15	D9	IO_L19P_T3_16
14	GPIO_BANK16_DATA14	C9	IO_L19N_T3_VREF_16
15	GPIO_BANK16_DATA13	E9	IO_L15N_T2_DQS_16
16	GPIO_BANK16_DATA12	E8	IO_24_T3_16
17	GPIO_BANK16_DATA11	F8	IO_L17N_T2_16
18	GND	NA	AN
19	GPIO_BANK16_DATA10	D11	IO_L12N_T1_MRCC_16
20	GPIO_BANK16_DATA9	C10	IO_L7N_T1_16
21	GPIO_BANK16_DATA8	A11	IO_L23P_T3_16
22	GPIO_BANK16_DATA7	B11	IO_L20P_T3_16
23	GPIO_BANK16_DATA6	A10	IO_L23N_T3_16
24	GPIO_BANK16_DATA5	B10	IO_L20N_T3_16
25	GPIO_BANK16_DATA4	A9	IO_L21P_T3_DQS_16
26	GPIO_BANK16_DATA3	A8	IO_L21N_T3_DQS_16
27	GPIO_BANK16_DATA2	B8	IO_L22N_T3_16
28	GPIO_BANK16_DATA1	C8	IO_L22P_T3_16

Continued on next page

Table A.2 – continued from previous page

J10	Net Name	FPGA Pin	Pad Function
29	GND	NA	NA
30	DIFF_DATA1_P	AA5	IO_L1P_T0_33
31	DIFF_DATA1_N	AB5	IO_L1N_T0_33
32	GND	NA	NA
33	DIFF_DATA2_P	AA6	IO_L3P_T0_DQS_33
34	DIFF_DATA2_N	AB6	IO_L3N_T0_DQS_33
35	GND	NA	NA
36	DIFF_DATA3_N	AB7	IO_L2N_T0_33
37	DIFF_DATA3_P	AB8	IO_L2P_T0_33
38	GND	NA	NA
39	DIFF_DATA4_N	AA8	IO_L5N_T0_33
40	DIFF_DATA4_P	AA9	IO_L5P_T0_33
41	GND	NA	NA
42	DIFF_DATA5_N	AB10	IO_L4N_T0_33
43	DIFF_DATA5_P	AA10	IO_L4P_T0_33
44	GND	NA	NA
45	DIFF_DATA6_N	AB11	IO_L20N_T3_33
46	DIFF_DATA6_P	AA11	IO_L20P_T3_33
47	GND	NA	NA
48	DIFF_DATA7_N	AB12	IO_L22N_T3_33
49	DIFF_DATA7_P	AB13	IO_L22P_T3_33
50	GND	NA	NA
51	VCC_5V5MAX	NA	NA
52	VCCO_3.3V	NA	NA
53	VCCAUX	NA	NA
54	GND	NA	NA
55	DIFF_DATA22_P	U8	IO_L9P_T1_DQS_33
56	DIFF_DATA22_N	V8	IO_L9N_T1_DQS_33
57	GND	NA	NA
58	DIFF_DATA21_N	T8	IO_L18N_T2_33
59	DIFF_DATA21_P	T9	IO_L18P_T2_33
60	GND	NA	NA
61	DIFF_DATA20_N	T10	IO_L16N_T2_33
62	DIFF_DATA20_P	T11	IO_L16P_T2_33
63	GND	NA	NA
64	DIFF_DATA19_P	T13	IO_L24P_T3_33
65	DIFF_DATA19_N	U13	IO_L24N_T3_33
66	GND	NA	NA

Continued on next page

Table A.2 – continued from previous page

J10	Net Name	FPGA Pin	Pad Function
67	DIFF_DATA18_N	W7	IO_L11N_T1_SRCC_33
68	DIFF_DATA18_P	V7	IO_L11P_T1_SRCC_33
69	GND	NA	NA
70	DIFF_DATA17_N	V9	IO_L14N_T2_SRCC_33
71	DIFF_DATA17_P	U10	IO_L14P_T2_SRCC_33
72	GND	NA	NA
73	DIFF_DATA16_N	U11	IO_L17N_T2_33
74	DIFF_DATA16_P	U12	IO_L17P_T2_33
75	GND	NA	NA
76	DIFF_DATA15_N	V12	IO_L23N_T3_33
77	DIFF_DATA15_P	V13	IO_L23P_T3_33
78	GND	NA	NA
79	DIFF_DATA14_P	Y13	IO_L21P_T3_DQS_33
80	DIFF_DATA14_N	AA13	IO_L21N_T3_DQS_33
81	GND	NA	NA
82	DIFF_DATA8_N	Y6	IO_L7N_T1_33
83	DIFF_DATA8_P	W6	IO_L7P_T1_33
84	GND	NA	NA
85	DIFF_DATA9_N	Y7	IO_L12N_T1_MRCC_33
86	DIFF_DATA9_P	Y8	IO_L12P_T1_MRCC_33
87	GND	NA	NA
88	DIFF_DATA10_P	W9	IO_L13P_T2_MRCC_33
89	DIFF_DATA10_N	Y9	IO_L13N_T2_MRCC_33
90	GND	NA	NA
91	DIFF_DATA11_N	W10	IO_L15N_T2_DQS_33
92	DIFF_DATA11_P	V10	IO_L15P_T2_DQS_33
93	GND	NA	NA
94	NC	NA	NA
95	GPIO_BANK33_DATA12	W11	IO_L6P_T0_33
96	GND_ADC	NA	
97	GPIO_BANK33_DATA13	W12	IO_L19P_T3_33
98	NC	NA	NA
99	GND	NA	NA
100	GND	NA	NA

Table A.2: The connection between board to board Connector (J10) and the FPGA

A.3 The J12 Connections to The FPGA

J12	Net Name	FPGAI Pin	Pad Function
1	VCCO_3.3V	NA	NA
2	GND	NA	NA
3	GPIO_BANK15_DATA5	D12	IO_0_15
4	GPIO_BANK15_DATA6	E14	IO_L6P_T0_15
5	GPIO_BANK15_DATA7	D14	IO_L6N_T0_VREF_15
6	GPIO_BANK15_DATA8	E16	IO_L14P_T2_SRCC_15
7	GPIO_BANK15_DATA9	D17	IO_L14N_T2_SRCC_15
8	GPIO_BANK15_DATA10	E17	IO_L13P_T2_MRCC_15
9	GPIO_BANK15_DATA11	E18	IO_L13N_T2_MRCC_15
10	GPIO_BANK15_DATA12	C19	IO_L19P_T3_A22_15
11	GPIO_BANK15_DATA13	C20	IO_L19N_T3_A21_VREF_15
12	GPIO_BANK15_DATA14	D19	IO_L18P_T2_A24_15
13	GPIO_BANK15_DATA15	D20	IO_L18N_T2_A23_15
14	GPIO_BANK15_DATA16	E19	IO_L17N_T2_A25_15
15	GND	NA	NA
16	GND	NA	NA
17	GPIO_BANK15_DATA17	B21	IO_L24N_T3_RS0_15
18	GPIO_BANK15_DATA18	B22	IO_L21N_T3_DQS_A18_15

Table A.3: Connection between J12 and the FPGA

Appendix B

UCF Design

B.1 The User Constraint File (UCF) of Auxiliary Inputs Connected to J11 and J4

```
NET "VAUX_AD0_N"  LOC = G16 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD0_P"  LOC = G15 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD1_N"  LOC = F16 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD1_P"  LOC = F15 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD2_N"  LOC = B13 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD2_P"  LOC = C13 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD3_N"  LOC = A16 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD3_P"  LOC = B16 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD4_N"  LOC = A18 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD4_P"  LOC = B17 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD5_N"  LOC = C18 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD5_P"  LOC = C17 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD8_N"  LOC = B12 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD8_P"  LOC = C12 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD9_N"  LOC = A14 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD9_P"  LOC = A13 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD10_N" LOC = C15 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD10_P" LOC = C14 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD11_N" LOC = A15 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD11_P" LOC = B15 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD12_N" LOC = D16 | IOSTANDARD = LVCMOS33;
NET "VAUX_AD12_P" LOC = D15 | IOSTANDARD = LVCMOS33;
```

In addition, The connector J4 has four pins connect to FPGA pins. These pins can be used as digital I/O. We can write the UCF as the following:

```
NET "GPIO_BANK15_DATA1" LOC = A19 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA2" LOC = A20 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA3" LOC = B20 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA4" LOC = A21 | IOSTANDARD = LVCMOS33;
```

B.2 The UCF of DDR2 SDRAM Memory

```
NET "ddr2_dq[0]"     LOC = "AB2" | IOSTANDARD = SSTL18_II_T_DCI;
NET "ddr2_dq[1]"     LOC = "AA3" | IOSTANDARD = SSTL18_II_T_DCI;
NET "ddr2_dq[2]"     LOC = "W1"  | IOSTANDARD = SSTL18_II_T_DCI;
NET "ddr2_dq[3]"     LOC = "AB1" | IOSTANDARD = SSTL18_II_T_DCI;
NET "ddr2_dq[4]"     LOC = "Y1"  | IOSTANDARD = SSTL18_II_T_DCI;
NET "ddr2_dq[5]"     LOC = "AA1" | IOSTANDARD = SSTL18_II_T_DCI;
NET "ddr2_dq[6]"     LOC = "AB3" | IOSTANDARD = SSTL18_II_T_DCI;
NET "ddr2_dq[7]"     LOC = "AA4" | IOSTANDARD = SSTL18_II_T_DCI;
NET "ddr2_ba[0]"     LOC = "U1"  | IOSTANDARD = SSTL18_II;
NET "ddr2_ba[1]"     LOC = "T1"  | IOSTANDARD = SSTL18_II;
NET "ddr2_ba[2]"     LOC = "N4"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[0]"   LOC = "R2"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[1]"   LOC = "N3"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[2]"   LOC = "P1"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[3]"   LOC = "M5"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[4]"   LOC = "K3"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[5]"   LOC = "R1"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[6]"   LOC = "L1"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[7]"   LOC = "M3"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[8]"   LOC = "K2"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[9]"   LOC = "N2"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[10]"  LOC = "P2"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[11]"  LOC = "L3"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[12]"  LOC = "L5"  | IOSTANDARD = SSTL18_II;
NET "ddr2_addr[13]"  LOC = "K1"  | IOSTANDARD = SSTL18_II;
NET "ddr2_ras_n"     LOC = "P4"  | IOSTANDARD = SSTL18_II;
NET "ddr2_cas_n"     LOC = "R4"  | IOSTANDARD = SSTL18_II;
NET "ddr2_we_n"      LOC = "R3"  | IOSTANDARD = SSTL18_II;
NET "ddr2_cke[0]"    LOC = "U2"  | IOSTANDARD = SSTL18_II;
NET "ddr2_odt[0]"    LOC = "V2"  | IOSTANDARD = SSTL18_II;
NET "ddr2_dm[0]"     LOC = "W5"  | IOSTANDARD = SSTL18_II;
NET "ddr2_cs_n[0]"   LOC = "T3"  | IOSTANDARD = SSTL18_II;
```

```
NET "ddr2_dqs_p[0]" LOC = "Y3"  | IOSTANDARD = DIFF_SSTL18_II_T_DCI;
NET "ddr2_dqs_n[0]" LOC = "Y2"  | IOSTANDARD = DIFF_SSTL18_II_T_DCI;
NET "ddr2_ck_p[0]"  LOC = "M2"  | IOSTANDARD = DIFF_SSTL18_II;
NET "ddr2_ck_n[0]"  LOC = "M1"  | IOSTANDARD = DIFF_SSTL18_II;
CONFIG INTERNAL_VREF_BANK34= 0.900;
```

B.3 UCF of UART Port

```
NET "TXD" LOC = "R22"  | IOSTANDARD = LVCMOS33;
NET "RXD" LOC = "R21"  | IOSTANDARD = LVCMOS33;
NET "RTS" LOC = "R18"  | IOSTANDARD = LVCMOS33;
NET "CTS" LOC = "R19"  | IOSTANDARD = LVCMOS33;
```

B.4 UCF of GPIO Leds

```
NET "GPIO_LED_1" LOC = "D22"  | IOSTANDARD = LVCMOS33;
NET "GPIO_LED_0" LOC = "C22"  | IOSTANDARD = LVCMOS33;
```

B.5 UCF of Board to Board Connector J11

```
NET "GPIO_BANK13_DATA1"  LOC = AA14  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA2"  LOC = AB15  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA3"  LOC = AA15  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA4"  LOC = AB16  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA5"  LOC = AA16  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA6"  LOC = AB17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA7"  LOC = AB18  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA8"  LOC = AA18  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA9"  LOC = AA19  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA10" LOC = AB20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA11" LOC = AA20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA12" LOC = AB21  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA13" LOC = AA21  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA14" LOC = AB22  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA15" LOC = Y21   | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA16" LOC = Y22   | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA17" LOC = W21   | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA18" LOC = W22   | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA19" LOC = V22   | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA20" LOC = U22   | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA21" LOC = U21   | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA3"  LOC = N20   | IOSTANDARD = LVCMOS33;
```

```
NET "GPIO_BANK14_DATA4"  LOC = M20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA14" LOC = L20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA15" LOC = K19  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA16" LOC = L18  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA17" LOC = K17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA18" LOC = G20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA19" LOC = F20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA20" LOC = P21  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA21" LOC = M21  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA13" LOC = J20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA22" LOC = Y14  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA23" LOC = W14  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA24" LOC = W15  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA25" LOC = Y16  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA26" LOC = W16  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA27" LOC = Y17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA28" LOC = Y18  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA29" LOC = W17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA30" LOC = Y19  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA31" LOC = W19  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA32" LOC = W20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA33" LOC = V19  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA34" LOC = V20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA35" LOC = U20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA36" LOC = T20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA37" LOC = V14  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA38" LOC = U15  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA39" LOC = T15  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA40" LOC = U16  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA41" LOC = V17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA42" LOC = V18  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA43" LOC = U18  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA44" LOC = U17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA45" LOC = T19  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA46" LOC = T21  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA47" LOC = V15  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA48" LOC = T16  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA49" LOC = R16  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK13_DATA50" LOC = T18  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA1"  LOC = P19  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA2"  LOC = P20  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA5"  LOC = R17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA6"  LOC = P16  | IOSTANDARD = LVCMOS33;
```

```
NET "GPIO_BANK14_DATA7"  LOC = P17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA8"  LOC = N19  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA9"  LOC = M18  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA10" LOC = M17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA11" LOC = N17  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK14_DATA12" LOC = H20  | IOSTANDARD = LVCMOS33;
```

B.6 UCF of Board to Board Connector J10

B.6.1 UCF of Differential Signal Pairs

```
NET "DIFF_DATA1_P"  LOC = "AA5"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA1_N"  LOC = "AB5"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA2_P"  LOC = "AA6"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA2_N"  LOC = "AB6"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA3_P"  LOC = "AB8"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA3_N"  LOC = "AB7"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA4_P"  LOC = "AA9"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA4_N"  LOC = "AA8"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA5_P"  LOC = "AA10" | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA5_N"  LOC = "AB10" | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA6_P"  LOC = "AA11" | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA6_N"  LOC = "AB11" | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA7_P"  LOC = "AB13" | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA7_N"  LOC = "AB12" | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA8_P"  LOC = "W6"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA8_N"  LOC = "Y6"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA9_P"  LOC = "Y8"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA9_N"  LOC = "Y7"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA10_P" LOC = "W9"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA10_N" LOC = "Y9"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA11_P" LOC = "V10"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA11_N" LOC = "W10"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA14_P" LOC = "Y13"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA14_N" LOC = "AA13" | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA15_P" LOC = "V13"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA15_N" LOC = "V12"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA16_P" LOC = "U12"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA16_N" LOC = "U11"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA17_P" LOC = "U10"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA17_N" LOC = "V9"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA18_P" LOC = "V7"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA18_N" LOC = "W9"   | IOSTANDARD = DIFF_SSTL18_II;
```

```
NET "DIFF_DATA19_P"  LOC = "T13"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA19_N"  LOC = "U13"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA20_P"  LOC = "T11"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA20_N"  LOC = "T10"  | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA21_P"  LOC = "T9"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA21_N"  LOC = "T8"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA22_P"  LOC = "U8"   | IOSTANDARD = DIFF_SSTL18_II;
NET "DIFF_DATA22_N"  LOC = "V8"   | IOSTANDARD = DIFF_SSTL18_II;
```

B.6.2 UCF of Single-Ended Signals

```
NET "GPIO_BANK33_DATA12" LOC = W11 | IOSTANDARD = LVCMOS18;
NET "GPIO_BANK33_DATA13" LOC = W12 | IOSTANDARD = LVCMOS18;
NET "GPIO_BANK16_DATA1"  LOC = C8  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA2"  LOC = B8  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA3"  LOC = A8  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA4"  LOC = A9  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA5"  LOC = B10 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA6"  LOC = A10 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA7"  LOC = B11 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA8"  LOC = A11 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA9"  LOC = C10 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA10" LOC = D11 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA11" LOC = F8  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA12" LOC = E8  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA13" LOC = E9  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA14" LOC = C9  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA15" LOC = D9  | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA16" LOC = D10 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA17" LOC = E11 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA18" LOC = F10 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK16_DATA18" LOC = F11 | IOSTANDARD = LVCMOS33;
```

B.7 UCF of Connector J12

```
NET "GPIO_BANK15_DATA5"  LOC = D12 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA6"  LOC = E14 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA7"  LOC = D14 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA8"  LOC = E16 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA9"  LOC = D17 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA10" LOC = E17 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA11" LOC = E18 | IOSTANDARD = LVCMOS33;
```

```
NET "GPIO_BANK15_DATA12" LOC = C19 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA13" LOC = C20 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA14" LOC = D19 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA15" LOC = D20 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA16" LOC = E19 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA17" LOC = B21 | IOSTANDARD = LVCMOS33;
NET "GPIO_BANK15_DATA18" LOC = B22 | IOSTANDARD = LVCMOS33;
```

Appendix C

PCB Layout of the Design

C.1 PCB Layout of the FPGA

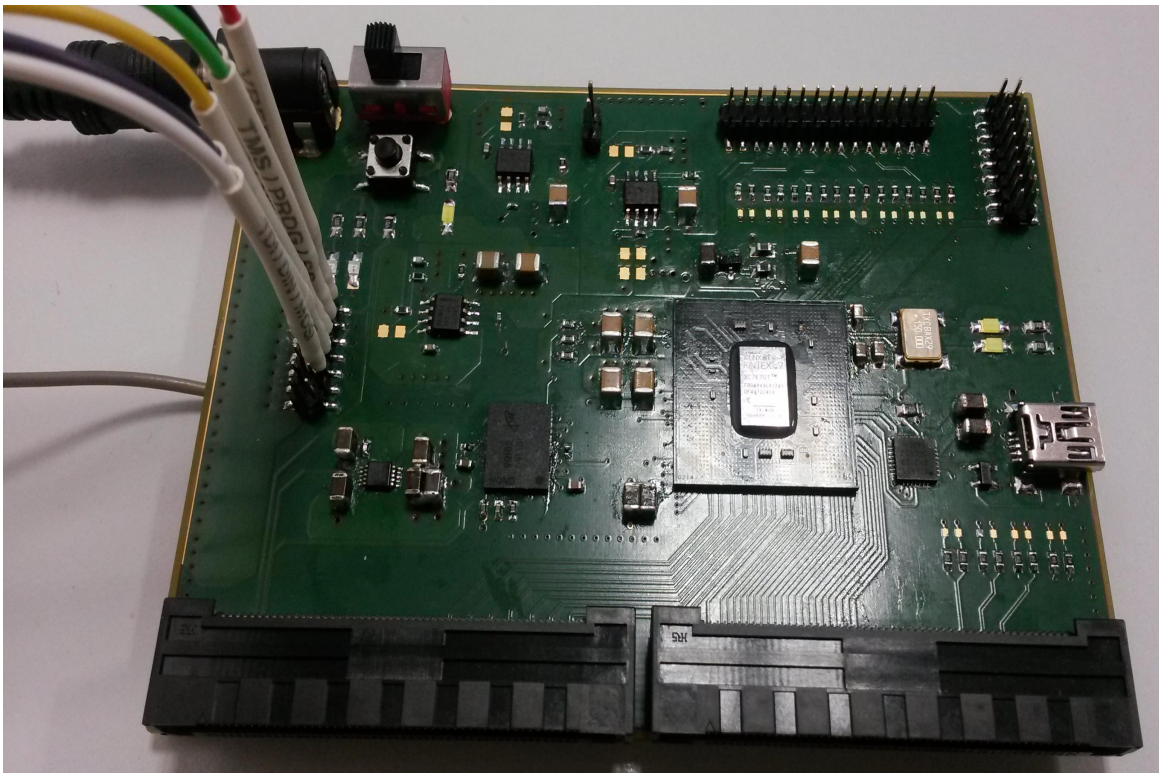
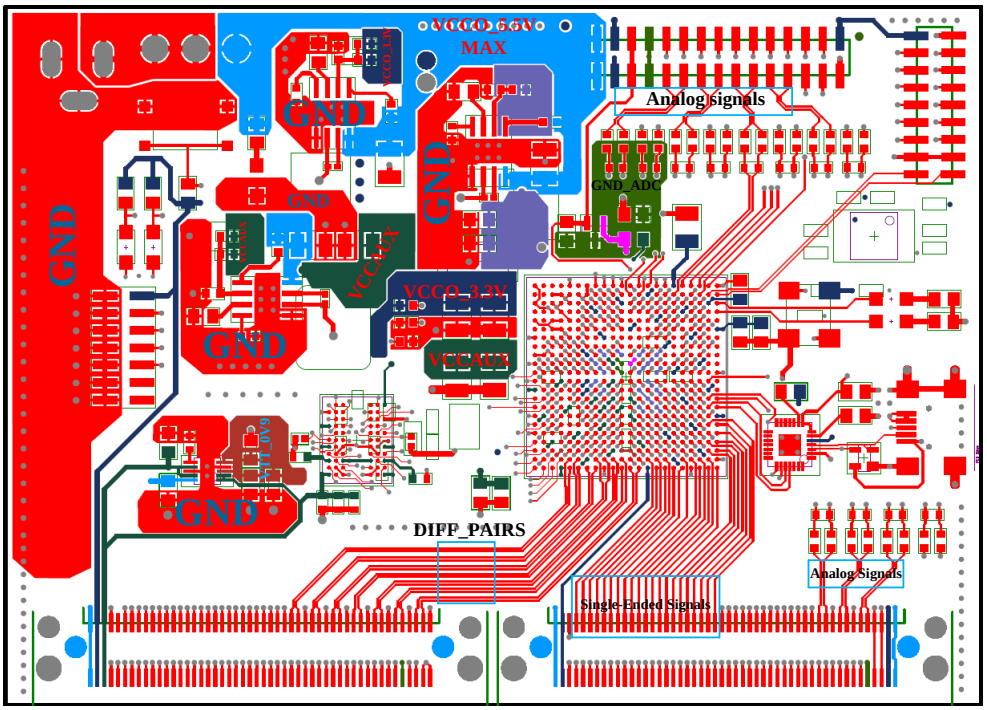
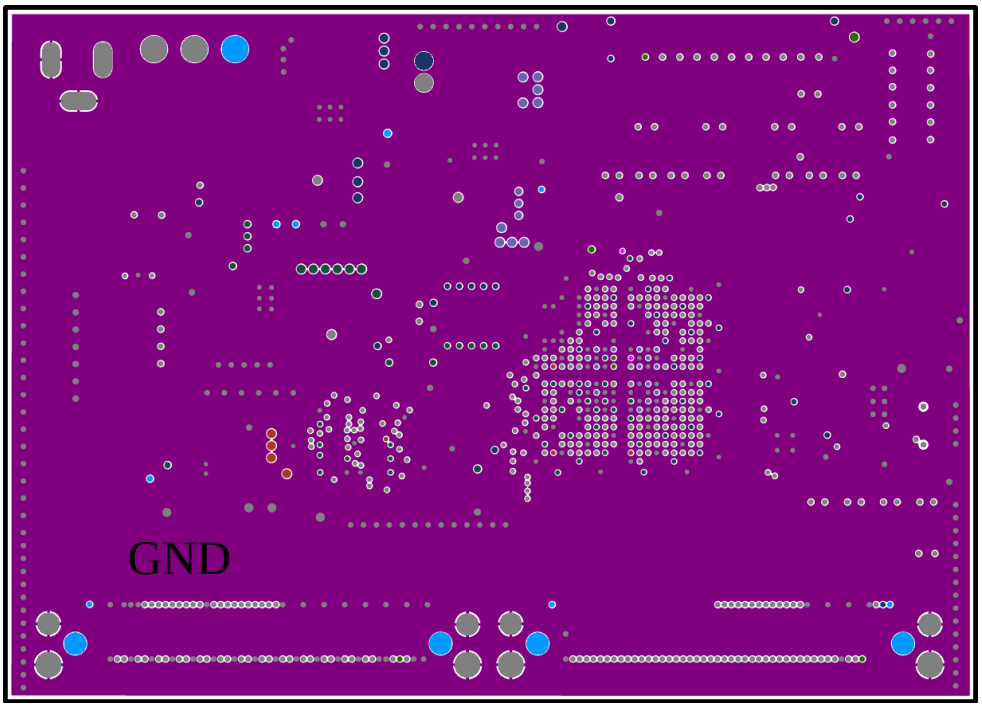


Figure C.1: The proposed FPGA board view after the fabrication

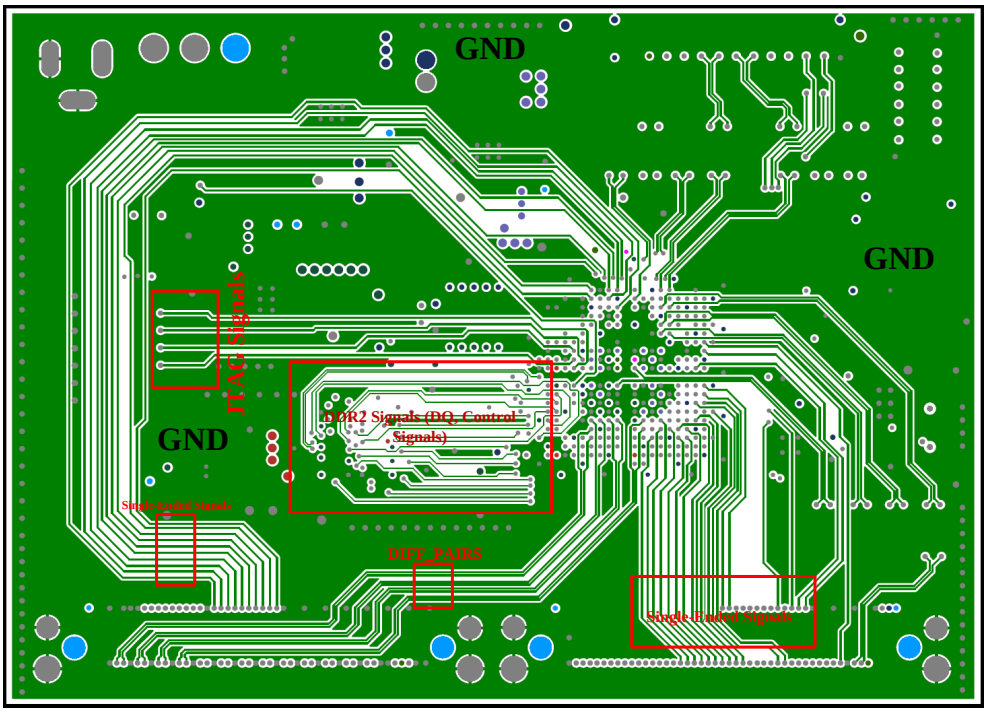


(a) Top layer (Mixed Signals)

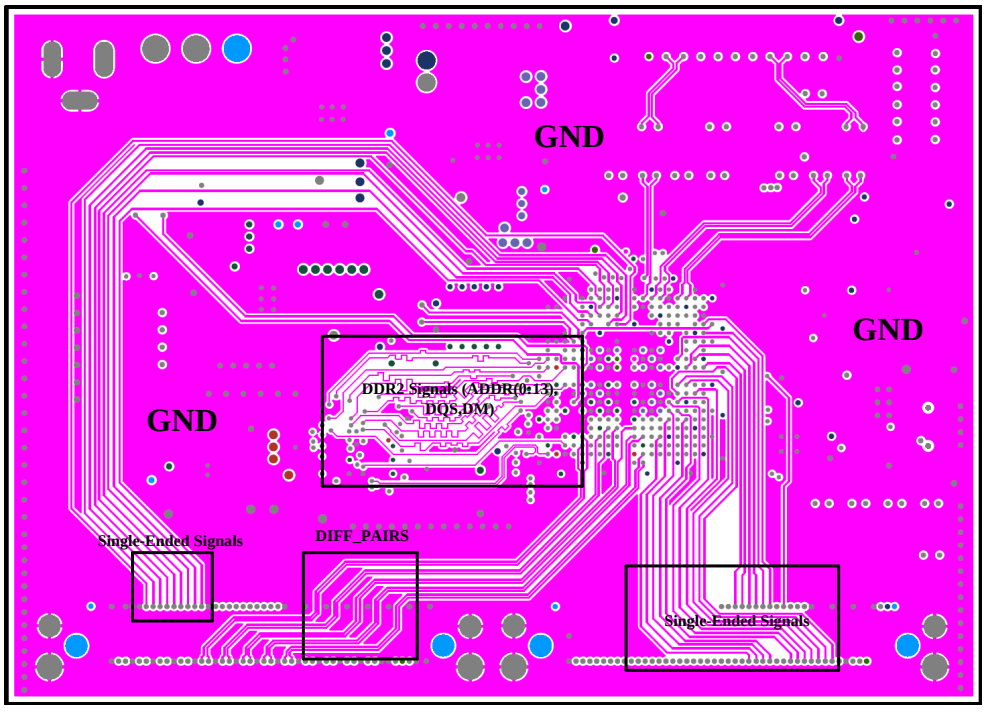


(b) Outer layer L2 (GND System)

Figure C.2: PCB layout of the FPGA design

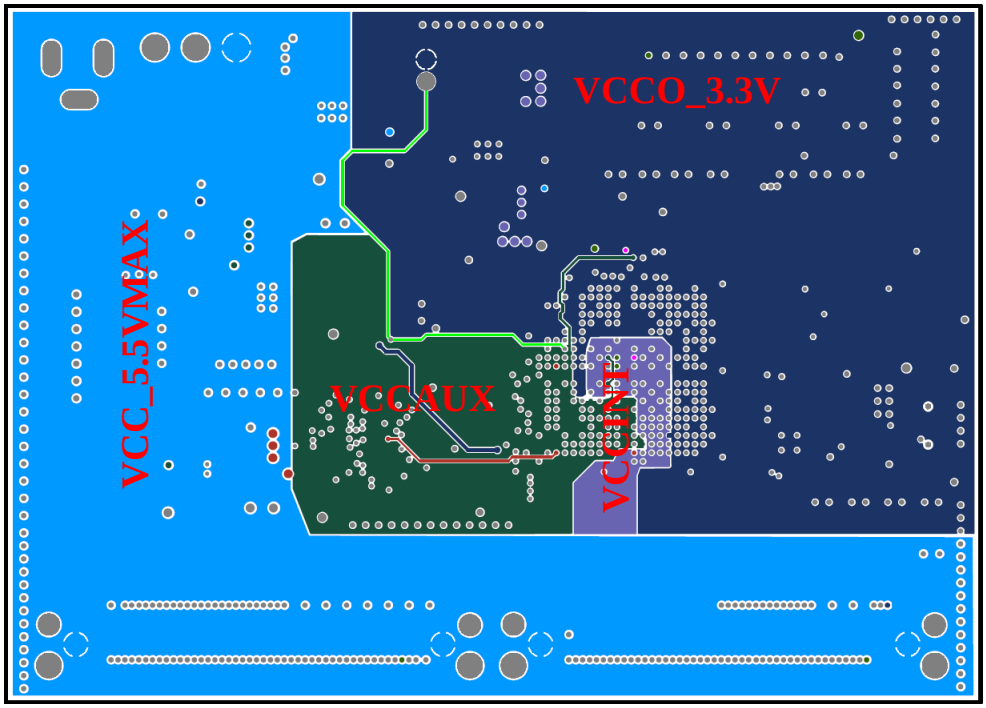


(c) Inner layer L3 (Digital Signals)

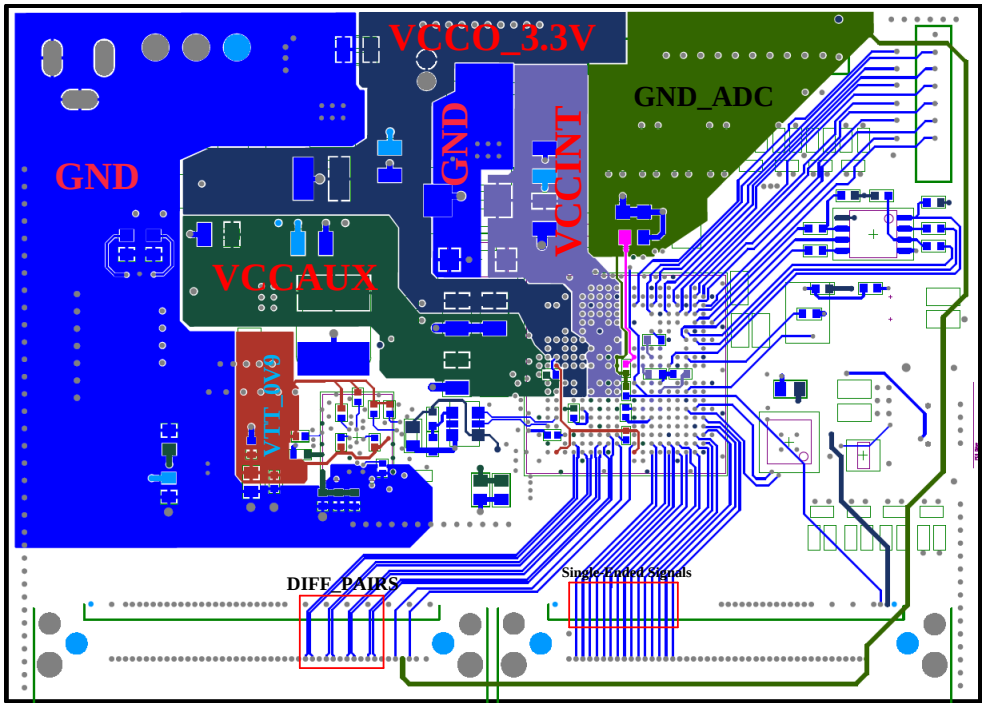


(d) Inner layer L4 (Digital Signals)

Figure C.2: PCB layout of the FPGA design (cont.)

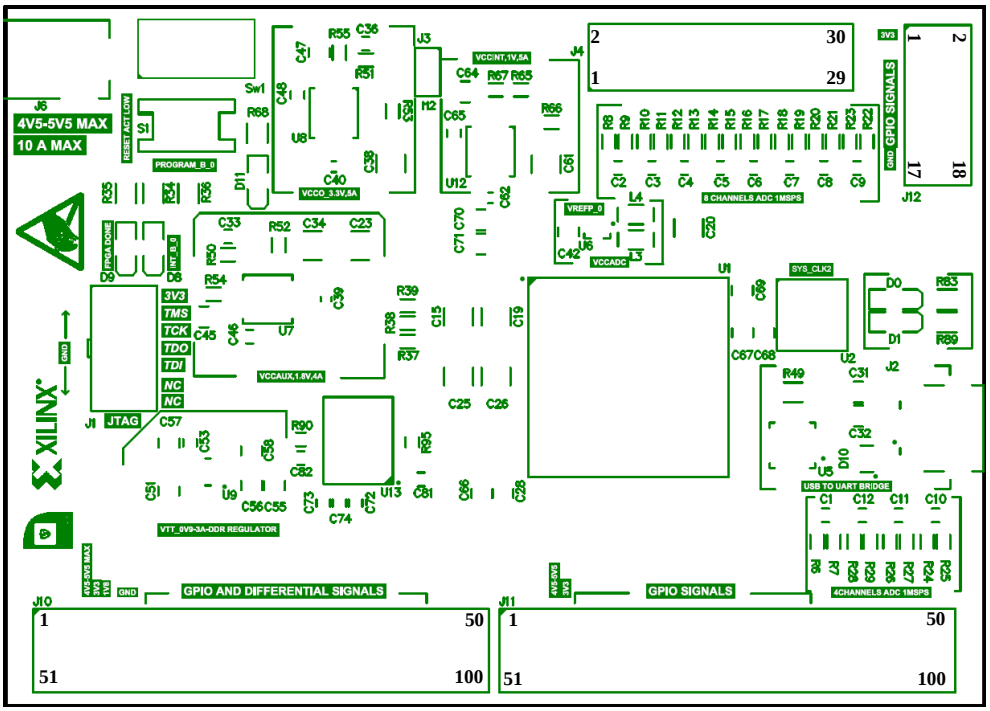


(e) The outer layer L5 for power distribution system

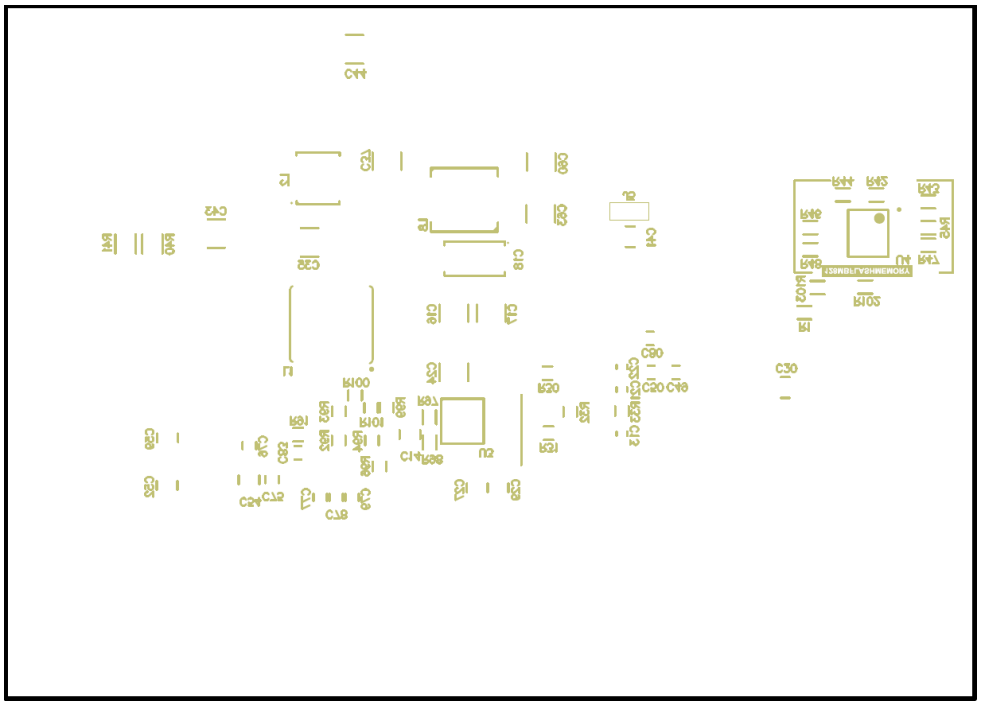


(f) Bottom Layer (Mixed Signals)

Figure C.2: PCB layout of the FPGA design (cont.)



(g) Top overlay



(h) Bottom overlay

Figure C.2: PCB Layout of the FPGA design (cont.)

Appendix D

Verilog Codes VTL and VTF

D.1 Verilog Top Level (VTL)

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////
3   // Company: VUTBR Czech Republic
4   // Engineer: Ziad Nouman
5   // Design Name:  SCS_Generator
6   // Module Name: Top_Level_SCS_signals_with_PWMController
7   // Project Name:
8   //////////////////////////////////////////////////////
9   module Top_Level_SCS_signals_with_PWMController(
10      input CLK_IN,
11      input PBRREST,
12      input SW_EN,
13      input [1:0] SWCOTROL,
14      output SCS_Q71,
15      output SCS_Q72,
16      output SCS_Q73,
17      output SCS_Q81,
18      output SCS_Q82,
19      output SCS_Q83
20      );
21  //------------- Registers and wires
22  wire PWMSIG;
23  wire [13 : 0] DataBCont;
24  wire [13 : 0] DataAin;
25  parameter  puls_time = 15'd32766;
26  parameter  delay = 17'd100000;
```

```
27  //-------- Clock Wizard ----------------------------
28    CLK_Wizard Clk_Gen
29     (
30      .CLK_IN(CLK_IN),
31      .CLK_OUT1(CLK_OUT1),     // OUT 100 MHz
32      .CLK_OUT2(CLK_OUT2),     // OUT 5 MHz
33      .RESET(PBRREST));
34  //-------------------------------------------------
35  // This top file contains the Control Signals
36  // and Debouncer digital Circuit
37  //-------------------------------------------------
38  Top_Level Top1 (
39      .CLK(CLK_OUT1),
40      .SW1(PBRREST),
41      .SW2(SW_EN),
42      .PWM(PWMSIG),
43      .SCS_Q71(SCS_Q71),
44      .SCS_Q72(SCS_Q72),
45      .SCS_Q73(SCS_Q73),
46      .SCS_Q81(SCS_Q81),
47      .SCS_Q82(SCS_Q82),
48      .SCS_Q83(SCS_Q83)
49      );
50  //---------------- PWM Generator-----------------
51  //---------------- UPDown Counter----------------
52  UpDown  #(.puls_time(puls_time))
53  UPD_Count (
54      .clk(CLK_OUT2),
55      .reset(PBRREST),
56      .enable(SW_EN),
57      .count(DataBCont)
58      );
59  //---------------- Comparator -------------------
60  Comparator comparator_data (
61      .CLK(CLK_OUT2),
62      .RST(PBRREST),
63      .Enable(SW_EN),
64      .Data_A(DataAin),
65      .Data_B(DataBCont),
66      .Data_out(PWMSIG)
67      );
68  //--------------- control data -----------------
69  control_data control_data (
70      .CLK(CLK_OUT2),
```

```
71        .CE(clk),
72        .RST(PBRREST),
73        .Enable(SW_EN),
74        .bt(SWCOTROL),
75        .controlled_data(DataAin)
76        );
77    //------------- 50 Hz divider------------------
78    CLK_divider #(.delay(delay))
79    clkdive (
80        .reset(PBRREST),
81        .refclk(CLK_OUT2),
82        .clk(clk)
83        );
84    endmodule
```

D.2 VTF Code for Simulation Results

```
1   `timescale 1ns / 1ps
2   ////////////////////////////////////////////////////////////////
3   // Company:  VUTBR
4   // Engineer: Ziad Nouman
5   // Design Name:   Top_Level
6   // Project Name:  Top_Level_SCS_Generator
7   // Verilog Test Fixture created by ISE for module: Top_Level
8   ////////////////////////////////////////////////////////////////
9   module Top_Level_SCS_GeneratorVTF;
10
11      // Inputs
12      reg CLK_IN;
13      reg SW1;
14      reg SW2;
15      reg PWM;
16
17      // Outputs
18      wire SCS_Q71;
19      wire SCS_Q72;
20      wire SCS_Q73;
21      wire SCS_Q81;
22      wire SCS_Q82;
23      wire SCS_Q83;
```

```
24
25      // Instantiate the Unit Under Test (UUT)
26      Top_Level uut (
27         .CLK_IN(CLK_IN),
28         .SW1(SW1),
29         .SW2(SW2),
30         .PWM(PWM),
31         .SCS_Q71(SCS_Q71),
32         .SCS_Q72(SCS_Q72),
33         .SCS_Q73(SCS_Q73),
34         .SCS_Q81(SCS_Q81),
35         .SCS_Q82(SCS_Q82),
36         .SCS_Q83(SCS_Q83)
37      );
38
39      initial begin
40         // Initialize Inputs
41         CLK_IN = 0;
42         SW1 = 0; // RESET
43         SW2 = 0; // ENABLE
44         PWM = 0; // PWM
45   // PWM: Assuming that this signal is generated by
46   //----------------------------
47         #100;
48         SW2 = 1;
49         PWM = 0;
50         SW1 = 1;
51         #100;
52   //----------------------------
53         SW2 = 1;
54         PWM = 0;
55         SW1 = 1;
56         #100;   // 10clock cycles
57   //----------------------------
58   // switching frequency = 5khz
59   //----PWM-- first puls -------
60         SW2 = 1;
61         PWM = 1;
62         SW1 = 0;
63         #50000;   //50us=5000 clock cycles
64   //----------------------------
65         SW2 = 1;
66         PWM = 0;
67         SW1 = 0;
68         #150000; //150us=15000 clock cycles
69   //----------------------------
```

```
70   //----PWM-- Second puls -------
71         SW2 = 1;
72         PWM = 1;
73         SW1 = 0;
74         #100000; //100us=10000 clock cycles
75   //-----------------------------
76         SW2 = 1;
77         PWM = 0;
78         SW1 = 0;
79         #100000; //100us=10000 clock cycles
80   //-----------------------------
81   //----PWM-- third puls --------
82         SW2 = 1;
83         PWM = 0;
84         SW1 = 0;
85         #15000; //15us=1500 clock cycles
86   //-----------------------------
87         SW2 = 1;
88         PWM = 1;
89         SW1 = 0;
90         #25000; //25us=2500 clock cycles
91   //-----------------------------
92         SW2 = 1;
93         PWM = 0;
94         SW1 = 0;
95         #160000; //160us=16000 clock cycles
96         $finish;
97      end
98   //-----------------------------
99         always begin
100        #3.333 CLK_IN = !CLK_IN;
101        end
102  //-----------------------------
103  endmodule
```

D.3 User Constraint File of the Verilog Top Level

```
1   NET "SWCOTROL[1]" IOSTANDARD = LVCMOS33;
2   NET "SWCOTROL[0]" IOSTANDARD = LVCMOS33;
3   NET "SWCOTROL[1]" LOC = D12;
4   NET "SWCOTROL[0]" LOC = E14;
5   NET "CLK_IN" LOC = N18;
6   NET "CLK_IN" IOSTANDARD = LVCMOS33;
7   NET "PBRREST" LOC = D14;
8   NET "SW_EN" LOC = E16;
9   NET "SW_EN" IOSTANDARD = LVCMOS33;
10  NET "PBRREST" IOSTANDARD = LVCMOS33;
11  NET "SCS_Q71" LOC = B21;
12  NET "SCS_Q72" LOC = B22;
13  NET "SCS_Q71" IOSTANDARD = LVCMOS33;
14  NET "SCS_Q72" IOSTANDARD = LVCMOS33;
15  NET "SCS_Q73" LOC = E19;
16  NET "SCS_Q73" IOSTANDARD = LVCMOS33;
17  NET "SCS_Q81" LOC = E18;
18  NET "SCS_Q81" IOSTANDARD = LVCMOS33;
19  NET "SCS_Q82" LOC = C19;
20  NET "SCS_Q83" LOC = D19;
21  NET "SCS_Q82" IOSTANDARD = LVCMOS33;
22  # PlanAhead Generated IO constraints
23  NET "SCS_Q83" IOSTANDARD = LVCMOS33;
```

Curriculum Vitae

Ing. Ziad Nouman
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Nationality: Syrian
Place of birth: Eskebleh

ACADEMIC EDUCATION

Since 2010	**Brno University of Technology – Czech Republic** Ph.D. student
2004 – 2005	**Tishreen University - Lattakia** Higher Study Diploma in Electrical Engineering The field of (electrical power systems)
2000 – 2004	**Tishreen University - Lattakia** Degree of Electrical Engineer. Section of Power Engineering.
1998 - 2000	**Industrial Institute of Electricity and Mechanics – Damascus**.

LANGUAGES

Arabic	Maternal language
English	Good
Czech	Good

SPECIAL KNOWLEDGE

Operating Systems	Windows 98, Windows me, Windows 2000, Windows XP Professional, Windows 7.
Office	Microsoft Office System
Languages of Programming	C, HDL (Verilog, VHDL), Matlab.
Software of Design	Altium Designer, Cadence, Microcontroller Design, FPGA Design.

PLACES OF INTEREST

Reading, Sport, learning languages, Tourism