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ÚSTAV RADIOELEKTRONIKY

MODULAR SYSTEM FOR ELECTRICAL IMPEDANCE TOMOGRAPHY

MODULÁRNÍ SYSTÉM ELEKTRICKÉ IMPEDANČNÍ TOMOGRAFIE

BACHELOR'S THESIS BAKALÁŘSKÁ PRÁCE

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Modulární systém elektrické impedanční tomografie

POKYNY PRO VYPRACOVÁNÍ:

Realizujte obvodové zapojení navržené v semestrální práci, které je tvořeno ze sady alespoň 4 aktivních sond realizujících předzpracování měřeného harmonického napětí v rozsahu jednotek mV až desítek V a kmitočtem cca do 100 kHz a případně z multiplexoru zajišťujícího digitální přepínání elektrod pro měření, resp. proudové buzení. Odlaďte elektrické zapojení a firmware mikroprocesoru vyhodnocujícího měřené napětí, proud, kmitočet a fázi a zajišťujícího komunikaci s připojeným PC. Vyhodnoťte skutečné rozsahy navržených obvodů pro měření napětí a proudu, jejich šířku kmitočtového pásma, fázový posun, přesnost, rychlost měření. Správnost návrhu realizovaných obvodů ověřte v laboratorních podmínkách.

DOPORUČENÁ LITERATURA:

[1] HOROWITZ, Paul a Winfield HILL. The art of electronics. Third edition. New York: Cambridge University Press, 2015. ISBN 978-0-521-80926-9.

[2] HOLDER, D. S. Electrical Impedance Tomography: Methods, History and Applications. B.m.: CRC Press, 2004. ISBN 978-1-4200-3446-2.

[3] ADLER, Andy a LIONHEART, William R. B. Uses and abuses of EIDORS: An extensible software base for EIT Physiol. Meas., 27:S25-S42, 2006

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ABSTRACT

This thesis presents a novel approach to an electrical impedance tomograph's system architecture design. It delves into the strategic decisions that shaped the hardware layer of a measurement system comprising multiple units and enabling intercommunication between them. The primary objective was to develop a cost-effective method for switching a current source among numerous electrodes and measuring voltage across each with a wide dynamic range while maintaining a minimal phase shift between the channel and input of an analog-to-digital converter. The measurement system is designed and documented, serving as a valuable reference for developing new additional units. The thesis describes the hardware and firmware of active electrodes as the key part of the tomograph and provides measurements verifying the correctness of the approach.

KEYWORDS

Electrical impedance tomography, active electrode, modular system, data acquisition system

ABSTRAKT

Tato práce představuje nový přístup k návrhu architektury systému elektrického impedančního tomografu. Zabývá se strategickými rozhodnutími, která formovala hardwarovou vrstvu měřicího systému sestávajícího z několika jednotek a umožňujícího vzájemnou komunikaci mezi nimi. Hlavním cílem bylo vyvinout levný hardware pro přepínání zdroje proudu mezi mnoha elektrodami a měření napětí na každé z nich s širokým dynamickým rozsahem při zachování minimálního fázového posunu mezi kanálem a vstupem analogově-digitálního převodníku. Měřicí systém je navržen a zdokumentován a slouží jako cenná reference pro vývoj nových dalších jednotek. Práce popisuje hardware a firmware aktivních elektrod, klíčové části tomografu a uvádí měření ověřující správnost tohoto přístupu.

KLÍČOVÁ SLOVA

Elektrická impedanční tomografie, aktivní elektroda, modulání systém, systém sběru dat

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ROZŠÍŘENÝ ABSTRAKT

Tato práce se zabývá systémovým návrhem modulárního systému pro elektrickou impedační tomografii, popisuje obecné úvahy a postupy při návrhu takého systému. Principem elektrické impedanční tomografie je měření napětí mezi elektrodami obklopující materiál, který je přes tyto elektrody i proudově buzen. Rekonstrukce konečného výsledku představujícího rozložení měrné impedance respektive admitance se provádí ze souboru naměřených napětí, proudů a fázových rozdílů mezi nimi. Tato metoda je ve více případech prací popisována pro využití v lékařství, zejména pro monitorování funkce plic. Existuje však značný potenciál pro rozšíření jejího použití i do dalších oblastí. Hlavním cílem tohoto projektu bylo vyvinout modulární systém měření, který by byl schopen pokrýt široký rozsah měřitelných impedancí.

Navržený systém je založen na modulárním přístupu, kdy je každý funkční blok realizován jako samostatná jednotka v podobě desky plošného spoje následně stohované do systému. Tyto jednotky jsou propojeny definovaným komunikačním rozhraním. Klíčovými částmi systému je napájecí modul zajištující stabilní napájení pro všechny ostatní moduly, hlavní řídící jednotka obsahující STM32 mikrokontrolér koordinující činnost celého systému a zajištující zpracování naměřených dat a odesílání dat uživateli, multiplexorový modul umožňuje přepínání proudu mezi jednotlivými elektrodami. Zdroj konstantního proudu budí materiál, aktivní elektrody obsahují zesilovače s programovatelným ziskem, které zajišťují vysoký rozsah měřitelných hodnot napětí. Systém je navržen tak, aby umožňoval snadnou adaptaci na různé měřené materiály. Použitím aktivních elektrod bylo vyřešeno zvýšení odstupu signálu od šumu, který je typický pro systémy s pasivními elektrodami a delšími vzdálenostmi mezi elektrodou a měřícím systémem.

Práce obsahuje blokový návrh systému, popisuje úvahy, které vedly k rozhodnutím týkajícím se obecného návrhu systému a jeho vnitřní sběrnice umožňující připojení modulů, dále schéma aktivní elektrody, firmware a software umožňující měření napětí na elektrodě. Během vývoje systému byly provedeny simulace a měření k ověření správnosti navrženého hardwaru. Naměřené hodnoty ukázaly, že systém je schopen spolehlivě měřit maximální napětí od 103 mV do 5.176 V pro DC až 100 kHz a od 26 mV do 48 V v rozsahu DC až 40 kHz, aniž by došlo k saturaci měřicích obvodů. Systém také vykazoval minimální fázový posun mezi kanály a vstupy analogově-digitálního převodníku, což je klíčové pro přesnost měření. Navržené schéma modulárního systém pro elektrickou impedanční tomografii a realizace aktivních elektrod představuje významný krok vpřed ke kompletnímu návrhu systému, který by díky své modularitě mohl být použit nejen v lékařství, ale i v dalších oblastech, jako je například geofyzika, materiálové inženýrství nebo k rozvoji metody elektrické impedanční tomografie jako takové.

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Author's Declaration

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I declare that I have written this paper independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the paper and listed in the comprehensive bibliography at the end of the paper.

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Content

In	trod	uction	11
1	The	oretical framework	12
	1.1	EIT Instrumentation	12
	1.2	Voltage measurement	13
	1.3	Current source	15
2	Ain	ns of the thesis	18
	2.1	Learning from mistakes	18
	2.2	System objectives	19
3	$\mathbf{Sys}^{\mathbf{r}}$	tem design	21
	3.1	Power supply module	23
	3.2	Main controller	23
	3.3	Multiplexer module	26
	3.4	Active electrodes	27
	3.5	Interconnection	36
4	Firi	nware	39
	4.1	Probe library	39
5	Eva	luation by measurement	42
Co	onclu	ision	46
Bi	bliog	graphy	47
Sy	mbo	ols and abbreviations	50
\mathbf{A}	List	ing of digital appendix	51

List of Figures

1.1	Frequency-dependent grounding impedances example	12
1.2	Resistivity distribution example	13
1.3	Single ended and differential voltage measurement	14
1.4	Voltage controlled current source topologies	16
3.1	System block diagram	22
3.2	DC offset adder schematic $\ldots \ldots \ldots$	24
3.3	Frequency characteristics of the DC offset adder $\ldots \ldots \ldots \ldots$	25
3.4	Schematic diagram of the active electrode/probe	28
3.5	Simulated probes power supply circuitry	35
3.6	Simulation of the probe connection to the system $\ldots \ldots \ldots \ldots$	35
3.7	Physical form of the active probe	36
3.8	Example of interface and galvanic isolation	37
3.9	System interface diagram	38
5.1	Frequency characteristics of probes settable amplifications $\ldots \ldots$	42
5.2	Phase shift characteristics of probes settable amplifications $\ldots \ldots$	43
5.3	Measurement of 7.071 V RMS for gain index = $0 \dots \dots \dots \dots \dots$	43
5.4	Measurement of 1.131 V RMS for gain index = 14	44
5.5	Measurement of 8.761 mV RMS for gain index = $42 \dots \dots \dots \dots$	44

List of Tables

2.1	Target parametrs of the system	20
3.1	Analog multiplexer parameters comparison	27
3.2	Voltage ranges of the active probe	31
3.4	Predicted current consumption of the active probe	34

Introduction

electrical impedance tomography (EIT) is a method of imaging the distribution of a material's specific conductivity (or impedivity). These images are constructed from voltage between electrodes that make direct contact with the material. The voltage is formed by injecting an alternating current into the material by the tomograph. The method is actively used in the medical field, utilizing lung function monitoring. There is a big potential for extending its applications to other fields. Assuming the material is not biological, the issue of securing non-invasive measurement is replaced by an option of supplying higher currents to electrodes, thus enabling the measurement of materials with a wider range of impedance.

The primary goal of this project is to develop an easily adaptable measurement system capable of handling a broad range of measurable impedances. To achieve this, a large dynamic range of voltage and current readings is required. The main approach to make the system modular was to create a block design of multiple units as individual printed circuit boards (PCB) and define interconnection between them. This involved studying all components of the EIT instrumentation, designing necessary units each meeting certain requirements to ensure the compatibility of possible extensions and adapting the communication bus for module connectivity. The entire measurement chain must essentially consist of signal synthesis, a voltage-controlled current source, current multiplexing, voltage measurement, voltage multiplexing, and a primary data acquisition unit that calculates voltage, current values, and phase differences. A high dynamic range is obtained by active probes containing amplifiers with programmable gain.

The following chapters will cover potential measured materials, methods of voltage measurement in EIT, circuits for current excitation into the material, a discussion of potential errors in system design and their solutions and detailed description of the system design process. This includes the hardware design of the multiplexer unit and active probe, firmware development using STM HAL, and software development for simple measurements in Matlab. This works was also presented in Student EEICT proceeding [1]. For enhance grammatical accuracy in writing of this theses ChatGPT 2024, an AI language model by OpenAI was utilized [2].

1 Theoretical framework

1.1 **EIT** Instrumentation

Getting away with the complex idea behind EIT, it gets quite simple, theoretical hardware design utilizes a controlled constant current source, load impedance, and measurement electrodes. The way we can terminate the parameters of each part is to assume a current range that is enabled by the constant current source. In practice, commonly used devices are around 0.1–5mA of used current range [3]. We increased these values to achieve a greater voltage drop at the farthest electrodes. With frequencies approximately 100 kHz maximum, as stated in the thesis assignment.



Fig. 1.1: "Frequency-dependent grounding impedances as a parameter of the length of counterpoise in the two-layered soils" redrawn from [4].

The aim was to measure a wide range of materials, given that soil would probably have the greatest range of impedances. Thus, the calculation below is done for the soil measurement case. The reactance of the ground can't be defined precisely. It is a function of electrode dimensions, the length between electrodes, and soil moisture level. However, the extent of the changes in reaction is not that great. For example, in Figure 1.1, in measurement with 10 m long counterpole electrode, it was determined that the soil has a capacitive character as impedance decreased by 10Ω and above from DC to 300 kHz, with frequencies above 300 kHz, frequency characteristic flipped to the inductive character as increased by 10Ω at 1 MHz [4].

We also need to take into account the resistivity of the soil. We also cannot tell what type of material or resistivity we will measure. In this case, we are also using measurements as a base. An electrical resistivity tomography method was performed on an earth dam. We can see layers of sediment differentiated by their impedance, ranging from units of ohms to thousands of ohms; see Figure 1.2.



Fig. 1.2: "Interpretation of the geoelectrical section of the ERT-P1 prole carried out in downstream of Abu Baara dam" redrawn from [4].

These numbers imply that if we want to measure material with greater impedances, we need to use active electrodes as amplifiers for small voltage between two adjacent electrodes or increase current through load impedance, thus increasing the supply voltage of all the components through which it flows to avoid saturation. Both options were applied in the design (more detail in Sections 3.4 and 3.1).

1.2 Voltage measurement

There are two types of voltage measurement: single-ended and differential, as shown in Figure 1.3. The single-ended measures voltage with respect to ground potential, and the differential measures the difference between two voltages utilizing preferably an instrumentation amplifier as a converter to single-ended output in the case of using ADC with single-ended input. Differential measurement is typically used in passive EIT system, where the measured voltage between adjacent electrodes is smaller than in the case of single-ended type. This allows reduction of the ADC dynamic range requirements [3].

The advantage of differential measurement is suppression of noise detected at both inputs of the instrumental amplifier; the problem with using the differential measurement in this application is that we cannot suspect that the gain of two

Fig. 1.3: Two types of voltage measurement using active electrodes: differential (a) and single-ended (b).

measuring active electrodes will be the same, in case of different gain settings on each active electrode there will be uncertainty inserted into the system because an instrumental amplifier located on the central system could cause phase inversion. However, an even more significant problem would be the potential phase delay introduced by one of the amplifiers in the active probe. This difference in phases at the input of the instrumental amplifier would cause frequency-dependant commonmode error at the output of the amplifier; these imbalances between electrodes were considered the principal sources of error in the differential voltage reading [5].

The single-ended type of voltage measurement lacks the advantages of common mode voltage rejection and typically low offset error of the differential voltage measurement. However, the significant advantage of this method is that we do not have to deal with the need for phase error correction. Furthermore, since we only need to set one gain, we can avoid the potential problem of phase inversion caused by the instrumental amplifier.

In order to meet the *electrical impedance tomography* (EIT) method requirements of measuring the voltage drop across material without creating a low impedance path to the ground of the current supply affecting the measurement, the negative input of the *operational amplifier* (Op Amp) in the single-ended configuration needs to be connected to the second ground galvanically isolated from the ground/negative pole of the current supply. With galvanic isolation done in the power supply section, we can use a simple high-voltage Op Amp (not isolated one) in the active electrodes to address both the high input impedance needed when using any attenuator and the high *signal-to-noise ratio* (SNR) addressed in section 2.2.

Having two *analog-to-digital convertor* (ADC)s available is essential; we can use dual regular simultaneous mode and sample two channels at the same time [6]. One channel is for current measurement, and one is for voltage measurement. The 12-bit ADC in the *microcontroller* (MCU) converts these values and stores them in a preallocated buffer utilizing the *direct memory access* (DMA) channel [7]. With a

use of the internal ADC of the MCU we get 24 Samples per period, when samling the highest acceptable frequency 100 kHz, which should be enough, but there is always option to add an aditions ADC unit to the system. Essentially, a calculation of the impedance \vec{Z} from determined magnitudes and phase shifts of voltage (U, ϕ_U) and current (I, ϕ_I) flowing through the measured phantom (1.1) [8].

$$\vec{Z} = \frac{U}{I} e^j (\phi_U - \phi_I). \tag{1.1}$$

1.3 Current source

This section will look at the most common current sources or voltage-to-current converters used in EIT applications. The current source must be able to drive a wide range of impedances with a constant current. Its frequency response should be flat in the range of used frequencies. This requirement places great demands on the output impedance parameter and the parasitic capacitance of the output, respectively. Figure 1.4 (a) shows a floating current source with transformer coupling, which galvanic isolates the current injection side. For this type, there is no need for another galvanic isolation on the power supply side.

Fig. 1.4: Typical voltage controlled current sources used in EIT systems: A floating current source with transformer coupling (a), Howland current source (b), Three-operational-amplifier current source (c), Operational transconductance amplifier current source (d).

Shunt resistor $R_{\rm S}$ used for measuring current magnitude to compensate the nonconstant conversion ratio of the circuitry caused by non ideal parameters of the transformer and Op Amp, the input voltage is iterated while measuring the output current to achieve the desired current value through the load impedance $Z_{\rm L}$. Figure 1.4 (c) shows a Three-operational-amplifier current source, which consists of a summing amplifier with control voltage and voltage amplifier in feedback as inputs, if trimmed, the current through $R_{\rm S}$ and $R_{\rm L}$ is proportional to 1.2 [3]:

$$I_{\rm L} = -V_{\rm in} \cdot R_{\rm S},\tag{1.2}$$

where $I_{\rm L}$ is the current through load resistor, $V_{\rm in}$ is the controlled input voltage and $R_{\rm S}$ being the shunt resistors value. Figure 1.4 (d) shows the operational transconductance amplifier current source as the simple bi-direction voltage-to-current converter. It utilizes a buffer with a gain of one driving resistor with a known value and a current mirror on each power supply rail, driving the load resistance with the

same current. Most used circuit in EIT field is a Howland current source shown in Figure 1.4 (b) and its variants. If resistor values are properly chosen as shown in equation 1.3, the output current will be a function of input voltage and resistor R_2 , see 1.4 [3, 8]:

$$\frac{R_4}{R_3} = \frac{R_2}{R_1},\tag{1.3}$$

$$I_{\rm L} = -\frac{V_{\rm in}}{R_3},\tag{1.4}$$

where R_1 and R_2 are resistor values in inverting amplifier topology, R_1 , R_2 are the resistor values in positive feedback, $R_{\rm L}$ is the load resistor value, $I_{\rm L}$ is the current through load and $V_{\rm in}$ being the controlled input voltage. This method requires the resistor ratios to be matched exactly, and then the output impedance of the current source for an ideal Op Amp is infinite. With trimming involved, we can achieve that. However, still, there is a limiting factor of low loop gain effect at high frequencies, which drops the output impedance from the ideal infinity to the Op Amps open-loop output impedance, typically a few hundred ohms [8]. The importance of trimmed resistor ratios is great; for example, if we use $10 \text{ k}\Omega$ resistors with a 1% tolerance, the worst case output impedance can reach down to $250 \,\mathrm{k\Omega}$ (it might be plus or minus $250 \,\mathrm{k\Omega}$). In practice, an "Improved" Howland circuit is used, solving a problem of poorly adjustable gain caused by the need for resistors ratio match and normally being $-1/R_3$. In the "improved" type, another resistor is added in series with R_4 and the output node with $R_{\rm L}$ is shifted in between the new resistor and R_4 . Now, the gain is set by the new resistor, which can now be low and others high. There is still a need for resistor raion matched, but now it will be $(R_4 + R_{\text{new}})/R_3 = R_2/R_1$. Trimer can be added in series with R_3 to adjust the ratio after assembly [9].

2 Aims of the thesis

The aim is to design EIT measurement system with a wide range of potential uses. Rather than focusing on a specific field or application, the device should have a high dynamic range to achieve multipurpose use for future study of next EIT applications. It should be capable of directing current from a constant current source to all electrodes. All that controller by itself using microcontroller (MCU) and with cost reduction of the whole system in mind. See the objectives listed below:

- Design active electrode with adjustable voltage gain.
- Discuss decisions done when designing the connection from the multiplexer to the probe.
- Design multiplexer unit without relying on mechanical relays.
- Specify physical connection between units.
- Define unit rules to achieve compatibility with the system.
- Conduct measurements evaluating the probe design.

2.1 Learning from mistakes

There are bachelor's theses that deal with a similar topic [10]; finding bugs in them and learning from them was necessary before designing the system. The problem with most works focusing on some part of the electrical design of EIT measurement system previously published at Brno University of Technology Faculty of Electrical Engineering and Communication (BUT, FEEC) were limited by global chip shortage. So, the selection of components was affected by the availability in warehouses. My thesis solves this potential problem by distributing the entire system from single PCB into several individual units or PCBs, each focusing on a specific part of the whole measurement chain. With this approach, one can change parameters like dynamic range, maximal values, or a section's circuit design that depends on chosen parts. Without recreating the whole system, thus ordering all components again, we can recreate and manufacture the one specific section that needs upgrading. Concentration on solving EIT problem can be performed, not worrying about other parts. To make these advantages work, system rules, described in Section 3, were created to ensure compatibility across all units.

Solutions trying to make wider use of EIT methodology are limited by a noiseinduced alongside the measurement loop as described in [11], where the problem is suppressed by introducing a band pass or low pass filter with an amplifier. The approach is not so usable for this type of voltage sensing with very high input impedance of active amplifier and low measured impedance, causing a significant impedance mismatch. Long cables connecting the electrode and a voltmeter contribute further to noise coupling, according to [12]. When measuring a highimpedance source, the stay capacitance of long cables starts to be a problem, lowering the cutoff frequency. This is not a concern in biomedical applications because lower frequencies are more optional for imaging blood volume changes [13]. In my system, active electrodes are used to extend the device's potential usage, increasing signal-to-noise ratio (SNR) at the output of the electrode, preventing the problems described above.

There is a requirement to measure voltages also on electrodes injecting current. This capability is for example available on systems like the ACE1 [14] or Zimnioks system [10], where a selection of electrode modes (injection and measurement described in Section 3.3) is done directly at the active electrode. Components used in active electrodes are increasing the price of the whole system with a multiplexer of the number of active electrodes. This has proven to be quite a significant increase in previous designs. I moved the control of the electrode mode to the Multiplexer unit. My system uses analog switches as ACE1 [14] uses rather than an array of relays for switching as Zimniok [10] did. The decision was declared at the very beginning of the project: Relays are expensive, and they tend to decrease the unit's longevity.

When designing a measurement chain and active probe, there must be a focus not to introduce low impedance paths to the ground as Zimniok [10] did in his active electrode front-end. Resistors directly connected to ground or RC low-pass filter with a cut-off frequency of approximately 20 Hz. We should avoid any capacitive coupling to ground, diverting current from a phantom, thus affecting the measurement. Especially in the case of single-ended measurement (more details on Section 1.2), there must be galvanic isolation between the grounds of the currently measuring electrode and the constant current source.

2.2 System objectives

In order to expand the field of use to the materials with higher impedance or measurements taken over greater distances with materials of relatively low specific impedivity, it is necessary to increase the current injected into the material. This will allow electrodes placed further from the injecting electrodes to detect a voltage drop greater than any noise present. To further enhance the SNR and low voltage measurement capabilities, we chose to use the active electrodes that will also compensate for the unwanted noise potentially coupled to the cables carried from the central system to the contact with the material.

With increasing current and the total impedance of the material, we will need to provide greater voltages for the constant-current source, *multiplexer* (MUX), and other active devices to avoid saturation. A study of the current electronics market was carried out to determine the maximal voltage we can achieve without using mechanical devices, as was required in the project assignment. The most sensitive part of the measurement chain will be the analog MUXs, which will handle the switching of current source output to the electrodes it must withstand both the current passed through the material and the voltage. It determinates the maximum current injected into the material by the device is also determined by the current capability of the MUX and constant-current source circuitry. The TMUX8108 chip with a switchable voltage of 100 V peak-to-peak maximal was chosen for its easy-to-solder package. It meets the requirements for wide frequency band with cut-off frequenci of 100 kHz and relatively low price compared to other solutions.

Another main component will be a programmable-gain amplifier (PGA) mounted on the active probe, enabling the amplitude and phase measurement of voltage between specific electrodes. The selected chip will determine the cut-off frequency of the device. Its configurable gains will set the minimum and maximum amplitudes potentially measurable by the active probe. It was chosen to use PGA280 with a TMUX8108 as a voltage divider (attenuator) in series. This configuration enables the extension of maximal measurable voltage because the PGA280 on its own is not capable of attenuating voltages above $13.2\,\mathrm{V}$ as its maximal attenuation the system will use is $0.25 \,\mathrm{V/V}$ for reaching desired 3.3 V maximum on ADC input, it would be exactly 13.2 V maximum that could be measured. With the use of TMUX8108 multiplexor as an additional attenuator with selectable attenuation, we increase the maximal measurable voltage to match the maximal voltage of 48V switchable by TMUX8108. In case of minimal voltage range selectable by the active probe we are limited by a maximal voltage gain of the PGA280 which is 128 V/V. That will set the minimum voltage range to approximately 25.8 mV. Further explanation of computed values and selectable gains can be found in Section 3.4. These properties of the components determine the system's initial properties; thus, we can determine the tomograph's potential maximum ranges as listed in Table 2.1. These ranges do not determine the system's capacities; they serve as a reference for comparison of differences between actual and predicted values.

Maximal voltage range	$\pm 48 \mathrm{V}$
Minimal voltage range	$\pm 28.8\mathrm{mV}$
Frequency range	m DC-100kHz

Table 2.1: Target parameters of the system

3 System design

This chapter clarifies the hardware design decisions. Specifically, decisions concerning the system architecture, the interconnection between measurement sections, the multiplexing signal, and the active electrode design.

The system was split into individual units, each focusing on a specific task together completing the measurement chain. This makes minor redesigns and contributions to projects much easier and more cost-efficient than redesigning or improving the system from scratch, as described in Chapter 2.1. The whole system was divided into modules listed below:

- Power supply module (see Section 3.1)
- Main controller module (see Section 3.2)
- Signal generator module
- Constant current supply module
- Multiplexer module (see Section 3.3)
- Active electrodes (see Section 3.4)

A block diagram was created to facilitate an overview of the entire system and its functioning between systems, see Figure 3.1. Individual modules have names in their boxes. They all have the same connector (more detail in Section 3.5) and the interfaces or power supplies used by the module are bolded. A connection between blocks within the module and available ways of communication between them are indicated by arrows, also showing the direction of communication. Some pins are not used by any of the modules. These are for future use and possible expansion with new modules.

Fig. 3.1: System block diagram.

3.1 Power supply module

To be able to measure with the single-ended method (described in Section 1.2) and not run into problems (see Section 2.1), there must be galvanic isolation somewhere in the circuit between the measurement side and the current excitation side, and it must be kept through the entire system. The system achieves it on the power supply module using isolated DC-DC converters, splitting power supply rails into two, one for constant current source (GND2) and one for measurement circuitry (GND). Galvanic of the constant source was done rather than isolating the main controller module, which would lead to the isolation of each connection used by the main controller module that uses a greater number of connections than the constant current source and the signal generator module. This option was more expensive. Hence, it was rejected.

The current block design consists of one DC-DC converter in a step-down configuration supplying the constant current module with greater voltage to not encounter saturation at its output. Other DC-DC converters supply voltages for digital and analog circuitry in step-down configuration. There was not much certainty about what voltage levels to select. One is clear: The 3.3 V is the voltage level used by MCU in the main controller unit. Thus, all devices communicating with the main controller should have 3.3 V logic level to avoid using level converters. Also, there shall be another 3.3 V line for direct digital synthesis (DDS) chip on the signal generator unit with reference to GND2 and ± 48 V rail to power constant current source, respecting the galvanic isolation described above. The selected multiplexer (MUX) chip; TMUX8108 have recommended maximum power supply of 100 V differential, thus ± 48 V was chosen to be on the safe side and it is dividable by 24 V, the output level of commonly available DC-DC converters.

Other voltages have no purpose in the system, but with future development in mind, they will have a place on the connector. Currently, the only potential use of another voltage level; 12 V is to power the STM32 Nucleo development board, which can use 12 V as input for its internal low-dropout regulator (LDO), thus powering ST-LINK its programmer and debugger, thus enabling development via USB without the need of an external programmer [15]. Also, the voltage of $\pm 12 \text{ V}$ is applicable in powering analog circuitry such as Op Amps.

3.2 Main controller

As a main controller, STM32F446RE was selected as the cheapest MCU (currently available); that has more than one internal ADC, and I already have experience with the STM32F4 series. When using two ADCs, we can make use of dual regular

simultaneous mode when sampling two channels [6]. One channel is for a current measurement and one for a voltage measurement, simultaneously measuring phase shifts between them. In this setup, where the conversion to a digital signal is happening on the main controller module, an offset voltage adder must mounted to ensure conversion from symmetrical voltage values to a proper range, accaptable by ADC, being 0–3.3V. To shift the input signal to the exact half of the power supply voltage, ensuring the use of the whole range, 1.65 V DC must be added.

Fig. 3.2: Offset adder simulation: active (a) and passive (b) voltage adder and low impedance simulation of the active electrode (c).

Two circuits were simulated to show the differences between a classical DC voltage adder with capacitive coupling and a voltage adder utilizing a summing amplifier. Both types share the same wiring for getting the offset voltage. It is obtained by a simple resistive divider consisting of R_3 , R_4 , R_5 , R_6 , all with the same value, dividing VDD respectively U_{ref} (pin of the MCU) by 2. To ensure the accuracy of this assumption, the values of resistors shall have a small tolerance. The advantage of using the active voltage adder is that it will work down to DC instead of passive capacitive coupling, but with a greater value of C_1 , the lower cutoff frequency f_1 will be very low (3.1), as a phase shift will be. Plus, we cannot measure DC voltage on probes, the whole concept stands on AC current injection and AC voltage measurement. With DC capabilities, we would not want to add offset voltage. Considering its convenience, the passive capacitive coupling circuit is used.

A second-order low-pass filter was added to limit noise and aliasing effect of ADC, consisting of R_{AIN} and C_{AIN} . This type was chosen as sufficient enough according to application note [6]. Sample rate of an ADC is 2.4 MSps, thus the Nyquist limit $(f_{samp}/2)$ equals 1.2 MHz, as shunt the cutoff frequency f_2 of the low-pass filter (3.2). Components with standard values were chosen. Thus, the final cutoff will not equal exactly that, but it is not a problem considering that in the current configuration, we will not measure signals greater than 100 kHz.

$$f_1 = \frac{1}{2\pi \cdot \left(\frac{R_5 \cdot R_6}{R_5 + R_6}\right) \cdot C_1} = \frac{1}{2\pi \cdot \left(\frac{100 * 100}{100 + 100}\right) \cdot 10^3 \cdot 100 \cdot 10^{-6}} = 0.032 \,\mathrm{Hz}$$
(3.1)

$$f_2 = \frac{1}{2\pi \cdot R_{\text{AIN}} \cdot C_{\text{AIN}}} = \frac{1}{2\pi \cdot 10 \cdot 10^3 \cdot 16 \cdot 10^{-12}} = 994.718 \,\text{kHz}$$
(3.2)

Fig. 3.3: Offset adder simulation: active (a) and passive (b) voltage adder and low impedance simulation of the active electrode (c).

The f_2 was verified by AC analysis in Figure 3.3 of the circuit in Figure 3.2, with results of simulation being the $f_2 = 960.557 \text{ kHz}$ for the passive offset adder. The cutoff frequency of the active offset adder was lower because the low-pass filter was more loaded by surrounding circuitry, resulting to $f_2 = 646.377 \text{ kHz}$. The small phase shift at 100 kHz should not be a problem because it happens both on the voltage measurement and on the current measurement. In the final calculation process, they subtract each other.

Pin assignment was done to ensure the most efficient way of rotting copper traces from MCU to connectors described in Section 3.5. Decupling, crystal circuitry, and other necessities are already mounted on the STM32 NUCLEO board. The problem with assembling the module with the STM32 NUCLEO development kit is that it will take a great amount of horizontal space; therefore, an additional connector is needed to extend the module's height.

All the communication interfaces SPI, I2C, and UART were separated into two, for example, SPI as an internal bus for the system and SPIp as the bus handling communicating with active electrodes, more detailed description in Section 3.5.

The Op Amp was added at the of the circuitry. It provides low output resistance for driving ADC. Also, it handles the protection by powering it via the same voltage the ADC is, saturating any potential voltage higher than the $U_{\rm ref}$.

3.3 Multiplexer module

As described in Section 2.1, we need some analog switches/multiplexers to replace relays; that was one of the main requirements to avoid noisy switching, high-cost and low lifetime. For measuring high impedances and constant current, we need to find the analog multiplexer with high voltage capabilities that correspond to the power supply voltage of the constant current source, that is ± 48 V. Table 3.3 lists high-voltage multiplexer/switch integrated circuits (ICs), currently available on the market [16, 17, 18, 19]. Communication interfaces used by multiplexers do not limit the selection of components; commonly used interfaces are available on the system's interconnection bus. Thus, no parameter in the Table 3.3 defines the interface. ¹

We decided to use a TMUX8108RUMR multiplexer for its easy-to-solder package, flat frequency characteristics, and no phase shift in the operation frequency band. As shown in Table 3.3, there is currently no device on the market that would allow the signals with 200 V peak-to-peak magnitude to pass. This implies that for using a higher voltages, it is necessary to use a relay for switching. Four analog

¹prices are only indicative, and they were taken from distributors as per unit quantity at the time of writing thesis.

Part number	$U_{\rm PP} - U_{\rm NN}, R_{\rm on}, f_{\rm cut-off},$ Package	Cost	Availability
TMUX8108RUMR	$200\mathrm{V}, 38\Omega, 200\mathrm{MHz},\mathrm{TSSOP}$	$206.40\mathrm{K}\check{\mathrm{c}}$	stock
ADG467BRZ	$80\mathrm{V}, 62\Omega, 170\mathrm{MHz},\mathrm{LQFP}$	$235.92\mathrm{K\check{c}}$	stock
CPC7601	$200\mathrm{V}, 27\Omega, 10\mathrm{MHz},\mathrm{LQFP}$	-	-
MAX4968	$210\mathrm{V}, 18\Omega, 30\mathrm{MHz},\mathrm{LQFP}$	$1507.68\mathrm{K\check{c}}$	stock

Table 3.1: Analog multiplexer parameters comparison

multiplexers are needed to choose between: (a) measuring active alectrode, labeled as U MUX, (b) reference groud for single-ended measurement, labeled as REG GND, (c) positive respectively and (d) negative electrode of constant current supply labeled as I+ and I- respectively. Four tracks are needed to control address pins; thus, sixteen will control all MUXs independently. The same tracks were used for controlling digital multiplexers, which will indicate the state of each electrode. As we have four states and only one can be active, connectors with two pairs of built-in LEDs in an anti-parallel configuration for each socket are used.

A classical RJ45 connector was used because it has enough pins to transfer all the signals, will always be available, and is the cheapest option. The same principle works for a cable. Also, we can use its twisted pairs as an advantage in power supply and the positive and negative connection of constant current supply. The number of output pins of selected TMUX8108RUMR determines a maximum of eight active electrodes connected to the module. Another module in the system is needed to extend the number of available electrode slots.

On the multiplexer module, there will be current measured in the form of an isolated operation amplifier, measuring a voltage drop across a shunt resistor with known resistance.

3.4 Active electrodes

In this section, a design process for an active electrode is described, resulting in a schematic diagram shown in Figure 3.4 and full hardware implementation on a board, which is shown in Figure 3.7. The upper limit of the input voltage on the active electrode is proportional to the power supply voltage of the constant current source, which is 48 V peak. The lower limit is not exactly stated. A suitable PGA supporting one of the interfaces provided by the system bus was required. After assessing the options, it was determined that the PGA280 was the most fitting choice for the intended application. A wide dynamic range of measurement must be accomplished.

Fig. 3.4: Schematic diagram of the active electrode/probe.

In other words, the active electrode must be able to measure voltages from units of millivolts to ± 48 V peak (power supply voltage of constant current source). To accomplish that, a programmable gain amplifier (PGA) must have been selected.

The PGA280 was chosen as the most suitable for the application. It has generalpurpose inputs/outputs (general-purpose input/outputs) that are used to control the attenuator and provide LED visualization of currently active modes directly on the probe. This additional feature has proven to be potentially helpful during the debugging stage of development or device usage in previous works. Commonly, these PGAs lack the high-voltage power supply capabilities required for our purposes. To address this insufficiency, a high-voltage switch, the TMUX8108 (the same used in the multiplexer module), is added before the PGA's input. This switch selects between R_1 to R_7 with R_8 forming resistor dividers to ensure attenuation from approximately 1 V/V to 0.28 V/V, respectively. The attenuation of 0.28 V/V will decrease the maximum input voltage ± 48 V to a voltage of 13.44 V which is further processable by the PGA. The second input of the PGA280 is used in combination with OPA2992 Op Amp with fixed gain to provide additional application for voltages below 25.8 mV, the minimal voltage range that with 1 V/V and 128 V/V gains set by the attenuator and PGA280 respectively matches the 3.3 V supply of the ADC. The fixed gain was experimentally set to 74 V/V with resistor values already used, ensuring a smooth link to ratios between the ranges established by the PGA280 and the attenuator. These three components, two of which have programmable amplification, allow several adjustable ranges to be built to take advantage of the full range of the n-bit ADC and, therefore, optimise the accuracy of the voltage level reading on the main unit side. These configurable ranges are listed in Table 2.1. These values were calculated accordingly:

$$U_{\rm max} = \frac{U_{\rm ref}}{K_{\rm pga}},\tag{3.3}$$

where U_{max} is a maximal voltage that can be attenuated/amplified by K_{pga} , the programmable gain of a PGA to match the maximal input voltage U_{ref} of an ADC without saturation. Above this value, it is necessary to decrease the K_{pga} gain to prevent saturation.

Gains of attenuator were created as arithmetic sequence from 1 V/V as the last term to the maximal attenuation needed K_N to between maximum input votlage 48 V and 13.2 V, the maximum voltage U_{max} of PGA280 with 3.3 V as the ADC reference voltage. The common gain difference ΔK_{att} of the attenuator is calculated via the equation

$$\Delta K_{\rm att} = \frac{1 - K_N}{N - 1},\tag{3.4}$$

$$K_N = \frac{U_{\text{max}}}{U_{\text{inp}}} \tag{3.5}$$

where U_{max} is maximal voltage that can be measured with the maximal attenuation of PGA, U_{inp} is maximal input voltage that needs to be measured at the input of the active probe and N is the number of switchable ranges.

In this case 7 outputs of the attenuator/multiplexer TMUX8108 are used, $U_{\rm inp} = 48$ V, maximal voltage that can be attenuated by PGA280 without saturation is $U_{\rm max} = 13.2$ V. After inserting the values into the equation, $\Delta K_{\rm att} = 0.120833$ V. All the gains $K_{\rm att}$ of the attenuator can subsequently be expressed as

$$K_{\text{att}_n} = 1 + (n-1) \cdot \Delta K_{\text{att}}, \qquad (3.6)$$

$$n \in \{1, 2, \dots, N\}. \tag{3.7}$$

These selectable gains are listed in fifth column of Table 2.1. Combining both the gain of attenuator and the gain of PGA, we get multiple values of total gain

$$K_{\rm U} = K_{\rm att} \cdot K_{\rm pga}, \tag{3.8}$$

thus mutiple ranges that can be switched. These ranges corresponds to a threshold voltages $U_{\text{threshold}}$ that are telling the mamimal voltage at the input of the active probe that can be measured without saturation due to the corresponding total gain K_{U} . The threshold voltage can be calculated accordingly:

$$K_{\text{threshold}} = \frac{U_{\text{ref}}}{K_{\text{U}}}.$$
 (3.9)

Some calculable ranges overlap with each other because their combination of K_{att} and K_{pga} results in a similar total gain K_{U} for higher K_{att} and lower K_{pga} and therefore it is not worth adding them to the list of ranges in Table 3.2 and because of this the 3 highest attenuations K_{att} are not used for indices 7 and higher.

Index	$U_{\text{threshold}}$ [V]	$K_{\rm U} [{\rm dB}]$	$K_{\rm U} [{\rm V/V}]$	$K_{\rm att} [{\rm V/V}]$	$K_{\rm pga} [{\rm V/V}]$
0	48.000	-23.255	0.069	0.275	
1	33.347	-20.091	0.099	0.396	
2	25.548	-17.777	0.129	0.517	
3	20.706	-15.952	0.159	0.638	0.25
4	17.407	-14.444	0.190	0.758	
5	15.014	-13.160	0.220	0.879	
6	13.200	-12.041	0.250	1.000	
7	10.353	-9.931	0.319	0.638	
8	8.703	-8.423	0.379	0.758	0.5
9	7.507	-7.139	0.440	0.879	0.5
10	6.600	-6.021	0.500	1.000	
11	5.176	-3.910	0.638	0.638	
12	4.352	-2.403	0.758	0.758	1
13	3.754	-1.119	0.879	0.879	1
14	3.300	0.000	1.000	1.000	
15	2.588	2.110	1.275	0.638	
16	2.176	3.618	1.517	0.758	2
17	1.877	4.902	1.758	0.879	2
18	1.650	6.021	2.000	1.000	
19	1.294	8.131	2.550	0.638	
20	1.088	9.638	3.033	0.758	4
21	0.938	10.923	3.517	0.879	4
22	0.825	12.041	4.000	1.000	
23	0.647	14.151	5.100	0.638	
24	0.544	15.659	6.067	0.758	0
25	0.469	16.943	7.033	0.879	0
26	0.413	18.062	8.000	1.000	
27	0.324	20.172	10.20	0.638	
28	0.272	21.680	12.13	0.758	16
29	0.235	22.964	14.06	0.879	10
30	0.206	24.082	16.00	1.000	
31	0.162	26.193	20.40	0.638	
32	0.136	27.700	24.26	0.758	<i>3</i> 0
33	0.117	28.984	28.13	0.879	52

Table 3.2: Voltage ranges of the active probe.

Index	$U_{\text{threshold}}$ [V]	$K_{\rm U} [{\rm dB}]$	$K_{\rm U} [{\rm V/V}]$	$K_{\rm att} [{\rm V/V}]$	$K_{\rm pga} \; [{\rm V/V}]$
34	0.103	30.103	32.00	1.000	
35	0.081	32.213	40.80	0.638	
36	0.068	33.721	48.53	0.758	64
37	0.059	35.005	56.26	0.879	04
38	0.052	36.124	64.00	1.000	
39	0.040	38.234	81.60	0.638	
40	0.034	39.741	97.06	0.758	199
41	0.029	41.026	112.5	0.879	128
42	0.026	42.144	128.0	1.000	

Table 3.2: Voltage ranges of the active probe (continued).

The attenuator is placed after high voltage Op Amp, the OPA454 in voltage follower configuration to ensure high input impedance of the active probe and not affect the measurement currently running on other electrodes by large leakage current.

Some interface should be established to control the active probe. The serial peripheral interface (SPI) was chosen because the PGA280 supports it directly. The probe are not connected in daisy-chain configuration, as it is done on most systems focusing on the medical field, where daisy-chaining a chest belt is the logical way of handling communication. Probes of the system cannot do that because they are isolated from current injection part of the system and the reference groud of the probe needs to be connected to some other electrode. Because of that all the probes are connected to the central system where the switching hapens, so also the communication is handle in star-like scheme. This involves handle probe multiplexing via a *chip select* (\overline{CS}) pin, that is pulled low if the probe is in MEASUREMENT mode.

The parts mounted on active probe requires multiple power supply voltages to work properly. The is need to supply ± 48 V for the TMUX8108 multiplexer and OPA454 Op Amp, ± 18 V is required to supply OPA2992 preamplifier and PGA280s internal analog circuitry, 3.3 V for both internal analog and digital circuitry of PGA280 and 1.65 V as a reference or common ground for internal output circuitry of the PGA280. It was decided to use linear regulators instead of switching regulators to optain all the voltages below ± 48 V. Linear regulator operates without swithing so they do not generate switching noise, harmonics etc. instead of switching regulators that do. Also they are much cheaper. Thermal considerations are important apect to take acount during power supply design consisting of linear regulators, especially in this case because it was needed to regulate 18 V from 48 V, so there is high fixed 30 V difference between input and output of the regulator. To lower the energy dissipation, it was necessary to keep the current consumption low as possible. The maximum power dissipation $P_{D_{max}}$ of the linear egulator is calculated accordingly:

$$P_{\rm D_{max}} = \frac{T_{\rm J_{max}} - T_{\rm A}}{\theta_{\rm JA}},\tag{3.10}$$

where $T_{\rm J_{max}}$ is a maximum juction temperature, the thermal rating of the device, $T_{\rm A}$ is ambient temperature and $\theta_{\rm JA}$ is a thermal resistance from juction to ambient. The current power dissipated by the devide $P_{\rm D}$ is expressed as

$$P_{\rm D} = (U_{\rm IN} - U_{\rm OUT}) \cdot I_{\rm OUT}, \qquad (3.11)$$

where $U_{\rm IN}$ is the input voltage and $U_{\rm OUT}$ is the output voltage of the linear regulator and $I_{\rm OUT}$ is the current sorced by the regulator (or sinced for negative rail regulator LM377) [20, 21]. It is useful to manupulate the equation to:

$$I_{\rm OUT} = \frac{P_{\rm D}}{U_{\rm IN} - U_{\rm OUT}}.$$
(3.12)

From known values the maximal current supplied by the regulator can be calculated. Given the $T_{\rm J_{max}} = 128$ °C for both the LM377 and LM317, $T_{\rm A} = 50$ °C as the natural convection air flow and $\theta_{\rm JA} = 66.8$ °C/W for LM317 and $\theta_{\rm JA} = 58.3$ °C/W for LM337, these thermal resistance values coresponds to specific package SOT-223. This package was chosen for is small diameters but its thermal characteristics are worst that larger TO-263 (D2PAK). If it turns out the package SOT-223 is not sufficient, TO-263 will be mouted on the *printed circuit board* (PCB). From given values we can calculate maximal power dissipation for both devices

$$P_{\rm D_{max}} = \frac{T_{\rm J_{max}} - T_{\rm A}}{\theta_{\rm JA}},\tag{3.13}$$

LM317:
$$P_{\rm D_{max}} = \frac{128 - 50}{66.8} = 1.167 \,\rm W,$$
 (3.14)

LM337:
$$P_{D_{\text{max}}} = \frac{128 - 50}{58.3} = 1.338 \,\text{W.}$$
 (3.15)

These values are similar to those measured for SOT-223 package sized copper fill in aplication report from manufacture [22]. From knowm maximal power disipipations, the calculation of maximal current proceeds:

$$I_{\rm OUT_{max}} = \frac{P_{\rm D_{max}}}{U_{\rm IN} - U_{\rm OUT}},$$
(3.16)

LM317:
$$I_{\rm OUT_{max}} = \frac{1.167}{48 - 18} = 38.92 \,\mathrm{mA},$$
 (3.17)

LM337:
$$I_{\rm OUT_{max}} = \frac{1.338}{48 - 18} = 44.60 \,\mathrm{mA}.$$
 (3.18)

Considering probe in MEASUREMENT mode with all peripherals enabled it can be predicted what will be the current consumption of the active probe. The maximal quiescent current I_Q of the devices are listed in Table 3.4 [23, 24, 25, 17, 26, 27, 28].

If we compare current consumption on 18 V rail in the third column of Table 3.4 with calculated maximal current sourced by LM317 there is sufficient room for current changes due to parts internal switching and passive components current consumptions that were not take to an account during calculation (3.17). This safe gab between maximal and predicted current consumption also applies for -18 V rail and LM337 (3.18). Another obstacle was a greater input-to-ouput differential voltage than absolute maximum rating of the rehulators that will accour after connecting the active probe to the ± 48 V power supply. If we assume all the capacitors after regulators are discharched, there will be input-to-output differential voltage $U_{\rm IN} - U_{\rm OUT} = 48$ V which is greater that the maximum rating which is 40 V [23, 24]. To solve it zener diodes D_1 and D_2 were added between the input and output of the regulator to prevent voltage $U_{\rm IN} - U_{\rm OUT}$ rise above 36 V. These diodes actes as low resistance path for changing capacitors placed after regulators in initial input voltage rise. This theory was simulated for LM317 using schematic in Figure 3.6. Results of the simulation proved the function of the diodes Figure 3.5.

As can be seen, the slow regulation $U_{\rm OUT}$ would cause device failure in approximately 40 µs where the differential volatege $U_{\rm IN} - U_{\rm OUT}$ would be greater that absolute maximum rating. Instead of failure diode provides low resistace way for regulator output capacitance charge. After approximately 130 µs regulators output will be charged to 12 V, zener diode will stop conduct and regular will start regulating. It is not shown in the simulation but the ouput voltage $U_{\rm OUT}$ will reach 18 V eventualy. PCB design was created and four PCBs were manufactured. Part were soldered using solder paste, stencil and hot air station with heated bed.

Voltage rail	$+3.3 \mathrm{V}$	-18 V	$+18 \mathrm{V}$	-48 V	$+48 \mathrm{V}$
LM3X7		$5.3 \mathrm{mA}$	$5.3 \mathrm{mA}$		
PGA280	$1.13~\mathrm{mA}$	$3 \mathrm{mA}$	$3 \mathrm{mA}$	-	-
OPA2992	-	$1.4 \mathrm{mA}$	$1.4 \mathrm{mA}$	-	-
OPA454	-	-	-	$2 \mathrm{mA}$	$2 \mathrm{mA}$
uA78M33	-	-	$6 \mathrm{mA}$	-	-
mode LEDS	$6 \mathrm{mA}$	-	-	-	-
power LED	-	$1.4 \mathrm{mA}$	$1.4 \mathrm{mA}$	-	-
Total	$7.13 \mathrm{~mA}$	$11.1 \mathrm{mA}$	$17.1 \mathrm{~mA}$	$2 \mathrm{mA}$	$2 \mathrm{mA}$
Probes predic	cted current	t consumpt	ion	$26.23 \mathrm{mA}$	13.1 mA

Table 3.4: Predicted current consumption of the active probe

Fig. 3.5: Schematic diagram used for simulation of probes power supply.

Fig. 3.6: Simulation of the probe connection to the system.

Fig. 3.7: Image render The rendered image on the left and the actual photo of the probe fitted with components on the right.

3.5 Interconnection

Before any physical connection can be defined, research on usable components must have been carried out. For example, there certainly must be available communication interfaces like I2C, SPI, and UART available for ICs mounted on modules. These interfaces are commonly used by ADCs, DDS chips, and some multiplexers use them also. The communication bus must be separated into interfaces used within the system and interfaces used for probes. The reason is that the probe interfaces are addressed/enabled differently than modules and ICs on them and for preventing the address collisions. All the interfaces that are labeled with the letter "P" at the end (SPI_P), signalizing the usage of probes/active electrodes and all the interfaces without it are used for communication within the system.

There is also a need to read and write logic signals without any interface. It is done by utilizing a GPIO extender MCP23017 connected to the modules' I2C bus, where this feature is needed. Modules are selected by an address set on the dipswitch of the module connected to address pins of the GPIO extender. In this configuration, it is more cost-efficient to galvanically isolate two wires of I2C communication than individual GPIOs between the main controller module and any module referencing the GND2 (GNDS) (signal generator or constant current source), the galvanic isolation is shown in Figure 3.8.

Fig. 3.8: Example of interface and galvanic isolation of a module.

It was also done instead of defining a GPIO bus, which would take up a large number of pins on a connector, and there would have to be logic to control reading, writing, and addressing each bit. On the connector, there is also carried power supply voltage sourced from the power supply module on Section 3.1, NRST signal connected to all ICs with RESET pin and button to full system capabilities, and UART interface for potential extension of a user interface module and analog pins A0–A3 for possible extension of analog reading/writing, MU for measured voltage, MI for measured current on the multiplexer module, and SIG pin referenced to the GND2 as the analog signal of a synthesized waveform.

All the analog pins must carry a signal with a range of ± 1.65 V; these values are related to the offset adder on the main controller side described in Section 3.2. All the digital pins can acquire only low or high states, respectively 0 V or 3.3 V as logical levels of the STM32 mounted on the main controller module. All the description is simplified in Figure 3.9.

Fig. 3.9: System interface diagram.

Pin header with 2.54 mm pitch was selected as the connector. As it is an unshielded type of connector, electromagnetic compatibility (EMC) performance precautions were taken, for example, using additional return conductors evenly spaced through the connector and always next to the carrying one. In practice, there is always one ground pin for a signal pin. The exact pin assignment scheme was done according to EMC standards [12]. All the modules are designed to be stackable with the exact dimension of PCB for all of them.Interconnection is split into two connectors, one for power and one for data, mounted opposite each other. This way, we ensure mechanical stability without the need for support. However, mechanical support is envisaged as standoffs, for which holes are prepared at each corner for seating. The connectors are different sizes and asymmetrical as opposed to holes on PCB to ensure the correct fitting of the modules to each other and to prevent short circuits. As described in main controller Section 3.2, if there is a need for extending height between modules, additional connectors can be stacked on top of each other to achieve the desired height.

For potential extension of the system with a module, these rules must be complied with: the position of the connector and holed for standoffs must be the same. If the new module is not passive, the GPIO extender must be connected to the I2C bus with a DIP switch and a new address assigned. A driver must be made for the new module, handling all its features.

4 Firmware

Firmware developed for main controller that utilizes STM32 microcontroller provides a comprehensive application programming interface (API) for interfacing with the active probes it the modular EIT system. Library simplifies the interaction with the peripherals of STM32 microcontroller with use of hardware abstraction layer (HAL) driver library. The use of HAL driver maximazes portability across the STM32 portfolio [29]. The library includes a set of functions and structures essential for controlling and managing the active probes. It is also prepared for interfacing modules directly, that means freeing the programmer from the fact that there are different units. The main idea is that the developer, after initializing the tomograph units, just calls functions from the **probe**.h library and the library takes care of calling functions of the other units from the system library set.

4.1 Probe library

Library defines multiple types to make it easier for the user to identify function paramters. This way, most of the parameters of a function are known and fixed and can be referenced by type definotions. One from these types is **Probe_TypeDef** which defines a handler for physical probe, it stores is variables and states. Most of the function within the library take **Probe_TypeDef** as a first parameter access specific peripherals that corresponds to the probe. There can be multiple probe with different SPI handler, they can be connected to different MUX unit etc. **Probe_TypeDef** type definition is shown in Listing 4.1.

```
typedef struct
{
    uint8_t initialized;
    uint8_t number;
    // storing last written gpio register of PGA
    mounted on probe
    uint8_t gpio_reg;
    // stores individual mode states currectly
    activated for the probe,
    // index of the array corespond to the probe mode
    declared in ProbeMode_Type
    ProbeModeStatus_Type modes[4];
    // index of currently selected gain from gains
```

```
uint8_t gain_index;
// calibrated values of actual configurable gains
ProbeGains_Type gains;
// currenty selected gain and range of PGA and
ATTENUATOR in the probe respectively
ProbeGainSet_Type gain;
ProbeRangeSet_Type range;
// pointers to SPI communication handler and MUX
module handler for probe selection
SPI_HandleTypeDef* hspix;
```

Mux TypeDef* hmuxx;

```
} Probe_TypeDef;
```

Listing 4.1: Probe structure type definition

Here is a brief overview of the primary functions declared in probe.h library.

```
void probe_init(Probe_TypeDef* probe,
SPI_HandleTypeDef* hspix, Mux_TypeDef* hmuxx,
const uint8_t number)
```

Probe initialization function sets default/startup bits in the PGA280 registers. It also assignes number to the probe instance and set specific SPIx inteface and $\overline{\text{CS}}$ /probe selection for communication with the active probes. It will soft-restart the PGA280, enable attenuator control through special function register and itterate through all the probe indicating successfull init visualization via *light-emitting diode* (LED). Function shall be called after HAL SPI initialization, hspix definition, $\overline{\text{CS}}$ pin and *general-purpose input/output* (GPIO) initialization. Function serves as probes configuration initialization for the probe API, so it need to be called before any probe API operation.

```
void probe_mode(Probe_TypeDef* probe, const
ProbeMode_Type mode, const ProbeModeStatus_Type
status)
```

Probe mode selection function sets the probe to one of four specific modes. Function access probes modes array which stores currently active modes of the probe. This Function also guard the forbidden state when the probe cannot acquire both POSITIVE and NEGATIVE current excitation modes. If user tries to set the probe to POSITIVE mode when the NEGATIVE mode is active, info message occurs and **NEGATIVE** is set after **POSITIVE** mode is disabled. After successful mode assignment, the function displays the current modes on the LEDs mounted on the probe.

```
void probe_gain(Probe_TypeDef* probe, const
uint8 t gain_index)
```

Probe gain selection function is used for swithing between voltage gains. The gain_index parameter corresponds to settable voltage gain listed in Table 3.2. The setted gain_index is stored within the probe structure and points to specific gain in gains array which can be calibrated for each probe separately with probe_calibrate function.

```
float probe_voltage(Probe_TypeDef* probe, const
    uint32_t adc_value)
{
    if (probe == NULL) goto catch_null_probe;
    float gain = ((float *)(&probe->gains))[probe->
    gain_index];
    return (float)(2.0f * (3.3f * (adc_value / 4096.0f)
        - 1.65f) / gain);
catch_null_probe:
    log("ERROR: Define probe before calling function.\n
    ");
    return 0;
}
```

Voltage conversion function tranform ADC value measured by the peripheral to actual voltage. ADC value is devided by the configured gain of the probe. The conversion assumes 12-bit differential ADC. It is necessary to ensure stable and accurate 1.65 V reference on the active electrode. In current state there is no way to measure reference voltage on electrode. It is proved that reference on active probe is sufficient, reference error if present would cause great diviating in voltage measurent near DC. The Stability of the reference is confirmed in Figure 5.1.

5 Evaluation by measurement

An application written in MATLAB was created for value measurement and development acceleration. It sends/reads data from the main controller/STM32 unit through the *universal asynchronous receiver-transmitter* (UART) interface. It includes the MEIT class, which provides simple API for this purpose. This class supports various functionalities, including setting operational parameters, initiating measurements, and processing the acquired data. The properties of the MEIT class are port, baud rate, sampling frequency, and measured data, which are structures that store measured parameters such as voltage, current, phase shift, and impedance. Using this application proceeding frequency characteristics of the probe were measured.

The frequency characteristics of the active probe were measured to evaluate hardware design decisions. Figure 5.1 shows voltage gain dependence on frequency for some configurable amplifications described by indexes in Table 3.2. Figure 5.2 shows phase dependence on frequency for specific indexes.

Fig. 5.1: Frequency characteristics of probes settable amplifications.

Fig. 5.2: Phase shift characteristics of probes settable amplifications.

Fig. 5.3: Measurement of 7.071 V RMS for gain index = 0.

Fig. 5.4: Measurement of 1.131 V RMS for gain index = 14.

Fig. 5.5: Measurement of 8.761 mV RMS for gain index = 42.

The frequency characteristics verified the functionality of the active probe amplification switching. Some gain indexes are not shown in the figures, but they were also tested, and they follow the same characteristics as nearby amplification. Figure 5.1 shows the amplitude voltage measurement frequency range for a particular amplification. This confirms near zero voltage measurement deviation error from DC to 100 kHz for amplification with gain index from 11 to 32, which we are able to measure voltage from 136 mV to 5.176 V with effectively occupied whole range of microcontrollers ADC. For voltages out of this range, the maximum frequency where near zero voltage deviation error is still fulfilled is 40 kHz. That means we can reliably measure voltage from 26 mV to 48 V within DC to 40 kHz with a whole range of microcontrollers ADC effectively occupied.

Figure 5.2 shows the amplification phase shift dependency on frequency. Undesirable phase error observed at frequencies near 100 kHz increases with electrode amplification value. Minor errors observed with amplification index 29 and higher will be partially compensated using the same circuitry in the current sensing part. The phase shift measurement error is near zero from (DC) to 40 kHz for gain indexes below 29. Above gain index 29 is near zero phase shift moved to the lower frequency of 6 kHz.

More detailed voltage measurements are shown in Figures 5.3 to 5.5. These plots show one measured set of points of phase and gain frequency characteristics from which the voltages and frequency of input signal were calculated. They representes an ADC buffer transformed to voltage buffer using probe_voltage function. All the signals are within the near-zero voltage deviation frequency range described above. The differences between actual input voltage on the electrode and measured voltage differences between gain indexes. The linearity of the frequency characteristic gain and calibration options proves compensation capabilities of the system for these errors.

Conclusion

The system was created in the form of a system design, allowing modules to be connected independently of their function and then implemented in the system. From the beginning, the system had to be seen as a whole so that no part of the measurement chain was missing. The active electrode was designed and manufactured. For the multiplexer module and the active electrode, the current state of the market was investigated, and the components corresponding to the needs were selected.

The initial thought of a measurement method using active electrodes with switchable reference has been clarified as correct. With the help of the designed firmware, which took care of the communication with the active electrode, read the ADC and software written in MATLAB and evaluated the correctness of the measurement. The system can reliably measure maximum voltages from 103 mV to 5.176 V for DC to 100 kHz and from 26 mV to 48 V in the DC to 40 kHz range without saturating the measurement circuitry. The system also exhibited minimal phase shift between the channels and the analogue-to-digital converter inputs, which is crucial for measurement accuracy. It was proven that relays would be needed for voltages above 48 V, especially current switching.

Schematic diagrams of other modules were not created because of the time concerns. Most of the time was spent designing a system without a forgotten flaw that would lead to rework. In this state, a strong foundation is given for the development of the modules and finalization of the system. The proposed scheme of a modular system for electrical impedance tomography and the implementation of active electrodes represents a significant step forward towards a complete system design that, due to its modularity, could be used not only in medicine but also in other fields such as geophysics, materials engineering or to develop the electrical impedance tomography method as such.

Bibliography

- Roman Vaněk and Jan Mikulka. Modular system for electrical impedance tomography. In Proceedings of the 30th Student EEICT 2024, Brno, 2024.
- [2] OpenAI. Chatgpt: A large language model for text generation and grammatical assistance, 2024. Accessed on May 27, 2024. URL: https://www.openai.com/ research/chatgpt.
- [3] Andy Adler and David Holder, editors. Electrical Impedance Tomography: Methods, History and Applications. CRC Press, Boca Raton, 2 edition, December 2021. doi:10.1201/9780429399886.
- [4] Jong-Hyuk Choi and Bok-Hee Lee. An analysis on the Frequency-dependent grounding impedance based on the ground current dissipation of counterpoises in the two-layered soils. *Journal of Electrostatics*, 70(2):184-191, April 2012. URL: https://www.sciencedirect.com/science/article/pii/ S0304388611002026, doi:10.1016/j.elstat.2011.12.003.
- [5] Alistair Mcewan, G Cusick, and David Holder. A review of errors in multifrequency EIT instrumentation. *Physiological measurement*, 28:S197–215, August 2007. doi:10.1088/0967-3334/28/7/S15.
- [6] STM32TM's ADC modes and their applications, 2010. URL: https://www.st.com/resource/en/application_note/ an3116-stm32s-adc-modes-and-their-applications-stmicroelectronics. pdf.
- [7] Tomasz Piasecki, Konrad Chabowski, and Karol Nitsch. Design, calibration and tests of versatile low frequency impedance analyser based on ARM microcontroller. *Measurement*, 91:155–161, September 2016. doi:10.1016/j. measurement.2016.05.057.
- [8] Paul Horowitz and Winfield Hill. *The Art of Electronics Third Edition*. Cambridge University Press, New York, third edition edition, 2015.
- [9] Texas Instruments. A Comprehensive Study of the Howland Current Pump, 2008. URL: https://www.ti.com/lit/an/snoa474a/snoa474a.pdf?ts= 1703462665762&ref_url=http%253A%252F%252Ffocus.ti.com%252Flit% 252Fpdf%252Fsnoa474.
- [10] David Zimniok. Analogově-digitální modul pro elektrickou impedanční tomografii, 2023. URL: http://hdl.handle.net/11012/212640.

- [11] B. Brazey, Y. Haddab, N. Zemiti, F. Mailly, and P. Nouet. An open-source and easily replicable hardware for electrical impedance tomography. *HardwareX*, 11:1-14, 2022. URL: https://www.sciencedirect.com/science/article/ pii/S2468067222000232, doi:10.1016/J.OHX.2022.E00278.
- [12] Keith Armstrong. Another emc resource from emc standards emc techniques in electronic design part 2 cables and connectors. *Design Techniques for EMC*, 44(2):-39, 2009. URL: https://www.emcstandards.co.uk/.
- [13] R. J. Yerworth, R. H. Bayford, G. Cusick, M. Conway, and D. S. Holder. Design and performance of the uclh mark 1b 64 channel electrical impedance tomography (eit) system, optimized for imaging brain function. *Physiological Measurement*, 23(1):149–158, 2002. doi:10.1088/0967-3334/23/1/314.
- [14] Michelle M. Mellenthin, Jennifer L. Mueller, Erick Dario León Bueno de Camargo, Fernando Silva de Moura, Talles Batista Rattis Santos, Raul Gonzalez Lima, Sarah J. Hamilton, Peter A. Muller, and Melody Alsaker. The ACE1 Electrical Impedance Tomography System for Thoracic Imaging. *IEEE Transactions on Instrumentation and Measurement*, 68(9):3137–3150, September 2019. doi:10.1109/TIM.2018.2874127.
- [15] STM32 Nucleo-64 boards, 2020. 14. URL: https://www.st.com/resource/en/user_manual/ um1724-stm32-nucleo64-boards-mb1136-stmicroelectronics.pdf.
- [16] Analog Devices Inc. ADG467 LC2MOS Octal SPST Switches, July 2009. Rev.
 D. URL: https://www.analog.com/media/en/technical-documentation/ data-sheets/ADG467.pdf.
- [17] Texas Instruments Incorporated. TMUX8108 8:1 Multiplexer, March 2021.
 Rev. A. URL: https://www.ti.com/lit/ds/symlink/tmux8108.pdf.
- [18] IXYS Integrated Circuits Division. CPC7601 Single-Channel Normally Open OptoMOS Relay, February 2013. URL: https://www.ixysic.com/home/pdfs. nsf/www/CPC7601.pdf/\$file/CPC7601.pdf.
- [19] Maxim Integrated. MAX4968/MAX4968A Ultra-Low Noise, Wideband, Variable-Gain Amplifiers, September 2012. URL: https://datasheets. maximintegrated.com/en/ds/MAX4968-MAX4968A.pdf.
- [20] Bruce Hunter and Patrick Rowland. Linear Regulator Design Guide For LDOs. Application Report, 2008.

- [21] Texas Instruments Incorporated. Semiconductor and ic package thermal metrics. Technical Report SPRA953D, Texas Instruments Incorporated, March 2024. Revised from December 2003. URL: http://www.ti.com/lit/an/ spra953d/spra953d.pdf.
- [22] Texas Instruments Incorporated. An-1028 maximum power enhancement techniques for power packages. Technical Report SNVA036B, Texas Instruments Incorporated, May 2013. Revised from June 2001. URL: http://www.ti.com/ lit/an/snva036b/snva036b.pdf.
- [23] Texas Instruments Incorporated. LM137/LM337-N 3-Terminal Adjustable Negative Regulators, November 2016. Rev. H. URL: https://www.ti.com/lit/ ds/symlink/lm137.pdf.
- [24] Texas Instruments Incorporated. LM317 3-Terminal Adjustable Regulator, August 2016. Rev. M. URL: https://www.ti.com/lit/ds/symlink/lm317.pdf.
- [25] Texas Instruments Incorporated. PGA280 Programmable Gain Amplifier, September 2015. Rev. E. URL: https://www.ti.com/lit/ds/symlink/ pga280.pdf.
- [26] Texas Instruments Incorporated. OPA2992 High-Voltage, Low-Noise Operational Amplifiers, October 2020. URL: https://www.ti.com/lit/ds/ symlink/opa2992.pdf.
- [27] Texas Instruments Incorporated. uA78M33 Positive Voltage Regulator, April 2017. Rev. D. URL: https://www.ti.com/lit/ds/symlink/ua78m33.pdf.
- [28] Texas Instruments Incorporated. OPA454 High-Voltage Operational Amplifier, June 2014. Rev. B. URL: https://www.ti.com/lit/ds/symlink/opa454. pdf.
- [29] STMicroelectronics. Description of STM32F4 HAL and low-layer drivers, 2021. UM1725. URL: https://www.st.com/resource/en/user_manual/ um1725-description-of-stm32f4-hal-and-lowlayer-drivers-stmicroelectronics. pdf.

Symbols and abbreviations

EIT	electrical impedance tomography
ADC	analog-to-digital convertor
PCB	printed circuit board
FEEC	Faculty of Electrical Engineering and Communication
BUT	Brno University of Technology
SNR	signal-to-noise ratio
MCU	microcontroller
MUX	multiplexer
DDS	direct digital synthesis
IC	integrated circuit
LDO	low-dropout regulator
Op Amp	operational amplifier
EMC	electromagnetic compatibility
GPIO	general-purpose input/output
PGA	programmable-gain amplifier
SPI	serial peripheral interface
$\overline{\mathrm{CS}}$	chip select
UART	universal asynchronous receiver-transmitter
API	application programming interface
LED	light-emitting diode
HAL	hardware abstraction layer
DMA	direct memory access

A Listing of digital appendix

/.....root directory of archive attachment _Firmware meit-f302r8 firmware was developed for STM32F302R8Tx Core Inc.....libraries of the firmware, partially generated by \$TM32CubeMX adc.h config.h dma.h gpio.h main.h _meit.h mux.h _probe.h.....for probe handling _spi.h _stm32f3xx_hal_conf.h _stm32f3xx_it.h _tim.h _usart.h Src soucre code of the firmware, partially generated by \$TM32CubeMX _adc.c dma.c _gpio.c _i2c.c _main.c.....main program loop, system initialization _meit.c _mux.c _probe.c....soucre code of the probe library _spi.c _stm32f3xx_hal_msp.c _stm32f3xx it.c _stm32f4xx_hal_msp.c _stm32f4xx it.c system_stm32f3xx.c system_stm32f4xx.c _tim.c _usart.c Drivers.....STM HAL driver F3 V1.11.4 _ . . . Makefile

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	MEIT_switch multiplexer unit hardware
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	D_Zener.lib
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