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Faculty of Electrical Engineering
and Communication

MASTER'S THESIS

Brno, 2020 Bc. Lukáš Jagla

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FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
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DEPARTMENT OF RADIOENGINEERING
ÚSTAV RADIOELEKTRONIKY

ADAPTATION OF DIGITAL PREDISTORTER TO LINEARIZE AMPLIFIERS USING COMPARATOR
ADAPTACE DIGITÁLNÍHO PŘEDZKRESLOVAČE PRO LINEARIZACI ZESILOVAČŮ S POUŽITÍM KOMPARÁTORU

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

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BRNO UNIVERSITY OF TECHNOLOGY
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Master's Thesis

Master's study field **Electronics and Communication**

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Student: Bc. Lukáš Jagla ***ID:*** 173665

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TITLE OF THESIS:

Adaptation of digital predistorter to linearize amplifiers using comparator

INSTRUCTION:

Get knowledge of digital predistortion methods for linearising radio-frequency power amplifiers. Focus especially at methods employing a comparator in the feedback, replacing the conventional analogue-to-digital converters. Design the digital predistorter hardware with the adaptation employing a level-crossing analogue converter based on a comparator and select the particular components.

Implement the designed hardware. Make the measurements with the realized hardware and evaluate its applicability for the digital predistorter adaptation. Try to adapt the digital predistorter by employing the realized hardware.

RECOMMENDED LITERATURE:

[1] LUO, Fa-Long et al. Digital Front-End in Wireless Communications and Broadcasting: Circuits and signal processing. Cambridge: Cambridge University Press, 2011. ISBN 9781107002135.

[2] WANG, H. et al. Forward modeling assisted 1-bit data acquisition based model extraction for digital predistortion of RF power amplifiers. In 2017 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR). Phoenix: IEEE, 2017. s. 59-62.

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Supervisor: doc. Ing. Tomáš Götthans, Ph.D.

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ABSTRACT

This master's thesis presents a development of a new hardware implementing a comparator in the feedback path of DPD systems. A new architecture is proposed and selected features are verified by simulations. Subsequently, the suitable components are selected for high-speed performance and an acquisition module is proposed. A 4-layer PCB is well designed, manufactured, and prepared for further work. Afterwards, an appropriate firmware is developed for signal transmission and data acquisition. The obtained results serves for the evaluation of the proposed architecture and for its future implementation in real DPD systems.

KEYWORDS

Digital predistortion, linearization, comparator, edge-time acquisition, FPGA

ABSTRAKT

Diplomová práce pojednává o návrhu nového hardwaru využívající komparátor ve zpětné vazbě systému pro digitální předzkreslování signálu. Vybrané vlastnosti navrhované architektury jsou ověřeny pomocí simulací a následně jsou zvoleny komponenty vhodné pro vysokofrekvenční použití za účelem implementace. Na bázi předložené architektury je navržen akviziční modul včetně obvodové realizace a vytvoření plošného spoje. Zhotovený plošný spoj je osazen a připraven pro další testování. Dále je navržen příslušný firmware pro příjem a vysílání signálu a získávání naměřených dat. Obdržené výsledky jsou určeny pro zhodnocení vlastností hardwaru a budoucího využití architektury v systémech digitálních předzkreslovačů.

KLÍČOVÁ SLOVA

Digitální předzkreslování, linearizace, komparátor, detekce času hrany, FPGA

JAGLA, Lukáš. *Adaptation of digital predistorter to linearize amplifiers using comparator*. Brno, 2019, 93 p. Master's Thesis. Brno University of Technology, Fakulta elektrotechniky a komunikačních technologií, Ústav radioelektroniky. Advised by doc. Ing. Tomáš Götthans, Ph.D.

ROZŠÍŘENÝ ABSTRAKT

Evoluční nároky kladené na lidskou populaci představují pro vývoj elektroniky nejen v oblasti bezdrátových komunikací stejné požadavky, a to zejména ve smyslu efektivity a účinnosti takovýchto systémů. Rychlost tohoto procesu lze reflektovat například faktem, že ačkoli 5G systémy se teprve zavádějí do běžné praxe, výzkum v oblasti 6G technologií již dávno započal.

Nedílnou součást vysílacího řetězce tvoří výkonový zesilovač, a to z pravidla na jeho konci, umožňující přenos signálu o jisté úrovni do okolního prostředí. Při práci s takovýmto zesilovačem je nutno počítat s jeho nelineární charakteristikou, jenž ji rozděluje na dvě oblasti. Jako první z nich lze označit oblast saturace, kde zesilovač pracuje s vysokou účinností, na druhou stranu výstupní signál je zde značně zkreslen. V oblasti lineární již zkreslení výstupního signálu pozorovatelné není, ovšem účinnost je v tomto případě velmi nízká. Využití linearizačních metod, jenž umožňují zesilovači pracovat poblíž saturace a tím i v oblasti s vyšší účinností, je tomto případě velmi přínosné.

Optimalizačním trendem každého elektrického zařízení je snižování jeho spotřeby nebo zjednodušování jeho vnitřní struktury. Touto cestou jsou taktéž vedeny systémy pro předzkreslování signálu určené pro linearizaci výkonových zesilovačů. Velmi slibnou metodou je digitální předzkreslování signálu, na jehož bázi je vystavěna architektura, kterou se tato práce zabývá, konkrétně jde o architekturu využívající komparátor ve zpětné vazbě namísto analogově-digitálního převodníku.

Tato práce je zaměřena na vývoj a evaluaci hardwaru využívající komparátor ve zpětné vazbě. Na základě navrhované architektury je vyvinut akviziční modul, jehož vybrané vlastnosti jsou ověřeny simulacemi a následně jsou vybrány komponenty pro jeho realizaci. Je zde představen návrh čtyřvrstvé desky plošného spoje, jenž je následně vyrobena a osazena. Na základě potřeb pro evaluaci architektury s využitím navrhovaného modulu je vyvinut firmware umožňující nastavení všech komponent, vysílání a příjem signálů a zachycení okamžiků času hrany na výstupu komparátoru.

Získaná data jsou zpracována v prostředí MATLAB a na jejich základě je provedeno zhodnocení navrhované architektury ve smyslu budoucího využití v reálných systémech digitálního předzkreslování signálu. Kromě prezentace výsledků jsou zde taktéž předvedena možná rozšíření systému v ohledech dosažení vyšší přesnosti nebo komfortu měření.

DECLARATION

I declare that I have written the Master's Thesis titled "Adaptation of digital predistorter to linearize amplifiers using comparator" independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the thesis and listed in the comprehensive bibliography at the end of the thesis.

As the author I furthermore declare that, with respect to the creation of this Master's Thesis, I have not infringed any copyright or violated anyone's personal and/or ownership rights. In this context, I am fully aware of the consequences of breaking Regulation § 11 of the Copyright Act No. 121/2000 Coll. of the Czech Republic, as amended, and of any breach of rights related to intellectual property or introduced within amendments to relevant Acts such as the Intellectual Property Act or the Criminal Code, Act No. 40/2009 Coll., Section 2, Head VI, Part 4.

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Introduction

The evolution process as a part of the everyday life of mankind has influenced wireless communications development as well in a manner of the most powerful solution researching. Although the 5G NR (New Radio) has not been fully deployed yet, the 6G technology research has already started. Every piece of this technology is always facing the demands on the efficiency and the overall overheads, therefore suitable methods for the best performance achieving have to be invented.

An essential part of the current wireless systems is a PA (Power Amplifier) enabling to transmit the RF (Radio Frequency) signal of the sufficient power through the environment. Nevertheless, this transmission is always confronted with a nonlinear characteristic of the PA. The issue coming up is a signal distortion and an amplifier efficiency. Even though the PA can work at a high-efficiency region of the characteristics, the significant distortion has to be taken into account. Vice versa, if the PA works in the high-linear region, it suffers from the poor efficiency. In order to deal with these facts, the DPD (Digital Predistortion) technique appears as a promising trade-off enhancing the overall efficiency which is very substantial for the IoT (Internet of Things) or 5G systems where a large number of devices is going to be expected.

This master's thesis is focused on the hardware evaluating implementation of a comparator in the feedback path of DPD systems. The evaluated architecture consists of an FPGA (Field Programmable Gate Array) module, a DAC (Digital-to-Analog converter) module and an acquisition module. The acquisition module is the main objective of the development. It is well designed, manufactured, tested, and prepared for further work. An appropriate firmware is developed to complete the proposed design and to acquire required data for the the overall assessment of the architecture for deployment in the DPD systems.

This work is divided into seven main parts. The first part is devoted to the PA imperfections, the second part refers to the PA linearization techniques. The third part handles information about DPD architectures. The fourth chapter introduces DPD architectures implementing comparator in the feedback path. The subsequent part contains the elements of the design process of hardware and firmware implementation. The sixth part presents hardware evaluation and outcomes discussion and finally, the last one is about future extensions.

1 Power Amplifier Imperfections

Ideal PA could be described as a memoryless device with a linear relationship between the input and output power which represents its constant gain G. However, a real PA suffers from several imperfections. As it is shown in Fig. 1.1, the output power of the real PA is not rising any more at a certain moment. This part is called saturation denoted by saturation power P_{Sat}. Even before the output signal reaches the saturation level, there is a point called 1 dB compression point (denoted by P_{1dB}) which indicates the moment when the output power varies from the input and the difference is just exactly 1 dB [1, 2, 3].

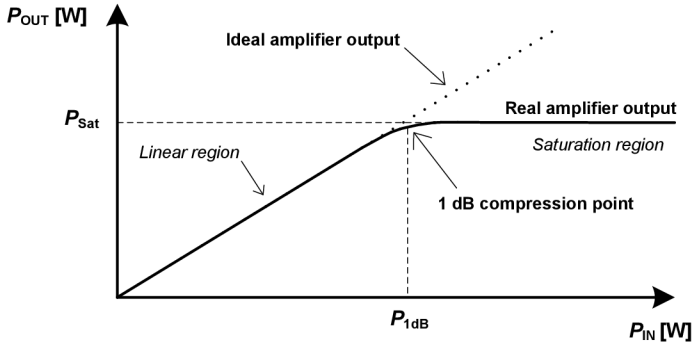


Fig. 1.1: Ideal and real PA characteristic.

In case the input signal exceeds the saturation level, the output is clipped in the saturation region which results in signal distortion and in the spectral re-growth causing out-of-band emissions in the adjacent frequency channels. On the other hand, there is another issue closely related to the mentioned one above and that is the power efficiency. PAs work the most efficiently when the input power levels are very close to the saturation. However, this requirement works in an antagonistic way alongside preservation of a linear behavior. Considering these two facts, designers have to make an appropriate trade-off depending on the system conditions. In general, power efficiency is not that critical at the base stations where the supply network is still connected, however, there are other aspects such as the power dissipation and overall size too [2, 4].

Power savings requirements are highly demanding at the UE (User Equipment) where the efficiency is playing a great role, regarding the total overheads while limited resources could be deployed. In the current communication systems, especially in the mobile cellular network, there is a high demand on the spectral efficiency which is enabled by implementing the high order modulation rates (e.g. up to 256-QAM (Quadrature Amplitude Modulation)). These new modulation schemes puts increased requirements on the output signal linearity as well [5, 6].

In LTE (Long Term Evolution) mobile systems, OFDM (Orthogonal Frequency Division Multiplexing) signals suffering from high PAPR (Peak-to-Average Power Ratio) are widely deployed. The high PAPR is a result of the subcarriers components combining. Comparing the real PA characteristics and the OFDM signal, it is obvious that the mean power is located in the linear region of the amplifier, but the amplitude peaks could reach the compression region, and therefore implicate the output signal distortion. There are several methods how to extend the linear region of the PAs. One of the opportunities is deploying the DPD. It is a cost-effective method, reducing the distortion while preserving satisfactory efficiency [4].

Apart from those phenomena, there is a memory effect which means that the output of the amplifier depends on the past values as well as on the current ones. In general, it could be observed in the case of wideband signal processing with high power amplifiers usage. There are two main memory effect categories i.e. long and short term memory effects. Long term memory effects are mainly caused by thermal constants and temperature changing, causing the parameter variation of the semiconductor parts in particular. Short term memory effects are assigned to the impedance changes when maintaining the wideband signals, and thereby varying the time constants e.g. in bias networks [7].

For PA behavior comprehension, it could be suitable to use AM/AM (Amplitude to Amplitude) and AM/PM (Amplitude to Phase) conversion characteristics. AM/AM describes the relationship between the input and output power where we can observe the effect of the non-linearities and the memory of the PA as well. A not least important characteristic is the AM/PM where the phase distortion dependent on the input power could be seen [2]. Fig. 1.2 shows the AM/AM and AM/PM example characteristics of the PA ADL5610.

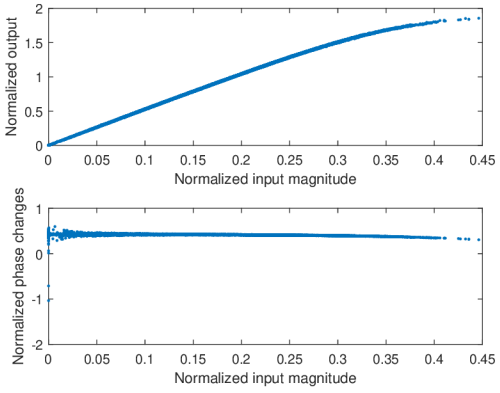


Fig. 1.2: Normalized AM/AM and AM/PM example characteristics of the PA ADL5610.

2 Linearization Techniques

There are several methods for the extension of the PA linear region. Although, the main aim of this work is to focus on the DPD technique, for completeness we shortly explain and discuss the other existing linearization methods.

2.1 Feedforward Linearization

Feedforward linearization architecture (depicted in Fig. 2.1 below) is consisting of the main PA and an error amplifier. Splitting the input signal enables to obtain a difference between the amplifier output and the original input. Subsequently, the signal is amplified via an error amplifier and coupled to the output of the PA. This results in the suppression of the undesired distortion components in the transmitter output. Both the subtractor input and the PA output are equipped with a time delay blocks to ensure the right time synchronization.

The main advantage of this linearization technique is that the entire system can work with large bandwidths without any stability problems. Concerning that fact, new problems arise with the parameters changes of the matching network over the wide bandwidth and additionally, aging of the components should be taken into account as well. Furthermore, the error amplifier should be also adequately linear in the region of its operation in the low power stage [2, 5].

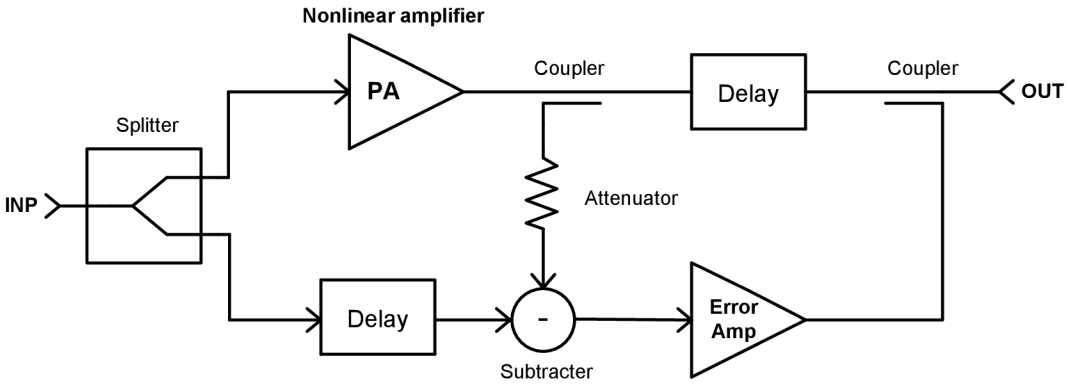


Fig. 2.1: Feedforward linearization scheme.

2.2 Feedback Linearization

Feedback implementation shown in Fig. 2.2 is the simplest method how to realize the PA linearization. The output signal is taken as a feedback, then it is attenuated and subtracted from the input signal. Obviously, this method creates a straightforward way of distortion suppression with the deployment of the minimum components. Naturally, between the input and the feedback is a certain delay caused by finite signal propagation speed. The system stability is constrained by the signal bandwidth and operation with wideband signals is limited by the system causality. Therefore, feedback systems are suitable only for narrowband signals [3].

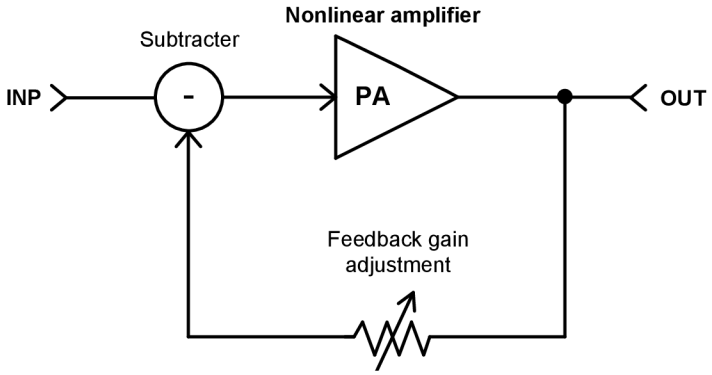


Fig. 2.2: Feedback linearization scheme.

2.3 Signal Predistortion

The predistortion technique could be used for PA linearization as well. The principle is hidden in the known PA output characteristic combined with its inverse which results in the overall linear characteristics (shown in Fig. 2.3). Often, predistortion techniques are based on the DSP (Digital Signal Processing) blocks, however, they could be implemented by the analog circuits too. The digital realizations are more stable and adaptable, moreover, they mitigate the number of discrete components which are often expensive and space-consuming [1].

We can classify the predistortion systems based on their adaptability into groups of adaptive and non-adaptive systems. The difference indicates that non-adaptive parts could work just with the certain PA unlike the adaptive systems which adjust their coefficients according to the actual PA characteristics [2].

Another classification of the predistortion systems can be made according to their implementation in RF, IF (Intermediate Frequency) or a baseband. In the case of

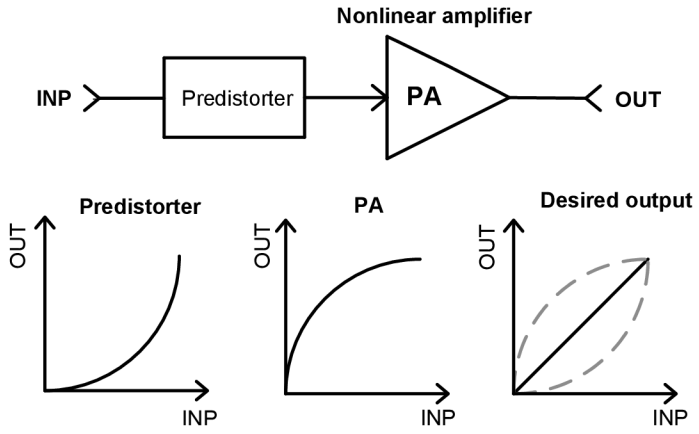


Fig. 2.3: Signal predistortion principle.

RF or IF predistortion, the requirements which the system should fulfil are almost the same. The predistorter has to process high frequencies depending on the system architecture. The RF or IF predistorter implementation could be achieved by the analog circuits, but the desired shape of the output characteristic is limited and the circuitry is often frequency-dependent due to wideband signals and these types of predistorters are often non-adaptible. Combining these facts makes the analog RF predistortes not suitable for the most nowadays communication systems[1, 3].

The baseband predistorter operates with the signal before the up-converting into the IF or RF band. The most effective way of predistorer realization appears as the digital implementation frequently performed in the DSP blocks (such as in FPGA, processor, etc.). The conventional DPD predistorter (with the block diagram depicted in Fig. 2.4) implements the DACs (Digital-to-Analog converter) and ADCs (Analog-to-Digital Converter) in the forward or the feedback path respectively. The output of DAC is up-converted, passed through the PA and down-converted. The greatest advantage of DPD is its flexibility.

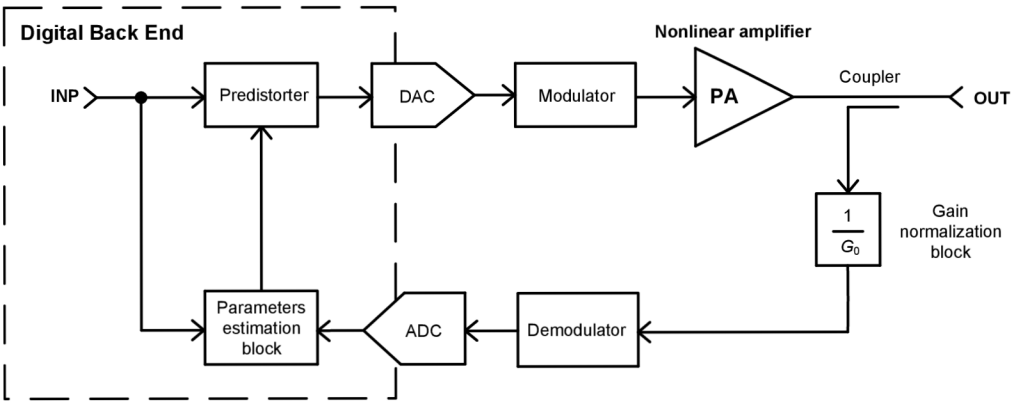


Fig. 2.4: Baseband predistortion scheme.

An example linearization results obtained by a predistorter are shown in Fig. 2.5, where the PSD (Power Spectral Density) of the original (input) signal, linearized output and trace without DPD is depicted in. Concerning the linearized output, it is obvious that the power spread out into the adjacent channels is significantly suppressed comparing to the output without the DPD, consequently, a highly improved ACPR (Adjacent Channel Power Ratio) is achieved [1, 2].

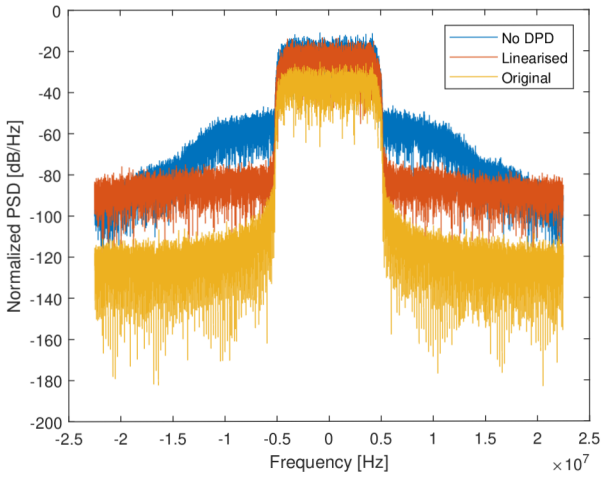


Fig. 2.5: Normalized PSD output of ILA operating with PA ADL5610.

2.4 Signal Postdistortion

Postdistortion of the signal can be implemented in the same manner as the predistortion but the processing block is located right after the PA. The main drawback of the postdistortion is coming up with its position and that is the high power which should be operating with. Sometimes it is not suitable or simply not possible and thus, these situations could be improved with an adequate postdistorter placed on the input of the receiver. The power level at the receiver plane is not that high in this case and moreover, it can improve the imperfections of the channel. On the other hand, the complexity of the receiver is growing up and the spectral regrowth caused by the PA on the transmitter side is not compensated [2, 3].

3 DPD Architectures

The DPD architectures ensure the coefficients extraction along with the parameter estimation based on the PA model. There are two main approaches in terms of calculating the new coefficient, i.e. DLA (Direct Learning Architecture) and ILA (Indirect Learning Architecture).

3.1 Direct Learning Architecture

Direct Learning architecture of the DPD system is depicted in Fig. 3.1. Output of the PA denoted by $y(t)$ is normalized which means that output power is attenuated according to the PA chosen gain G_0. The purpose of the parameter estimation block is to minimize the error $e(t)$ between the desired input $z(t)$ and the normalized PA output. Accordingly to the error signal, the predistorter coefficients are calculated. A slow convergence time and possible complexity of the estimation block belong to the main disadvantages of DLA implementation [2, 5].

Mathematically, the situation could be explained as

$$e(t) = z(t) - y(t), \tag{3.1}$$

where $y(t)$ is the normalized output. The ideal state of the DPD system occurs when

$$z(t) = y(t), \tag{3.2}$$

and thus it means that $y(t)$ has to be equal to

$$y(t) = \frac{A(F_{\text{pre}}(z(t)))}{G_0} = z(t), \tag{3.3}$$

where A is the transfer function of the PA, and $F_{\text{pre}}(z(t))$ is the predistorter transfer function. Finally, we can establish the function of the predistorter $F_{\text{pre}}(z)$ [2]

$$F_{\text{pre}}(z) = A^{-1}(G_0 z). \tag{3.4}$$

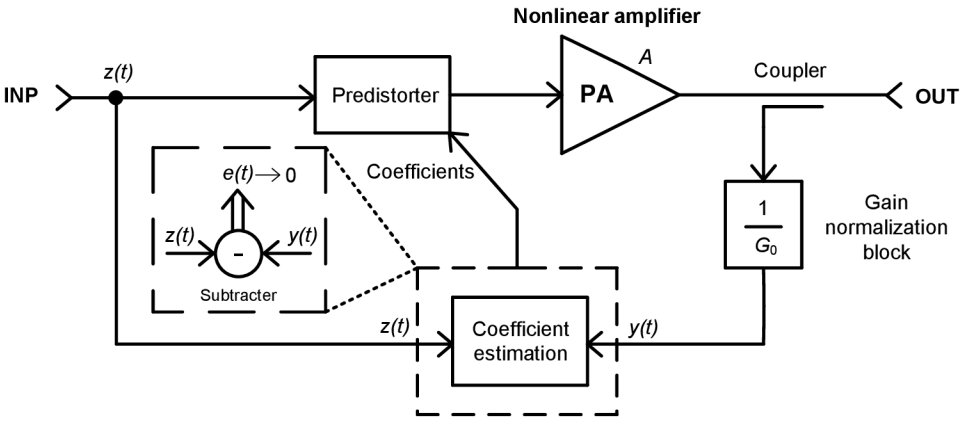


Fig. 3.1: Direct learning architecture scheme.

3.2 Indirect Learning Architecture

Indirect learning architecture (shown in Fig. 3.2) makes another possibility how to calculate the new DPD coefficients. The main difference between ILA and DLA is that ILA operates with postdistorter in the feedback path. The postidistorter collects the PA output samples, and subsequently calculates the post-inverse characteristic coefficients. Finally, the predistorter in the forward path is initialized by the postdistorter coefficients [3].

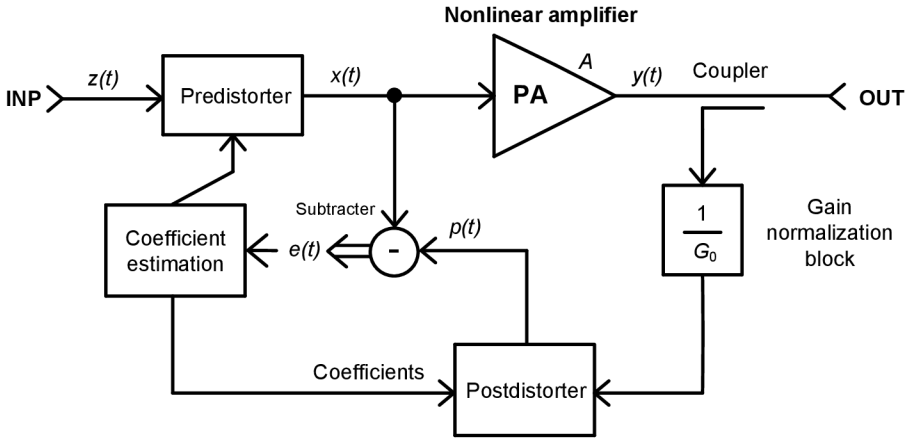


Fig. 3.2: Indirect learning architecture scheme.

The principle of the ILA is based on the minimization of the error function between the predistorted PA input $x(t)$ and the postdistorted signal $p(t)$

$$e(t) = x(t) - p(t), \tag{3.5}$$

where $x(t)$ equals to

$$x(t) = F_{\text{pre}}(z(t)), \tag{3.6}$$

and $p(t)$ equals to

$$p(t) = F_{\text{post}}\left(\frac{y(t)}{G_0}\right), \tag{3.7}$$

where F_{post} denotes the postdistortion function and $y(t)$ is the PA output.

In the ideal situation, the predistortion and postdistortion function should be equal

$$F_{\text{pre}}(z(t)) = F_{\text{post}}\left(\frac{y(t)}{G_0}\right), \tag{3.8}$$

but the model preparation and the final parameter estimation process is suffering from certain inaccuracies, therefore, the predistortion function is just closely approaching the desired output [5].

4 DPD Architectures Implementing Comparators

The conventional baseband DPD architectures operate with ADCs in the feedback paths, however, these ADCs could become the main bottleneck of the current developing systems which require high data rates and consequently the wide bandwidths. For example, in 3GPP (3rd Generation Partnership Project) Release 15 (i.e. 5G NR) the maximum frequency bandwidth is specified up to 400 MHz in the range FR2 [9]. Operating with a high resolution ADC (e.g. 14-bit and more) and the high sampling rate is very difficult in terms of the design feasibility. The required ADCs are often very expensive or hardly available. Another disadvantage of the conventional ADCs is the power consumption which is increasing with the sampling rate. Possible approach to prevent these issues is to use comparator instead of ADC in the feedback path [10].

4.1 1-bit ADC Predistortion Architecture

The proposed DPD architecture in [10] contains two comparators in the feedback path. In principle, it means that the expensive high resolution ADC is replaced with a 1-bit ADC represented by a comparator. The entire architecture is depicted in Fig. 4.1. The feedback signal after the gain normalization is connected to the input of the comparators where it is compared with an auxiliary signal produced by another DAC in the feedback. Finally, the sign of the difference between the feedback signal and the forward model is obtained. This situation is explained in the equation below

$$\mathbf{s} = sign(\boldsymbol{y} - \hat{\boldsymbol{y}}), \tag{4.1}$$

where $\mathbf{s}$ is the sign vector, $\boldsymbol{y}$ denotes the feedback signal, $\hat{\boldsymbol{y}}$ is the forward model output, and finally $sign$ is the function which separately calculates the sign of real and imaginary part of the signals. Afterwards, the DPD coefficients are extracted on the basis of the obtained signs, therefore, the feedback signal restoration can be omitted [10].

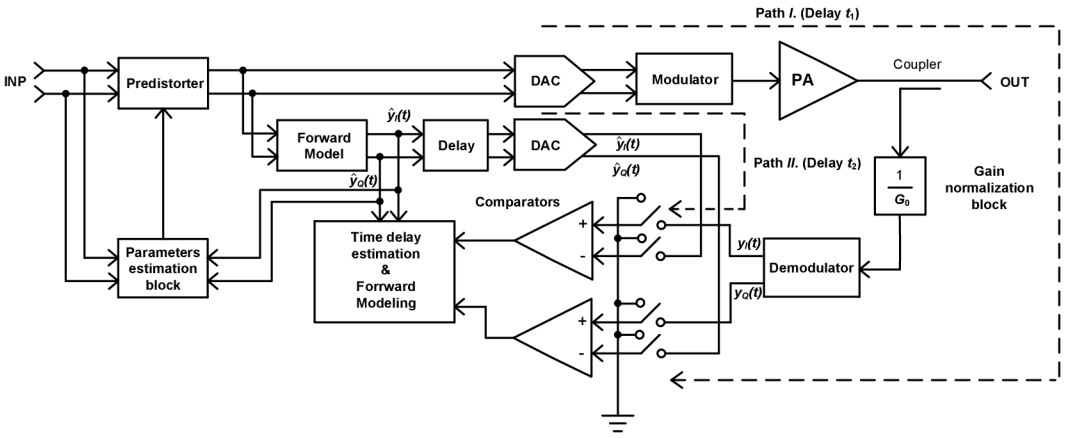


Fig. 4.1: Architecture scheme implementing 1-bit ADC.

The entire predistortion process and coefficients estimation is based on two main stages, i.e. a time delay estimation and a forward modelling. Basically, the forward model coefficients are calculated based on the sign of the erorr signal at the comparator output. At first, the time delays on the signal paths are to be measured. The first delay denoted by t_1 represents the delay between the main DAC and the comparators including the PA. The second delay t_2 is the delay of the path between the auxiliary DAC and the comparators. The difference between these two delays is compensated by the delay block, therefore, the time samples can be aligned appropriately. Another issue is the power alignment, which means that the signals before reaching the comparators have to have the equivalent levels. In this way could be really beneficial to use e.g. VGA (Variable Gain Amplifier) or integrated circuit solution to maintain an appropriate level [10, 11].

Wang et al. are proposing in [11] another kind of this predistortion architecture, in principal very similar to one above. For the delay estimation, it is not possible to use time domain based cross correlation of the signal because the architecture operates just with signs of the output signal. Therefore, the frequency domain algorithm is designed utilizing the discrete Fourier transform. The main disadvantage of this procedure is a necessity of the apriory knowledge of the PA properties. In [10] Wang proposed another way how to deal with this issue and how to avoid the whole step size calculation procedure. A new loss function is therefore proposed, and the DPD model can be calculated deploying an optimizing algorithm. The DPD coefficients are subsequently extracted on the basis of the solution. The main advantage of this architecture compared to [11] is the fast convergence ensured by the loss function employment. On the other hand, both architectures [10] and [11] use additional DAC which could be disadvantageous in certain designs regarding the power consumption and the total overheads.

4.2 Proposed Architecture Implementing Comparator

In Fig. 4.2 the proposed architecture of the DPD system implementing comparator and the LSDAC (Low Speed Digital-to-Analog Converter) in the feedback path is shown. At the beginning, baseband digital signal is converted to the analog domain and IQ branches are up-converted to desired carrier. Mixed signal continuous through the PA, and finally, its certain portion is coupled back into the feedback path. The feedback signal is down-converted and passed to the comparator input along with the signal from the LSDAC of a set voltage level. Subsequently, the signals are compared and the time instants of the signal edges on the comparator output are acquired. In the end, the DPD coefficients are derived from these instants.

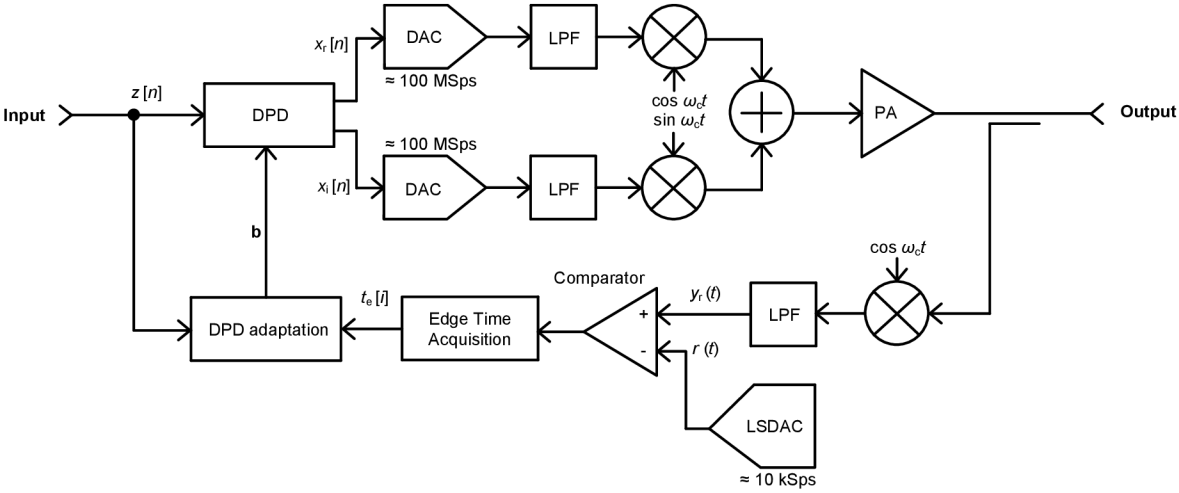


Fig. 4.2: Architecture scheme implementing comparator.

Mathematically, the main idea of the entire process could be explained as follows

$$y_{\mathrm{r}}(t_{\mathrm{e}}[i]) = r(t_{\mathrm{e}}[i]), \tag{4.2}$$

where y_{r} is the input signal of the comparator, r denotes the voltage level generated by the LSDAC and $t_{\mathrm{e}}[i]$ are time instants when the edges at the comparator output occured. The capability of calculating the DPD coefficients is hidden in the known time moments when the signal is equal to the set value r. Considering the DPD is modeled by the memory polynomial, the baseband PA input $x[n]$ could be described as [12]

$$x[n] = \sum_{k=1}^{K} \sum_{q=0}^{Q} b_{\mathrm{k-1,q}} z[n-q]|z[n-q]|^{k-1}, \tag{4.3}$$

where n is the sample index, $z[n]$ is the desired scaled PA output sample, $b_{\mathrm{k-1,q}}$ denotes the DPD model coefficients, K is the order of the model nonlinearity, finally, Q describes the memory length. In the time domain, (4.3) can be defined as

$$x(t) = \sum_{k=1}^{K} \sum_{q=0}^{Q} b_{\mathrm{k-1,q}} z(n - qT)|z(n - qT)|^{k-1}, \tag{4.4}$$

where T is the sampling period. Sampling the signal $x(t)$ at the certain time instants can result in the matrix form of N equations where N depends on the amount of the samples. This can be written as

$$\mathbf{x} = \mathbf{U}\mathbf{b}, \tag{4.5}$$

where $\mathbf{b}$ is the coefficients vector of $b_{\mathrm{k-1,q}}$ and the memory polynomial kernels are described by matrix $\mathbf{U}$. In the full form the matrix could be prescribed as

$$\begin{bmatrix} x(t_1) \\ x(t_2) \\ \vdots \\ x(t_N) \end{bmatrix} = \begin{bmatrix} z(t_1) & \dots & z(t_1)\,|z(t_1)| & z(t_1 - T)\,|z(t_1 - T)| & \dots & z(t_1 - QT)\,|z(t_1 - QT)|^{K-1} \\ z(t_2) & \dots & z(t_2)\,|z(t_2)| & z(t_2 - T)\,|z(t_2 - T)| & \dots & z(t_2 - QT)\,|z(t_2 - QT)|^{K-1} \\ \vdots & \ddots & \vdots & \vdots & \dots & \vdots \\ z(t_N) & \dots & z(t_N)\,|z(t_N)| & z(t_N - T)\,|z(t_N - T)| & \dots & z(t_N - QT)\,|z(t_N - QT)|^{K-1} \end{bmatrix} \begin{bmatrix} b_{1,0} \\ \vdots \\ b_{2,0} \\ b_{2,1} \\ \vdots \\ b_{K,Q} \end{bmatrix}. \tag{4.6}$$

Deploying the damped Newton's method, the $\mathbf{b}$ coefficient can be solved iteratively, and thus

$$\mathbf{b}[m+1] = \mathbf{b}[m] - \mu\mathbf{e}[m], \tag{4.7}$$

where m denotes the number of iterations, μ is the step size of the iteration and $\mathbf{b}[m]$ along with $\mathbf{b}[m+1]$ characterize the former and updated DPD coefficients respectively. The vector $\mathbf{e}$ contains the coefficient errors. It is given as the least-square solution of

$$\Delta = \mathbf{U}\mathbf{e}, \tag{4.8}$$

where vector Δ is defined as

$$\Delta = \mathbf{z} - \mathbf{y}. \tag{4.9}$$

Vector $\mathbf{z}$ denotes the desired output and vector $\mathbf{y}$ the measured output of the PA. This proposed architecture requires just one comparator in the feedback path, because it processes only one of the IQ signals. Nevertheless, it can be established either with the in-phase or quadrature branch. For further mathematical expression of the problem, we use complex baseband signal, and subsequently we split Δ into the real and imaginary part as follows

$$\boldsymbol{\Delta}_{\mathrm{r}} + j\boldsymbol{\Delta}_{\mathrm{i}} = (\mathbf{U}_{\mathrm{r}} + j\mathbf{U}_{\mathrm{i}})(\mathbf{e}_{\mathrm{r}} + j\mathbf{e}_{\mathrm{i}}). \tag{4.10}$$

In accordance to the in-phase and the quadrature output of IQ mixer in the feedback path, we can consider the following representation of the split least-square solution ($\mathbf{\Delta}_\mathrm{r}$ for in-phase and $\mathbf{\Delta}_\mathrm{i}$ for quadrature)

$$\mathbf{\Delta}_\mathrm{r} = \begin{bmatrix}\mathbf{U}_\mathrm{r} & -\mathbf{U}_\mathrm{i}\end{bmatrix} \begin{bmatrix}\mathbf{e}_\mathrm{r} \\ \mathbf{e}_\mathrm{i}\end{bmatrix}, \tag{4.11}$$

$$\mathbf{\Delta}_\mathrm{i} = \begin{bmatrix}\mathbf{U}_\mathrm{i} & +\mathbf{U}_\mathrm{r}\end{bmatrix} \begin{bmatrix}\mathbf{e}_\mathrm{r} \\ \mathbf{e}_\mathrm{i}\end{bmatrix}. \tag{4.12}$$

By establishing the substitutions $\mathbf{A} = \begin{bmatrix}\mathbf{U}_\mathrm{r} & -\mathbf{U}_\mathrm{i}\end{bmatrix}$ and $\mathbf{B} = \begin{bmatrix}\mathbf{U}_\mathrm{i} & +\mathbf{U}_\mathrm{r}\end{bmatrix}$, the error vector $\mathbf{e}$ can be determined for the in-phase branch as

$$\begin{bmatrix}\mathbf{e}_\mathrm{r} \\ \mathbf{e}_\mathrm{i}\end{bmatrix} = (\mathbf{A}^\mathrm{H}\mathbf{A})^{-1}\mathbf{A}^\mathrm{H}\mathbf{\Delta}_\mathrm{i}, \tag{4.13}$$

and for the quadrature branch as

$$\begin{bmatrix}\mathbf{e}_\mathrm{r} \\ \mathbf{e}_\mathrm{i}\end{bmatrix} = (\mathbf{B}^\mathrm{H}\mathbf{B})^{-1}\mathbf{B}^\mathrm{H}\mathbf{\Delta}_\mathrm{i}, \tag{4.14}$$

where $\mathbf{A}^\mathrm{H}$ and $\mathbf{B}^\mathrm{H}$ denotes the Hermitian transpose of matrices $\mathbf{A}$ and $\mathbf{B}$ respectively. In the next step, vector $\mathbf{y}$ of the feedback baseband signal, $\mathbf{z}$ of the input baseband signal and $\mathbf{r}$ of the set voltage levels has to be declared as follows:

$$\mathbf{y} = [y(t_1) \quad y(t_2) \quad \dots \quad y(t_\mathrm{N})]^\mathrm{T}, \tag{4.15}$$

$$\mathbf{z} = [z(t_1) \quad z(t_2) \quad \dots \quad z(t_\mathrm{N})]^\mathrm{T}, \tag{4.16}$$

$$\mathbf{r} = [r(t_1) \quad r(t_2) \quad \dots \quad r(t_\mathrm{N})]^\mathrm{T}, \tag{4.17}$$

where t_i equals to the time instants $t_\mathrm{e}[i]$. In the end, we can obtain the final DLA equation by substituting (4.13) into (4.7) which leads to

$$\begin{bmatrix}\mathbf{b}_\mathrm{r}[m+1] \\ \mathbf{b}_\mathrm{i}[m+1]\end{bmatrix} = \begin{bmatrix}\mathbf{b}_\mathrm{r}[m] \\ \mathbf{b}_\mathrm{i}[m]\end{bmatrix} - \mu(\mathbf{A}^\mathrm{H}\mathbf{A})^{-1}\mathbf{A}^\mathrm{H}\mathbf{\Delta}_\mathrm{i}(\mathbf{z}_\mathrm{r} - \mathbf{r}). \tag{4.18}$$

One of the most essential parts of the architecture is the edge time acquisition circuit (depicted in Fig. 4.3). Assembling two D flip-flops creates the desired function of the edge time detector but note that at the input of the first one there is a delay block ensuring an appropriate difference of the signal time arrival between the flip-flop inputs. The input signal is captured at the positive edge of the clock signal and sent into the FPGA module afterwards. Once the edge of the observed signal

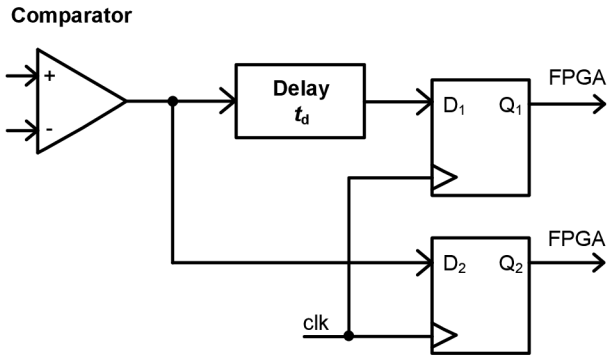


Fig. 4.3: Edge time acquisition circuit.

comes, it results in unequal states of the D flip-flop outputs which can be detected in the FPGA.

Referring to the architecture scheme depicted in Fig. 4.2, it is obvious that there is no need for the ADC which is a great advantage. The only fundamental parts are the LSDAC and comparator which appear as the inexpensive items on a budget. The less complexity could give rise to the deployment of the proposed design in future applications.

4.2.1 Simulation of the Edge Time Acquisition Circuit

For the simulation purposes, we selected the edge time acquisition circuit together with the comparator. Although the final architecture should operate up to 500 MHz clock signal frequency, it was not possible to find suitable behavioral models for the simulation. In terms of the best performance, the chosen models are just approaching the desired properties of the final deployed parts. Consequently, the chosen comparator is TLV3501 and the D flip-flop is SN74LVC74A in dual package (both models are available at [13]). Capability of the clock signal operation is limited to 100 MHz and the maximum input signal frequency of the comparator is 80 MHz. The entire circuit was simulated in OrCAD PSpice.

The simulation settings were adjusted as follows: power supply voltage was set to 3.3 V, signal at the non-inverting input of the comparator was a sine wave of the frequency 10 MHz and at the inverting input there was the reference signal of the constant voltage level 1.35 V. One of the D flip-flops was connected directly to the comparator output and the another one was attached to 50 Ω transmission line which produced the desired delay $t_\mathrm{d} = 6$ ns. Finally, the 100-MHz clock signal was used.

Results of the simulation can be seen in Fig. 4.4. Exceeding of the reference voltage level of the input sine wave signal causes the stimuli at the D flip-flop inputs where we can see the evident time delay between them. These events are acquired by the clock edge, and transferred to the output. In the lower plot of Fig. 4.4 there are the output signals of D flip-flops which are sent to the FPGA to obtain the particular edge time instants.

Unfortunately, the available models do not achieve the desired performance in terms of the timing properties, however, we expect almost the same behavior when the high-speed components are deployed.

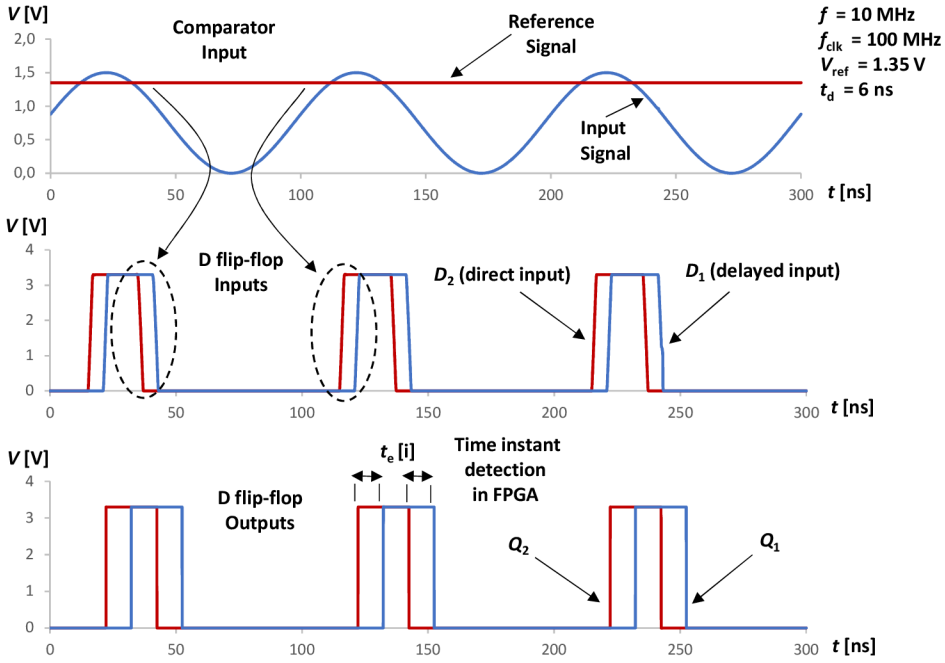
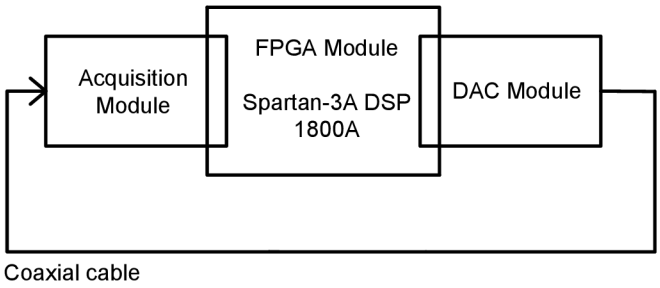


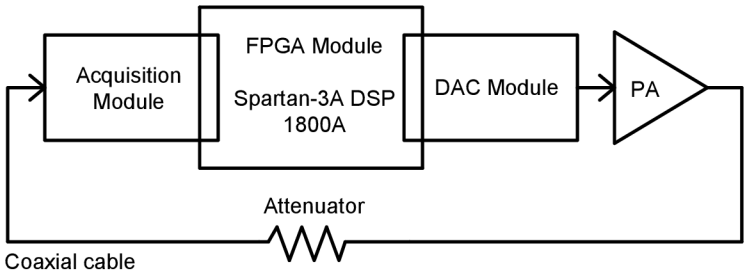
Fig. 4.4: Simulation of the edge time acquisition block.

5 Architecture Design

For implementing the DPD with the comparator in the feedback, we propose an architecture depicted in 5.1a consisting of FPGA module, DAC module and acquisition module. In order to ensure less complexity and to maintain high performance, we decided to use existing platforms as a supporting units, i.e. the FPGA module Spartan-3A DSP 1800A [14] and the DAC module AES-HSDAC-EXP-PCB-C by Avnet (operating with DAC5682z [15]) providing 16-bit DAC and IQ Modulator. The developed module is the acquisition module with the comparator.



(a) Concept for testing purposes.



(b) Concept for deployment in real DPD system.

Fig. 5.1: Concepts of the proposed architecture.

The core component of the proposed architecture is the FPGA module where the IQ signal samples are stored in a memory and sent to the DAC module. Subsequently, the signal is up-converted and continuous through the PA and attenuator to the input of the acquisition module. In the case of testing mode, these components are bypassed. The acquisition module consists of down-convertor and the baseband processing section implementing the comparator. The obtained output signals follow back into the FPGA, finally, the processed data are sent to PC (Personal Computer) for subsequent evaluation in MATLAB.

The proposed hardware serves as a proof of concept of the above described DPD architecture with a comparator and the results will be used for overall hardware

assessment focused on an entire error and behaviour observation. Thus, the main objective is to verify that a method implementing comparator is capable to acquire several time instants suitable for DPD realization. For subsequent evaluation, we proposed the full testing chain, depicted in Fig. 5.1b, deploying the PA and an attenuator on the signal path which introduces the real usage in DPD systems.

5.1 Hardware Design

We aimed at developing a hardware which would work with various input signal bandwidths, clock signal frequencies up to 500 MHz, carrier frequencies up to 1600 MHz, and adjustable delays between the flip-flop inputs. In accordance to these criteria, a selection of the final components was made. Another important concern is the cooperation of all modules, therefore, the overall compliance is necessary, mostly in case of data and analog signal transmission.

5.1.1 IQ Demodulator

The first part of the acquisition module is the IQ Demodulator (can be seen in Fig. 5.2) which is down-converting the RF signal to the baseband. The chosen one is TRF371125 covering the frequency range from 0.7 to 4.0 GHz [16]. Apart from the mixer itself, this component is equipped with adjustable low pass filter, PGA (Programmable Gain Amplifier) and DC offset control which creates a great possibility to use the output baseband signal directly without any additional components. All analog signal inputs and outputs are operated deferentially, therefore, the RF baluns are necessary to transform the single-ended signals into differential. The RF inputs are equipped with ADTL2-18 transformers (frequency range 30-1800 MHz [17]) and at the baseband outputs with ADT2-1T+ (frequency range 0.4-450 MHz [18]). The mixer inputs and outputs have to be connected correctly to the neighbouring circuits using the coupling capacitors.

The control registers are programmed via the SPI (Serial Peripheral Interface) from the FPGA module. We adjust an internal oscillator frequency (900 kHz) for DC offset calibration procedure, a corner frequency of a low pass filter (4 MHz) and a baseband signal amplifier gain (0 dB). It is not necessary to amplify the baseband signal because the power loss on coaxial cables is negligible and the power level can be adapted on the LO (Local Oscillator) signal generator. A specific explanation of the initial setup is going to be present in the next section.

The mixer is supplied from +5 V branch, whereas the FPGA signals can reach the maximum voltage level +3.3 V. Therefore, the bi-directional voltage translator TXS0108E [19] was selected for the voltage-level translation.

Finally, there is an opportunity to setup the common-mode voltage of the output baseband signal which is provided by a simple voltage divider at the VCM (Common-Mode Voltage) input. Considering the mathematical explanation in the previous chapter, the system requires just one component of the IQ signal. In this case, it is the in-phase output BBI connected to an SMA (SubMiniature version A) connector and zero-ohm resistors for debugging purposes.

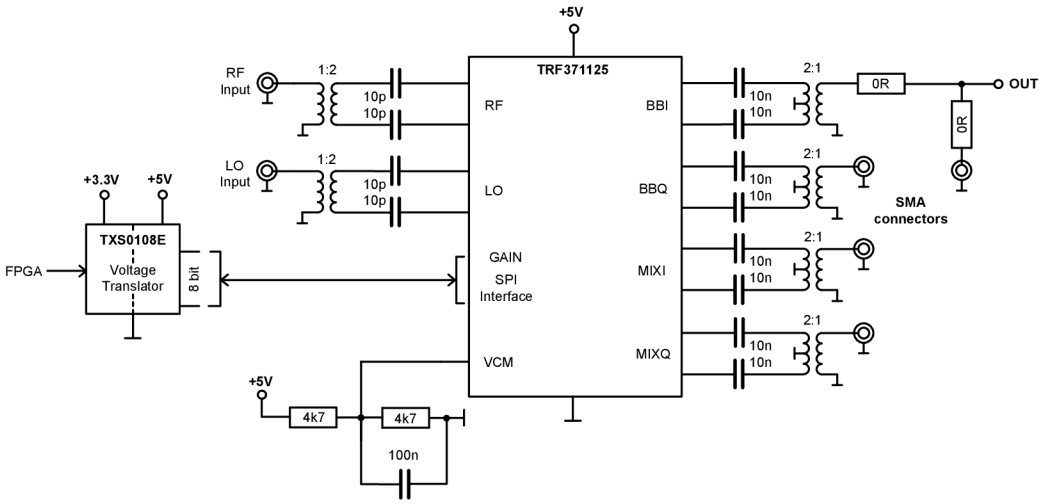


Fig. 5.2: IQ Mixer circuit.

5.1.2 Baseband Section

The next part included in the design is the baseband section shown in Fig. 5.3 below. The input signal is provided by the IQ Mixer baseband output and is terminated to the 50 Ω load which is defined by the voltage divider resistors. Additionally, the voltage divider sets the required common-mode voltage. The capacitor on the input is necessary due to an appropriate coupling between the baseband balun transformer and the comparator.

The most important part of this entire architecture is the comparator. The chosen one is ADCMP582 [20]. Its main characteristic is 200 fs random jitter enabling 10 Gbps operation. The comparator is supplied from ±5 V branches providing the possible input voltage range from -2 V to 3 V. A hysteresis value is set to 10 mV by an external 2 kΩ resistor whose value is determined in [20].

The comparator inverting input is connected to the LSDAC output with simple low pass filter ensuring to remove the possible undesired noise and glitches on the output of LSDAC operating with R-2R architecture. The filter cutoff frequency f_{LP} is set according to the settling time t_{s} of the LSDAC [21], i.e. 100 kHz and 1 μs

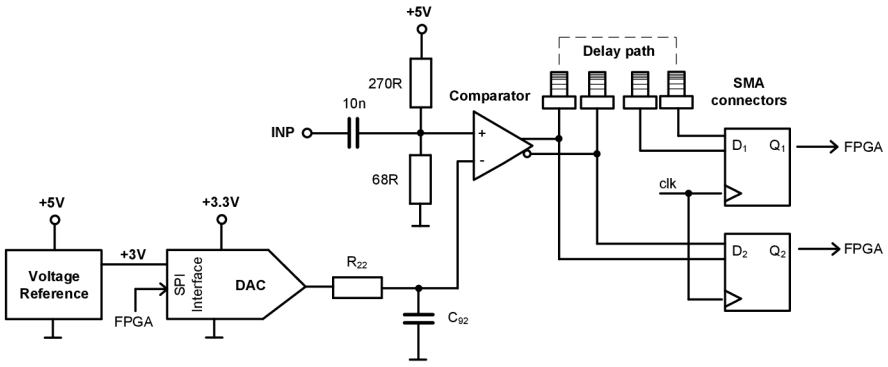


Fig. 5.3: Baseband stage of the architecture.

respectively. For chosen capacitor value $C_{92} = 1$ nF we can calculate a suitable resistor

$$R_{22} = \frac{1}{2\pi f_{\mathrm{LP}} C_{92}} = \frac{1}{2\pi \cdot 100 \cdot 10^3 \cdot 1 \cdot 10^{-9}} \approx 1.6\,\mathrm{k\Omega}. \tag{5.1}$$

Once the output voltage level of LSDAC is set by SPI interface, it is compared with the input signal. Inside the comparator, the output is driven by an LVPECL (Low-Voltage Positive Emitter-Coupled Logic) driver which sends impulses to the D flip-flops through the delay path created by coaxial cables and SMA connectors.

The D flip-flops NB7V52M are driven differentially and works with the clock frequency up to 10 GHz [22]. One advantage of NB7V52M is the termination resistors integrated on the chip which can be beneficial for the space savings on the PCB (Printed Circuit Board). Another great feature is the possibility to operate with different logic standards at the input, i.e. LVPECL, CML (Current Mode Logic) and LVDS (Low-Voltage Differential Signaling), but at the output there is just CML driver which has to be translated to LVDS using differential translator SN65LVDS100DGK [19] because the FPGA module is not able to work with CML.

5.1.3 Clock Jitter Cleaner

As the clock signal source we selected the integrated circuit LMK04133 [23]. It is a jitter cleaner and clock synchronizer, providing five dedicated signal outputs of different logic standards. The maximum added jitter produced by the internal VCO (Voltage Controlled Oscillator) is approx. 160 fs. The component architecture is based on a cascaded PLL (Phase-Locked Loop) where the input reference signal is synchronized to the VCXO (Voltage Controlled Crystal Oscillator), afterwards, it is synchronized again to the internal VCO. The simplified schematic diagram is depicted in Fig. 5.4. The high number of the outputs is necessary due to implementation of two D flip-flops and the DAC module together with the FPGA module.

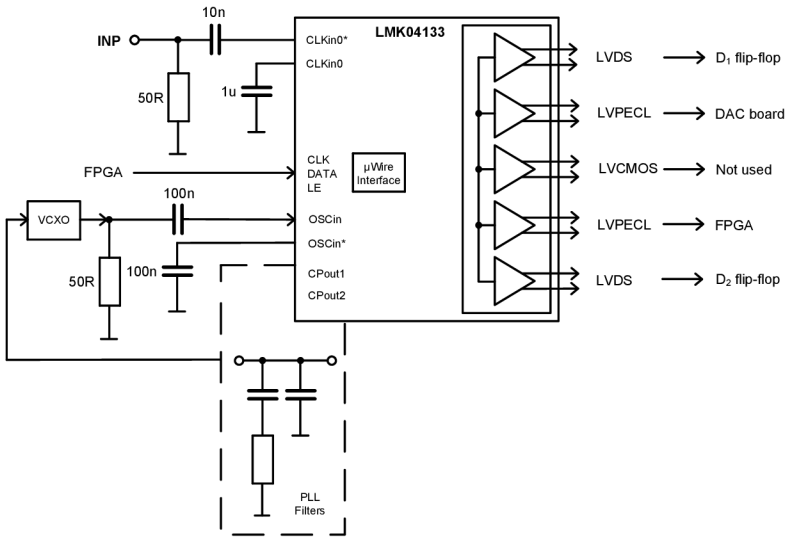


Fig. 5.4: Jitter cleaner circuit.

The single-ended input of a reference clock signal can be transformed into the differential easily using termination resistor and coupling capacitor. The non-inverting input is tied to the ground via capacitor whose value is recommended in [23] and the clock input capacitor value was selected with regards to the evaluation module user's guide [24]. The first PLL of the jitter cleaner is connected via charge pump output CPout1 to the loop filter and VCXO. The chosen crystal oscillator is CVHD-950 with its center frequency 122.88 MHz [25]. The VCXO output is terminated ideally by a 50-Ω resistor and coupled with a capacitor. Its value is recommended by [24]. The VCXO provides a single-ended output, thus, the non-inverting VCXO input of the jitter cleaner has to be tied to the ground with a capacitor.

The internal system setup is depicted in Fig. 5.5 where the divider values and any other essential properties can be found. The system is working with the input frequency 12.288 MHz produced by an external signal generator. R1 and N1 dividers are adjusted to operate the VCXO at its center frequency. The dividers of the second PLL circuit are set to provide an appropriate clock signal outputs. It is necessary to hold the frequency rate at the phase detector 2 as high as possible to ensure the low in-band phase noise from the reference input of the PLL2 circuit. The phase detector frequency at the PLL1 is not such critical because the filter bandwidth is much narrower. The output clock dividers are adjusted in order to get the clock for the D flip-flops of the frequency 122.88 MHz and the same frequency has to be delivered into the FPGA module. The DAC at the DAC module requires 491.52 MHz

clock signal frequency which is a quadrupled value of 122.88 MHz clock necessary for a DAC proper function. Our aim was to distribute the same clock logic standards to both D flip-flops to preserve equal conditions. Although the FPGA module is able to work with the LVPECL signal, there are no available termination resistors close to the chip, consequently, it was necessary to use differential translator [19].

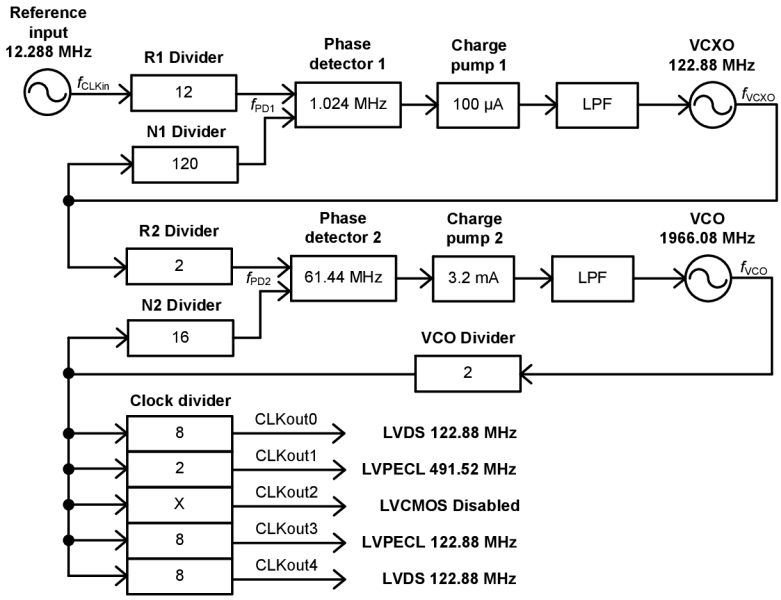


Fig. 5.5: Jitter cleaner setup block schematic.

The LMK04133 circuit has to be equipped with two PLL loop filters and the second filter consists of an external and internal part. The desired bandwidth of the first loop filter is supposed to be between 10 Hz - 200 Hz and in the case of the second one, the loop bandwidth should be more than 100 kHz according to [24]. Regarding these facts, the corresponding loop filters were designed using the Clock Design Tool [26].

The loop filter of the PLL1 circuit is depicted in Fig. 5.6a and the filter of the PLL2 is in Fig. 5.6b. The components of the PLL2 filter can be set by a register R13. Proposed filter properties were verified by simulation which results in frequency response characteristics depicted in Fig. 5.7 (for PLL1 filter) and in Fig. 5.8 (for PPL2 filter).

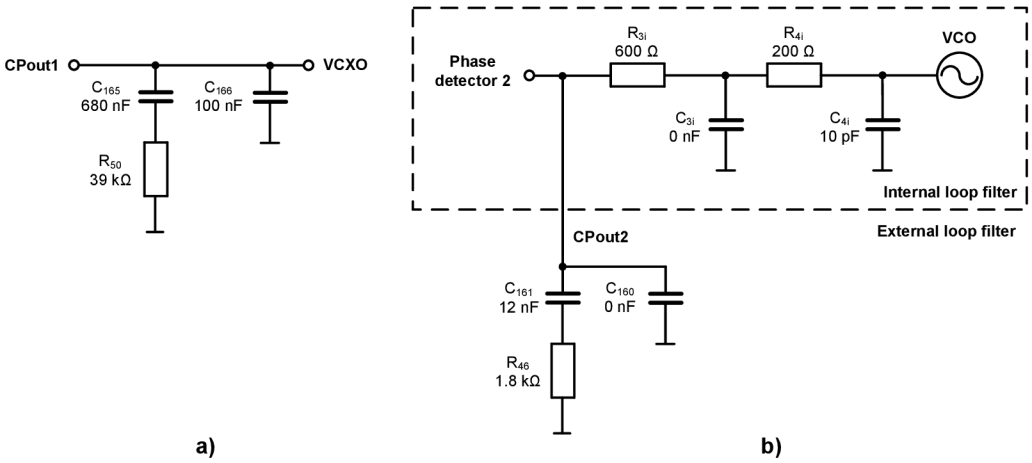


Fig. 5.6: PLL loop filters.

The simulation results show the PLL1 loop bandwidth is 12 Hz and a phase margin equals to 49 degrees. In the case of PLL2 circuit, it is 534 kHz and 84 degrees respectively. Considering these results, it is obvious that their properties are fulfilling the initial premises and proposed filters can be used for the design.

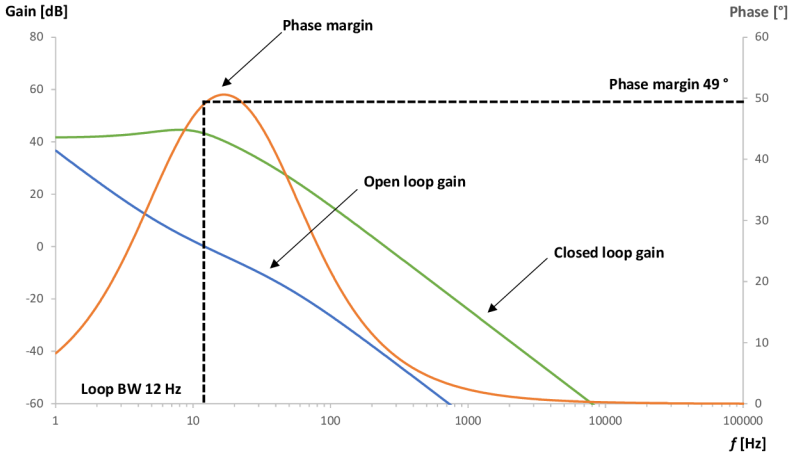


Fig. 5.7: Simulation results of PLL1 filter frequency response.

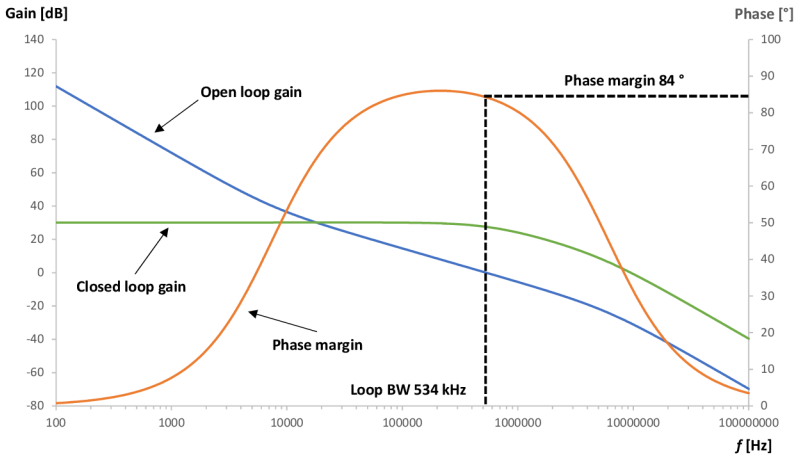


Fig. 5.8: Simulation results of PLL2 filter frequency response.

The simulation results of the phase noise characteristics for each logic signal output are depicted in Fig. 5.9 and in Fig. 5.10. Note that the characteristics do not take into account the phase noise produced by the reference signal source, and consequently they are just product of the jitter cleaner clock source. Referring to the narrow bandwidth of the PLL1 filter, the final impact on the characteristics will be insignificant.

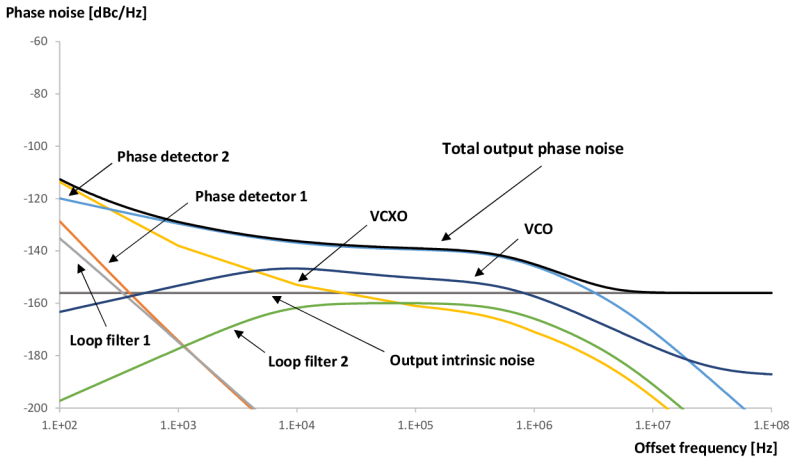


Fig. 5.9: Phase noise characteristics of the 122.88 MHz frequency clock output (LVDS).

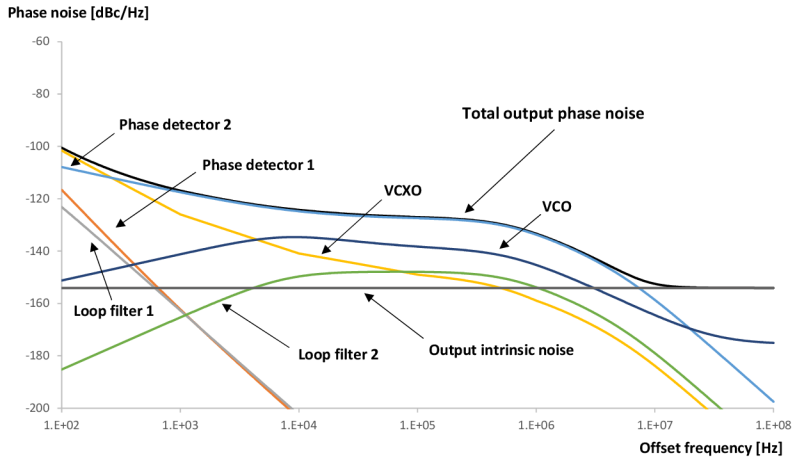


Fig. 5.10: Phase noise characteristics of the 491.52 MHz frequency clock output (LVPECL).

With regard to the obtained results, it is obvious that the most relevant source of the phase noise is created by the phase detector in the PLL2 together with the VCXO. There is no difference in the phase noise behaviour at the output in terms of the output logic standard. On the contrary, the noise characteristics slightly differ considering the output frequencies.

5.1.4 Signal Termination

Working with high communication frequencies requires an appropriate termination at the end of both single-ended and differential signal lines. In Fig. 5.11 we can see logic standards used in the final design with their proposed termination. The simplest situation (Fig. 5.11a) is with the LVDS logic where a single 100 Ω resistor is sufficient. The D flip-flop outputs are driven by the CML logic which needs to be terminated according to Fig. 5.11b. The more complex termination is required by the LVPECL logic as show in Fig. 5.11c and 5.11d. The main goals of these structures is to set up the termination voltage at both nodes of the transmission line $V_{\mathrm{TT}} = V_{\mathrm{CC}}$ - 2 V. This condition could be achieved by the voltage divider application in accordance to the Thevenin's theorem of the equivalent circuit [27].

An example situation is described below where R_{term} means the resulting termination resistance and R_{term1}, R_{term2} express the resistors of a simple voltage divider. The AC analyses expects the ideal voltage source of zero-ohm internal resistance, thus, the parallel combination of termination resistors can be calculated as

$$R_{\mathrm{term}} = R_{\mathrm{term1}} \parallel R_{\mathrm{term2}} = \frac{R_{\mathrm{term1}} \cdot R_{\mathrm{term2}}}{R_{\mathrm{term1}} + R_{\mathrm{term2}}} = \frac{130 \cdot 82}{130 + 82} \approx 50\,\Omega, \tag{5.2}$$

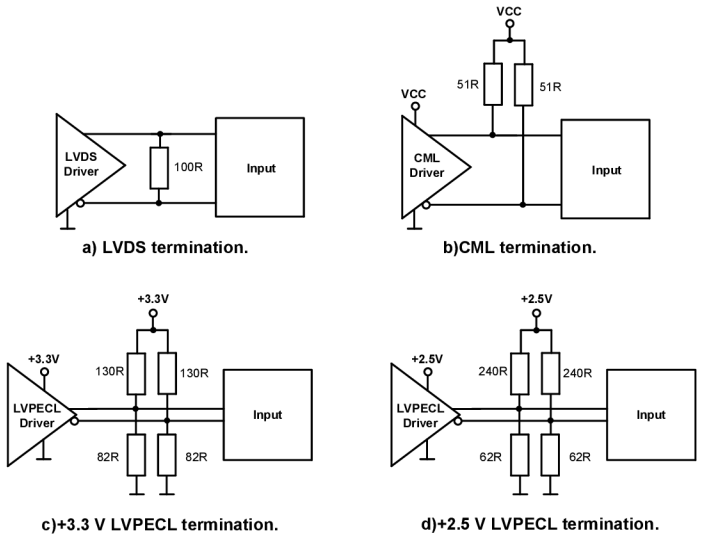


Fig. 5.11: Termination of the logic standards.

which creates the target 50 Ω resistance. Subsequently, the termination voltage V_{TT} can be expressed as follows

$$V_{\mathrm{TT}} = V_{\mathrm{CC}} \left(\frac{R_{\mathrm{term2}}}{R_{\mathrm{term1}} + R_{\mathrm{term2}}} \right) = 3.3 \cdot \left(\frac{82}{130 + 82} \right) \doteq 1.27 \text{ V}. \tag{5.3}$$

5.1.5 Low-Noise Voltage Regulators

The chosen components required four supply voltage branches, i.e. +2.5 V, + 3.3 V and ±5 V. In order to achieve low-noise performance, selected voltage regulators are low-noise LDO (Low-dropout), namely TPS7A90 for the positive branches and TPS7A30 for the negative one respectively [28, 29]. A schematic diagram of the positive linear regulator is depicted in Fig. 5.12.

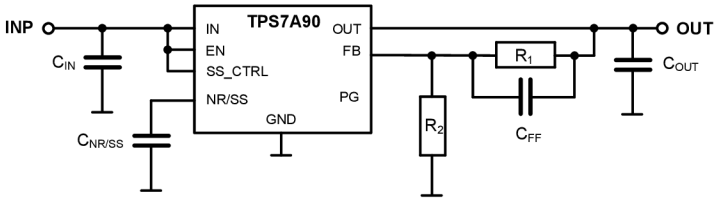


Fig. 5.12: Power supply schematic.

The initial condition for the resistor value selection is

$$\frac{V_{\mathrm{ref}}}{R_2} > 5\ \mu\mathrm{A}, \tag{5.4}$$

where the reference voltage $V_{\text{ref}} = 0.8$ V. Choosing $R_2 = 2.2$ kΩ meets the requirement, thus, the R_1 value could be calculated as:

$$R_1 = R_2 \left(\frac{V_{\text{out}}}{V_{\text{ref}}} - 1 \right) = 2200 \cdot \left(\frac{2.5}{0.8} - 1 \right) = 4.675 \approx 4.7\,\text{k}\Omega. \tag{5.5}$$

The voltage regulator design is constrained by two main aspects, by the power dissipation and the noise performance. It is not practical to work just with one power input for positive regulators due to high power dissipation. To lower the dissipation, we decided to split power inputs into three independent branches. Positive +2.5-V and +3.3-V regulators are powered together and +5-V and -5-V regulators have separete input. Moreover, this arrangement enables to set a proper voltage drop on the regulators, thus, PSRR (Power Supply Rejection Ratio) can be optimized.

The total power dissipation of +2.5-V branch regulator can be estimated assuming the total current consumption of the voltage branch is $I_{\text{out}} = 371$ mA and the input voltage is set to $V_{\text{in}} = 3.5$ V. The power dissipation P_{D} equals to

$$P_{\text{D}} = (V_{\text{in}} - V_{\text{out}}) \cdot I_{\text{out}} = (3.5 - 2.5) \cdot 0.371 = 0.371\,\text{W}. \tag{5.6}$$

Nevertheless, the maximum power dissipation is limited by the junction temperature T_{J} and in accordance to [28] its maximum recommended value is 125 °C. Assuming the ambient temperature equals to $T_{\text{A}} = 23$ °C the following relation can be established

$$T_{\text{J}} = T_{\text{A}} + (\theta_{\text{JA}} \cdot P_{\text{D}}) = 23 + (56.9 \cdot 0.371) \doteq 44.1\,^{\circ}\text{C}, \tag{5.7}$$

where θ_{JA} denotes the junction-to-ambient thermal resistance which is 56.9 °C/W. The estimated value of the junction temperature is not significantly high and we can expect lower value on the outer side of the package. The estimated results of the dissipated power and the junction temperature of each voltage branch can be found in Tab. 5.1.

Voltage branch	**Set input voltage [V]**	**Voltage drop [V]**	**Current cons. [A]**	**Power dissip. [W]**	**Thermal res. [W/°C]**	**Junction temp. [°C]**
+2.5 V	+3.5	1	0.371	0.371	56.9	44.1
+3.3 V	+3.5	0.2	0.448	0.896	56.9	28.1
+5 V	+5.2	0.2	0.393	0.786	56.9	27.5
-5 V	-5.2	0.2	0.050	0.01	47.7	23.5

Tab. 5.1: Estimated properties of the voltage regulators.

The entire circuit is equipped with the input and output capacitors. In general, their values have to be more then 10 μF which is ensured by the parallel combination of two or three capacitors to achieve finer filtration. Connecting an external capacitor to the noise reduction pin can improve the total performance as well. Consequently, the generated noise by the internal band-gap reference is reduced. Finally, there is a feed-forward capacitor in the feedback path maintaining the same noise reduction function along with the PSRR enhancement [28].

5.1.6 DAC Module

Although the DAC module (depicted in Fig. 5.13) is a pre-manufactured product, it has to be modified to cooperate with the other components in the proposed architecture. The key part on the module is the DAC which has an interface created by data inputs and the clock signal input. The clock input source is located in the FPGA module and it behaves as a sampling clock frequency signal of the provided data. The asserted data on the bus inputs are stored in the input FIFO (First In, First Out) and the whole process is synchronized to the clock signal using DLL (Delay-Locked Loop). The I samples have to be asserted on the rising edge and the Q samples on the falling edge of the clock signal. The DAC on the module requires another clock signal of quadrupled clock rate [15] for channel A and channel B output proper synchronization. This clock signal is produced on the acquisition module and connected using coaxial cables.

The DAC module is equipped with a clock synchronizer CDCM7005 [30] for self-synchronization but to achieve the overall coherence in the system, this synchronizer needs to be in the "bypass" mode. The reference clock source on the module is not relevant in this situation and it is necessary to provide a clock signal on the VCXO synchronizer input and set the output multiplexer to divide the signal frequency by one. The VCXO input is able to work only with LVPECL signals and this requirement is met because the acquisition module provides that one.

The last part on the DAC module is an IQ Modulator [31]. This part requires an external +5 V power supply and has to be connected to LO signal source. Note that the same LO signal has to be connected to the acquisition module to ensure coherency between modulated and demodulated signal.

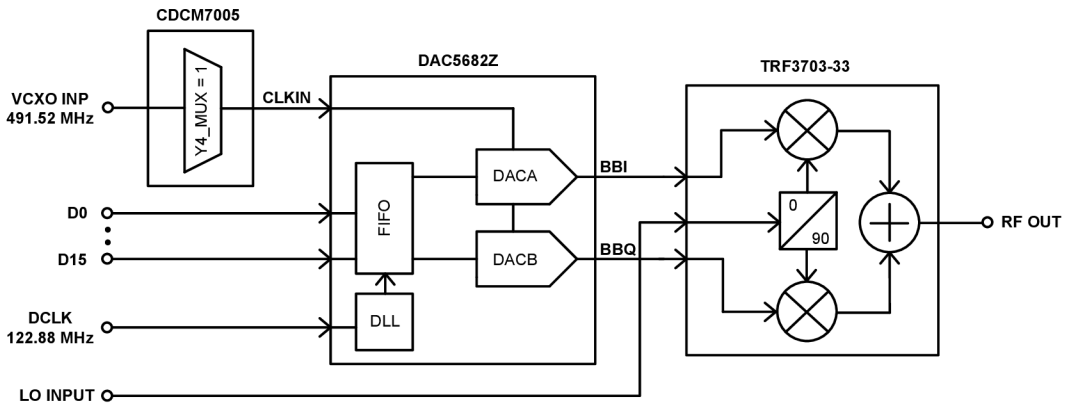


Fig. 5.13: DAC module inner schematic.

5.1.7 FPGA Module

The FPGA module is the Spartan-3A DSP 1800A platform [14] containing XC3-SD1800A FPGA [32]. This module is the core component of the proposed design enabling to join the other modules through the expansion connectors. Moreover, it provides power supply branches for undemanding components in terms of noise performance. Apart from these, it stores the IQ signal samples which can be assigned either to a BRAM (Block Random Access Memory) inside the FPGA or to a SDRAM (Synchronous Dynamic Random Access Memory) on the module. Note that the internal BRAM size is just 189 KB and for larger amount of data we can use the SDRAM of 128 MB. For communication proposes, there is a serial port connected to UART (Universal Asynchronous Receiver Transmitter).

5.2 PCB Design

To achieve the best noise performance and proper impedance matching, 4-layer PCB (Printed Circuit Board) was proposed. The design has to cover the requirements stated in [33] for chosen manufacturing process and the PCB stack-up is depicted in Fig. 5.14. The top layer is intended for RF components, differential signals routing, and all other sensitive parts. On the contrary, the bottom layer is determined for remaining insensitive components. To maintain an appropriate value of differential or single-ended route impedance, we used the inner ground and power layers as the reference layers. Although the manufacturing process creates a great opportunity to produce cost-effective prototypes, there are several limitations which could negatively contribute to the design performance.

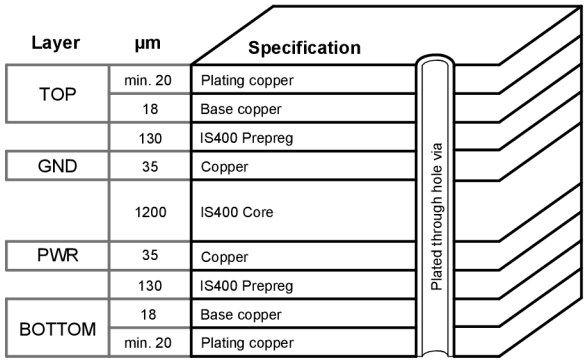


Fig. 5.14: 4-layer PCB stackup.

For calculation purposes of the transmission line impedance, it was utilized freeware environment Saturn PCB Design Toolkit (available at [34]) and the final outcomes can be found in Fig. 5.15. A single-ended signal has to be 0.25 mm wide and the differential pairs width should be equal to 0.2 mm together with spacing of 0.35 mm. Both results were computed for 0.13 mm distance between the conductive traces.

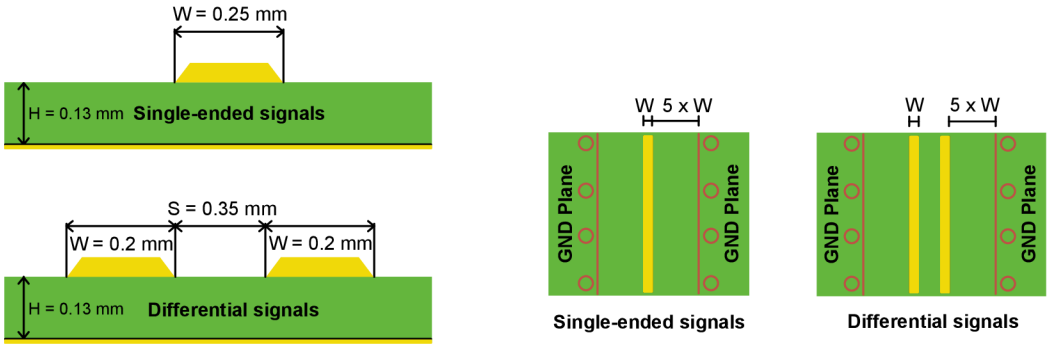


Fig. 5.15: Signal trace properties.

In accordance to [35], an appropriate gap is essential between the differential pair signals and ground plane. In particular, it means to maintain blank space equivalent to the fifth multiple of the trace width. The same rule is applied in case of single-ended signals. The noise performance and undesirable emissions can be significantly improved by stitching vias. Referring to [36], the best solution is achieved when the distance between the vias is between $\lambda/8$ and $\lambda/20$, where λ denotes the wavelength of the carrier signal frequency in this case.

The PCB is equipped with several SMA connectors [37] ensuring the signal connection to other parts of the architecture. The selection of a connector type was arranged to fit an appropriate trace width into a middle pin. An attachment to the FPGA module is established by expansion connector QSE-060-01-F-D-A [38].

A proposed feature that should not have been overlooked is the interconnection between the comparator output and the D flip-flop inputs which is introduced in Fig. 5.16. In fact, the flip-flops are connected in parallel, but the first one is placed as closed as possible to the comparator output. The final distance between the pins equals approx. to 2 mm. Subsequently, the differential pair on the output is split and distributed through the bottom layer to the SMA connector on the PCB edge. The signal follows through the delay line, and afterwards, it returns into the module. An indicated length of the delay line is 500 mm but it can be changed during the debugging process. The termination resistors located on the end of the path are indispensable for proper function of the entire circuit. On the contrary, the termination on the exact output of the comparator become unwanted due to the short distance of the components placement. Finally, the proposed PCB design was manufactured and assembled which can be seen in Fig. 5.17a (top view) and in Fig. 5.17b (bottom view).

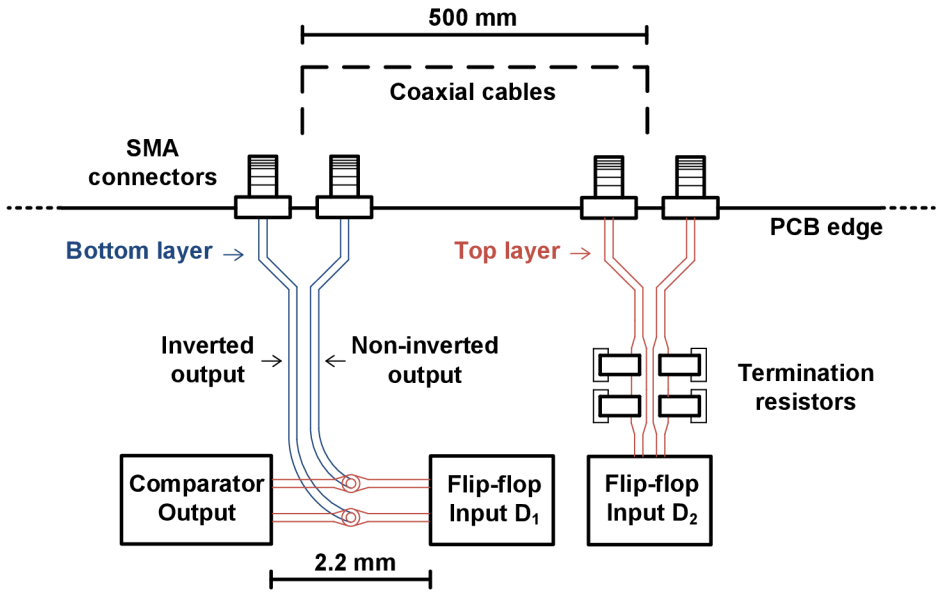
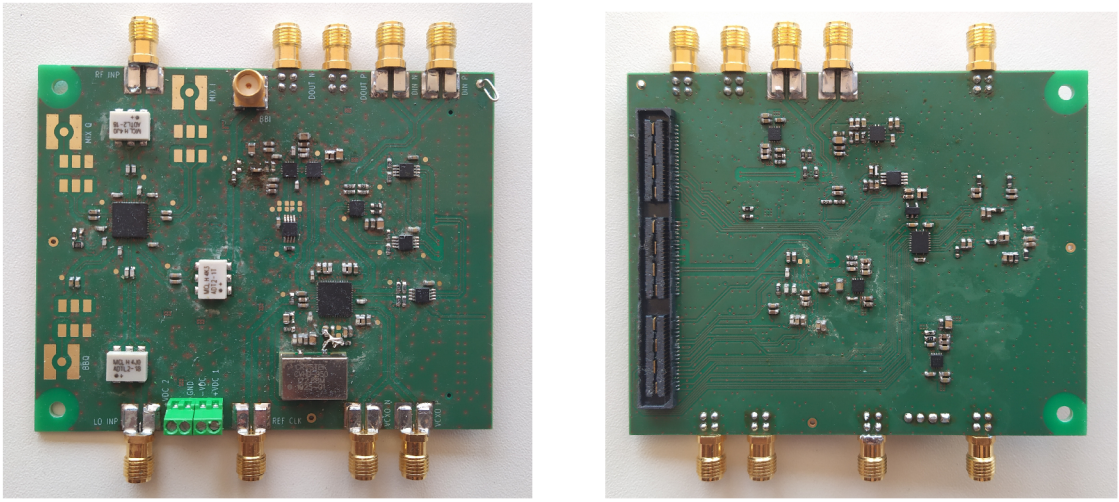


Fig. 5.16: Delay line connection (not in scale).



(a) Top view. (b) Bottom view.

Fig. 5.17: Proposed PCB design.

5.3 Firmware Development

The next point on the way of the proposed architecture evaluation was to develop a firmware enabling to acquire the edge time instants. At first, the firmware has to be able to communicate with all employed parts via appropriate data buses. Subsequently, it is required to sent the IQ data samples and to acquire the edge time instants. Finally, the proposed firmware has to send the data to the PC for subsequent evaluation in the MATLAB environment. The entire code structure is attached in listings (chapter E) together with the register settings (chapter F).

5.3.1 Program Development and Execution

Spartan 3A DSP 1800A is supported by ISE Design Suite environment (available at [39]) where the project was developed. The main part of the code was realized in VHDL (Very High Speed Integrated Circuit Hardware Description Language) with a minor part written in assembly language. The flow of the program is depicted in Fig. 5.18. Firstly, the registers of the clock distributor LMK04133 and IQ Demodulator TRF371125 are set up. For this purpose, the PicoBlaze core (available at [40]) is used which is embedded 8-bit RISC (Reduced Instruction Set Computer) microcontroller optimised for assembler code. The remaining components i.e. CDCM7005 (clock distributor) and DAC5682Z (DAC) settings are stated in VHDL entities CDCM7005_SPI.vhd and DAC5682Z_HW_SPI.vhd. All components utilize SPI interface, therefore, a freeware core specified for SPI communication (available at [41]) was modified and implemented into the project.

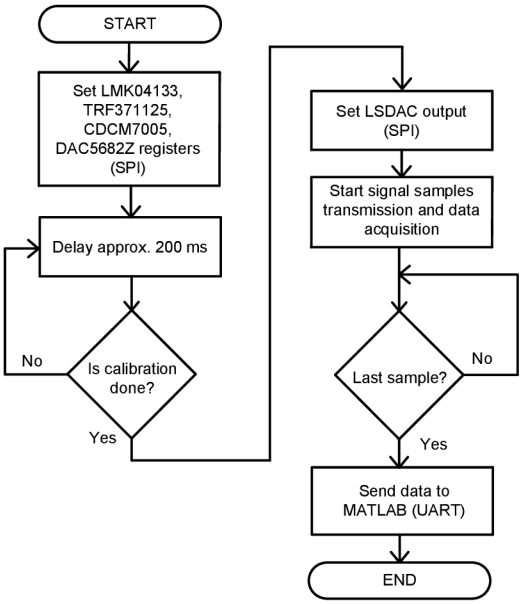


Fig. 5.18: Flowchart of the proposed FW.

First we need to set registers of jitter cleaner LMK04133 which is based on Fig. 5.5 to produce an appropriate output clock signals. Subsequently, we set registers of the main DAC DAC5682Z. This part is connected to the clock source provided by the acquisition module, thus, the internal PLL frequency multiplier function is disabled. The other set properties are DLL delay adjustment to skew the input clock signal (90°), the input data format (2's complement), and data interpolation (performed four times).

Next, we set the clock distributor CDCM7005 on the DAC module. The only requirement is to provide the input VCXO signal to the output without any modifications. In order to achieve this premise, the output multiplexer (Y4_MUX) is assigned to divide the signal by one. The last component on the setting list is the IQ Mixer. Apart form the properties mentioned in the previous chapter, it is providing a DC offset calibration. The process is initiated by assertion of a specific bit (EN_AUTOCAL) in register 2. The number of calibration steps and the oscillator frequency is determined according to [16]. The clock divider ratio is as high as possible to achieve the best results of IQ balance, although the time of the calibration is increasing with the divider ratio which is not relevant in this case. In accordance to the calculation stated in [16], a 200 ms delay is inserted into the program flow to reach the calibration convergence time with certain margin. If the specific bit is asserted after the process is finished, the program continues to the next stage. Otherwise, the delay is applied again along with the state inquiry.

An example procedure of the SPI communication is depicted in Fig 5.19 with the 14-bit LSDAC. An input interface of the converter enable to latch data in the input register operating SS (Slave Select), SCLK (Serial Clock), and MOSI (Master Output Slave Input) signals. The transferred data word on the MOSI line contains value of 5554_{16} which equals to 101010101010100_2 in binary. The least two significant bits do not belong to the 14-bit data word, but has to be set to zero for proper function. Thus, the transferred value is 5461_{10}.

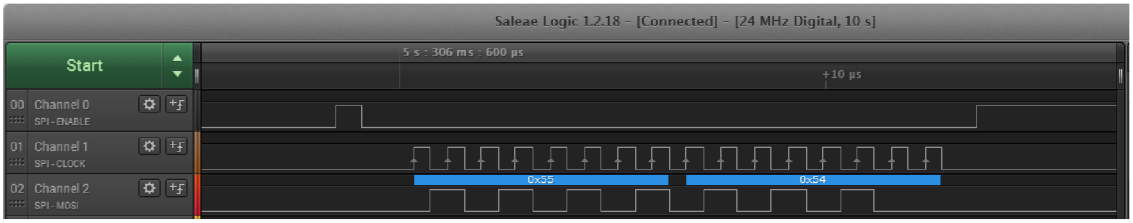


Fig. 5.19: LSDAC SPI communication capture.

The output voltage V_{out} of the LSDAC is set according to

$$V_{\text{out}} = V_{\text{ref}} \cdot \frac{DATA}{N_{\text{max}}}, \tag{5.8}$$

where V_{ref} denotes the reference voltage which is 3 V, $DATA$ refers to the transferred data word, and the maximum number N_{max} of 14-bit converter output voltage levels equals to 2^{14}. A comparison between the set level and the measured output can be seen in Fig. 5.20. It is evident that there is a certain offset and its value equals approximately to -65 mV. Please note that the depicted input range does not cover the full capabilities of the LSDAC.

To check the mixer calibration state, we developed a communication module (mixer_readback.vhd) enabling to read certain register content of the IQ Mixer. A capture of the established communication is depicted in Fig. 5.21. Unlike the previous figure, the SPI bus is extended to include the MISO (Master Input Slave Output) line. In this case, the first half of the communication on the bus contains an address of the register which is supposed to be read (Register 2, Address 010_2) and the second half contains the register data. Finally, the content of the register is asserted by the IQ Mixer logic on the next falling edges of the SCLK signal. Both captures are realized using Saleae Logic Analyzer software (available at [43]).

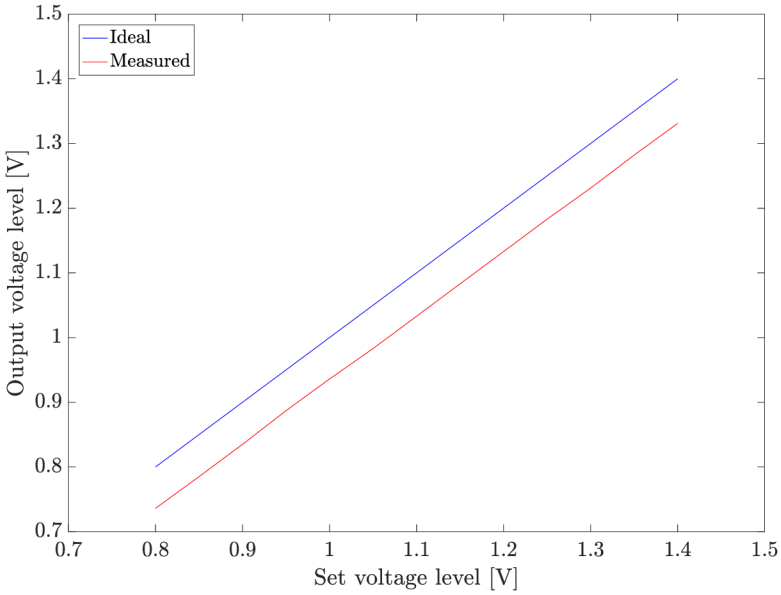


Fig. 5.20: LSDAC output characteristics.

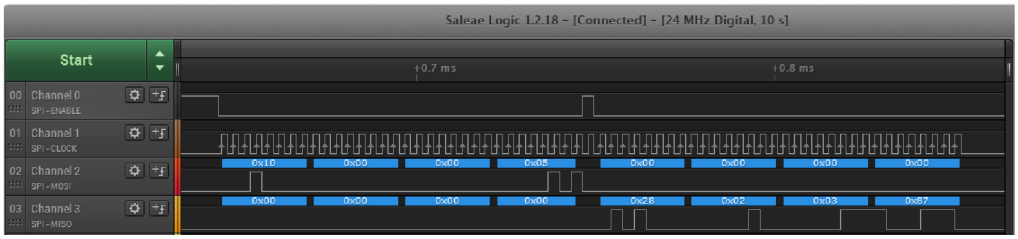


Fig. 5.21: IQ Mixer SPI communication capture.

The program execution is synchronized to the clock signal distributed on the FPGA module until a new one is provided by the acquisition module. Once the system is synchronized, a signal sample transmission is initiated simultaneously with data acquisition. The timing diagram of the program signals is depicted in Fig. 5.22. At first, the LSDAC output voltage level is set. Once the last bit of the word is latched, the transmission of signal samples starts. The I-component data samples are assigned to DAC on the rising edge of the system clock (provided as data clock as well in fact) and the Q data on the falling edge. To ensure this, there is an ODDR (Output Double Data Rate Register) on the output. During the transmission, the time instants are acquired and stored in BRAM when the acquisition circuit recognizes the edge and this time moment is specified by the DAC-sample counter. For the hardware evaluation, we are limited by 65536 number of IQ samples which can fit into the internal memory, and the LSDAC output is set

just once at the beginning. For further testing, the proposed firmware is prepared for easy modifications including the possibility to set the LSDAC output at a specified time (counter state) implicating a capability to acquire longer sequences.

After the last sample is sent, obtained data are transferred into the PC by the UART core (uart.vhd) available at [42]. Afterwards, the received data are converted into the time samples and properly aligned with the transmitted signal in the MATLAB.

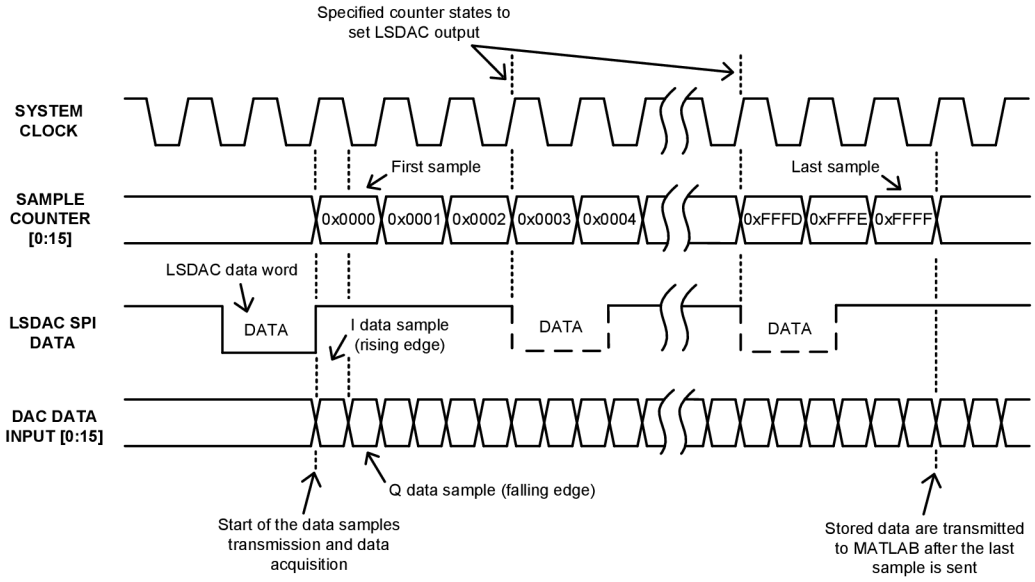


Fig. 5.22: Signal output waveforms.

5.3.2 Input Timing Constraints

The received signal from the D flip-flop outputs has to be aligned with the clock signal to constrain the setup and hold times. The entire estimation is based on Fig. 5.23. Apart from the path delay, a clock signal skew of the jitter cleaner T_{skew1}, the clock-to-output time T_{cko} of the D flip-flops, and part-to-part skew T_{skew2} of the high-speed translator have to be taken into account. A summary of particular element delays is stated in Tab. 5.2.

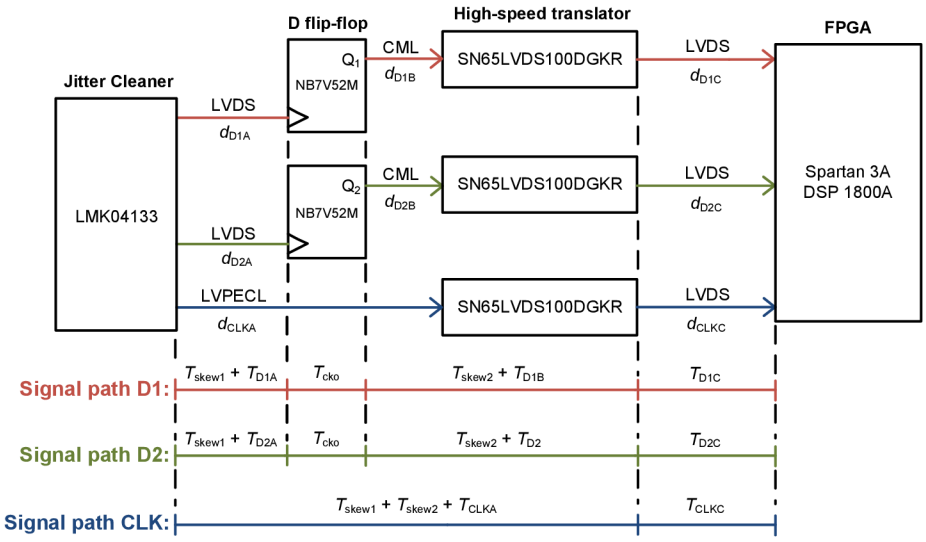


Fig. 5.23: Path delay estimation.

Element	**Length [mm]**	**Delay [ps]**
d_{D1A}	27.7	185
d_{D1B}	25.9	173
d_{D1C}	154.6	1031
d_{D2A}	25.9	173
d_{D2B}	11.2	75
d_{D2C}	142.9	953
d_{CLKA}	13.7	92
d_{CLKC}	164.8	1099

Tab. 5.2: Path element delay.

Assuming an average propagation signal velocity v_{p} on the PCB is approximately 150 $\mathrm{mm} \cdot \mathrm{ns}^{-1}$, the path delay T_{D1A} which can be observed on the end of a distance element d_{D1A} equals to

$$T_{\mathrm{D1A}} = \frac{d_{\mathrm{D1A}}}{v_{\mathrm{p}}} = \frac{27.7}{150} \doteq 185\ \mathrm{ps}. \tag{5.9}$$

The delay of the whole signal path D1 denoted as $T_{\mathrm{path\_D1}}$ can be obtained as follows:

$$T_{\mathrm{path\_D1}} = T_{\mathrm{D1A}} + T_{\mathrm{D1B}} + T_{\mathrm{D1C}} = 185 + 173 + 1031 = 1389\ \mathrm{ps}. \tag{5.10}$$

Nevertheless, the signal processing components can cause an additional delay. For this purpose, we determine the maximum possible delay $T_{\text{tot\_max}}$ and in the case of the D1 signal path, $T_{\text{tot\_max\_D1}}$ equals to

$$\begin{aligned} T_{\text{tot\_max\_D1}} &= (T_{\text{path}} + T_{\text{cko}} + T_{\text{skew1}} + T_{\text{skew2}}) \cdot 1.2 = \\ &= (1389 + 600 + 40 + 100) \cdot 1.2 \doteq 2555 \text{ ps}. \end{aligned} \tag{5.11}$$

A sum is multiplied by 1.2 factor to obtain 20 % margin. On the other hand, the minimum delay is assumed as $T_{\text{tot\_min\_D1}} = T_{\text{path}}$. Tab. 5.3 states all calculated values for each signal path.

Signal path	T_{path} [ps]	T_{cko} **[ps]**		T_{skew1} **[ps]**		T_{skew2} **[ps]**		T_{tot} **[ps]**	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
D1	1389	0	600	0	40	0	100	1389	2555
D2	1201	0	600	0	40	0	100	1201	2329
CLK	1191	-	-	0	40	0	100	1191	1597

Tab. 5.3: Total path delay estimation.

Setup and hold times are related to the rising edge of the clock signal as depicted in Fig. 5.24. The main aim of this calculation is to determine "OFFSET IN BEFORE" and "VALID" properties which are required for the UCF (User Constraints File).

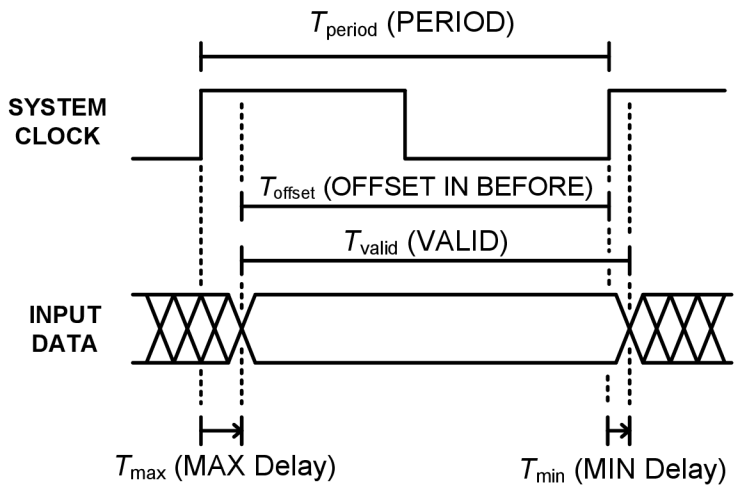


Fig. 5.24: Input timing constraints parameters.

At first, it is essential to obtain minimal and maximal data signal arrival time after the rising clock edge. The worst case occurs when the clock edge arrives with the minimal delay value $T_{\text{tot\_min\_clk}}$. The minimal arrival time of the signal from the D flip-flop output $T_{\text{min\_D1}}$ can be calculated as

$$T_{\text{min\_D1}} = T_{\text{tot\_min\_D1}} - T_{\text{tot\_min\_clk}} = 1389 - 1191 = 198\,\text{ps} \tag{5.12}$$

and the maximum arrival time $T_{\text{max\_D1}}$ equals to

$$T_{\text{max\_D1}} = T_{\text{tot\_max\_D1}} - T_{\text{tot\_min\_clk}} = 2555 - 1191 = 1364\,\text{ps}. \tag{5.13}$$

The system clock period is set to $T_{\text{period}} = 8.138\,\text{ns}$, afterwards we can obtain the time offset $T_{\text{offset\_D1}}$

$$T_{\text{offset\_D1}} = T_{\text{period}} - T_{\text{max\_D1}} = 8138 - 1364 = 6774\,\text{ps} \tag{5.14}$$

and the time valid $T_{\text{valid\_D1}}$

$$T_{\text{valid\_D1}} = T_{\text{offset}} + T_{\text{min\_D1}} = 6774 + 198 = 6972\,\text{ps}. \tag{5.15}$$

In Tab. 5.4 we can see the entire subset of parameters for both D1 and D2 inputs.

Input	T_{min} **[ps]**	T_{max} **[ps]**	T_{offset} **[ps]**	T_{valid} **[ps]**
D1	198	1364	6774	6972
D2	10	1138	7000	7010

Tab. 5.4: Input constraints parameters.

Finally, the obtained values can be inserted into the UCF as stated below. Each differential input pair is coupled into the group by TNM constrain and the calculated parameters are assigned to them.

```
INST "d1_outq_n" TNM = D1_FLIP_FLOP;
INST "d1_outq_p" TNM = D1_FLIP_FLOP;
INST "d2_outq_n" TNM = D2_FLIP_FLOP;
INST "d2_outq_p" TNM = D2_FLIP_FLOP;
TIMEGRP "D1_FLIP_FLOP" OFFSET = IN 6.77 ns VALID 6.97 ns BEFORE
"ACQ_CLK_n" RISING;
TIMEGRP "D2_FLIP_FLOP" OFFSET = IN 7 ns VALID 7.01 ns BEFORE
"ACQ_CLK_n" RISING;
```

6 Architecture Evaluation

In this chapter we present the entire evaluation of the proposed architecture. The hardware adjustment is described together with the path delay calculation. Finally, the measurement results are presented including the edge time acquisition outcomes and the system power consumption.

6.1 Hardware Adjustment

To produce the desired clock signal frequencies, the jitter cleaner circuit located on the acquisition module was modified to ensure the proper function. Detected fault was based on the improper voltage level on the VCXO output (exceeding the maximum acceptable value of 2 $V_{\mathrm{p-p}}$ according to [23]). This defect was solved by deploying an additional voltage divider at the OSCin input pin which is depicted in Fig. 6.1.

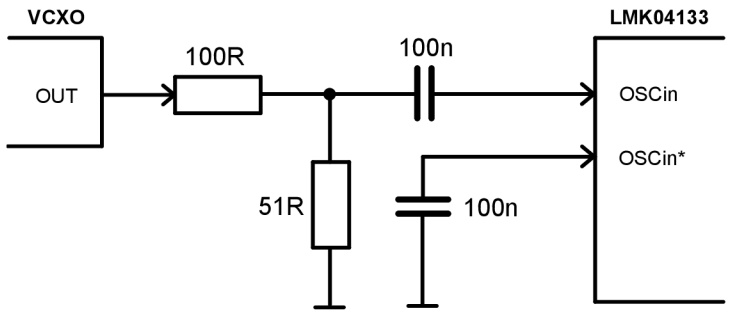


Fig. 6.1: Additional voltage divider at the VCXO output.

The clock source distributes signal of two logic standards, i.e. LVDS and LVPECL. The output 122.88 MHz signal can be seen in Fig. 6.2. According to [23], the LVDS differential voltage range has to be 250-450 m$V_{\mathrm{p-p}}$ and the LVPECL 660-965 m$V_{\mathrm{p-p}}$. Regarding the measurements, these values met the specifications, but a slight difference can be observed due to the coarse probe measurements.

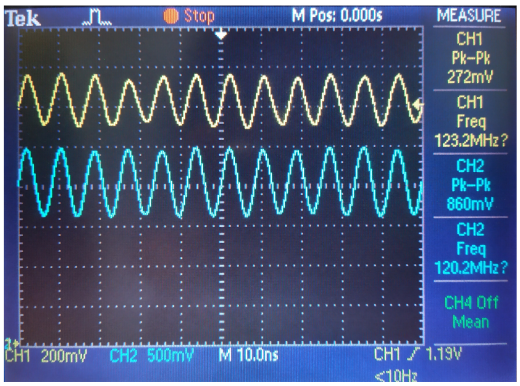
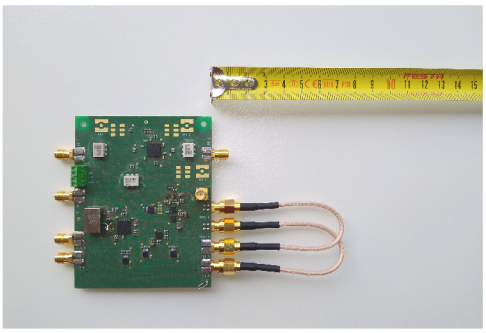
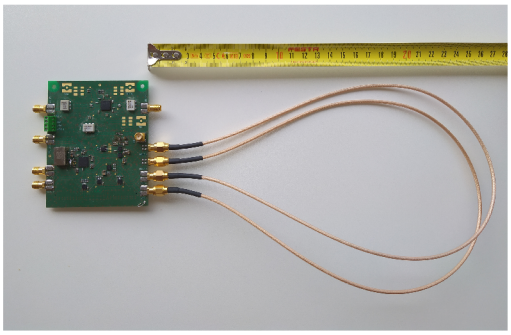


Fig. 6.2: LVDS and LVPECL clock signal output.

We adjusted the delay path of the edge time acquisition circuit. We connected the SMA connectors on the PCB by the coaxial cables. The circuit was evaluated for 300 mm and 600 mm cable lengths as depicted in Fig. 6.3a and 6.3b respectively.



(a) Coaxial cable – length 300 mm.



(b) Coaxial cable – length 600 mm.

Fig. 6.3: Delay path adjustment.

The path delay of these two coaxial cables can be estimated as follows:

$$t_{\mathrm{d300}} = \frac{l_{300}}{v_{\mathrm{p}}} = \frac{l_{300}}{\frac{c}{\sqrt{\epsilon_{\mathrm{eff}}}}} \approx \frac{0.3}{\frac{2.99 \cdot 10^8}{\sqrt{2.1}}} \approx 1.45\ \mathrm{ns}, \tag{6.1}$$

$$t_{\mathrm{d600}} = \frac{l_{600}}{v_{\mathrm{p}}} = \frac{l_{600}}{\frac{c}{\sqrt{\epsilon_{\mathrm{eff}}}}} \approx \frac{0.6}{\frac{2.99 \cdot 10^8}{\sqrt{2.1}}} \approx 2.91\ \mathrm{ns}, \tag{6.2}$$

where t_{d300} and t_{d600} denotes 300 mm and 600 mm cable path delay respectively, v_{p} equals to the propagation velocity of the signal inside the coaxial cable and ϵ_{eff} is the effective permittivity of the coaxial cable material (PTFE (Polytetrafluoroethylene)) and it equals approximately to 2.1. The cable delays need to be added to the signal propagation on the PCB. The length l_{PCB} of the copper trace from the components

to the SMA connectors and vice versa is roughly 68 mm, thus, the PCB delay t_{dPCB} equals to

$$t_{\mathrm{dPCB}} = \frac{l_{\mathrm{PCB}}}{v_{\mathrm{p}}} = \frac{l_{\mathrm{PCB}}}{\frac{c}{\sqrt{\epsilon_{\mathrm{eff}}}}} \approx \frac{0.068}{\frac{2.99 \cdot 10^8}{\sqrt{2.84}}} \approx 0.38 \text{ ns}. \tag{6.3}$$

Finally, the total delay t_{d300} for the 300 mm coaxial cable equals to

$$t_{\mathrm{d300}} = t_{\mathrm{d300C}} + t_{\mathrm{dPCB}} = 1.45 + 0.38 = 1.83 \text{ ns}, \tag{6.4}$$

and in the case of 600 mm coaxial cable, delay t_{d600} equals to

$$t_{\mathrm{d600}} = t_{\mathrm{d600C}} + t_{\mathrm{dPCB}} = 2.91 + 0.38 = 3.29 \text{ ns}. \tag{6.5}$$

After the implementation of the proposed delay path in the edge time acquisition circuit, we performed initial tests. The input sine wave with frequency of 100 kHz signal and amplitude of 1.25 $V_{\mathrm{p-p}}$ was compared with the LSDAC output voltage level which equals to 0.933 V. The DC voltage level at the comparator input was set to 1.012 V by the voltage divider. The results of the test can be seen in Fig. 6.4. The channel 1 depicts the input signal and the channels 2 and 3 are the output signals of the D flip-flops. The test was held for both proposed path delays.

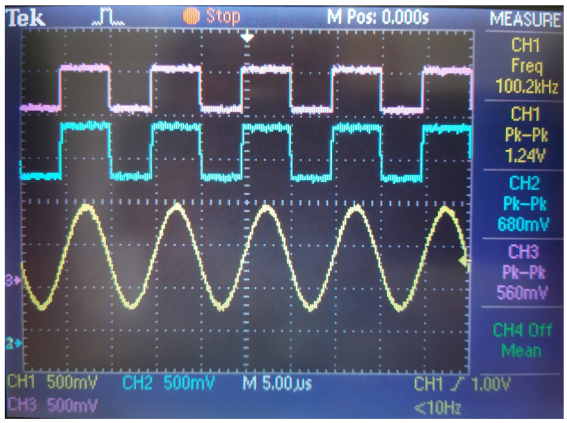


Fig. 6.4: Comparator input signal and D flip-flop outputs signal diagram.

The next steps of the debugging process were heading towards the assembly of each architecture module together with the signal generators which can be seen in Fig. 6.5. As the reference clock signal source we used the arbitrary waveform generator Sigilent SDG 2042X providing 12.288 MHz signal of 1 $V_{\mathrm{p-p}}$ amplitude. The carrier frequency 806 MHz was generated by the RF Signal Generator Keysight N9310A. The frequency was chosen in accordance to the center of LTE (Long-Term Evolution) downlink band no. 20 [44]. Considering the results during the debugging, the optimal power level of -31 dBm was set.

Subsequently, the received signal was compared with the transmitted to verify the appropriate transmission chain settings. For this purpose, a sine wave IQ samples were generated in the MATLAB software and converted to a coefficient file to be stored in the internal BRAM in the FPGA. Once the transmission was verified by the measurement with the oscilloscope, the edge time acquisition circuit debugging was initiated. Received data were processed in the MATLAB environment as well. The transmission process was tested with both coaxial cable lengths but the meaningful results were obtained only with the 600 mm long cable. The entire test environment containing all used instruments is depicted in Fig. 6.6. A detailed view of the assembled modules can be seen in Fig. 6.7.

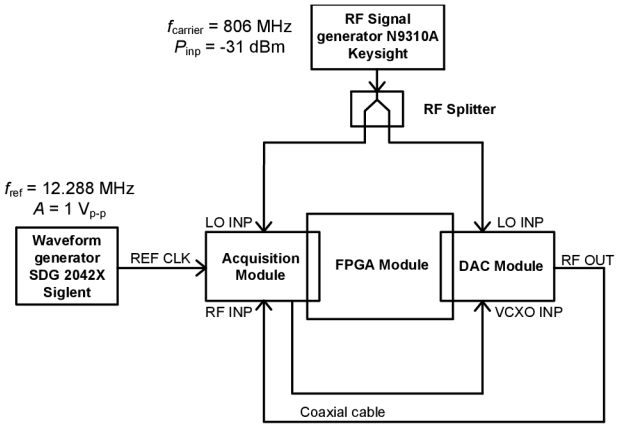


Fig. 6.5: Wiring diagram of HW components.

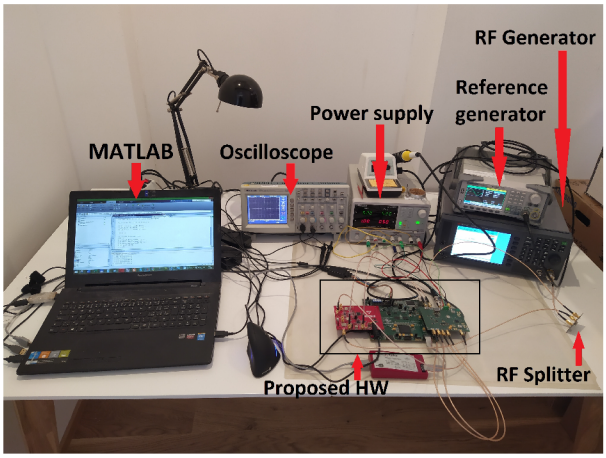


Fig. 6.6: Test environment.

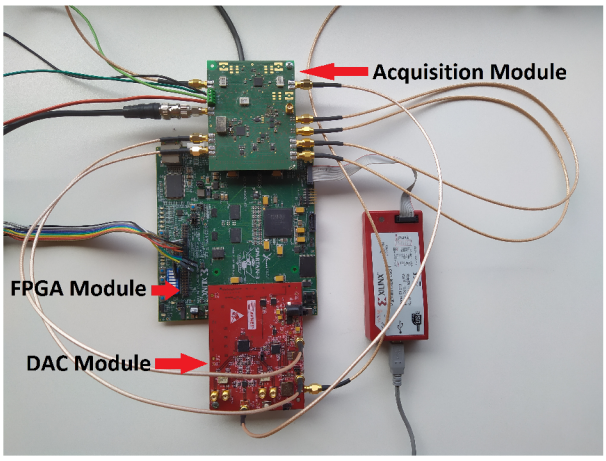


Fig. 6.7: Architecture modules.

6.2 Measurement Outcomes

For the purpose of the architecture evaluation, two sets of the signal samples were generated, i.e. sine wave and 64QAM signal. The entire number of the signal samples was 65536 what equals roughly to 530 μs long sequence with 122.88 MHz sampling rate. The MATLAB software was used for the post-processing to fit the received data with the original signal by minimizing the MSE (Mean Squared Error).

The sine wave signal frequency was 480 kHz which we chose based on the corner working range of the baseband balun transformer which is 400 kHz. The timing diagram of the original signal and the acquired time instants over a certain period of samples is depicted in Fig. 6.8.

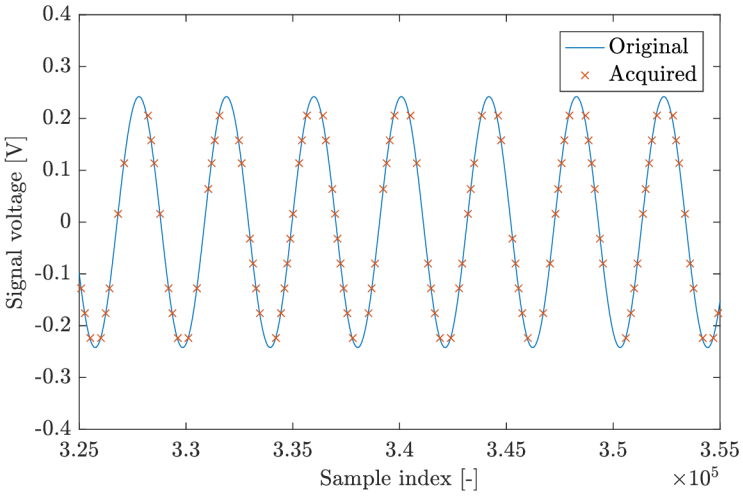


Fig. 6.8: Original sine wave signal (blue line) and acquired time instants (red crosses).

It is evident, that the system is not able to acquire each edge time moment but the proposed method for DPD coefficient calculation does not require to restore the overall signal. The difference between the original signal and the acquired samples can be seen in the input-output transfer characteristics in Fig. 6.9. Although the error deviation is almost constant over the signal voltage level, the maximum value can be observed around the zero level crossing (the closest measured value is -0.032 V). The absolute errors are depicted in histograms in Fig. 6.10 and in Fig. 6.11. The error is in a range from -5 mV to +10 mV.

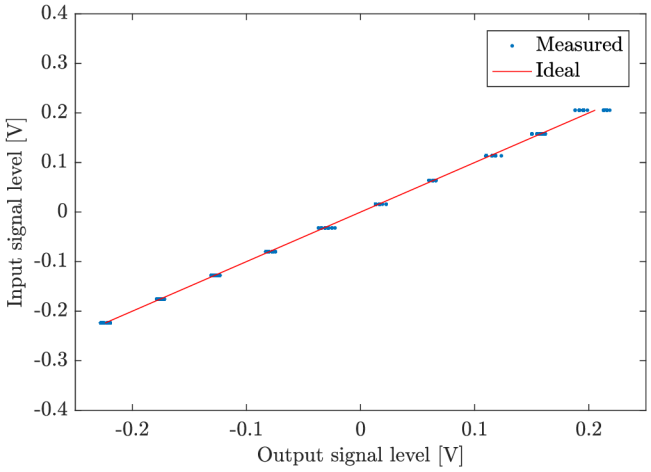


Fig. 6.9: Input-output characteristics for the sine wave signal.

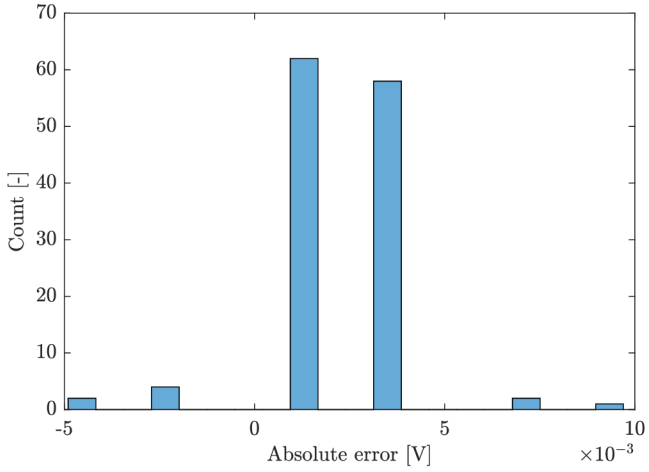


Fig. 6.10: Absolute error histogram of -0.032 V level for the sine wave signal.

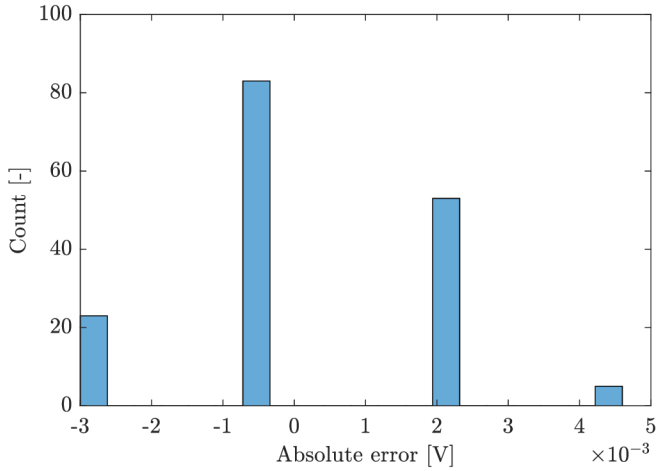


Fig. 6.11: Absolute error histogram of -0.128 V level for the sine wave signal.

We performed the next evaluation with the 64QAM signal of 500 kHz bandwidth frequency-shifted to 1 MHz due to the working frequency range of baseband balun. The timing diagram of transmitted signal and the acquired time instants is depicted in Fig. 6.12.

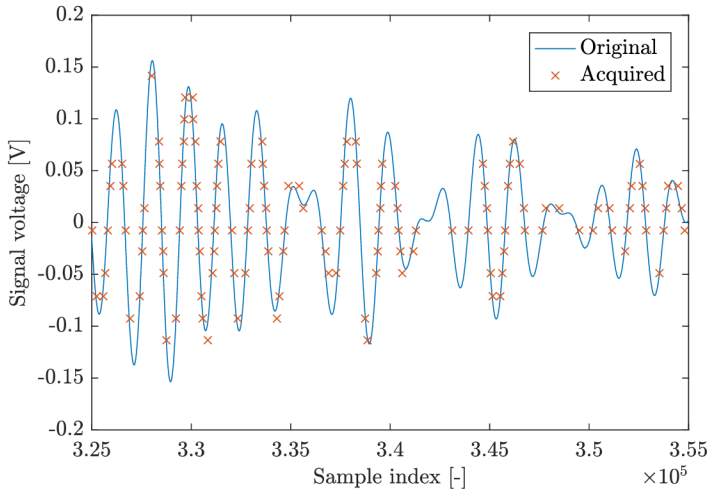


Fig. 6.12: Original 64QAM signal (blue line) and acquired time instants (red crosses).

A better view on the transmission results can be found in the conversion characteristics in Fig. 6.13. The absolute error is reaching its maximum when the signal is crossing the zero voltage level, on the contrary, the minimum can be found on the ends, thus, obviously the error deviation is changing across the signal amplitude. According to the histogram of the absolute errors for the reference voltage of -0.014 V and 0.121 V (depicted in Fig. 6.14 and in Fig. 6.15 respectively), the maximum error can be observed in a range from -40 mV to +40 mV.

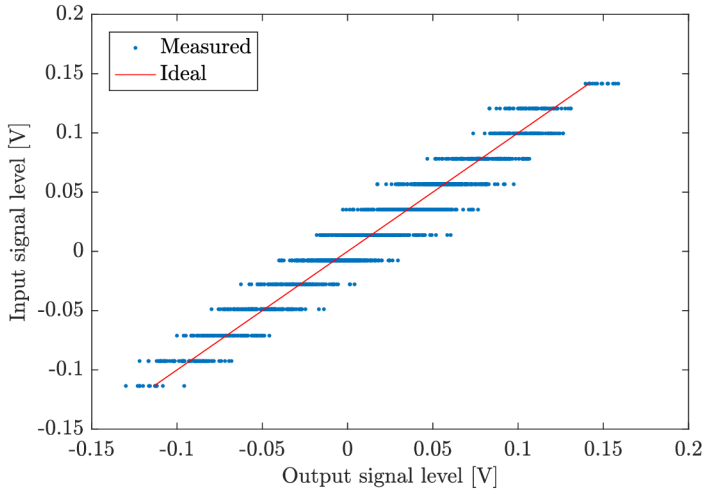


Fig. 6.13: Input-output characteristics for the 64QAM signal.

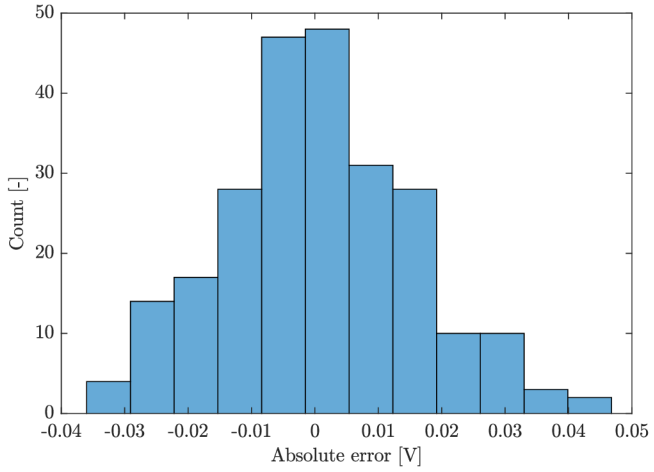


Fig. 6.14: Absolute error histogram of -0.014 V level for the 64QAM signal.

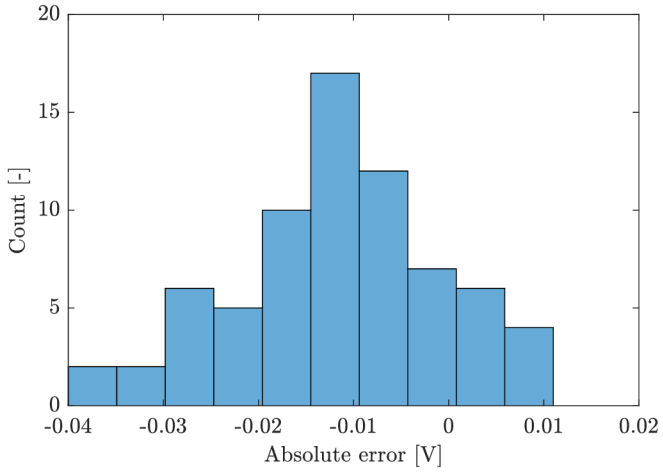


Fig. 6.15: Absolute error histogram of 0.121 V level for the 64QAM signal.

Although the system is synchronized to the same clock domain, it does not ensure a relevant timing of the received analog signal according to the digital time instants. There are several aspects contributing to this imperfection. The most significant is the possibility of setup and hold time violation of the D flip-flops. This causes the metastability making the edge time acquisition impossible. Another great aspect is added noise into the transmitted signal produced by the RF generator and by the power supplies placed on the PCB, therefore, an error between the transmitted and acquired signal can be observed.

The edge time acquisition circuit is constrained by the comparator hysteresis value which was adjusted to 10 mV. To prevent the undesired oscillations, this

value should not be decreased, but sometimes it can misrepresent the obtained results. Another property of the circuit which influences the results is the delay path adjustment. For the architecture evaluation, we decided to use a cable of 600 mm length. Future work should cover various delay modifications to find the optimum.

Another significant aspect influencing the proposed architecture behaviour is the bandwidth of the transmitted signal. The executed measurements were performed with a single tone sine wave and with the 64QAM signal of 500 kHz bandwidth. The single tone was used just for the system function verification and its utilization in the current communication systems is unrealistic. Thus, the 64QAM signal measurement is more valuable. On the contrary, its error deviation is reaching approximately the range from -40 mV to +45 mV which could be still applicable under certain conditions in this system using 64QAM signal of 400 m$V_{\mathrm{p-p}}$ amplitude. Nevertheless, it should be noted that the deviation error reaches its maximum at the signal zero crossing level but a significant distortion is expected on the peaks which positively contribute to utilization in DPD systems. Regarding these facts, the proposed system should undergo certain tests deploying a nonlinear power amplifier and DPD realization.

6.3 Power Consumption Comparison

Implementing the comparator in the feedback path can significantly contribute to the whole performance of the system. Apart from its simplicity, power consumption reduction appears as one of the most important features. For the performance comparison, the entire consumption was measured and the results can be found in Tab. 6.1 below. The measured consumption is slightly below the maximum power consumption by data sheets.

Voltage branch	**Input voltage [V]**	**Measured current consumption [A]**	**Power consumption [W]**	**Maximum power consumption [W]**
+2.5 & +3.3 V	+3.5	0.68	2.38	2.87
+5 V	+5.2	0.48	2.50	2.04
-5 V	-5.2	0.03	0.16	0.26
Total power consumption			**5.04**	**5.17**

Tab. 6.1: Acquisition module power consumption.

In Tab. 6.2 we can find the maximum power consumption of the edge time acquisition circuit components by the data sheets. The LSDAC and a voltage reference are not included because their contribution is negligible in comparison to the other parts. The acquisition circuit serves as a replacement of the ADC in the conventional DPD system, there for the comparison we chose an equivalent ADC. For example, the ADC ADS5483 [45] from Texas Instruments with 135 MSps has the maximum power dissipation of 2.35 W or AD9461 [46] from Analog Devices with 130 MSps has the maximum power dissipation of 2.4 W. In both cases, the ADC replacement results in approximately 50 % power savings in this example.

Component	**Maximum power consumption [W]**
Comparator (ADCMP5682)	0.258
D flip-flops (NB7V52M)	0.71
High-speed translator (SN65LVDS100DGKR)	0.22
TOTAL	**1.19**

Tab. 6.2: Edge time acquisition circuit power consumption.

7 Future Extensions

For further implementation of the architecture in the DPD assessment systems, several extensions were proposed to ensure better precision along with the measurement convenience improvement covering hardware and firmware modifications.

The implemented firmware works with the internal BRAM which limits the number of samples and thus enables only the short signal sequences. Possible prolonging could be achieved by the external DDR2 SDRAM on the FPGA module. In this case, a specific approach should be considered because the data is accessible just in the bursts. Additionally, the SDRAM has to be refreshed periodically to ensure the data integrity. Considering these facts, the FIFO is a necessary part of the design ensuring the continuous data flow to the DAC module to preserve the sampling rate. Nevertheless, the FIFO depth has to be adjusted adequately because the SDRAM controller is able to work with the maximum frequency of 133 MHz at the -4 speed grade of the used FPGA, therefore, it is not possible to increase the reading frequency arbitrarily [47].

Although, the main advantage of the proposed architecture is the implementation of the comparator instead of the ADC in the feedback path, it could be beneficial to use external ADC module to acquire the received signal for proper post-processing signal alignment. This suggestion is made just for debugging purposes and consequently, the ADC is not included in the final proposed architecture design. This should be really beneficial for the better precision achieving because we used only the oscilloscope probe during the measurement at this time.

The finer delay value utilization could be valuable together with the longer signal sequences measurement as well. A reason why to operate with the longer signals is the memory effect of the PAs which has to be taken into account. Additionally, more LSDAC output voltage levels could be set at once during the measurement, and consequently better precision could be achieved.

The proposed design evaluation was based on the sine wave and 64QAM signal measurement, nevertheless, the further assessment should be heading towards the measurements operating with higher PAPR signals, such as OFDM or FBMC (Filter Bank Multicarrier). Finally, it will be crucial to extend the design by the PA and the attenuator to fully evaluate the DPD performance.

8 Conclusion

There are several approaches to linearize power amplifiers and the DPD is one of the most promising methods optimizing the signal distortion and the system efficiency. The conventional predistorters utilize ADC in the feedback path, but this might be the main bottleneck. The main goal of this master's thesis is to propose an architecture implementing a comparator which replaces the ADC. An acquisition module based on this architecture was proposed and its behaviour evaluated.

The edge time acquisition circuit as the key part of the acquisition module was presented. The circuit function was verified by simulations and the final properties of the circuit, especially the delay path was adjusted. The path was arranged to ensure an appropriate delay, but the meaningful results were obtained just with the delay value of 3.3 ns. The main objective of the architecture evaluation was the capability of the edge time acquisition, consequently, the measurement of the sine wave and 64QAM signal transmission was established. According to the presented results, the minimal absolute error between the transferred and received signal was observed in the case of the sine wave measurement. On the contrary, a significant absolute error was discovered deploying the 64QAM signal. Despite the higher values, the error deviation was less noticeable on the peaks of the signal. Nevertheless, the substantial distortion of the transferred signal is expected there and this fact can positively contribute to future DPD realization.

The main aspect affecting the edge time acquisition is the metastability emerging as a result of the setup and hold time violation of the D flip-flops. Another great factor is the added noise contributing to the data misrepresentation. A not least important property influencing the acquisition error is the comparator hysteresis which has to be set accordingly to the measured signal levels.

The deployment of the proposed acquisition circuit in the feedback path instead of ADC can positively contribute to the power consumption reduction in the DPD architecture. The proposed solution introduces up to 50% power savings in comparison with the conventional system using ADC.

Regarding the obtained results, the utilization of the developed acquisition module is suitable for the proposed architecture, and the designed hardware will serve in future research on the DPD system realization.

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List of symbols and abbreviations

ϵ_{eff}	Effective permittivity
θ_{JA}	Junction-to-ambient thermal resistance
ω	Angular frequency
3GPP	3rd Generation Partnership Project
$A()$	Power amplifier's function
ACPR	Adjacent Channel Power Ratio
ADC	Analog-to-Digital Converter
AM/AM	Amplitude to Amplitude
AM/PM	Amplitude to Phase
b	Matrix of coefficients
BRAM	Block Random Access Memory
c	Speed of light
C	Capacitor
Clk	Clock
CML	Current Mode Logic
d_{N}	Distance of Nth element
DAC	Digital-to-Analog converter
DC	Direct current
DLA	Direct Learning Architecture
DLL	Delay-Locked Loop
DPD	Digital Predistortion
DSP	Digital Signal Processing
e	Error variable
f	Frequency
f_{LP}	Low pass filter cut-off frequency
$F_{\text{post}}()$	Postdistorter function
FBMC	Filter Bank Multicarrier
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
G	Gain
G_0	Appropriate gain
i	Index
IC	Integrated Circuit
IF	Intermediate Frequency
ILA	Indirect Learning Architecture
IoT	Internet of Things
K	Model non-linearity order

l	Length
LO	Local Oscillator
LDO	Low-dropout
LVDS	Low-Voltage Differential Signaling
LSDAC	Low Speed Digital-to-Analog Converter
LTE	Long-Term Evolution
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSE	Mean Squared Error
n	Sample index
NR	New Radio
ODDR	Output Double Data Rate Register
OFDM	Orthogonal Frequency Division Multiplexing
p	Signal variable
PA	Power Amplifier
PC	Personal Computer
P_{1dB}	1 dB compression point
P_{D}	Power dissipation
P_{Sat}	Saturation power
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase-Locked Loop
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PTFE	Polytetrafluoroethylene
Q	Memory length
QAM	Quadrature Amplitude Modulation
r	Signal variable
R	Resistor
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
s	Signal variable
SS	Slave Select
SCLK	Serial Clock
SDRAM	Synchronous Dynamic Random Access Memory
SMA	SubMiniature version A
SPI	Serial Peripheral Interface

t	Time
t_{d}	Transmission line delay
t_{s}	Settling time
T_{A}	Ambient temperature
T_{cko}	Clock-to-Output
T_{J}	Junction temperature
T_{max}	Maximum time delay
T_{min}	Minimum time delay
T_{offset}	Timing offset
T_{path}	Path delay
T_{skew}	Clock skew time
T_{tot}	Total delay
T_{valid}	Valid data time
$\mathbf{U}$	Memory polynomial kernel matrix
UART	Universal Asynchronous Receiver Transmitter
UCF	User Constraints File
UE	User Equipment
v_{p}	Propagation velocity
V_{CC}	Supply voltage
VCM	Common-Mode Voltage
V_{in}	Input voltage
V_{in}	Output voltage
V_{ref}	Reference voltage
V_{out}	Output voltage
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VGA	Variable Gain Amplifier
VHDL	Very High Speed Integrated Circuit Hardware Description Language
x	Signal variable
y	Signal variable
z	Signal variable

List of appendices

A Schematic Diagrams

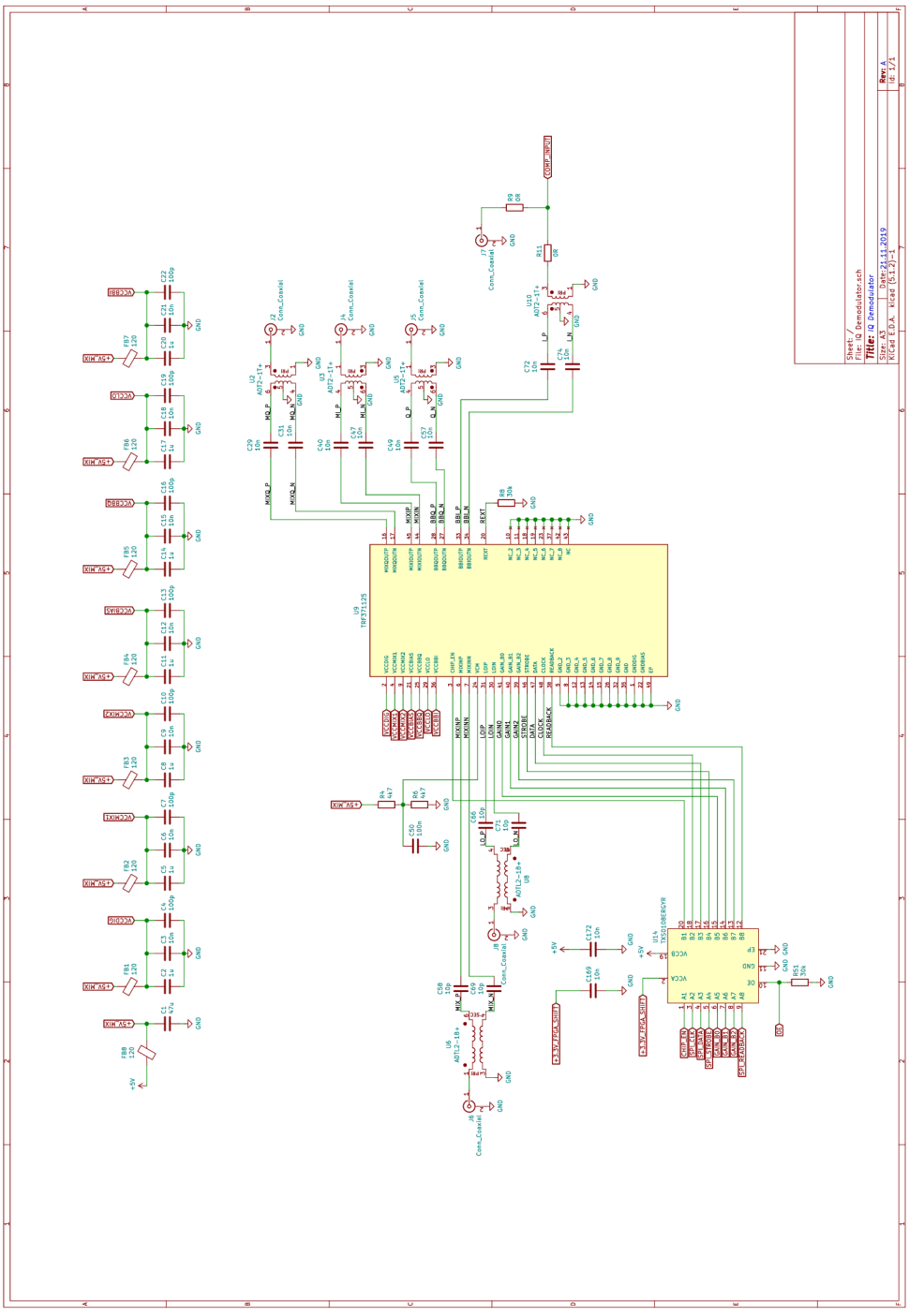

Fig. A.1: IQ Demodulator section schematic.

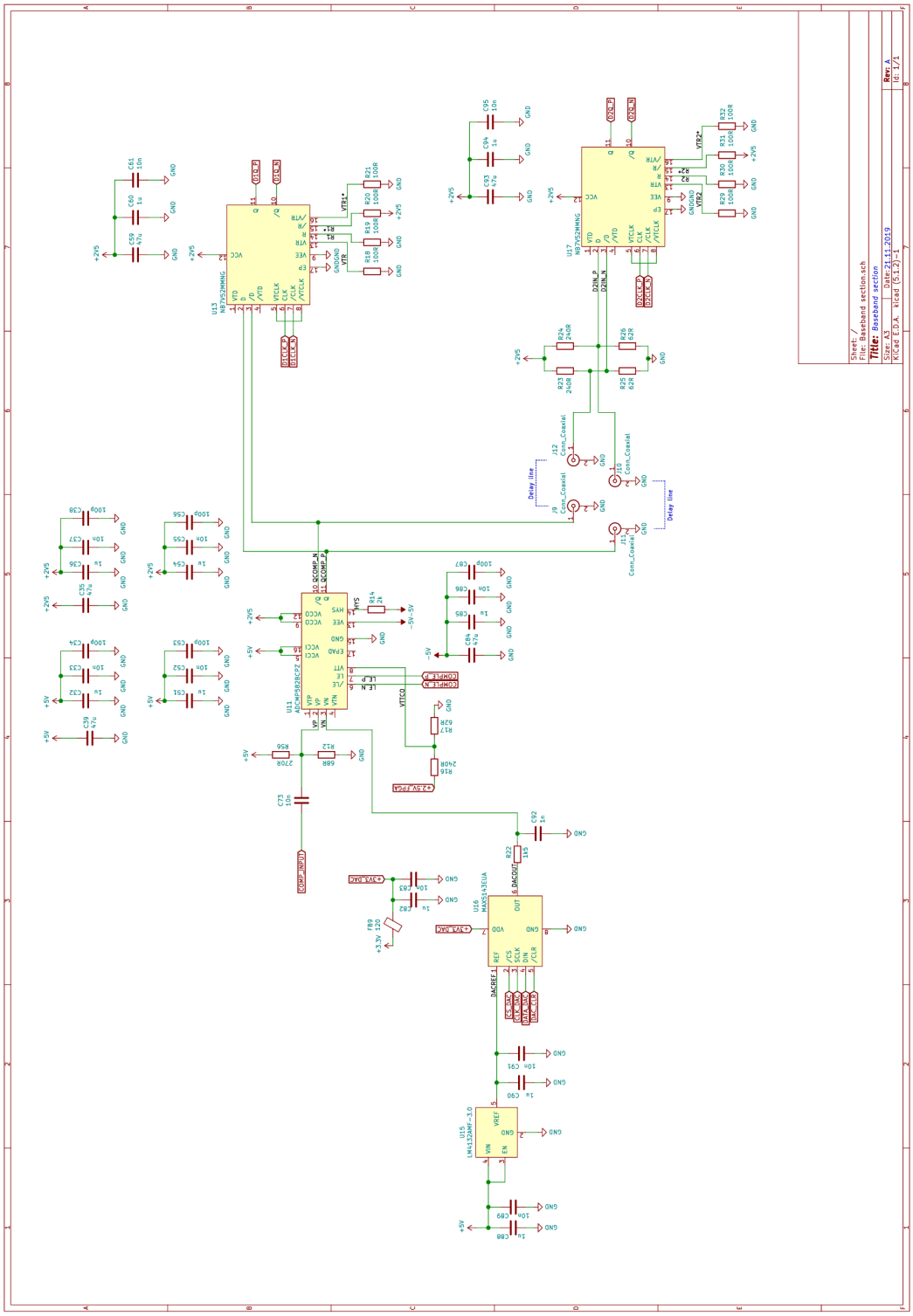

Fig. A.2: Baseband section schematic.

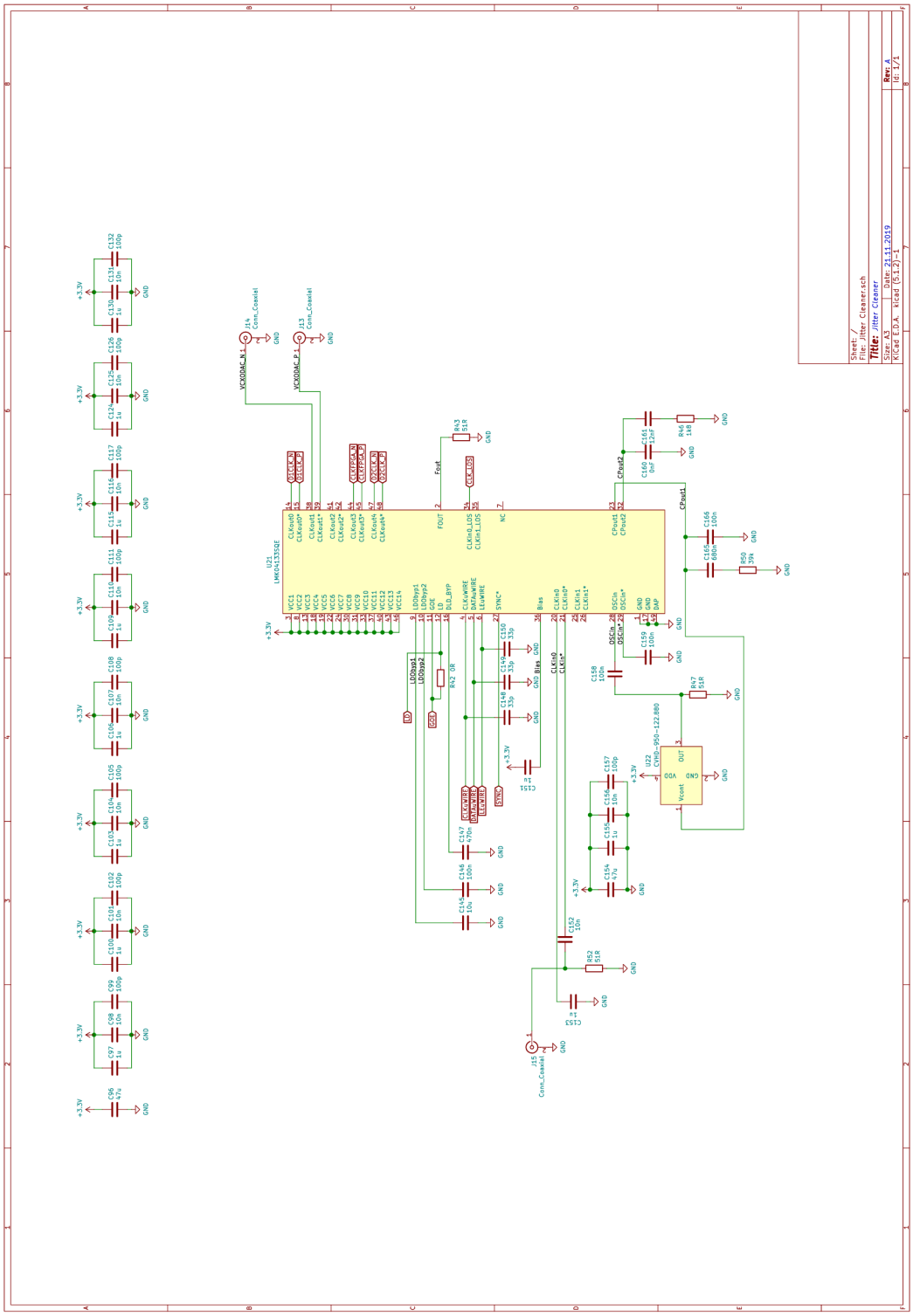

Fig. A.3: Jitter cleaner section schematic.

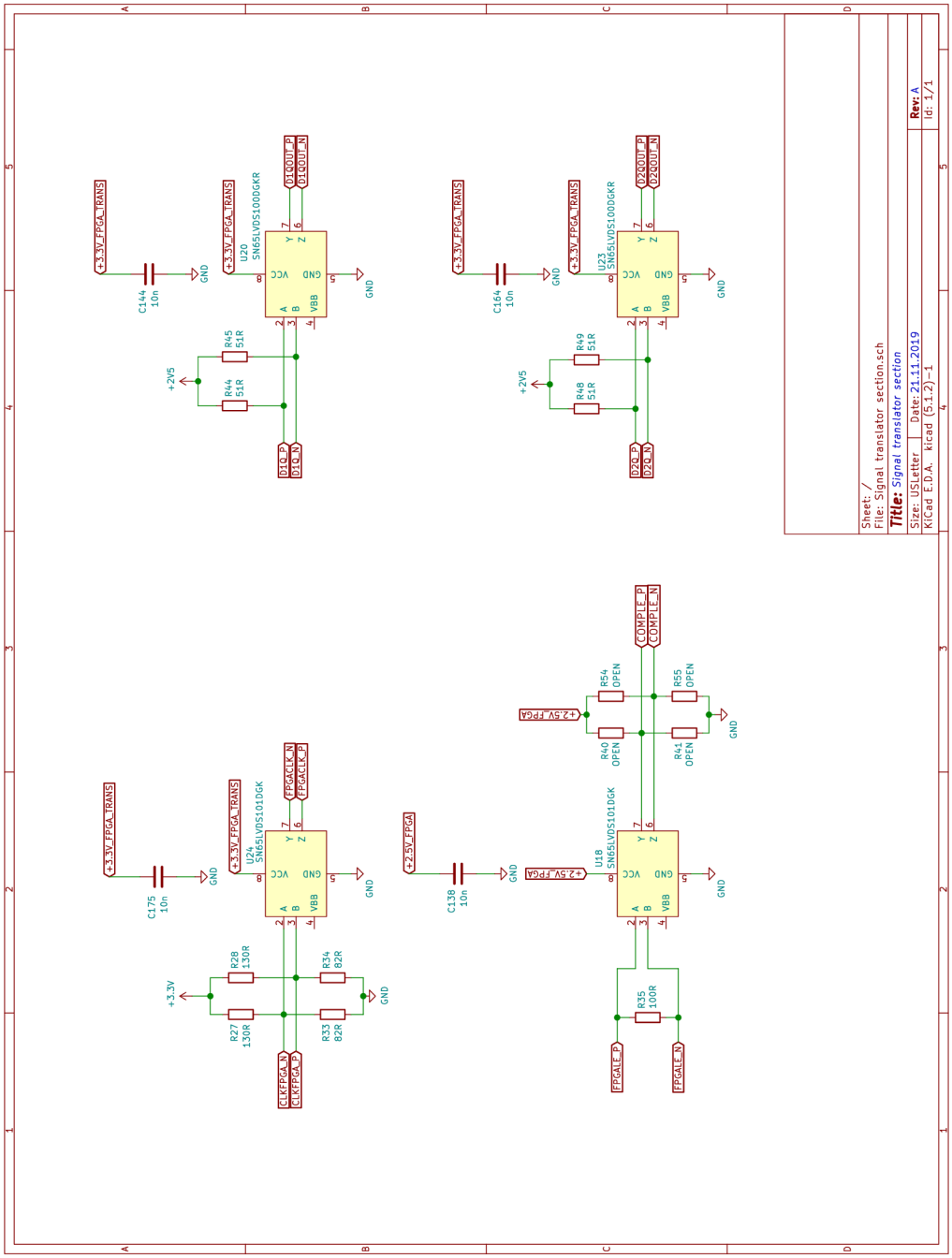

Fig. A.4: Signal translators section schematic.

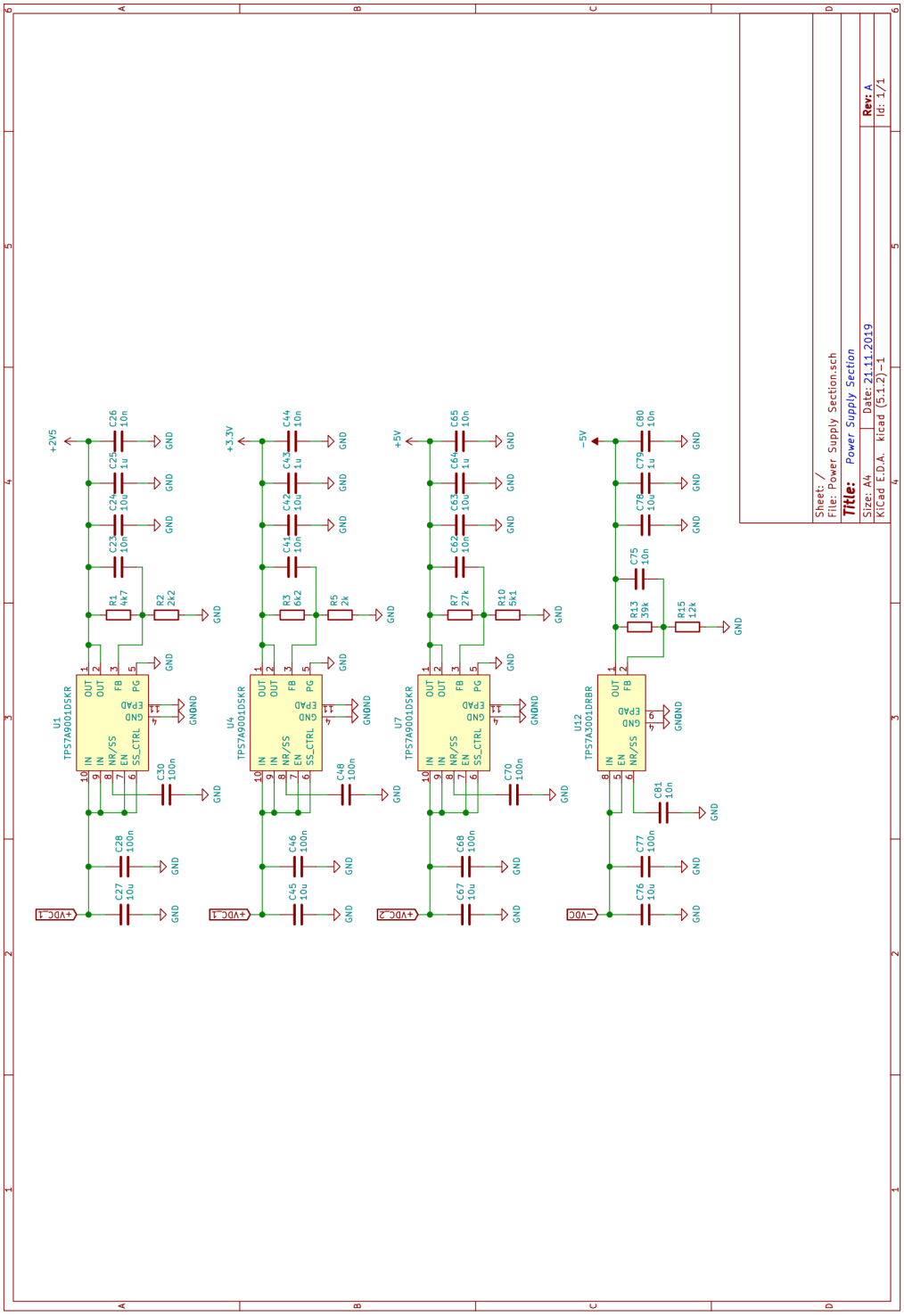

Fig. A.5: Power supply section schematic.

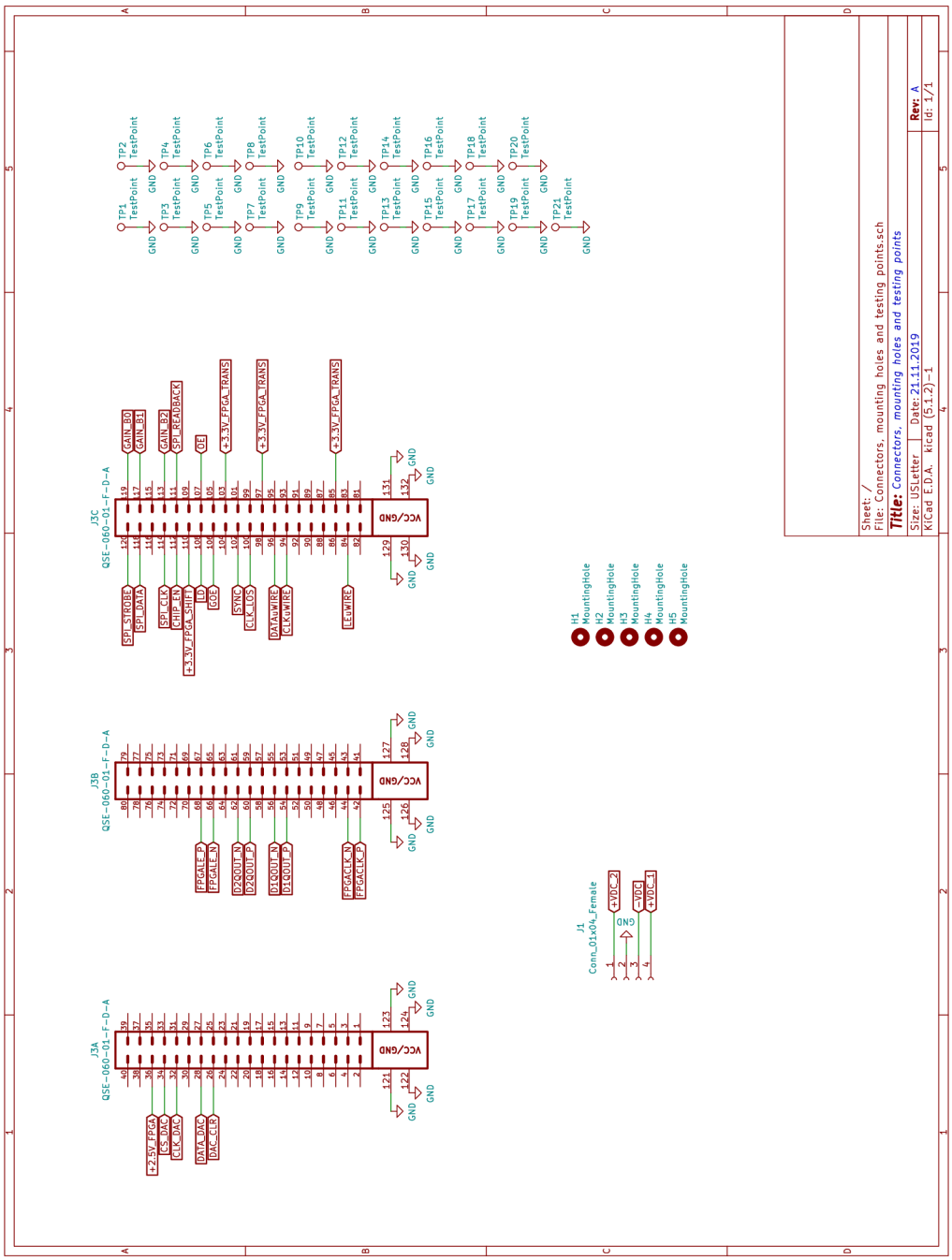

Fig. A.6: Connectors, mounting holes and testing points schematic.

B PCB Layouts

(PCB layouts are depicted on the pages below due to the page resolution reasons).

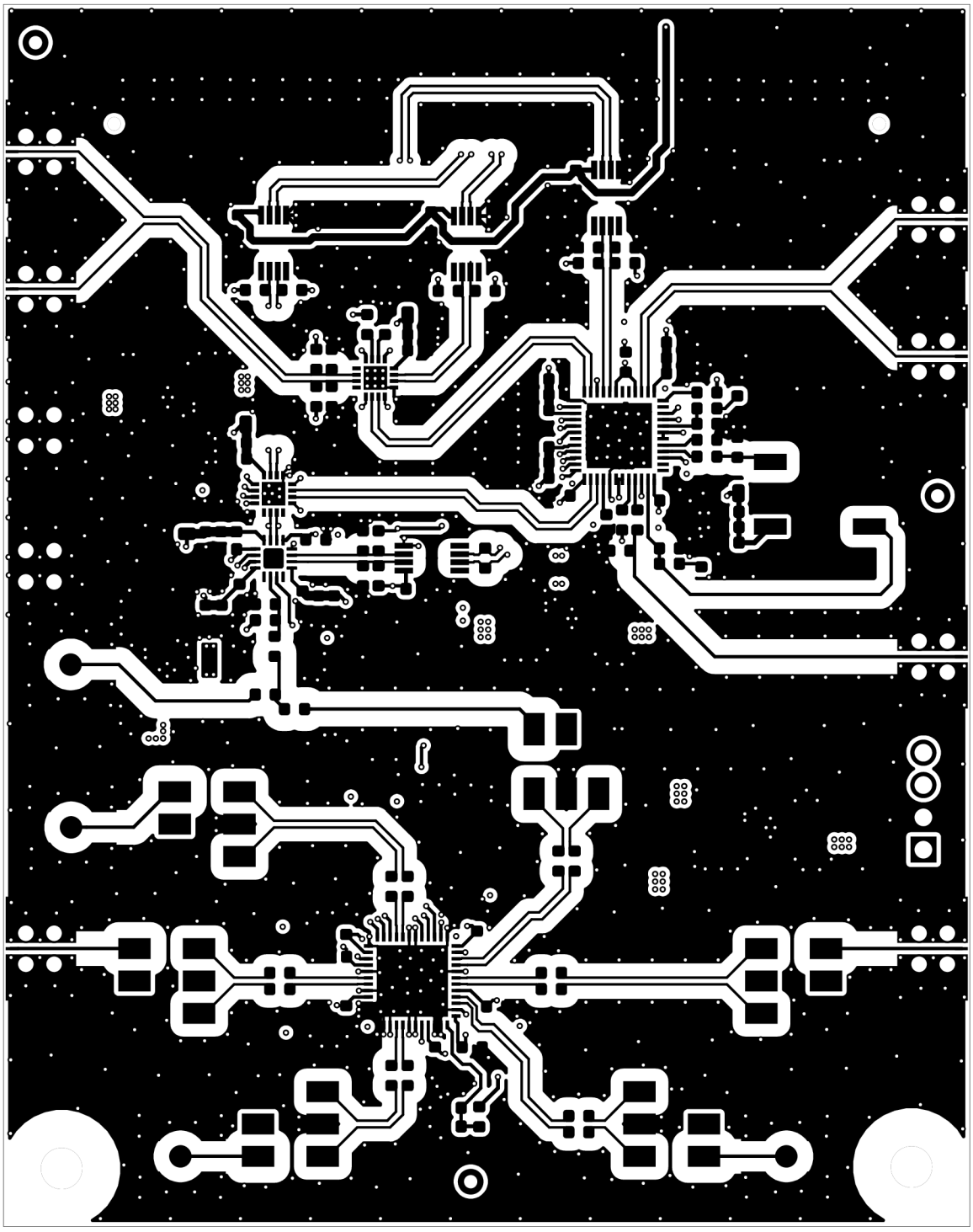

Fig. B.1: Top layer of the PCB (scale 2:1).

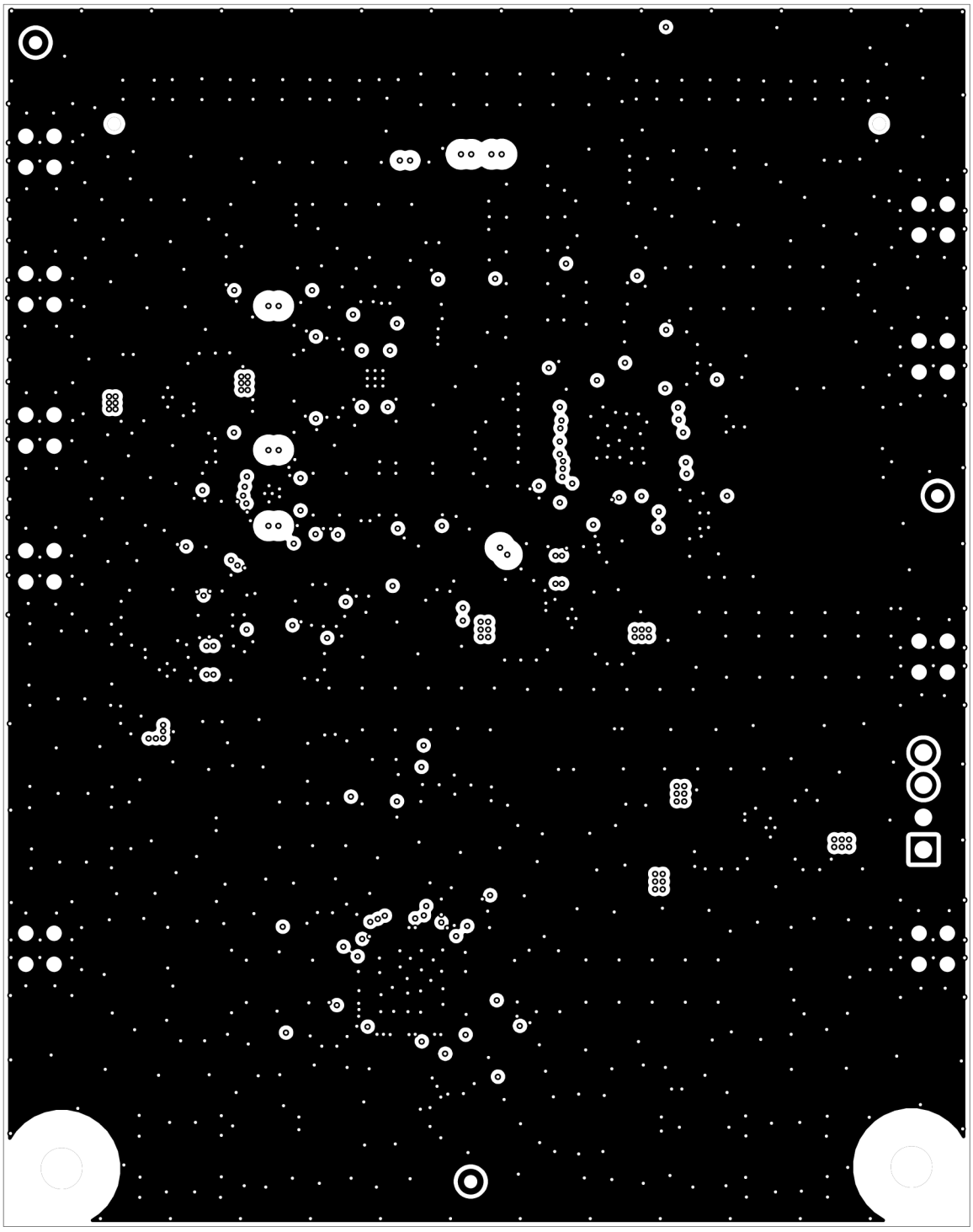

Fig. B.2: Ground layer of the PCB (scale 2:1).

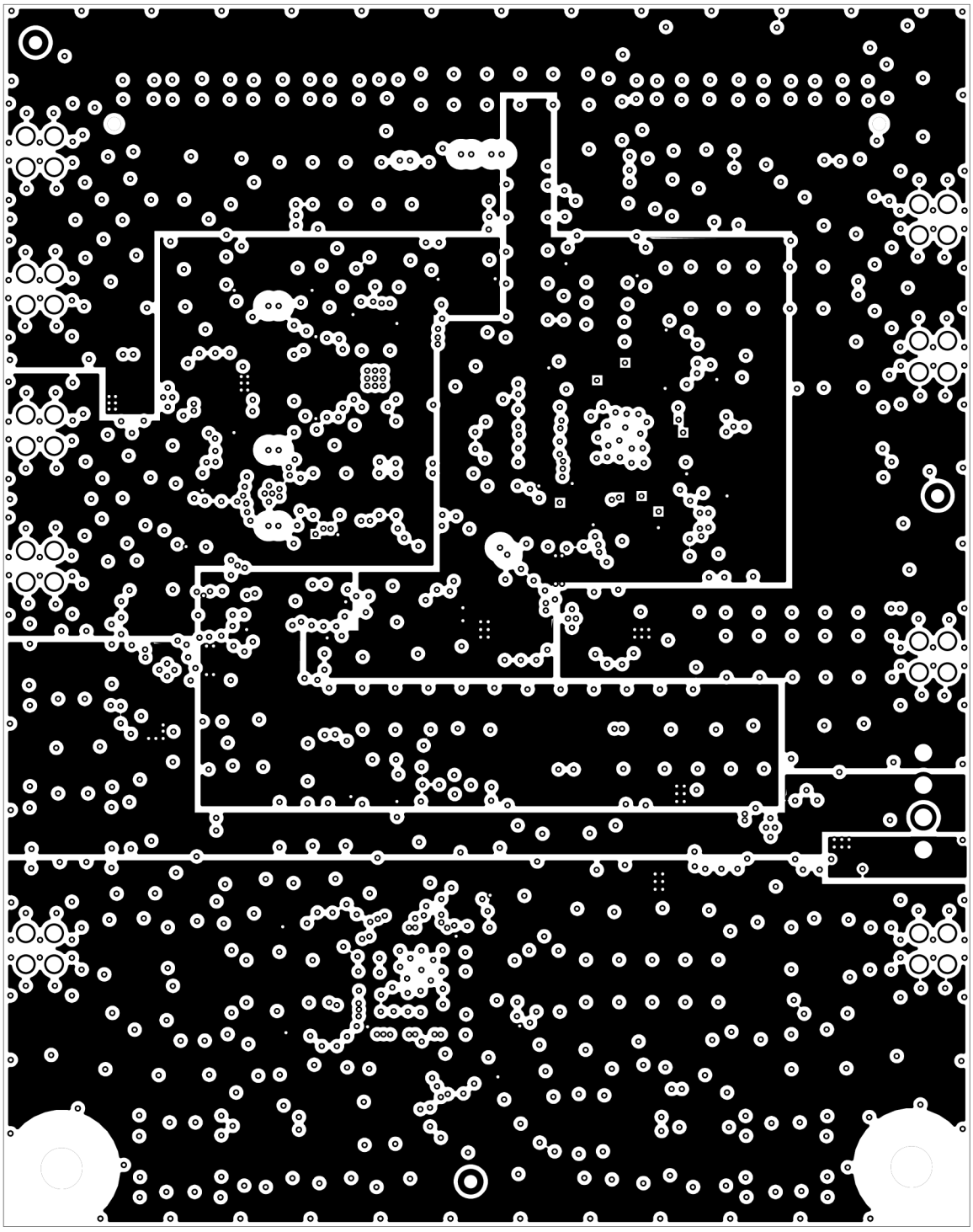

Fig. B.3: Power layer of the PCB (scale 2:1).

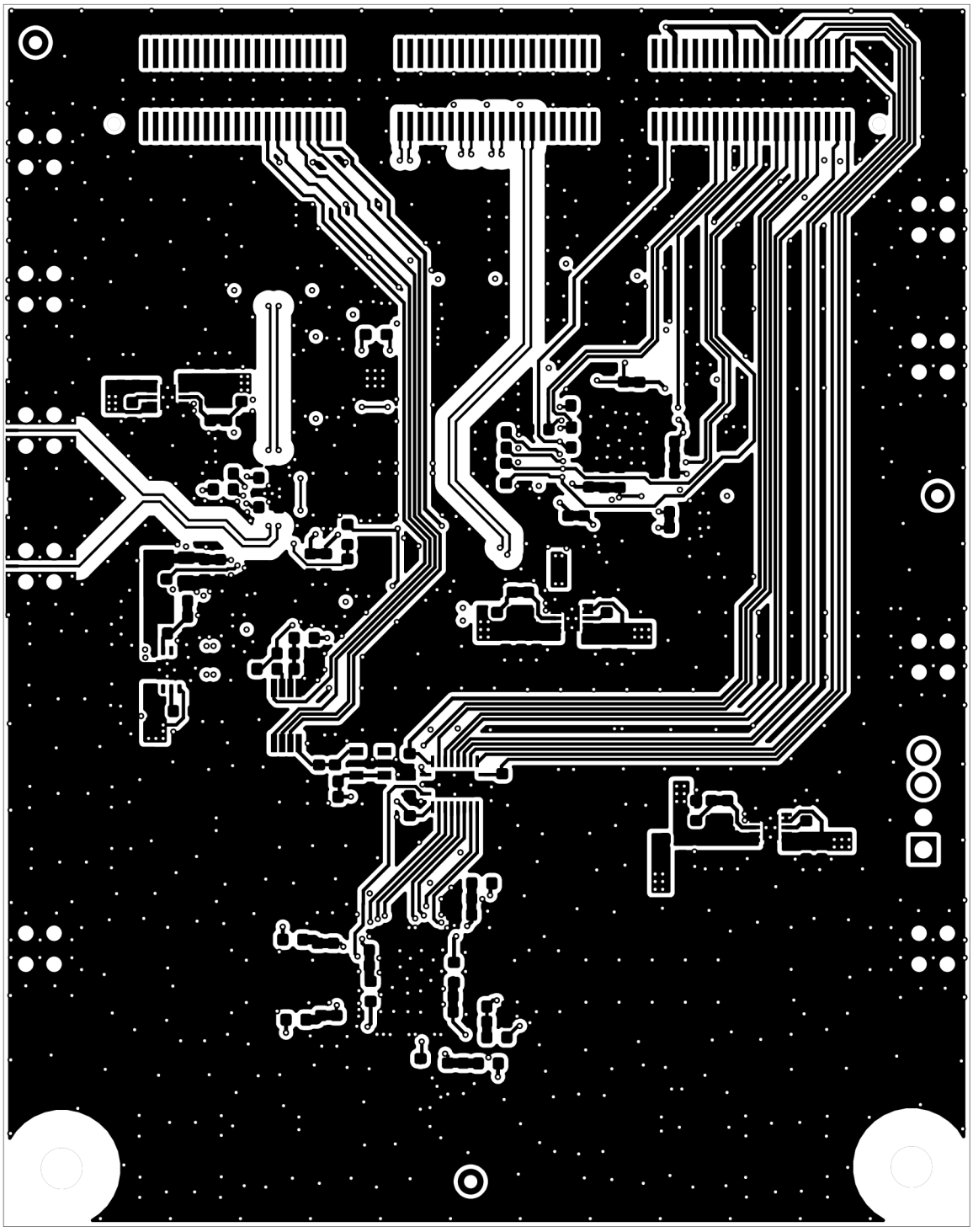

Fig. B.4: Bottom layer of the PCB (scale 2:1).

C Assembly Diagrams

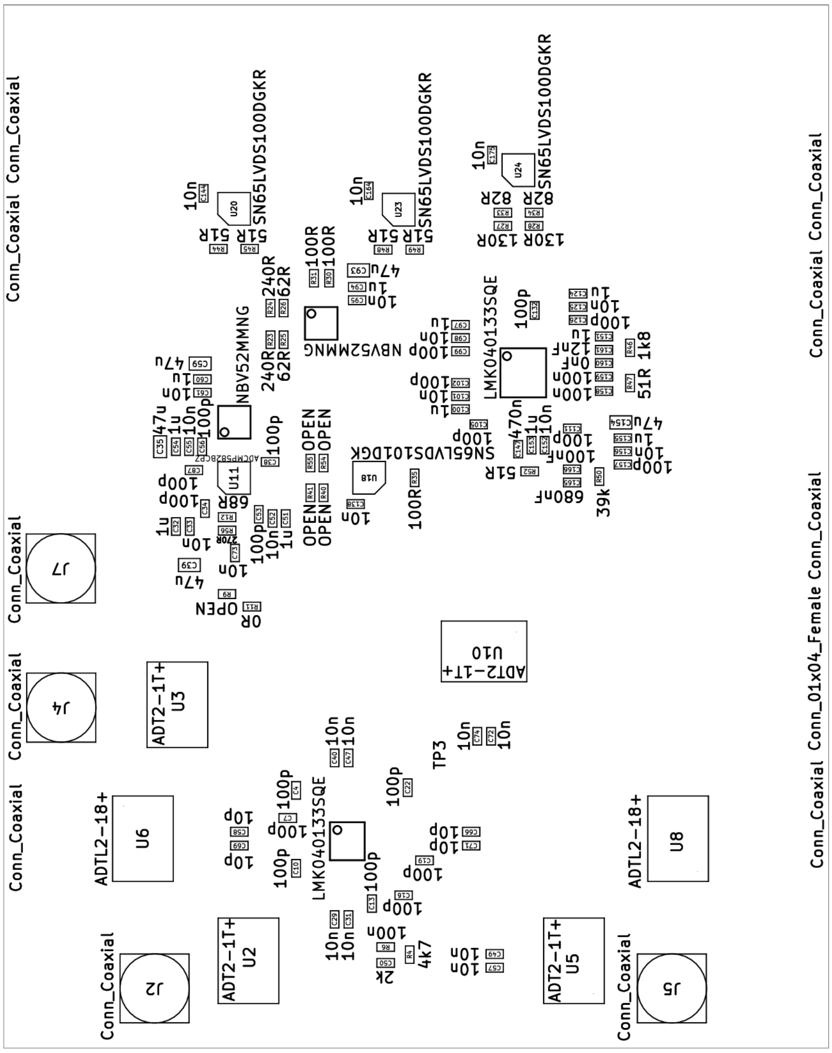

Fig. C.1: Assembly diagram of the Top layer.

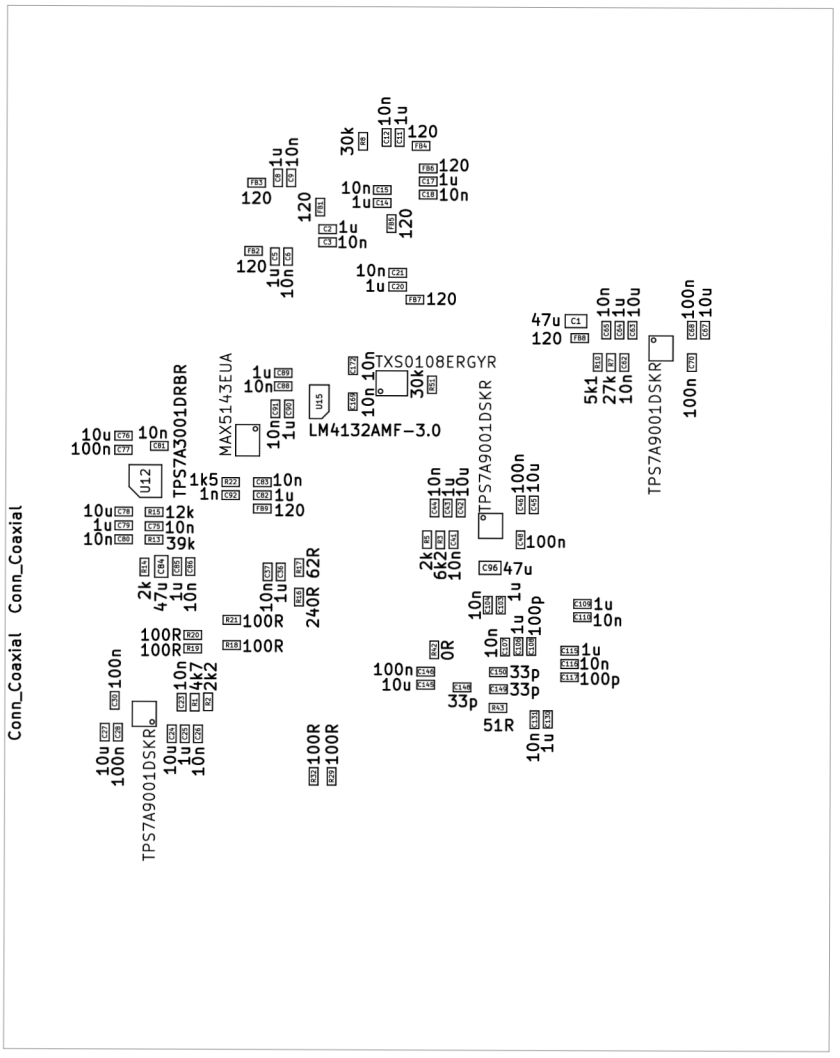

Fig. C.2: Assembly diagram of the Bottom layer.

D Bill of Materials

Qty	Reference	Value	Package	Specification
8	C1, C35, C39, C59, C84, C93, C96, C154	47u	0805	MLCC
32	C2, C5, C8, C11, C14, C17, C20, C25, C32, C36, C43, C51, C54, C60, C64, C79, C82, C85, C88, C90, C94, C97, C100, C103, C106, C109, C115, C124, C130, C151, C153, C155	1u	0603	MLCC
51	C3, C6, C9, C12, C15, C18, C21, C23, C26, C29, C31, C33, C37, C40, C41, C44, C47, C49, C52, C55, C57, C61, C62, C65, C72, C73, C74, C75, C80, C81, C83, C86, C89, C91, C95, C98, C101, C104, C107, C110, C116, C125, C131, C138, C144, C152, C156, C164, C169, C172, C175	10n	0603	MLCC
21	C4, C7, C10, C13, C16, C19, C22, C34, C38, C53, C56, C87, C99, C102, C105, C108, C111, C117, C126, C132, C157	100p	0603	MLCC
9	C24, C27, C42, C45, C63, C67, C76, C78, C145	10u	0603	MLCC
12	C28, C30, C46, C48, C50, C68, C70, C77, C146, C158, C159, C166	100n	0603	MLCC
4	C58, C66, C69, C71	10p	0603	MLCC

Qty	Reference	Value	Package	Specification
1	C92	1n	0603	MLCC
1	C147	470n	0603	MLCC
3	C148, C149, C150	33p	0603	MLCC
1	C160	0nF	0603	MLCC
1	C161	12nF	0603	MLCC
1	C165	680nF	0603	MLCC
9	FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9	120R	0603	Ferrite bead
2	R1, R4	4k7	0603	Resistor
1	R2	2k2	0603	Resistor
1	R3	6k2	0603	Resistor
3	R6, R5, R14	2k	0603	Resistor
1	R7	27k	0603	Resistor
2	R8, R51	30k	0603	Resistor
3	R9, R11, R42	0R	0603	Resistor
1	R10	5k1	0603	Resistor
1	R12	270R	0603	Resistor
7	R43, R44, R45, R47, R48, R49, R52	51R	0603	Resistor
2	R13, R50	39k	0603	Resistor
1	R15	12k	0603	Resistor
3	R16, R23, R24	240R	0603	Resistor
3	R17, R25, R26	62R	0603	Resistor
9	R18, R19, R20, R21, R29, R30, R31, R32, R35	100R	0603	Resistor
1	R22	1k5	0603	Resistor
2	R27, R28	130R	0603	Resistor
2	R33, R34	82R	0603	Resistor
4	R40, R41, R54, R55	OPEN	0603	Resistor
1	R46	1k8	0603	Resistor
1	R56	68R	0603	Resistor
1	J1	282834-4	-	Wire-to-Board connector
4	J2, J4, J5, J7	132134-10	-	Coaxial connector

Qty	Ref.	Value	Package	Specification
1	J3	QSE-060-01-F-D-A	-	Board-to-Board connector
9	J6, J8, J9, J10, J11, J12, J13, J14, J15	901-10510-2	-	Coaxial connector
3	U1, U4, U7	TPS7A9001DSKR	WSON-10	LDO Linear regulator
4	U2, U3, U5, U10	ADT2-1T+	-	RF Balun
2	U6, U8	ADTL2-18+	-	RF Balun
1	U9	TRF371125	VQFN-48	IQ Demodulator
1	U11	ADCMP582BCPZ	LFCSP-16	Analog comparator
1	U12	TPS7A3001DRBR	WSON-8	LDO Linear regulator
2	U13, U17	NB7V52MMNG	QFN-16	D flip-flop
1	U14	TXS0108ERGYR	VQFN-20	Voltage shifter
1	U15	LM4132AMF-3.0	SOT-23-5	Voltage reference
1	U16	MAX5143EUA	UMAX-8	DAC
2	U18, U24	SN65LVDS101DGK	VSSOP-8	Signal translator
2	U20, U23	SN65LVDS100DGKR	VSSOP-8	Signal translator
1	U21	LMK04133SQE	WQFN-48	Jitter cleaner
1	U22	CVHD-950-122.880	-	VCXO

E Firmware File Structure

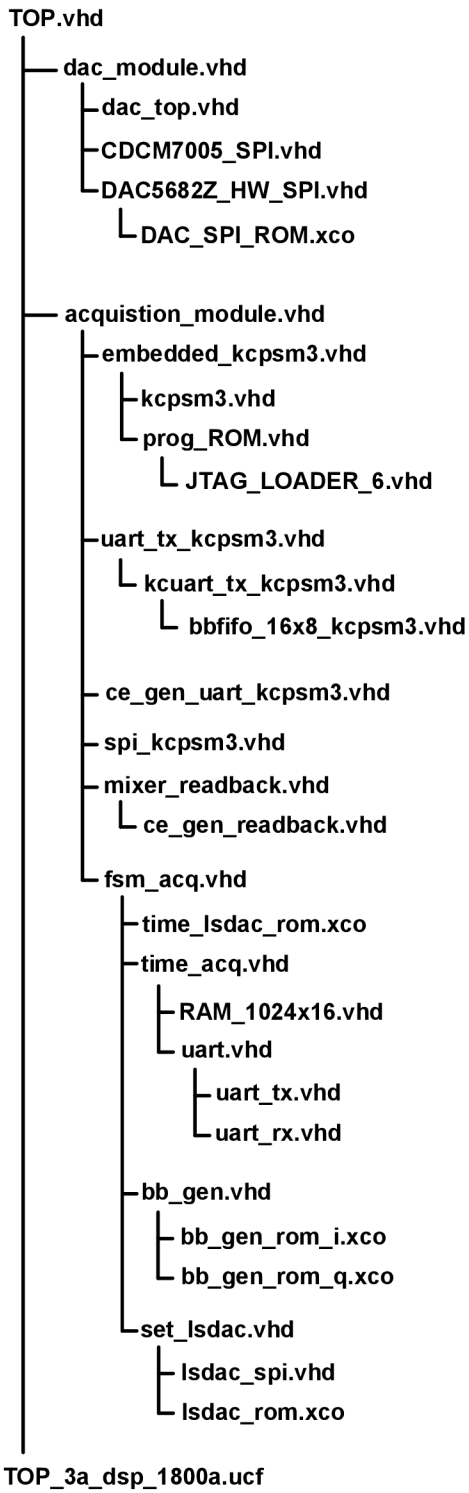

Fig. E.1: FW file structure.

F Register Setup

	LMK04133	**DAC5682ZI**
Register #	**Word (MSB to LSB)**	**Word (MSB to LSB)**
R0	0x01030400	read only
R1	0x010B0101	0x10
R2	0x01530402	0xE0
R3	0x010B0403	0x00
R4	0x01030404	read only
R5	0x00000005	0x82
R6	0x08000076	0xE0
R7	0x00000007	0xFF
R8	0x00000008	0x00
R9	0x00A22A09	0x00
R10	0x2150000A	0x00
R11	0x0065010B	0x00
R12	0xE00C078C	0x00
R13	0x0A04000D	0x00
R14	0x0F63002E	0x00
R15	0x1C80010F	0x00

	CDCM7005	**TRF371125**
Register #	**Word (MSB to LSB)**	**Word (MSB to LSB)**
R0	0x001801F0	read only
R1	0x0000007D	0x0900F319
R2	0xD1450CA2	0xE8704005
R3	0x0000006F	0x2000000D
R4	-	-
R5	-	0x0000555B