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DEPARTMENT OF MICROELECTRONICS

ÚSTAV MIKROELEKTRONIKY

DESIGN OF CHOPPER OPERATIONAL AMPLIFIER WITH INPUT OFFSET REDUCTION IN CMOS TECHNOLOGY

NÁVRH OPERAČNÍHO ZESILOVAČE S POTLAČENÍM VSTUPNÍ NAPĚŤOVÉ NESYMETRIE METODOU CHOPPING V TECHNOLOGII CMOS

MASTER'S THESIS

DIPLOMOVÁ PRÁCE

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VEDOUCÍ PRÁCE

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BRNO FACULTY OF ELECTRICAL
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Master's Thesis

Master's study program **Microelectronics**

Department of Microelectronics

Student:	Bc. Dominik Gaži	*ID:*	203150
Year of study:	2	*Academic year:*	2022/23

TITLE OF THESIS:

Design of chopper operational amplifier with input offset reduction in CMOS technology

INSTRUCTION:

Study the origin of the input offset of an operational amplifier and introduce methods, which reduce this offset. Next, choose a topology which is appropriate for a practical design of an operational amplifier in 0.25 μm CMOS technology. Main focus should be the effective bandwidth of the chopper op-amp, depending on the properties of the processed signal, and the value of the chopping frequency. Design a filter for the output signal demodulation. Evaluate the chopper operational amplifier's input offset reduction ability in feedback loop connection. Use software Cadence Virtuoso for verification of the chopper op-amp's mentioned parameters.

RECOMMENDED LITERATURE:

Podle pokynů vedoucího práce

Date of project specification:	6.2.2023	*Deadline for submission:*	23.5.2023

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doc. Ing. Lukáš Fujcik, Ph.D.
Chair of study program board

Diplomová práce

magisterský navazující studijní program **Mikroelektronika**

Ústav mikroelektroniky

Student: Bc. Dominik Gaži   *ID:* 203150

Ročník: 2   *Akademický rok:* 2022/23

NÁZEV TÉMATU:

Návrh operačního zesilovače s potlačením vstupní napěťové nesymetrie metodou chopping v technologii CMOS

POKYNY PRO VYPRACOVÁNÍ:

Prostudujte problematiku vzniku vstupní napěťové nesymetrie operačního zesilovače a seznamte se s metodami, které se zabývají potlačením této napěťové nesymetrie. Dále zvolte vhodnou topologii operačního zesilovače pro praktický návrh v technologii CMOS 0,25 μm. Zaměřte se především na efektivní šířku pásma chopper operačního zesilovače v závislosti na vlastnostech zpracovávaného signálu a hodnotě chopping kmitočtu. Navrhněte filtr pro demodulaci výstupního signálu. V zapojení chopper operačního zesilovače ve zpětné vazbě zhodnoťte schopnost potlačení vstupní napěťové nesymetrie. V návrhovém prostředí Cadence Virtuoso ověřte simulací výše uvedené parametry chopper operačního zesilovače.

DOPORUČENÁ LITERATURA:

Podle pokynů vedoucího práce

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Vedoucí práce: Ing. Roman Prokop, Ph.D.

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Abstract

The thesis provides the design of a chopper operational amplifier topology focused on correcting input offset. The thesis contains an overview of inaccuracies which occur in op-amps, as well as methods preventing them. Focus of the practical part is designing an op-amp used for amplification and filtering and switches, which are connected into a final circuit and verifying their functionality in simulation environment Cadence Virtuoso. The design is using CMOS 0.25 µm technology.

Keywords

Analogue IC design, operational amplifier, chopping, chopper amplifier, offset, CMOS technology, auto-zeroing, active low-pass filter

Abstrakt

Táto práca sa zaoberá návrhom chopper topológie potláčajúcu vstupnú napäťovú nesymetriu operačného zosilňovača. Práca obsahuje prehľad nepresností vyskytujúcich sa v operačnom zosilňovači ako aj metód ich prevencie. Hlavným cieľom praktickej časti je design operačného zosilňovača, ktorý je použitý na zosilnenie a následne aj útlm a spínačov, ktoré sú použité vo finálnom zapojení a overenie ich funkcie v simulačnom prostredí Cadence Virtuoso. V návrhu bola použitá technológia CMOS 0.25 µm.

Kľúčové slová

Analógový návrh, operačný zosilňovač, chopping, chopper zosilňovač, offset, napäťová nesymetria, technológia CMOS, auto-zeroing, aktívny filter typu dolný priepust

Rozšírený abstrakt

Operačné zosilňovače sú základným stavebným blokom modernej analógovej techniky, a pri neustálej snahe o minimalizáciu plochy a spotreby obvodov sa prirodzene dostávame signálmi na úroveň, kde vnútorná nepresnosť operačného zosilňovača môže ovplyvňovať funkcionalitu aplikácie. Táto práca sa zaoberá návrhom potlačenia vstupnej napäťovej nesymetrie pomocou metódy chopping.

Na začiatku skúmame, čo sú hlavné príčiny vzniku tejto napäťovej nesymetrie (offsetu) a principiálne si vysvetlíme, ako fungujú dve základné metódy eliminácie offsetu – auto-zeroing a chopping. Funkcionalita oboch metód je priblížená aj rovnicami, ktoré znázorňujú vplyvy jednotlivých parametrov obvodu a komponentov na výsledné potlačenie. Chopping je zaujímavou voľbou potlačenia offset hlavne vďaka nepretržitej operácii a taktiež dobrým šumovým vlastnostiam.

Samotná návrhová časť sa skladá z teoretických základov analógovej techniky a popisu stavebných blokov (prúdové zrkadlo, diferenčný pár), na čo plynule nadväzuje praktický návrh dvojstupňového operačného zosilňovača použitého v práci, uvedenie jednotlivých stupňov, rozmerov tranzistorov a odôvodnenie návrhu. Uvedený je aj návrh chopping spínačov. Aktívny filter typu dolný priepust je vybudovaný na takmer identickom obvode ako hlavný OZ s pridanými pasívnymi komponentmi. Predstavu o celkovom zapojení dopĺňajú schémy jednotlivých blokov ako aj zjednodušená schema celého systému. Celý nárh je realizovaný v technológii CMOS 0.25 µm.

Simulácie v návrhovom prostredí Cadence Virtuoso tvoria verifikačnú časť diplomovej práce, kde sa overuje funkcionalita jednotlivých častí obvodu (gm1, gm2) ako aj celého obvodu primárne v zapojení napäťový sledovač. Výstupné grafy znázorňujú výsledky a dopĺňajú vysvetlenie princípu metódy chopping.

Bibliographic citation

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Author's Declaration

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Paper type:	*Master's thesis*
Academic year:	*2022/23*
Topic:	*Design of chopper operational amplifier with input offset reduction in CMOS technology*

I declare that I have written this paper independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the project and listed in the comprehensive bibliography at the end of the project.

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Brno, May 23, 2023

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author's signature

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I would like to express my deepest gratitude to my supervisor Ing. Radek Lang for his countless hours of consultations and for his helpful and easy-to-understand teaching methods. I would also like to thank my family for their emotional support.

Brno, May 23, 2023   ---
                                                                                    Author's signature

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INTRODUCTION

Operational amplifiers are nowadays utilized and relied on in many modern applications. With the constant push to reduce electronics in dimensions and power consumption, and to maximize the efficiency in devices used day-to-day, logically, we are obliged to proceed towards gradually smaller signals that are handled and measured. With smaller signals, however, there arise constantly stricter requirements for precision and error-free operation during the whole lifetime of an application. If we operate in, say, microvolts range, achieving precision in this area involves pushing the means of electronics to its very physical limits, or demands new configurations. Offset is the elementary problem, which is the cause of the inaccuracies occurring in operations with small signals. The focus of this thesis is to resolve, eliminate, or minimalize offset to a marginal degree.

The first chapter describes errors of op-amps, from where offset originates, and what factors contribute to its presence the most.

The second chapter is focused on the most frequent methods used for offset correction. Trimming, auto-zeroing and chopping are described.

The third chapter provides the theory for analogue IC design with a brief overview of basic building blocks.

The fourth chapter is focused on designing the chopper operational amplifier, design's main requirements and solution are provided in this chapter.

The fifth and last chapter supports the design choices by verification done by simulation software. Essential simulations are described and evaluated.

1. OPERATIONAL AMPLIFIER INACCURACIES

1.1 Main types of errors

Operational amplifiers (op-amps) suffer from errors. There exist three major types of errors [1] that occur in op-amps:

- offset,
- drift,
- 1/f noise.

The following figure shows, where these errors occur in the frequency domain.
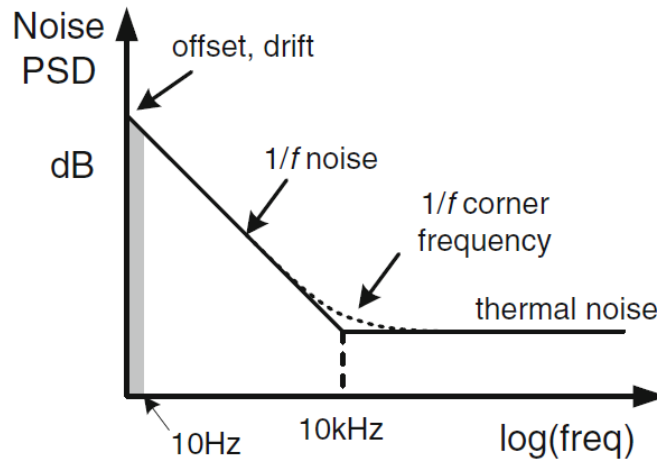
Fig. 1.1   Representation of error occurrences in frequency domain [1]

1.1.1   Offset

Offset is a DC parameter of operational amplifier, which denotes the value of voltage applied at the input of the op-amp so that zero voltage is showing at its output. Most of the time we can indicate offset as a source of DC voltage at one of the amplifier's inputs. Definition of an ideal op-amp asserts that both inputs should be at the same, zero potential when grounded i.e., the potential or voltage difference between the inputs is nonexistent. Naturally, we can conclude from this fact that the offset is an error, which can cause severe inconsistencies and inaccuracies in many applications.

We distinguish three main factors that contribute to the existence of an input offset:

- manufacturing process and drift of the process,
- junction temperature,
- bias point of the internal circuit.

The most prominent of these factors is caused during the transistor manufacturing. Contemporary manufacturing processes and state-of-the-art technological procedures constantly strive to push the limits of size of transistors, however, with gradually smaller dimensions of the devices occurs higher difficulty of keeping the transistors parameters truly identical. It has been observed, that in CMOS technology, the offset of a differential pair can reach as high as 10 mV [2].

Mismatch in CMOS transistors can be caused by multiple sources [3]:
- physical variation of device dimensions,
- metallurgical variation of device parameters,
- electronic parameters of the device.

The first two occurrences mentioned can be minimized by extending the transistor dimensions, however, as with every parameter change in electronics, there comes a trade-off in form of more sizeable area occupied on the chip. More importantly, the physical variation only occurs at the edges of the devices, therefore with the greater size the less impactful the neglection of this mismatch is. Nevertheless, the greatest mismatch is caused by the third source, which can appear in forms of "the trapped charges in the gate oxide, or the surface states in a MOS transistor that can change the threshold voltage of the device [3]." It has been proved that in general, the devices which are more affected by the semiconductor surface properties have greater mismatch than the ones who are more dependent on semiconductor further from the surface. To sum up, there is an inverse proportionality between the transistor's area and mismatch [3].

We can work with a concrete example of a differential pair consisting of two MOS transistors. The gates of the input transistors are connected to an insulator (silicon dioxide) and therefore the difference between the gate currents is close to zero; the input offset between the currents of differential MOS transistors is zero as well. However, MOS transistors have poorer transconductance at the same current values compared to bipolar transistors. This is exhibited in worse input offset voltages and common-mode rejection ratio compared to differential pairs built from bipolar transistors [4].

What is more, offset can also be created internally in the operational amplifier with setting a bias point of the given application. For example, in three-stage comparator we can produce a variable voltage at the cascaded output of the first stage of differential pair created with MOS transistors, which occurs due to a slight inequality of source and sink current, thus generating offset at the input. It will therefore have a value approx. A (gain) times lower than the output voltage imbalance.

1.1.2 Drift

Offset is a static DC error in a defined moment of the op-amp's function. We can easily measure this quantity, provided the measuring equipment has a sensitivity threshold lower than the offset value itself and thus does not introduce any additional error. In comparison, offset drift is the relationship of change of offset with respect to time (dVos/dt). Operational amplifier's offset properties suffer with varying absolute temperature present across the integrated circuit. Temperature can, in fact, pronounce the already existing mismatch between the transistors. Even though the relationship between absolute temperature and offset cannot be denoted in a simple manner, it is safe to say that temperature has an impact on offset drift. In short, "drift is caused by the cross-sensitivity of some error sources to temperature or time [1]". However, estimating its general precise value is redundant, since there exists a dependence on multiple factors such as topology of the circuit, physical placement of transistors and utilized manufacturing technology. According to Analog Devices, offset drift in opamps used for precise application can attain typically 1-10uV/C. However, in some cases only the maximal value of the offset drift is provided, which can introduce further ambiguity into an already imprecise operation.

Moreover, offset exhibits another added change with gradual aging in a square root proportion to the age of the opamp. It is difficult to enumerate the aging effect in a precise quantity, and the closest estimate is in the range of uV/sqrt(month). Operational amplifiers also suffer from gain drift, which can together with offset and temperature drift appear more than problematic in measuring of temperatures, such as thermocouples [1].

2. OFFSET CANCELLATION

Ideally, we want to eliminate all offset inaccuracies from the system. In real word, however, only partial removal of the offset is possible, and even that is effective only up to a certain point, where we enter the territory of ones of uV and encounter noise created not only in our own integrated circuit, but in the whole application as well. Trying to regulate offset beyond this point would be rendered meaningless, since the noise will always interfere with the inputs of operational amplifier, regardless of the imbalance at the output.

2.1 Trimming

The most elementary method of correcting offset used in analog integrated circuit design is trimming. From technological point of view, operational amplifiers are built on a silicon wafer, which can be described as a very thin plate of grown semiconductor substrate, upon which we can further build more complex structures. By numerous manufacturing processes, we can achieve that the behavior of such structures becomes comparable to that of transistors, resistors, or capacitors [6]. Texas Instruments present their method where resistors or capacitors on the wafer have bits of them incinerated, which diminishes the total surface area of the thin plate resistor, thus lowering its resistance or capacitance, respectively [7]. This effect is very desirable in various applications striving to achieve extremely high precision, where passive components are used e.g., differential pairs, current mirrors, voltage references, timing operations or resistor networks.

However, destructive trimming works only in one direction, and that is lowering the value of the passive component. In an environment, where the process drifts both ways from a nominal value, this presents a risk where, tentatively, a resistor with already lower than nominal value should appear on a chip. Two-way trimming essentially works based on adding a resistor network on the chip which can be further adjusted by switching its respective parts to ground or short-circuit them.

Furthermore, trimming is a one-time action employed during the assembly process and serves only as an initial calibration. Its main advantages lie in no necessity for additional components or circuit designs and relatively straightforward application. On the other hand, this method heavily manifests itself in prolonging the manufacturing process, since there is a need for repeating this calibration for every chip individually. On top of that, trimming is simply a nonrecurring method of nulling the offset, therefore we do not account for the drift caused by any of the factors previously mentioned. In a practical example, a brand-new component could be potentially exposed to a heavy

thermal stress directly after being installed, rendering it inaccurate for the whole lifetime, with the aging drift further increasing the offset.

2.2 Auto-correction

From the brief trimming overview, we can clearly see that there arises a necessity for a dynamic and continuous method of adjusting the offset, with an effort to minimize it during the whole life cycle of the component and allowing for as little impact of external factors as possible. The first concepts of auto-correcting amplifiers were introduced as far back as in 1950s, with the name chopping amplifiers [8]. This concept shall not be confused with the chopper amplifiers used today, as the name is the only remnant of its predecessor. Another source [9] supports the fact, that the name chopping amplifier or chopper-stabilized amplifier was used in the first auto-zeroing topologies. In the very beginning of the thesis, we have defined the offset being practically a DC error, in theory comparable to a DC source connected to one of the operational amplifier's inputs. Based on this knowledge, we can assume that the high frequency band is not affected by the offset while passing through the op-amp and the correction shall occur only in the low frequency/dc signal band.

2.2.1 Auto-zeroing method

The pioneering methods of the offset correction by chopping were undeniably ambitious, but due to their shortcomings, many expert engineers were skeptical about the unpredictable behavior they could possibly introduce in their circuits. Hence, the auto-zeroing approach has over time become more favorable method. In fact, chopper-stabilized method is in its very core almost identical to the auto-zero method. The only crucial difference is the connection between the wide-band and stabilizer amplifiers, which is in the latter option executed by interconnection through a nulling input rather than a differential input, resulting in a stable zero over much wider frequency band of operation.

Auto-zeroing offset correction works on the concept of self-stabilizing operational amplifiers by sampling and holding their respective offset values at their outputs, which are then used to oppose the offset during their function. The topology resembles the copper-stabilized method with using the amplifying and nulling amplifier, splitting the input signal in two portions. The main principle can be divided into two stages of operation:

- phase A (auto-zero stage),
- phase B (output or amplifying stage).

Phases are flip-flopping between each other in a frequency given by a system clock. Firstly, it is important we notice the arbitrary offset voltages V_{OSA} and V_{OSB} at the amplifiers' inputs, symbolized by the DC voltage sources. A significant contribution to V_{OSB} is caused by the charge injection due to the switches mismatch. As a rule of

thumb, the auxiliary amplifier's gain should be at least 50 times smaller than the main amplifier's [1].

In the Phase A, as is denoted in the figure, we configure the switching pairs to close Φ_A switches and open Φ_B switches to short the differential inputs of the auxiliary amplifier A_A. Thus, the offset voltage V_{OSA} will be amplified by the internal gain of the opamp A_A at the output, and the sampling capacitor C_{M1} will be charged accordingly to the corresponding output voltage. What is more, since the output is also connected to null the A_A op-amp, the output voltage will combat the input offset with the nulling feedback connection with gain B_A. The outcome of this phase is the auxiliary amplifier with theoretically zero offset voltage (in reality, a negligible offset in order of μVs) appearing at the output. Looking at the main op-amp A_B, regular differential input signal is passing through and gets compensated by the voltage sampled at C_{M2} (which is during the first iteration of the calibrating process theoretically 0 V, or an unknown value).
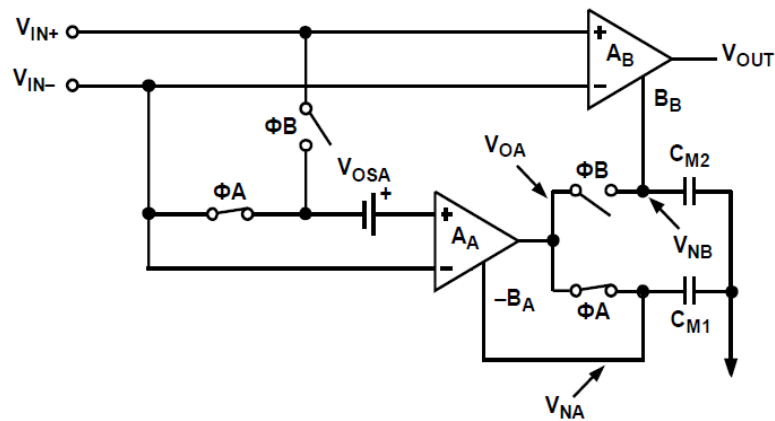
Fig. 2.1　　　Calibration phase of auto-zeroing [10]

Mathematical relations can help us imagine the impact of multiple factors. Time domain expressions for Phase A are as follows:

$$V_{OA}[t] = A_A V_{OSA}[t] - B_A V_{OA}[t] \,, \tag{2.1}$$

which can be reduced to

$$V_{OA}[t] = \frac{A_A V_{OSA}[t]}{1 + B_A}. \tag{2.2}$$

Thus, we can conclude that the nulling voltage of the auxiliary amplifier depends on the internal and nulling gains.

Phase B is when we can finally start using the op-amp for processing the input signal. The inputs of the nulling and main are interconnected together now. Thus, the auxiliary op-amp is still being auto-zeroed by the sampled voltage on C_{M1} capacitor through the nulling pin, therefore we are directly sensing the main amplifier's input offset V_{OSB}, amplifying it with the auxiliary amplifier, and nulling it through the nulling pin V_{NB}. What is more, the feedback loop of the main amplifier will help to maintain the offset in very near proximity of zero. Capacitor C_{M2} stores the voltage and corrects the offset during the next iteration of calibrating Phase A. The capacitors do not have to be in fact external, as Miller capacitances can be effectively used instead [9].
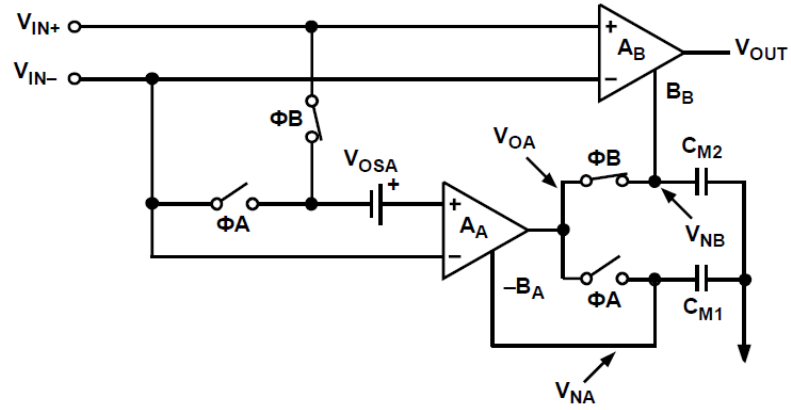
Fig. 2.2   Nulling phase of auto-zeroing [10]

The main op-amp input offset can be denoted as

$$V_{IN} = (V_{IN+} - V_{IN-}).$$

(2.3)

Therefore, the auxiliary amplifier's output is

$$V_{OA}[t] = A_A(V_{IN}[t] - V_{OSA}[t]) - B_A V_{NA}[t].$$

(2.4)

Capacitor C_{M1} cannot be discharged and voltage V_{NA} is equal to value of V_{OA} in the moment when the phases were switched. If the switching period is denoted as ts and the duty phase cycle of the switching clock is 50%, we can express the nulling amp's voltage followingly:

$$V_{NA}[t] = V_{NA}\left[t - \frac{1}{2}t_S\right].$$

(2.5)

To simplify the equations, we can assume that the offset is virtually static, when compared to the autozero clock frequency; we have already established at what rate offset drifts. Followingly, combining the previous equations, we arrive at

$$V_{OA}[t] = A_A\left(V_{IN}[t] + \frac{V_{OSA}}{1 + B_A}\right).$$

(2.6)

As we can see, the auxiliary amplifier greatly reduces its own offset with the nulling input gain. Finally, we can describe the output of the main amplifier:

$$V_{OUT}[t] = A_B(V_{IN}[t] + V_{OSB}) + B_B V_{NB}. \tag{2.7}$$

Since $V_{OA} = V_{NB}$ during the Phase B, we can establish

$$V_{OUT}[t] = A_B V_{IN}[t] + A_B V_{OSB} + B_B \left[A_A \left((V_{IN}[t] + \frac{V_{OSB}}{1 + B_A}) \right) \right]. \tag{2.8}$$

In case of the described op-amps AD855x, the architecture is designed so that $A_A = A_B$; $B_A = B_B$; $B_A \gg 1$ and $A_A B_B \gg A_B$. This allows us to simplify the equation to the following form:

$$V_{OUT}[t] \approx V_{IN}[t] A_A B_A + A_A(V_{OSA} + V_{OSB}). \tag{2.9}$$

We can notice that the product of output and nulling gains of the auxiliary opamp creates a very high open-loop gain in the topology. To relate the gain and the inherent offset, we can start with a generic amplification equation

$$V_{OUT} = k \times (V_{IN} + V_{OS}). \tag{2.10}$$

Adding this term to the previous equation results in

$$V_{OUT}[t] \approx V_{IN}[t] A_A B_A + A_A B_A V_{OS} \tag{2.11}$$

and after minor changes it becomes apparent that

$$V_{OS} \approx \frac{V_{OSA} + V_{OSB}}{B_A}. \tag{2.12}$$

To summarize the mathematical explanation of the topology, we can clearly state that the total offset is, in the specific case of Analog Devices 855x series autozero op-amps, highly dependent on the gain of the auxiliary op-amp. What is more, with the rising gain of this stage, the input offset is decreasing due to the feedback loop. Auto-zeroing is a discrete-time operation since half of the clock cycle is used for calibrating the system, which perfectly matches with switched capacitors circuitry [1]. As was said previously, this method employs sampling and therefore is prone to noise interference and noise folding. "Noise bandwidth is determined by the time constant of the system is usually chosen to be larger than the auto-zeroing frequency, so that the under-sampled noise folds back to DC, increasing the noise PSD at the baseband [1]." The noise folding itself is created by undersampling of the system, it essentially means that we are

increasing the noise power. A very interesting observation can be made; low-frequency noise without auto-zeroing is mostly consisting of 1/f noise, while with auto-zeroing, the white noise from high frequencies starts to dominate the low-frequency signal [1].

2.2.2 Chopping method

The earlier and simpler method, chopping "used switched ac coupling of the input signal and synchronous demodulation of the ac signal to re-establish the dc signal at the output. These amplifiers had limited bandwidth and required post-filtering to remove the large ripple voltages generated by the chopping action [8]." The term 'chopping' has been adopted due to the chopping away from the dc signal (by switching it), thus modulating it into an ac signal [9]. However, since the limitation of the input signal frequency bandwidth was especially unpleasant, a method of chopper-stabilized amplifier was introduced, which greatly improved on this characteristic. Fundamentally, the principle lies in first dividing the incoming signal into two portions of the input frequency band, one portion consisting of high frequencies and the other comprising low frequencies and DC. The AC signal follows a straight path through the main op-amp, while the dc portion passes through the stabilizing op-amp first and then connects to the main op-amp non-inverting terminal, finally creating an inverted output. This topology therefore used the chopper only as an auxiliary amplifier in contrast to the first method, where it was used as the sole component. While achieving satisfying results, employing chopper-stabilized method of nulling the offset was not deficient in its own problems and imperfections [9]. First and foremost, the 'chopping' switches would introduce their own, not negligible noise into the system while switching at high frequencies. "It also causes intermodulation distortion (IMD), which looks like aliasing between the clock signal and the input signal, producing error signals at the sum and difference frequencies [8]." Another one of their faults were voltage spikes at the output, that were still present despite filtering, rendering them almost unusable for high frequency applications. On top of that, switches also could present a potential source of dc offset themselves.

As we have already established, using the chopper method is based on the principle of up-modulating the offset (a DC signal) onto the AC signal, whose frequency is out of the amplifier's bandwidth, and followingly demodulating the offset- and 1/f noise-free signal back into the DC plane. Essentially, the chopping operation is done by two pairs of switches working at the same switching frequency with opposite polarity, which results in switching the op-amp's inputs polarity being swapped every T/2 seconds. It is necessary to mention that there is a need for a low-pass filter at the output stage of every chopping-based method to filter out chopper ripples, the up-modulated offset and noise peaks [1].

The most fundamental approach is basic chopping amplifier, which is using a single operational amplifier with the switching pairs connected to its input and output stage. The topology is simple; the input chopping (CH_{in}) moves the input signal to the odd harmonic of the chopping frequency f_{CHOP}, stage G_{m1} amplifies the signal and the output chopping (CH_{out}) up-modulates the offset and 1/f noise to the odd harmonic of f_{CHOP} too, while bringing the "corrected" portion of signal down to DC. The gain of this chopping method is equal to G_{m1} gain at frequency f_{CHOP}, which is a significant decrease compared to the original DC gain. On the other hand, the offset is modulated by the DC gain of G_{m1}.
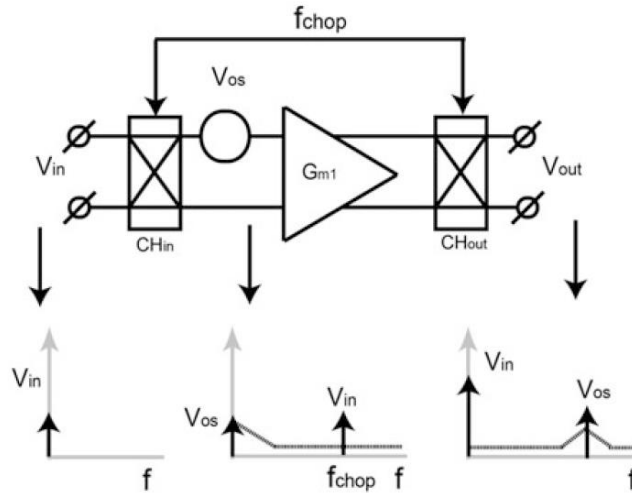

Fig. 2.3   Up-modulation of the offset [1]

To maximize the effective gain of this topology, the chopping frequency should ideally be around 3dB bandwidth of the amplification stage.

However, a more effective result can be achieved by adding one or more stages to the topology to increase gain, one of the examples is by simply adding another stage after the CH_{out}, multiplying the original lower gain by the DC gain of the newly added stage. The additional stages do not introduce any additional noise that will interfere with the operation, as the main source of noise is the input chopper. The origin of the noise is the switches' on-resistance, however, connecting the choppers to high-impedance nodes diminishes it greatly [1]. Already mentioned chopper ripple at the output is filtered by Miller compensation capacities in one or more stages and manifests itself as a triangular ripple with a peak-to-peak amplitude of

$$V_{ripple} = \frac{V_{os} \times G_m}{2C_M \times f_{CH}}.$$
(2.13)

We can deduct from the equation that the output ripple can be suppressed by using higher compensation capacities, higher chopping frequency or by lowering the stage

gain. Compared to auto-zeroing, chopping method is clearly inferior in this aspect of introducing a new portion of signal to the output, where it needs to be filtered. On the other hand, one of chopping's major advantages is in its almost noise-free design, where it does not increase the noise present in the system, unlike auto-zeroing.

2.2.3   Chopper-stabilized method

This kind of processing is used even in modern low-offset operational amplifiers on the market. The signal processed with this technique is split into two bands - high frequency and low frequency paths. High frequency path (HFP) has wider signal bandwidth, whereas low frequency path operates with a narrow bandwidth, higher DC gain and lower offset.
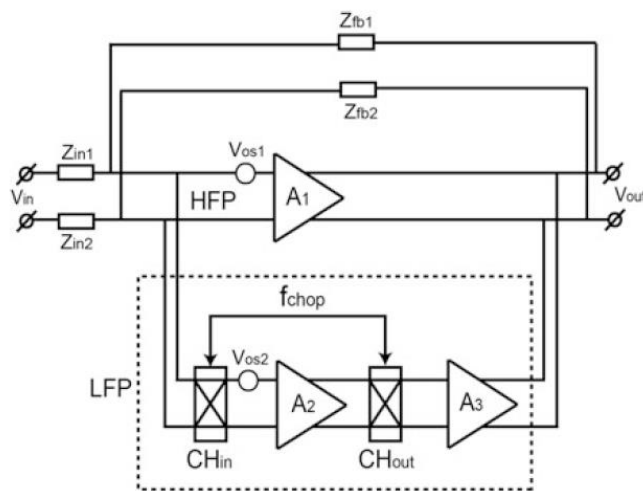

Fig. 2.4   Chopper-stabilized offset reduction topology [1]

The most important factors in this topology are sufficiently high gain of the LFP path and a negative feedback loop in the HFP path. The operation of the offset regulation is then following. Firstly, the input offset of the LFP path is constantly being removed (or up-modulated) by chopping. The input voltage offset difference is amplified by the HFP path and sent back to its input, which is also the LFP path's input. Finally, the LFP amplifying stage, due to its high gain, regulates the offset at the output of the circuit. Total residual offset can be explained as [1]

$$V_{OS} = \frac{V_{OS1} \times A_1}{A_2 \times A_3}.$$

(2.14)

The necessity for a high gain of the LFP is apparent from the formula. Moreover, the 1/f noise is removed with chopper-stabilized technique in the same manner as the offset. Major improvement from the more primitive chopping method is significantly broadening the bandwidth of the operational amplifier while keeping the gain high. On the other hand, this topology has a higher power consumption since there is need for

supplying two or more amplifiers. Separating the signal into two paths also decreases the power efficiency of the circuit. To keep the LFP's bandwidth narrow, we use a low-pass filter. In terms of layout, we might come into complications while designing the filter, as it may take a sizable area of the die, which is resulting in the unfavorable increase of the chip size [1].

3. OPERATIONAL AMPLIFIER DESIGN

In the previous chapter, we describe basic topologies that employ chopping as a means of regulating the input offset of an operational amplifier. From there we can claim that the topology consists of three crucial parts:

- operational amplifier,
- switches,
- low-pass filter.

Each of the parts plays an undeniably important role, which greatly affects the overall result of the design, therefore, it is important that we look at specific challenges which arise with the design of the individual parts and how they influence one another.

3.1 Introduction

Operational amplifier is a component, which has been used in electronics since its first introduction to the public in the late 1960's. Most frequently it serves as a differential-input single-ended output amplifying stage, however, the applications for it are numerous; an op-amp can perform mathematical operations, work as a voltage follower, comparator, or Schmitt trigger. Nowadays, it is the elementary building block for analog integrated circuits.

An ideal model of an operational amplifier has following parameters [12]:

- Infinite open-loop gain $A_V \rightarrow \infty$ dB
- Infinite input resistance $R_{in} \rightarrow \infty$ Ω
- Zero output resistance $R_{out} = 0$ Ω
- Zero differential voltage (offset) at the input $V_{diff} = 0$ V
- No current flows into the operational amplifier $I_{in} = 0$ A
- Unity gain frequency $\rightarrow \infty$ Hz

3.2 Small-signal model

An operational amplifier is built from numerous CMOS transistors and thus, it is important to begin with a small-signal model of a unipolar transistor.
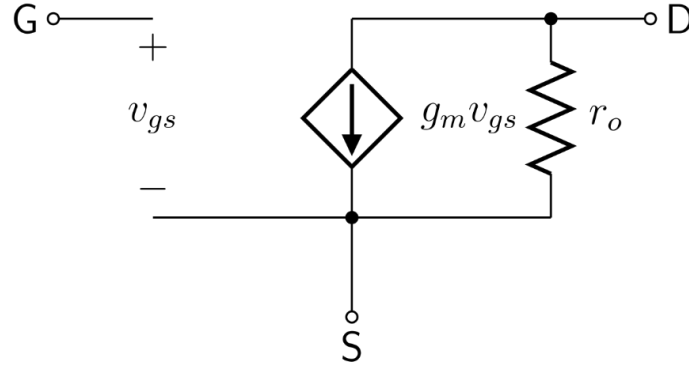

Fig. 3.1   Small-signal model of a MOSFET [11]

The applied input voltage between the gate and source terminals is amplified by the transistor's internal transconductance gm and controls the current I_D between the drain and source i.e., the output resistance r_{DS} of the transistor is dependent on V_{GS}. No current flows between gate and source terminals. To proceed with the opamp design, we must know the basic equations for calculating the operation point of the transistor and biasing it into the saturation region, thus fulfilling the requirement $V_{DS} \geq V_{GS} - V_{TH}$ [13] [14].

Saturation current I_D can be denoted as:

$$I_D = \frac{1}{2} K_P \frac{W}{L} (V_{GS} - V_{TH})^2,$$

(3.1)

where:

- K_P is the transconductance technological parameter,
- W is the width of the transistor's channel,
- L is the length of the transistor's channel,
- V_{GS} is the voltage between gate and source,
- V_{TH} is the threshold voltage of the transistor.

Another important parameter of a transistor is its transconductance gm, which denotes the change of saturation current ID depending on the input voltage VGS while VDS is constant.

$$g_m = \sqrt{2 I_D K_P \frac{W}{L}}.$$

(3.2)

3.3 Current mirror

Current mirror is a basic building block in analogue circuits. Most commonly, they are used as a source of constant current or as a replacement of resistors in form of active load for amplifiers. A simple current mirror (Fig 3.1) consists of two identical transistors that are in saturation mode.
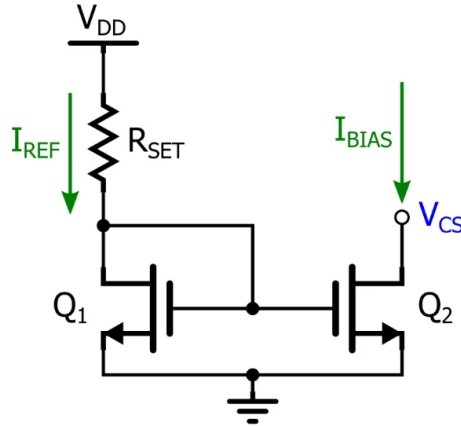

Fig. 3.2   Current mirror principle [17]

Through the transistor Q1, which is in a diode connection, flows referential current I_{REF}. The current sets a given V_{GS1}, which also appears at the gate of the transistor Q2. Thus, both transistors are biased in the same operating point for which following equation applies:

$$\frac{I_{BIAS}}{I_{REF}} = \frac{\left(\frac{W}{L}\right)_{Q2}}{\left(\frac{W}{L}\right)_{Q1}}.$$

(3.3)

The main advantage of this connection is relatively high accuracy of current mirroring with using just two transistors. As is apparent from the formula, we can create various multiples of the referential current by using different W/L ratios in the mirroring transistors. Another advantage is the broad output voltage range, which is only limited by the saturation voltage of transistor Q2. However, basic current mirror can lack in the output resistance

$$r_o = \frac{1}{I_{BIAS} \times \lambda}.$$

(3.4)

For this reason, we use more complex structures, such as cascoded connections [14].

3.4 Differential pair

Differential pair is a building block which allows for amplification of the difference between two input signals while suppressing the common portion of their signals. The topology (Fig 3.2) consists of two transistors M_{DP} and $M_{DP'}$ which have their source electrodes shorted and connected to drain of transistor M_{TAIL}, that serves as a biasing current source. Drains of M_{DP} and $M_{DP'}$ are connected to the active load created by top transistors (M_{P1}, $M_{P1'}$), resulting in high output resistance and therefore also high gain of the amplifying stage. If we consider that V_{GS} of both input transistors is the same, the currents flowing through each transistor is calculated by Kirchoff's law accordingly,
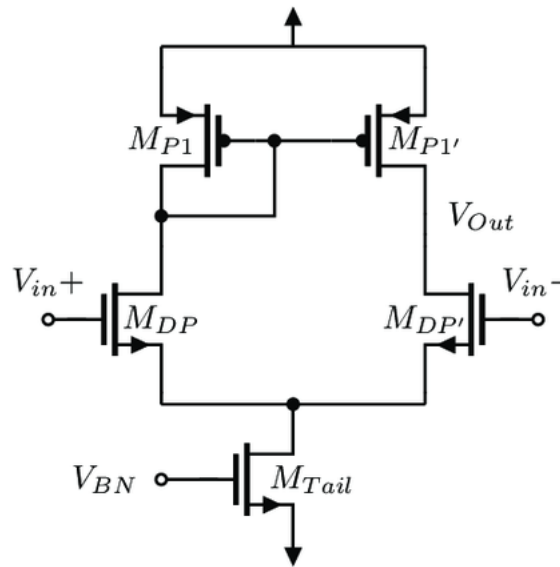
$$I_{TAIL} = I_{MDP} + I_{MDP'} . \tag{3.5}$$

Fig. 3.3   Differential pair with active load [18]

If we increase the input voltage of M_{DP}, the current flowing through the transistor increases too. However, the biasing tail current remains constant, therefore the current $I_{MDP'}$ must decrease, according to the formula 3.x and the transistor is closing. Since I_{MDP} flows also through the active load, and by increasing it, the voltage $V_{GSP1,P1'}$ also increases. Finally, this achieves that the transistor $M_{P1'}$ opens and the current $I_{MDP'}$ is once again increased [14]. The total gain of the stage is

$$A_V = g_m(r_{DSP1'} \parallel r_{DSDP'}). \tag{3.6}$$

3.5 Operational amplifier basic parameters

The aim is to design such an amplifier, which achieves the parameters as close as the ideal ones, although it is impossible.

Open-loop gain (A_V)

Denotes the amplification of different potentials at the op amp's input with no feedback.

$$A_V = \frac{V_{OUT}}{V_{IN}}, \qquad (3.7)$$

$$A_V = 20 \times log_{10} \frac{V_{OUT}}{V_{IN}} \ [dB]. \qquad (3.8)$$

Unity gain frequency (f_T)

Denotes the frequency at which the total amplification of the amplifier in feedback loop is equal to 1 (0 dB) [15].

Slew rate (SR)

Denotes the maximum rate of output voltage change per time unit. It is mostly affected by compensating capacitances or parasitic capacitances of the transistors [14].

Phase margin (PM)

Denotes the absolute value of phase shift of the feedback loop at unity gain frequency.

$$PM = 180° - \Phi, \qquad (3.9)$$

where Φ is phase shift at f_T.

Common-mode rejection ratio (CMRR)

Denotes the ability of the operational amplifier to suppress the common-mode signals at the input. It is expressed as ratio of differential and common-mode gain

$$CMRR = 20 \times log_{10} \frac{A_V}{A_{cm}} \ [dB], \qquad (3.10)$$

where A_{CM} is common-mode gain.

Power supply rejection ratio (PSRR)

Denotes the ability of the operational amplifier to suppress the voltage changes (noise) of the power supply from appearing at the output. It is expressed in a similar fashion to CMRR (equation 3.10).

4. CHOPPER OPERATIONAL AMPLIFIER DESIGN

The design developed for this chopping application is a two-stage operational amplifier consisting of a differential input stage with cascoded amplifying stage. The op-amp is internally self-regulating with a feedback loop using a differential stage, which will be elaborated upon later.

4.1 Requirements

The operational amplifier is an experimental design which can be subject to changes as we proceed further because the surrounding blocks will affect the behaviour of the op-amp itself. Most importantly, the resistive and capacitive load of the output filter is not yet known, but for experimental purpose, the minimal gain bandwidth of the op-amp was determined according to proposed chopping frequency. In the same manner, a value of the capacitive load was given to serve as substitution for a low pass filter, which will be elaborated upon later. Thus, the initial requirements were not highly demanding:

- Open loop gain $A_V > 60$ dB
- GBW > 500 kHz
- Load capacitance $C_L = 4$ pF
- Phase margin > 60º
- Asymmetrical 5.2 V supply voltage

CMOS transistors with 250 nm technology were used for the designing of this operational amplifier. The typical values of the transistors are as follows:

Table   4.1   Typical parameters of transistors used for design

Parameter	NMOS	PMOS
K_P for low V_{DS} (0.1V) [$\mu A/V^2$]	130	35.4
K_P for high V_{DS} (2V) [$\mu A/V^2$]	37.9	13
λ (@ V_{DS} = - 2V, V_{GS} = -1.5V, V_{BS} = 0V)	0.04	0.06
Vth (@ V_{DS} = -0.1V)	0.792	-0.874

4.2 Biasing circuit

The first step of designing an op-amp is determining and setting the current flowing through the branches. Therefore, we create a simplified biasing circuit consisting of an ideal current source and current mirrors. With using a ratio between input and output part of the current mirror, we can create biasing currents which can be used for biasing our op-amp stages. The value of the current provided by the ideal current source is set to 10 µA. In current mirroring, it is a good practice to use a lengthy channel of transistor to

minimize the mismatch of V_{DS} voltages caused by the slope of the $\frac{dV_{GS}}{dV_{DS}}$ curve after the transistor is saturated (value of λ). The output resistance and noise characteristics are improved as well [16]. Thus, the width and length of the biasing transistor have been chosen arbitrarily to put the transistor in saturation and in a way that also allows easy division in the mirroring.

$$V_{DS,sat\,M1} = \sqrt{\frac{2I_D}{K_P \frac{W}{L}}} = \sqrt{\frac{2 \times 10 \times 10^{-6}}{35.4 \times 10^{-6} \times \frac{32}{6}}} \cong 0.1V. \qquad (4.1)$$

The current is then mirrored in three branches in the ratio 2:1, creating a 5 µA current. Thus, the width of the transistors M1, M2 and M3 is half of the current source transistor M1.

Lower transistors (M4-M6) fulfil the function of setting a precise V_{DS} voltage for the operation of the upper, mirroring transistors, which improves the accuracy of the mirror. In this case, it is not necessary to make the length of the transistors gate longer, however, the transconductance of the transistors must be high enough to be able to conduct the maximum 5 µA current in the branch.

$$g_m = \frac{2I_D}{V_{DS,sat}} = \frac{2 \times 10 \times 10^{-6}}{0.2} = 1 \times 10^{-4} = 100 \text{ µS}. \qquad (4.2)$$

By choosing values and optimizing with simulation, we arrive at the ideal W/L ratio,

$$g_m = \sqrt{2I_D \times K_P \times \frac{W}{L}},$$

$$g_m = \sqrt{2 \times 10 \times 10^{-6} \times 35.4 \times 10^{-6} \times \frac{32}{0.8}} = 168 \text{ µS}. \qquad (4.3)$$

In similar fashion, dimensions of M4 and M6 were obtained.

The V_{GS} voltage created at the gates keeps the lower transistors at a V_{DS} that does not cut the upper transistors off the saturation mode.

$$(V_{GS,pbias} - V_{TH})^2 = \sqrt{\frac{2I_D}{K_P \frac{W}{L}}} = \sqrt{\frac{2 \times 10 \times 10^{-6}}{35.4 \times 10^{-6} \times \frac{32}{6}}} \cong 0.1V,$$

$$(V_{GS,pbias} + 0.874) \cong -0.326V$$

$$V_{GS,pbias} = -1.19V \qquad (4.4)$$

Table 4.2   Transistor sizes in biasing circuit

Transistor	W/L [-]	W [µm]	L [µm]
M1	5.33	32	6
M2, M3	2.66	16	6
M6	40	32	0.8
M4, M5	20	16	0.8
M7	4.1	30.4	7.4
M8	0.34	5	15

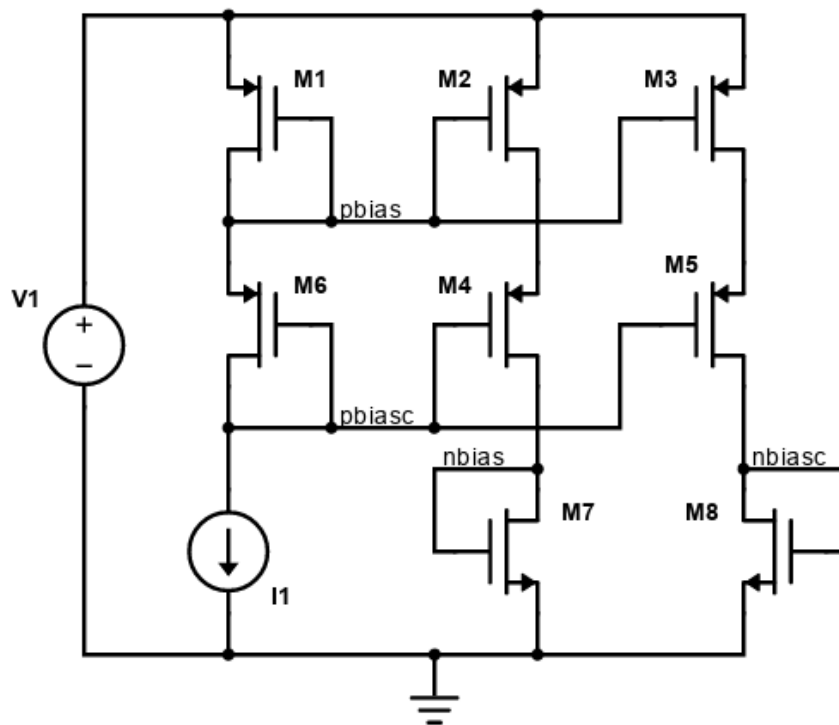
Fig. 4.1   Biasing circuit design

4.3 Differential input stage

For the transistors of the differential pair we choose dimensions as follows. Good practice in analogue design is to keep the channel length at least three times higher than the minimum length possible in the used technology process $L_{min} = 3 \times 600\,nm = 1.8\,\mu m$ for standard maximum Gate voltage ratings [13]. To increase the output resistance of the differential pair further, we chose the channel length to be 7 µm. For a given GBW and C_L we can calculate the minimum transconductance of the differential pair.

$$g_{m1} > GBW \times 2\pi C_L,$$
$$g_{m1} > 500 \times 10^3 \times 2\pi \times 4 \times 10^{-12}, \qquad (4.5)$$
$$g_{m1} > 12.57 \ \mu S.$$

Tail current for the differential pair is 10 uA, based on mirroring the current source from biasing circuit in ratio 1:1. Transcoductance is calculated in 4.5 to be at least 12.5, and the chosen gm is set to be around two times of this value due to increasing gain and ensuring that the manufacturing process will not affect our minimum gain bandwidth. In order to achieve arbitrary gm of approximately 25 μS, we calculate W followingly:

$$\frac{W}{L} = \frac{g_m{}^2}{2I_D \times K_P} = \frac{(25 \times 10^{-6})^2}{2 \times 5 \times 10^{-6} \times 13 \times 10^{-6}} = 4.8,$$
$$W = 4.8 \times 7 \times 10^{-6} \cong 33.7 \ \mu m. \qquad (4.6)$$

The width has then been optimized based on the best simulation results. The output impedance of the differential stage can be calculated followingly:

$$r_o = \frac{1}{I_D \times \lambda} = \frac{1}{10 \times 10^{-6} \times 0.06} \cong 16.67 \ M\Omega. \qquad (4.7)$$

The differential pair has a defined tail current of 10 μA by mirroring the current created in the biasing circuit (M1) with the transistor M9, therefore their channel dimensions must be the same. Transistor M19 is maintaining a constant voltage room for the top transistor.

Table 4.3 Transistor sizes in differential input stage

Transistor	W/L [-]	W [μm]	L [μm]
M22, M23	5.86	41	7
M9	1.33	8	6
M19	40	32	0.8

4.4 Folded cascode

Top pair of transistors (M10, M11) serve as the two current sources which share the bias voltage from the biasing block. The width of their channels is half to deliver halved value of the original current source.

From the formula used in equation 4.2, we can calculate that the g_m of the pair of transistors M26 and M27 should be at least 50 μS. The dimensions were therefore chosen to create two times higher transconductance, in case of all the current flowing

through the one branch and that the V_{GS} change is small enough not to push cascoded transistors M10, M11, M30 and M31 to linear region.

$$g_m = \sqrt{2I_D \times K_P \times \frac{W}{L}} = \sqrt{2 \times 5 \times 10^{-6} \times 35.4 \times 10^{-6} \times \frac{32}{1}} \qquad (4.8)$$

$$g_m = 106.43\ \mu S.$$

Their transconductance is relatively high, because it manifests itself the most in the total gain of the cascode.

Bottom transistors M30 and M31 of the cascode must be able to sink current flowing both from the differential stage and the top cascode current source,

$$I_D = I_{D,diff} + I_{D,casc} = 15\ \mu A. \qquad (4.9)$$

The transistors are biased by another differential pair's output, which senses the differential voltage at the output of the cascode and sets a common mode output voltage.

Table 4.4   Transistor sizes in folded cascode amplifying stage

Transistor	W/L [-]	W [μm]	L [μm]
M10, M11	4	24	6
M26, M27	32	32	1
M30, M31	8.2	60.8	7.4

4.5 Differential biasing feedback pair

We have established in the previous subchapter that the bottom transistors of folded cascode need low V_{GS} of approx. 1 V. The output of the differential pair has the same voltage, as it is shorted with their gates.

This stage only serves the purpose of keeping the common mode cascode output voltage at around $V_{dd}/2 = 2.6$ V. Thus, the V_{GS} of the transistor M24 and M25 is calculated

$$V_{GS} = 2.6 - 1 \cong 1.6\ V. \qquad (4.10)$$

The tail current of 5 μA is set by the current source M32 and the g_m of M24 and M25 can be defined. It is important to remember that this stage is not used as an

amplifier, hence we choose low W/L ratio to keep the transconductance and gain low and V_{GS} high enough to keep our desired value.

Based on the formula used in equation 4.2, the transconductance of the transistors in differential pair is

$$g_m = \sqrt{2 \times 5 \times 10^{-6} \times 37.9 \times 10^{-6} \times \frac{0.6}{4}} = 5.33 \ \mu S. \tag{4.11}$$

Table   4.5   Transistor sizes in differential biasing feedback stage

Transistor	W/L [-]	W [μm]	L [μm]
M24, M25	1.5	0.6	0.4
M27	4.1	30.4	7.4
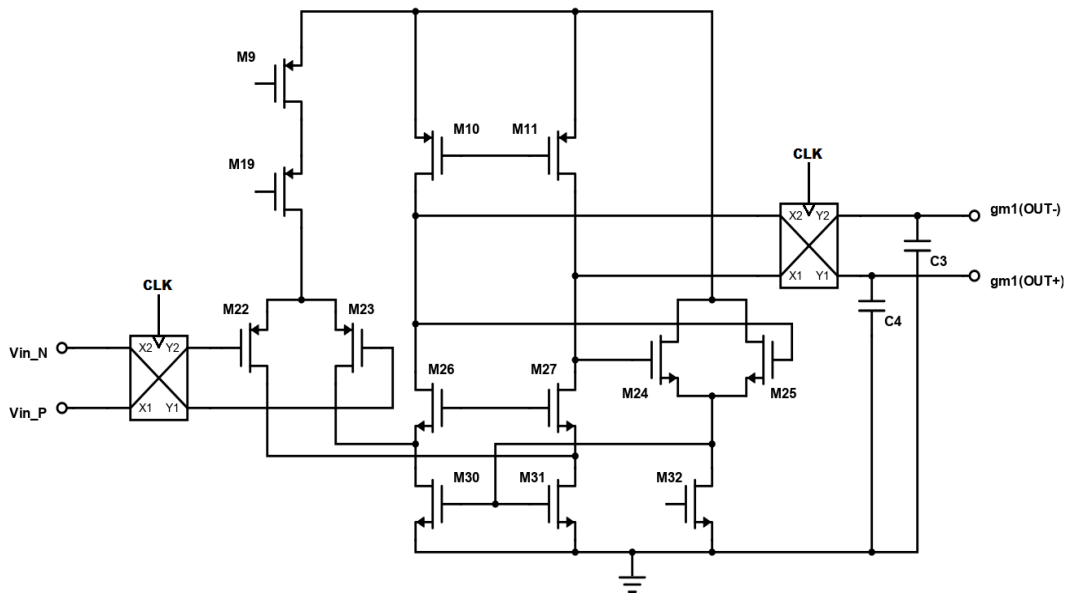
Fig. 4.2   Operational amplifier design

4.6 Charge injection compensation in switches

The final offset of the regulating amplifier depends mainly on the charge injection asymmetry and clock feed-through [1]. There exist multiple methods on how to limit these two effects, which are caused by the switches. First of the methods is using dummy switches, which compensate the charge injection of the main switches by using a complementary signal to the one used by choppers. The lower the mismatch between the injections of main and dummy switches, the more effective is the charge injection

"sinking"; ideally, we would want to achieve an equal distribution of charge between the source and drain of the main switch, which is impossible, and thus this approach is not an attractive one. A more advanced method is to use complementary switches, where NMOS and PMOS opposite polarity charge carriers work against each other resulting in recombination. The downside to this technique is that it can effectively work only in the range of the input signal being the half of the supply voltage. Using a fully differential circuit, we can avoid most of the previous complications, as the manifested mismatch in charge injection only appears at the common voltage output. It has been observed that with this method, we can reduce the residual chopping offset by at least tenfold [1].

4.7 Chopping switches

Switches fulfil the main function of the chopping introduced in the system – interchanging the input and output branches of the op-amp. Their function is also to modulate the offset from DC to certain harmonics based on switching frequency. The choice for the switches is based on the basic rules of analog design; choosing MOS transistors with smallest width and length possible in the technological process used for this thesis gives us the smallest parasitic capacitances of the transistors, which is beneficial both for increasing the switching speed and keeping the charge injection and clock feedthrough as low as possible. The topology for switches is transmission gate, a parallel connection of N-type and P-type transistors controlled with complementary clocks which enables us to efficiently switch a wide voltage range.

There exist multiple options for positioning the switches in chopping amplifiers, depending on the desired functionality. The position we have chosen is at the input of the differential pair and at the cascode differential output. This configuration does not allow for a wide swing at the output, but the local feedback differential pair creating a common voltage for the cascode in the main op-amp is already limiting the swing of V_{OUT}, thus there is no need to be concerned with this disadvantage. The switch placed directly at the output can cause charge injection, as will become apparent later.
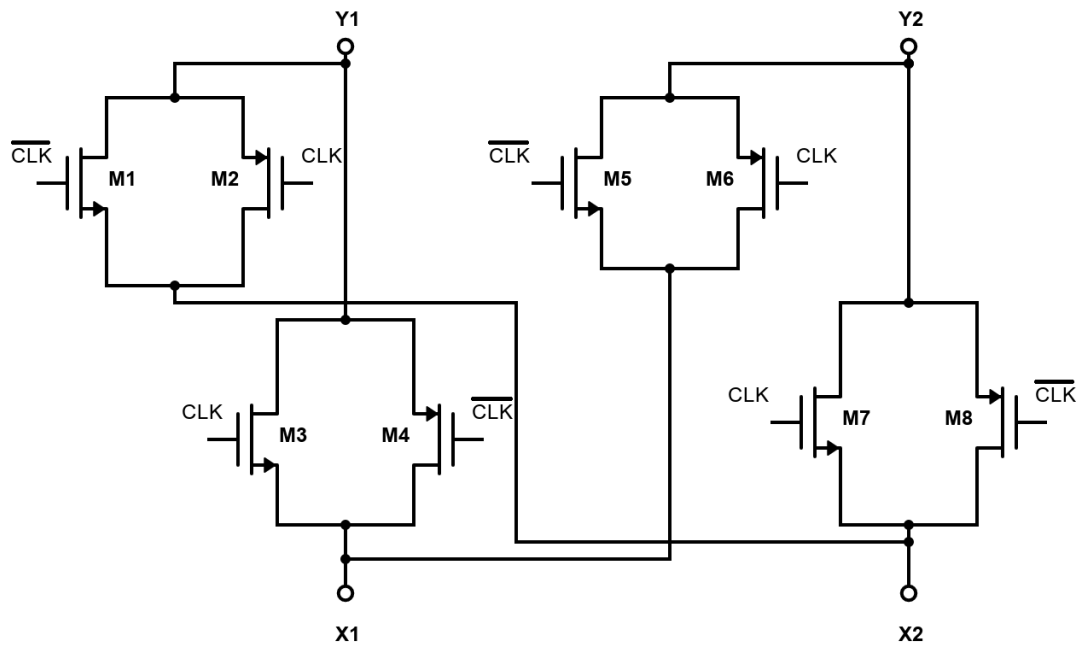
Fig. 4.3　Internal connection of chopper switch

Table　4.6　Transistor sizes in chopper switches

Transistor	W/L [-]	W [μm]	L [μm]
M1-M8	1	0.6	0.6

4.8　Output filter design

The output signal of the operational amplifier with the chopping operation applied results in a triangular wave superimposed on the common mode voltage which is approximately $V_{DD}/2$. Granted, in case of no input offset, only spikes introduced by chopper switches will be added to the output signal.

Therefore, there is a need for an output filter to demodulate the output of the op-amp (filter out the modulated offset altered by chopping) and further attenuate the ripple and filter out the spikes from the output signal. Most important to notice are capacitances inside the op-amp; we use capacitor C1 with R1 to set up a bandwidth of the filter and another added capacitance is a Miller capacitor C5 between the two gain stages of the filter further lowering the gain bandwidth and stabilizes the system.
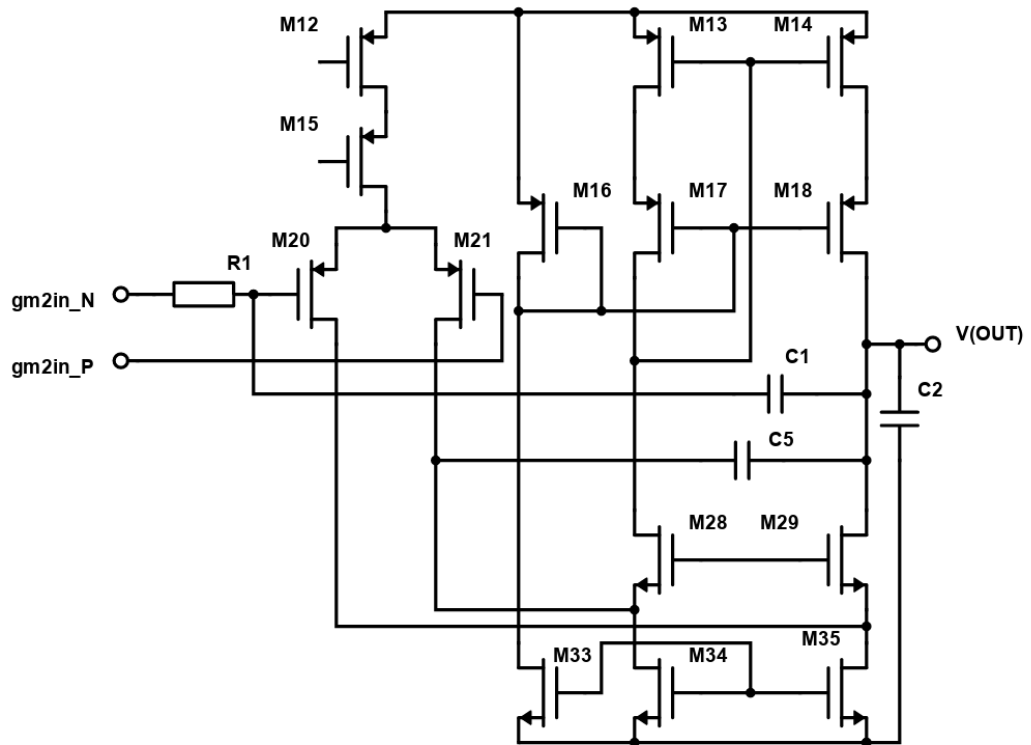
Fig. 4.4   Active low-pass filter design

Table   4.7   Transistor sizes in active low-pass filter

Transistor	W/L [-]	W [μm]	L [μm]
M12	0.67	4	6
M15	5	4	0.8
M20, M21	5.86	41	7
M16	0.5	6	12
M13, M14	2.67	16	6
M17, M18, M28, M29	32	32	1
M33, M34, M35	2.05	15.2	7.4

Table   4.8   Component values in active low-pass filter

Component	Value
C1	20 pF
C2	8 pF
C5	4 pF
R1	1 MΩ

4.9 System topology

In the figure 4.4 we can see the principial idea of the system's topology. The configuration consists of the main op-amp (gm1) with offset being chopped by the switches on its differential inputs and outputs and followingly filtered by an active low-pass filter (gm2).
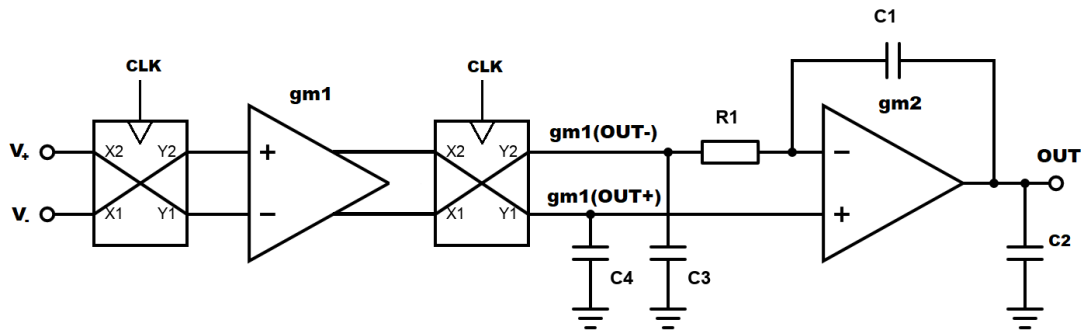
Fig. 4.5   Simplified diagram of the system

The output signal should ideally be offset-free; however, the offset will only be suppressed to a certain extent. Individual stages have been designed with certain requirements for the system's functionality. The choice of chopping frequency is mainly dependent on finding the balance of being higher than the system's bandwidth and achieving an adequate attenuation by the low-pass filter (gm2). It also must be as low as possible to limit the charge injection to the circuit. Another requirement for choosing a chopping frequency is to be higher than the corner frequency of 1/f noise, which in our case $f_c \approx 10$ kHz. Thus, a chopping frequency of 700 kHz has been chosen. The operational amplifier is using a differential input stage and followed by folded cascode with load capacitances C3, C4 of 5 pF to limit the slew rate of the gm1 stage and further limits the system's bandwidth.

The design choice for gm2 stage is an active low pass filter built upon a similar topology which was used for gm1 stage of the system, with several changes which creates a possibility to enclose the feedback loop or to drive another connected circuitry. The dimensions for the transistors were derived in a similar fashion and the folded cascode output is single ended. Filter must have high enough DC gain for biasing the main op-amp to the referential voltage in voltage follower configuration and the attenuation at the chopping frequency must be sufficient to suppress the amplified offset. R1 and C1 create the low-pass filter at gm2 stage with a given gain and cut-off frequency. C2 at the output is smoothing the residual offset ripple. By subsequential simulations, the parameters of the surrounding components have been adjusted to provide the best results while taking the final area taken by the circuit on the chip into

consideration. This is also the main limitation in the resulting offset suppression; increasing attenuation of the filter to lower residual offset takes bigger area as a trade-off.

With the addition of the filter, the DC gain of the whole system naturally rises, which creates higher requirement for stability. Firstly, the current I_D used in gm1 had to be decreased from the original 10μA used in calculations to new value of 2.5 μA, altering the frequency response of the main operational amplifier, lowering the gain of both amplifying and filtering stages. This affects the calculated values and transistor dimensions provided in chapter 4. The change also decreased slew rate (equation 4.13) that means lower triangular wave's magnitude, which then requires lower attenuation from the filter at the chopping frequency. The DC gain of gm1 stage has been chosen so that it amplifies the offset with sufficient gain of 59 dB.

$$\text{SR} = \frac{I_D}{C} = \frac{2.5 \ \mu A}{5 \ pF} = 0.5 \ V/\mu s. \tag{4.12}$$

5. SIMULATIONS

The performance of the designed chopped operational amplifier can be verified by simulations done in Cadence Virtuoso environment.

5.1 Frequency analysis

Frequency analysis is an essential simulation determining operational amplifier's and low-pass filter's basic parameters, which have already been mentioned in section 3.5.
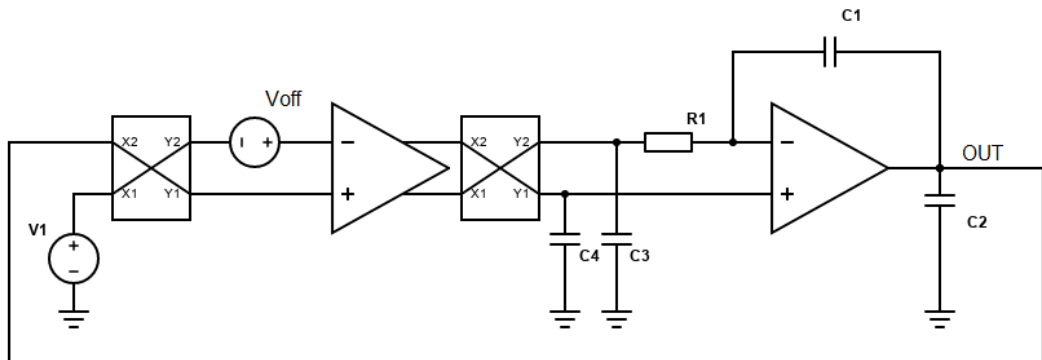

Fig. 5.1   Schematic of circuit setup for simulation – voltage follower

5.1.1 Operational amplifier

Simulation settings:

- Range: 10 Hz – 10 MHz
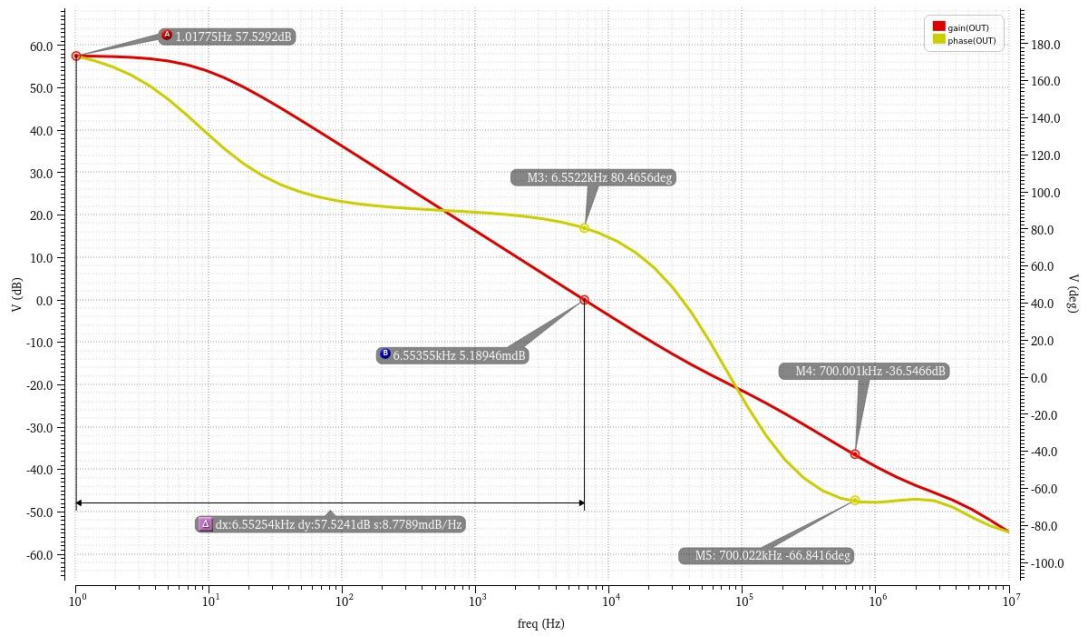- Closed-loop connection (voltage follower)
- $V^+ = 1$ V
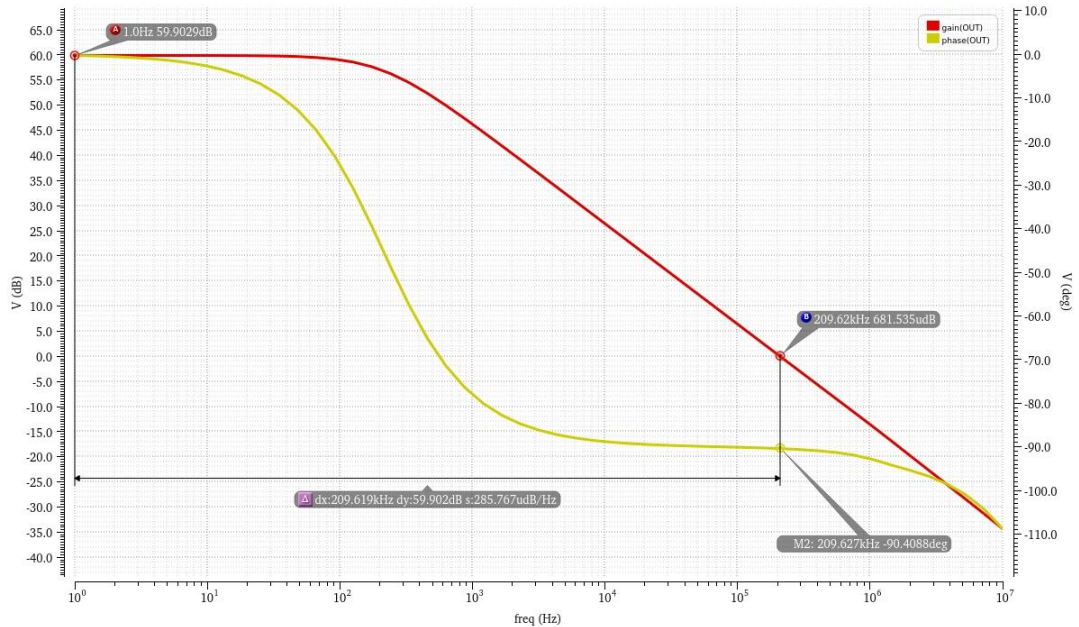
Fig. 5.2   Frequency analysis of the operational amplifier

The resulting graph provides us with following parameters:

- DC gain = 59.9 dB
- Unity gain frequency $f_T = 209$ kHz
- GBW = 209 kHz
- Phase shift = -90 º

5.1.2 Active low-pass filter

Simulation settings:

- Range: 10 Hz – 10 MHz
- Closed-loop connection (voltage follower)
- $V^+ = 1$ V

Fig. 5.3   Frequency analysis of the active low-pass filter

The resulting graph provides us with following parameters:

- DC gain = 57.5 dB
- Unity gain frequency f_T = 6.55 kHz
- Phase margin PM = 80 º
- Attenuation at the chopping frequency -36.5 dB

5.1.3 Stability of the closed loop analysis (STB)

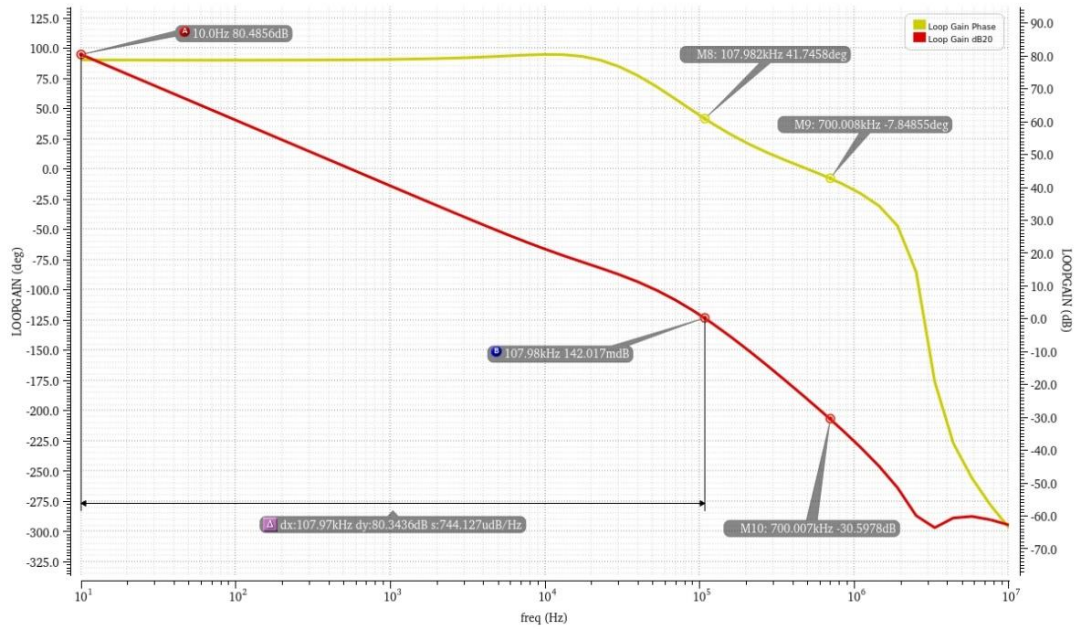To verify whether the designed system is stable, the phase margin in closed loop at 0 dB gain must be higher than 0º.

Fig. 5.4   Stability analysis of the system

We can observe that the system is stable with a phase margin higher than 40º.

5.2 Transitional analysis

This set of simulations shows and verifies modulation of the offset as well as the functionality of the circuit. The results were captured near the end of the simulation, as the currents have settled into equilibrium, all capacitances have been charged and the system begins to function properly.
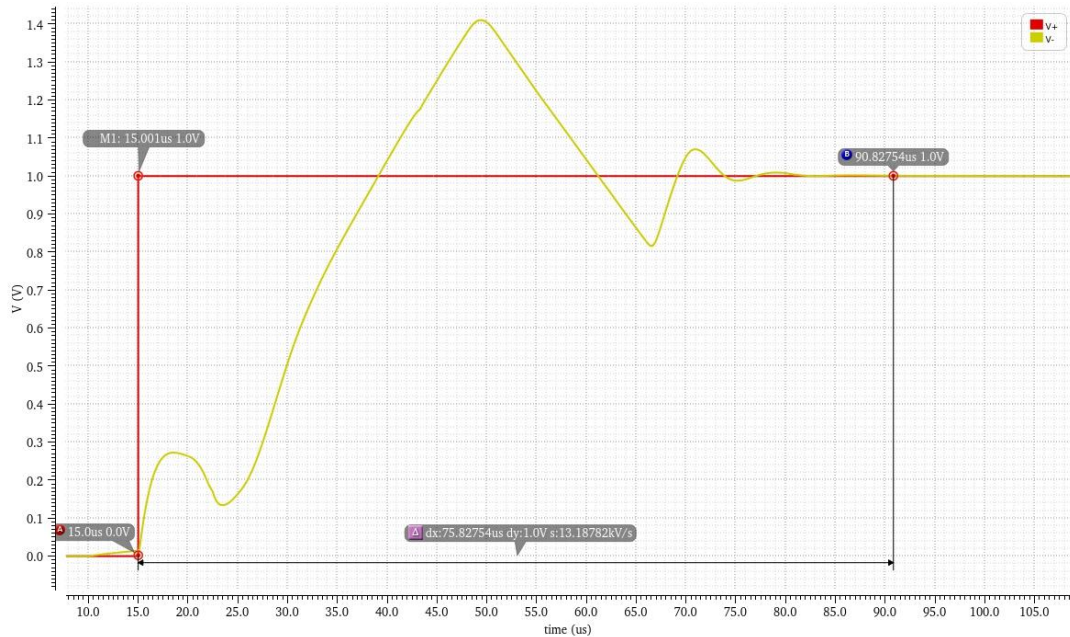
5.2.1 Transient step response

Fig. 5.5   Step response of the system

The resulting graph shows the system's step response in a voltage follower connection. The step rises from 0 to 1 V and the step's rise time is 1 ns. We can see that the system's response is stable, with the time necessary to regulate itself onto the new input value corresponding to around 75 µs.

5.2.2 Operational amplifier's output after switches

Simulation settings:
- Duration: 600 µs
- Voltage follower connection
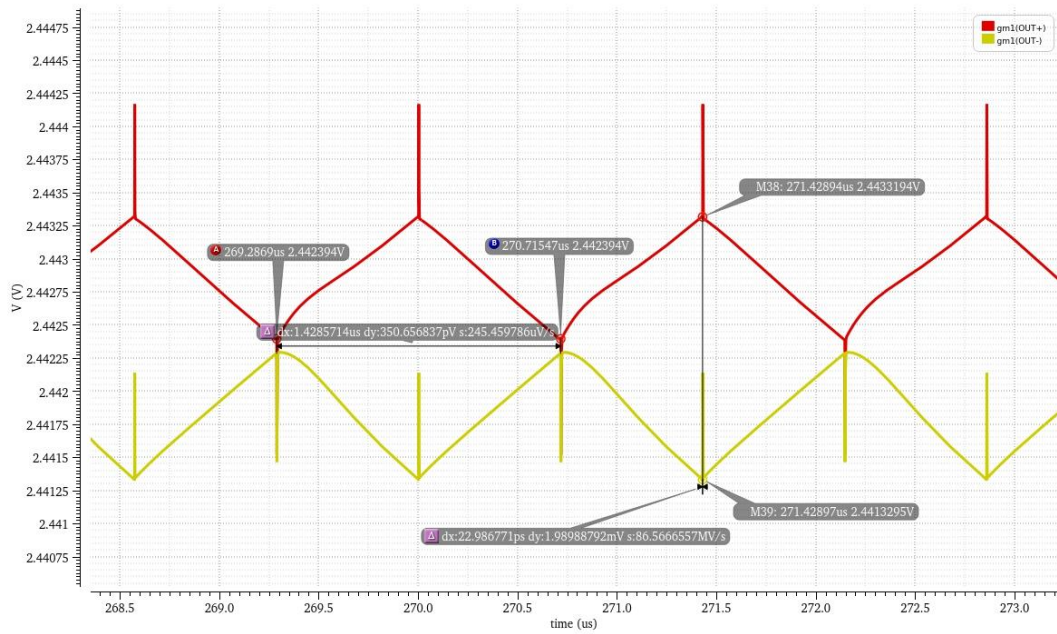- $V^+ = 1$ V
- $f_{chop} = 700$ kHz
- $V_{off} = 1$ mV

Fig. 5.6 Modulation of the offset

The switching of non-ideal switches realized as MOSFET transmission gates at a certain frequency introduces charge injections and clock feedthrough to our circuit.

5.2.3 Chopper amplifier's output

Results of this subchapter show residual offset after being chopped. The simulations have been conducted with a 1 mV and 5 mV offset to verify the extent of the offset suppression with respect to offset drift.

Simulation settings:
- Duration: 600 µs
- Voltage follower connection
- $V^+ = 1$ V
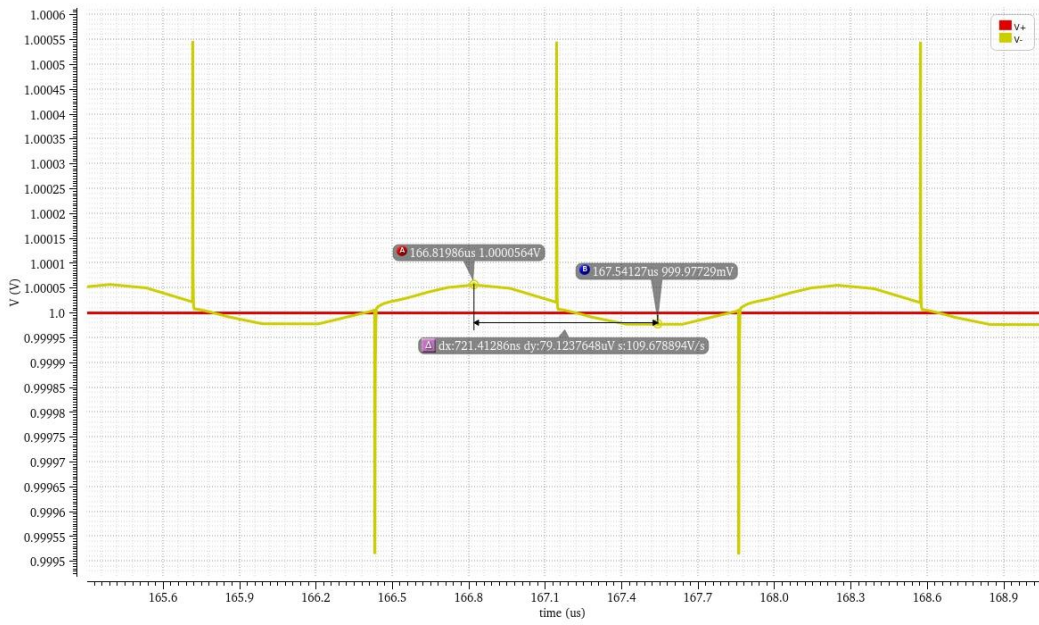- $f_{chop} = 700$ kHz
- $V_{off} = 1$ mV, 5 mV

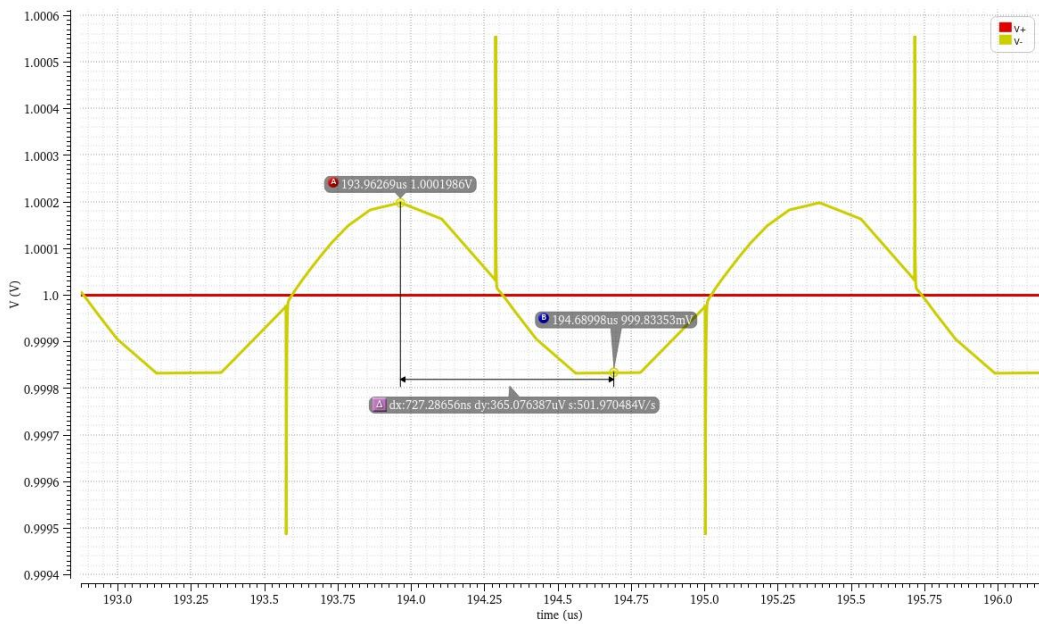Fig. 5.7　Residual offset ripple with input offset 1 mV

Fig. 5.8　Residual offset ripple with input offset 5 mV

We can observe from the graphs that the offset suppression has been successfully performed by the circuit. In case of 1 mV offset, the residual offset was 40 µV, which is a 25 times reduction of the initial offset. Same conclusion can be made with 5 mV offset, where the offset after chopping resulted in a ripple with amplitude of 182.5 µV, amounting to 27 times lower offset than without chopping. Thus, the magnitude of offset suppression is mainly determined by the filter's attenuation.
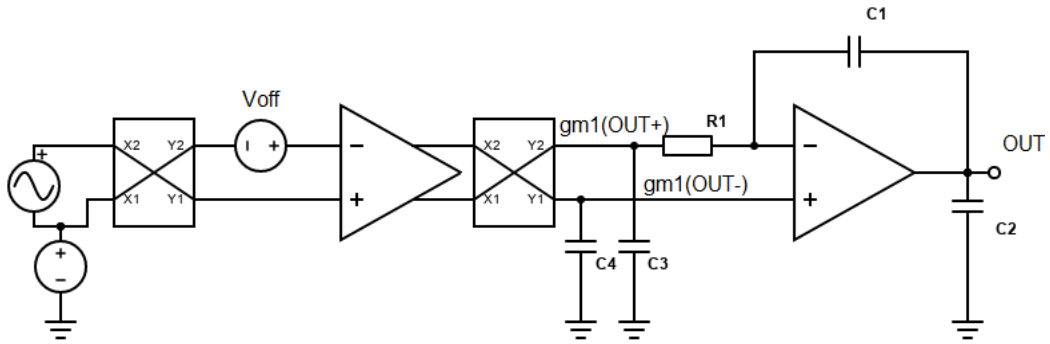
Fig. 5.9   Schematic of circuit setup for simulation

Simulation settings:

- V_{diff} = VAC 200 μV, frequency = 5 kHz
- V^+ = 1 V
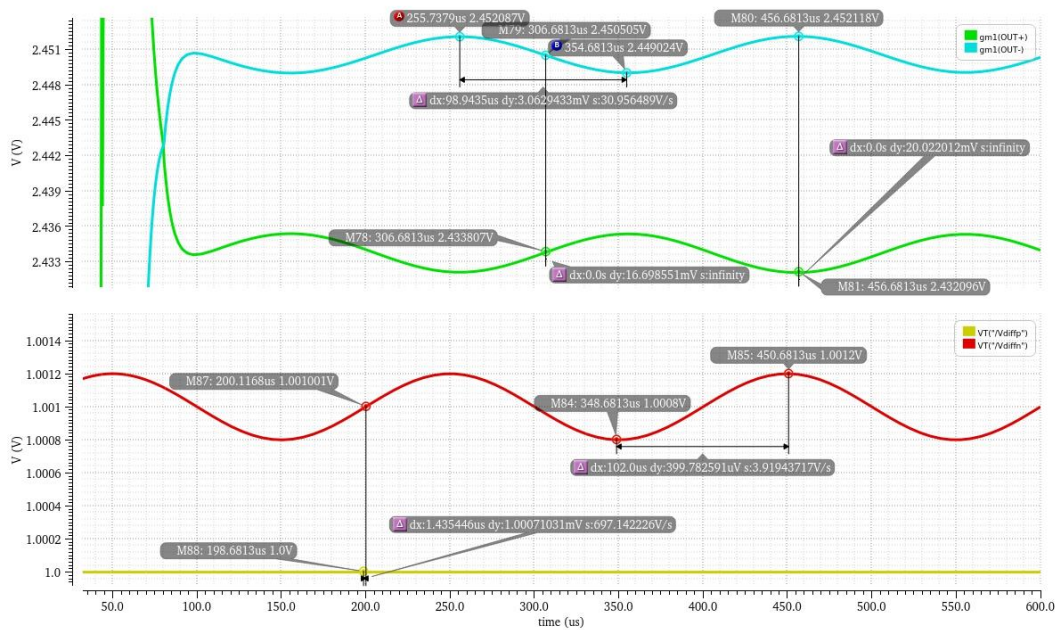- V_{off} = 1 mV

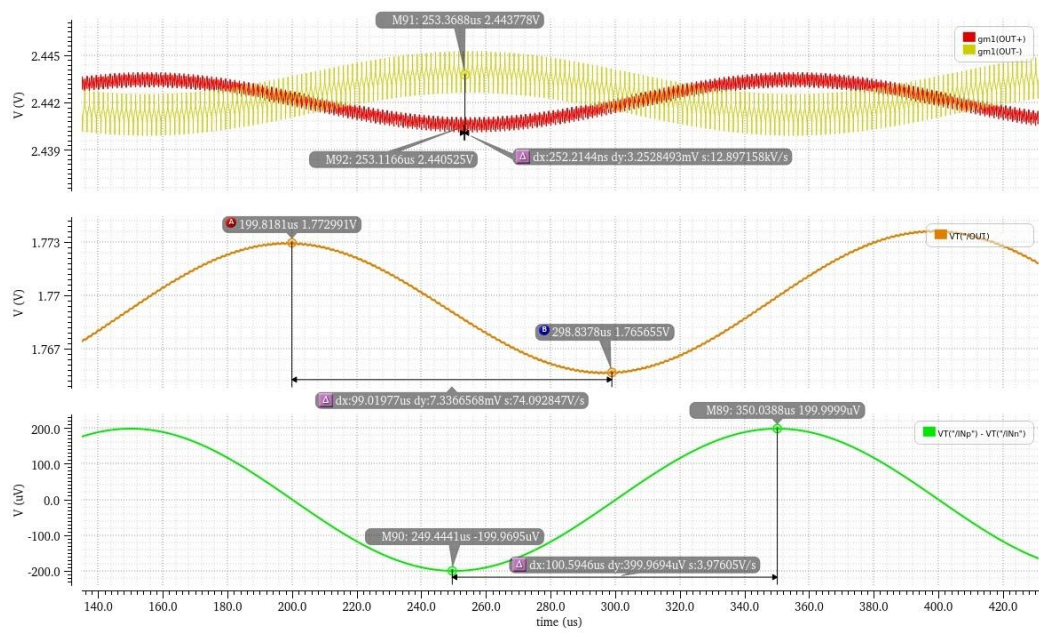Fig. 5.10   gm1 output and input without chopping with 1 mV offset

Fig. 5.11   gm1 and gm2 outputs with chopping with 1 mV offset.
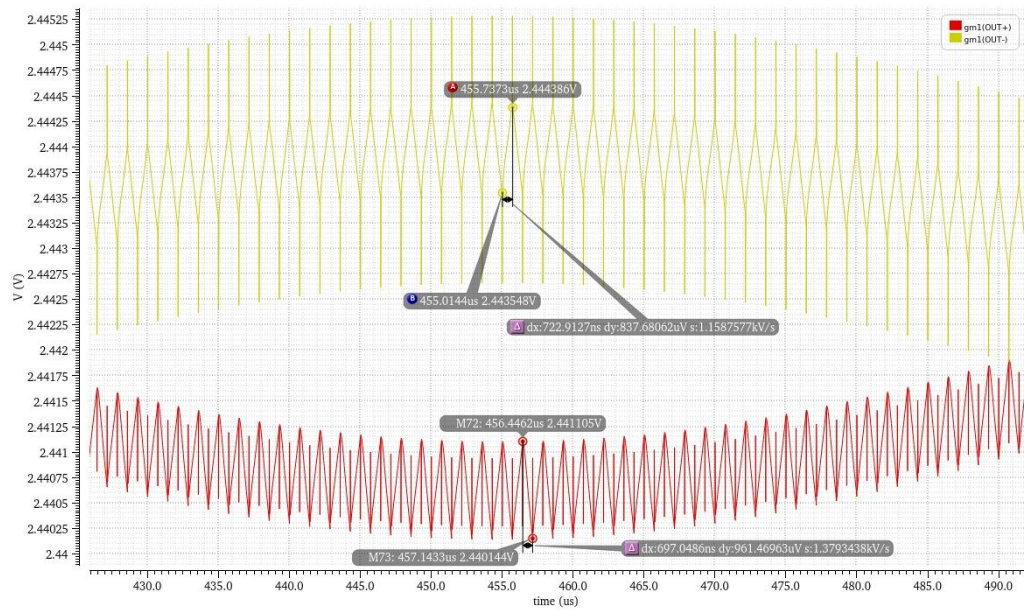

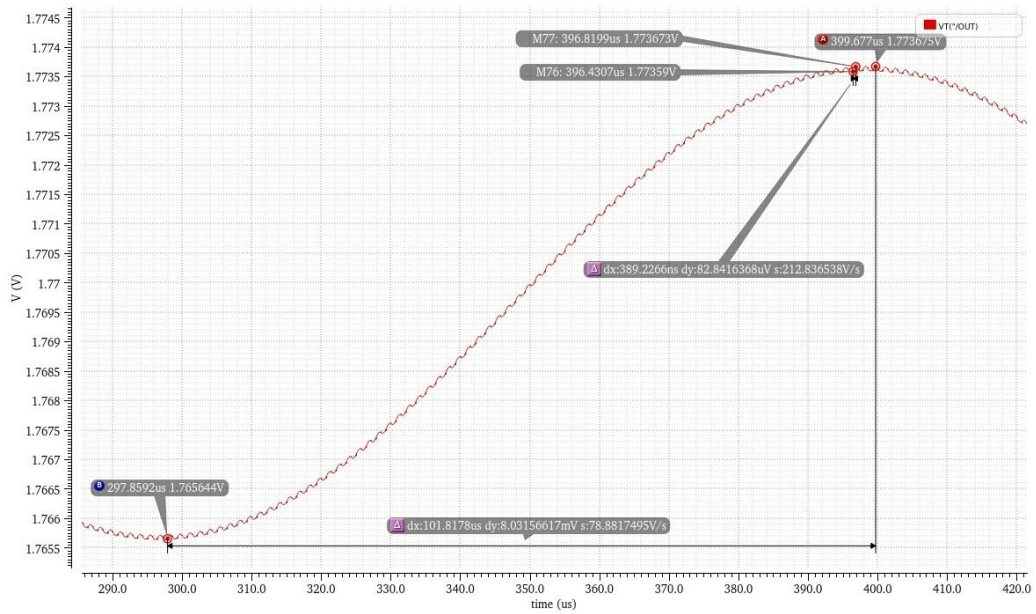Fig. 5.12   gm1 – modulated offset detail

Fig. 5.13   gm2 – chopper residual ripple detail

The graphs provide a detailed overview on how the signal is processed during the chopping operation. First, the comparison with the situation with chopping off (figure 5.10) shows that the gm1 stage can amplify the signal which is smaller than the inherent offset at its input differential stage, however, the output branches are oscillating around different voltages with a 16-mV difference, with the input signal being amplified to 3 mV, and such signal cannot be further processed by the next stage.

With chopping on, the chopper ripple is modulated on the output signal of gm1 stage, and the signals oscillate around a common voltage, passing into the gm2 stage, where this ripple is significantly filtered out. The detailed views of both ripples denote that the ripple initially takes on a peak-to-peak value at around 800-900 µV, roughly corresponding with the input offset. The filter then processes the signal, based on the chopping frequency biases itself into a DC operating point created by the voltage divider R1 and C1 (shown on figure 5.9) around which the output signal oscillates with a residual ripple. From the results, we can conclude that the ripple was decreased tenfold by the filter, down to only 80 µV. The input signal of 200 µV has been amplified to 8 mV, gain of 32 dB, which was amplified primarily by the gm1 stage, as the filter's cut-off frequency is around 6 kHz.

5.3 Periodic steady-state simulation

The simulations provide us with harmonic spectrum before and after the filter, showing the demodulation of the offset by gm2 stage.

Simulation settings:

- Voltage follower connection
- $V^+ = 1$ V
- $f_{chop} = 700$ kHz
- $V_{off} = 1$ mV
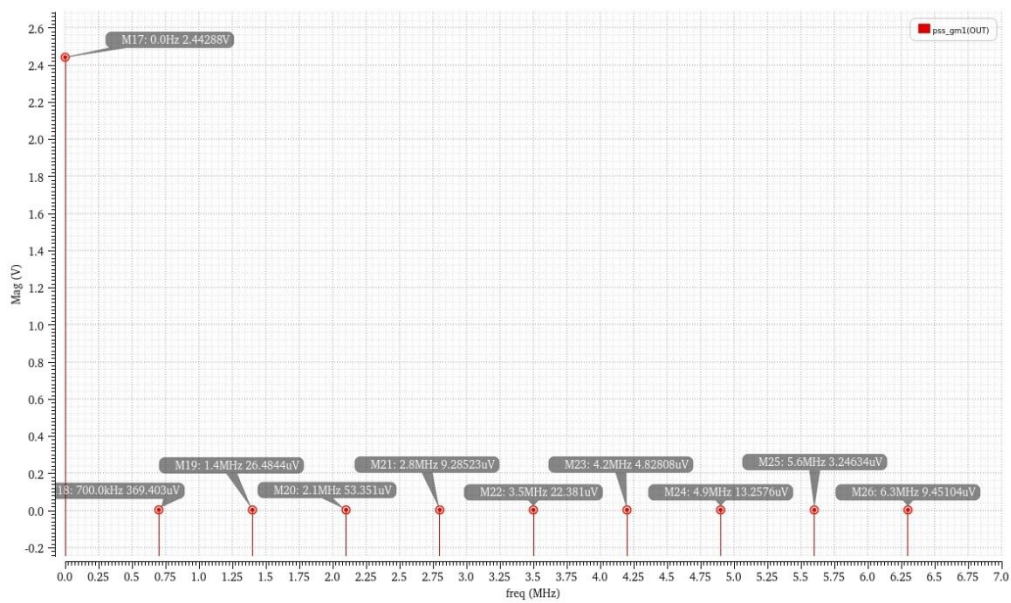- Number of output harmonics: 10

Fig. 5.14   Harmonic spectrum before the filter's input

DC portion of the signal has the magnitude of 2.4 V, which is the common mode voltage set within the gm1 stage. The offset is modulated primarily on the first harmonic of the signal and then its smaller portions on higher odd harmonics.
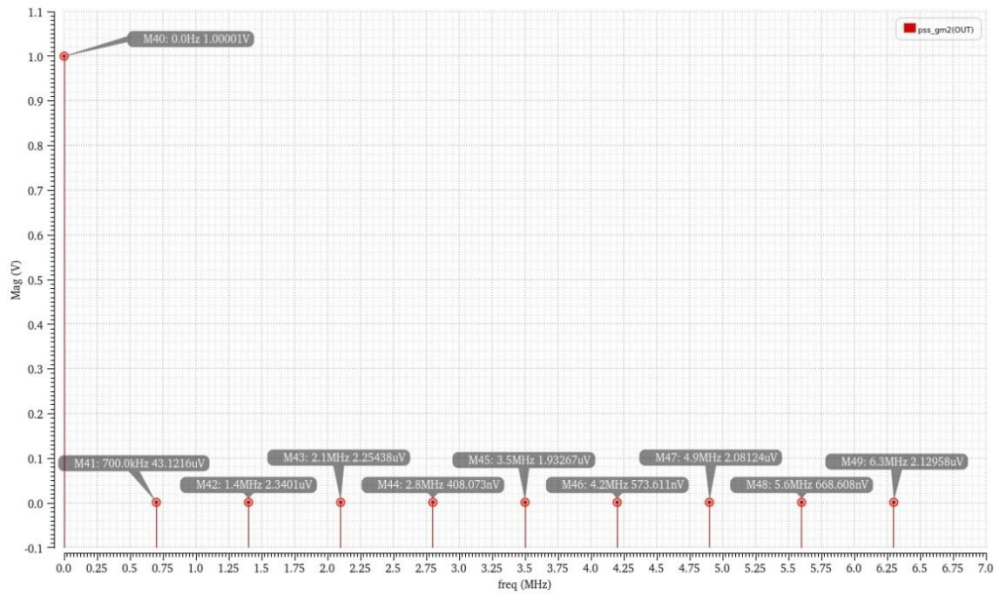
Fig. 5.15   Harmonic spectrum after the filter's input

After passing through the filter, the DC portion of the signal is now set to 1 V by voltage follower connection and the residual offset at 700 kHz and higher harmonics is now suppressed.

5.4 Monte Carlo simulation with corner temperatures

A Monte Carlo simulation with process mismatch has been performed on the circuit with voltage follower connection. The number of runs per one setting was set to 200, and the simulation used three temperatures: -40, 27 and 125 ºC, amounting to a total number of 600 runs. The comparison of highest input offset with enabled and disabled chopping can be seen in the table 5.1.
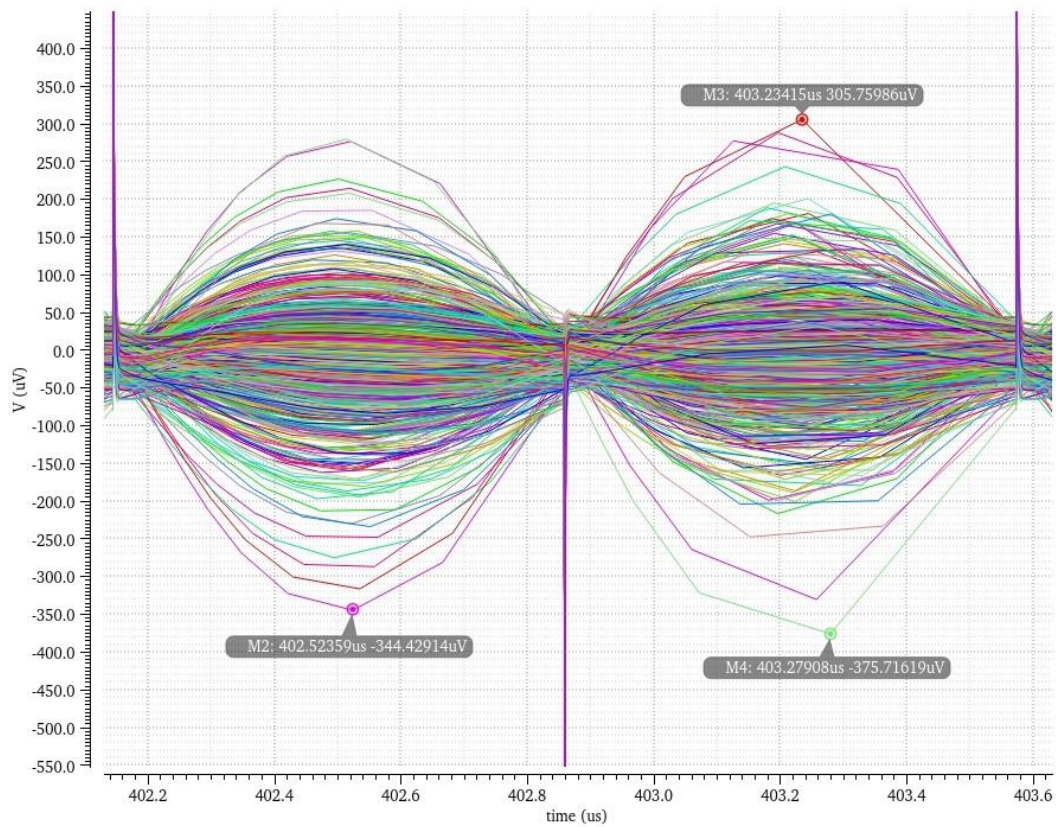
Fig. 5.16   Monte Carlo simulation – voltage difference at the inputs with chopping

Table   5.1   Effects of chopping on suppressing offset caused by temperature and
process mismatch

Temperature [ºC]	Highest measured offset without chopping[mV]	Highest measured offset with chopping [mV]
-40	6.55	0.375
27	5.89	0.247
125	5.02	0.177

As we can see, offset is affected by both process mismatch and temperature, with
the first factor being more impactful. Chopping is greatly reducing the offset created by
manufacturing inaccuracies, in the worst case more than 28 times.

5.5 Noise analysis

Noise analysis and periodic steady state noise analysis with the beat frequency equal to chopping frequency (700 kHz) of the system have been conducted.
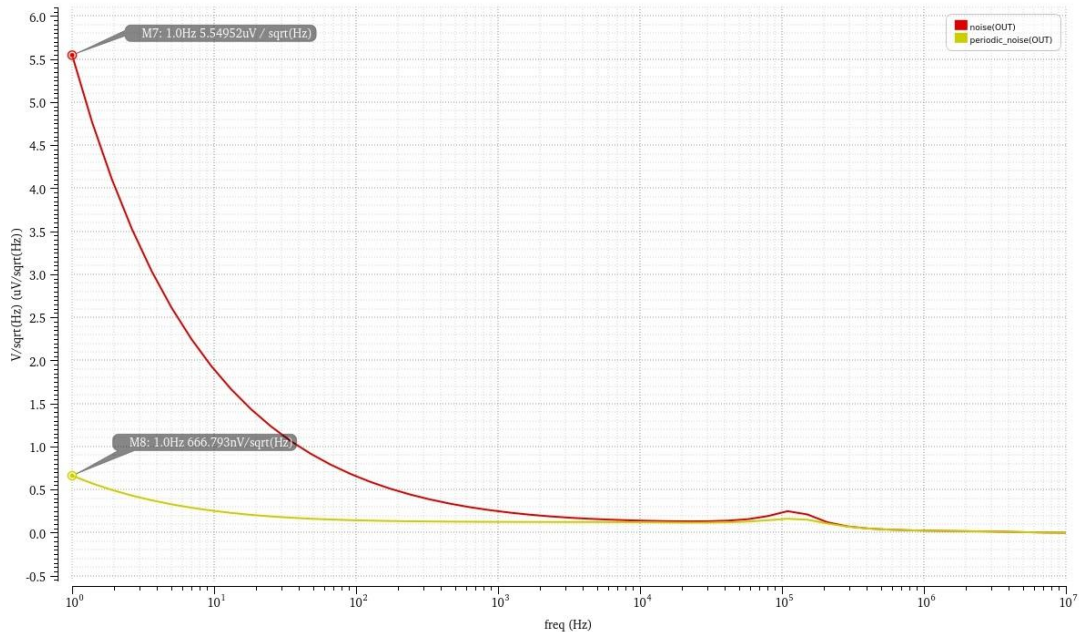
Fig. 5.17   Noise and periodic steady state noise analysis

The noise analysis demonstrates noise presence in the circuit as is, without chopping being taken into consideration. The periodic steady state noise analysis shows noise presence with chopping on, and we can observe that the low frequency noise is considerably lower, by around 9 times. Chopping supresses low frequency noise by modulating it to higher odd harmonics of the chopping frequency alongside with the offset, where it is filtered by the active low-pass filter.

6. CONCLUSION

The aim of the master's thesis was to design a chopper operational amplifier for offset cancellation with using CMOS 0.25 µm technology. The main requirement was a noticeable offset suppression in voltage follower connection and ability to suppress the offset drift as well.

The requirements have been successfully achieved by designing a two-stage operational amplifier and subsequentially an active low-pass filter based on the same topology with relatively low complexity and low consumption of only 40 µA. The dimensions of transistors are denoted in chapter 4 with their respectful calculations and clarification of their use. Chapter 5 verifies that all the requirements are met by simulating the circuit in Cadence Virtuoso environment.

Most notable results are offset suppression in voltage follower connection with 1 mV offset to 40 µV. The degree of offset suppression stays nearly constant with increasing the offset to 5 mV, which verifies the system's resistance to offset drift. and Ability to suppress process and mismatch offset across the whole temperature reaches hundreds of µV Another advantage of the chopper amplifier is also capability of processing signals smaller than its inherent input offset. The differential input stage of PMOS transistors allows for input voltage range of $0 - 3.5$ V across the whole temperature range and output voltage range depends on the design of the output stage; in our case it is almost rail-to-rail. The chopper operational amplifier's bandwidth is 100 kHz, which is shown in the frequency analysis.

This configuration allows for a potential extension to chopper-stabilized amplifier with corresponding adjustments to bandwidth and filter properties.

The results of the master's thesis show that with a relatively simple topology and a low number of components, it is possible to suppress offset to values which do not interfere with low voltage signals, which are frequently used in many applications nowadays. The residual ripple and switching spikes of the output signal reach tens and hundreds of µV, respectively, depending on the input signal's frequency. Such signal is satisfactory for use with many applications, depending on the individual application's requirements.

An estimation of the layout using software Cadence Virtuoso Layout Suite L shows that the circuit takes a chip area of approximately 132 µm x 116 µm, which amounts to 0.018 mm^2 after considering the additional space for isolation and wiring. Taking into account a regular size of AC/DC converter's chip area of 1 mm x 2 mm, there certainly is a possibility of using the chopper amplifier as one of the blocks on the chip.

It is important to notice that the chopper's performance greatly depends on the used area on chip and larger passive components can further improve the results. A possible major advancement in chopper amplifier offset reduction is using switched-capacitor method for filtering.

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SYMBOLS AND ABBREVIATIONS

Abbreviations:

FEEC	Faculty of Electrical Engineering and Communications
BUT	Brno University of Technology

Symbols:

A_v	open-loop gain	[dB]
BW	bandwidth	[Hz]
C_L	load capacitance	[F]
$CMRR$	common-mode rejection ratio	[dB]
GBW	gain bandwidth	[Hz]
g_m	transconductance	[S]
I_D	drain current	[A]
I_{OUT}	output current	[A]
K_P	technological parameter	[A/V^2]
L	length of transistor channel	[m]
$PSRR$	power supply rejection ratio	[dB]
R_{out}	output resistance	[Ω]
r_{ds}	drain-source resistance	[Ω]
V_{DD}	positive supply voltage	[V]
V_{DS}	drain-source voltage	[V]
V_{GS}	gate-source voltage	[V]
V_{th}	threshold voltage	[V]
W	width of transistor channel	[m]
λ	channel length modulation parameter	[V^{-1}]

LIST OF APPENDICES

Appendix A - Schematics

A.1 Chopper operational amplifier