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VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF MICROELECTRONICS

ÚSTAV MIKROELEKTRONIKY

DESIGN OF AD CONVERTER WITH LOW SUPPLY VOLTAGE IN CMOS TECHNOLOGY

NÁVRH PŘEVODNÍKU AD S NÍZKÝM NAPÁJECÍM NAPĚTÍM V TECHNOLOGII CMOS

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

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VEDOUCÍ PRÁCE

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Diploma thesis

Masters's study field
Microelectronics

Student: Bc. Jiří Holas ***ID:*** 134312
Year of study: 2 ***Academic year:*** 2015/16

NÁZEV TÉMATU:

Design of AD converter with low supply voltage in CMOS technology

INSTRUCTION:

Study different architectures of A/D converters and their performance. Focus on high speed (hundreds of kHz) and medium resolution architectures (>10 bits). Implement the ADC system by designing critical sub-modules on transistor level and verify the overall top-level ADC performance as a whole with Cadence simulation environment.

REFERENCE:

According to recommendations of supervisor

Assigment deadline: 8.2.2016 ***Submission deadline:*** 26.5.2016

Head of thesis: Ing. Vilém Kledrowetz, Ph.D.
Consultant:

doc. Ing. Lukáš Fujcik, Ph.D.
Subject Council chairman

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Diplomová práce

magisterský navazující studijní obor **Mikroelektronika**
Ústav mikroelektroniky

Student: Bc. Jiří Holas ***ID:*** 134312
Ročník: 2 ***Akademický rok:*** 2015/16

NÁZEV TÉMATU:

Návrh převodníku AD s nízkým napájecím napětím v technologii CMOS

POKYNY PRO VYPRACOVÁNÍ:

Prostudujte struktury převodníků AD. Zaměřte se na struktury vhodné pro dosažení rozlišení > 10 bitů a zpracování signálů v řádu stovek kHz. Porovnejte vybrané struktury. Na vybrané struktuře proveďte simulace zahrnující reálné parametry dílčích bloků (Matlab). Navrhněte převodník AD na tranzistorové úrovni v technologii TSMC 180 nm a ověřte dosažené parametry.

DOPORUČENÁ LITERATURA:

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Termín zadání: 8.2.2016 ***Termín odevzdání:*** 26.5.2016

Vedoucí práce: Ing. Vilém Kledrowetz, Ph.D.
Konzultant diplomové práce:

doc. Ing. Lukáš Fujcik, Ph.D., *předseda oborové rady*

ABSTRAKT

Tato diplomová práce se zabývá návrhem 12 bitového řetězového A/D převodníku. Součástí návrhu bylo vytvořit referenční model převodníku v prostředí Matlab a determinovat faktory, které negativně ovlivňují výsledek konverze. S využitím nabytých poznatků navrhnout řetězový převodník na transistorové úrovni v prostředí Cadence. V teoretické části jsou shrnuty základy A/D převodu a dále jsou představeny nejčastěji používané architektury A/D převodníků. V dalších částech je popsán a diskutován vliv neidealit na vlastnosti řetězových převodníků. Praktická část se již věnuje popisu základních charakteristik řetězových převodníků a dokazuje funkci modelu. Z výsledků modelové struktury byly stanoveny reálné parametry, které byly dále využity v procesu tvorby návrhu v CMOS technologii TSMC 0,18μm s nízkým napájecím napětím.

KLÍČOVÁ SLOVA

Řetězový A/D převodník, model, Matlab, Cadence, TSMC 0,18μm, 2,5 bit MDAC

ABSTRACT

This master thesis is dedicated to the design of 12-bit pipeline ADC. The part of the design was to create a reference model ADC in the Matlab environment and to determine factors that negatively affect the results of the conversion. Based on experiences gained in the mathematical model, the pipeline ADC on the transistor level was designed in the Cadence environment. The theoretical part summarizes the fundamentals of A / D conversion and introduces the most commonly used architecture of A / D converters. Furthermore, the influence of non-idealities on the conversion process is described and discussed. The practical part is dedicated to description of ADC's model basic characteristics and confirms the model functionality. From the results of the model structure the real parameters were determined and used in the design process in CMOS technology TSMC 0,18μm with low power supply.

KEYWORDS

Pipelined ADC, model, Matlab, Cadence, TSMC 0.18 μm, 2.5-bit MDAC

Holas, J. Design of AD converter with low supply voltage in CMOS technology. Brno: Brno University of Technology, Faculty of Electrical Engineering and Communication, Department of Microelectronics, 102 p., Master's Thesis. Supervised by: Ing. Vilém Kledrowetz, Ph.D.

DECLARATION

I declare that I have written my semester project on the theme of „Design of AD converter with low supply voltage in CMOS technology“ independently, under a guidance of semester's thesis supervisor and using the technical literature and other sources of information which are all quoted in the thesis and detailed in the list of literature at the end of the thesis.

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Brno ....

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INTRODUCTION

This master's thesis is dedicated to ADC conversion process and its classification. The first part of the document is a theoretical part, which deals with introducing the reader into Analog-to-Digital conversion basics. The fundamental parameters such an SNR, SNDR, INL, DNL and other common terms are introduced and explained.

The work continues with various ADC architectures introduction and aims to explain their advantages and disadvantages. Then the preferable pipelined ADC architecture is chosen and described in details.

Next part of the project is dedicated to the real design of 12-bit pipelined ADC model in Matlab environment. The model serves to determine weak parts of conversion chain in this structure and serves as a reference for following realization in TSMC 0.18μm CMOS technology.

The stated parameters were taken into account during the real design process in Cadence environment in next part of the document. This chapter also reveals the step-by-step design of individual stages along with numerous simulation results that confirm functionality of the converter.

At the end of the practical part, the model and real design results are discussed and compared. The theoretical proposal how to compensate non-idealities is introduced.

THEORETICAL PART

This part of the document is dedicated to AD (Analog to Digital) conversion principles. It consists of detailed ADC function description and point to reveal conversion non-idealities.

1 AD CONVERTERS BASICS OVERVIEW

1.1 ADC conversion chain

The AD converters facilitate the conversion of an analog input signal to relevant output digital signal. The input is an mostly voltage signal and the output represents a digital word with stated bit resolution. In Figure 1 is shown how the input signal is converted into its digital form.

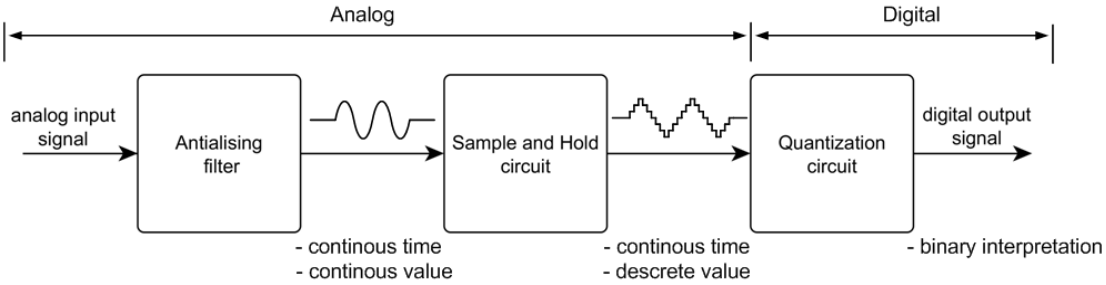


Figure 1: Analog to digital conversion principle

The first segment of conversion chain is an anti-aliasing filter. Basically, it is represented by a low-pass filter. The reason why this block is used in almost every converter is due to filtering capability of higher frequencies to fulfill a Nyquist criterion. The Nyquist criterion (or theorem) determines maximal input frequency that is sensed and processed by converter to avoid appearance of aliasing effect. The equation (eq.1) shows,

$$f_{\mathrm{Sample}} \geq 2 \cdot f_{\mathrm{in\_max}}, \tag{1}$$

where f_{Sample} is ADC sample frequency and $f_{\mathrm{in\_max}}$ is maximal input frequency. If this condition is accomplished, the aliasing effect will not intervene the output signal and the signal obtained by conversion can be reversely reconstructed [1].

When the signal passes through anti-aliasing filter is further fed into Sample and Hold circuit (S&H). This signal is „sampled“. It means that appropriate input voltage is held at the output for defined period of time. That is necessary for next processing in quantization block where actual signal value is compared to reference value.

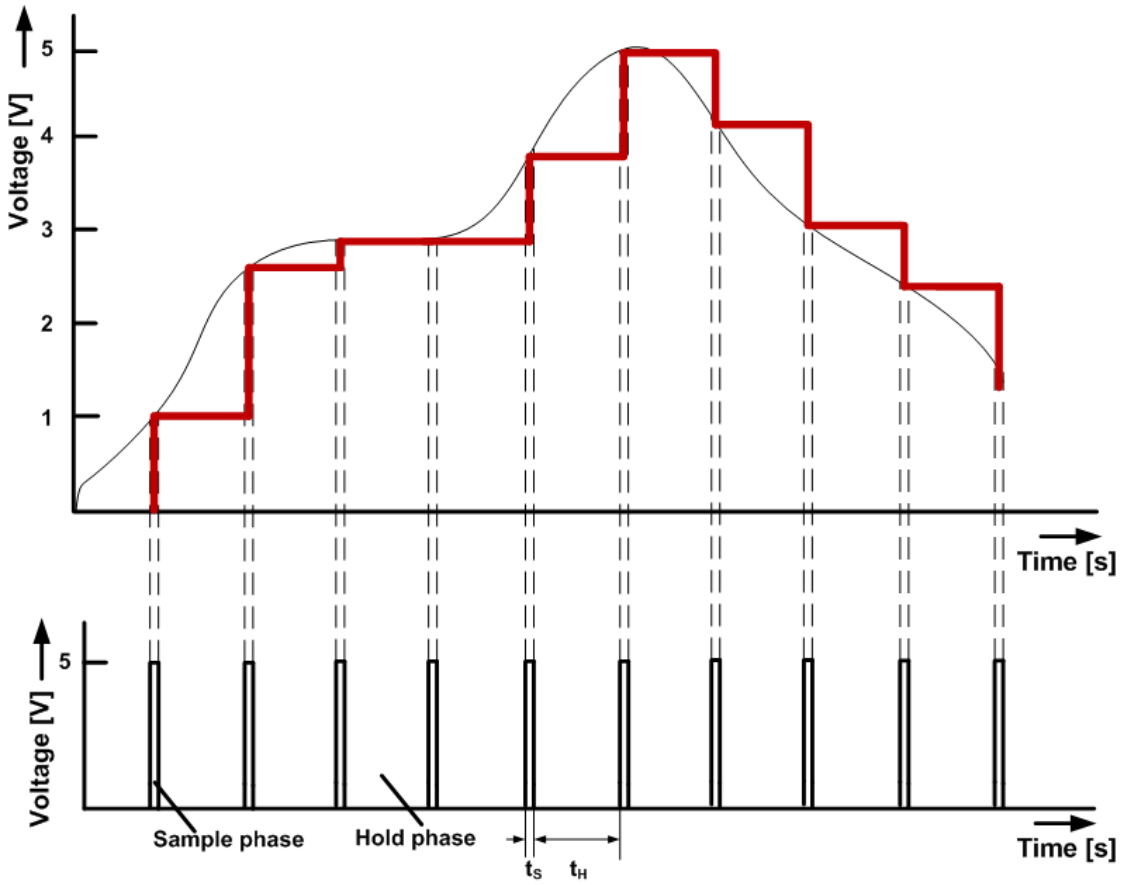


Figure 2: Sample and Hold circuit - simplified function

The principle of S&H circuit function is shown in Figure 2. During the sampling phase, which should be as narrow as technology allows, the input voltage is sampled until the hold phase time occurs. During the hold phase is the sampled signal value held in memory – constant – as long as another sampling time arises. It serves to pick and maintain the actual signal value for quantization. All mentioned above depend on sampling speed. If the speed of sampling increases twice, the hold time decreases for the same amount and it introduces the main limitation of these types of circuits. In every real circuit, we have to calculate with settling time and overshoots caused by transitions during switching. As far as we know these limitations, we have to consider them in real design because sampling speed or sampling rate belongs to one of the key parameters in ADC conversion systems. Other non-idealities related with sampling are mentioned below [1].

Non-idealities in Sample and Hold circuits [1]:

- slew rate,
- settling time,
- nonlinearity,
- gain error,
- gain offset,
- aperture error.

Another block in conversion chain is quantization circuit where constant values from previous sample and hold block are converted into digital form. Quantization is a process that assigns a discrete binary value to individual sample. This value is influenced by resolution of whole ADC. Resolution is determined by number of levels which the input signal can be divided into. If we assume that the output digital word is usually expressed by binary code, then the resolution is determined by number of bits – in the other words, length of digital word [1].

Let's consider that we have 12-bit ADC, the resolution can be derived from the following formula

$$Resolution = 2^{\mathrm{N}}, \tag{2}$$

where N designates number of bits of the converter. If we substitute N into equation, the resolution (or the amount) of discrete levels is

$$Resolution = 2^{12} = 4096 \text{ levels.} \tag{3}$$

Unfortunately, a quantization error so-called quantization noise is formed during this process. If we want to minimize these errors in order to obtain uncorrupted digital word, the quantization noise has to be equal to one-half of LSB (Least Significant Bit) [1]. A transfer characteristic for an ideal 3-bit ADC and its quantization error is shown in Figure 3. As can be seen in this plot, the quantization error for ideal case is equal to one-half of LSB.

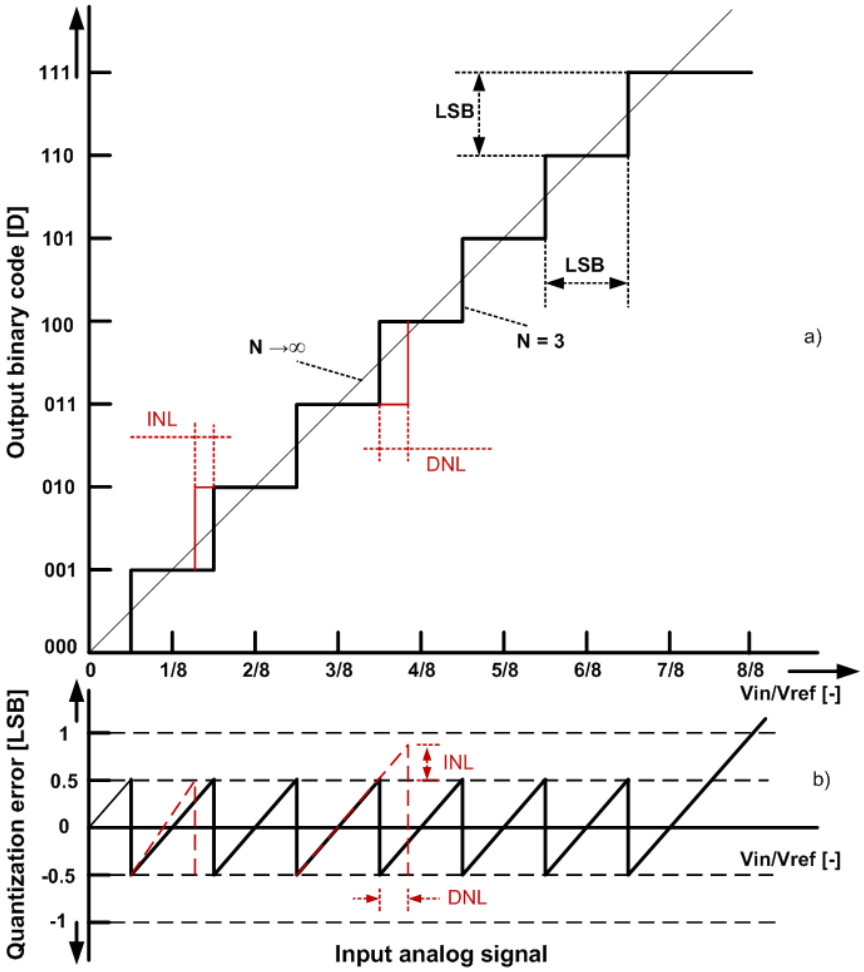


Figure 3: a) Transfer curve for ideal 3-bit ADC, b) quantization error centred about zero

1.1.1 Integral Non-Linearity and Differential Non-Linearity

The red curve in Figure 3 reveals further very important dynamic parameters such as INL (Integral Non-Linearity) and a DNL (Differential Non-Linearity) and can be thought of quantization error consequences.

— **INL** is defined as a deviation of an actual transfer function from ideal straight line connection between two end points of the converter's transfer function.

— **DNL** is defined as a difference between the size of an actual and an ideal step size. The ideal step size is equal to 1 LSB or $V_{LSB} = V_{FS}/2^N$ where V_{FS} is a full-scale input range.

From mathematical point of view, the DNL can be described as

$$DNL(k) = \frac{(step\ size\ of\ code(k) - V_{LSB})}{V_{LSB}} \quad [LSB] \tag{4}$$

and for INL the following equation applies,

$$INL(k) = \sum_{i=0}^{k} DNL(i) \quad [LSB]. \tag{5}$$

1.1.2 Signal to Noise Ratio

Signal to Noise Ratio (SNR) is the ratio of the power of full-scale input signal to total noise power present at the output of a converter. The SNR can be obtained by applying a sinusoidal signal to the converter and performing a Fast Fourier Transform (FFT) of the digital output of the converter. The equation to determine this parameter is then,

$$SNR = 10 \cdot log\left(\frac{Signal\ power}{Total\ Noise\ Power}\right) \quad [dB] \tag{6}$$

The maximum achievable theoretical SNR is given by,

$$SNR = 6.02 \cdot N + 1.76 \quad [dB] \tag{7}$$

where *N* is ADC resolution and if only quantization noise is taken into account [3].

SNR parameter neglects higher harmonics of the signal but it consists of quantization and white noise.

1.1.3 Signal to Noise and Distortion Ratio

The Signal to Noise and Distortion Ratio is the ratio between the power of the full-scale input signal and total noise including harmonics. The corresponding formula can be written as

$$SNDR = 10 \cdot log\left(\frac{Signal\ power}{Noise\ and\ Harmonic\ Distortion\ Power}\right) \quad [dB]. \tag{8}$$

1.1.4 Effective Number of Bits

The Effective Number of Bits (ENOB) can be calculated from SNDR by following equation

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad [bits] \tag{9}$$

1.2 Architectures

In the present time, ADCs come in several basic architectures, although many variations exist for each type. The most used structures were chosen and they will be explained in next parts of a document in a briefly way. The attention is aimed to introduce each architecture and compare its advantages and disadvantages with the other ones.

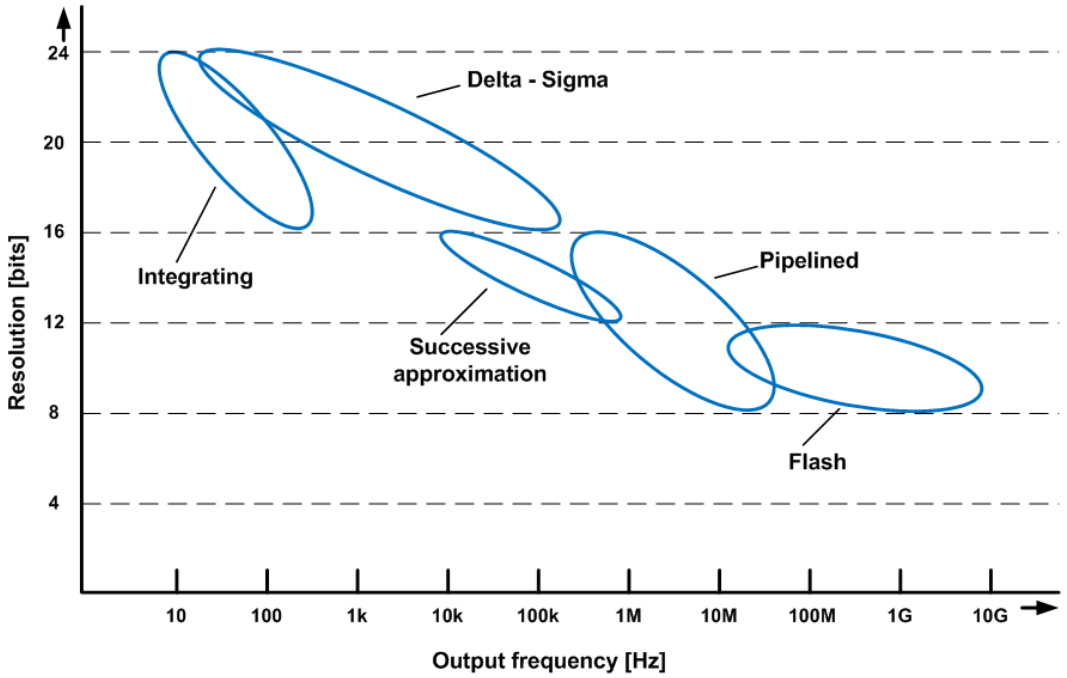


Figure 4: ADC architectures comparison

In Figure 4 is shown a resolution dependency on sample rate of individual converter architectures. It can be read out from a graph above that each architecture has its trade-offs due the parameters which influence the other. For example, very fast flash ADC architecture achieves very high conversion speed at the cost of lower resolution. On the other side the integrating ADC excels with very high-resolution parameter but the conversion rate comes up to units of kHz. Every architecture has got a different ratio of trade-offs and the next chapter aims to explain them shortly.

1.2.1 Integrating ADC

The history of integrating ADC's dates back to 1950's and was a real breakthrough in high-resolution applications such as digital voltmeters [7]. The most used variant - a dual-slope integrating ADC is shown in Figure 5 and its output waveforms can be seen in Figure 6.

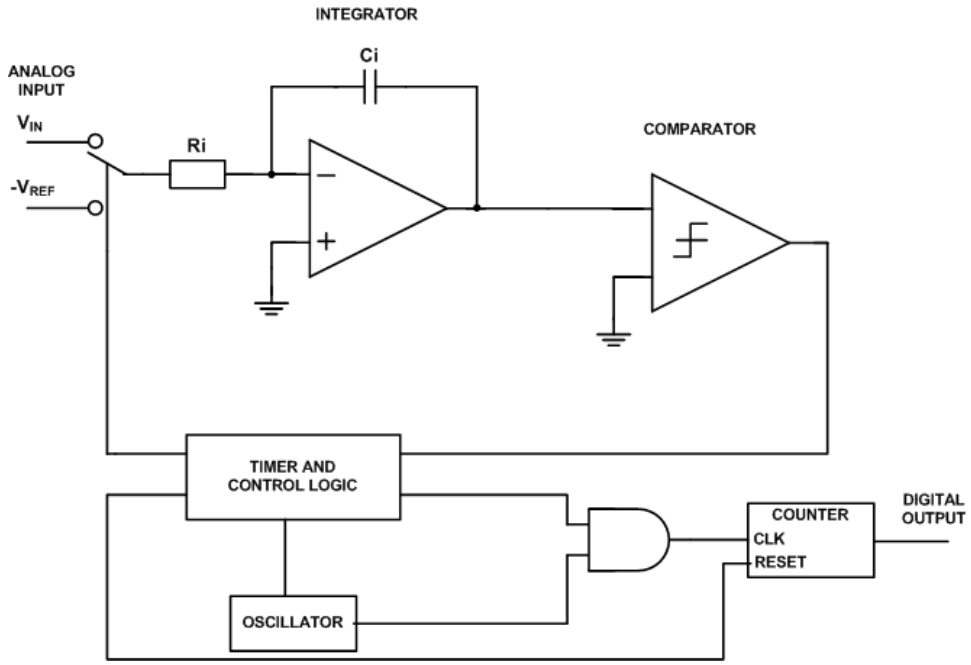


Figure 5: Dual-slope integrating ADC [7]

The input signal V_{IN} is applied to an integrator. At the same time, the enable signal for the counter is asserted and it starts counting clock pulses. The time of integrating is fixedly determined. When this time is reached the reference voltage with a different polarity is applied to the integrator. The accumulated charge on integrating capacitor is directly proportional to average value of the input over integration interval T and can be expressed as

$$Charge_{slope} = \frac{V_{\mathrm{IN}}}{R \cdot C}. \tag{10}$$

The capacitor is discharging with slope that corresponds to equation

$$Discharge_{slope} = \frac{V_{\mathrm{REF}}}{R \cdot C}, \tag{11}$$

where RC is a charge/discharge constant of the capacitor. At the same time, the counter is again counting from zero and when the integrator output reaches zero, the count is stopped with the simultaneous reset of analog circuitry.

If we put equation (10) and equation (11) in equivalence, we can determine the discharge time that represents digital output word.

$$\frac{V_{\mathrm{IN}}}{R \cdot C} \cdot T = \frac{V_{\mathrm{REF}}}{R \cdot C} \cdot t_x \tag{12}$$

$$t_x = \frac{V_{\mathrm{IN}}}{V_{\mathrm{REF}}} \cdot T \quad [s]$$

As is shown in Figure 6, the discharge slope remains still the same. On the other hand, the charging slope depends of on input signal amplitude.

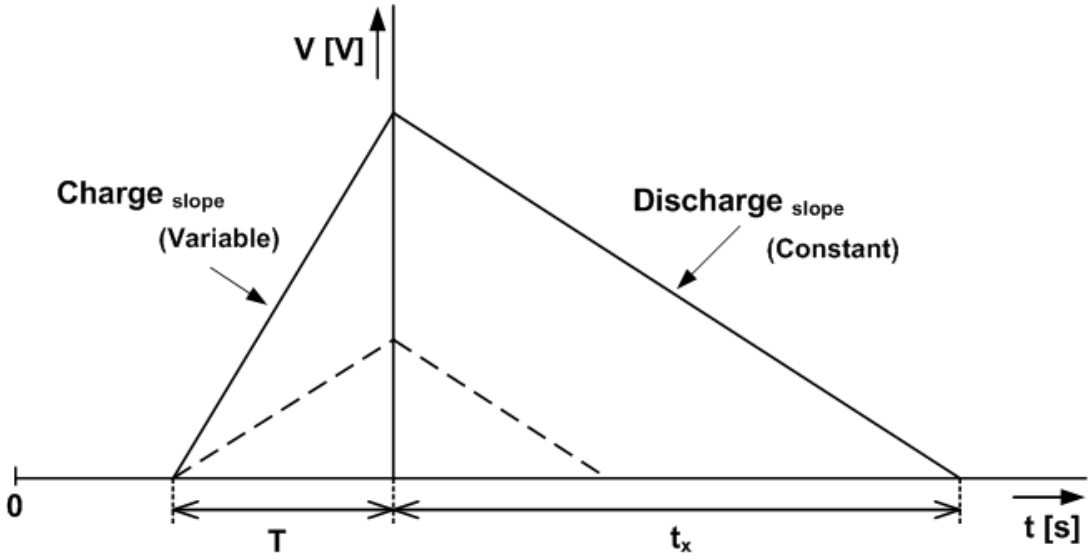


Figure 6: Dual-slope integrating ADC output waveforms

Advantages:

- high reachable resolution (up to 24 bits),
- conversion accuracy is independent of capacitance and clock frequency – affects both slopes (charge and discharge) by the same ratio.

Disadvantages:

- relatively low conversion speed – units of kHz.

1.2.2 Delta - sigma ADC

A delta-sigma ADC is known as an oversampling data converter due to its operation on much higher samplings rates than the Nyquist rate [8]. The relation between how much is the sampling frequency above Nyquist frequency describes an oversampling ratio (OSR). With increasing OSR the quantization noise power decreases.

Another approach connected with oversampling ADCs is a noise-shaping technique. Thank this method the quantization noise is moved to higher frequencies using negative feedback, where is filtered out by digital low pass filter. It is not possible to eliminate quantization noise totally, but can be reduced by a significant amount.

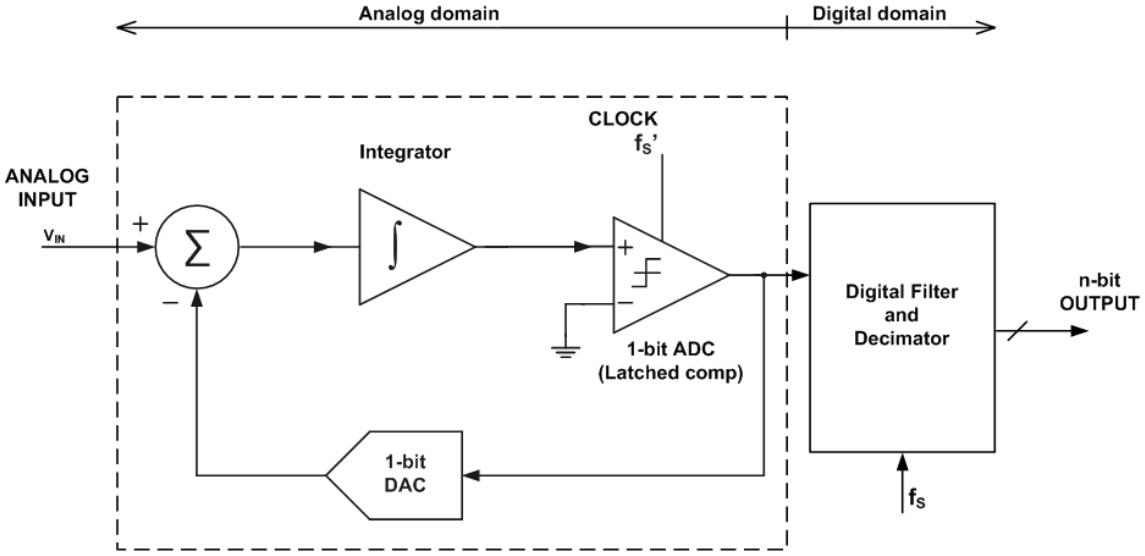


Figure 7: First order delta-sigma ADC architecture

With the increase of resolution of the quantizer, the total resolution of ADC can be enhanced. This method is limited with linearity of designed DAC and special method in layout procedure must be used. Another way how to enhance resolution is to increase the order of the modulator. This approach has its problems as well. With increasing order of the modulator, the stability problems are starting to enforce.

Advantages:

- high reachable accuracy (up to 24 bits),
- higher speed with respect to integrating ADC.

Disadvantages:

- higher speed at the cost of complexity,
- stability problems in higher order designs.

1.2.3 Successive approximation ADC

The conceptual block diagram of a successive approximation ADC is shown in Figure 8. It performs a conversion on command, which means, that for every conversion cycle the acquisition command has to be asserted. The principle of SAR ADC is as follows [9].

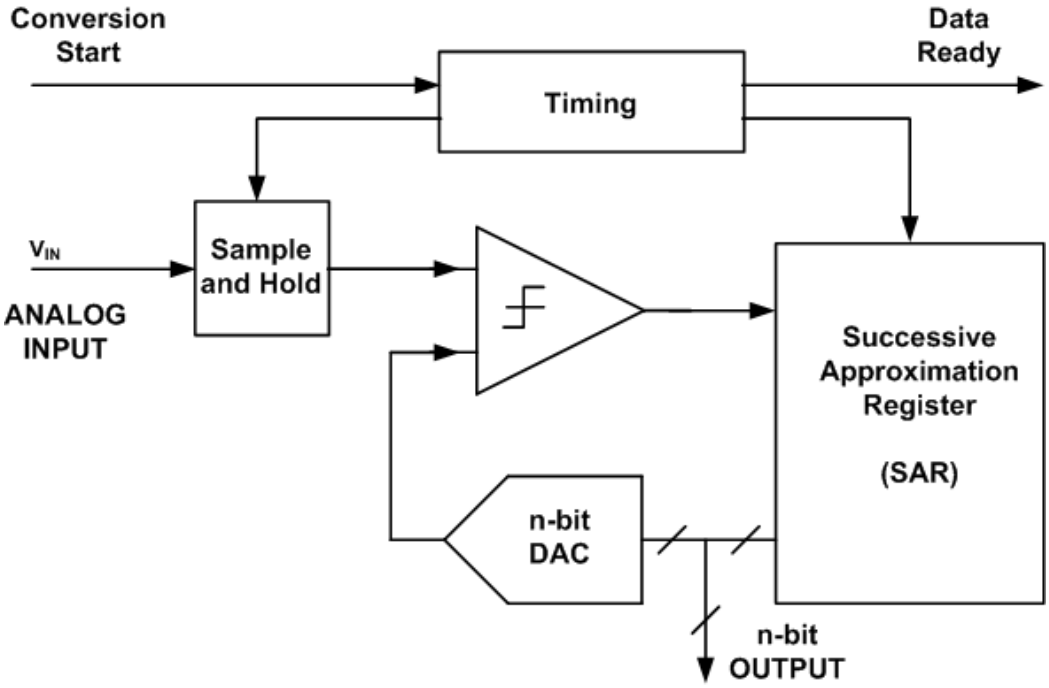


Figure 8: Successive approximation ADC conceptual schematic diagram

The input signal is first sampled and then compared to midscale DAC reference. The comparator, which ensures the comparison process, decides whether the sampled input value is above the midscale or not and the result (MSB) is stored in successive approximation register (SAR). The DAC is internally set to one-quarter or three-quarter scale (depending on the value of bit 1) and the comparator makes the decision for a less significant bit of the conversion. The result is again stored in shift register and the process continues until all of the bit values are determined. Accordingly to achieve *N*-bit resolution, the SAR ADC requires *N* clock cycles. Due to limited DAC linearity, the calibration is often used to achieve higher resolutions.

In Figure 9 is explained a successive approximation algorithm principle graphically.

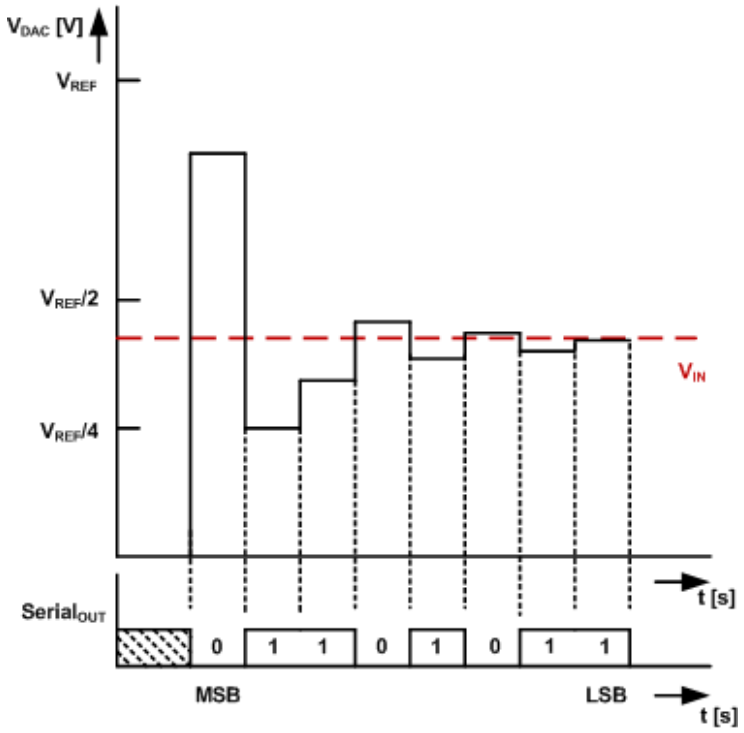


Figure 9: Successive approximation algorithm – graphical explanation

Advantages:

- high resolution (up to 16 bits),
- conversion accuracy,
- low power consumption.

Disadvantages:

- higher demands on inner circuitry design,
- lower sampling rate with comparison to Flash and Pipelined ADCs.

1.2.4 Flash ADC

Flash ADCs, as well known as parallel converters, are the fastest converters in semiconductor technology [3],[10]. One example of simple flash ADC is shown in Figure 10. It uses a series of comparators (2^N) and resistors (2^N-1) to quantize the input analog signal in parallel and produce the output code, that is so called „thermometer code“. The designation comes from analogy with well-known medical thermometer. Produced code is usually converted into *N*-bit binary signal, since the $2^N - 1$ data outputs are not practical at all.

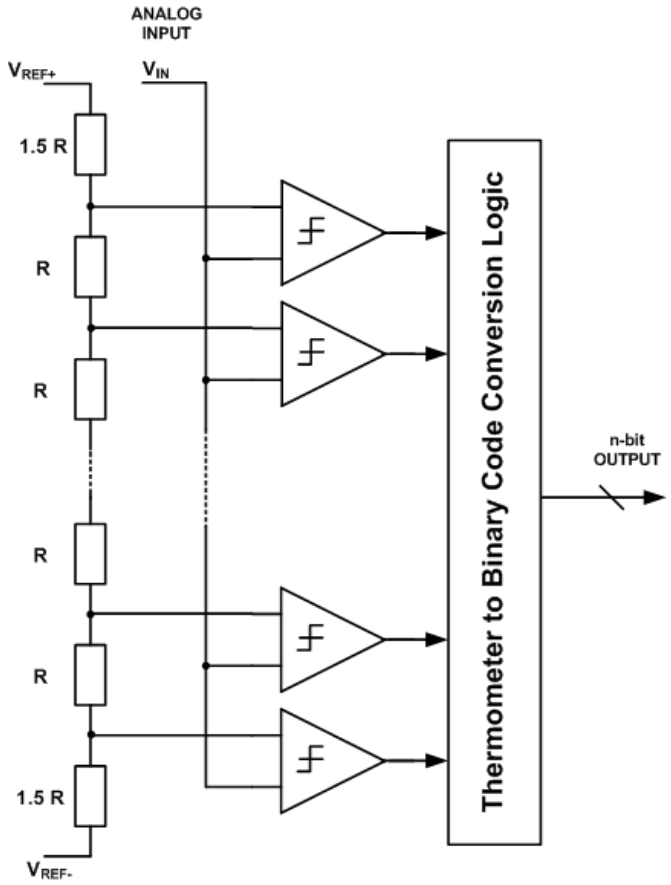


Figure 10: Flash ADC conceptual diagram

The function of Flash ADC is simple. The input signal is applied to all comparators at once, so the thermometer output is delayed by only one comparator delay from the input. The additive delay is caused by few gate delays in binary conversion logic, so overall conversion speed is very fast. However, the flash converter uses a very large number of comparators and resistors, it is limited to low resolution. Another fact is that the speed of comparator is directly proportional to its bias current. This consequently results in high power consumption specifications.

Advantages:

- fastest architecture,
- design simplicity.

Disadvantages:

- high demands on comparators and resistors accuracy,
- high power consumption,
- high number of components (comparators, resistors),
- low reachable resolution (up to 12 bits).

2 PIPELINE ADC

This chapter aims to closely describe pipeline ADC architecture and define its major parameters that influence conversion speed, resolution, and accuracy. It further presents principle of operation and introduces a reader to basic converter block function. Also, it declares possible sources of errors and non-idealities and proposes a possibility for its compensation.

2.1 Principle of pipeline ADC

Pipeline ADCs are commonly used in applications that achieve resolution up to 16 bits and sampling rate in range from dozens MS/s up to hundreds MS/s. The pipelined architecture had largely replaced flash ADCs in modern applications due to its higher resolution, although the sampling rate is lower. As a trade for parameters, the pipelined ADC uses more sophisticated approaches to get higher resolution at the cost of system complexity. The main application portfolio of pipelined ADCs remains in image processing, communication and video processing [4],[5]. The typical pipeline architecture is illustrated in Figure 11. It contains five basic elements such as Sample and Hold circuit, a sub-ADC, a sub-DAC, a summation block and an inter-stage gain amplifier

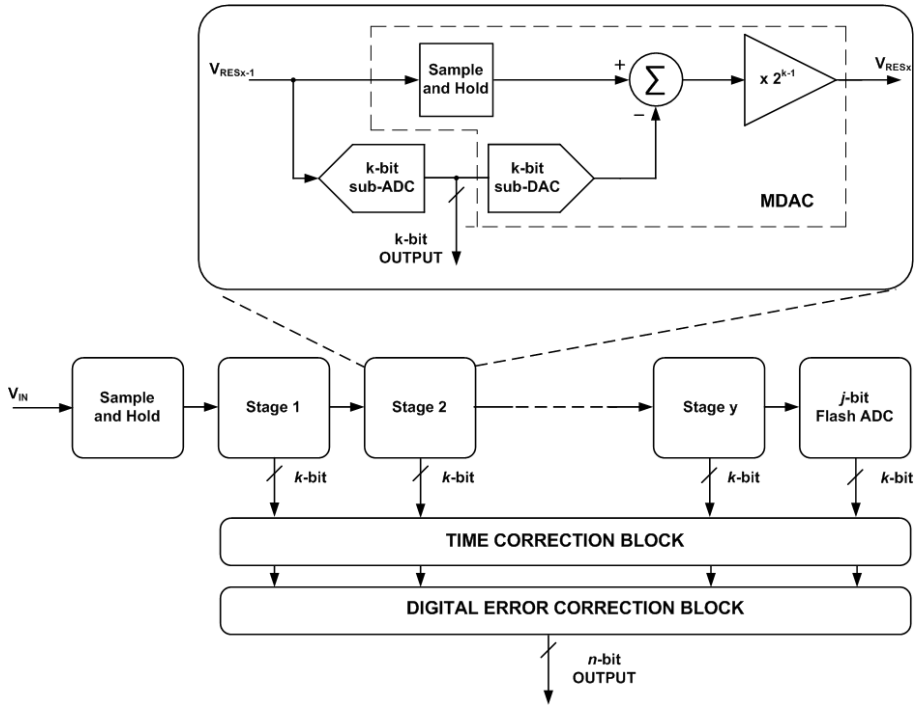


Figure 11: Pipelined ADC block scheme

The operation principle of every single stage is as follows. The input analog signal is captured by sample and hold circuit. In sub-ADC is quantized and digital output is produced. The processed signal is sensed by sub-DAC and converted back to analog signal, where is subtracted from the original signal. After this step, the residuum of original signal is obtained and gained up to the full-scale range through the inter-stage amplifier. The residual signal (quantization error) is passed to next stage, where the described procedure is repeated. The last stage is usually *j*-bit flash ADC because at the end of the pipeline chain is no need to generate residual signal [4].

Due to the presence of sample and hold circuit in every stage, the conversion is done for each stage at the same time. Obviously, this type of signal processing brings a latency of *y*-clock cycles into process. Latency is described as a time difference between first sampled input signal and corresponding digital output prepared at the output. However, the latency is not present for next sample acquisition, since the *y*-clock cycles passed away. In other words, after *y*-clock cycles the overall ADC latency is equal to single clock cycle. The total conversion speed is determined by the speed of the single stage, but is independent of a number of stages [5]. In fact, the particular outputs of single stages are generated at the different time, the synchronization is necessary. The time synchronization block serves for this purpose and it will be discussed later in chapter 2.3.

2.2 Multiplying Digital to Analog Converter

The Multiplying Digital to Analog Converter (MDAC) is a term for common implementation of S&H, sub-DAC, subtractor and inter-stage amplifier in Switched Capacitor (SC) technique. From top-block point of view, it can be said, that one stage of pipelined ADC can be realized from only two blocks – sub-ADC and MDAC (Figure 12). These blocks are frequently implemented with use of low-resolution flash ADCs. The MDAC resolution divided into two main branches during the time and they will be discussed in next chapter 2.2.1 [2],[3].

2.2.1 1.5-bit MDAC versus 2.5-bit MDAC

A number of real designs contain an MDAC with 1.5-bit resolution. The justification for that is simple. The 1.5-bit resolution allows wider offset error correction with respect to the 2.5-bit variant. Conversion linearity is better as well. On the other hand, the 2.5-bit MDAC resolution requires only half number of comparators to achieve the same resolution. The disadvantage of 2.5-bit variant is higher demand on comparator offset.

For both architectures is the main specification identical. The accuracy of comparators must be as high as the overall accuracy of ADC conversion.

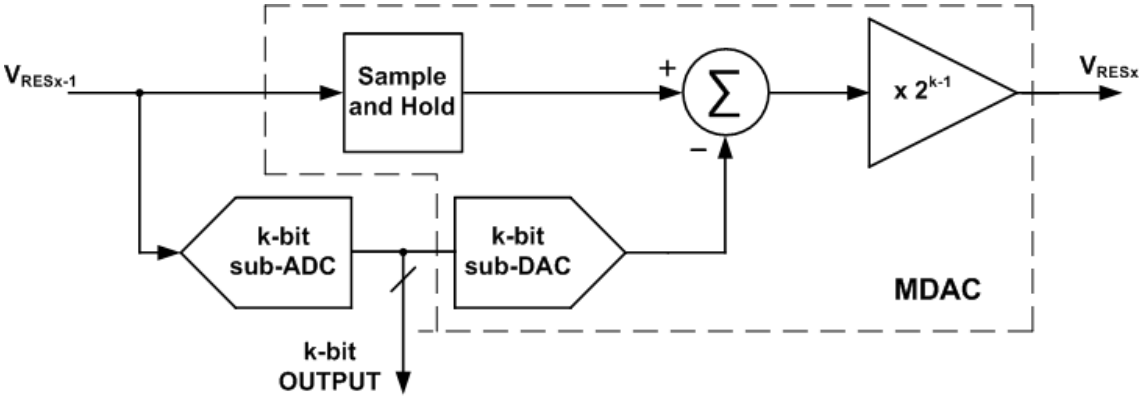


Figure 12: Block scheme of single pipeline stage

One possible specification improvement implies from the function of pipelined ADC in design process. If we consider the fact, that MSBs (Most Significant Bits) are processed on first stage, we can exploit it for power consumption reduction while maintaining the simultaneous accuracy and resolution specs. The idea is to relax comparator's accuracy requirements in the following stages. The Figure 13 shows typical transfer characteristics for 1.5 and 2.5-bit MDAC resolution [3],[4] and [5].

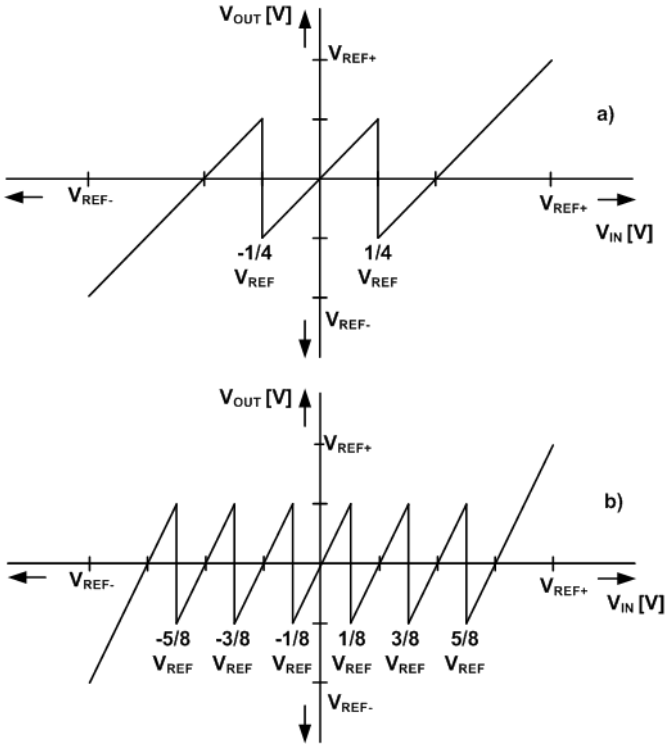


Figure 13: a) 1.5-bit MDAC and b) 2.5-bit MDAC transfer characteristic

2.3 Time correction block

As it implies from function of pipelined ADC, the individual stages work in two phases and they are related to sampling signal. This results in signal delay on the output. It is necessary to synchronize these signals before they pass to digital correction block. It should be mentioned first, that delay of each individual stage is determined as half of period of sampling signal. As the signal passes trough pipeline chain the total delay is a sum of individual delays. The time correction block made from D Flip-Flops creates

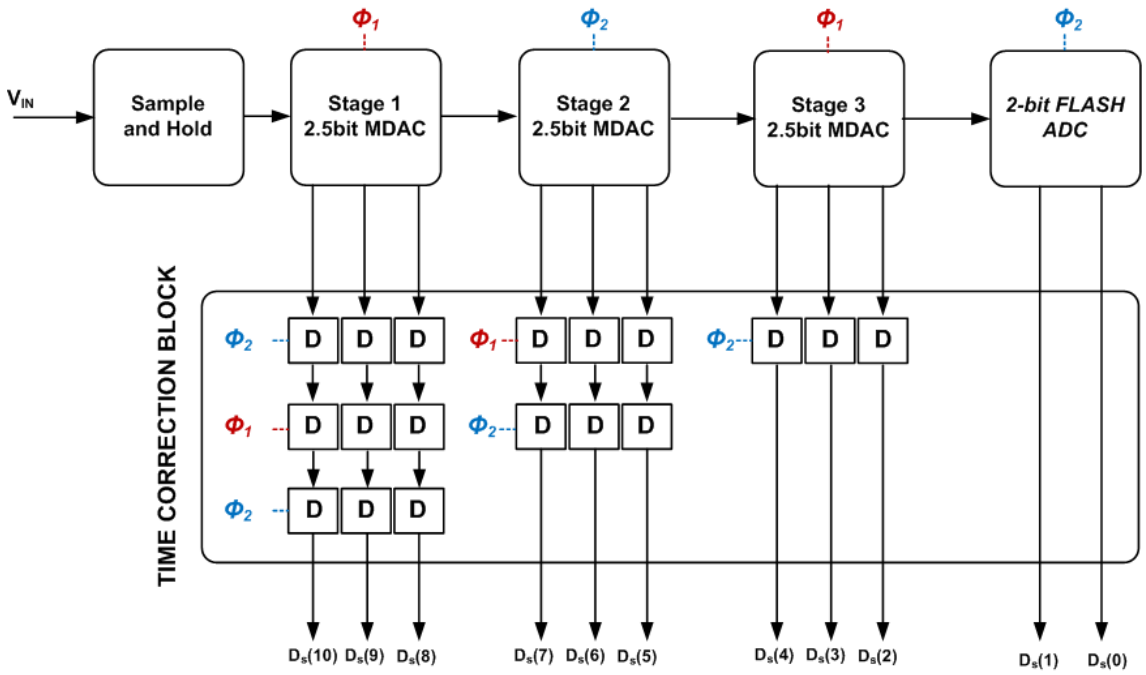


Figure 14 : Time correction block for 8-bit pipelined ADC

a shift register in Figure 14. During the phase Φ_1, the input signal is processed and is shifted at the output when phase Φ_2 arises. The next stage process the signal in the same manner, but with reversed phases. The last stage (2-bit flash ADC) has a delay of its inner structure and is no need to add additional delay. All the mentioned above results in total delay, that is equal to 2Φ [2],[3].

2.4 RSD correction block

Redundant Signed Digit (RSD) is digital correction approach eliminating non-idealities of inner ADC structure. The main error contributor in pipelined ADC is the comparator offset voltage in the sub-ADC block. The ideal transfer characteristic with influence of offset error is shown in Figure 15.

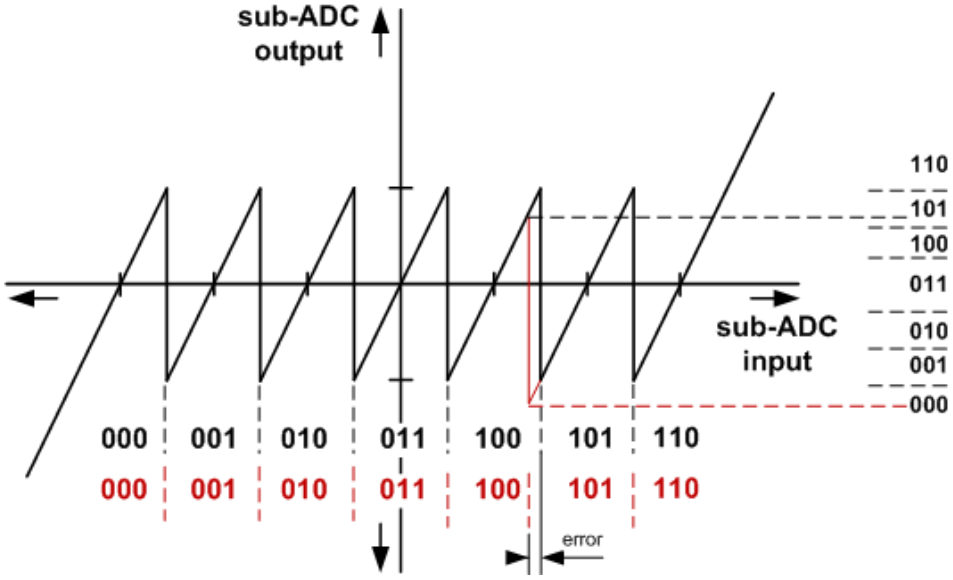


Figure 15: Transfer function of 2.5bit MDAC with comparator offset error.

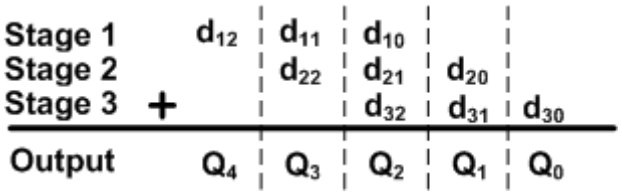


Figure 16: RSD correction principle

The 2.5 bit MDAC sends actually 2.5 bits into correction block, although half a bit is used as a correction bit in digital logic. The offset causes a shift between decision levels and in the end, it results in code miss-interpretation. To avoid these errors, RSD correction technique is often used in the literature [3],[4]. The partial MDACs outputs are cascaded, shifted by one position and added together. I other words, the most significant bit of first stage d_{12} is directly shifted to the output and produces digit Q_4. The second most significant bit d_{11} from first stage is added to most significant bit of second stage d_{22} and produces output Q_3, and so on. The visualization of these processes is shown in Figure 16. RSD correction technique can solve the over-range problem that

comes from comparator's offset. Comparison between function without offset of comparator, and with offset of comparator is shown in Figure 17, respectively in Figure 18. For case of 8-bit pipelined ADC, the total number of signals that are sensed by RSD correction block is 11 (Q_0-Q_{10}). The outputs of the correction block correspond to 8-bit digital signal (D_0-D_7). Now considering an example (Figure 18) where the comparator in stage 2 and 3 has some offset and produces an irrelevant output [2].

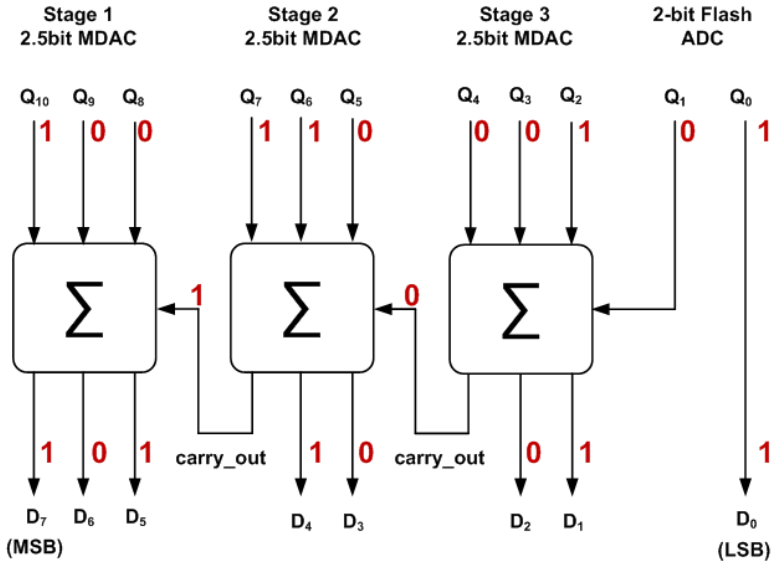


Figure 17: RSD correction function

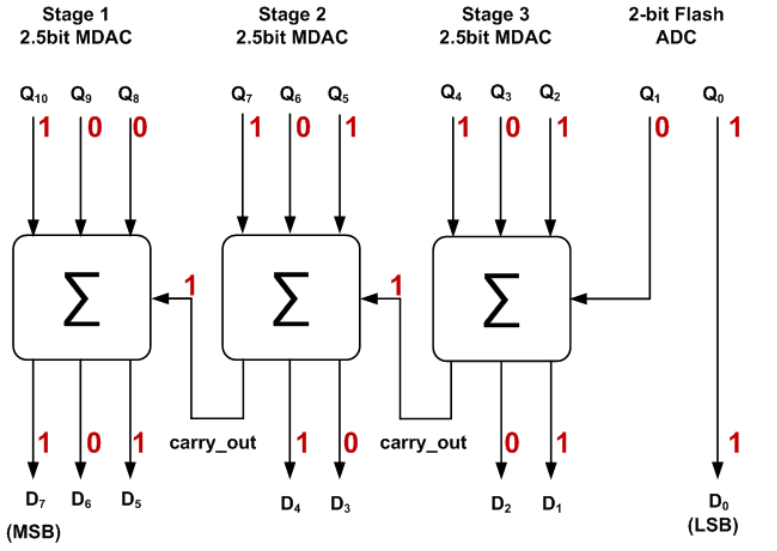


Figure 18: RSD correction function with comparator offset

The bits have changed in stage 2 (from 110 to 101) and in stage 3 (from 001 to 101). This forces the internal logic (it is made of half and full adders) to change its inner state to correct and hold the same output value.

It can be said, that the most significant bits from each stage are added to next stage (except stage 1). As mention earlier in the text, one conversion bit is used for correction. This functional approach helps with correcting the most severe errors as they will not appear in output digital word.

2.5 Calibration techniques

A number of calibration techniques can be found in the various resources. They are usually mixed signal techniques that help with improving performance over the frequency range and mainly over resolution. One of these techniques is called foreground calibration. This method uses an extra amount of additional circuitry to improve incorrect parameters during the conversion process. It can be said, that calibration algorithm influences the result of conversion.

The second type of calibration method is known as background calibration. The difference between the foreground and background calibration approach is that the foreground calibration does not force into conversion. Calibration mechanism corrects the output digital word passively. The advantage of foreground calibration is in its lower demand on system complexity, with respect to background calibration.

These techniques will be discussed later in practical part of document in chapter 5.

2.6 Influence of non-idealities on conversion process

As an every conversion process is encumbered by various errors, offset, uncertainties (in general non-idealities), the same applies for pipelined ADC. A presence of non-ideality degrades conversion specifications, such a speed, accuracy, resolution etc. The pipelined ADCs are always connected with switched capacitor design architecture.

Three main contributors of error are discussed a graphically displayed, in the chapter below. We will start with error mentioned earlier that can be compensated with using digital correction, as outlined in chapter 2.4 – comparator's offset voltage error.

2.6.1 Comparator offset voltage error

The offset voltage is the main error source in sub-ADC. The purpose of a comparator presence is to produce output signal, depending on the input signal. If the input signal is above reference level, the output goes high [3]. The offset voltage behaves as an additional voltage on the top of reference level causing increase or decrease the decision level. It results in possibility, that comparator makes a wrong decision. A number of sources can cause voltage offset, but the transistor mismatch is the main contributor. It is a trade-off for comparator's speed or accuracy.

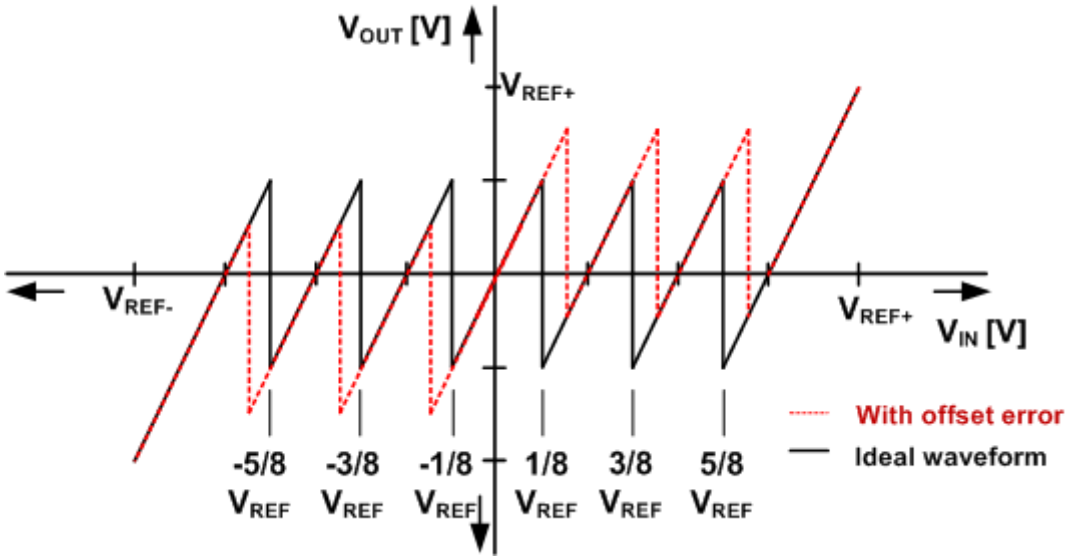


Figure 19: 2.5 bit MDAC transfer characteristic with offset voltage error

With smaller devices (transistors), the mismatch increases and the total comparator offset error increases as well. On the other hand, with larger devices the matching is improved, but the power consumption increases.

2.6.2 Finite DC gain of operational amplifier

An operational amplifier is one of the most critical blocks in pipelined ADC's implementation. Proper understanding and modelling impacts of non-idealities on pipelined ADCs performance are crucial.

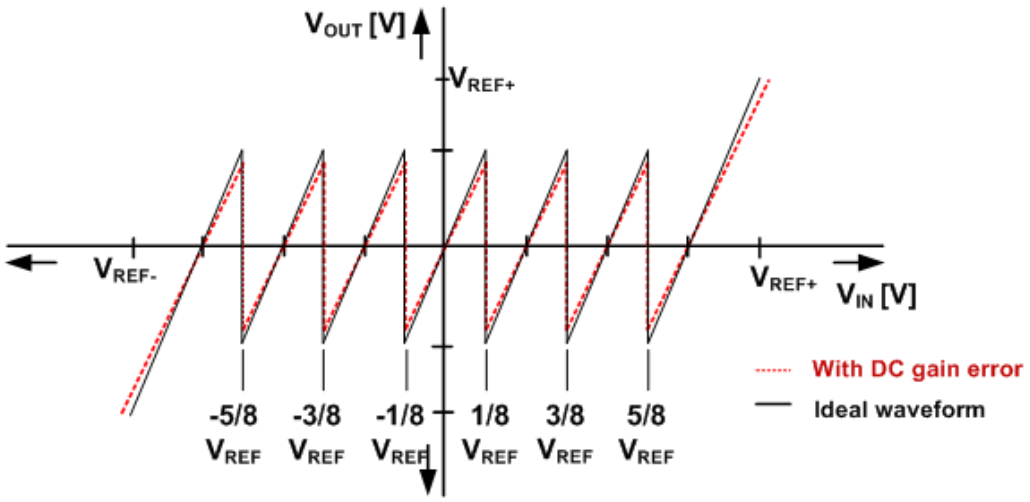


Figure 20: Finite DC gain and its influence on transfer function on 2.5 bit MDAC

The differential amplifier is usually made with use of switched capacitor structure as can be found in the paper [3]. From this source implies that the output of the MDAC can be described as

$$V_{RESx} = V_{RESx-1}\left(\frac{C_S + C_F}{C_F}\right) + V_{REF-} \cdot \left(\frac{C_S + C_F + C_P}{C_F}\right) - V_{DAC} \cdot \frac{C_S}{C_F}. \quad (13)$$

The feedback factor beta describes how much of the output voltage of operational amplifier is fed back to Op-Amp input and is given by,

$$\beta = \left(\frac{C_S}{C_S + C_F + C_P}\right). \quad (14)$$

The DC gain requirement can be obtained from (13).

The Op-Amp error gain should be smaller than ¼ LSB of remaining resolution and can be calculated from (14).

$$\frac{1}{A \cdot \beta} < \frac{1}{4} LSB \quad (15)$$

2.6.3 Finite bandwidth of operational amplifier

Finite bandwidth of Op-Amp is another important non-ideality to study in designing pipelined ADCs.

The settling behaviour of the Op-Amp in switched capacitor circuits is not entirely linear. The settling error is largest when the input signal voltage is close to $\pm V_{REF,}$ where the output voltage changes to full scale.

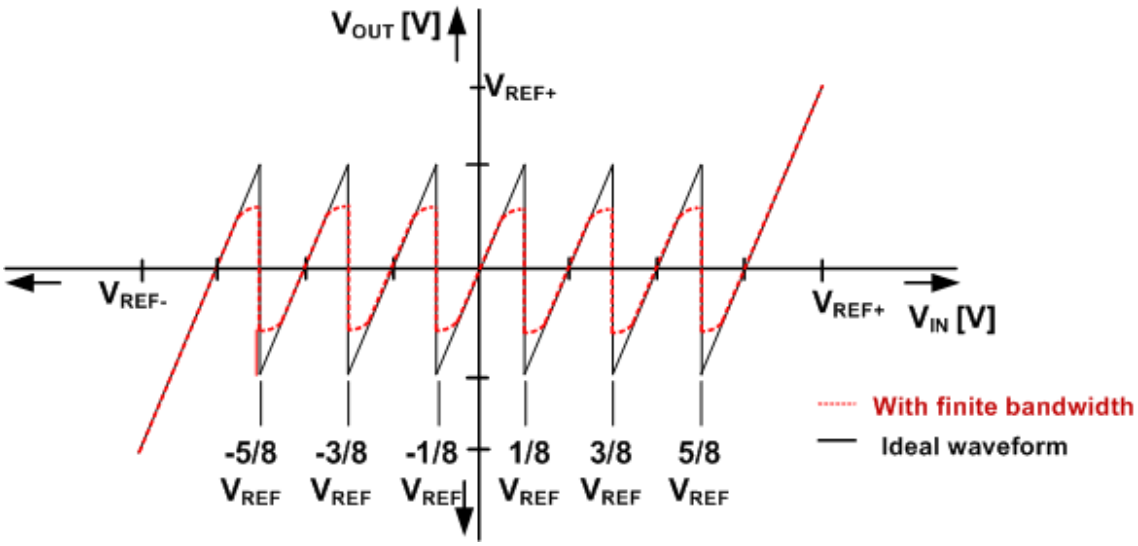


Figure 21: Finite Op-Amp bandwidth and it influence on transfer function on 2.5 bit MDAC

The consequence of settling error is harmonic distortion at the output. Therefore, the gain bandwidth of Op-Amp should be large enough to avoid harmonic distortion, caused by settling error [3]. The example of how the DC gain affects transfer characteristic is shown in Figure 21. The black line represents an ideal transfer function and the red dotted line shows transfer function with finite gain bandwidth.

2.6.4 Gain error of operational amplifier – capacitor mismatch

The gain of switched capacitor MDAC is given by a capacitor ratio. From that reason, it is necessary to produce capacitors that match as much as possible. The capacitor value is given by equation (16),

$$C = A \cdot \frac{\varepsilon_{oxid}}{t_{oxid}} = A \cdot C_{oxid} \tag{16}$$

Where A is the area of a capacitor, ε_{oxid} is the dielectric constant of silicon dioxide, t_{oxid} is the oxide thickness and C_{oxid} is a capacitance per unit area.

From equation above arises fact, that overall capacity is directly proportional to capacitor oxide thickness and its area. The improvement in capacity matching can be done by increasing the area. The integrated circuit capacitor can be determined as

$$C' = C + \Delta C\ , \tag{17}$$

where ΔC is a mismatch error of capacitor C. Then the ratio of C_F a C_S can be written as

$$\frac{C'_S}{C'_F} = \frac{C_S + \Delta C_S}{C_F + \Delta C_F}, \tag{18}$$

where C_F is a feedback capacity and C_S is a sample capacity in switched capacitors circuit[5].

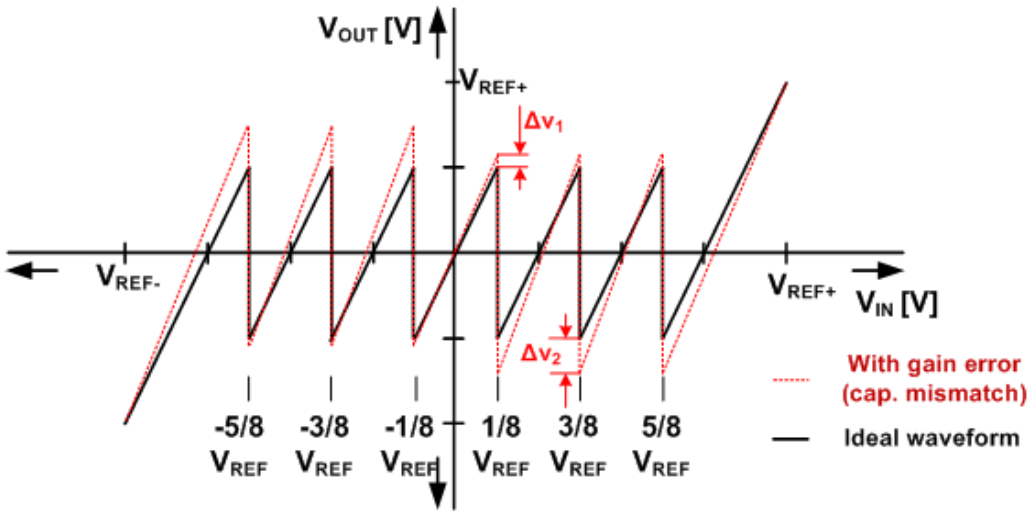


Figure 22: Gain error (capacity mismatch) and its influence on transfer function

The typical transfer function of 2.5-bit MDAC is shown in Figure 22. The black line represents an ideal transfer function and the red line shows a transfer function with capacitor mismatch.

PRACTICAL PART

This part of thesis is dedicated to MATLAB model creation. The main sources of error and non-idealities were described and the objective of next parts is to create functional model that can emulate behaviour of the circuit. Also, the non-idealities are incorporated in model. The primary purpose of model creation is to simulate and determine the weak parts of design with aim to achieve best performance in given technology. In other words, the model will serve as a reference for oncoming work where real technology TSMC 0.18μm is used.

3 12-BIT PIPELINE ADC MODEL

The modern ADC architectures were introduced in theoretical part 1.2. The practical part aims to develop a simulation model of 12-bit pipelined ADC in Matlab environment. The detailed model structure is present in following parts concerning chosen topology and its advantages. The basic structure is taken from literature [2],[3],[4],[5],[12] and [14].

3.1 Model structure

Block model of 12-bit pipelined ADC model is shown in Figure 23. It consists of six stages. The first five stages are identical. Each individual stage is made of 2.5-bit sub-ADC, 2.5-bit MDAC, sample and hold circuit subtraction circuit and gain amplifier. The last stage is a 2-bit flash ADC. Corresponding to the introduced architecture in part 2.2.1 the residual signals from each block go to time correctional block where they are synchronized. Then the already synchronized signals pass to digital correction block (RSD correction block) where conversion errors are processed and corrected. Overall structure will be designed in switched capacitor technology, so the model includes block that emulates behaviour of SC technique.

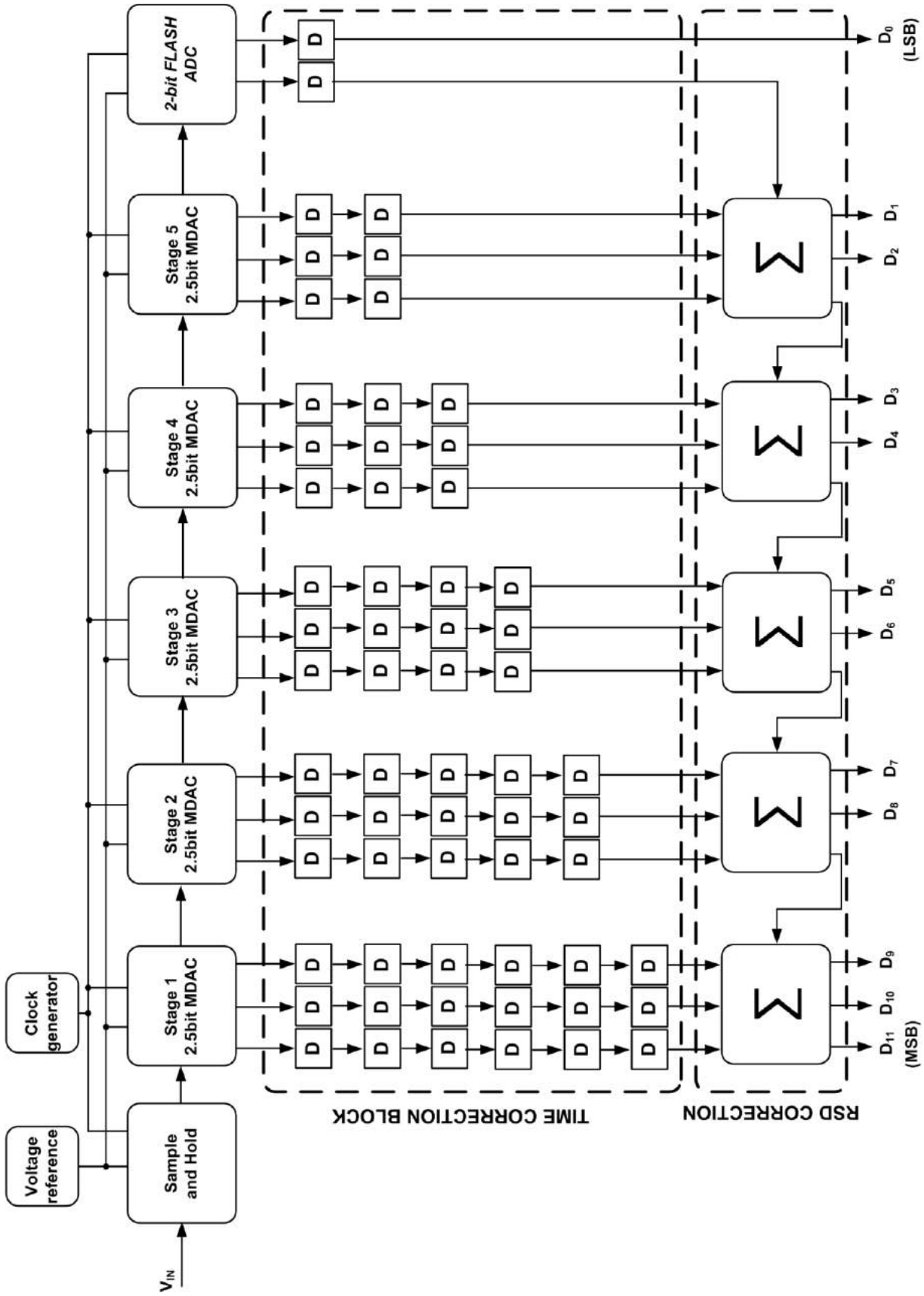


Figure 23: 12-bit pipelined ADC model with 2.5-bit MDAC, time correction and digital RSD correction block – block schematic

3.1.1 The 2.5-bit sub-ADC & sub-DAC model

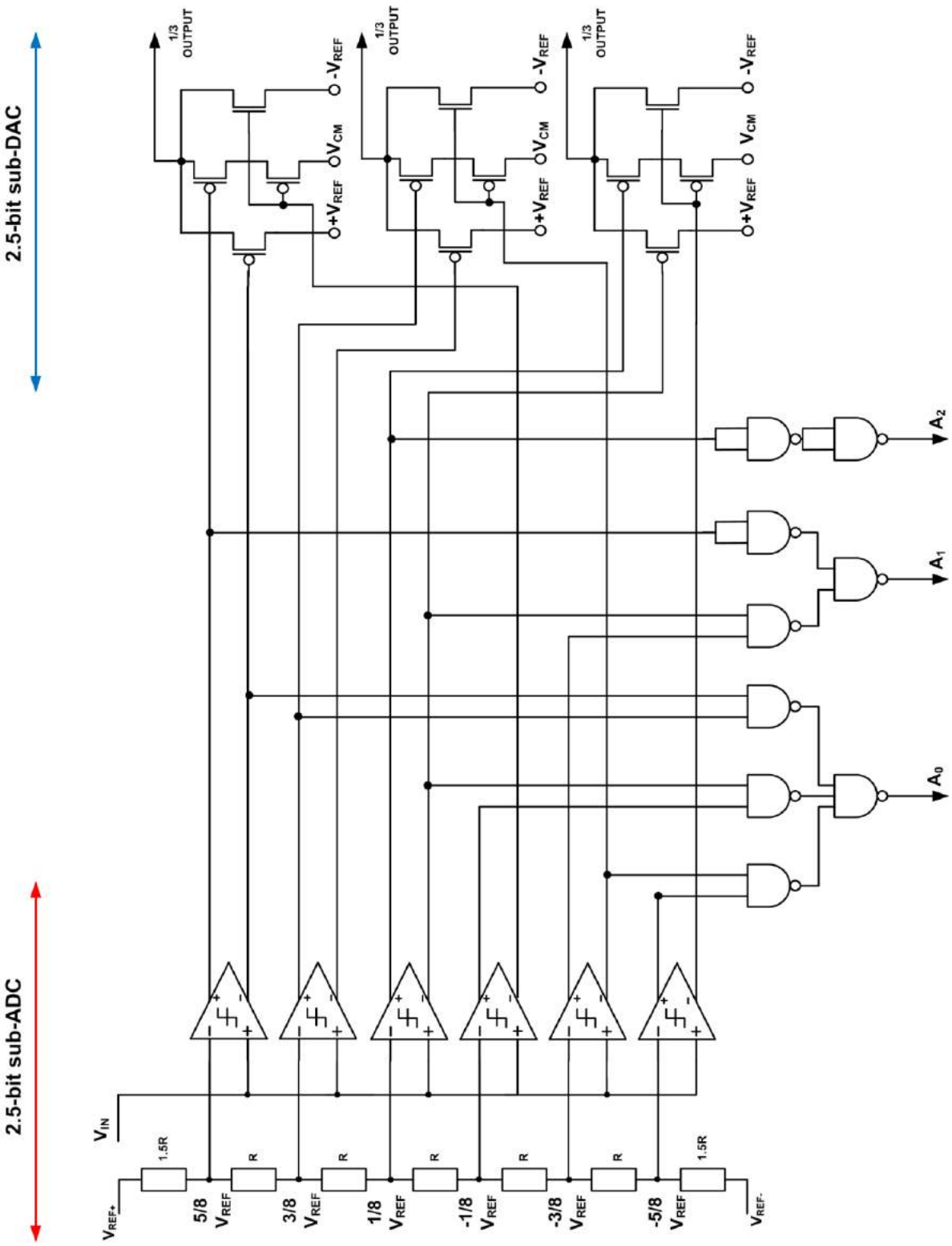


Figure 24: Sub-ADC and sub-DAC schematic for 2.5-bit MDAC – structural level [2].

The complete schematic of 2.5-bit MDAC is shown in Figure 24. It is created with use of six comparators, three 1.5-bit multiplexers, and NAND gates. The input signal V_{RESx-1} is compared with reference voltage using comparators in the first phase. Reference voltages V_{REF+} = 1V and V_{REF-} = -1V are set according to maximal amplitude of input signal that is 2V peak-to-peak. The outputs of the comparators are sensed by 1.5-bit multiplexers and are transformed to analog signal reversely. Every multiplexer creates one-third of total amplitude that is subtracted from input V_{RESx-1} in next phase. The truth table of sub-DAC is shown in Table 1.

Table 1: Sub-DAC truth table – summation of three multiplexers [2]

Sub-DAC output			**After summation**
V_{DAC2}	**V_{DAC1}**	**V_{DAC0}**	**$V_{DACtotal}$**
V_{REF+}	V_{REF+}	V_{REF+}	V_{REF+}
V_{REF+}	V_{REF+}	V_{CM}	2/3 V_{REF+}
V_{REF+}	V_{CM}	V_{CM}	1/3 V_{REF+}
V_{CM}	V_{CM}	V_{CM}	V_{CM}
V_{CM}	V_{CM}	V_{REF-}	1/3 V_{REF-}
V_{CM}	V_{REF-}	V_{REF-}	2/3 V_{REF-}
V_{REF-}	V_{REF-}	V_{REF-}	V_{REF-}

The output of the comparator goes to encoding logic that uses NAND gates and converses the signal into desired code. These outputs then pass to time correction block, where they are synchronized. A truth table and function description of relation between sub-ADC, output code, and sub-DAC is summarized in Table 2.

Table 2: Sub-ADC and sub-DAC truth table [2]

Input signal	**Output code**			**Sub-DAC output**		
V_{RESx-1}	**A_2**	**A_1**	**A_0**	**V_{DAC2}**	**V_{DAC1}**	**V_{DAC0}**
$V_{RESx-1} > 5/8V_{REF}$	1	1	0	V_{REF+}	V_{REF+}	V_{REF+}
$5/8V_{REF} > V_{RESx-1} > 3/8V_{REF}$	1	0	1	V_{REF+}	V_{REF+}	V_{CM}
$3/8V_{REF} > V_{RESx-1} > 1/8V_{REF}$	1	0	0	V_{REF+}	V_{CM}	V_{CM}
$1/8V_{REF} > V_{RESx-1} > -1/8V_{REF}$	0	1	1	V_{CM}	V_{CM}	V_{CM}
$-1/8V_{REF} > V_{RESx-1} > -3/8V_{REF}$	0	1	0	V_{CM}	V_{CM}	V_{REF-}
$-3/8V_{REF} > V_{RESx-1} -5/8V_{REF}$	0	0	1	V_{CM}	V_{REF-}	V_{REF-}
$V_{RESx-1} > 5/8V_{R} > _{EF}$	0	0	0	V_{REF-}	V_{REF-}	V_{REF-}

As it was said earlier, the converted signal has to be subtracted from input signal, to produce residual signal. Furthermore, it needs to be amplified to full-scale range. This is achieved with differential amplifier [2]. The complete model of 2.5-bit MDAC in Matlab is shown in Figure 25.

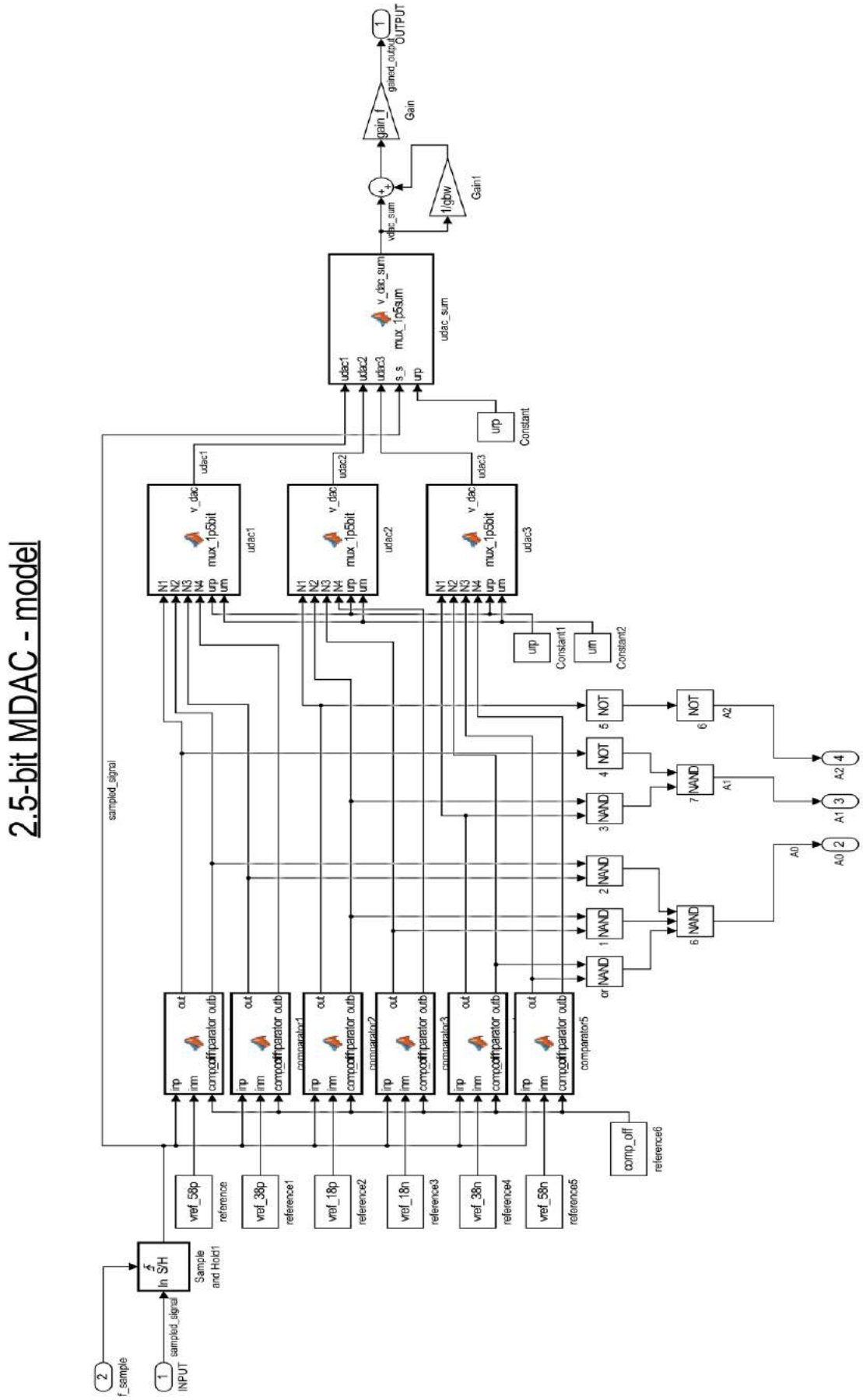


Figure 25: Real schematic of 2.5-bit MDAC in Matlab environment

The Figure 25 shows internal circuitry of 2.5-bit MDAC that emulates real pipelined ADC behaviour in SC technique. The particular blocks are modelled by behavioural description. The reasons for that are practical. The behavioural model facilitates the same functionality as gate level model. This approach can be exploited for modelling wide variety of circuits in Matlab environment if the functionality of circuit isknown. The circuit function can be expressed as a truth table or as mathematical expressions. It was decided to model the particular blocks behaviourally because the necessary data are presented in literature [2],[3],[4],[12] and [14] on which the work is based. The reference voltage levels are produced via pre-determined constants instead of resistor divider as is described in Figure 24. In this part, it is not necessary to include errors caused by resistor divider mismatch. As it corresponds to function mentioned earlier, the input voltage passes to comparators. There is it decided, whether the voltage is above the reference level or not. This produces output digital signal that address the multiplexers. The 1.5-bit multiplexers function is based on the data from Table 2.

The next necessary part of model is a summation block. As was mentioned above, the subtraction in SC technique is made by differential amplifier. This functionality represents behavioural description of the MDAC in model. Table 3 fully explains the relation between input signal V_{RESx-1} and output signal V_{RESx}.

Table 3: Table of multiplexers output summation [2]

Condition	V_{RESx} [V]
If $V_{RESx-1} > 5/8\ V_{REF+}$	$4V_{RESx-1} - 3\ V_{REF+}$
If $5/8\ V_{REF+} > V_{RESx-1} > 3/8\ V_{REF+}$	$4V_{RESx-1} - 2\ V_{REF+}$
If $3/8\ V_{REF+} > V_{RESx-1} > 1/8\ V_{REF+}$	$4V_{RESx-1} - V_{REF+}$
If $1/8\ V_{REF+} > V_{RESx-1} > 1/8\ V_{REF-}$	$4V_{RESx-1}$
If $1/8\ V_{REF-} > V_{RESx-1} > 3/8\ V_{REF-}$	$4V_{RESx-1} + V_{REF+}$
If $3/8\ V_{REF-} > V_{RESx-1} > 5/8\ V_{REF-}$	$4V_{RESx-1} + 2\ V_{REF+}$
If $V_{RESx-1} < 5/8\ V_{REF-}$	$4V_{RESx-1} + 3\ V_{REF+}$

The error sources such as Op-Amp gain error, comparator voltage offset, and Op-Amp finite DC gain are parts of real design. These non-idealities are also implemented in the model.

Modelling comparator offset voltage:

The additional voltage can be added to comparator reference via constant *comp_off*. This facilitates the option to model comparator's offset voltage and observe its influence on conversion process and transfer characteristic of MDAC.

Modelling Op-Amp gain error:

The capacitor mismatch or Op-Amp gain error can be modelled with error amplifier when gain ≠1 (parameter *gain_f*).The error amplifier is shown in Figure 25.

Modelling Op-Amp DC gain error:

The finite DC gain of the operational amplifier is designated as *A*0 and was mentioned in theoretical part. For this purpose, the model consists of another amplifier with gain = (1/ *A*0). The error portion formed by amplifier is then subtracted from output residual signal, which produces additional error that corresponds to finite gain of operation amplifier.

In previous chapters, the block, structural and behavioural structure was described. The simulation results and transfer characteristic, with discussion about functionality, are described later.

3.1.2 2-bit Flash ADC

The 2-bit Flash ADC is the last element in pipeline conversion chain. It facilitates full two-bit conversion as there is no need to produce residuum. It consists of three comparators and encoding logic, which converts the input signal to desired output value. The conceptual schematic is shown in Figure 26 and real Matlab model can be seen in Figure 27.

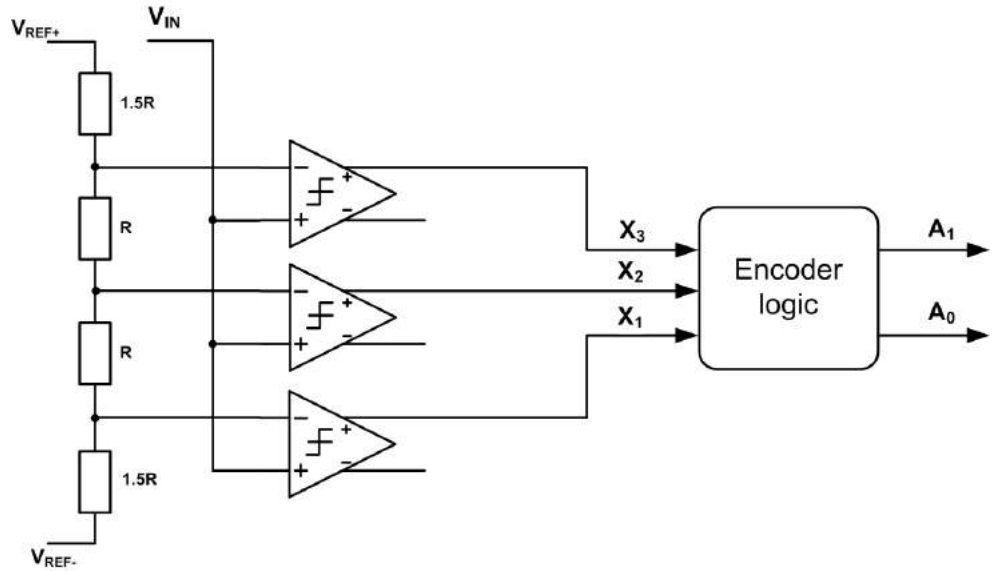


Figure 26: 2-bit Flash ADC – conceptual schematic [2]

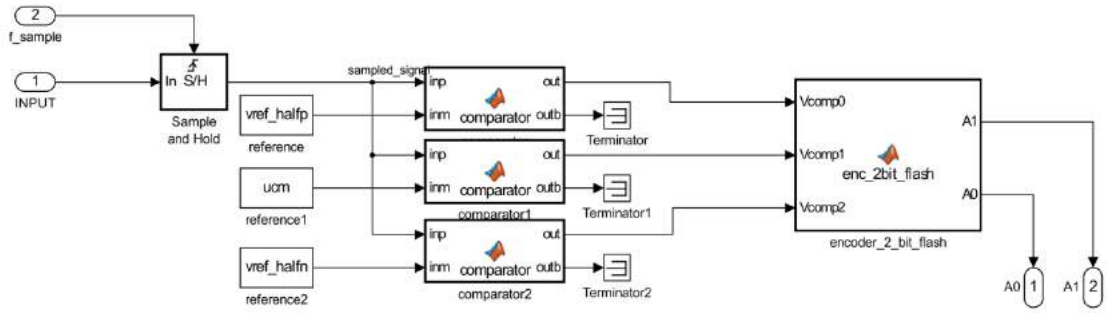


Figure 27: 2-bit Flash ADC – Matlab schematic

The input signal is sampled and fed to comparators inputs. The comparator makes a decision if the sample is above reference level or not and set its output accordingly to logical 1 or 0. The encoder logic in Matlab model uses these comparators outputs to produce the output code. This logic table is described in Table 4.

Table 4: Encoder logic truth table

Encoder input			**Encoder output**	
$\mathbf{V_{COMP2}}$	$\mathbf{V_{COMP1}}$	$\mathbf{V_{COMP0}}$	$\mathbf{A_1}$	$\mathbf{A_0}$
0	0	0	0	0
0	0	1	1	0
0	1	1	0	1
1	1	1	1	1

The difference between 2.5-bit sub-ADC and 2-bit flash ADC is that at the output of flash converter is full two-bit digital word – including combination 11.

3.1.3 Time correction block

This chapter is based on chapter 2.3 where time correction principle was described for 8-bit pipelined ADC. The situation is the same for 12-bit ADC. The only difference is in a number of stages (increased from 4 to 6) that has to be synchronized. The conceptual block schematic is shown in Figure 28 and the real model in Matlab can be seen in Figure 29.

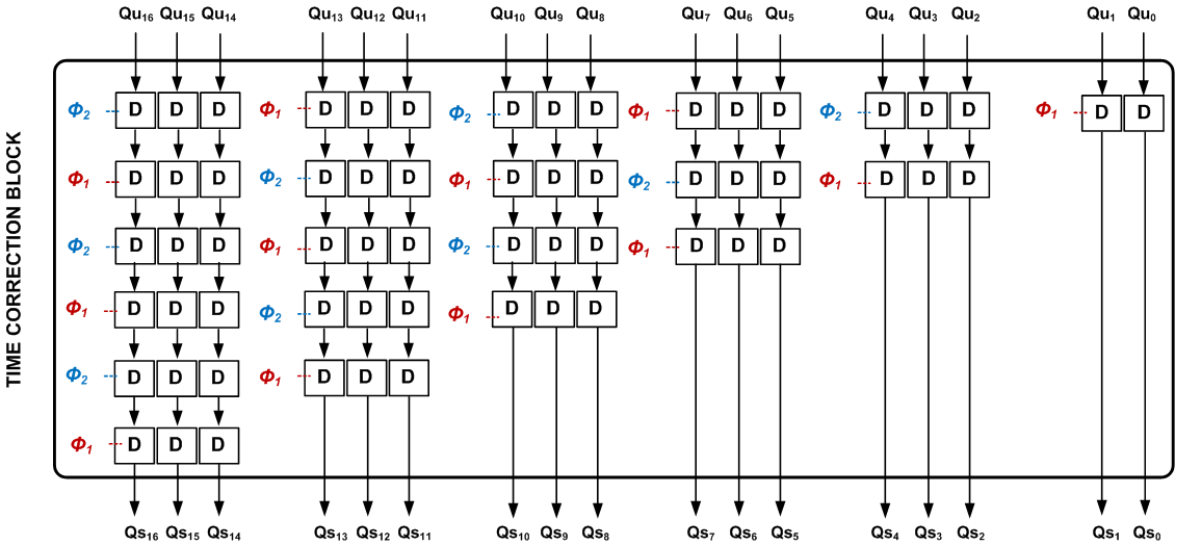


Figure 28: Conceptual block diagram of time correction for 12-bit pipelined ADC

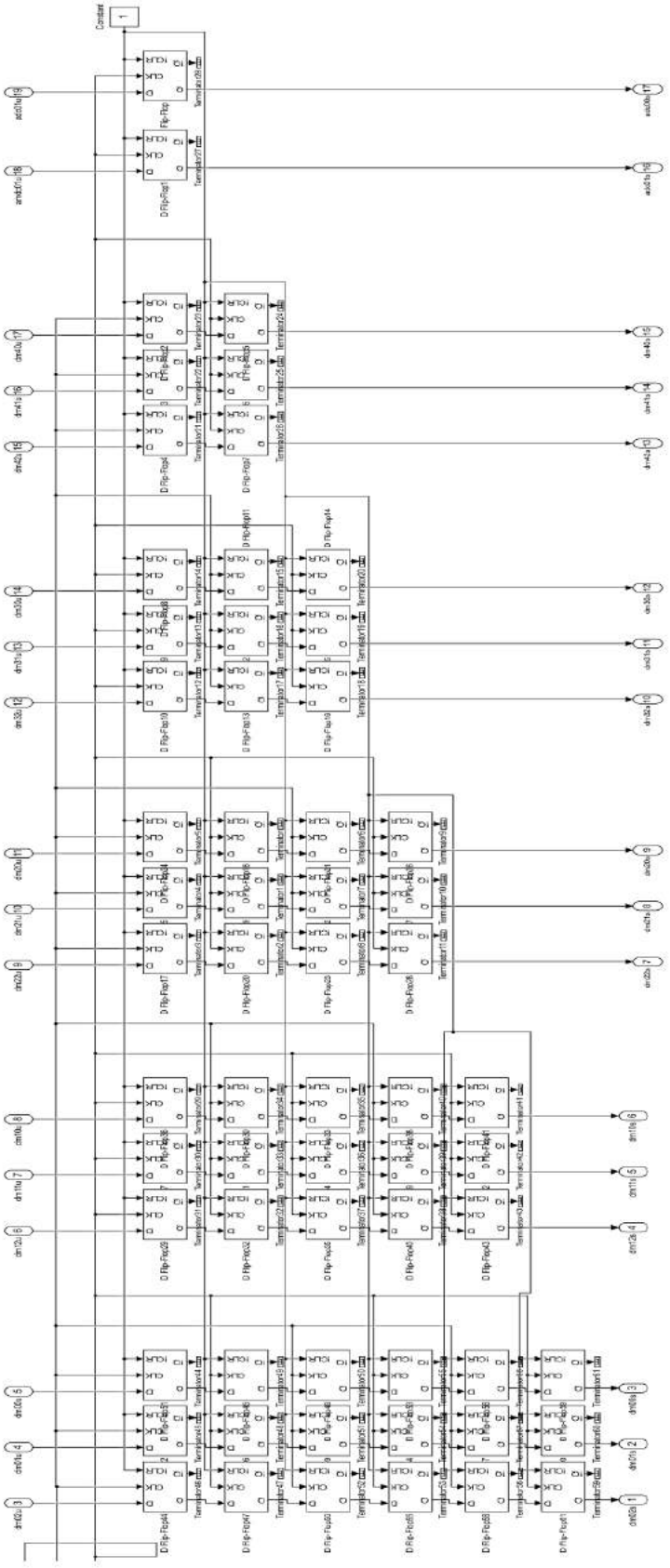


Figure 29: Time delay block for 12-bit pipelined ADC – Matlab schematic

As it was mentioned in part dedicated to time delay block explanation, the principle stays the same for 12-bit variant. Signals designated as $Qu_0 - Qu_{16.}$ (Figure 28) represent the unsynchronized digital outputs of each pipeline stage. The D Flip-Flops shift its inputs to the outputs accordingly to clock phase as is described in the picture. The clock phase Φ_2 is shifted by half of a sample period with respect to Φ_1. The synchronized outputs are marked as $Qs_0 - Qs_{16.}$ This structure guarantees, that the captured samples are synchronized in time and signals can forward to the last stage – to RSD correction block.

3.1.4 RSD correction block

Digital correction, described in part 2.4, is an important element in high-resolution pipelined ADCs. The 2.5-bit MDACs produce redundant codes and they are used for correction process. It widely improves the converter performance. Conceptual block schematic is shown in Figure 30 and Matlab implementation is described in Figure 31.

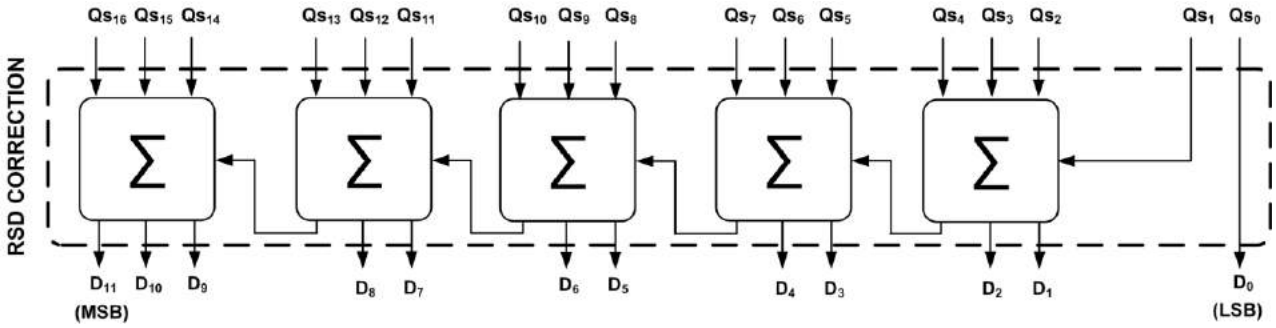


Figure 30: RSD correction block for 12-bit pipelined ADC – conceptual schematic

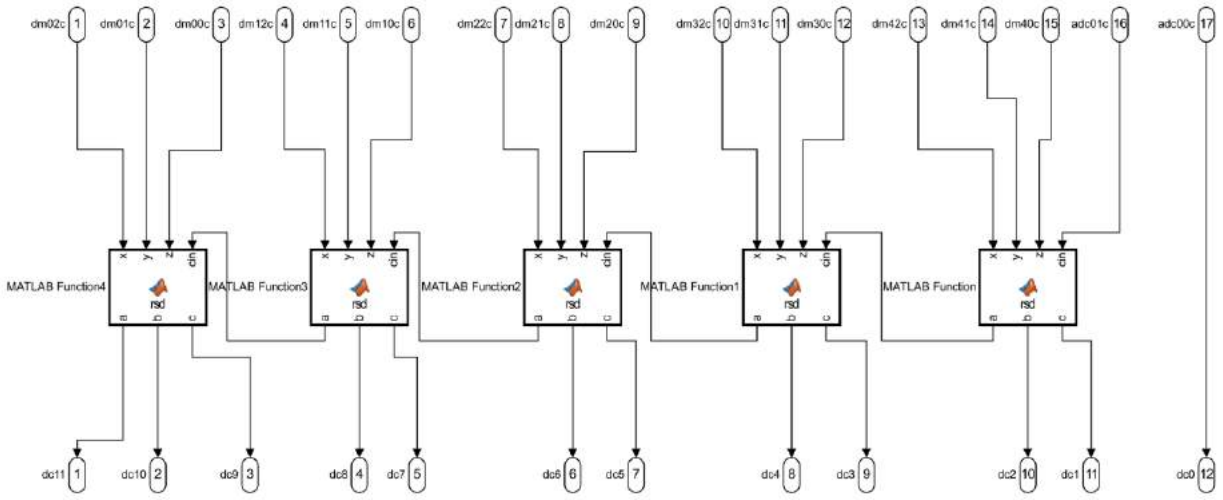


Figure 31: RSD correction block for 12-bit pipelined ADC – real Matlab implementation

When the signal passes through RSD correction block, the conversion is accomplished and the 12-bit digital word is prepared at the output. The whole Matlab model schematic is showed in Figure 32.

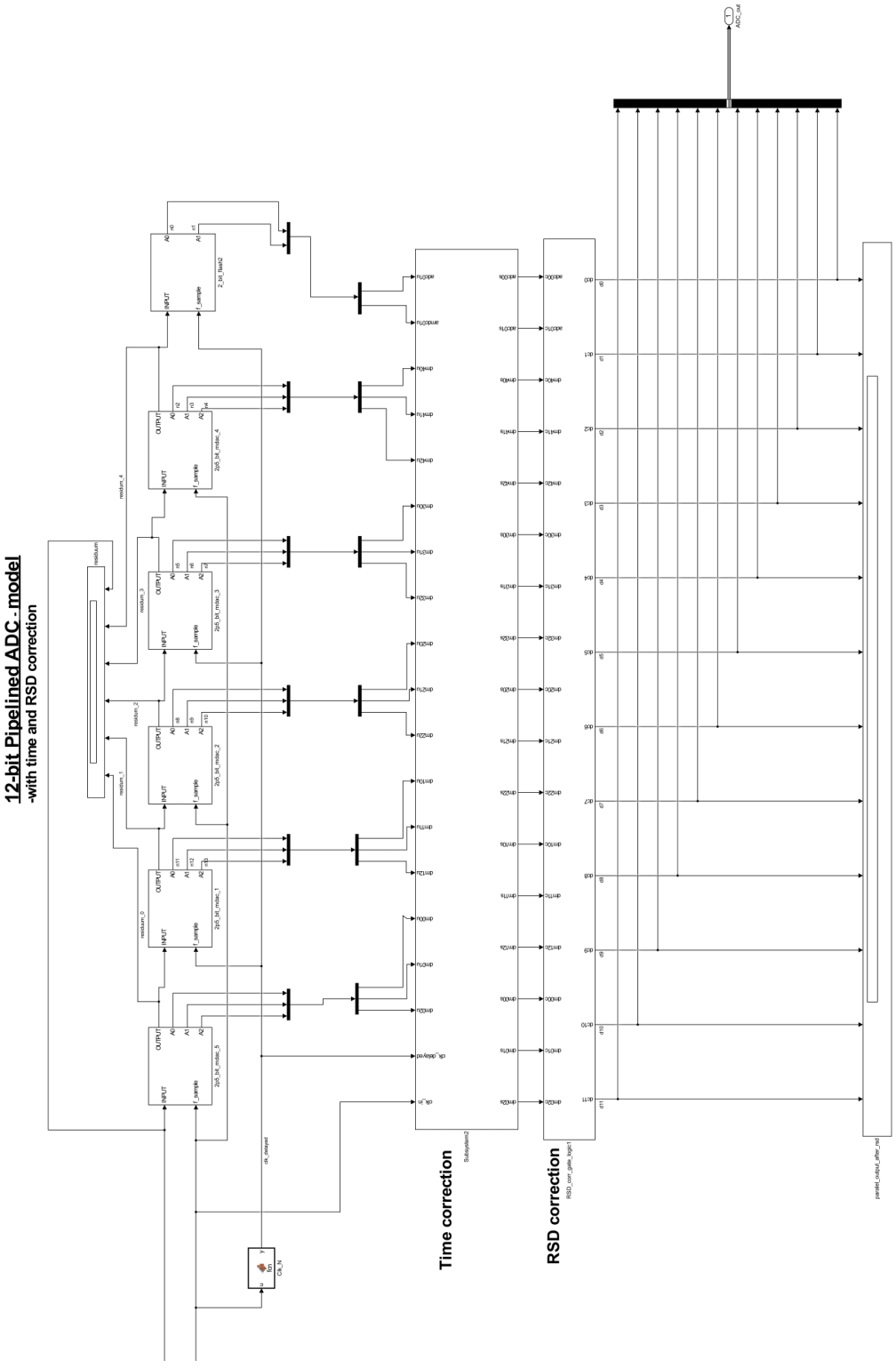


Figure 32: 12-bit pipelined ADC - top level schematic

Next part is dedicated to show practical simulation results and confirm theoretical expectations described in this document earlier.

3.1.5 Model functionality

Figure 33 shows the output of the ADC after conversion for ideal case. That means with presence of no non-idealities (offset, gain error etc.). The simulation parameters are as follows.

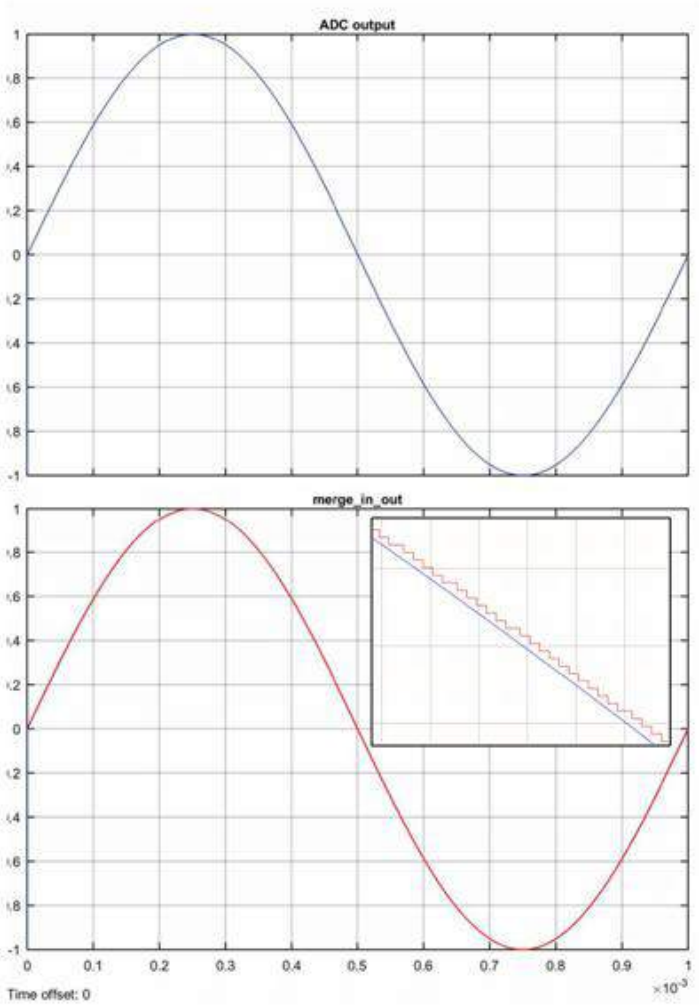


Figure 33 : Output of 12-bit pipelined ADC. Top – input signal, bottom – ADC output

Sample frequency F_{SAMPLE}=10MHz, input signal frequency F_{SIGNAL}=1kHz, input signal amplitude A_{SIGNAL}= 2V, common mode signal V_{CM}= 0V, reference voltages V_{REF+} =1V, V_{REF+} =-1V.

The MDAC output residue is shown in Figure 34.

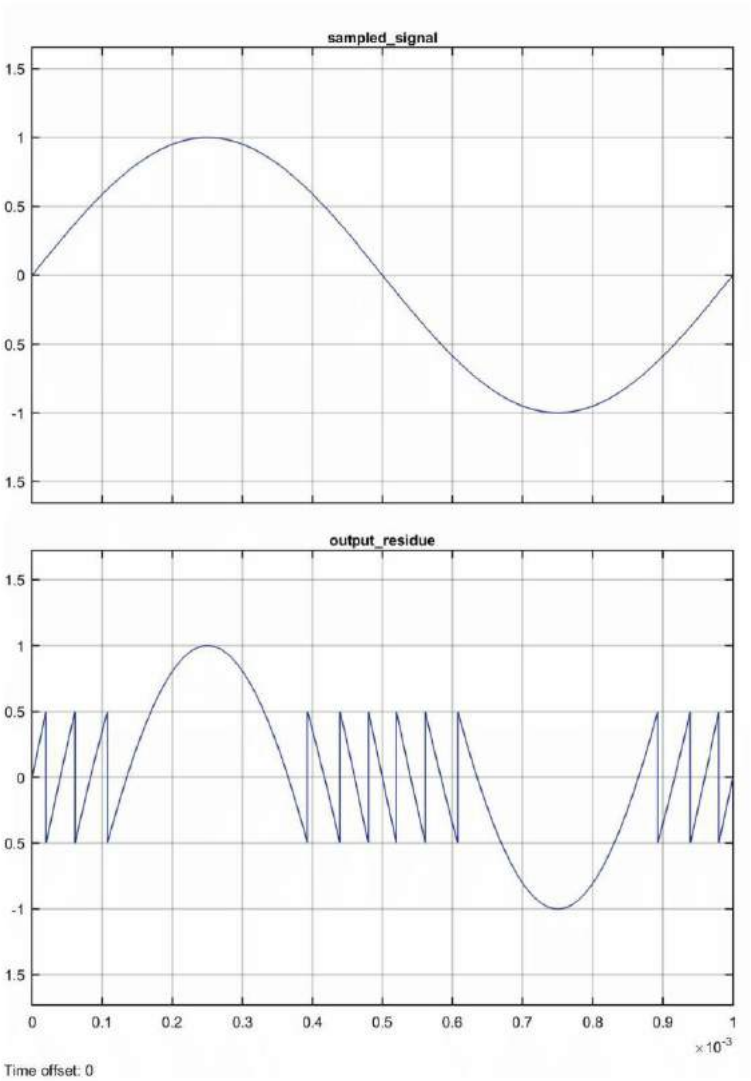


Figure 34: 12-bit pipeline ADC, first stage residue. Top – input sampled signal, bottom – residual signal at the output of 1st stage.

The output residue corresponds to theoretical expectations from articles [3],[4] and [5].

The rest of residual signals (signals between all stages) are shown in Figure 35.

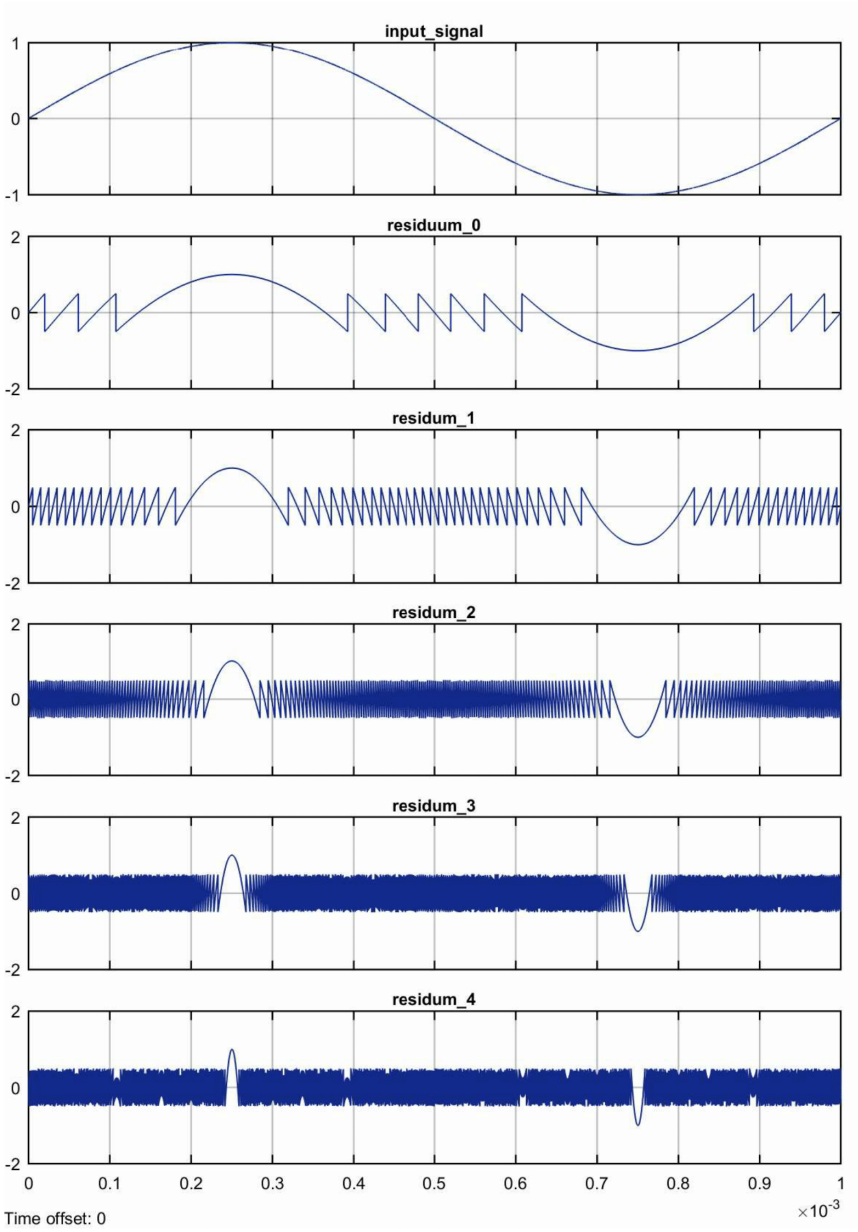


Figure 35: Residual signals at the end of each stage. Top – input signal, the others, residual signals for particular stages

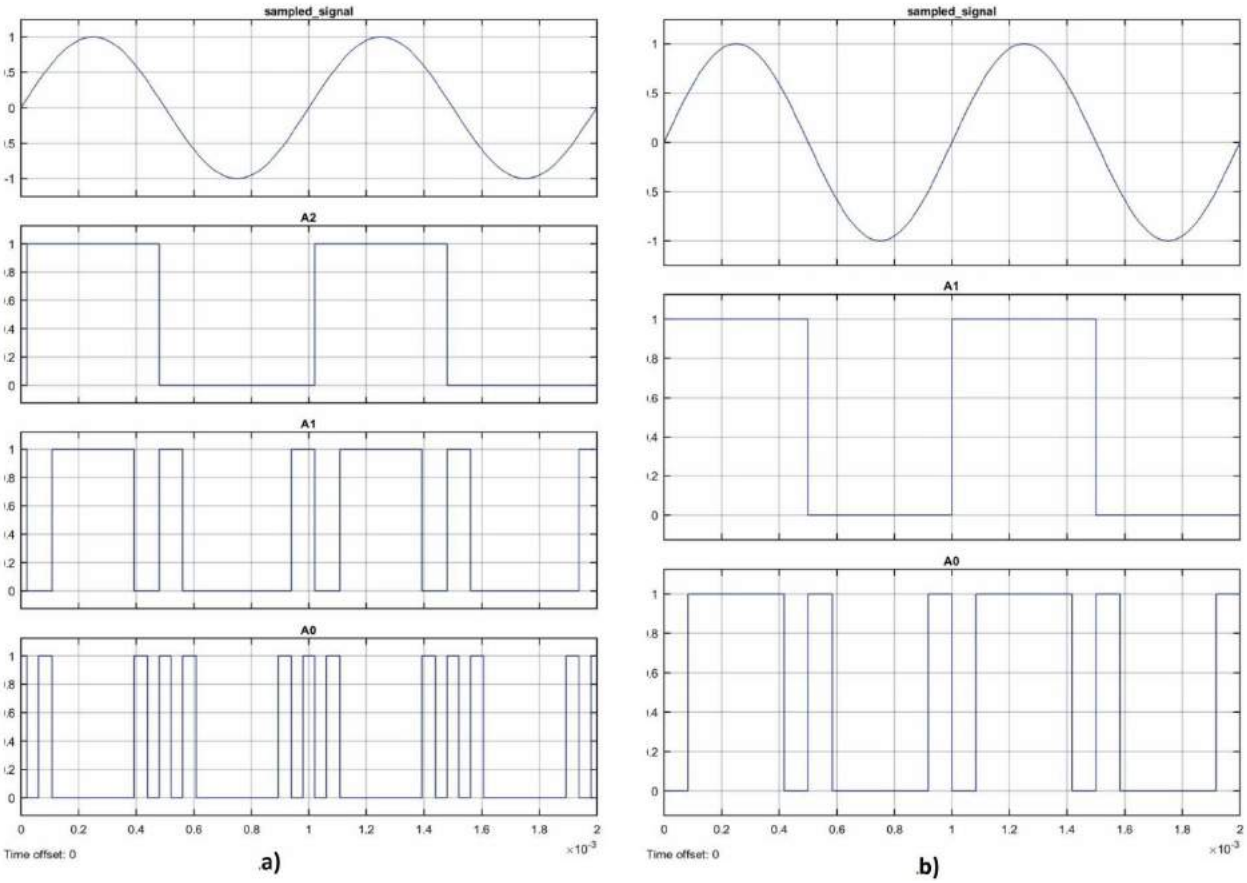


Figure 36: a) Outputs of 2.5-bit sub-ADC, b) outputs of 2-bit flash ADC

The important outputs of sub-ADC and 2-bit flash ADC are showed in Figure 36.

3.1.6 Ideal transfer characteristic – simulation

The ideal transfer function of 2.5-bit MDAC is plotted in Figure 37.

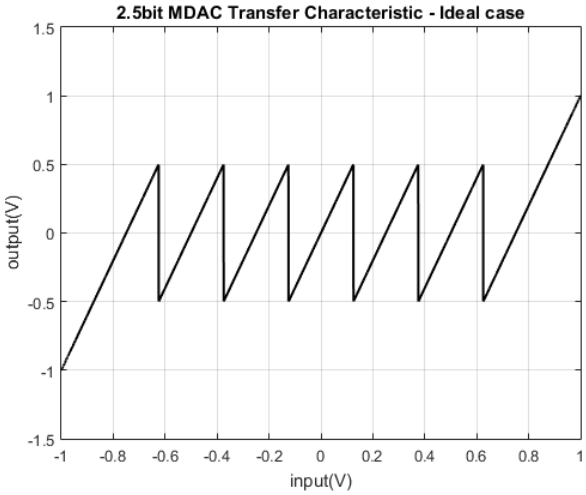


Figure 37: Ideal transfer characteristic of 2.5-bit MDAC – simulation result

Picture above describes and ideal transfer characteristic of 2.5-bit MDAC model and confirms model functionality. Theoretical (Figure 13) and simulated transfer functions (Figure 37) are identical.

The ideal waveforms such as INL, DNL, power spectral density and ADC output

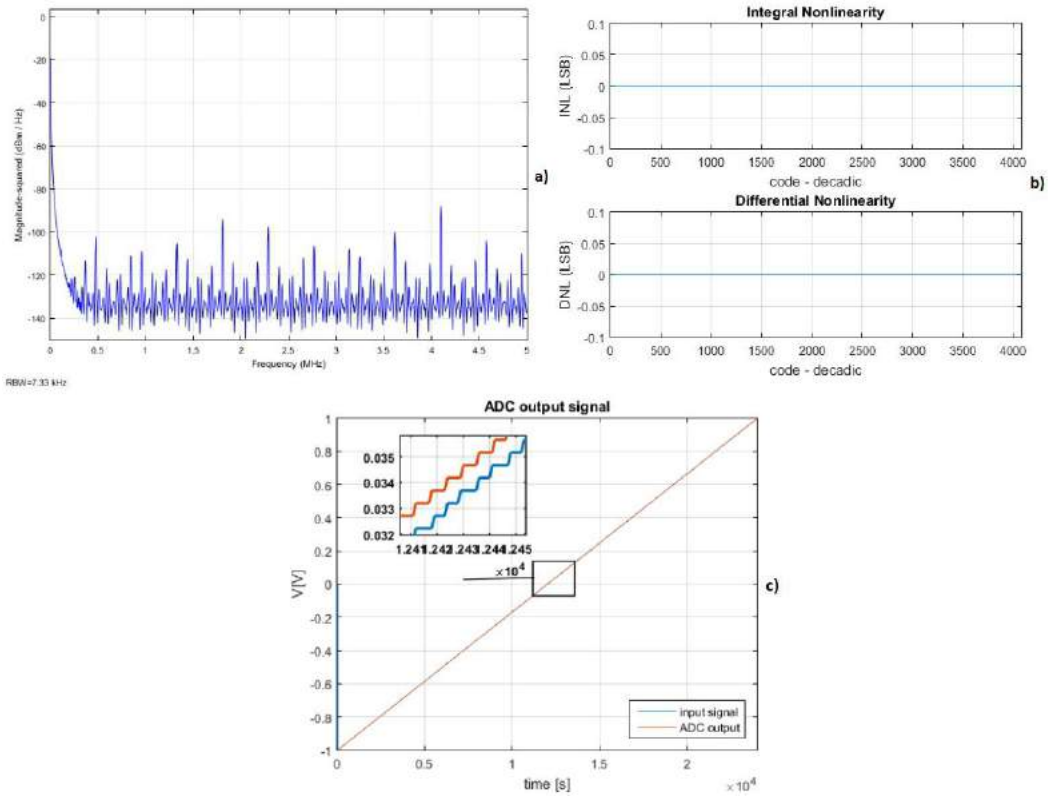


Figure 38: a) Ideal Power spectral density of the ADC output, b) ideal INL and DNL, c) output staircase function – simulation results

are shown in Figure 38. The output ADC signal has typical staircase shape with the step width of 1 LSB over whole operation range. This ensures that the INL and DNL equal to zero. The mean noise floor level reaches value 130dB in power spectral density diagram. Within these ideal conditions (no errors were involved) the ENOB is equal to 12 bit. Unfortunately, this resolution is very difficult to reach, because the errors are present in every real conversion process. To get closer to ideal specifications it is necessary to understand, which error parameter has got the highest influence on conversion process. The simulations with error contributors are presented in next chapter.

3.2 Conversion non-idealities – simulation

In following parts, the particular errors in simulation are introduced and discussed. The simulations aim to explain the influence of particular error, so the other error contributors are neglected. For example, if the comparator offset voltage error is under scope, the gain error and the finite DC gain of Op-Amp are suppressed and not taken into account.

3.2.1 Comparator offset voltage

This chapter is dedicated to discovering the real influence of mentioned errors on transfer function, and consequently on overall conversion process. The comparator

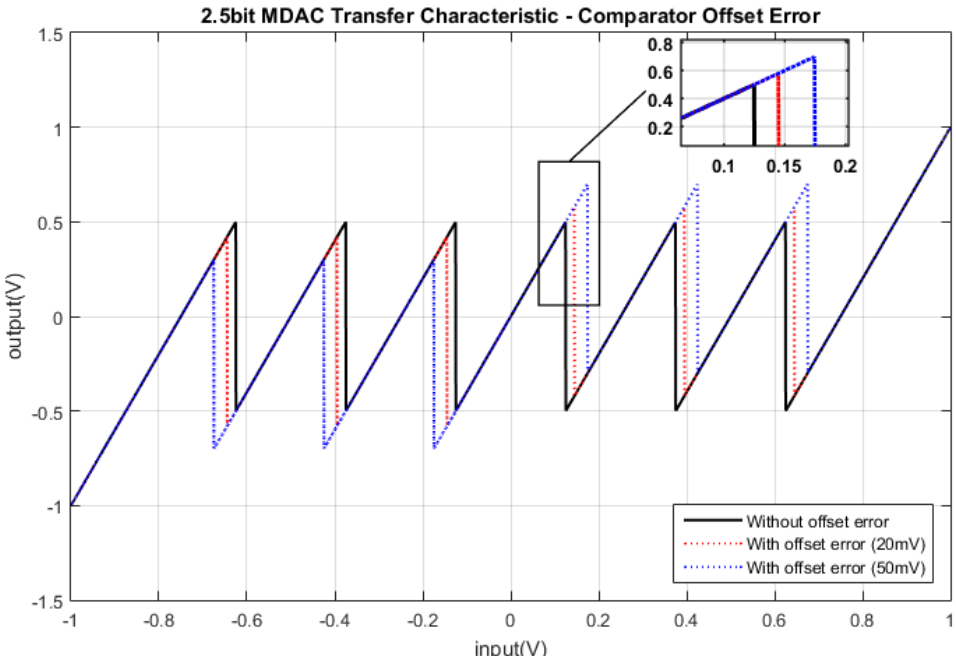


Figure 39: Influence of comparator voltage offset on transfer function – simulation result

voltage offset error is shown in Figure 39. Offset voltage of the comparator results in reference level shift that causes output code misinterpretation. The transfer characteristic appears to be shifted from ideal reference value to the right for positive reference levels and to the left for negative reference levels. The vertical shift is present in the picture as well. As the offset voltage increases, the shift is more significant. The simulation results for comparator offset voltage $V_{COMPerr}$ = 150mV are shown in Figure 40.

As the offset voltage increases, the staircase waveform starts to have some missing codes. The DNL and INL graph shows the amount of these presented errors. The power spectral density shows a noise floor level shift to approximately 110dB. However, it has to be mentioned, that 150mV offset voltage is really high value even in real process implementation. The offset voltage does not influence the accuracy specification until the mentioned value 150mV. The explanation for this comes from RSD block function. The RSD correction block can correct the gain over-shots caused by comparator. Once the offset error is higher than the limit, the RSD correction cannot fully handle out produced error and the offset occurs at the output. This value was determined by simulation exactly to 150mV.

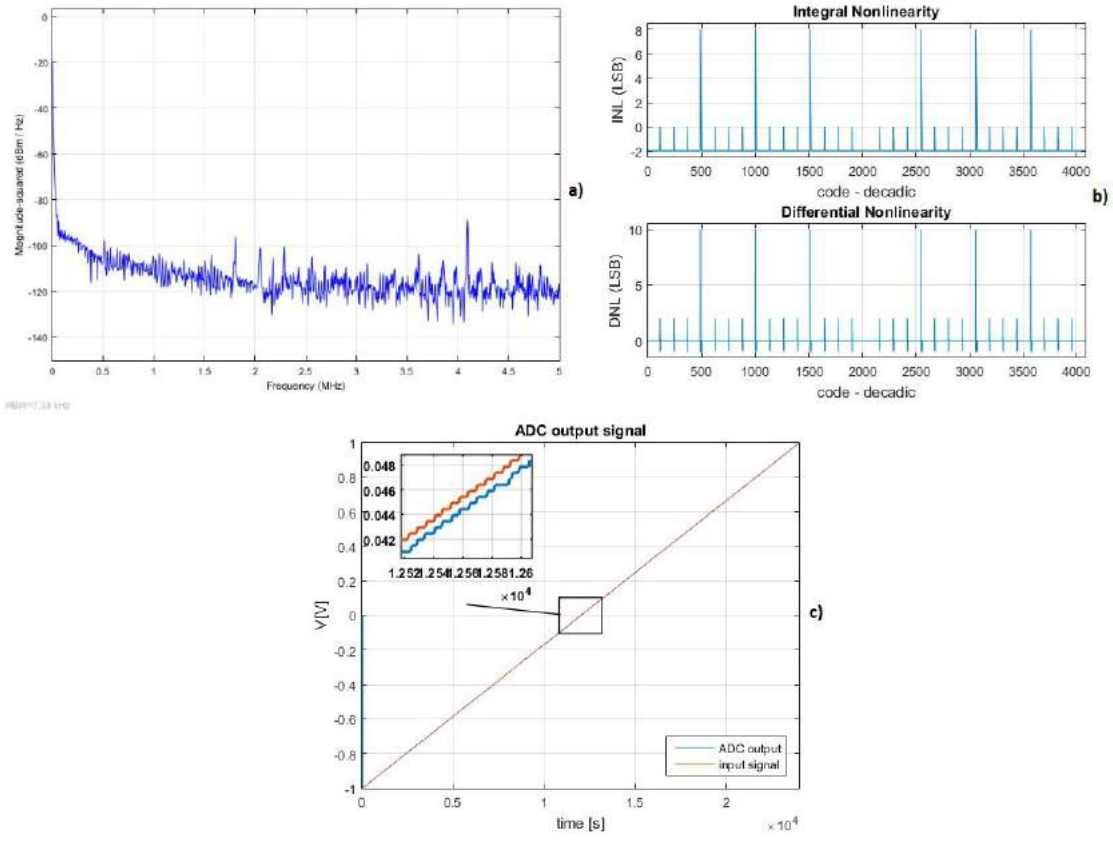


Figure 40: a) Power spectral density for ADC with 150mV offset error voltage,

b) corresponding INL and DNL and c) corresponding ADC transfer function.

As it implied in the paragraph above, the comparator offset voltage has got significant influence on conversion accuracy. On the other hand, it can be successfully compensated with RSD correction. In the end, it results in comparator offset specs relaxation because there is no need to design comparator with, for example, 1mV offset voltage specification.

3.2.2 DC gain error of operational amplifier

The finite DC gain error is plotted in Figure 41. Op-Amp's non-ideal DC gain causes a decrease in output voltage amplitude. The feedback factor β determines the amount of output voltage, that is fed back to input of the Op-Amp.

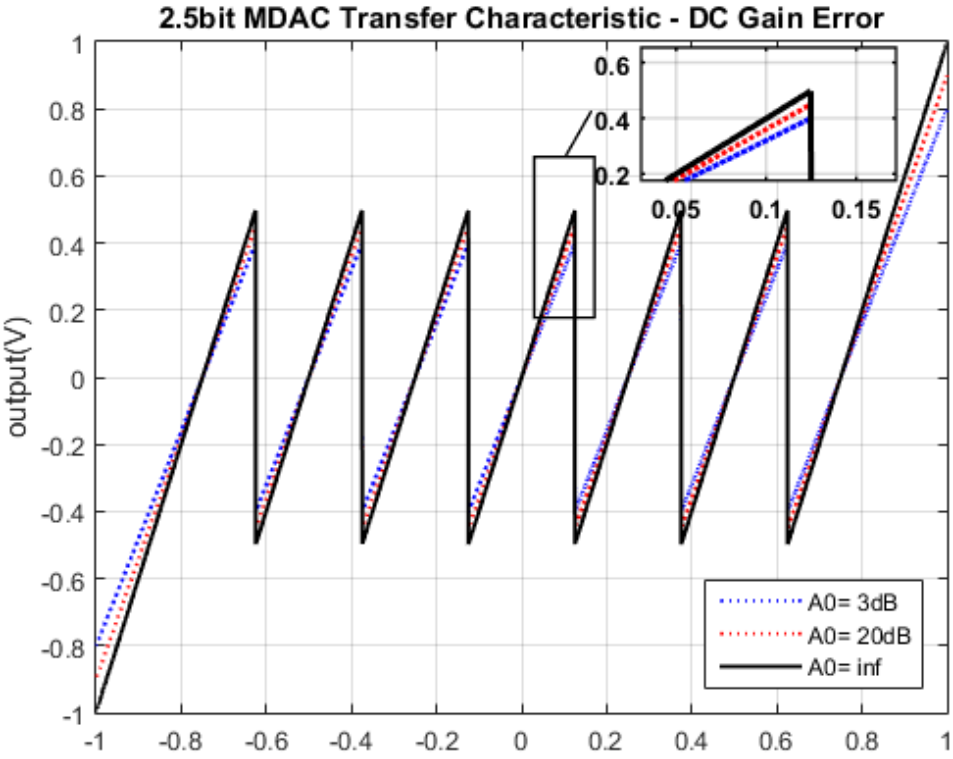


Figure 41: Influence DC gain error on transfer function

If we consider pipeline structure, the error in first block is projected to the next one, and causes another error increase. The Op-Amp DC gain has to be as high as the technology allows for high-resolution designs. Figure 42 shows the same characterization utilities as in previous two parts, but for finite DC gain of Op-Amp $A0$ = 50dB. This DC gain introduces error in MDAC and has influence on integral and

differential nonlinearity of converter. The 50dB finite DC gain shows its influence on conversion accuracy.

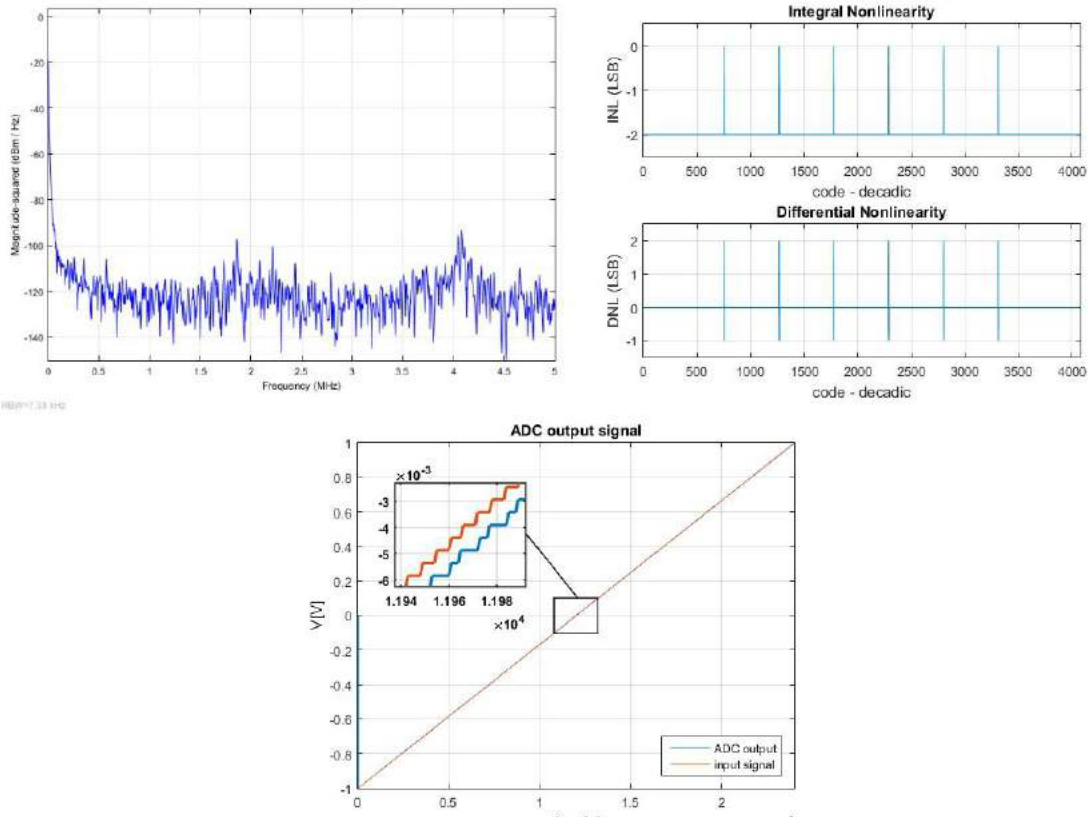


Figure 42: a) Power spectral density of ADC with 50dB DC gain ,b)corresponding INL and DNL, c) corresponding ADC output

The effect of DC gain error in DNL an INL characteristic disappears when the DC gain of Op-Amp increases to 60dB. This is the second parameter that was deducted from simulation results. It results in following conclusion. To obtain conversion without influence of finite DC gain, the DC gain should be larger than 60dB in real design application.

3.2.3 Gain error of operational amplifier - capacitor mismatch

If the capacitors are not sufficiently matched, the transfer characteristic gets stretched vertically. It means that output signal has a higher amplitude than the input

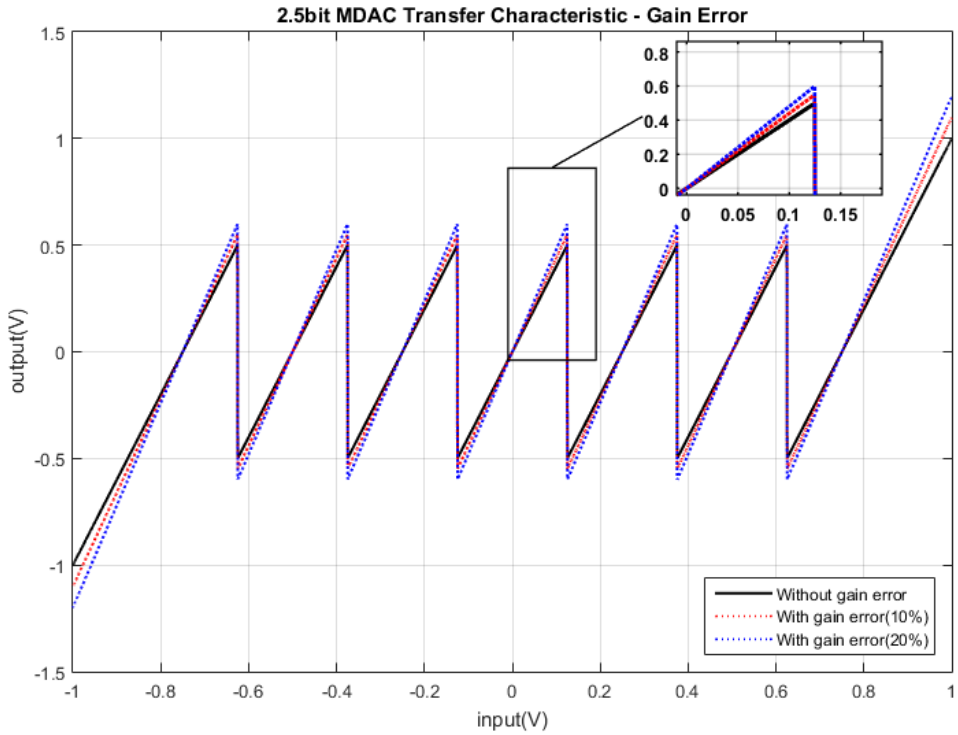


Figure 43: Influence of capacitor mismatch on transfer function

signal. This ratio uncertainty is responsible for the main error source in pipeline ADC architecture. Figure 44 shows a shifted power spectrum density for 1% gain mismatch, which is represented in SC circuits by capacitor mismatch ratio. The INL and DNL had increased and their occurrence over full-scale range became more frequent. The transfer characteristic became more rippled as well (Figure 44c).

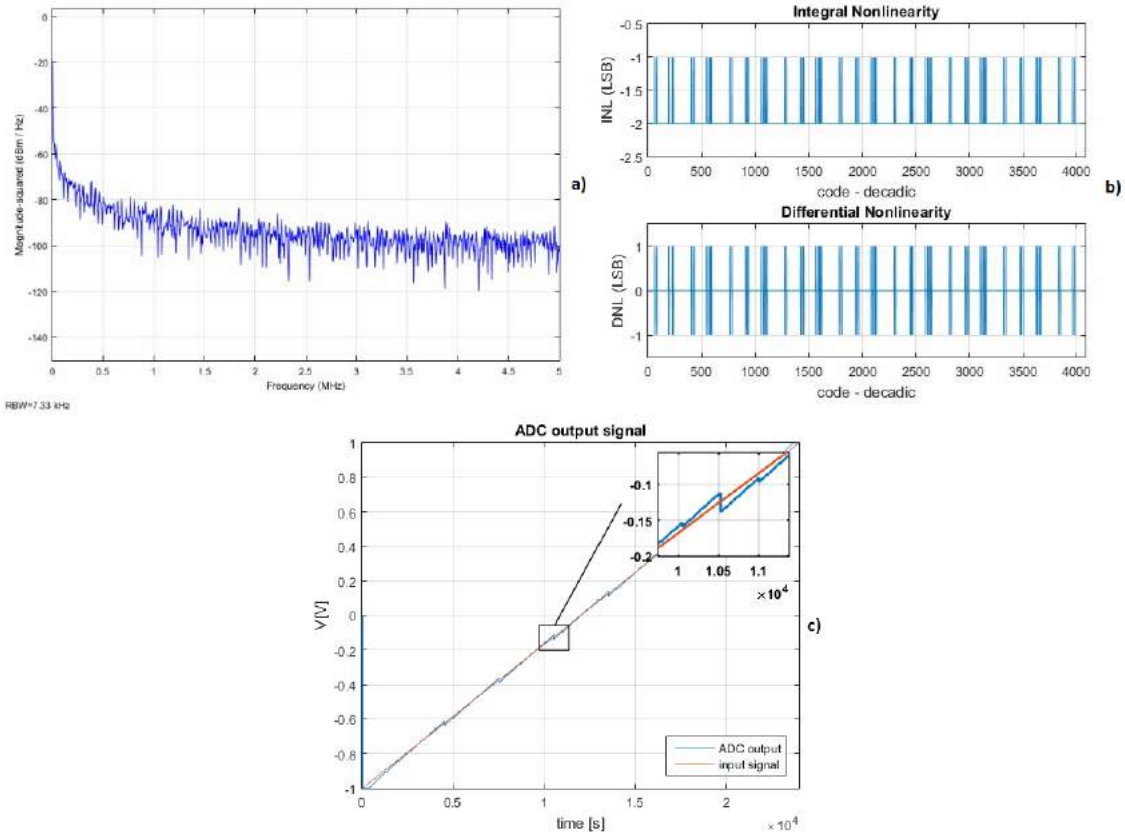


Figure 44: a) Power spectrum density for ADC with 1% capacitor mismatch error, b) corresponding INL and DNL, c) an ADC "rippled" output.

Figure 45 approaches the capacitor mismatch influence on SNDR and ENOB parameters. The FFT – Fast Fourier Transform was performed for the output of the ADC with following simulation parameters. The sample frequency F_{SAMPLE}=10MHz, the input signal frequency F_{SIGNAL}=500 kHz, the input signal amplitude A_{SIGNAL}= 2V, the common mode signal V_{CM}= 0V, reference voltages V_{REF+} =1V, V_{REF-} =-1V. The number of FFT points N_{FFT} =2048. The picture shows how the ENOB and SNDR parameters decrease with increasing capacitor mismatch.

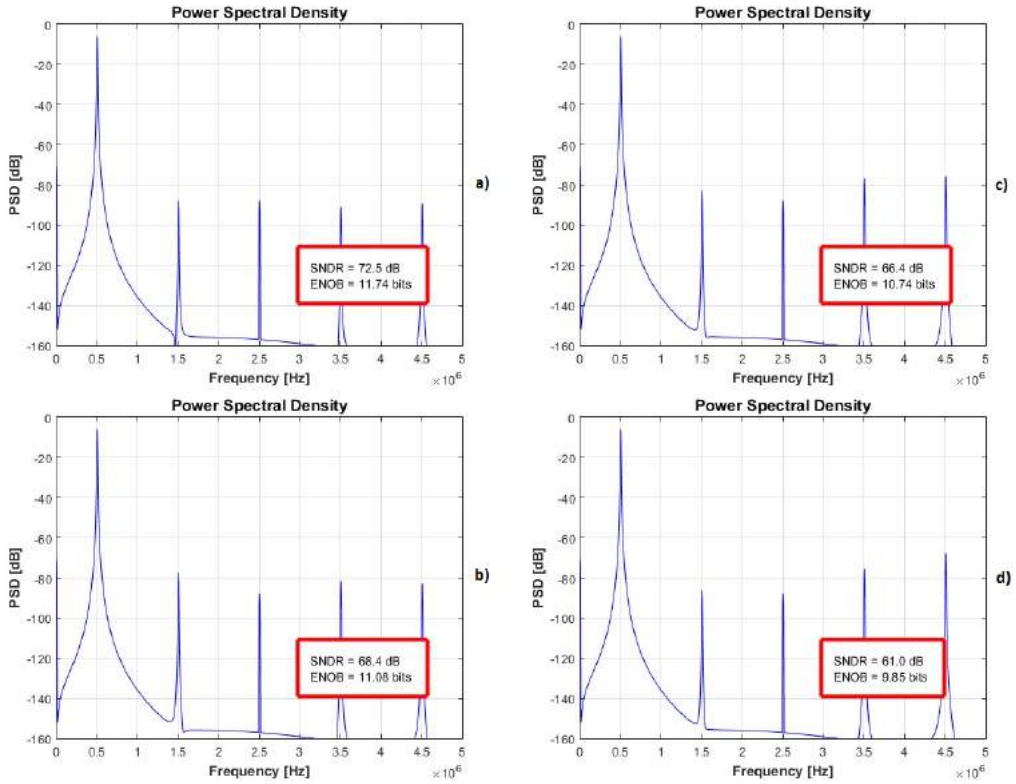


Figure 45: FFT for Op-Amp gain error a) 0.1%, b) 0.25%, c) 0.5% and d) 1%

3.2.4 Realistic parameters definition for transistor level design

As it was introduced, explained and proved in chapter 3.2, the non-idealities in conversion process can negatively influence all converter specifications. The minimal error parameter specifications were estimated to avoid (or at least eliminate) a presence of those errors in real design.

- the comparator offset voltage has to be lower than **150mV**,
- the Op-Amp DC gain (or the bandwidth) has to be larger than **60dB**,
- the Op-Amp gain error has to be lower than **0.1%**.

The estimated parameters are supported by numerous simulation results during a model development. The absolute maximal ratings of ADC conversion including conversion non-idealities are determined using ENOB and SNDR parameters and can be seen in Figure 46.

The following design work aimed to achieve this specification in TSMC 0.18µm technology.

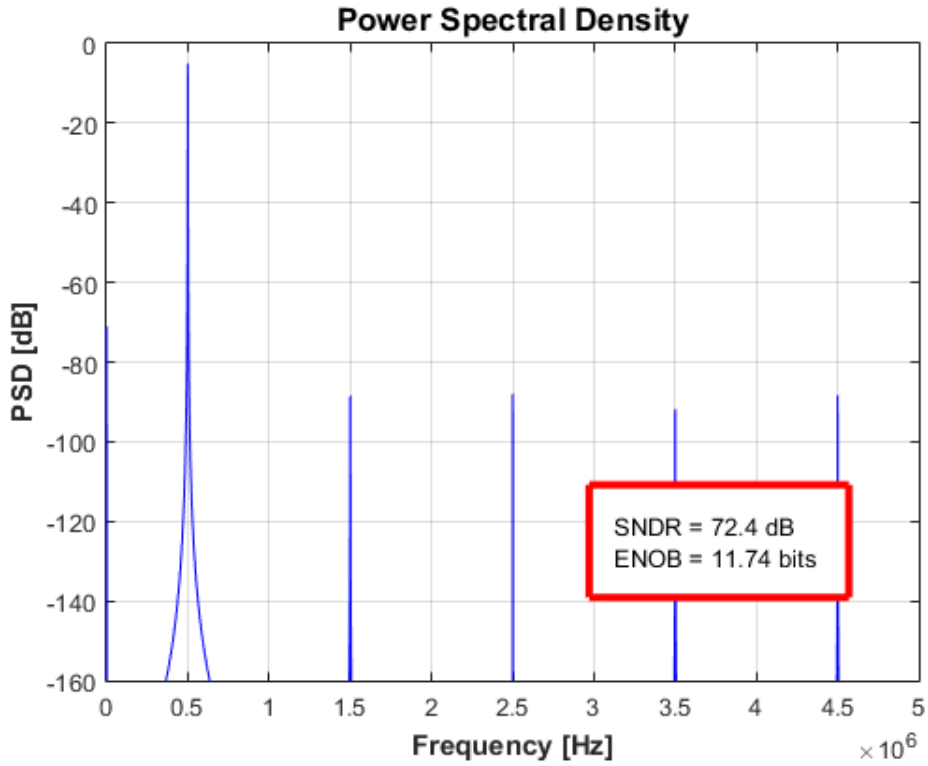


Figure 46: Maximal achievable ENOB and SNDR in model simulation ($A0$ = 60db, V_{OFFSET} =140mV, $A_{MISMATCH}$ = 0.1%)

4 12-BIT PIPELINE ADC DESIGN

Following chapter deals with description of fundamental blocks on transistor level that are further used in the design process. Moreover, chapter covers their design and results of particular simulations in TSMC 0.18μm technology with use of these main technological parameters:

Table 5: Technological parameters for TSMC 0.18μm

Cell name	Parameter description	Parameter	Corner(SS)	Corner(TT)	Corner(FF)	Units
nmos2v	Threshold voltage	V_{THN}	0.597	0.557	0.483	V
	Transconductance par.	KP_N	168	185	225	$\mu A/V^2$
pmos2v	Threshold voltage	V_{THP}	- 0.583	- 0.561	- 0.471	V
	Transconductance par.	KP_P	37	43	65	$\mu A/V^2$

The parameters above were simulated with use of self-made test benches from literature [16]. The reason to do this was to get the most precision values of parameters and get closer to realistic simulation results. All the parameters were evaluated with 1.8V power supply.

4.1 Comparator

The comparator is one of the most used circuits in analog design. It behaves as a 1-bit DAC and converts the input analog signal into binary output value. The name comes from its functionality because it compares two analog inputs resulting in corresponding two-state output value. The design of comparator in pipelined ADC directly affects the accuracy and power dissipation of the overall converter as was proven in chapter 3.

The comparators are used in sub-ADC and in 2-bit Flash ADC in this design. Each comparator is composed of pre-amplifier with positive feedback and R-S latch and is shown in Figure 47. When CLK signal is low, NMOS transistor M6 is off, PMOS transistors M7 – M10 are on, and nodes *R, S, X*, and *Y* are pre-charged to A_{VDD} placing the comparator in the reset mode. When CLK goes high M6 turns on and M1 and M2 compare the input signal V_{INP} with reference voltage on terminal $V_{INM.}$ Since M0-M3 are initially off, the resulting differential current flows through the total parasitic capacitance represented at nodes *X* and *Y*, creating a differential voltage at these nodes by the time M2 and M3 turn on. When cross-coupled transistors M2-M3 and M0-M1 turn on, the circuit regeneratively amplifies the voltage, producing rail-to-rail swings at

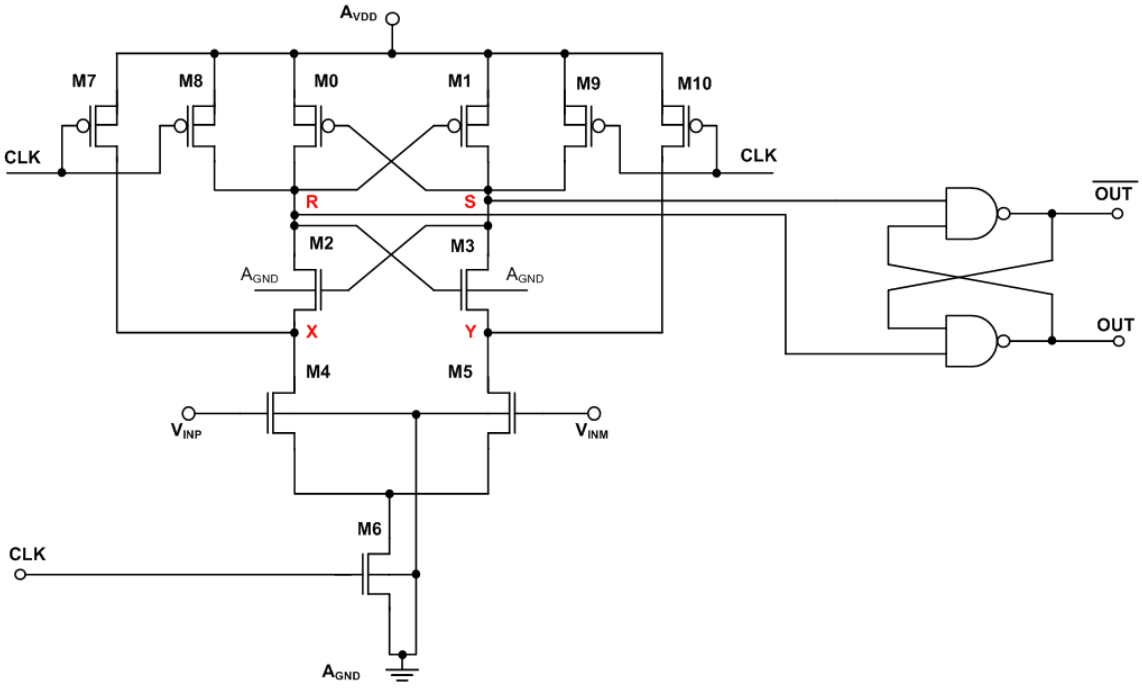


Figure 47: Comparator at transistor level schematic

nodes *R* and *S*. Because the comparator is clocked and also rising edge sensitive, the R-S latch is placed at the output to hold previous state of comparator during the reset mode[17].

The benefits of this architectures are interesting mainly for high-speed usage. The circuit requires only single-phase clock and its static power dissipation is zero. Because the current travers through circuit to the ground only during CLK in logic 1. The input offset of this structure is denominated by input devices rather then cross-coupled devices with respect to other architectures [2]. The only concern is to satisfy sufficient gain of differential pair. It means to size the cross-coupled devices properly to eliminate their offset. Previous implies in the trade-off between size (resistance) of cross-coupled transistors and their offset. The satisfactory size of transistors M0-M3 was optimized in simulation.

The proposed dimensions of transistors and the simulation results along with achieved specifications are shown in Figure 48 and summarized in Table 6.

Table 6: Comparator – transistor's dimensions and achieved specifications

Dimensions		Achieved specs	
Transistor	**W/L[um/um]**	**Parameter**	**Value**
M0,M1,M2,M3	6/0.18	Slew Rate	75 V/us
M4,M5	3/0.36	Delay (at 10kHz)	500 ns
M6,M7,M8,M9,M10	4/0.18	Hysterezis (at 10kHz)	500 uV
-	-	Power dissipation	300 uW

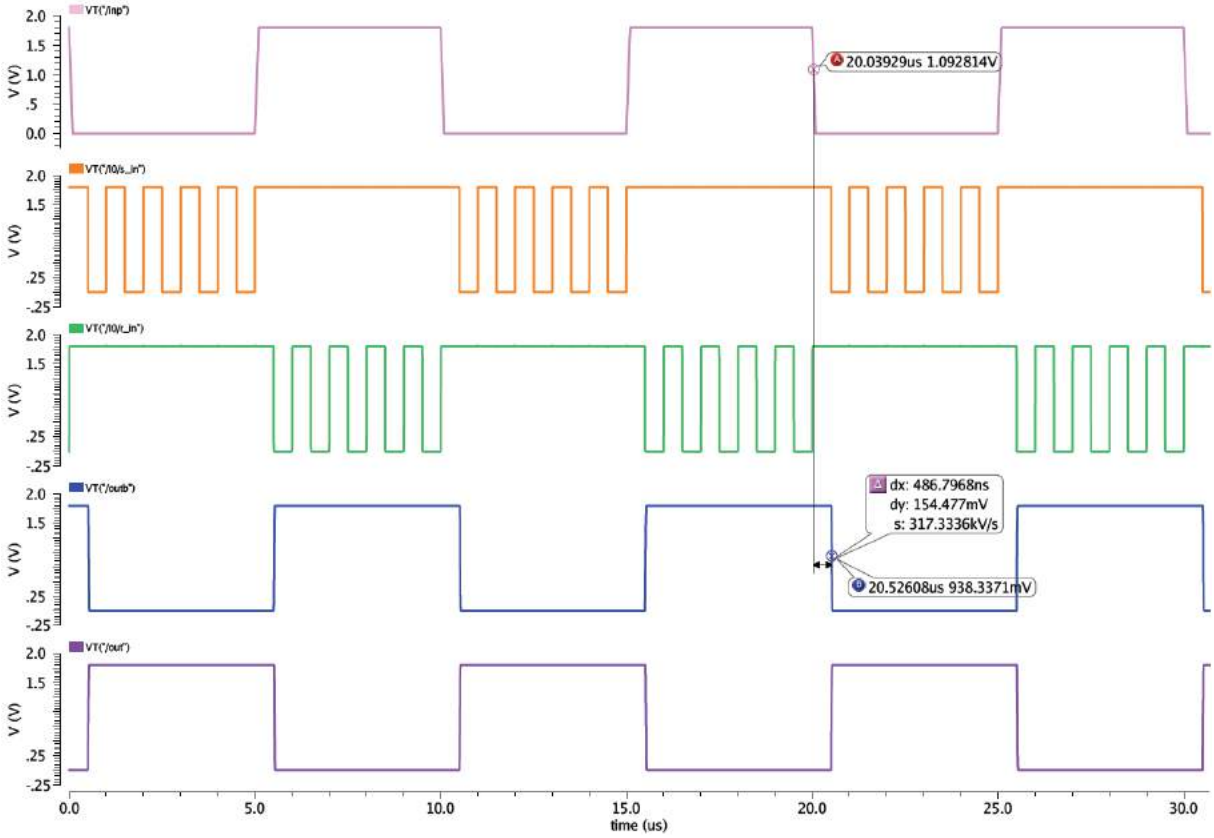


Figure 48: Clocked comparator outputs

Proposed comparator architecture has delay equal to half of the period of clocked signal (500ns for this simulation). With increase clock signal frequency, the delay decreases proportionally.

4.2 Operational amplifier

Operational amplifier (Op-Amp) takes a main place in pipeline ADC design, because of its effect on ADC conversion. It restricts speed, accuracy and consumes a significant fraction of total power. The realistic parameters to achieve were stated in chapter 3.2.4. From this part implies that the Op-Amp gain has to be higher than 60dB and gain mismatch lower than 0.1%. These requirements were taken in account during the design process and next part explains how they were achieved step by step.

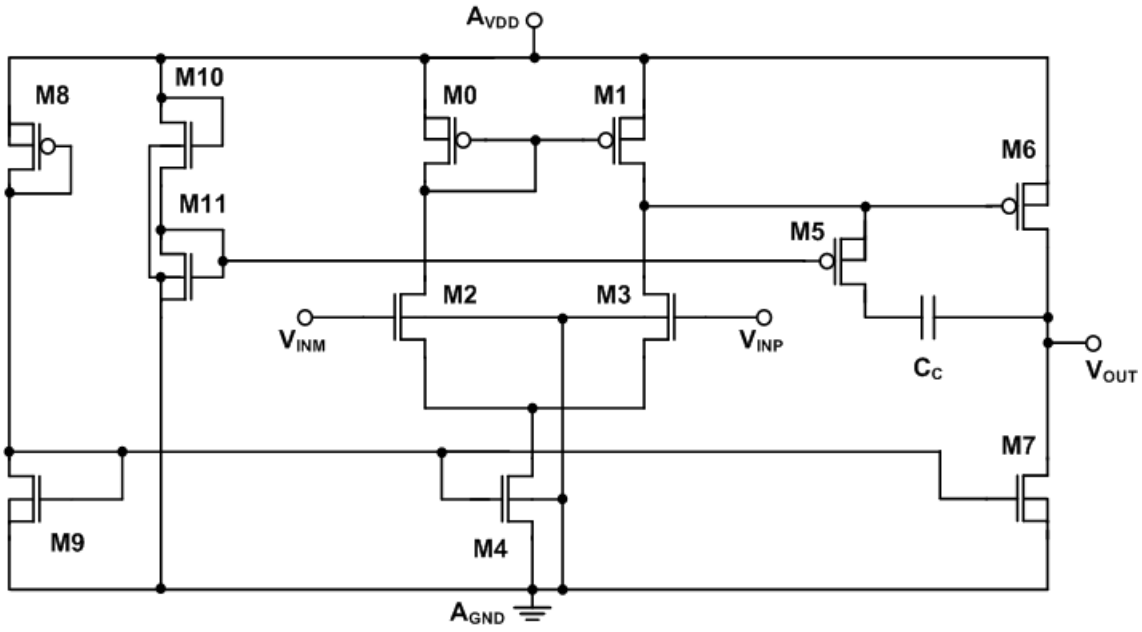


Figure 49: Op-Amp schematic

The inner circuitry of Op-Amp is shown in Figure 49. The schematic represents a two-stage operational amplifier. The first stage formed by transistors M0 – M4 is a differential amplifier with active load (M0, M1) and the second stage is a source follower represented by transistors M6 and M7. The C_C capacitor is a compensation capacitor that facilitates stability in frequency domain and is connected in series with transistor M5. It serves as a compensation resistor.

The first step in Op-Amp design is to determine compensation capacity C_C. It is based on required phase margin (PM) and was stated to 60 º. From literature [18,19] implies, that the compensation capacity is roughly

$$C_C \geq 0.22 \cdot C_L \,. \tag{19}$$

The minimal current that needs to be supplied into differential pair to fulfil slew rate (SR) requirements is determined from equation

$$I_4 = SR \cdot C_C \,. \tag{20}$$

This current is provided by current mirror formed by M9 and M4 transistors. Their size is determined from equation for MOS transistor in saturation,

$$I_D = \frac{K_P}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \,. \tag{21}$$

If we recalculate width W to the left side of formula and substitute all variables, we get

$$W_{M9,4} = \frac{2 \cdot I_4 \cdot L_{9,4}}{K_{pn} \cdot (V_{GS} - V_{TH})^2}, \tag{22}$$

where V_{GS}-V_{TH} was chosen 0.182 V, to remain transistors in saturation.

From calculated capacity C_C and stated GBW we can find out the minimal transconductance of differential pair that has to be satisfied

$$g_{m\,first\_stage} = 2 \cdot \pi \cdot GBW \cdot C_C \,. \tag{23}$$

Thanks to previous step the size of differential pair is given by empiric equation

$$g_m = \sqrt{2 \cdot K_P \cdot \frac{W}{L} \cdot Id} \;\; \rightarrow \; W_{2,3} = \frac{(gm\,first\;stage)^2 \cdot L_{0,1}}{2 \cdot K_{pn} \cdot I_1}, \tag{24}$$

where I_1 is a half of the I_4.

The dimensions of M0,M1 can be then calculated from

$$W_{M0,1} = \frac{2 \cdot I_1 \cdot L_{0,1}}{K_{pn} \cdot (V_{GS} - V_{TH})^2} \,. \tag{25}$$

Now follows a calculation of second stage amplifier. From literature [18], where detailed calculations can be found, implies following. If the PM should be 60º, then transconductance of transistor M6, that forms the second stage, is given by

$$g_{m\,second\_stage} \approx 3 \cdot \; g_{m\,first\_stage} \cdot \frac{C_L}{C_C} \cdot , \tag{26}$$

and current that flows in the second stage is equal to

$$I_{6,7} = \frac{g_{m\,second\,stage} \cdot (V_{GS} - V_{TH})}{2} \,. \tag{27}$$

The appropriate current has to be supplied to second stage amplifier. The $I_{6,7}$ is already known, so for width of M7 transistor applies

$$W_7 = W_9 \cdot \frac{I_{6,7}}{I_4}, \tag{28}$$

when the length of M7 remains the same to achieve willed gain ratio.

The size of voltage follower M6 is stated from equation (23)

$$W_6 = \frac{2 \cdot I_{6,7} \cdot L_6}{K_p \cdot (V_{GS} - V_{TH})^2}, \tag{29}$$

Since the currents and dimensions of first and second stage are known, we can calculate the transistor M5 that serves as a nulling resistor.

From simulation is known, that the nulling resistor should have a resistance approximately 5 kΩ. That corresponds to g_m around 200 μS. Instead of using discrete resistor (which takes a large area on the chip) the transistor that operates in triode region was used. Its resistance follows the equation

$$R_c = \frac{1}{\frac{Kp}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})}, \tag{30}$$

If we assume that the transconductance is inversely proportional to resistance, we can substitute g_{m5} into following equation and determine size of M5

$$W_5 = \frac{(g_{m5})^2 \cdot L_{0,1}}{2 \cdot K_{PN} \cdot I_5}, \tag{31}$$

On gate terminal of transistor M5 has to be constant voltage above threshold. Transistor M11 is used for this purpose. The V_{GS} of M11 is approximately 0.45V, hence, the condition mentioned above is satisfied.

Transistor M12 connected as a diode sets the current to M11. Its resistance can be simplified as

$$R_{10} = \frac{A_{VDD} - V_{TH}}{I_{M10}}. \tag{32}$$

Transconductance is inversely proportional to resistance, so g_{m10} is

$$g_{m10} = \frac{1}{R_{10}}, \tag{33}$$

And dimensions of M11 can be calculated again from basic equation (23)

$$W_{11} = \frac{(g_{m12})^2 \cdot L_{M11}}{2 \cdot K_{PN} \cdot I_{11}}. \tag{34}$$

Transistor M8 facilitates the same function as M10 and its size is calculated according to equations (33,34 and 35).

For two-stage operational amplifier gain applies

$$A_u = A_1 \cdot A_2 = \\ = g_{m\ first\_stage} \cdot (rd1||rd3) \cdot g_{m\ second\_stage} \cdot (rd6||rd7) \cdot \tag{35}$$

And the total power consumption is a sum of all currents flowing from A_{VDD} to A_{GND} multiplied by A_{VDD}.

$$P_{TOT} = (I_4 + I_7 + I_9 + I_{11}) \cdot A_{VDD} \tag{36}$$

Calculation of all transistors was described. The Op-Amp specifications along with calculated and optimized dimensions of transistors are visualized in Table 7 and Table 8.

Table 7: Op-Amp specifications

Op-Amp specs	**Determined specs**
Parameter	**Value [units]**
Au	> 60 dB
SR	≥ 20 V/us
GBW	> 30 MHz
PM	> 60°
V_{OFFSET}	< 5 mV
P_{TOTAL}	< 5 mW
C_L	10pF
A_{VDD}	1.8V

Table 8: Op-Amp calculated and optimized transistors dimensions

Component	**Calculated dimensions [µm/µm]**	**Optimized dimensions [µm/µm]**
M0,M1	20/0.54	16.3/0.54
M2,M3	5/0.54	4/0.54
M4,M9	7/0.54	6/0.36
M5	10/0.36	20/0.36
M6	254/0.36	254/0.36
M7	51/0.36	60/0.36
M8	3/0.36	1/0.36
M10	1/8	0.22/8
M11	5/0.36	6/0.36
C_C	2.2 pF	2.1pF

A number of simulations were run to verify Op-Amp functionality. The fundamental parameters such as gain A_U and phase margin PM (Figure Att. 1), hysteresis V_{HYST} (Figure Att. 2), slew rate SR (Figure Att. 3,Figure Att. 4), input voltage range (Figure Att. 5) and output common mode range (Figure Att. 6) were simulated. Additional simulations such as corner analysis (Figure Att. 7, Figure Att. 8), matching analysis (Figure Att. 9) along with transistor's saturation check (Figure Att. 10) are situated also at the end of the document.

Table 9 : Op-Amp's achieved specifications

Op-Amp specs	**Achieved specs**
Parameter	**Value [units]**
Au	73 dB
SR	20 V/us
GBW	50 MHz
PM	83.5 ^{o}
$\mathbf{V_{OFFSET\ (random)}}$	62 uV
$\mathbf{V_{OFFSET\ (systematic)}}$	3.275mV
$\mathbf{V_{HYST}}$	42 mV
$\mathbf{P_{TOTAL}}$	1 mW
Input voltage range	(0.1 – 1.714) V
Output CM range	(100n – 1.792) V

Operational amplifier design was successfully done and minimal requirements were achieved. The proposed MDAC's operates with sample frequency 1 MHz with input signal frequency up to 500 kHz. From the table above is evident that the operational amplifier fulfilled stated requirements from chapter 3.2.4 and can be used in top level design.

4.3 Non-overlap generator

Correctly aligned and synchronized clock signals are essential for switched-capacitor circuits. Complementary switches are controlled by two signals Φ_1 and Φ_2 along with their inverted variants. They have to have opposite phase and must not overlap to guarantee charge preservation. For this purpose, a non-overlap generator is used in design. Its simplified schematic and idea of operation is shown in Figure 50.

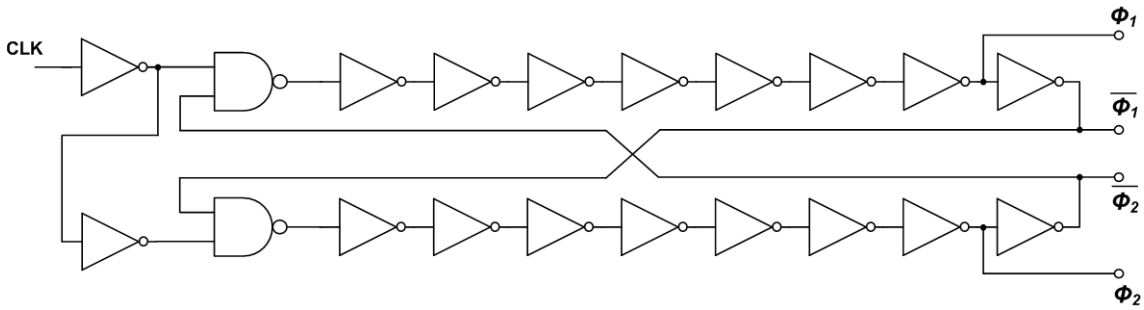


Figure 50: Non-overlap generator schematic view

Generator's inner structure is basically a series connection of inverters and NAND gates where the individual element delay is exploited to provide desired functionality. The time delay depends on number of inverters that were used. The external 1 MHz clock source is connected to the input of the generator.

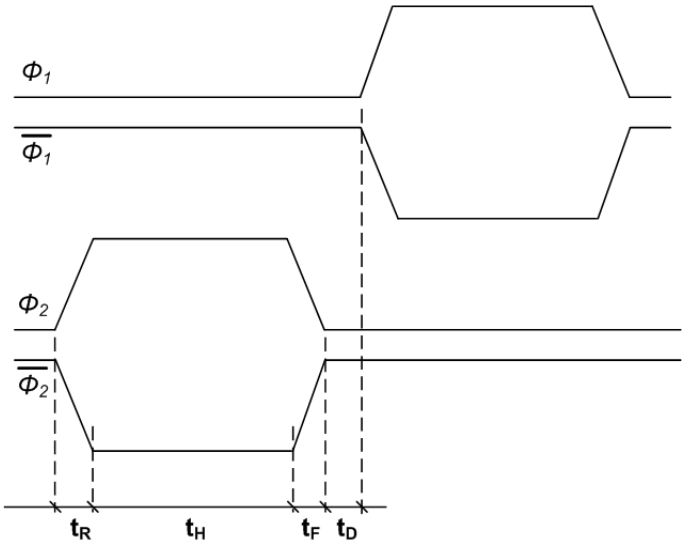


Figure 51: Idea of generated clock pulses

The parameters in Figure 51 indicate duration of rising edge (t_R), falling edge (t_F), hold time (t_H) and delay between Φ_1 and Φ_2 (t_D). The simulation results of generator are shown in Figure 52.

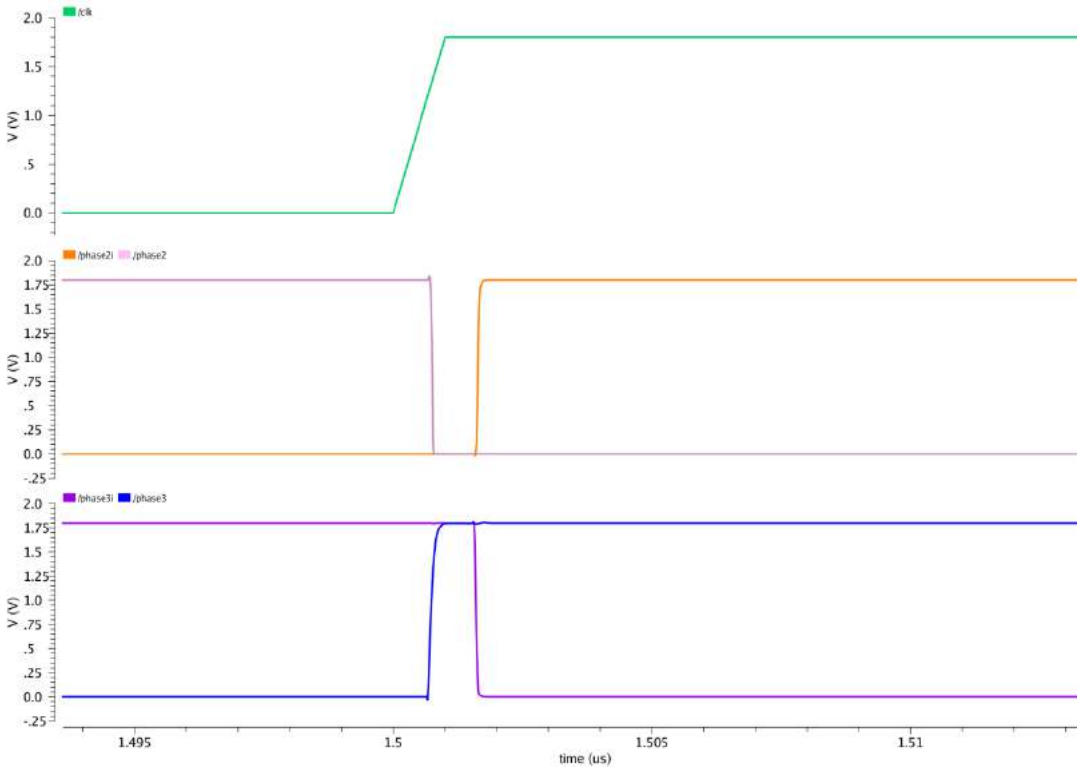


Figure 52: Non-overlap generator outputs

Phase 1 and phase 2 in Figure 52 are designated as Φ_1 and Φ_2, respectively. The input signal from external generator is on very top. The non-overlap signals for NMOS devices switching are shown underneath. Their negative variants serve for switching PMOS devices.

A 5pF capacitor was connected to the output of the non-overlap generator for parasitic capacities of MOS switches emulation. The parameters such as rising edge t_R = 0.5ns, falling edge t_F =0.1ns, and active level duration t_H = 499ns were extracted from simulation.

4.4 The 2-bit Flash ADC

The last segment of pipeline ADC conversion chain is the Flash converter. As it was mentioned in chapter 3.1.2 the 2-bit variant was chosen due to the fact, that there is no need to produce any residual signal. For two bit Flash ADC converter, 2^{N-1} comparators have to be used. The conceptual schematic is the same as in chapter 3.1.2. Moreover, the comparator was already introduced in chapter 4.2, so the full schematic will not be shown in this chapter again. On the other hand, the encoder logic structure has not been revealed yet, therefore, it is shown Figure 53.

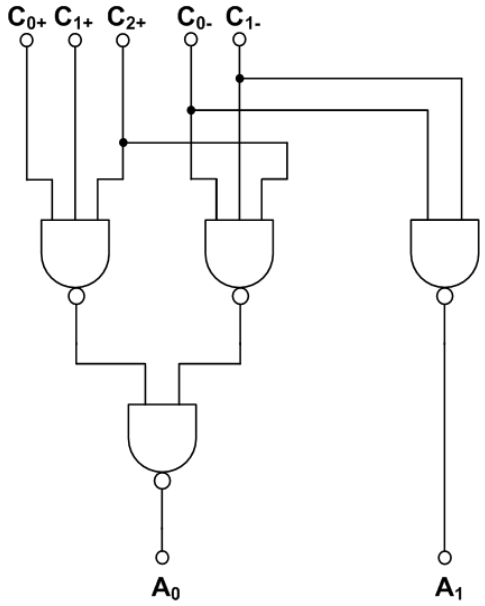


Figure 53: 2-bit Flash encoder schematic

Letters with index – for example, C_{0+} or C_{1-} – represent comparators outputs (C_{0+} → comparator 0, positive output ; C_{1-} → comparator 1, negative output etc.) and A_0 and A_1 are the digital outputs. Logical function of the output A_0 and A_1 is described in term of Boolean algebra below

$$A_0 = C_0C_1C_2 + \overline{C_0C_1}C_2 = \overline{\overline{C_0C_1C_2} \cdot \overline{\overline{C_0C_1}C_2}}\ , \tag{37}$$

$$A_1 = \overline{C_0C_1}\ . \tag{38}$$

The output waveforms are shown in Figure 54 and they correspond to the outputs extracted from Matlab model in Figure 36 b).

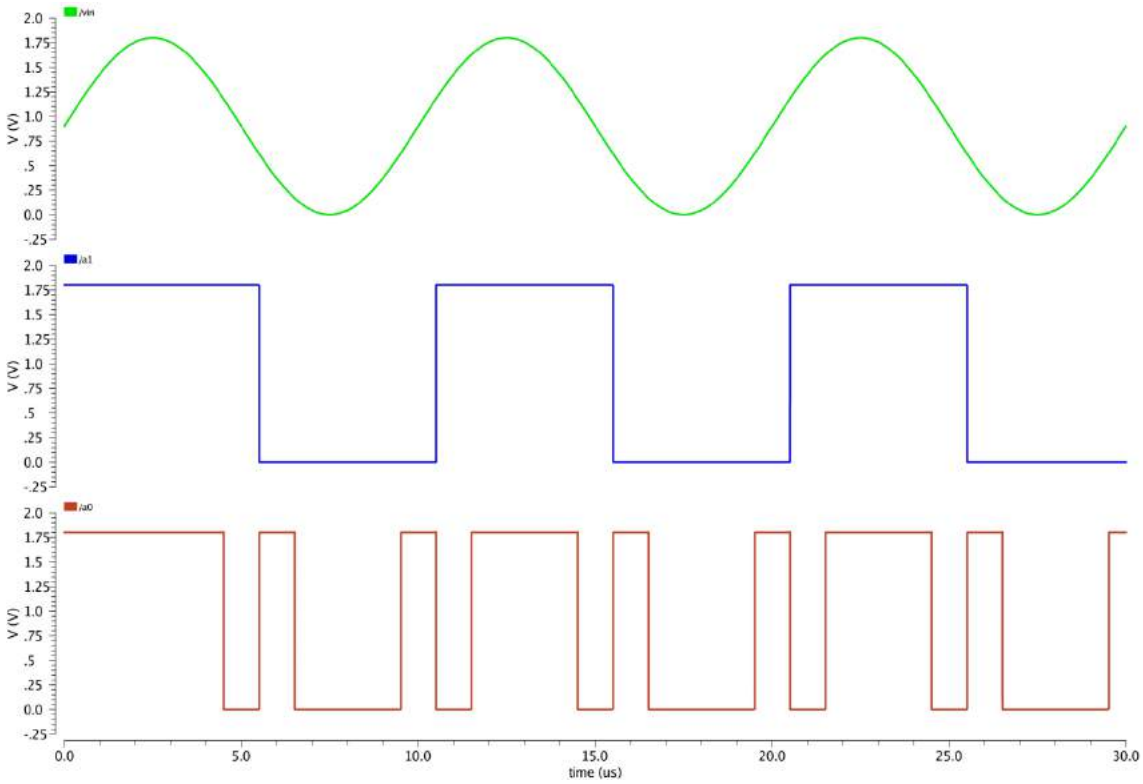


Figure 54: 2-bit Flash ADC outputs

4.5 The 2.5-bit MDAC

The following chapter is based on proposed design architecture from part 3.1. The principle of function will not be recapitulated, but the design process will be explained instead. The block schematic of designed MDAC is identical with the block diagram in Figure 24. The full design schematic is due to its size situated in Attachment 2 at the end of the document.

The 2.5-bit MDAC's – more precisely subADC's – consists of 6 comparators that compare the input signal with reference voltages ±5/8 V_{REF}, ±3/8 V_{REF} and ±1/8 V_{REF}. These reference voltages come from voltage divider similar to the one in Figure 24. The value of $\pm V_{REF}$ is derived from maximal and minimal amplitude of input signal. The input signal peak-to-peak value was stated to A_{IN} = 900mV with respect to common mode voltage which is V_{CM} = 900mV. That gives the voltage swing from V_{REF_P} =1.35V to V_{REF_N} = 0.45V.

These levels were selected due to two aspects. First, the operation amplifier architecture was designed with single supply, which leads to use voltage range above analog ground. Second, this approach simplifies the overall design, because it is not necessary to produce another voltage levels.

The digital signal is present at the output of the comparators. It is decoded by MDAC digital logic (Figure 55) and sent as a particular output to time correction block. The same signal is in parallel applied to sub-DAC's address inputs (V_{IN_0} – V_{IN_2}). There are three sub-ADCs in design and they are basically multiplexers. Their transistor schematic, along with transistors dimensions, is shown in Figure 56 and full conceptual schematic is visualized in Figure 24 .

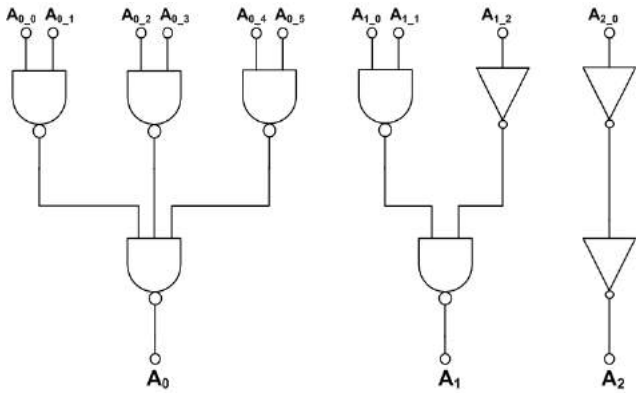
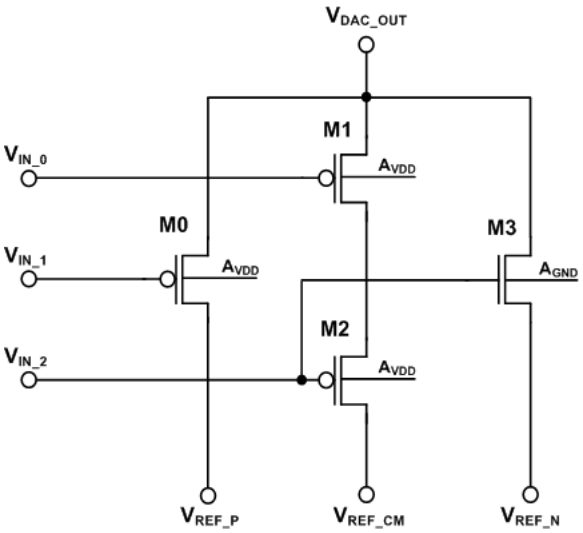


Figure 55: MDAC digital output logic



Dimensions	
Transistor	**W/L [um/um]**
M0	60/0.18
M1	60/0.18
M2	60/0.18
M3	120/0.18

Figure 56: 1.5-bit sub-DAC – multiplexer.

The reference voltage (Figure 56) V_{REF_P}, V_{REF_N} and V_{REF_CM} are applied to output V_{DAC_OUT} according to multiplexer input voltage. The output of each multiplexer is a one-third (1/3) of overall signal amplitude which is subtracted from input signal V_{RESX} in next step.

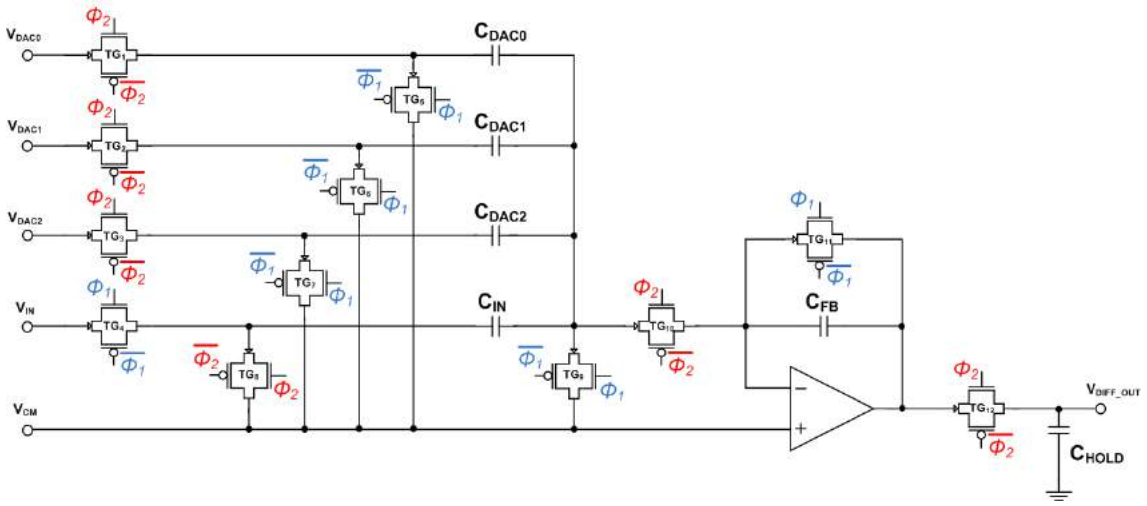


Figure 57: Subtraction circuit

Circuit in Figure 57 realizes subtraction of three already converted signals $V_{DAC0} - V_{DAC2}$ from the input signal. The mathematical representation of this operation, according to Table 3, is following.

$$V_{RESx} = V_{RESx-1} - \frac{V_{DAC\_OUT0} + V_{DAC\_OUT1} + V_{DAC\_OUT2}}{3} \qquad (39)$$

This circuit is basically a differential amplifier realized in SC technique. Switches designated as TG_1 – TG_{12} are complementary MOS transistors also known as Transmission Gates (T-Gates). Their structure and schematic will be shown and discussed later. Subtraction circuit operates in two phases.

The transmission gates TG_4 TG_5 TG_6 TG_7 TG_9 and TG_{11} are on in phase 1 (Φ_1). The input signal from terminal V_{IN} charges the capacitor C_{IN} with respect to common mode voltage V_{CM} and this voltage is applied to the positive terminal of Op-Amp. Capacitor C_{FB} is shorted in the same time and the voltage at Op-Amp's negative input terminal corresponds to voltage at positive input terminal.

In phase 2 (Φ_2) TG_1, TG_2, TG_3, TG_8, TG_{10} and TG_{12} are on, meanwhile, the previous active switches are off. The signal from particular sub-DAC is connected to individual capacitors (C_{DAC0}, C_{DAC1}, and C_{DAC2}) and they are charged proportionally to connected voltage. The voltage proceeds to negative terminal of Op-Amp and is subtracted from voltage that was stored on capacitor C_{FB} during the phase 1 (Φ_1). The residual signal is preserved on C_{HOLD} capacitor and the whole process repeats.

Because the subtraction circuit has to perform specific operation (see Table 3), the individual capacitors value was estimated in conformity with following formula

$$V_{DIFF} = \frac{C_{IN}}{C_{FB}} \cdot V_{IN} - \left(\frac{C_{DAC0}}{C_{FB}} \cdot V_{DAC0} - \frac{C_{DAC1}}{C_{FB}} \cdot V_{DAC1} - \frac{C_{DAC2}}{C_{FB}} \cdot V_{DAC2} \right). \qquad (40)$$

— C_{IN} = 4pF

— C_{DAC0} = C_{DAC1} = C_{DAC2} = C_{FB} = 1pF.

Use of complementary switches, as they were mentioned earlier, is common approach for SC technique. Structure in Figure 58 provides transfer of input signal to the output when Φ_2 is in logic 1 and Φ_1 in logic 0. Because MOS transistor charge injection and clock feed-through effect significantly affects performance of SC circuits (see literature [20]), the basic concept of transmission gate was amended with two shorted transistors connected besides the main transistor (M2 and M5). These „dummy" switches serve for discharging parasitic capacities to improve switch recovery time. This approach allows minimize problems connected with charge injection and improves T-Gate functionality.

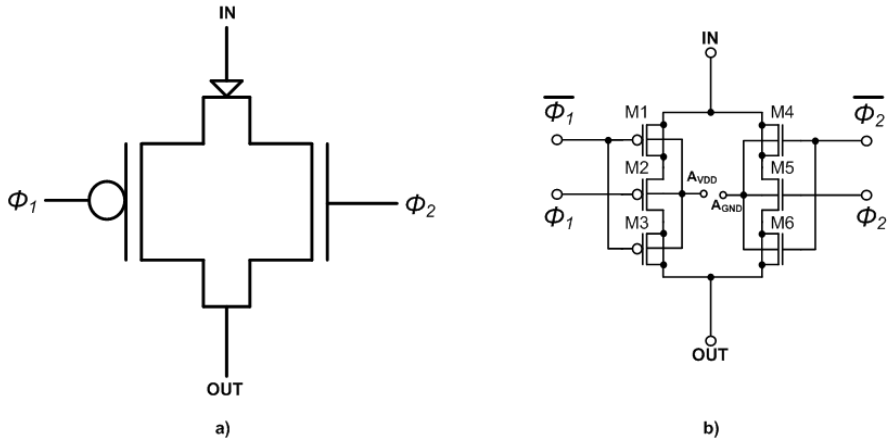


Figure 58: a) Transmission Gate symbol, b) corresponding transistor level schematic

The results in Figure 59 correspond to simulation results from Matlab in Figure 35 and in Figure 36a. Because all results match theoretical expectations, the MDAC functionality is considered to be proven.

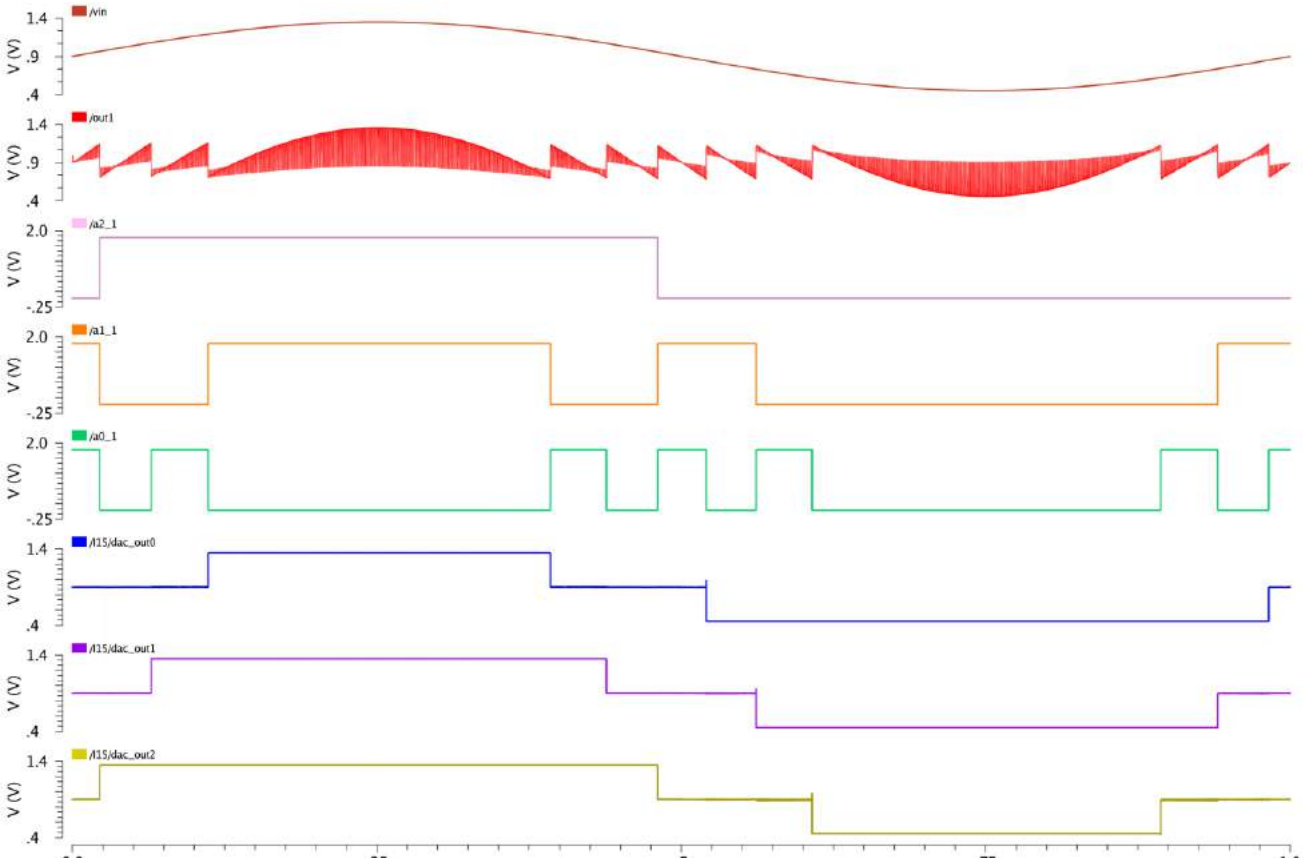


Figure 59: The 2.5-bit MDAC outputs (from top to bottom): a) input signal, b) output residuum, c) digital output A2,d) digital output A1, e) digital output A0, f) – h) sub-DAC outputs 0,1,2

4.6 Time correction

Each MDAC consists of circuits driven by two separate clock phases as was described in chapter 4.3. It initially results in signal delay of individual outputs and also in delay between MDAC stages. The time delay of single MDAC is proportional to a half period of input clock signal. As the signal passes through conversion chain the delays are added together. If the RSD correction has to fulfill its function, the signals have to be synchronized. The time correction block was designed for this purpose.It is realized as a shift register made of D Flip-Flops. The inner circuit diagram of D Flip-Flop is shown in Figure 60 and principle of operation is visualized in Figure 61.

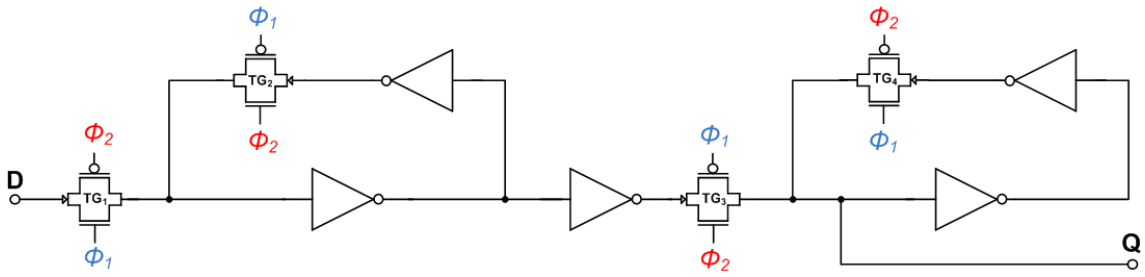


Figure 60: D Flip-Flop made of inverters and transmission gates

The transmission gates were used in D Flip-Flop realization. The function of delay element is as follows. When D is high and TG1 is on (Φ_1), the signal is inverted twice in a row and is stored at the input of TG2. The same inverted signal is at the input of TG3. When D goes low, the stored value is proceeded to the output Q during phase 2 (Φ_2).

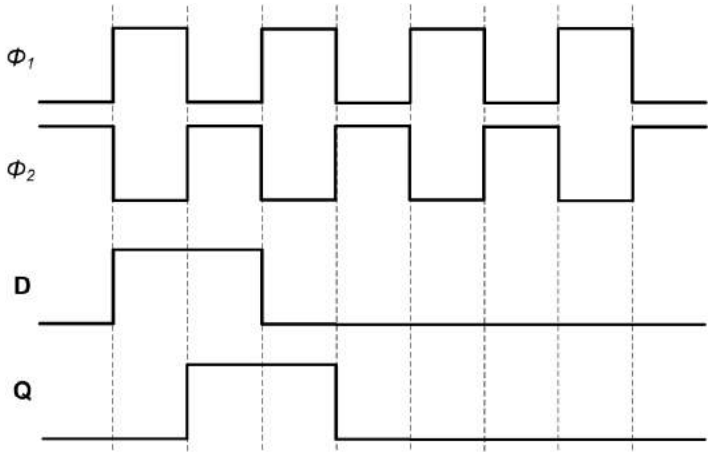


Figure 61: D Flip-Flop as a shift register

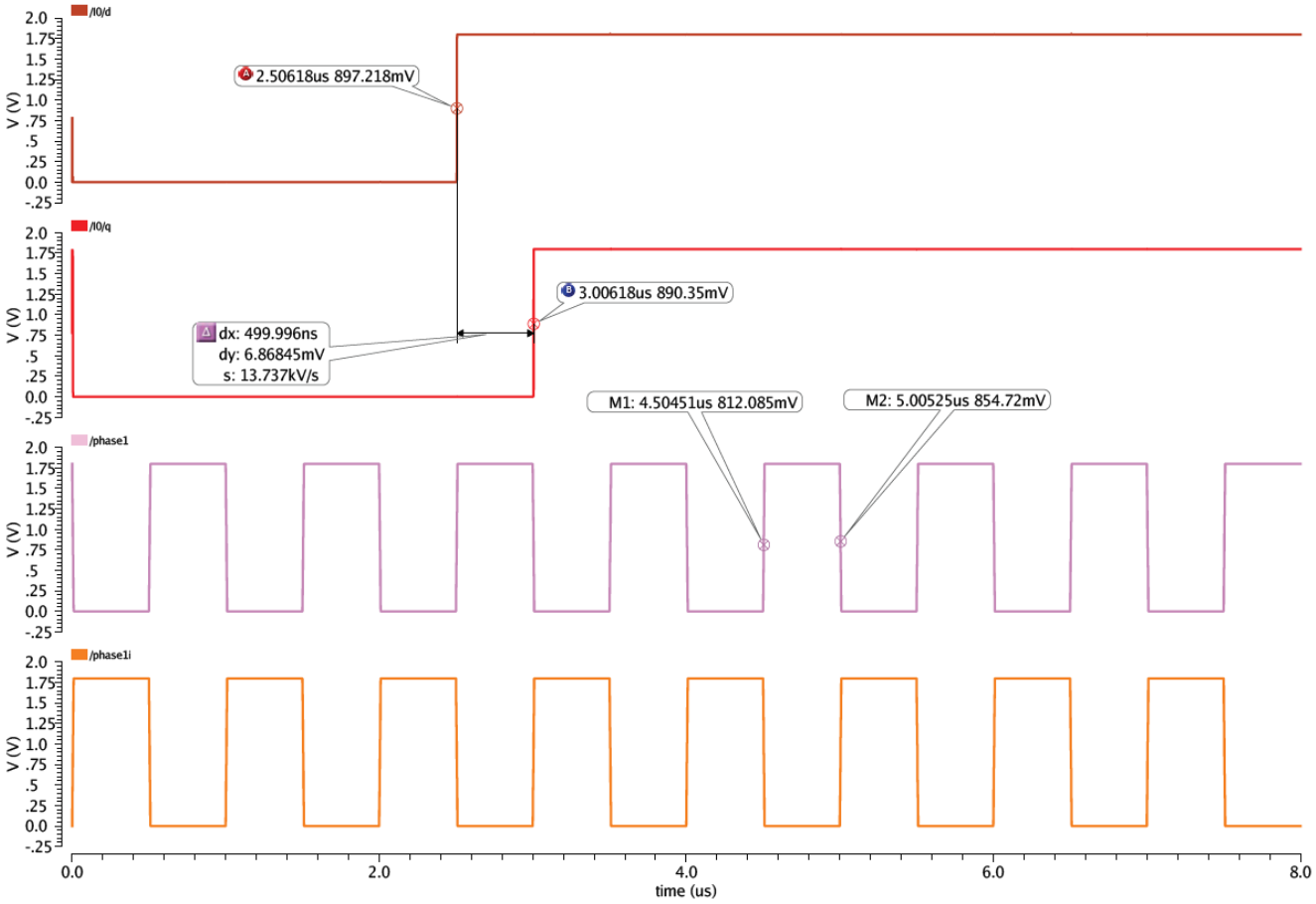


Figure 62: D Flip-Flop function demonstration (from top to bottom):
a) input signal, b) delayed signal, c) clock phase 1, d) clock phase 1 inverted

The results extracted from simulation in Figure 62 correspond to theoretical expectations from Figure 61. The output signal is delayed by half of a period of clock signal, which is 500ns.

4.7 RSD correction

When the signals are synchronized, they can pass to last conversion block – RSD (Redundant Signed Digit) correction circuit. The task of this block is to sum two corresponding signals and correct the possible errors in structure that were described in chapters (2.4 and 3.1.4). Because all circuits in design operate synchronously the delay elements (D Flip-Flops) were added at the output of RSD correction. In phase 1 (Φ_1), the synchronized outputs are applied to RSD correction logic inputs. The logical operation is made and change traverse through individual (RSD_cell0 – RSD_cell4) elements. The already corrected signal is passed through D Flop-Flops to the output in phase 2 (Φ_2). This delaying process helps to improve overall circuit performance. It helps avoiding voltage glitches and meta-stability states traverse to the output during phase 1, meanwhile, the logical operation is processed.

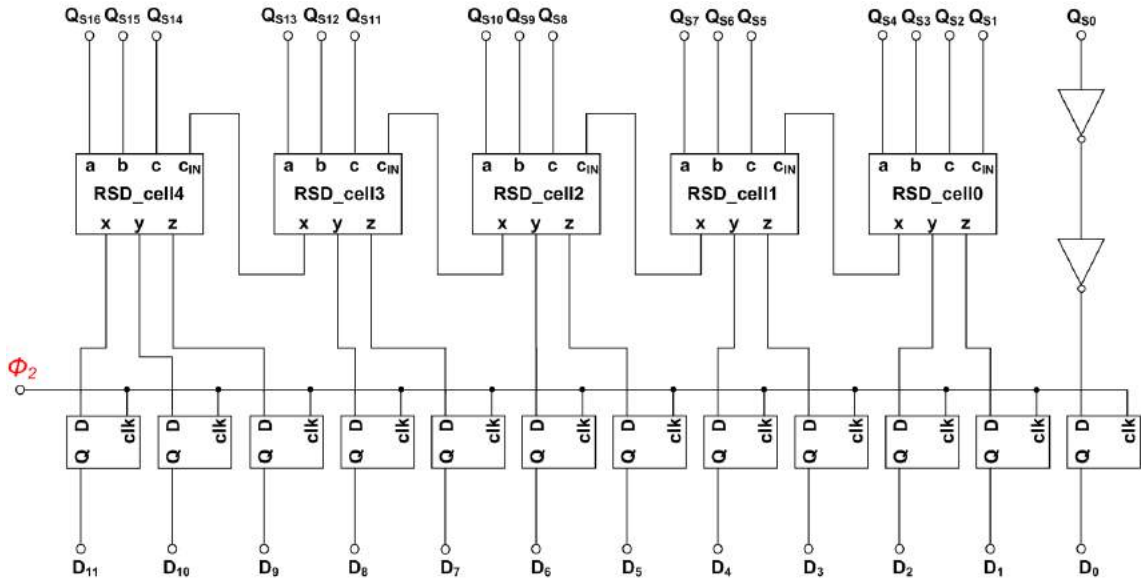


Figure 63: RSD correction block schematic

In terms of Boolean algebra, the logical operation of single RSD cell can be explained as

$$X = \overline{\overline{(A \cdot \overline{B})} \cdot \overline{(A \cdot \overline{C})} \cdot \overline{(A \cdot \overline{D})} \cdot \overline{(\overline{A} \cdot B \cdot C \cdot D)}}, \tag{41}$$

$$Y = \overline{\overline{(B \cdot \overline{C})} \cdot \overline{(B \cdot \overline{D})} \cdot \overline{(\overline{B} \cdot C \cdot D)}}\,, \tag{42}$$

$$Z = \overline{\overline{(C \cdot \overline{D})} \cdot \overline{(\overline{C} \cdot D)}}\,. \tag{43}$$

The gate level implementation of RSD cell is shown in Figure 64.

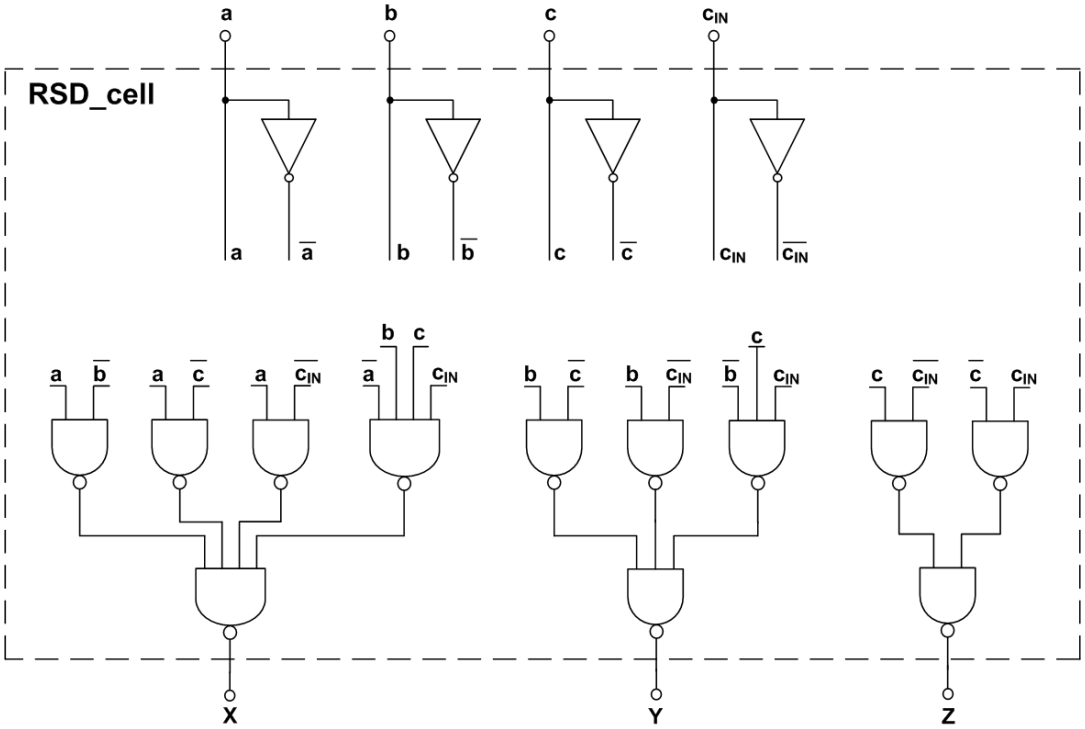


Figure 64: Implementation of RSD cell using NAND gates

The results of digital correction block operation with comparison with Matlab model are shown in Figure 65. The sequence representing output without offset error is (MSB => LSB) 111001010011_b, and sequence with corrected offset error is 111001010101_b.

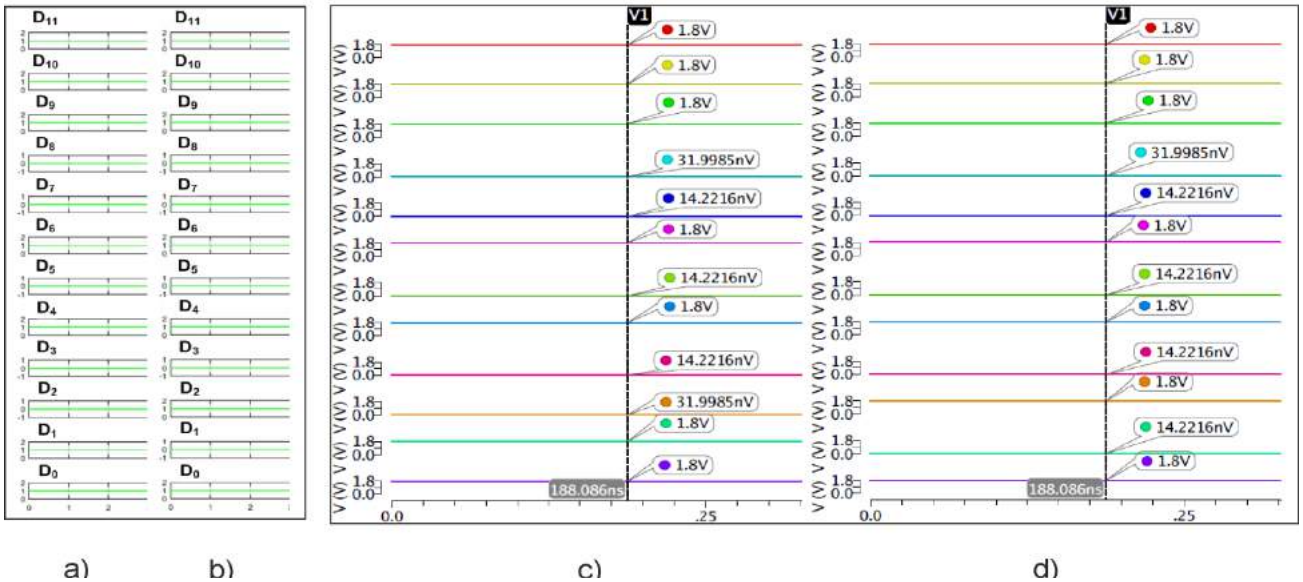


Figure 65: RSD outputs: a) without offset error – Matlab, b) with offset error – Matlab, c) without offset error – Cadence, d) with offset error – Cadence,

4.8 Top level design simulation

This chapter summarizes overall ADC performance. The top level functionality is reviewed and static parameters such as INL and DNL are reviewed in Figure 66. The next Figure 67 also reveals reconstructed output signal using ideal 12-bit DAC. The output of ADC is shown in Figure 68 in its transient form and the residual signals are visualized in Figure 69. All conversion results were reached under following conditions:

- Sample frequency: $F_{SAMPLE} = 1$ MHz
- Input signal frequency: $F_{IN} = 1$ kHz
- Input signal amplitude: $A_{IN} = 0.45$ V (0.9V Pk–to–Pk)
- Supply voltage: $A_{VDD} = 1.8$ V
  $A_{GND} = 0$ V
- Reference voltages: $V_{REF\_P} = 1.35$ V
  $V_{REF_CM} = 0.9$V
  $V_{REF\_N} = 0.45$ V
- LSB value: $LSB = 220$ µV

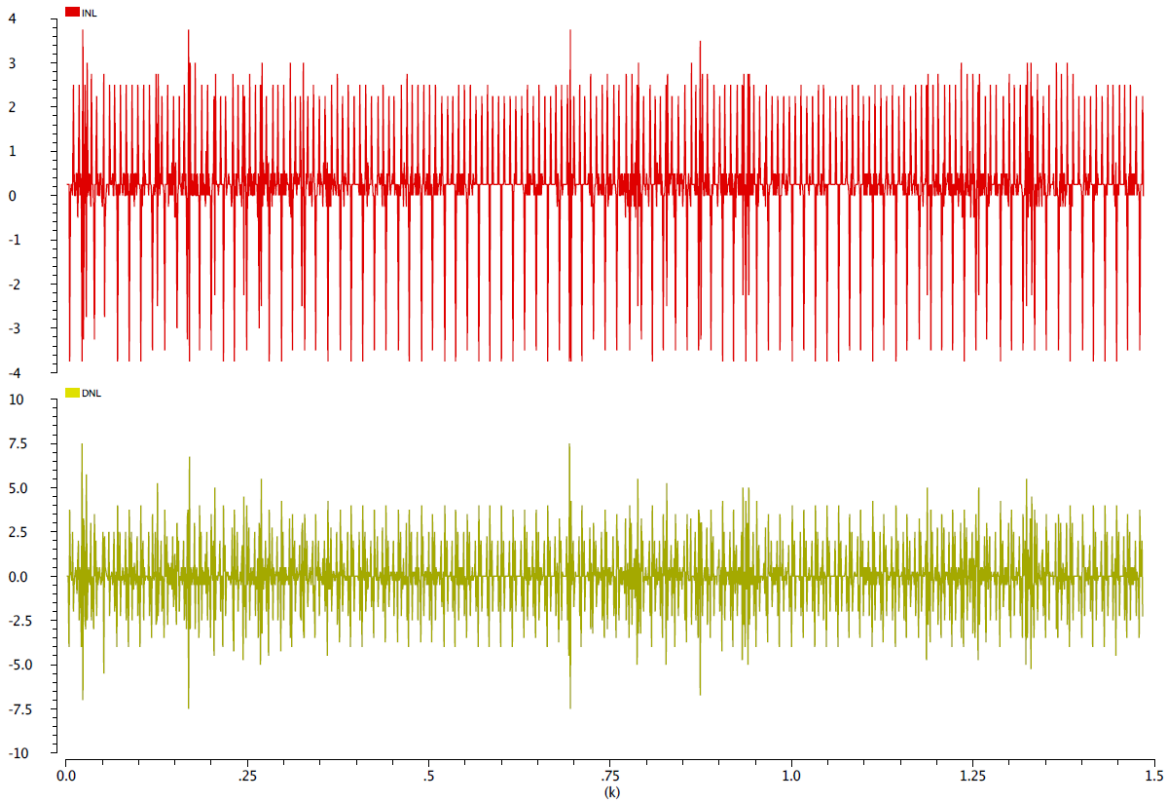


Figure 66 : Extracted INL (top) and DNL (bottom)

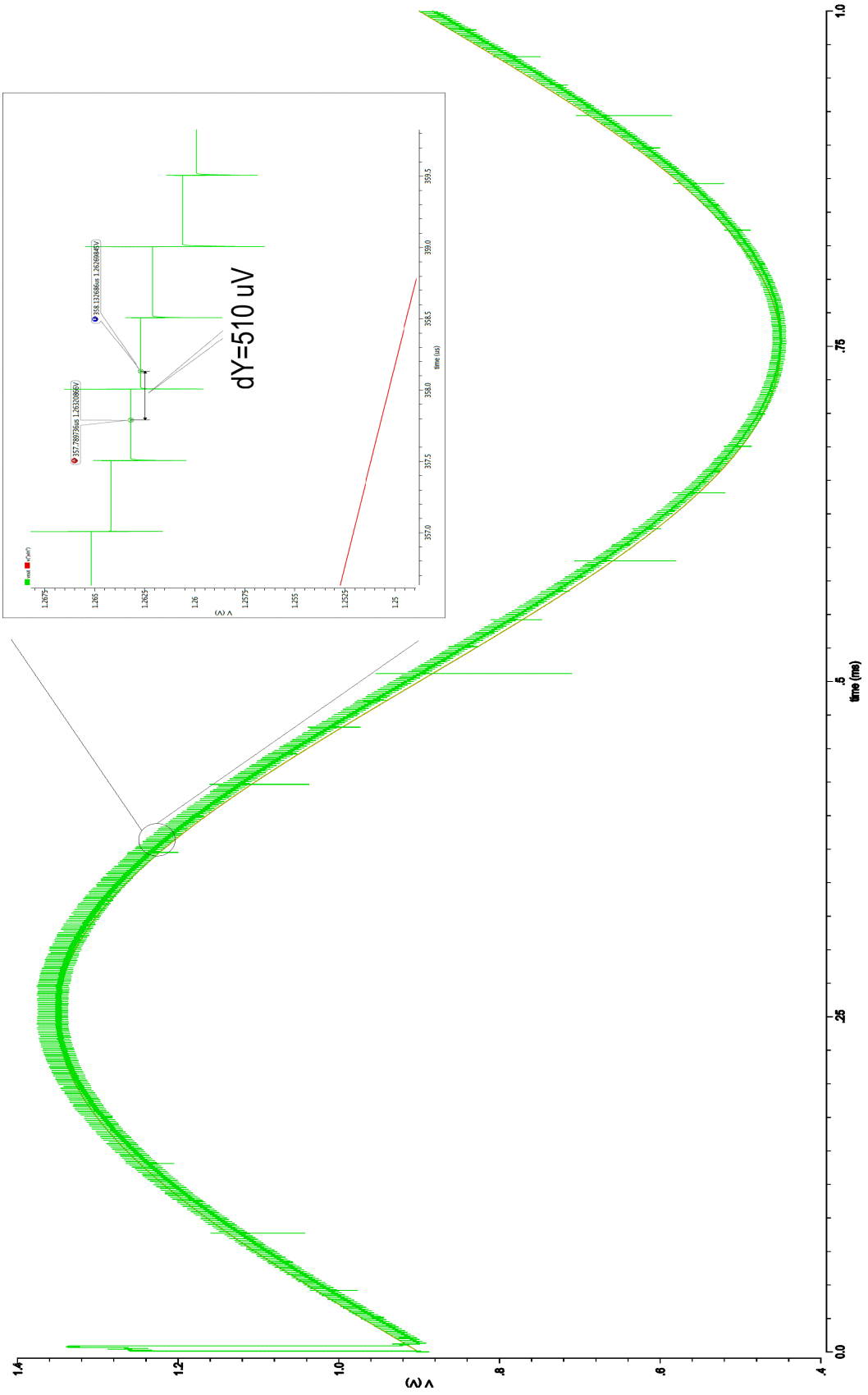


Figure 67: Reconstructed ADC output signal

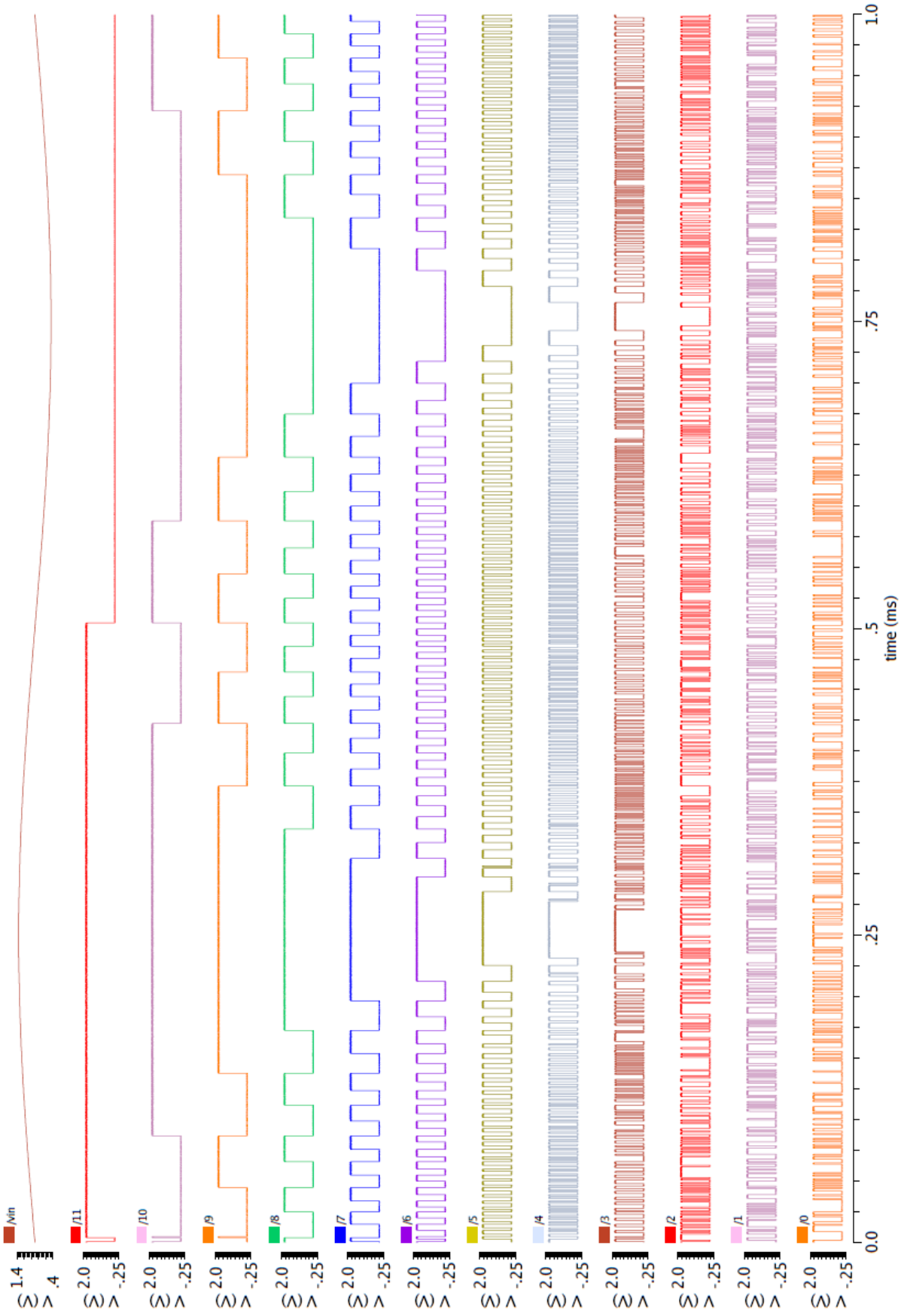


Figure 68: Digital output waveforms of 12-bit Pipeline ADC, MSB (top), LSB (bottom)

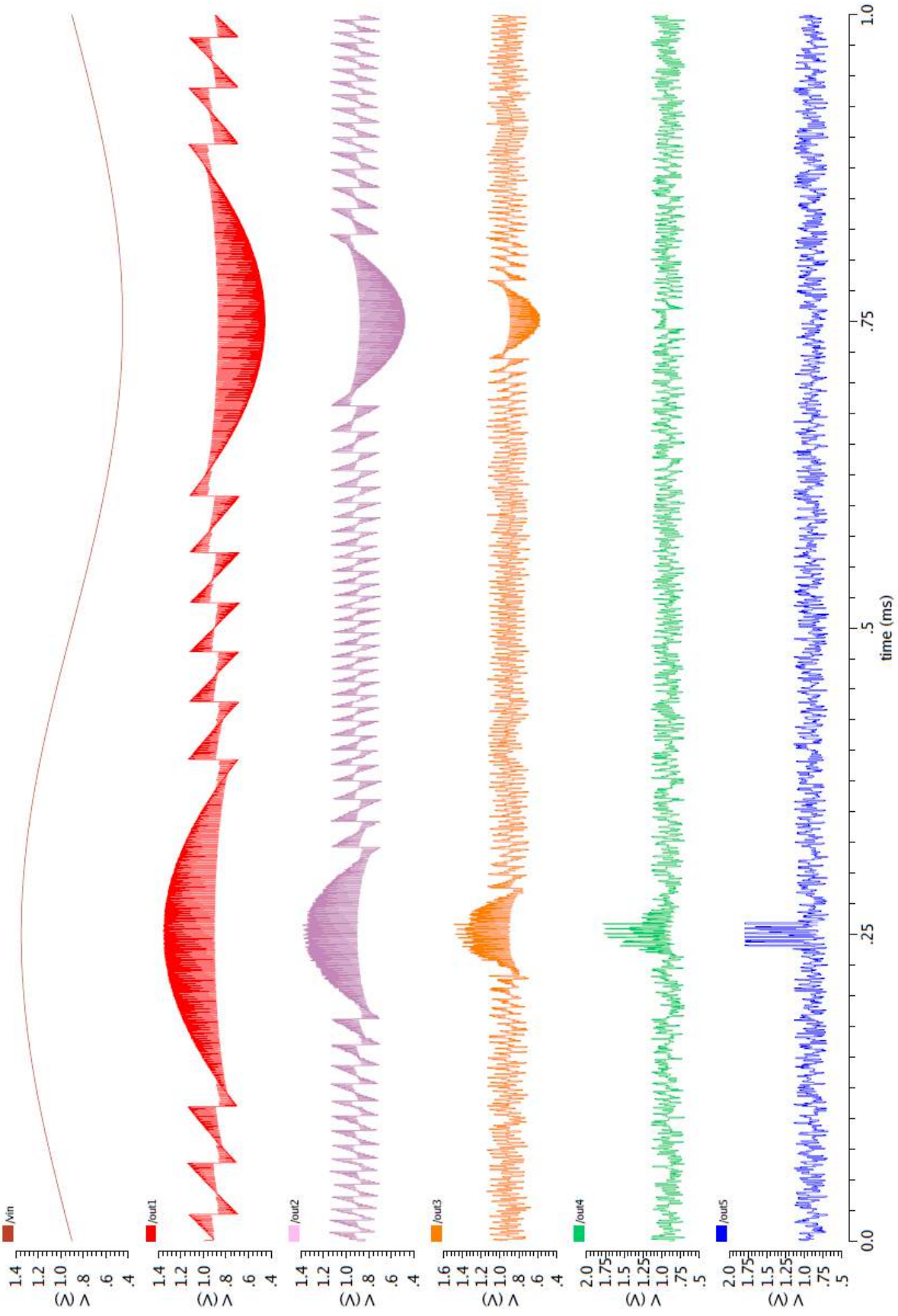


Figure 69: Residual signal between individual stages Stage1 (top) –Stage 5 (bottom)

Table 10: The 12-bit pipeline ADC achieved specifications

Parameter	Value [units]
Resolution	12 bits
Sample Rate	1 MHz
Supply Voltage	1.8 V
P_{TOTAL}	18 mV
INL	± 4 LSB
DNL	± 7 LSB

The results of top-level simulation demonstrate the operation of designed AD converter. As is evident from Figure 68 the last three bits have some missing codes. This is caused by numerous influences mainly by a gain mismatch of subtraction circuits. The output residual signals in Figure 69 correspond to the expectations at three first stages. The two last residual signals have significant errors. The residual signal does not reach maximal and minimal reference levels and the shape of signal becomes more chaotic instead of being „saw tooth" waveform. The solution of the problem might be in increasing sampling rate frequency. But on the other hand, it is necessary to point out, that the parasitic resistivity and capacitance of T-Gates depend on sample frequency and on size of the devices. This dependency is hard to determine and even harder to suppress because a number of parameters have to be considered on. With higher frequency and with larger devices, we get higher parasitic capacitance along with higher parasitic resistivity causing a voltage drop on the switches and increase of parasitic capacity, respectively. However, the cancelation (dummy) transistors were used in T-Gate's structure, the parasitic effects were not sufficiently suppressed. Along with mentioned problems, the SC technique is very sensitive to accurate clock timing.

Despite all efforts, these errors were not acceptably suppressed to obtain ideal effective number of bits (ENOB) resolution. Debugging and evaluation process is very time-consuming. Especially if we consider, that one top level simulation run (over one period of the input signal) takes four hours of calculation with 1 MHz sample rate frequency. With higher sample rate the simulation time arises proportionally. This fact made the debugging process even more complicated.

The additional simulation results with sample frequency F_{SAMPLE} = 2.5 MHz are mentioned in the Attachment 4 where the finest resolution corresponds to 1 LSB, but the INL and DNL parameters have worsened hundred times.

5 NON-IDEALITIES COMPENSATION PROPOSAL – FOREGROUND CALIBRATION TECHNIQUE

It is necessary to use one of the calibration techniques to achieve high resolution in pipelined ADC. The foreground calibration technique seems to be most suitable for this application due to its lower demands on system complexity with respect to background calibration techniques. One article dedicated to foreground calibration can be found in [14]. The foreground calibration technique is described in simplifying block diagram in Figure 70.

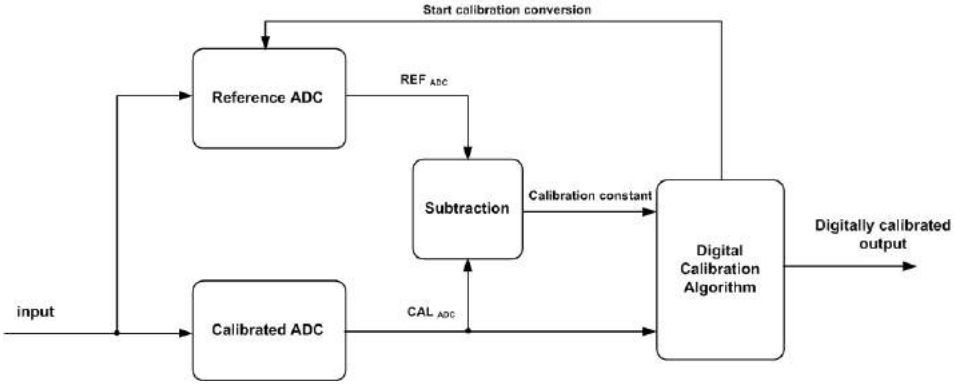


Figure 70: Foreground calibration block model proposal

The input signal is processed with calibrated ADC. The reference ADC does the conversion of the same input signal but not all the time. It produces conversion on command. This command comes from Digital Calibration block that evaluates the results and provides calibration when it is necessary. The reference ADC does not need to be fast as calibrated ADC, but must have the same or higher resolution than the calibrated ADC. When the conversion on command signal asserts, the reference ADC makes a single conversion and proceeds the conversion word to subtraction block. Here is reference digital word subtracted from calibrated word and the calibration constant for a single sample is fed to digital calibration algorithm block. The calibrated signal is processed by this block and the digitally corrected word is prepared at the output [15].

This type of calibration procedure can help to improve ADC performance and increase its accuracy. Due to ubiquitous parasitic factors presence in every design the trend in high-resolution (12-bit and more) pipeline ADC’s is to use some form of calibration to reach desired resolution.

6 CONCLUSION

The semester project was dedicated to the design of 12-bit pipeline ADC in Cadence environment using TSMC 0.18μm technology. To ease the design process and properly understand the function of pipeline ADC, the behavioural model in Matlab environment was created and the consequent specifications were used in the real design process.

Chapter 1 summarized the ADC's conversion static parameters such as SNR, SNDR, ENOB, DNL, and INL. Then the main modern architectures were introduced and explained. Special attention was devoted to their advantages and disadvantages and all architectures were compared together.

The pipeline ADC architecture was described in details in chapter 2. The particular blocks such as MDAC, sub-ADC, sub-DAC, time correction block and RSD correction block were described and their function was explained. Then the presence of non-idealities in conversion system was described and their influence on conversion accuracy was discussed.

The practical part was divided into two parts. The first part (chapter 3) aimed to the creation of Matlab model using the knowledge described in theoretical part. The behavioural model was created and its functionality was proven. The output waveforms, transfer functions, power signal spectrum density and other utilities served as a relevant evidence of functionality. The achievable specifications on real technology were estimated from the model and used in the design process of the real converter on transistor level using Cadence environment in chapter 4.

The pipeline structure was successfully created and its functionality was proven with various simulations. The individual test-benches were made for every sub-block to verify its functionality. The comparator was designed first and reached parameters are stated in Table 6. Then the operational amplifier was designed and step by step description was also explained. The achieved Op-Amp specifications are summarized in Table 9. The rest of sub-blocks were designed one after another and results are summarized in chapters 4.3, 4.4, 4.5, 4.6 and 4.7.

The top level design simulation was made and it is described in chapter 4.8. The converter operates with sample frequency F_{SAMPLE} = 1MHz and supply voltage A_{VDD} =1.8V. Total power consumption of a circuit is 18mW. The ADC LSB value depends on ADC maximal input amplitude, which is A_{IN} = 0.45V or 0.9V peak-to-peak. The LSB corresponds to 220uV. Despite all efforts during the design and verification process, the ADC converts the signal with accuracy in terms of INL = ±4 LSB

and DNL = ±7 LSB over the whole input range. Possible error contributors are stated in chapters 2.6 and 4.8.

Based on previous experiences in design, the individual simulation test-benches were created using OCEAN scripting language embedded in Cadence core. This approach helps to precisely customize each simulation goals and control computational performance more accurately. Each test-bench can be run again as a batch or in single simulation mode. The scripts are attached in electronic form on CD-ROM.

The foreground calibration technique proposal is introduced for further accuracy enhancement at the end of the document in chapter 5.

BIBLIOGRAPHY

[1] HÁZE, J., R. VRBA, L. FUJCIK a O. SAJDL. Teorie vzájemného převodu analogového a číslicového signálu. Brno, 2006 [cit. 2015-12-14]. Skriptum. Vysoké učení technické v Brně.

[2] KLEDROWETZ, Vilém. The influence of MDAC resolution on basic blocks of pipelined AD converter[online]. Brno, 2009 [cit. 2015-12-14]. Dostupné z: https://www.vutbr.cz/studium/zaverecne-prace?zp_id. Master thesis. Vysoké učení technické v Brně. Supervisor Jiří Háze.

[3] CHO, Chang-Hyuk. A power optimized pipelined analog-to-digital converter design in deep sub-micron CMOS technology. 2005 [cit. 2015-12-14]. Ph.D. thesis. Georgia Institute of Technology.

[4] KLEDROWETZ, Vilem. Analysis of Non-ideal Effects of Pipelined ADC by Using MATLAB - Simulink: Pipelined Subranging ADCs [online]. ADVANCES in SENSORS, SIGNALS and MATERIALS, 2008 [cit. 2015-12-14].

[5] KLEDROWETZ, Vilem a Jiri HÁZE. MATLAB – SIMULINK MODEL OF PIPELINED ADC INCLUDE ERRORS ARISING IN SC TECHNIQUE [online]. Vysoké učení technické v Brně, 2010 [cit. 2015-12-14].

[6] BARRA, Samir, Souhil KOUDA a Abdelghani DENDOUGA. Simulink Behavioral Modeling of a 10-bit Pipelined ADC [online]. Algeria, 2013 [cit. 2015-12-14]. DOI: 10.1007/s11633-013-0706-0

[7] KESTER, Walt a James BRYANT. ADC Architectures VIII: Integrating ADCs. Analog Devices Inc [online]. 2008 [cit. 2015-12-14]. Dostupné z: http://www.analog.com/media/en/training-seminars/tutorials/MT-027.pdf

[8] KESTER, Walt. ADC Architectures III: Sigma-Delta ADC Basics [online]. 2008 [cit. 2015-12-14]. Dostupné z: http://www.analog.com/media/en/training-seminars/tutorials/MT-022.pdf?doc=cn0354.pdf

[9] KESTER, Walt. ADC Architectures II: Successive Approximation ADCs. Analog Devices Inc [online]. 2008 [cit. 2015-12-14]. Dostupné z: http://www.analog.com/media/en/training-seminars/tutorials/MT-021.pdf

[10] KESTER, Walt. ADC Architectures I: The Flash Converter. Analog Devices Inc [online]. 2008 [cit. 2015-12-14]. Dostupné z: http://www.analog.com/media/en/training-seminars/tutorials/MT-020.pdf

[11] KESTER, Walt. ADC Architectures V: Pipelined Subranging ADCs. Analog Devices Inc [online]. 2008 [cit. 2015-12-14]. Dostupné z: http://www.analog.com/media/en/training-seminars/tutorials/MT-024.pdf

[12] BUTTERFIELD, J.D. 12-Bit Pipelined ADC Design Project [online]. Boise State University, 2011 [cit. 2015-12-14]. Boise State University.

[13] BAKER, R.J. CMOS: Circuit Design, Layout and Simulation, 3rd Eddition [online]. 2011 [cit. 2015-12-14]. ISBN: 978-0-0470-88132-3.

[14] RAY, Sourja. Calibration of Multi-Bit per stage Pipelined ADC: Using Statistical Properties of Capacitor Arrays [online]. 2008 [cit. 2015-12-14]. Dostupné z: https://books.google.cz/books?id=xAqEiX_zRDIC

[15] WANG, X. a P.J. HURST. A 12-Bit 20-Msample/s Pipelined Analog-to-Digital Converter With Nested Digital Background Calibration [online]. In: . 2004, s. 1799-1808 [cit. 2015-12-14]

[16] ÖZGÜR, Çobanoğlu. Estimating Hand Calculation Parameters (K, μCox, Vth). Home Page of Özgür Çobanoğlu [online]. [cit. 2016-05-17]. Dostupné z: http://personalpages.to.infn.it/~cobanogl/lowlevelstuff/tutparext/

[17] RAZAVI, Behzad a Yun-Ti WANG. An 8-Bit 150-MHz CMOS A/D Converter. IEEE JOURNAL OF SOLID-STATE CIRCUITS. 2000, 35(NO. 3), 308 - 317.

[18] ALLEN,P., E., HOLBERG, D.,R. CMOS analog circuit design, second edition. Oxford University Press, New York 2002, ISBN 0-19-511644-5.

[19] SEDRA, S., A., SMITH, K, C. Microelectronics Circuits, fifth edition. Oxford University Press, New York 2004, p. 871-883, ISBN 0-19-51422-7.

[20] EVZELMAN, Michael. The effect of switching transitions on switched capacitor converters losses. *IEEE JOURNAL OF SOLID-STATE CIRCUITS*. Eilat, 2012, , 1-5. DOI: 10.1109/EEEI.2012.6377071. ISSN 978-1-4673-4682-5.

LIST OF USED SHORTCUTS AND SYMBOLS

ADC	Analog to Digital Converter
A_U	Voltage gain
DAC	Digital to Analog Converter
DNL	Differential Non-Linearity
GBW	Gain Bandwidth
INL	Integral Non-Linearity
KP_N	Transconductance parameter for NMOS transistor
KP_P	Transconductance parameter for PMOS transistor
L	Length of MOS transistor channe
Latch	Bistable Flip-Flop circuit
MDAC	Multiplying Digital to Analog Converter
Op-Amp	Operational Amplifier
SC	Switched Capacitor
SR	Slew Rate
sub-ADC	Analog to Digital Converter in MDAC block
sub-DAC	Digital to Analog Converter in MDAC block
V_{DD}	Power supply
V_{CM}	Common mode voltage
V_{DAC}	Voltage on sub-DAC output
V_{OFF}	Op-Amp offset voltage
V_{REF_P}	Positive reference voltage
V_{REF_N}	Negative reference voltage
V_{RESx}	Output voltage of MDAC
V_{RESx-1}	Input voltage of MDAC
V_{TH}	Threshold voltage
W	Width of MOS channel

LIST OF ATTACHMENTS

Attachment 0: Op-Amp evaluation simulations

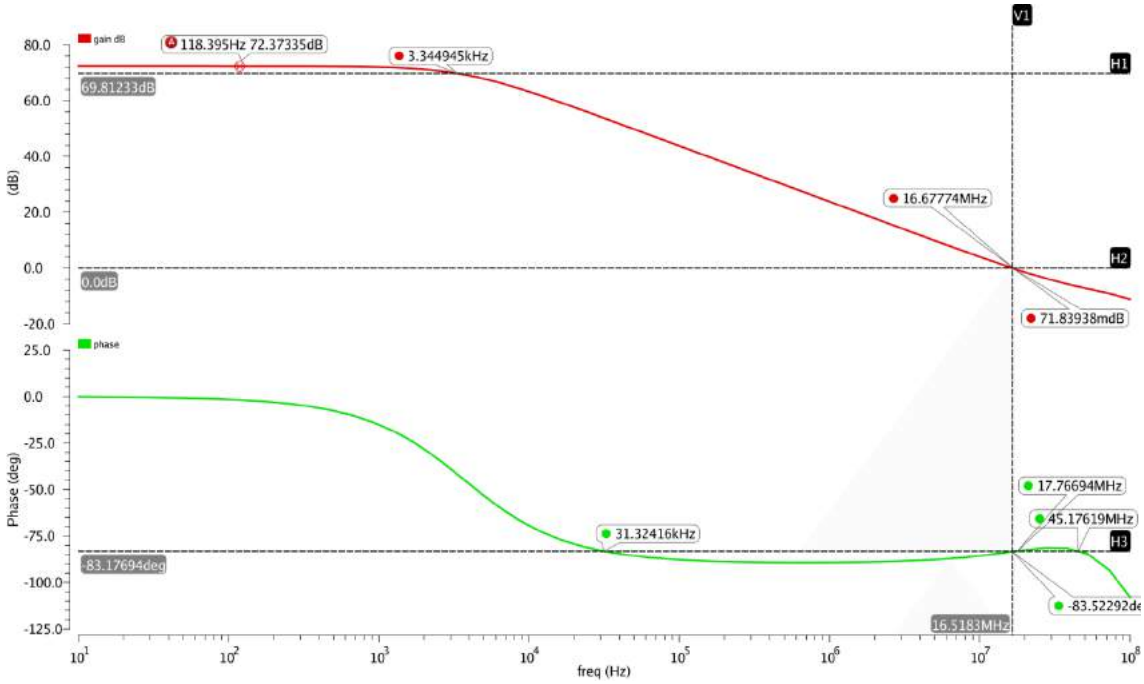


Figure Att. 1: Op-Amp Gain-Phase plot

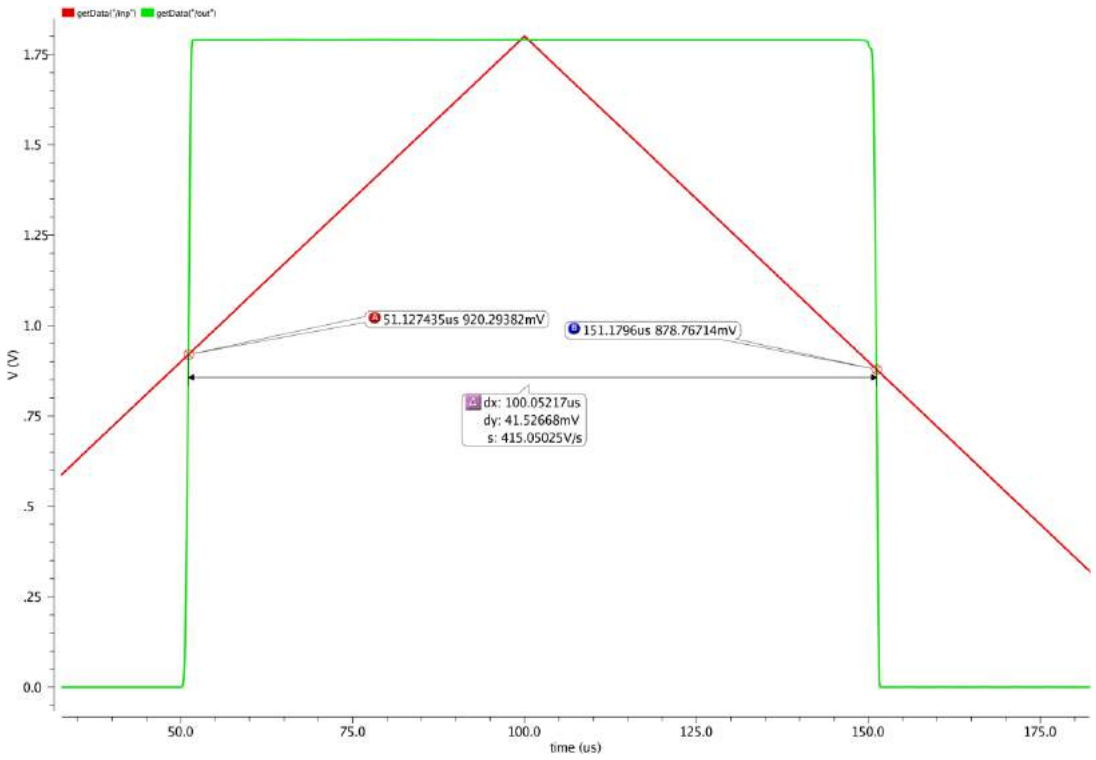


Figure Att. 2: Op-Amp hysteresis

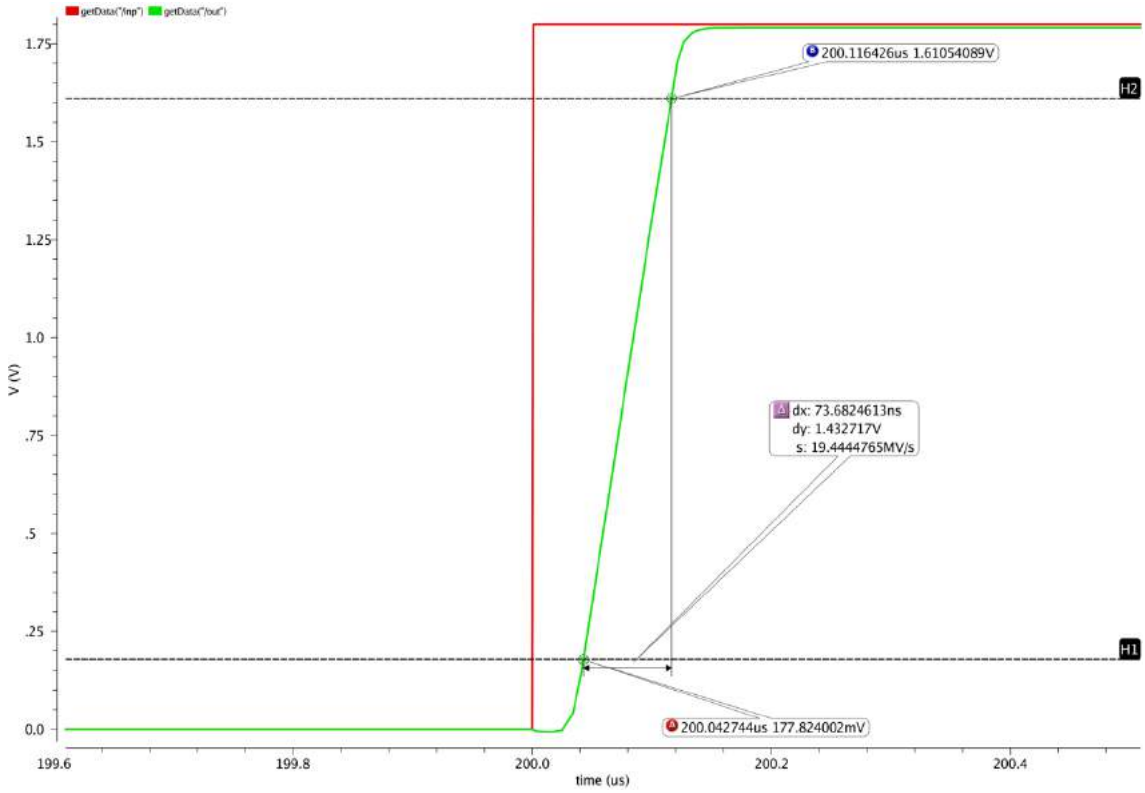


Figure Att. 3: Op-Amp slew rate – rising edge

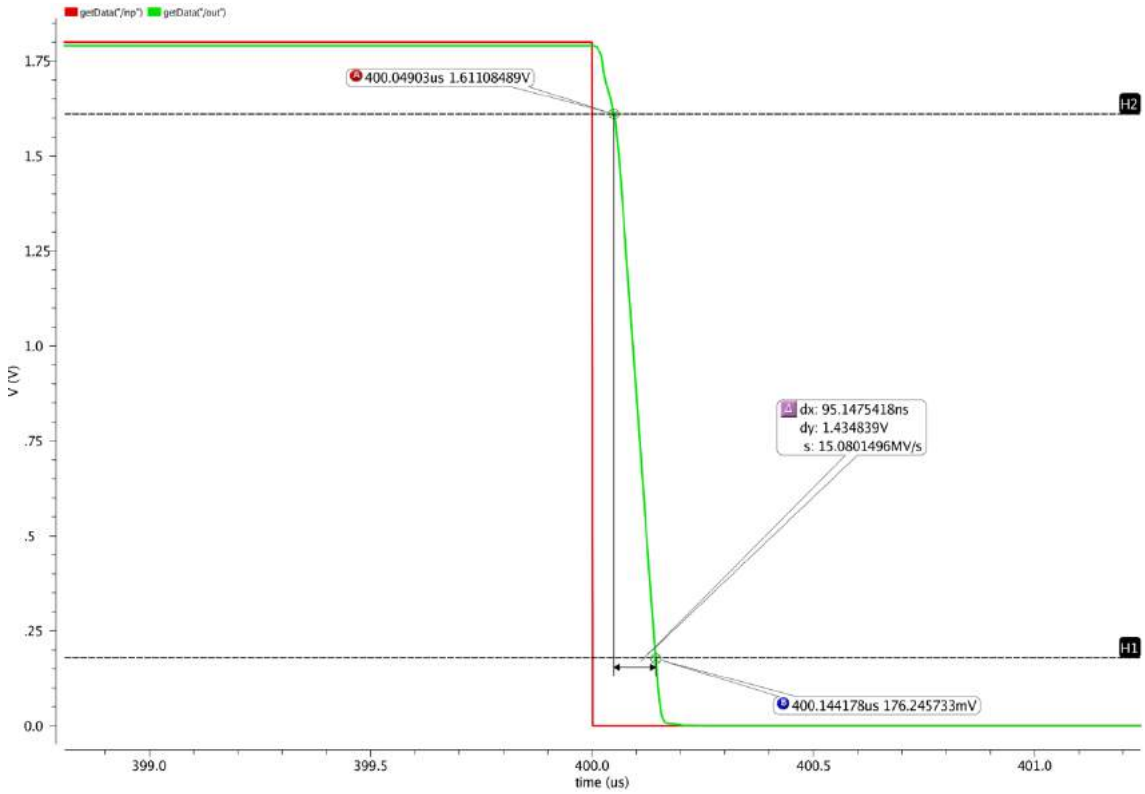


Figure Att. 4: Op-Amp slew rate – falling edge

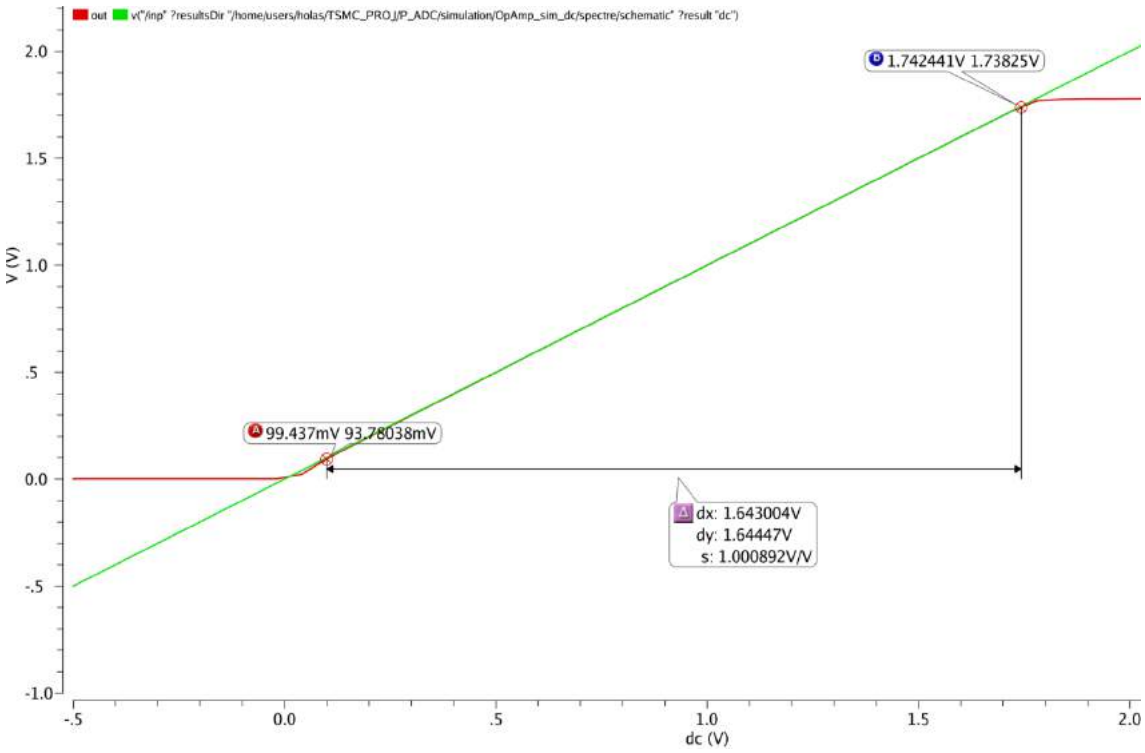


Figure Att. 5: Op-Amp input range

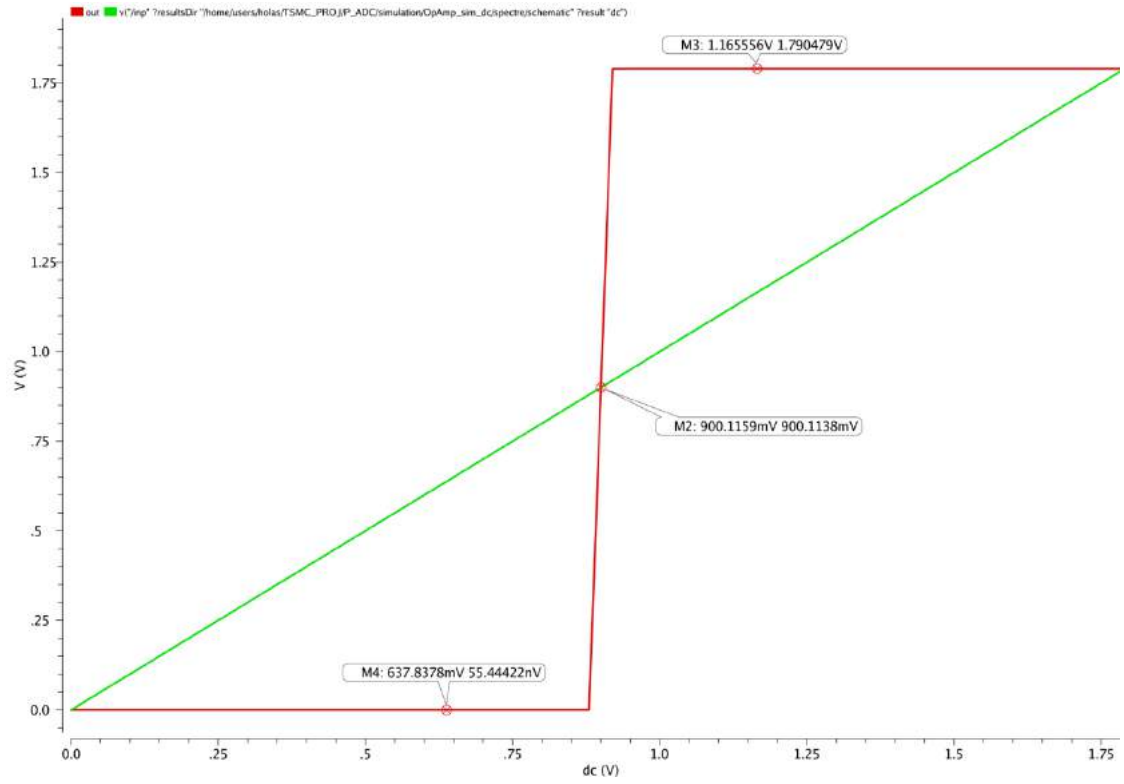


Figure Att. 6: Op-Amp output common mode range

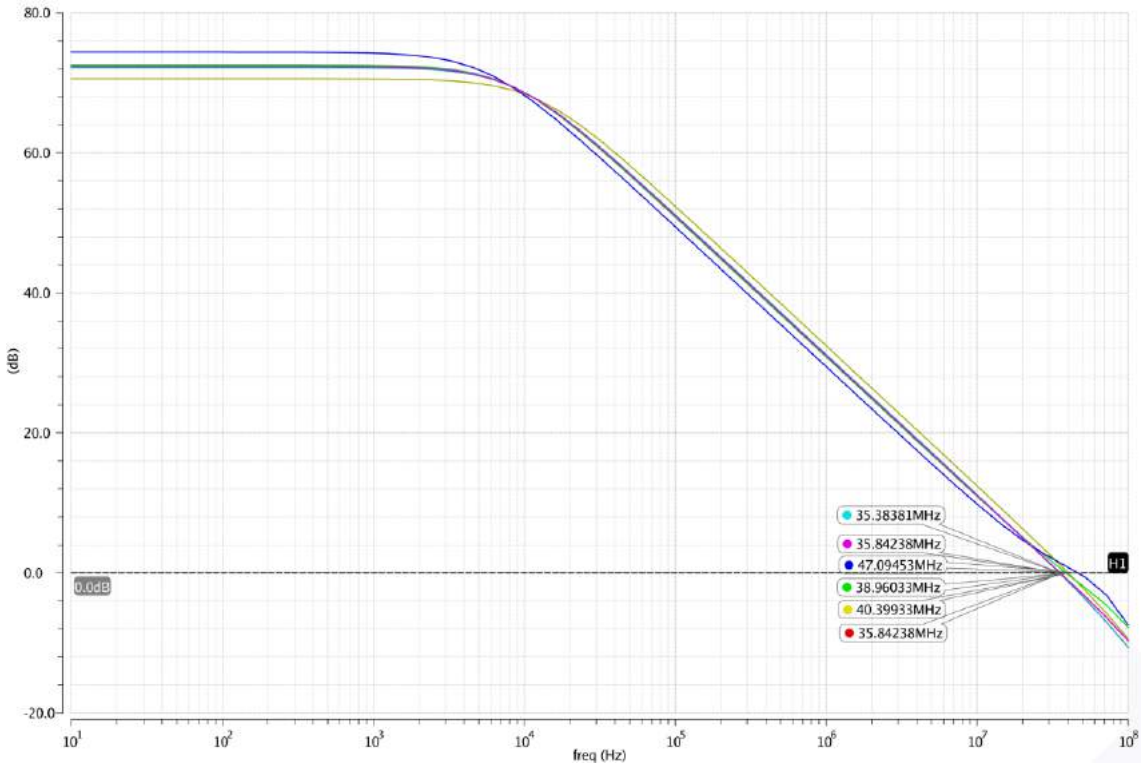


Figure Att. 7: Op-Amp corner analysis (ss,ff,fs,sf) – gain plot

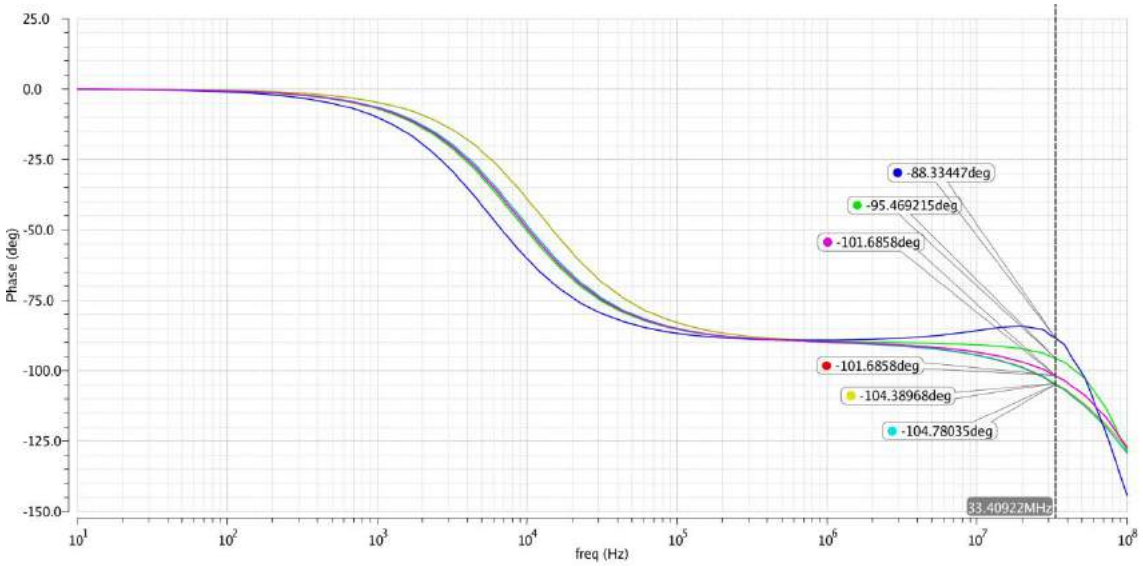


Figure Att. 8: Op-Amp corner analysis (ss,ff,fs,sf) – phase plot

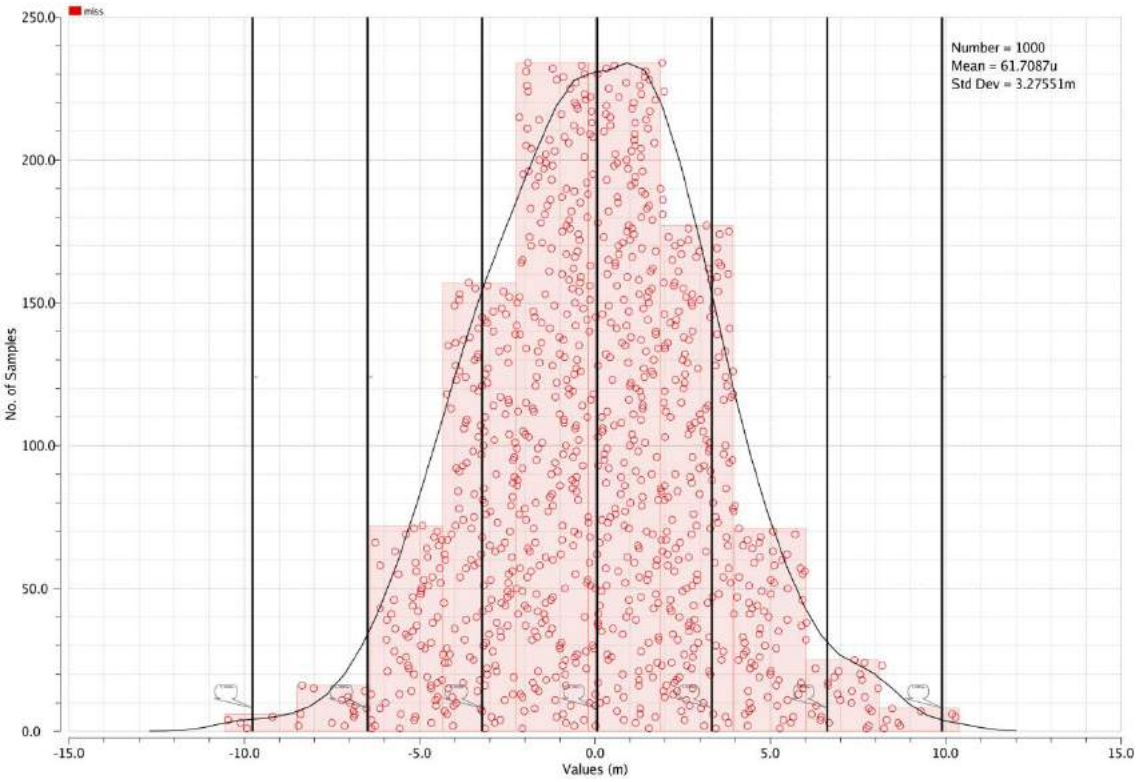


Figure Att. 9: Op-Amp matching analysis – systematic and random offset variation

```
Transistor's key parameters overview for component - OpAmp
This report was created with use of OCEAN scripting language with
own created functions that can be found in the attachement at the
end of the document and also in attached CD-ROM.

=============================================================
|-Device-|-Type-|--Vth---|Reg|----gm----|-Vdsat--|  ---Id----- |
|    M0    | Nmos |   0.584  | 2 |  0.000231 |   0.131 |   0.0000200 |
|    M1    | Pmos | -0.515 | 2 |  0.000235 | -0.114 | -0.0000200 |
|    M2    | Pmos | -0.515 | 2 |  0.000236 | -0.114 | -0.0000201 |
|    M3    | Pmos | -0.531 | 2 |  0.005574 | -0.104 | -0.0004417 |
|    M4    | Nmos |   0.584  | 2 |  0.000231 |   0.131 |   0.0000201 |
|    M5    | Nmos |   0.539  | 2 |  0.000465 |   0.120 |   0.0000401 |
|    M6    | Pmos | -0.696 | 1 |  0.000000 | -0.127 |   0.0000000 |
|    M7    | Nmos |   0.542  | 2 |  0.005198 |   0.119 |   0.0004417 |
|    M8    | Pmos | -0.523 | 2 |  0.000108 | -0.489 | -0.0000439 |
|    M9    | Nmos |   0.539  | 2 |  0.000512 |   0.120 |   0.0000439 |
|    M11    | Nmos | 0.539 | 3 |  0.000052 |   0.054 |   0.0000023 |
|    M12    | Nmos | 0.507 | 2 |  0.000005 |   0.773 |   0.0000023 |

Total power dissipiation is:
Ptot=    0.000950397   W
```

Figure Att. 10: Op-Amp DC analysis – transistor's saturation check report

Attachment 1: Full design schematics in Cadence environment – part 1

This appendix can be found on attached CD-ROM or on the A3 paper format in the back cover.

Attachment 2: Full design schematics in Cadence environment – part 2

This appendix can be found on attached CD-ROM or on the A3 paper format in the back cover.

Attachment 3: Full design schematics in Cadence environment – part 3

This appendix can be found on attached CD-ROM or on the A3 paper format in the back cover.

Attachment 4: The 2.5 MHz Pipeline ADC – additional simulations

This appendix can be found on attached CD-ROM or on the A3 paper format in the back cover.