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ÚSTAV RADIOELEKTRONIKY

AN EMC ROBUST PRECISE VOLTAGE REFERENCE FOR AUTOMOTIVE APPLICATIONS

EMC ROBUSTNÍ PŘESNÁ NAPĚŤOVÁ REFERENCE PRO AUTOMOBILOVÉ APLIKACE

DOCTORAL THESIS
DIZERTAČNÍ PRÁCE

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Abstract

A crucial component of modern integrated circuits is the voltage reference that acts like the heart for analog blocks providing stable voltage. This doctoral thesis explores advanced methods to reduce electromagnetic interference (EMI) susceptibility of low-power voltage references for an automotive environment with a wide temperature range. The EMI susceptibility is an unwanted phenomenon that can cause electronic system malfunctions. Electromagnetic disturbances can easily couple to the circuit via a cable harness and a printed circuit board. This thesis provides a literature overview, research suggestions, and results that focus on hidden effects in the voltage reference core, such as the impact of parasitic capacitance from bipolar transistors' collectors to the substrate and the effects of a used operational amplifier. Recommendations for improving voltage reference EMI robustness are presented and implemented. To prove the validity of the suggested improvements, test chips with proposed voltage references using various technologies were fabricated and measured.

Keywords

Bandgap voltage reference, Brokaw bandgap voltage reference, electromagnetic compatibility, electromagnetic interference, electromagnetic susceptibility, element-by-element extraction, passive network synthesis, transmission line, voltage reference.

Abstrakt

Klíčovou součástí moderních integrovaných obvodů je napěťová reference, která funguje jako srdce analogových bloků poskytující stabilní napětí. Tato disertační práce zkoumá pokročilé metody pro snížení citlivosti nízko příkonových referencí na elektromagnetické interference (EMI) pro automobilová prostředí s širokým teplotním rozsahem. Citlivost na EMI je nežádoucí jev, který může způsobit poruchy elektronického systému. Elektromagnetické rušení se může snadno vázat do obvodu prostřednictvím kabelového svazku a desky s plošnými spoji. Práce poskytuje přehled literatury, návrhy výzkumu a výsledky, které se zaměřují na skryté efekty v napěťovém referenčním jádru, jako je vliv parazitní kapacity z kolektorů bipolárních tranzistorů do substrátu integrovaného obvodu a efekty použitého operačního zesilovače. Jsou uvedena a implementována doporučení pro zlepšení EMI odolnosti napěťové reference. Aby se prokázala platnost navrhovaných vylepšení, byly vyrobeny a změřeny testovací čipy s navrženými napěťovými referencemi v různých technologiích.

Klíčová slova

Brokawova napěťová reference typu bandgap, elektromagnetická citlivost, elektromagnetická interference, elektromagnetická kompatibilita, extrakce prvek-po-prvku, napěťová reference typu bandgap, napěťová reference, přenosové vedení, syntéza pasivního obvodu.

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Declaration

I declare that I have written this doctoral thesis on the theme of "An EMC Robust Voltage Reference for Automotive Applications" independently, under the guidance of the supervisor, and using the technical literature and other sources of information which are all cited in the text and detailed in the list of literature at the end of this text. As the author of this text on the doctoral thesis, I furthermore declare that, as regards the creation of the text on the doctoral thesis, I have not infringed any copyright. In particular, I have not unlawfully encroached on anyone's personal and/or ownership rights and I am fully aware of the consequences in the case of breaking Regulation § 11 and the following of the Copyright Act No 121/2000 Sb., and of the rights related to the intellectual property right and changes in some Acts (Intellectual Property Act) and formulated in later regulations, inclusive of the possible consequences resulting from the provisions of Criminal Act No 40/2009 Sb., Section 2, Head VI, Part 4.

In Brno ....

Author's signature

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Contents

List of Symbols and Abbreviations

Symbols:

A	…	Area of the semiconductor junction, voltage gain.	[m^2, -]
B	…	Bandwidth.	[Hz]
C	…	Electric capacity.	[F]
f	…	Frequency.	[Hz]
gm	…	Transconductance.	[S]
I	…	Electric current.	[A]
J	…	Electric current density.	[A/m^2]
$\boldsymbol{J}_0$	...	The first order Bessel function of the first kind.	[-]
k	…	Boltzmann constant.	[J/K]
K	…	Scaling factor.	[-]
k_z	…	Impedance norm factor.	[-]
L	…	Electric inductance.	[H]
n	…	Temperature coefficient of charge carrier mobility.	[-]
P	…	Electric power.	[W]
q	…	Elementary charge of an electron.	[C]
Q	…	Quality factor of RLC circuit.	[-]
R	…	Electric resistance.	[Ω]
$\boldsymbol{s}$	…	Laplace operator.	[rad/s]
T	…	Absolute temperature, period of the signal.	[K, s]
T_a	…	Ambient temperature	[°C]
T_j	…	Junction temperature of semiconductor	[°C]
t	…	Time.	[s]
TC	…	Temperature coefficient.	[unit/K]
V	…	Electric voltage.	[V]
Y	…	Electric admittance.	[S]
Z	…	Electric impedance.	[Ω]
α	…	Current density temperature coefficient.	[-]
β	…	Electric current gain coefficient.	[-]

Δ	…	Absolute difference of value.	[-]
δ	…	Relative error.	[%]
λ	…	Channel length modulation factor.	[-]
μ	…	Average value.	[-]
σ	…	Standard deviation.	[-]
τ	…	Time constant.	[s]
φ	…	Electric phase.	[rad, °]
ω	…	Circular frequency.	[rad/s]

Abbreviations:

AC	…	Alternating Current.
BCD	…	Bipolar-CMOS and DMOS technology.
BCI	…	Bulk Current Injection.
BG	…	Band-Gap.
BLN	…	Buried Layer of N-type semiconductor.
CMOS	…	Complementary Metal Oxide Semiconductor technology.
CMRR	…	Common-Mode Rejection Ratio.
CTAT	…	Complementary to Absolute Temperature.
DC	…	Direct Current.
DMOS	…	Double-Diffused MOS transistor.
DPI	…	Direct Power Injection.
DTI	…	Deep Trench Isolation.
DUT	…	Device Under Test.
DVI	…	Direct Voltage Injection.
EMC	…	Electro-Magnetic Compatibility.
EME	…	Electro-Magnetic Emission.
EMI	…	Electro-Magnetic Interference.
ESD	…	Electro-Static Discharge.
GBW	…	Gain Band-Width.
GND	…	Electric ground.
HF	…	High-Frequency signal.

IC	…	Integrated Circuit.
ICM	…	Input Common Mode.
ICMR	…	Input Common Mode Range.
LC	…	Electric circuit consisting of inductor and capacitor.
NBLHV	…	High-voltage BLN.
NDMOS	…	N-type DMOS transistor.
NEPI	…	N-type semiconductor Epitaxial layer.
NMOS	…	N-type Metal Oxide Silicon transistor.
NPD	…	N-type Pass Device.
NPDAL	…	N-type Pass Device with Active Load.
NWELL	…	N-type semiconductor Well.
OPA	…	Operational Amplifier.
OTA	…	Operational Transconductance Amplifier.
PCB	…	Printed Circuit Board.
pdf	…	Probability density function.
PDMOS	…	P-type DMOS transistor.
PEPI	…	P-type semiconductor Epitaxial layer.
PMOS	…	P-type Metal Oxide Silicon transistor.
PPD	…	P-type Pass Device.
PPDAL	…	P-type Pass Device with Active Load.
PSRR	…	Power Supply Rejection Ratio.
PSUB	…	P-type semiconductor Substrate of IC.
PTAT	…	Proportional to Absolute Temperature.
PWELL	…	P-type semiconductor Well.
RC	…	Electric circuit consisting of resistor and capacitor.
RF	…	Radio Frequency signal.
RFI	…	Radio Frequency Interference.
RLC	…	Electric circuit consisting of resistor, inductor and capacitor.
SUB	…	Substrate of IC.
UGBW	…	Unity Gain Band-Width.
VCVS	…	Voltage-Controlled Voltage Source.

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INTRODUCTION

With the increasing advent of high-speed and radio frequency (RF) mix-signal devices, maintaining signal integrity and electromagnetic interference (EMI) susceptibility have become one of the major issues facing modern integrated circuit design. It must be noted that the automotive industry sets high requirements for electronics, especially for used semiconductors, concerning a very wide temperature operating range, ESD pulses, transient overvoltage pulses on supply and signal lines, supply voltage variations, requirements for very low electromagnetic emissions (EME), high immunity to EMI and low power consumption [1]. Harsh EMC disturbances can easily couple from the environment to the ICs through cabling harnesses or printed circuit board (PCB) tracks [2].

An EMC robust integrated circuit design together with a low power design sets a new challenge. One of the EMC robust design guidelines suggests to keep node impedances low and increase current biasing to improve the EMI immunity of the circuit [2]. This is directly opposite to a low-power design, where all currents are minimized. The low-power EMC robust design requires new circuit principles and circuit topologies, and the complete design is dictated by these requirements.

A commonly utilized reference for ICs is a bandgap voltage reference. It is a temperature-independent voltage reference circuit, which produces ideally a fixed (constant) voltage regardless of power supply variations, temperature changes, and circuit loading.

The main topic of this dissertation thesis is to define a methodology for a design of low power and EMC robust voltage references. The proposed EMC robust bandgap design recommendations verified by designs, simulations, and measurements of test chips are presented.

This work is divided into five chapters. Chapter 1 presents the state of the art. The main aims of the dissertation thesis are outlined in chapter 2. Chapter 3 discusses the EMI susceptibility measuring concept at an IC level, and chapter 4 lists all achieved results of the research. Finally, chapter 5 concludes the thesis.

1 STATE OF THE ART

A literature study and key aspects of current EMC robust voltage reference solutions are described in this chapter. This chapter also lists several used ideas to help focus the research effort for the dissertation.

1.1. Introduction to the Temperature Compensated Voltage Reference

The requirements for a stable and temperature-independent reference voltage are almost universal in electronic circuits. For this reason, the key parameter of voltage references is a temperature coefficient, which describes its temperature stability due to the temperature dependence of all circuit elements. The linear temperature coefficient is defined by the following equation [3]:

$$TC_{Vref} = \frac{1}{V_{ref}} \frac{\partial V_{ref}}{\partial T}, \tag{1}$$

where TC_{Vref} is the linear temperature coefficient of the output reference voltage, V_{ref} is the output reference voltage and T is an absolute temperature. According to the sign of the temperature coefficient, the temperature dependence is divided into PTAT (proportional to absolute temperature) and CTAT (complementary to absolute temperature) dependence of electric parameters. The PTAT has a positive and the CTAT has a negative temperature coefficient. The PTAT voltage can be created by a difference of two CTAT voltages with different temperature coefficient values. The sum of the appropriate CTAT and PTAT voltages, which are well predictable, ideally creates independent temperature voltage as is shown in Fig. 1 [4].

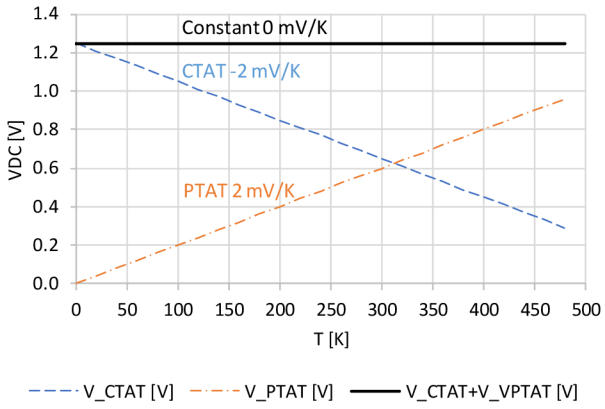


Fig. 1: An ideal first-order temperature compensation in electronic circuits [5].

This principle is generally used for first-order temperature compensation in analog circuit design. However, the practical circuit component's temperature dependences are not only linear (first order). The first-order compensation technique in most cases compensates sufficiently the dominant part of the temperature dependence.

Currently, there are higher-order temperature compensations, but due to their complexity, the first-order temperature compensation will be only described in this work. For example, the overall voltage reference accuracy can be described according to [3] by the following equation

$$\delta_{ref} = \frac{\Delta V_{IA} + \Delta V_{TC} + \Delta V_{LNR}}{V_{ref}}, \tag{2}$$

where ΔV_{IA} is absolute voltage initial accuracy given by production deviations, ΔV_{TC} is absolute voltage accuracy dependent on the temperature coefficient and ΔV_{LNR} is absolute voltage accuracy dependent on the line regulation (power supply).

1.2. Brokaw Bandgap Voltage Reference

The Brokaw bandgap [6] is very popular because it has better noise performance and smaller temperature drift at a lower quiescent current compared to the Kuijk reference [7]. Depending on the topology, the Brokaw reference normally has a lower power supply rejection ratio (PSRR) [7]. A voltage difference between two P-N junctions with different current densities is PTAT voltage (seen across a resistor $R3$ in Fig. 2). Voltage across a P-N junction with a constant current is CTAT voltage (V_{BE} of Q2). When summing these two voltages multiplied by a proper ratio, the first-order effects of CTAT and PTAT voltage temperature dependences are canceled out, and the resulting output voltage is temperature stable [6]. An idealized classical Brokaw bandgap voltage reference circuit is shown in Fig. 2.

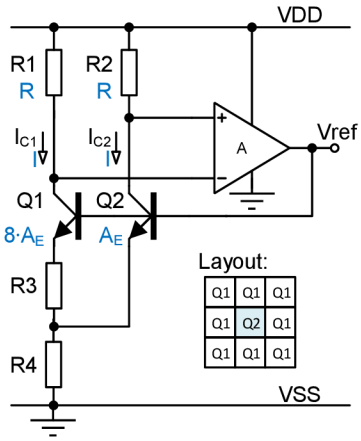


Fig. 2: Idealized two-transistor Brokaw bandgap cell [6].

The classical Brokaw bandgap (Fig. 2) usually employs the same collector currents I_{C1} and I_{C2} through bipolar transistors Q1 and Q2. This means that resistors $R1$ and $R2$ have the same value and the ratio N of emitter areas $A_{\mathrm{E1}}/A_{\mathrm{E2}}$ is usually 8 in order to get a common centroid layout due to bipolar transistors matching. When assuming infinite current gain β of used bipolar transistors then the reference output voltage V_{ref} is given by

$$V_{ref} = V_{BE2} + \left(1 + \frac{I_{C1}}{I_{C2}}\right)\frac{R4}{R3}\frac{kT}{q} ln\left(\frac{I_{C2}}{I_{C1}}\frac{A_{E1}}{A_{E2}}\right), \tag{3}$$

where k is Boltzmann constant $1.381 \cdot 10^{-23}$ J/K, T is the absolute temperature and q is elementary electron charge $1.602 \cdot 10^{-19}$ C. Note that $(kT)/q$ is a thermal voltage V_T. If the collector currents I_{C1} and I_{C2} are the same and the ratio of emitter areas is N, (3) can be simplified to

$$V_{ref} = V_{BE2} + 2\frac{R4}{R3} V_T \, ln(N). \tag{4}$$

For a deeper understanding of the first-order temperature compensation of the voltage reference, the V_{ref} voltage temperature dependence needs to be elaborated in more detail. This dependence can be deduced from the equation of the bipolar transistor base-emitter voltage V_{BE}, which is without Early effect given by

$$V_{BE} = V_T \, ln\left(\frac{I_C}{I_S}\right). \tag{5}$$

The I_S is a saturation current, and its temperature dependency is described in [8] and [9]. The output reference voltage of the Brokaw voltage reference (Fig. 2) can be expressed by the general following simple equation [8]

$$V_{ref} = V_{BE2} + KV_T, \tag{6}$$

where K is the scalable constant, which is used for minimizing the temperature dependency of V_{BE2} voltage. According to [10], the (6) can be expressed with temperature dependency by the following equation

$$V_{ref} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0\_Q2}\frac{T}{T_0} + (4 - n - \alpha)V_T \, ln\left(\frac{T_0}{T}\right) + KV_T, \tag{7}$$

where V_{G0} is a band-gap voltage at 0 K, and V_{BE0_Q2} is the voltage between the base and emitter of the Q2 bipolar transistor in the bandgap voltage reference core at temperature T_0. The n is the temperature coefficient of charge carrier mobility and α is the current density temperature coefficient. The reference voltage first-order temperature dependence factor equation is given by differentiation of (7) with respect to absolute temperature

$$\frac{\partial V_{ref}}{\partial T} = -\frac{V_{G0}}{T_0} + \frac{V_{BE0\_Q2}}{T_0} + (4 - n - \alpha)\frac{k}{q}\left[ln\left(\frac{T_0}{T}\right) - 1\right] + K\frac{k}{q}. \tag{8}$$

The K constant is calculated for the zero-temperature dependence factor of the reference voltage at the chosen reference temperature T_0 from equation (9) which is obtained from (8) by equating to zero and T_0 substitution for T

$$\left.\frac{\partial V_{ref}}{\partial T}\right|_{T=T_0} = 0 \Rightarrow K = \frac{V_{G0} - V_{BE0\_Q2} + (4 - n - \alpha)\frac{kT_0}{q}}{\frac{kT_0}{q}}. \tag{9}$$

Equating equation (6) to basic Brokaw reference voltage equation (4) yields equation (10), which describes a relationship between the K constant and a ratio of the resistors $R4$ and $R3$ as follows

$$K = 2\frac{R4}{R3}ln(N). \tag{10}$$

After that, the important resistor ratio for the first-order voltage temperature compensation can be calculated from the following equation

$$\frac{R4}{R3} = \frac{K}{2\,ln(N)}. \tag{11}$$

The main resistor $R3$ is calculated by the chosen main bias current I_{C1} of the voltage reference core according to (12) and then $R4$ is determined from (11). This resistor can be trimmable around its calculated value for TC_{Vref} tuning.

$$R3 = \frac{\Delta V_{BE}}{I_{C1}} = \frac{V_T ln(N)}{I_{C1}}. \tag{12}$$

Fig. 3 shows theoretically absolute and normalized reference voltage temperature characteristics of the described first-order temperature compensated voltage reference for various m coefficients with typical $R4/R3$ resistors ratio values. The coefficient m is a substitution for the term $(4 - n - \alpha)$ in above equations. A normalized reference voltage is normalized to the reference voltage at reference temperature T_0. The reference temperature is chosen as a mid-value from the considered entire temperature range. Note that the m coefficient never will be zero due to the existing temperature dependency of the charge carrier mobility and current density. The zero m coefficient shows an idealistic voltage temperature dependence example.

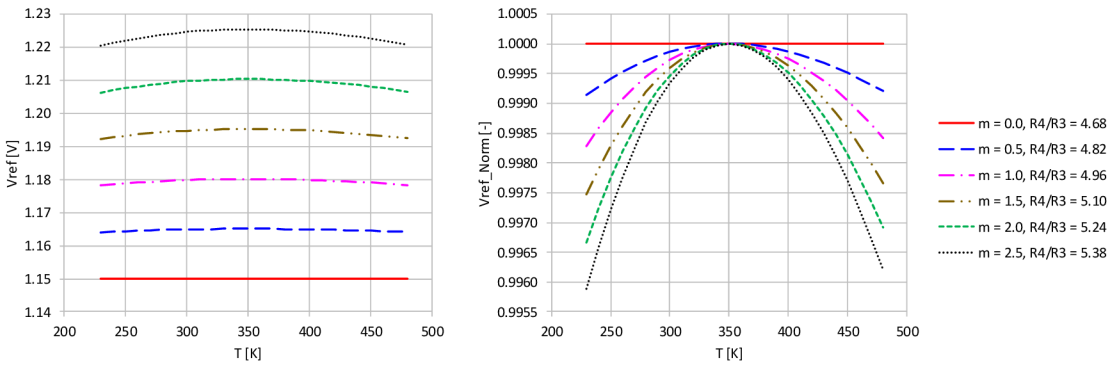


Fig. 3: The reference voltage temperature characteristics after first-order temperature compensation for various m coefficients (T_0 = 350 K).

1.3. Methods Used in Voltage References for EMI Susceptibility Reduction

Several papers about EMI susceptibility reduction of bandgap voltage references have been published [11] – [23]. The susceptibility of the Kuijk bandgap reference [24] is studied in several papers [11] – [19], but less attention is paid to the EMI susceptibility of the Brokaw bandgap reference [20] – [23]. The Kuijk and Brokaw voltage reference simplified circuit schematics are shown in Fig. 4.

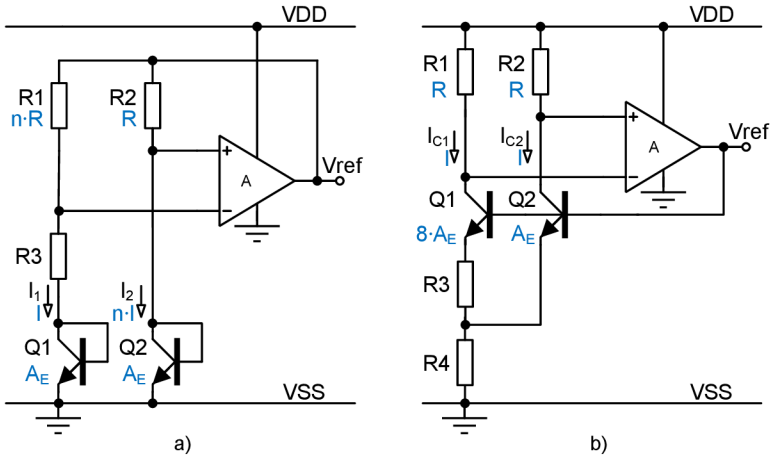
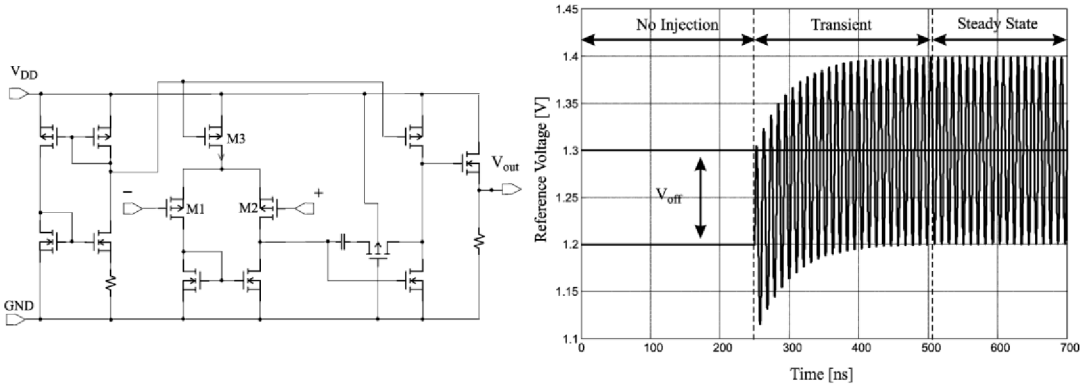


Fig. 4: Fundamental circuits of a) Kuijk [24] and b) Brokaw [6] voltage references.

The idea of papers [11] and [16] is, that designing a highly EMI immune operational amplifier (OPA) is a sufficient condition to increase overall EMI immunity of the bandgap. For example, a two-stage OPA with input PMOS devices differential amplifier is used in [11]. This OPA has a DC open loop gain of about 70 dB, a cutoff frequency of 6 MHz, and a common mode input swing from 0.6 to 4.0 V. The circuit schematic of the OPA and typical output voltage waveform of such Kuijk voltage reference in EMI presence at V_{DD} are shown in Fig. 5.



a) b)

Fig. 5: a) The PMOS-input two-stage Miller OPA circuit schematic and b) typical voltage reference output waveform in the presence of 100 MHz and 1 V amplitude EMI signal at V_{DD} supply [11].

The results of the measurements according to [11] point out that EMI-induced offset in the regulated reference voltage is closely connected to the nonlinear operation of the OPA included in the bandgap circuits. The impact of NMOS or PMOS pass device (M5 in following Fig. 6 a) - c)) at the output of the OPA is shown in [14]. The circuit schematics of such Kuijk voltage references and reference voltage DC shifts induced by 0.5 V amplitude EMI at power supply are shown in Fig. 6, where NPD means N-pass device, PPD is P-pass device and PPDAL is PPD with active load.

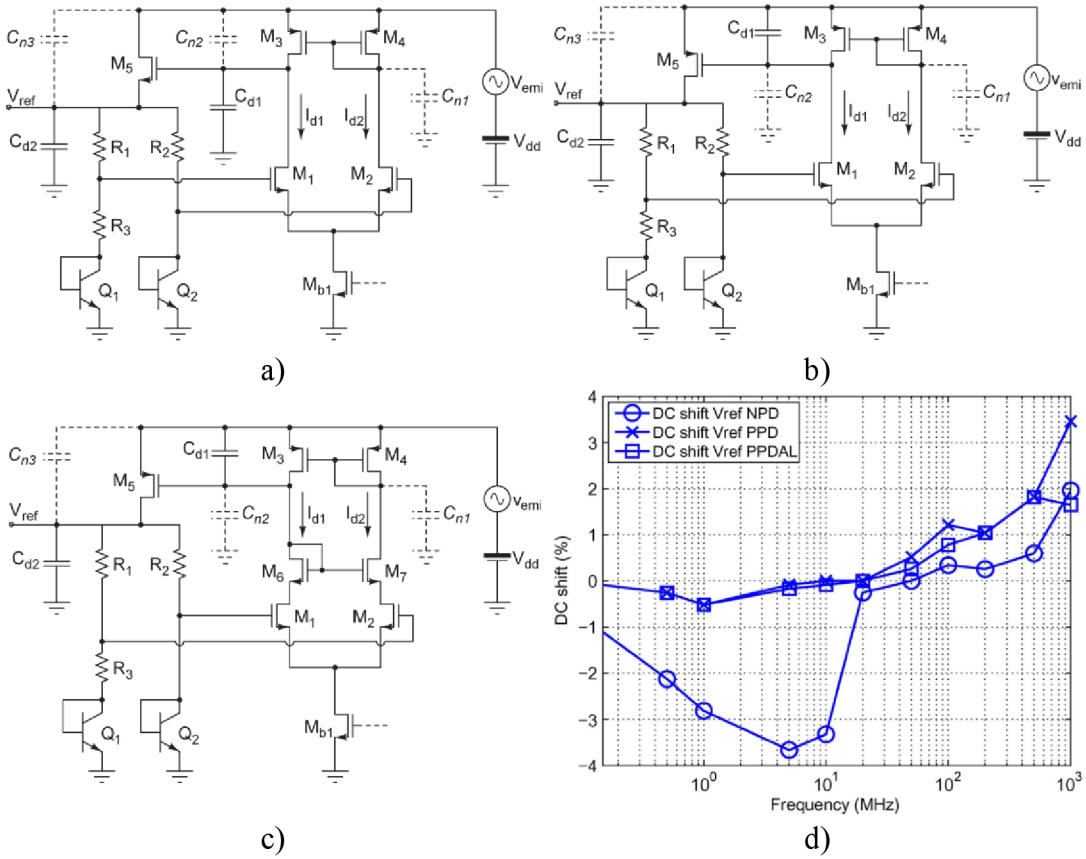
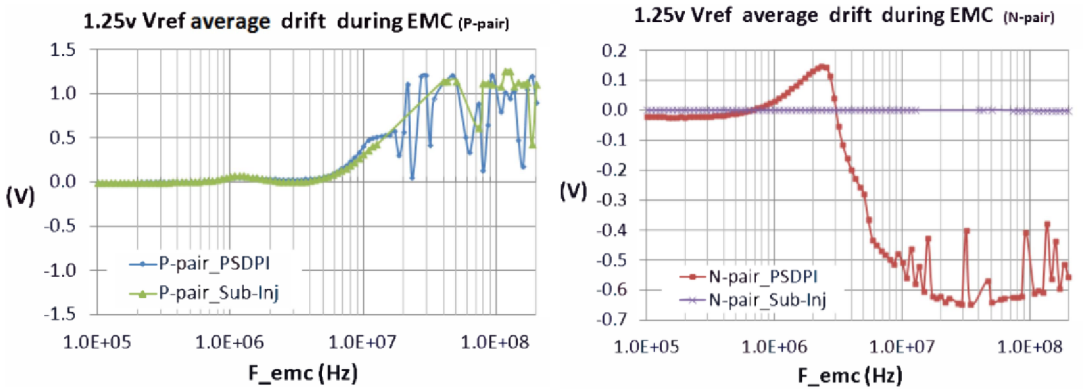


Fig. 6: Kuijk voltage reference with a) NPD or b) PPD or c) PPDAL OPA and d) DC voltage shift of these references for 0.5 V amplitude EMI at the power supply [14].

All OPAs have unity gain bandwidth (GBW) of about 3.6 MHz and a DC open loop gain of 50 dB except for PPDAL OPA which has a DC open loop gain of 61 dB. Measurement results of a test chip in Fig. 6 d) show a beneficial choice of the PPDAL OPA in the Kuijk bandgap circuit with good EMI performance [14].

The paper [15] presents important EMI facts in the field of the used OPA in voltage references as well. These facts are about a chosen input differential pair type influence on the EMI susceptibility of the used OPA. In [15] has been shown that the NMOS input differential pair has a little bit less power supply EMI susceptibility and greater substrate EMI injection immunity than the commonly used PMOS differential pair. These results were achieved by the simulations of the output reference voltage DC offsets induced by the 1 V amplitude EMI. The simulation results are shown in Fig. 7.



a) b)

Fig. 7: Power supply (PSDPI) and substrate (Sub-Inj) EMI susceptibility simulations of Kuijk voltage reference with a) PMOS or b) NMOS differential pair OPA [15].

A Miller operational transconductance amplifier (OTA) with a wide swing cascode current source used in [20] also shows its impact on the reference voltage offset induced by EMI at the power supply. This OTA has a DC open loop gain of about 83 dB with a 240 Hz cutoff frequency. The simulation results of such a Brokaw voltage reference with the real Miller OTA and an ideal OPA (same gain and cutoff frequency but without nonlinear effects) are shown in Fig. 8.

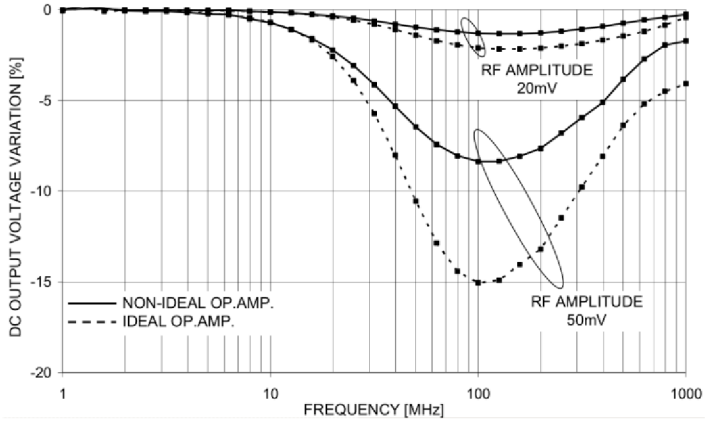
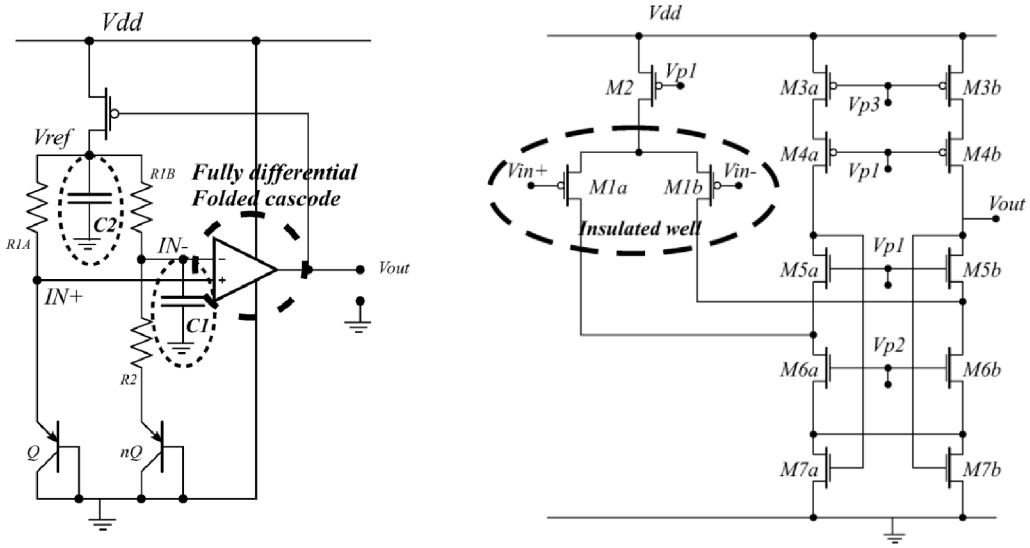


Fig. 8: Simulations of Brokaw voltage reference power supply EMI susceptibility with Miller OTA and an ideal OPA with the same gain and cutoff frequency [20].

The results show that the voltage reference EMI susceptibility is consequently determined by nonlinear effects induced in its basic core. In particular, the DC output voltage variation can be explained as the rectification phenomena concerning the NPN bipolar transistors in the voltage reference core [20]. This effect is supported by the Brokaw output voltage equation (4) from chapter 1.2 where it is clear that a change in the absolute value of the base-emitter voltage (mainly V_{BE2}) determines a shift of the output reference voltage, even if the OPA continues to work correctly (assuring good feedback and bipolar transistor currents mirroring).

For these reasons, many articles focus on how to provide good EMI signal filtering in the voltage reference core. As an example, can be used another Kuijk voltage reference with additional filtration capacitors and a fully symmetrical single-stage folded cascode OPA. Moreover, the differential pair of the OPA was created in an insulated well with the bulk terminal connected to the common source [16]. The circuit schematic diagrams of the voltage reference and OPA are shown in Fig. 9.



a) b)

Fig. 9: a) The improved Kuijk voltage reference with additional filtration capacitors and b) the fully differential folded cascode OPA [16].

The Kuijk voltage reference EMI improvements are supported by simulations, which point to the benefits using of the additional filtration capacitors $C1$ and $C2$ in the bandgap core. This design technique provides a good tradeoff between the voltage reference performance and good immunity to EMI, thanks to small changes in the circuit schematic and layout of the IC [16]. A simulated reference voltage offset induced by 0.5 V amplitude EMI at the supply line is shown in Fig. 10.

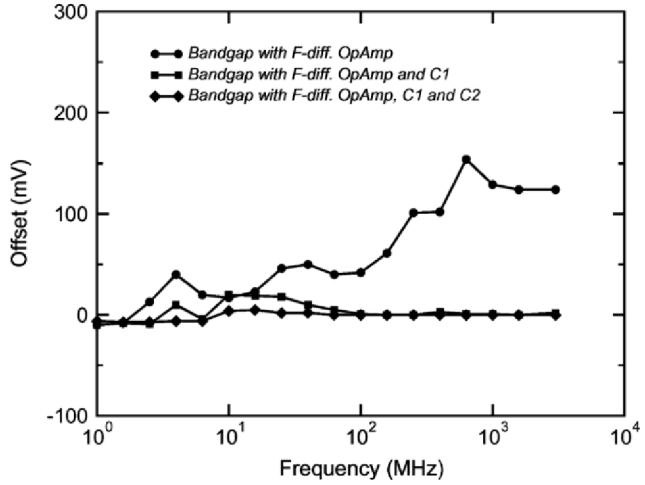


Fig. 10: Reference voltage offset of the improved Kuijk voltage reference induced by 0.5 V amplitude EMI at V_{DD} supply [16].

The EMI filtering in the Brokaw bandgap core to limit nonlinearity effects is also presented in [20] - [23] and layout modifications for higher immunity towards noises coming from the supply line are discussed in [11]. In order to reduce the EMI coupled to the BJTs base-emitter junction, some filtering can be used as well as a 500 fF capacitor between the base and emitter of Q2 in Brokaw bandgap circuit from Fig. 4 b) or the same capacitor between the Q2 emitter and ground in the same bandgap. Both approaches lead to a decrease in the voltage reference EMI susceptibility [21]. The capacitive filtering between the base-emitter of both Q1 and Q2 in the Brokaw bandgap core is used in [22] with a great result. The simulated power line EMI susceptibility results of the Brokaw bandgap filtering are shown in Fig. 11.

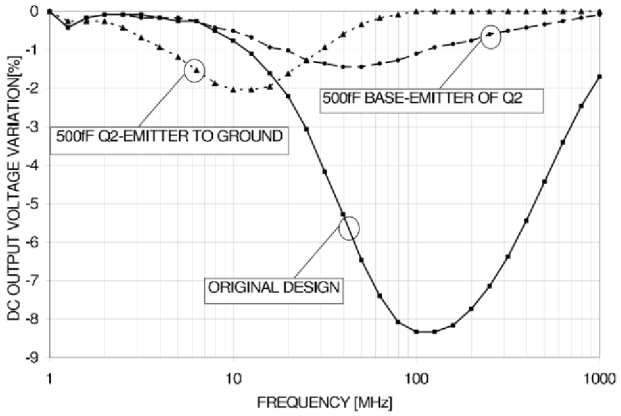
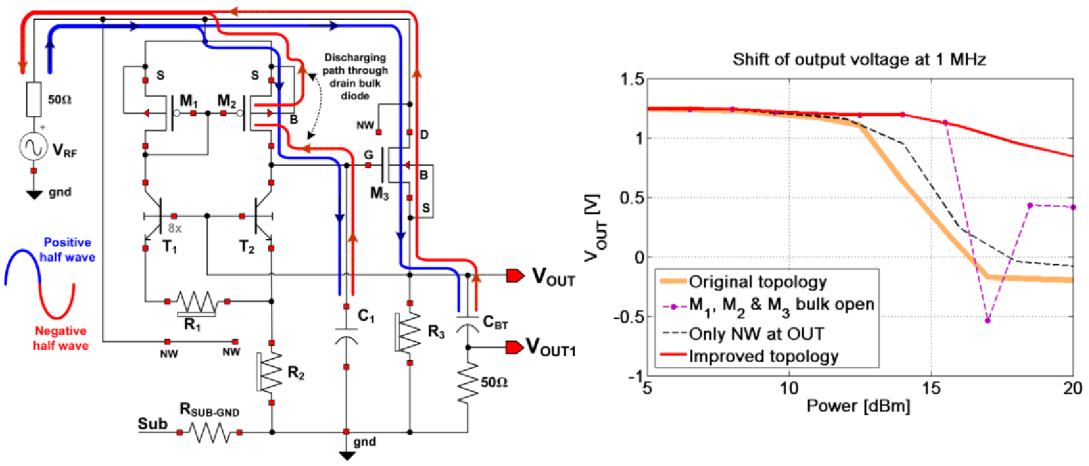


Fig. 11: The EMI supply line simulations of the Brokaw bandgap with the original design and with two different filtration solutions in the core [21].

Another phenomenon as a rectification on the drain-bulk diode of MOS transistors in a simple Brokaw bandgap is discussed with a possible solution in [23]. The simple Brokaw voltage reference circuit and its power line EMI simulation results for different EMI power levels and constant frequency are shown in Fig. 12, where improved topology means using all presented solutions (open bulk connections and N-well of P-body resistors connected to V_{OUT}).

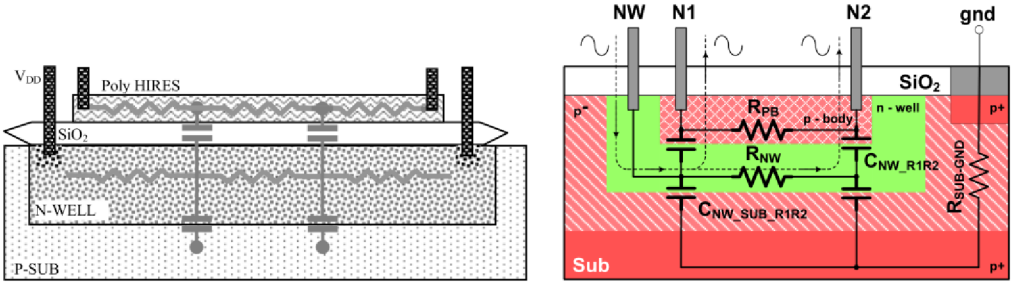


a) b)

Fig. 12: a) Interaction between M_2 and M_3 during the positive and negative half wave of high EMI excitation in original topology and b) output reference voltage DC offset induced by EMI at different power levels and constant frequency of 1 MHz [23].

The rectifications by drain-bulk diodes cause charging and discharging capacitors inside the voltage reference at a high-power line EMI level. The charging and discharging times of C_1 impact the charging and discharging time of C_{BT}, which is extracted from the measurement setup as a part of the voltage reference output load. Moreover, the charging and discharging of C_1 cause additional negative offset to the output reference voltage. A simple way to avoid drain-bulk diode activation is to leave bulk connections open. But this is not very typical in circuit design, because NMOS and PMOS transistors are always processed near to each other in the IC. Besides drain-bulk diodes, there is also a parasitic thyristor formed by e.g., layers of M_2 and M_3 in Fig. 12 a) [23]. The thyristor causes a possible risk known as a latch-up [25]. It is also possible to process dielectrically isolated circuits, at which each MOSFET is separated by an oxide-isolated well. In this case, the thyristor doesn't exist, and circuits are latch-up-free [23], but this technology is expensive.

The EMI susceptibility of the voltage references influenced by coupling through parasitic capacitances of polysilicon resistors (via isolation layer) is analyzed in [20], [21] and [15], and diffusion resistors are utilized and analyzed in [23]. The cross sections of one finger of polysilicon and a P-body diffusion resistor are shown in Fig. 13.



a) b)

Fig. 13: Simplified cross sections of one finger of a) the polysilicon resistor [20] and b) the P-body diffusion resistor [23].

An isolation N-well layer under resistors is always connected to the supply net. The designer can put a substrate guard ring around the bandgap cell resistors in order to reduce the disturbances below the overall bandgap cell. Another possible solution is using a triple-well beneath (buried N-layer and trenches) for the resistors that would create a series of capacitive connections toward both the supply net and the substrate [12]. These layout or technology solutions can be applied to reduce the EMI coupled from the resistors to the bipolar transistor's base-emitter junctions or possibly superimposed to the OPA differential pair inputs.

Another solution to this issue used in [23] is to avoid direct contact of the N-well to the power supply but connect the N-well somewhere else in order to provide a quieter node and increase the resistivity of the path to the supply network. To avoid activation of a parasitic diode between the N-well and the substrate if some unexpected fast transients appear, it is the best way for the N-well of the P-body resistors to connect to the output reference voltage V_{OUT}. The EMI simulation results of the original topology and resistors N-well connected at the output voltage of the Brokaw voltage reference from Fig. 12 a) are shown in the following Fig. 14.

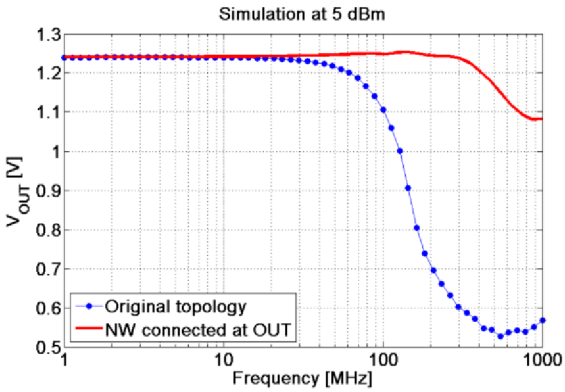
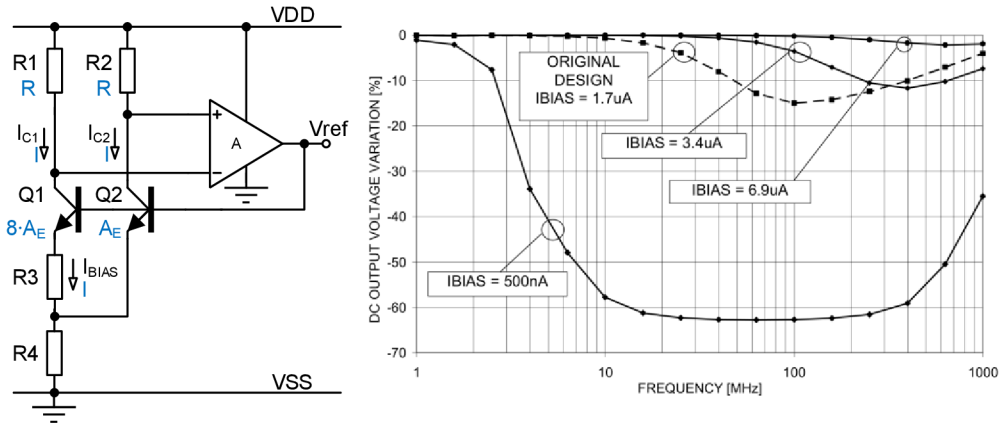


Fig. 14: Output reference voltage DC offset induced by EMI with original topology from Fig. 12 a) and topology when N-well of resistors is connected to V_{OUT} [23].

As can be seen from Fig. 14, the resistor's N-well reconnection to the output voltage has a great beneficial impact on the voltage reference EMI susceptibility. This fact is also confirmed by the results published in [15].

Another interesting point of view on the typically connected isolation layer of the bandgap resistors related to the chosen bias current of the bandgap core is described in [20]. In particular, an increase of the bias current implies a reduction of resistance $R3$ in the following Fig. 15 a), which intrinsically determines a decrease of the capacitive coupling from the resistor polysilicon and the underlying N-well. This situation reduces the bandgap core susceptibility to power supply EMI. The classical Brokaw bandgap circuit schematic and the EMI simulation results with different bandgap core bias currents are shown in Fig. 15.



a) b)

Fig. 15: a) Brokaw bandgap circuit and its b) VDD EMI susceptibility simulations of decreasing or increasing the basic bandgap core bias current [20].

According to [15], for a good global EMC performance in systems, it would be helpful to improve the power supply and substrate EMI susceptibility trade-off by following three factors: using N-differential pair OPA, connection isolation layer of bandgap resistors to a regulated output signal and adding some capacitors as high-frequency filters.

From the available literature, the generally used methods for voltage reference EMI susceptibility reduction can be summarized and formulated as follows:

a) Using a fully differential solution for high CMRR.

b) Using good symmetrical topology everywhere, where it is possible, for high CMRR and PSRR.

c) Keep all possible nodes in a low impedance state at high frequencies.

d) Limit bandwidth of all used external signals.

e) Make symmetrical filtering of all differential signals and keep the same time constants.

f) Count with hidden structures of the IC.

It must be noted that papers dealing with for example parasitic capacitances of used bandgap core bipolar transistors towards substrate were not found. Papers dealing with practical low power and EMC robust bandgap design were not found as well. The automotive ICs are characteristic of low current (low power) consumption that causes high impedance of power supply pins. This is the opposite of the typical EMC robust design, where it is necessary to keep a low-impedance state of the IC pins and internal nodes. Therefore, the research continues in this work by the investigation of the EMI coupled via substrate to the bandgap core and searching for a new EMC robust bandgap topology with new circuit principles.

2 AIMS OF DISSERTATION

This doctoral dissertation is focused on a study of bandgap voltage reference EMI susceptibility, especially in the automotive environment. The main aim of this dissertation is to define a methodology to improve the EMC robustness of low-power bandgap voltage references. Proposed methodology recommendations are verified by design, simulations, and measurements of bandgap references fabricated on test chips in various technologies.

To be able to study the EMC robustness of the voltage references, the first step is to understand how the IC EMI susceptibility is measured and how the measurement setup can be modeled in the IC impedance environment. A new method for impedance circuit modeling was formulated and implemented. It was utilized for a low power supply network with an EMC power supply filter (a bias-tee) which is used for the power supply EMI susceptibility measurement of the IC.

A detailed study of an existing low-power integrated bandgap voltage reference, which was designed for a harsh automotive environment with a wide temperature range from -40 °C to 160 °C and a demanding immunity to EMI, was performed and results are presented in this work. The possibilities of the power supply EMI susceptibility reduction of the voltage references are also discussed.

Based on this study, a new EMI simulation method was developed. The method involves creating a circuit model of the external coupling path and implementing new requirements for an improved voltage reference that can operate in an extended temperature range from -50 °C to 200 °C. Studies of different topologies for reference functional blocks were conducted, and results are presented in this work. From the achieved results, the best topology was selected and improved. A new methodology for EMC robust low-power voltage reference designs was proposed and verified by manufacturing a test chip with the proposed EMC robust voltage reference.

In summary, the most important aims of the dissertation thesis are:

a) Create a circuit model of the external impedance environment of the voltage reference with respect to EMI susceptibility analysis, measurements, and simulations.

b) Systematically analyze EMI susceptibilities of existing and commonly used integrated voltage references, which are divided into functional blocks, and analyze these blocks. Compare these results and draw conclusions.

c) Based on the outcome of the analysis, propose the best topologies, and try to further improve them with respect to EMI susceptibility. Perform a detailed theoretical study. Propose a design methodology for EMC robust low power bandgap voltage references.

d) Verify the proposed methodology by designing and manufacturing a test chip with a new EMC robust voltage reference and perform a detailed evaluation of the performance. Compare the expected and achieved results.

3 EMI SUSCEPTIBILITY MEASURING CONCEPT AT THE IC LEVEL

The first step of this dissertation is to understand how the IC EMI susceptibility is measured and how the measurement setup can be modeled in the IC impedance environment for analytical methods of circuit design.

3.1. Direct Power Injection Measurement Method

The RF Direct Power Injection (DPI) method to the dedicated IC pin described in IEC 62132-4 [26] is used for the EMI susceptibility measurement at the IC level. The typical DPI measurement setup with a directional coupler, which is used for an RF power measurement on a line, is shown in Fig. 16.

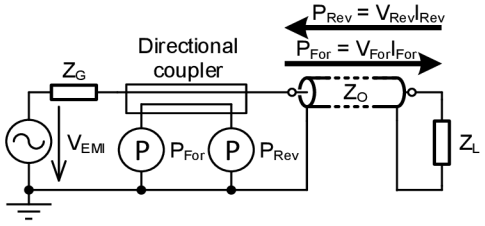


Fig. 16: RF power on the line and its transfer in the typical DPI setup [27].

The RF generator with amplifier is represented by the V_{EMI} sinusoidal voltage source with output (internal) impedance Z_G and the injected IC pin with the coupling capacitor is represented by load impedance Z_L. It must be noted that the value of the coupling capacitor has to be selected with respect to the functionality of the applied IC pin (e.g., according to the maximum capacitive load of the pin). The directional coupler should be matched to the characteristic impedance Z_O and it is always placed between the source and the coaxial line. The source side of the line is matched to its source and therefore the measured forward power P_{For} is equal to the source nominal power P_N [27].

For a deeper understanding of RF power and how can be simulated for the worst-case situation, the power of the alternating current needs to be discussed in more detail. Consider a sinusoidal EMI signal, where its power is the product of instantaneous voltage and current. The alternating voltage V_{AC} and current I_{AC} can be described by the following equations

$$V_{AC} = V_{Peak}\, sin(\omega t + \varphi_V), \tag{13}$$

$$I_{AC} = I_{Peak}\, sin(\omega t + \varphi_I), \tag{14}$$

where V_{Peak} (I_{Peak}) is the amplitude, ω is the angular frequency, t is time, and φ_V (φ_I) is a phase of the alternating voltage or current. The alternating power oscillates around its average value as described by the following equation

$$P_{AC} = V_{AC} I_{AC} = \frac{1}{2} V_{Peak} I_{Peak} [cos(\varphi_V - \varphi_I) - cos(2\omega t + \varphi_V + \varphi_I)]. \tag{15}$$

The average value of the alternating power is typically measured by power sensors on R_{RF} resistors, which is equal to characteristic impedance Z_O due to impedance matching (minimum reflection is obtained). The average value of e.g., forward wave power can be calculated according to the following equations

$$P_{For} = \frac{1}{2} I_{ForPeak}^2 R_{RF}, \tag{16}$$

$$P_{For} = \frac{1}{2} \frac{V_{ForPeak}^2}{R_{RF}}. \tag{17}$$

In order to easily cover and read a high dynamic range of power values, the absolute value of power is often expressed as a level in dBm, which is a value relative to the nominal power of 1 mW [27]

$$P_{For\_dBm} = 10\, log\left(\frac{P_{For}}{0.001W}\right)\ [dBm]. \tag{18}$$

A general RF coaxial cable or an RF coaxial transmission line has a 50 Ω characteristic impedance. It must be noted that the output of the used coaxial line can be connected to the impedance whose value is unknown [28]. For this reason, there can be three general cases of transmission line loading as shown in Fig. 17.

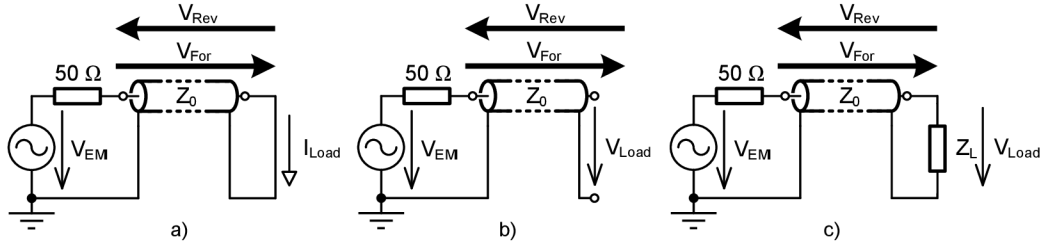


Fig. 17: Three possible states of the RF power injection: a) short, b) open, and c) general load at the end of the transmission line (DPI coupling point).

In the case of short-circuited end of the transmission line, the maximum I_{Load} current flows through the line which can be expressed by equation (19) for $Z_L = 0$ Ω (impedance of ideal electrical short) if the loss-less transmission line is considered.

$$I_{Load} = V_{EMI} \frac{1}{50 + Z_L}. \tag{19}$$

On the other hand, the maximum V_{Load} voltage appears at the line end in the case of the open-circuited end of the transmission line. This voltage can be expressed from the equation for a general loaded loss-less transmission line (20) where Z_L is infinity (impedance of ideal open circuit). For this situation, the maximum V_{Load} voltage is equal to V_{EMI}.

$$V_{Load} = V_{EMI} \frac{Z_L}{50 + Z_L} = V_{EMI} \frac{1}{\frac{50}{Z_L} + 1}. \tag{20}$$

Another explanation for the voltage at the transmission line end can be by using voltage standing wave description on the line with very HF excitations with wavelength shorter than the length of the line according to [29] and [30]. For this situation, it can be considered a 1 GHz voltage wave that is propagated from input to output of the transmission line, which has, in the worst cases, a short or open-circuited end. These situations are shown in Fig. 18 which describes voltage standing waves caused by voltage wave reflections from different transmission line ends (short or open end).

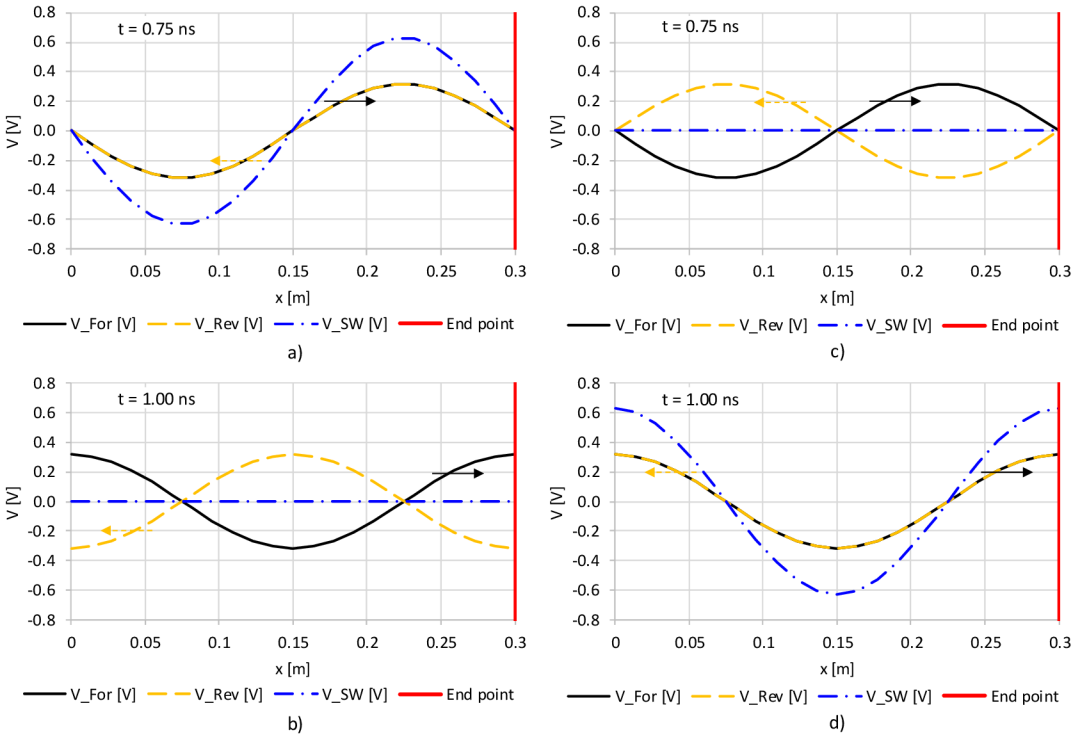


Fig. 18: Examples of 1 GHz ideal voltage standing waves at the endpoint of the lossless line for a) and b) short or c) and d) open-circuited end for two different times and P_{For} = 1 mW (0 dBm).

The worst case of the load voltage is for the open-circuited transmission line end as is shown in Fig. 18 d). Because the low-power IC has low power current consumption and its decoupling capacitors are not often effective at very high frequencies, the high impedance state at the power supply line end can be considered. Therefore, the worst case for the EMI simulation is the DPI to high impedance load. The basic power supply EMI susceptibility simulation is performed with DC and AC (EMI) voltage sources connected in series to form one voltage source, that supplies the analyzed IC.

3.2. Impact of the DPI Measurement Setup

The EMI susceptibility of the real IC is often given by an IC environment. The IC environment is considered such as electric impedances of bond wires, lead frame, and PCB tracks with electrical components at the IC inputs and outputs. An equivalent circuit model of the RF DPI coupling path to the IC pin is a vital task for the IC EMI susceptibility simulation.

3.2.1. Synthesis of Passive Circuit Network Model

The passive circuit network model synthesis form required circuit function is a classical well-known subject in the electrical circuit theory which was researched in a "golden era" from the 1930s to 1970s, for example [31] and [32]. Nowadays modeling of passive network elements according to high-frequency S-parameters is developed for example in [33] – [35]. The disadvantage of these methods is a very long execution time with many different measurements. The following text describes an extended passive network synthesis method, which requires only a simple two-terminal impedance frequency characteristic measurement.

The passive network model synthesis is an estimation of all passive circuit elements of the circuit model which is valid for the required circuit function in a specified range (e.g., frequency range) and conditions (simplifications). According to [36], the known techniques for a linear system equivalent calculation frequency domain are:

a) A resonance frequency matching method,

b) A corrective filter method,

c) A continuous fractional expansion method, and

d) An approximate Foster equivalent method.

These methods are examples of different iterative direct synthesis techniques. The advantages of direct methods are simple and straightforward calculations. The following described synthesis method based on the element-by-element extraction algorithm [36] is modified and extended to calculate serial and shunt resistors as lossy elements of a passive (linear) circuit network.

The first step of passive network model synthesis from the measured impedance frequency characteristic is obtaining the impedance frequency function [37]. The Laplace representation of impedance can be described by a rational function. The polynomial roots of the rational impedance function determine the impedance frequency characteristic shape. The general impedance rational function according to [36] and [38] with a scaling constant K is given by the following equation

$$Z(\boldsymbol{s}) = \frac{N(\boldsymbol{s})}{D(\boldsymbol{s})} = \frac{\sum_{k=0}^{n} a_k \boldsymbol{s}^k}{\sum_{l=0}^{m} b_l \boldsymbol{s}^l} = K \frac{\prod_{k=1}^{n} (\boldsymbol{s} - \boldsymbol{s}_{z,k})}{\prod_{l=1}^{m} (\boldsymbol{s} - \boldsymbol{s}_{p,l})}, \tag{21}$$

where $N(\boldsymbol{s})$ is the numerator polynomial, $D(\boldsymbol{s})$ is the denominator polynomial, a_k is the k-th numerator polynomial coefficient, b_l is the l-th denominator polynomial coefficient, $\boldsymbol{s}_{z,k}$ is the k-th position of impedance zero, $\boldsymbol{s}_{p,l}$ is the l-th position of impedance pole in the complex **s**-plane and $\boldsymbol{s}$ is the Laplace variable. The Laplace variable $\boldsymbol{s}$ is known as a complex frequency and for a sinusoidal steady-state linear circuits calculation (or an AC analysis) following substitution according to [39] is used

$$\boldsymbol{s} = \sigma + j\omega = 0 + j2\pi f, \tag{22}$$

where σ is the damping factor, j is the imaginary unit of the complex number, ω is the angular frequency and f is the frequency of the excitation (or driving) signal. In a case when only purely complex conjugate imaginary root pairs of impedance function polynomials will be considered then the impedance function according to [37] is

$$Z(\boldsymbol{s}) = K\frac{\prod_{k=1}^{\frac{n}{2}}\left(\boldsymbol{s}^2 + \omega_{2z,k}^2\right)}{\prod_{l=1}^{\frac{m}{2}}\left(\boldsymbol{s}^2 + \omega_{2p,l}^2\right)}. \tag{23}$$

When will be assumed one pole at the beginning of a complex $\boldsymbol{s}$-plane due to a reference circuit element (in the $\boldsymbol{s}$-plane origin, e.g. a coupling capacitor) then the impedance function will be in the following form

$$Z(\boldsymbol{s}) = K\frac{\prod_{k=1}^{\frac{n}{2}}\left(\boldsymbol{s}^2 + \omega_{2z,k}^2\right)}{\boldsymbol{s}\prod_{l=2}^{\frac{m-1}{2}}\left(\boldsymbol{s}^2 + \omega_{2p,l}^2\right)}, \tag{24}$$

where $\omega_{2z,k}$ is k-th angular serial resonance frequency (angular frequency of double zero) of impedance function and $\omega_{2p,l}$ is l-th angular parallel resonance frequency (angular frequency of double pole) of impedance function. The serial resonance frequency is reflected as a local impedance minimum with zero impedance phase at this frequency. The parallel resonance frequency is reflected as a local impedance maximum with zero impedance phase at this frequency [40].

This extended passive network model synthesis method aims to add frequency bandwidths of impedance resonances to obtain lossy elements (resistors and conductors) of the passive circuit model for cases with quality factors lower than infinity. For this situation, a biquad impedance function with complex conjugate pairs of zeros and poles is according to [41]

$$Z(\boldsymbol{s}) = \frac{\boldsymbol{s}^2 + \frac{\omega_z}{Q_z}\boldsymbol{s} + \omega_z^2}{\boldsymbol{s}^2 + \frac{\omega_p}{Q_p}\boldsymbol{s} + \omega_p^2}, \tag{25}$$

where ω_z is the angular serial resonance frequency, Q_z is the zero-quality factor, ω_p is the angular parallel resonance frequency and Q_p is the pole quality factor of the biquad impedance function. By comparing this function with the general quality factor equation according to [42]

$$Q = \frac{\omega_0}{B}, \tag{26}$$

where Q is the bandpass (or resonance) quality factor, ω_0 is the center (or resonance) frequency and B is the bandpass (or resonance) frequency bandwidth, the following impedance function with frequency bandwidths of each resonance and one pole at the beginning of $\boldsymbol{s}$-plane is obtained

$$Z(\boldsymbol{s}) = K\frac{\prod_{k=1}^{\frac{n}{2}}\left(\boldsymbol{s}^2 + B_{2\mathrm{z},k}\boldsymbol{s} + \omega_{2\mathrm{z},k}^2\right)}{\boldsymbol{s}\prod_{l=2}^{\frac{m-1}{2}}\left(\boldsymbol{s}^2 + B_{2\mathrm{p},l}\boldsymbol{s} + \omega_{2\mathrm{p},l}^2\right)}, \tag{27}$$

where $B_{2\mathrm{z},k}$ is the k-th angular frequency bandwidth of serial resonance, and $B_{2\mathrm{p},l}$ is the l-th angular frequency bandwidth of parallel resonance. For passive circuit model synthesis, it is necessary to calculate all polynomial coefficients of the impedance rational function (21) after substituting resonance frequencies and their bandwidths with numeric values into the impedance function (27). The scaling constant K includes an impedance norm coefficient that is described by the following equation

$$k_{\mathrm{Z}} = \frac{Z_{\mathrm{norm}}(\boldsymbol{s})}{Z(\boldsymbol{s})}, \tag{28}$$

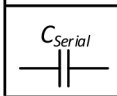
$$K = \frac{1}{k_{\mathrm{Z}}}, \tag{29}$$

where k_{Z} is the impedance norm, Z_{norm} is the normalized impedance and Z is the original impedance [43].

A numerator polynomial degree n of impedance function (21) may be different from a denominator polynomial degree m by no more than one. If this condition is violated, then the circuit model cannot include passive circuit elements only (resistors, conductors, inductors, and capacitors) [36]. The values of angular frequencies can be normalized to the lowest resonance frequency for reducing large numbers in calculations. A software multiplication of polynomials can be done using a simple polynomial multiplication algorithm mentioned for example in [44].

After obtaining all coefficients of the rational impedance function (21) and fulfillment of the passive circuit elements condition, the next step is a passive network model elements extraction. In [36], a nice algorithm is used to extract simple circuit elements from the impedance function. This algorithm is extended to serial and shunt resistors (lossy elements) calculation. The proposed element-by-element extraction algorithm is shown in Appendix 1. The polynomial division is used for the impedance elements calculation which brings six considered solutions from all possible solutions summarized in Tab. 1.

Tab. 1: Simple circuit element extraction conditions and calculations (the first step of extraction for this case, for the next step, there is residual polynomial after polynomials division) [28].

Element	$Z_x(s)$ or $Y_x(s)$	Conditions of $Z(s)$ function	Element value
	$Z_x(\boldsymbol{s}) = R_{\text{Serial}}$	$n = m, D[m] > 0$ and the previous element is $Z(\boldsymbol{s})$ type	$R_{\text{Serial}} = \frac{N[n]}{D[m]}$
	$Y_x(\boldsymbol{s}) = G_{\text{Shunt}}$	$n = m, N[n] > 0$ and the previous element is $Y(\boldsymbol{s})$ type	$G_{\text{Shunt}} = \frac{D[m]}{N[n]}$
	$Z_x(\boldsymbol{s}) = \boldsymbol{s}L_{\text{Serial}}$	$n > m$ and $D[m] > 0$	$L_{\text{Serial}} = \frac{N[n]}{D[m]}$
	$Z_x(\boldsymbol{s}) = \frac{1}{\boldsymbol{s}C_{\text{Serial}}}$	$N[0] > 0$ and $D[0] = 0$	$C_{\text{Serial}} = \frac{D[1]}{N[0]}$
	$Y_x(\boldsymbol{s}) = \frac{1}{\boldsymbol{s}L_{\text{Shunt}}}$	$N[0] = 0$ and $D[0] > 0$	$L_{\text{Shunt}} = \frac{N[1]}{D[0]}$
	$Y_x(\boldsymbol{s}) = \boldsymbol{s}C_{\text{Shunt}}$	$n < m$ and $N[n] > 0$	$C_{\text{Shunt}} = \frac{D[m]}{N[n]}$
$Z(\boldsymbol{s}) = \frac{N(\boldsymbol{s})}{D(\boldsymbol{s})} = \frac{N[0] + N[1]\boldsymbol{s} + N[2]\boldsymbol{s}^2 + \cdots + N[n]\boldsymbol{s}^n}{D[0] + D[1]\boldsymbol{s} + D[2]\boldsymbol{s}^2 + \cdots + D[m]\boldsymbol{s}^m}$			

The following equations (30) – (32) show an example of impedance rational function polynomial divisions (without resonance bandwidths for clarity), where $Res_x(\boldsymbol{s})$ is the residual polynomial.

$$Z(\boldsymbol{s}) = \frac{N(\boldsymbol{s})}{D(\boldsymbol{s})} = Z_1(\boldsymbol{s}) + \frac{Res_1(\boldsymbol{s})}{D(\boldsymbol{s})}, \tag{30}$$

$$\frac{D(\boldsymbol{s})}{Res_1(\boldsymbol{s})} = Y_1(\boldsymbol{s}) + \frac{Res_2(\boldsymbol{s})}{Res_1(\boldsymbol{s})}, \tag{31}$$

$$\frac{Res_1(\boldsymbol{s})}{Res_2(\boldsymbol{s})} = Z_2(\boldsymbol{s}) + \frac{Res_3(\boldsymbol{s})}{Res_2(\boldsymbol{s})}. \tag{32}$$

The condition for performing the next polynomial division is the positive real residual function after the current division. If the residual function Res_x is negative, then the impedance rational function cannot be assembled from the passive circuit elements in the Cauer passive network model form. On the other hand, negative resistors in the mathematical circuit model can be considered because this model can be used for computer simulation only. If the above polynomials division steps are applied, then the division results can be written into the following continuous fraction expansion

$$Z(\boldsymbol{s}) = Z_1(\boldsymbol{s}) + \cfrac{1}{Y_1(\boldsymbol{s}) + \cfrac{1}{Z_2(\boldsymbol{s}) + \cdots}}. \tag{33}$$

This ladder equation according to [45] has passive network realizations called first and second Cauer canonical forms which are shown in Fig. 19.

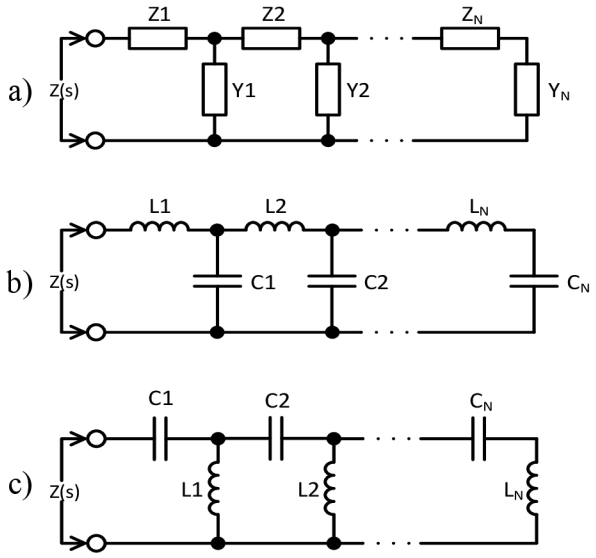


Fig. 19: a) The general Cauer passive network impedance model, b) the first Cauer, and c) the second Cauer canonical form [28].

From a practical point of view, it must be noted that all measured impedance function elements are unknown except the one element that is always presented in the measurement setup. This element is an RF input coupling capacitor that creates the one impedance pole at the beginning of the ***s***-plane. The first serial capacitor C_C of the synthesized passive network is the coupling capacitor, and its capacity value is used as the reference value for the calculation of other circuit model elements [28]. This coupling capacitor capacity can be measured by an electronic impedance meter like an LCR meter with four terminal-pair definitions [46]. Fig. 20 shows a realization example of measured impedance function with lossy elements.

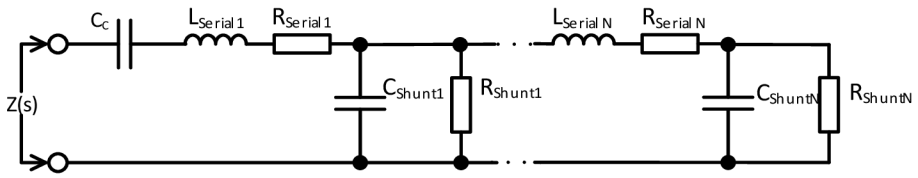


Fig. 20: A passive circuit network model example of the proposed element-by-element extraction method.

For the calculation of other circuit model elements, the impedance norm coefficient k_Z is used. This coefficient is calculated from the measured coupling capacitor capacity and the first serial capacitor capacity of the synthesized circuit model as

$$k_Z = \frac{C_C}{c_{serial1}}, \tag{34}$$

where k_Z is the impedance norm coefficient, C_C is the coupling capacitor capacity and $c_{serial1}$ is the first serial capacitor value of the synthesized circuit model. The real values of synthesized circuit model elements are calculated by the following equations

$$L_x = \frac{l_x}{k_Z}, \tag{35}$$

$$C_x = k_Z c_x, \tag{36}$$

$$R_x = \frac{r_x}{k_Z}, \tag{37}$$

where the L_x, C_x, R_x are real values of inductors, capacitors, and resistors, and the l_x, c_x, r_x are normalized values of inductors, capacitors, and resistors from the synthesized circuit model with the impedance norm coefficient k_Z [28].

3.2.2. Accuracy Check of the Passive Circuit Network Model Synthesis

An ideal passive circuit model with three impedance resonances has been chosen as a reference circuit model for verification of the proposed synthesis method, as described in [28]. The reference circuit model is shown in Fig. 21.

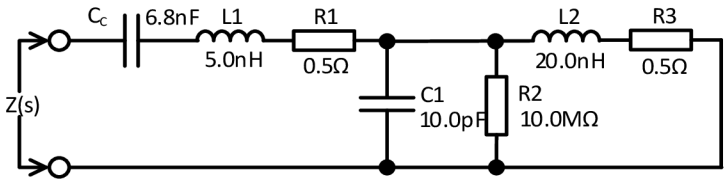


Fig. 21: The reference passive circuit model for the impedance synthesis method verification [28].

Values of resonance frequencies and resonance bandwidths of the reference circuit model are shown in Tab. 2, where f_{ser_res} is serial resonance frequency, B_{ser} is serial resonance bandwidth, f_{par_res} is parallel resonance frequency and B_{par} is parallel resonance bandwidth. These values were obtained by an AC simulation of the reference model in the SPICE circuit simulator.

Tab. 2: The reference passive circuit model impedance resonance frequencies and bandwidths (rounded to five decimal places) [28].

f_{ser_res} [MHz]	B_{ser} [MHz]	f_{par_res} [MHz]	B_{par} [MHz]
12.20064	6.37313	355.87286	4.01481
796.17750	13.56498	Not exist	Not exist

After applying the proposed synthesis method, the synthesized circuit model has the same circuit topology as the reference circuit model from Fig. 21. The extracted circuit elements values and their relative error ($\delta_{Synthesis}$) are shown in Tab. 3.

Tab. 3: The reference passive circuit model synthesis results (rounded to three decimal places) [28].

Model element	Reference value	Synthesis result	$\delta_{Synthesis}$ [%]
C1	6.800 nF	6.800 nF	0.000
L1	5.000 nH	4.999 nH	-0.020
R1	0.500 Ω	0.500 Ω	0.000
C2	10.000 pF	9.999 pF	-0.010
R2	10.000 MΩ	0.678 MΩ	-93.220
L2	20.000 nH	20.002 nH	0.010
R3	0.500 Ω	0.502 Ω	0.400

The proposed synthesis method shows very good results but there is an issue with the high value of shunt resistors because the proposed extraction method has high sensitivity on parallel resonance bandwidth value. The high shunt resistor value causes very narrowband parallel resonance bandwidth which cannot be easily precisely determined. The proposed extraction method's basic sensitivity analysis results on resonance bandwidth changes are shown in Tab. 4.

Tab. 4: The basic sensitivity of the proposed extraction method on resonance bandwidths values (rounded to one decimal place) [28].

ΔB_{ser_res} [Hz]	ΔR_{Serial} [Ω]	ΔB_{par_res} [Hz]	ΔR_{Shunt} [Ω]
1.0	$0.1 \cdot 10^{-6}$	1.0	21.7
10.0	$0.4 \cdot 10^{-6}$	10.0	217.3

As Tab. 4 refers, the change of parallel bandwidth resonance by about 1 Hz caused the change of shunt resistance of about 21.7 Ω, but the same change of serial resonance caused only a 0.1 μΩ change of the serial resistor. Moreover, the bandwidth change of about 10 Hz brings a change of the shunt resistor of about 217.3 Ω, but the change of the serial resistor is still small, about 0.4 μΩ. The high error of parallel resonance value estimation brings the high error of the shunt resistor value calculation. The impedance characteristics vs. frequency as the AC simulation results of the reference and synthesized circuit model from the SPICE circuit simulator are shown in Fig. 22 and Fig. 23.

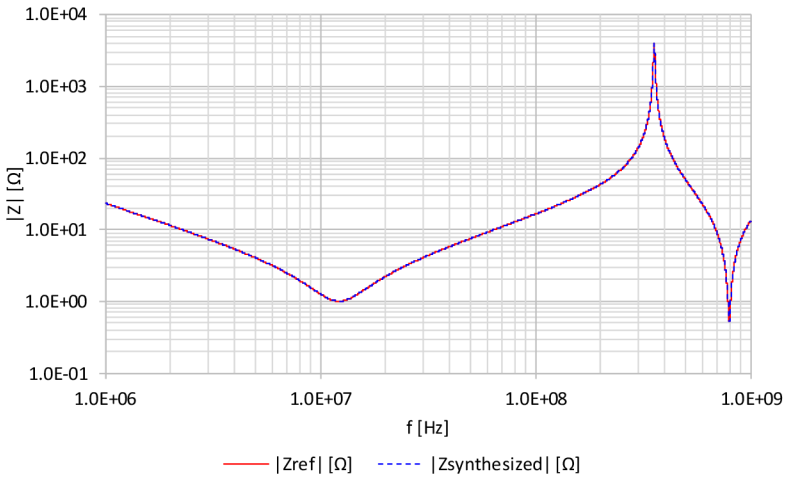


Fig. 22: The impedance magnitude characteristics of reference and synthesized circuit model [28].

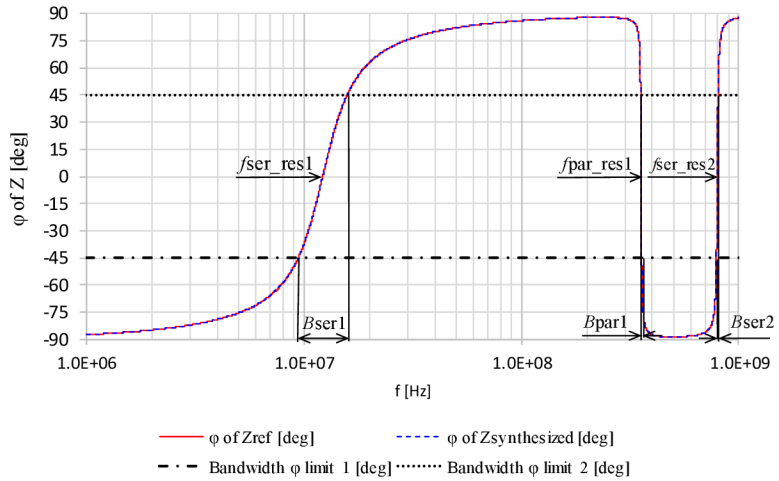


Fig. 23: The impedance phase characteristics of reference and synthesized circuit model [28].

3.2.3. Bias-Tee High-Frequency Circuit Model

The bias-tee is a three-port EMC filter that combines the DC and AC (high frequency) signal path into one path with the DC and AC part of the signal. The target of this device is to isolate the coupling path or tested pin from the low impedance of the DC power supply. Otherwise, the bias-tee can be used for AC signal part minimalization for DC signal measurement as a protection of a voltmeter. The bias-tee is often used in EMC susceptibility setup which is used for the DPI method measurement at the IC level according to IEC 62132-4 [26]. The real example of the bias-tee, its photo, its schematic diagram, and its high-frequency impedance measurement setup diagram are shown in Fig. 24.

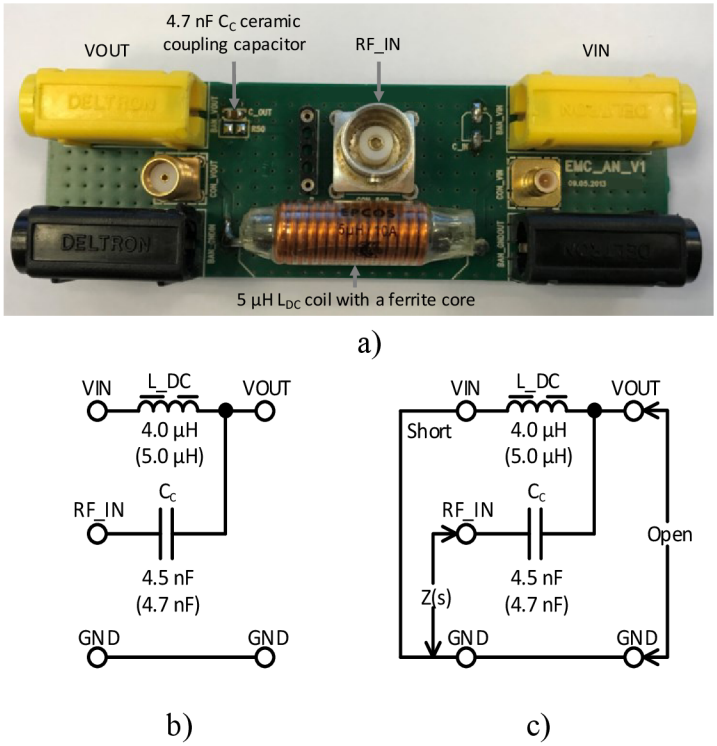


Fig. 24: The bias-tee a) photo, b) its schematic diagram, and c) its impedance measurement setup schematic diagram [28].

The 4.7 nF coupling capacitor was selected according to the RF DPI immunity test method, which is used for the EMS test at the IC level [26]. The bias-tee high-frequency impedance was measured at high-frequency input (RF_IN) for the case when the DC power supply input (VIN) connector is short to ground with very low impedance (by the very short conductor). Then the resonance frequencies and band-widths were extracted from the measured impedance characteristic vs. frequency. The synthesized passive circuit model from these parameters is shown in Fig. 25.

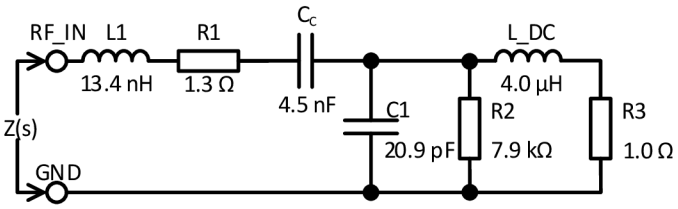


Fig. 25: The synthesized passive circuit model of the bias-tee [28].

Tab. 5: The RF_IN bias-tee impedance resonance frequencies and bandwidths with the V_IN shorted to the ground (rounded to five decimal places) [28].

f_{ser_res} [MHz]	B_{ser} [MHz]	f_{par_res} [MHz]	B_{par} [MHz]
1.17968	0.09662	17.38654	1.01143
302.02947	16.14057	Not considered	Not considered

Tab. 5 shows values of extracted resonance frequencies and resonance bandwidths from the measured impedance characteristic of the bias-tee, where f_{ser_res} is serial resonance frequency, B_{ser} is serial resonance bandwidth, f_{par_res} is parallel resonance frequency and B_{par} is parallel resonance bandwidth. The synthesized circuit model element's values and description are summarized in the following Tab. 6.

Tab. 6: The synthesized circuit model elements of the bias-tee (rounded to one decimal place) [28].

Model element	Value	Description
L1	13.4 nH	The total inductance of the BNC connector, PCB track, and coupling capacitor.
R1	1.3 Ω	The total DC resistance of the BNC connector, PCB track, and coupling capacitor.
C_C	4.5 nF	The coupling capacitor capacity (verified by the LCR meter).
C1	20.9 pF	The inter-turn capacity of the DC coil with the PCB track capacity (to the ground).
R2	7.9 kΩ	The ferrite core loss resistance of DC coil.
L_DC	4.0 μH	The inductance of the DC coil (verified by the LCR meter).
R3	1.0 Ω	The winding resistance of the DC coil and short to the ground.

The impedance characteristics vs. frequency as the impedance measurement and AC simulation results of the bias-tee real circuit and its synthesized circuit model from the SPICE circuit simulator are shown in Fig. 26 and Fig. 27.

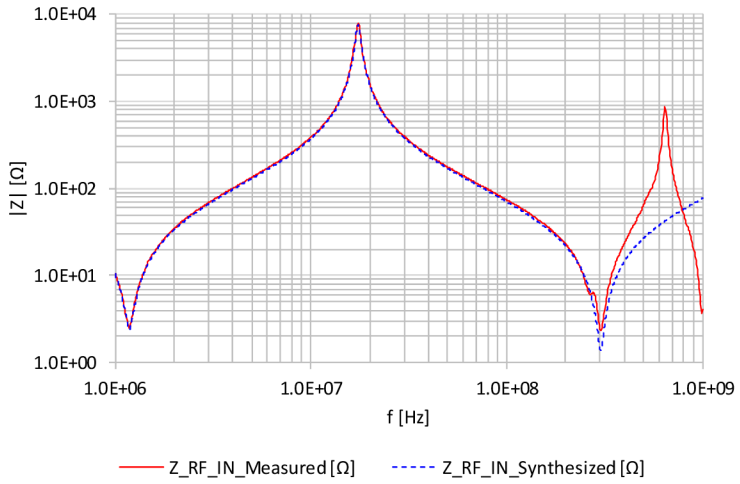


Fig. 26: The impedance magnitude characteristics of the measured bias-tee and its synthesized circuit model [28].

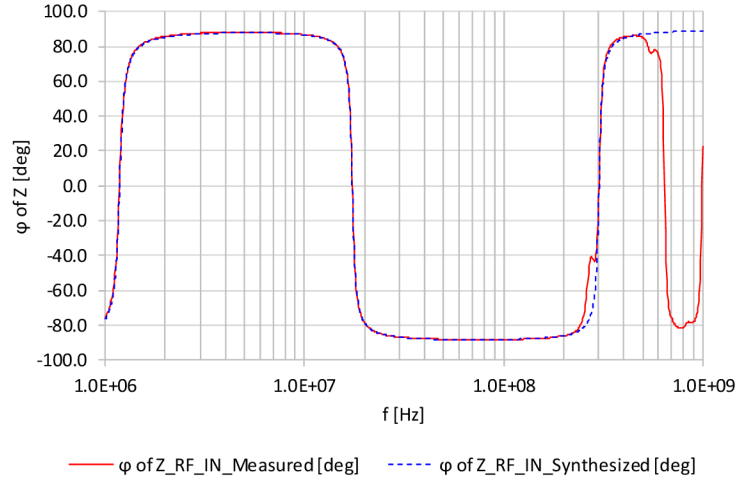


Fig. 27: The impedance phase characteristics of the measured bias-tee and its synthesized circuit model [28].

The bias-tee circuit model is built of frequency-independent elements and the simulated results show a very good correlation with measured results in the frequency range from 1 to 200 MHz. The synthesized circuit model is a simplified finite lumped approximation for distributed parameter circuit systems. Therefore, the correlation at last considered resonance frequency is poor. From the impedance characteristic, there is an apparent limitation of the proposed synthesis method. It is impossible to obtain all input parameters for the synthesis method when the resonances are very close to each other. The very close measured resonances are seen in Fig. 26 and Fig. 27 from 300 MHz approximately. But if a certain inaccuracy of the model is considered, a simple approximation can be used for the resonance bandwidth determination as described in the following equations.

$$f_1 = \frac{f_0^2}{f_2}, \tag{38}$$

$$B = f_2 - f_1, \tag{39}$$

where f_0, f_1, and f_2 are the resonance frequency, first and second frequencies which determine B resonance bandwidth. For this approximation, it is necessary to know at least one boundary and resonant frequencies of considered resonance bandwidth [47]. The extracted circuit model of the bias-tee can be used for high-frequency immunity SPICE simulation of dedicated IC.

This passive network synthesis can be used for the estimation of the load impedance model of IC pins, for a more accurate passive circuit simulation model, for the estimation of the impedance model of PCB tracks with passive circuit components, etc. The proposed synthesis method is accurate, and fast and does not need many special measurements for the input parameters of this method. However, there are some limitations as well as the accuracy of the shunt resistor (conductivity) calculation due to high sensitivity on correct parallel resonance bandwidth value and usability on circuits with clear resonances. On the other hand, this method can be improved for other possible circuit model variations.

For all presented passive network circuit model calculations in this chapter 3.2 an impedance network synthesizer software was used. The software uses all methods corresponding with the element-by-element extraction method which was described in this chapter 3.2. A graphical user interface of the impedance passive network synthesizer software which was written in C# for fast passive circuit elements calculation is shown in Fig. 28.

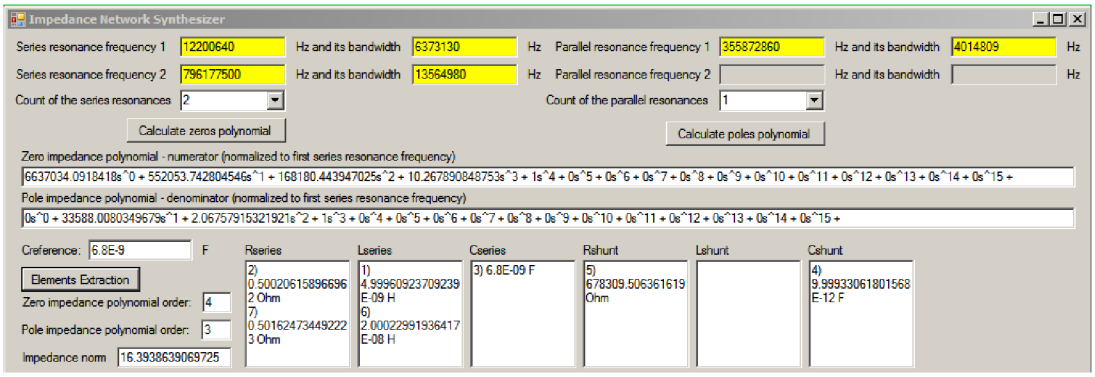


Fig. 28: The passive network impedance synthesizer software using the proposed element-by-element extraction method (results are rounded to appropriate decimal places) [28].

The described passive network model synthesis method and the achieved results were published in the "A Passive Network Synthesis from Two-Terminal Measured Impedance Characteristic" paper [28].

4 PROPOSED VOLTAGE REFERENCES

Detailed study of the existing EMC improved Brokaw bandgap voltage reference and systematic EMI susceptibility analyses of voltage reference blocks are presented in the following chapters 4.1 and 4.2. Chapter 4.3 discusses the theoretical possibilities of power supply EMI susceptibility reduction. Systematic analyses of commonly used voltage reference blocks are outlined in chapters 4.4 and 4.5. Based on the outcome of these analyses, chapter 4.6 presents the new proposed EMC robust voltage reference with the proposed new EMC robust design methodology.

4.1. Existing EMC Improved Brokaw Voltage Reference

The real design of the low power voltage reference carries its pitfalls corresponding with the fact that all circuit components are on the same substrate of the IC. This means that it is necessary to take into account not only the basic functionality but also the parasitic structures of individual integrated circuit components. For example, a simplified cross-section of a vertical NPN bipolar junction transistor used in the bandgap core in onsemi I3T50 technology (350 nm automotive high voltage BCD – Bipolar, CMOS, and DMOS technology) is shown in Fig. 29.

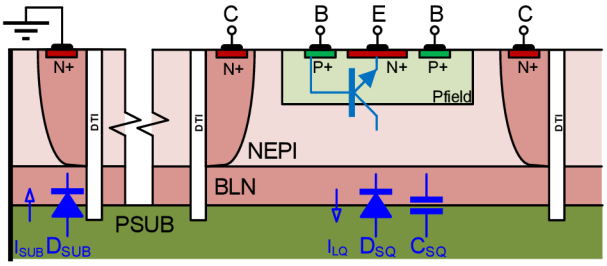


Fig. 29: Simplified cross-section of I3T50 vertical NPN BJT in the IC (NEPI is an N-type epitaxial layer, BLN is an N-type buried layer, PSUB is a P-type substrate, and DTI is deep trench isolation) [48].

The collector of such a vertical NPN transistor is isolated from the substrate by a reverse polarized junction diode D_{SQ} (D_{SQx} in Fig. 30). Leakage current of this substrate diode influences the accuracy of the bandgap reference, especially when working with small currents in the bandgap core at high temperatures. When counting with diode leakage I_{LQ}, the bandgap output voltage is

$$V_{ref} = V_{BE2} + \left(1 + \frac{I_{R1} - NI_{LQ}}{I_{R2} - I_{LQ}}\right)\frac{R4}{R3} V_T \, ln\left(\frac{I_{R2} - I_{LQ}}{I_{R1} - NI_{LQ}} N\right). \quad (40)$$

The diode leakage can be compensated by adding $N-1$ dummy bipolar transistors in parallel to Q2 similar to [49]. The idea of this compensation technique is to keep the stable current ratio as described by the following equations

$$V_{ref} = V_{BE2} + \left[1 + \frac{I_{R1} - NI_{LQ}}{I_{R2} - I_{LQ} - (N-1)I_{LQ}}\right]\frac{R4}{R3} V_T \, ln\left[\frac{I_{R2} - I_{LQ} - (N-1)I_{LQ}}{I_{R1} - NI_{LQ}} N\right], \quad (41)$$

$$V_{ref} = V_{BE2} + \left(1 + \frac{I_{R1} - NI_{LQ}}{I_{R2} - NI_{LQ}}\right)\frac{R4}{R3} V_T \, ln\left(\frac{I_{R2} - NI_{LQ}}{I_{R1} - NI_{LQ}} N\right). \quad (42)$$

In the classical structure with $N = 8$, this means adding 7 dummy NPN transistors. With 9 (1 + 8) units and 7 dummy leakage compensation units, it is more difficult to achieve perfect symmetry, and the area is significantly increased. To optimize area and achieve a perfectly symmetrical layout of the bipolar core, the emitter area ratio N was chosen 2 and the collector currents I_{C1} and I_{C2} were chosen in a ratio of 2:3 (Fig. 30). This ratio requires the addition of only two dummy NPN transistors to compensate the leakage currents. In layout, the bipolar transistors can be placed symmetrically in a single row as shown in Fig. 30.

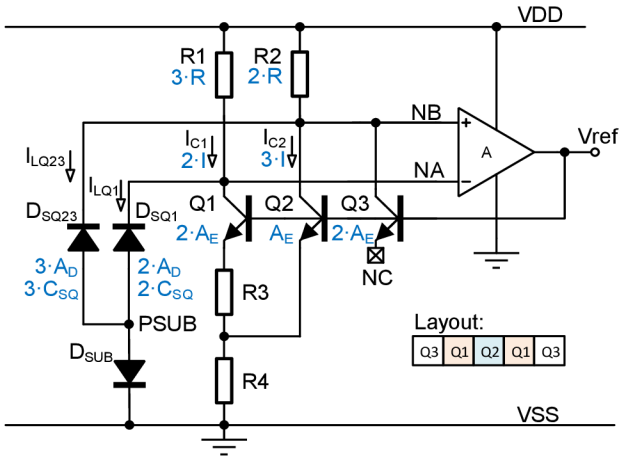


Fig. 30: Brokaw bandgap with bipolar transistor leakage current compensation.

The reference voltage of the proposed Brokaw configuration is as follows

$$V_{ref} = V_{BE2} + \left(1 + \frac{2}{3}\right)\frac{R4}{R3} V_T \, ln\left(\frac{3}{2} 2\right). \quad (43)$$

The consequence of adding dummy bipolar transistors for leakage compensation is also balancing the C_{SQx} capacities caused by the parasitic substrate diodes. These capacitances allow entry of undesired HF disturbances from the substrate to Q1, Q2, and Q3 collectors and thus also into inputs of the OPA. When using the same currents I_{C1}, and I_{C2}, in the classical structure with $N = 8$ and adding seven dummy transistors (Fig. 2 with 7 additional dummy transistors), then the number of collectors on both branches is the same and the substrate noise coupling is symmetrical as well.

When using the current ratio I_{C1}:I_{C2} = 2:3 and the ratio of bipolar transistors including dummy transistors A_{E1}:A_{E23} = 2:3, and neglecting input capacitance of the OPA, the time constant on node NA is $R1 \cdot C_{SQ1} = 6 \cdot R \cdot C_{SQ}$ and the time constant on node NB is $R2 \cdot C_{SQ23} = 6 \cdot R \cdot C_{SQ}$ (C_{SQ} is parasitic collector capacitance towards substrate of one bipolar transistor). It means both time constants are the same and disturbances are coupled to the OPA input as common mode disturbances, which can be suppressed by the OPA.

To decrease the amplitude of the disturbances at the OPA input, filtering capacitors C_A and C_B (Fig. 32) are used with a capacity ratio equal to the NPN BJTs ratio of 2:3, which means that $C_A = 2C$, $C_B = 3C$. The parasitic capacitances C_{SQ1} and C_{SQ23} with filtering capacitances C_A and C_B create symmetrical capacitive voltage dividers, which decrease the coupling of disturbances from the substrate to the input of the OPA and minimize differential disturbances and suppress the influence of non-symmetricity caused by input capacitances of the OPA. The value of the filtering capacitors is chosen to be bigger than the value of the parasitic capacitances ($C \approx 1$ pF). Another advantage of using C_A and C_B capacitors is to minimize the coupling of disturbances from the VDD supply net. In this case, $R1$ and $R2$ resistors together with C_A and C_B capacitors and parasitic substrate capacitors of bipolar transistors form first-order low-pass filters with the same time constants τ_A and τ_B.

$$\tau_A = R1\left(C_A + C_{SQ1}\right) = 6R\left(C + C_{SQ}\right), \tag{44}$$

$$\tau_B = R2\left(C_B + C_{SQ23}\right) = 6R\left(C + C_{SQ}\right). \tag{45}$$

To extend a range of common mode disturbances on NA and NB nodes without voltage clamping, common mode regulating transistors M1 and M2 were added into the voltage reference core. These transistors regulate voltage on NA and NB nodes one V_{GS} below supply voltage VDD. These transistors are included in Fig. 32 and their sizes are corresponding to their currents. Another important aspect of high-frequency disturbance coupling to the Brokaw bandgap core is polysilicon resistors and their parasitic capacitance to a diffusion below these resistors [20], [21]. A simplified cross-section of one finger of polysilicon resistors laying on NWELL and PWELL is shown in Fig. 31.

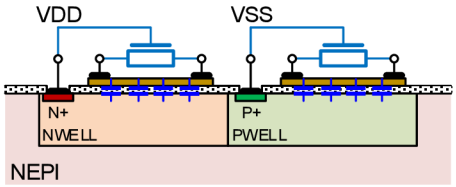


Fig. 31: Simplified cross-section of polysilicon resistors.

The advantage of using I3T50 technology is the possibility to choose if the matched resistors will be placed on NWELL or PWELL and to isolate these wells from the substrate. Resistors $R1$ and $R2$ were placed over NWELL at VDD and resistors $R3$ and $R4$ were placed over PWELL at VSS. The circuit schematic of the final low power and wide temperature range Brokaw voltage reference with described improvements against EMI is shown in Fig. 32.

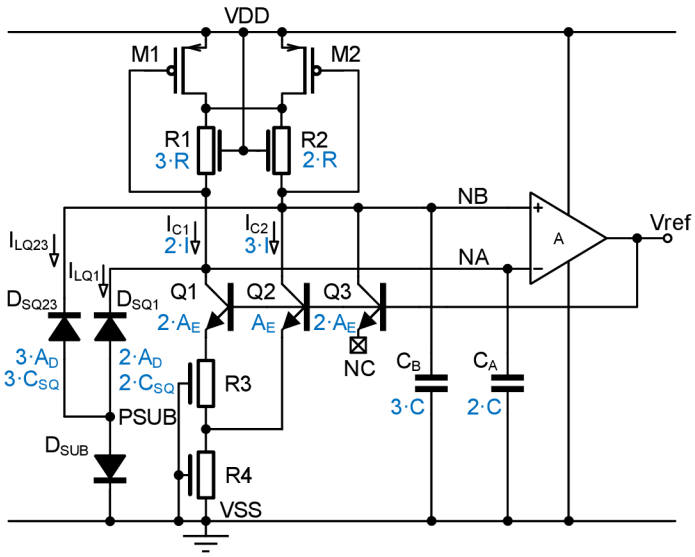


Fig. 32: Final low power and wide temperature range Brokaw bandgap with bipolar transistor leakage current compensation.

To estimate the acceptable maximum EMI disturbance voltage amplitude at VDD, it is necessary to determine a minimum VDD supply voltage from an acceptable voltage dynamic range in a circuit critical part. In this case, the critical part is the bandgap core. The minimum VDD supply voltage can be estimated if it is assumed that V_{ref} is 1.2 V, to keep bipolar transistors in the linear region ($V_{\mathrm{CBQ123min}}$ can be greater or equal to 0 V) and PMOS transistors M1 and M2 in saturation (V_{GSM1min} and V_{GSM2min} can be chosen 0.9 V). This gives a minimum supply voltage of 2.1 V. The amplitude of disturbances superimposed on a 3.0 V DC supply can be approximately 0.9 V. The theoretical voltage room of the voltage reference core for 1 MHz EMI signal on the VDD supply net is shown in Fig. 33, where V_CBQx is a collector-base voltage of the BJTs and V_CQx is the collector of the BJTs to VSS voltage which also represents input common mode voltage of the regulating OPA.

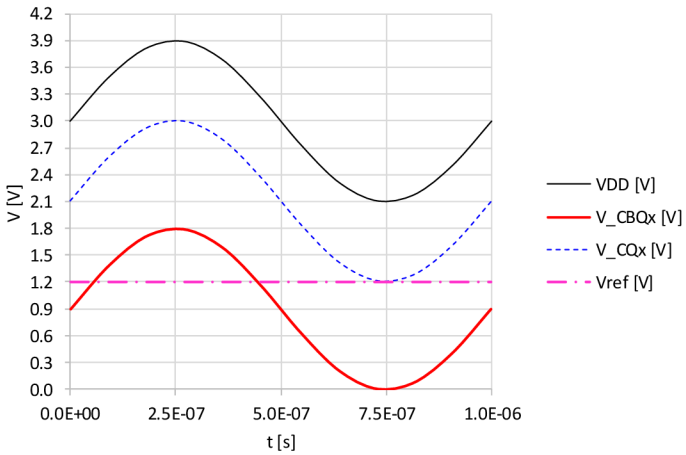


Fig. 33: The voltage room estimation for maximum harmonic VDD supply disturbance.

4.2. EMI Susceptibility Analysis of the Voltage Reference

In the previous chapter, the existing low-power Brokaw bandgap voltage reference design and recommendations on how to improve the bandgap, and EMI robustness are presented and implemented. The simulation analysis of these modifications is given in this chapter.

4.2.1. EMI Susceptibility of the Voltage Reference Core

The heart of any reference is its reference element or reference core. Whether it is a Zener diode or a bandgap cell the final result is sometimes only as good as the reference element [50]. To verify the performance of the conventional bandgap core, basic EMI susceptibility transient simulations were performed with an ideal OPA using the following configurations of this bandgap core:

a) Without leakage compensation bipolar transistor Q3, filtration capacitors C_A and C_B, and common mode transistors M1 and M2.

b) With leakage compensation bipolar transistor Q3 (see chapter 4.1).

c) With leakage compensation bipolar transistor Q3 and filtration capacitors C_A and C_B (see chapter 4.1).

d) With leakage compensation bipolar transistor Q3, filtration capacitors C_A and C_B, and common mode transistors M1 and M2 (see chapter 4.1).

The ideal OPA has a 100 dB open loop gain with a dominant pole (cutoff frequency) at 0.14 Hz which is defined by the R_{DP} resistor and C_{DP} capacitor. The output of the ideal OPA is created by the NMOS transistor (M10 in the following figures) as a source follower with an R_{Load} resistor from the original design. The bandgap voltage reference core configurations are shown in the following figures: Fig. 34, Fig. 35, Fig. 36, and Fig. 37.

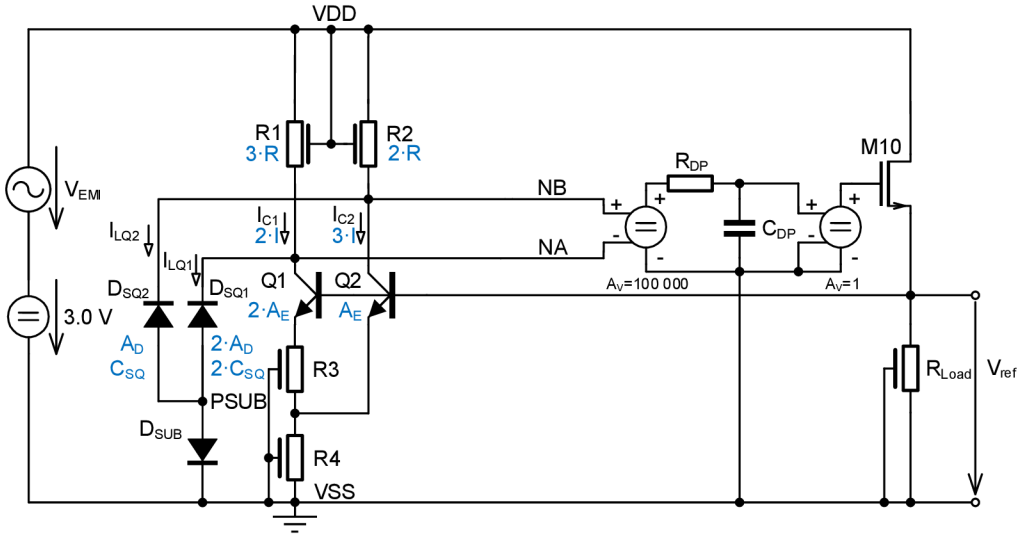


Fig. 34: Configuration a), the basic bandgap core without leakage compensation.

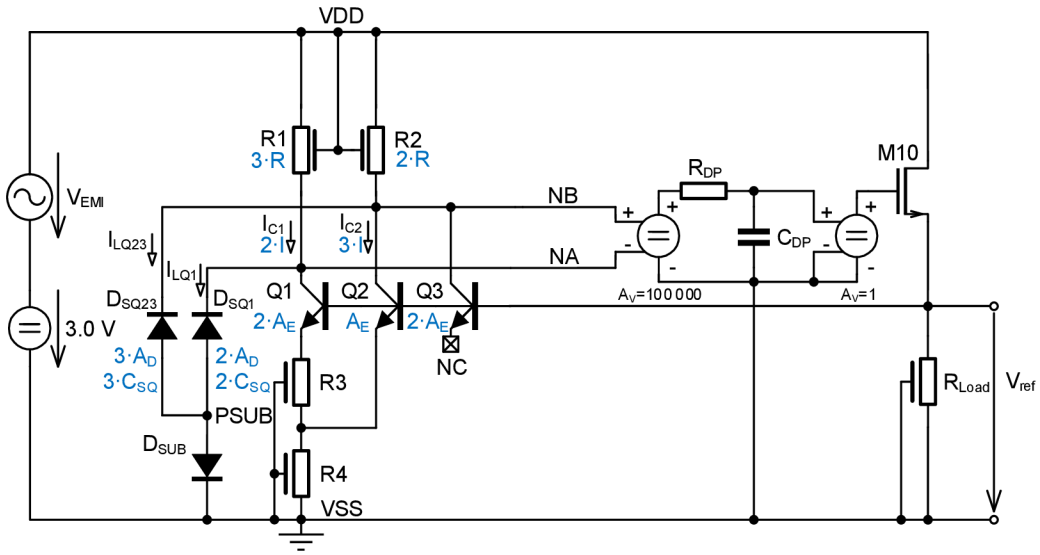


Fig. 35: Configuration b), the basic bandgap core with leakage compensation (additional transistor Q3, for more information, see chapter 4.1).

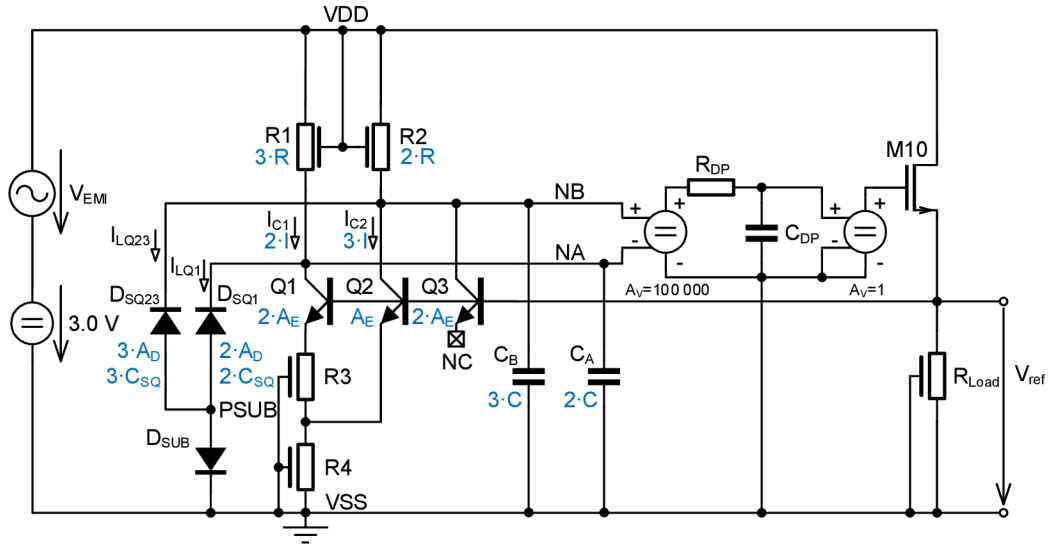


Fig. 36: Configuration c), the basic bandgap core with leakage compensation (Q3) and filtration capacitors C_A and C_B (for more information see chapter 4.1).

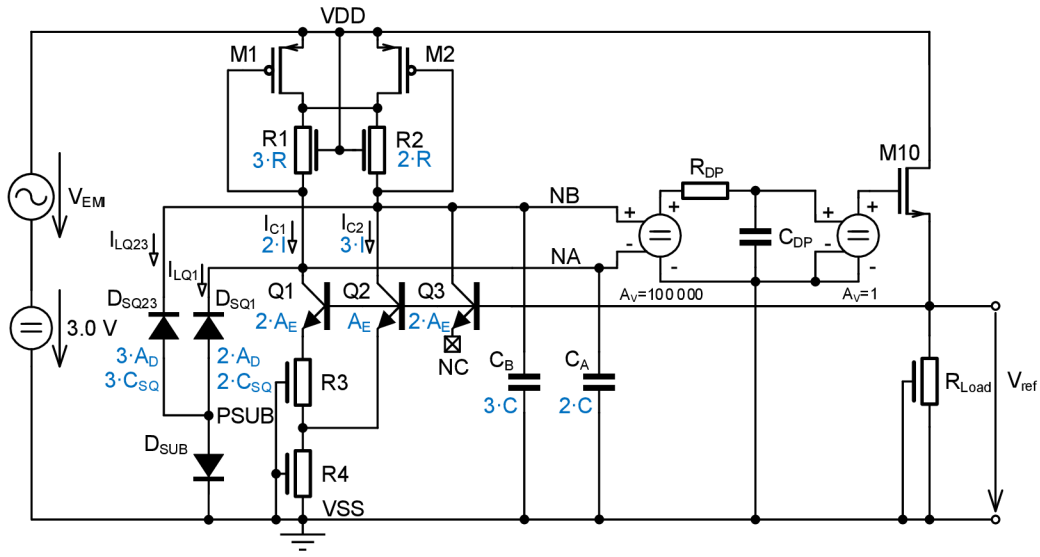
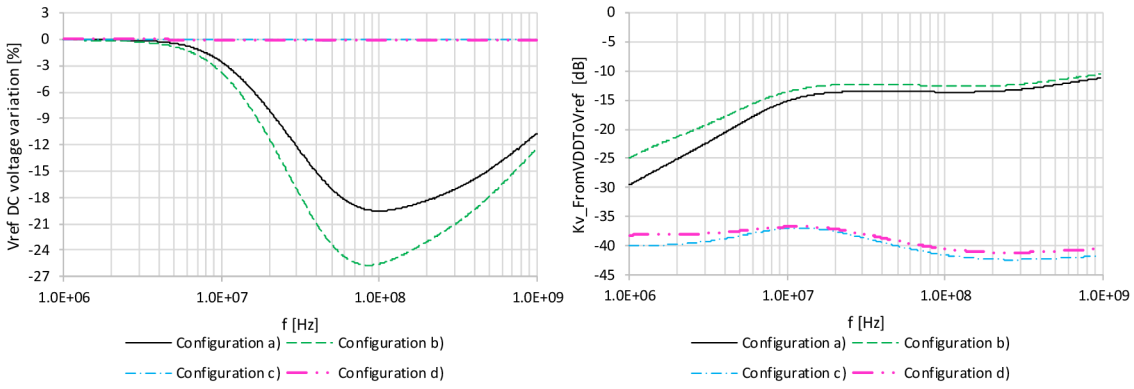


Fig. 37: Configuration d), the basic bandgap core with leakage compensation (Q3), filtration capacitors C_A and C_B, and common mode regulator (M1 and M2, for more information, see chapter 4.1).

Transient simulations were performed with 3 V VDD supply voltage. The HF EMI signal was simulated by a V_{EMI} sinusoidal voltage source with variable frequency and chosen 0.632 V amplitude which is large in comparison with the 3 V supply voltage. The 0.632 V amplitude of the V_{EMI} source is approximately equal to 1 mW (0 dBm) power of the DPI method according to IEC 62132-4 [26] when driving high impedance load [27] as the worst-case situation. The V_{EMI} voltage of the EMI sinusoidal voltage source is calculated from the following equation

$$V_{EMI} = 2\sqrt{2P_{For}R_{RF}}. \tag{46}$$

The EMI susceptibility simulations were performed as an envelope simulation with fifteen harmonics in the Cadence Spectre RF® simulator with postprocessing of the V_{ref} average and the first harmonic voltage values after circuit settling time. The basic VDD EMI susceptibility simulation results of all described bandgap core configurations are shown in Fig. 38.



a) b)

Fig. 38: Basic VDD EMI susceptibility of the bandgap core various configurations: a) V_{ref} DC voltage variations and b) AC voltage transmissions with $V_{DD\_EMIpeak}$ of 0.632 V.

From these results, it is evident that adding a leakage compensation transistor (Q3 in Fig. 35, Configuration b)) causes higher EMI susceptibility than the basic voltage reference core. It is due to an impedance change in the voltage reference core that causes a higher EMI differential signal which is rectified by bipolar transistors in the bandgap core. But adding filtration capacitors (C_A and C_B in Fig. 36, Configuration c)) for the effective symmetrical filtration EMI signal on both branches in the bandgap core has proven its essence to improve bandgap core EMI robustness. Even more, the common mode regulator (M1 and M2 in Fig. 37, final Configuration d)) doesn't worsen significantly the VDD EMI susceptibility of the bandgap core. The details of VDD EMI susceptibility simulation results for DC reference voltage variation of bandgap core configurations c) and d) are shown in Fig. 39, where configuration d) is the final configuration implemented in the test chip.

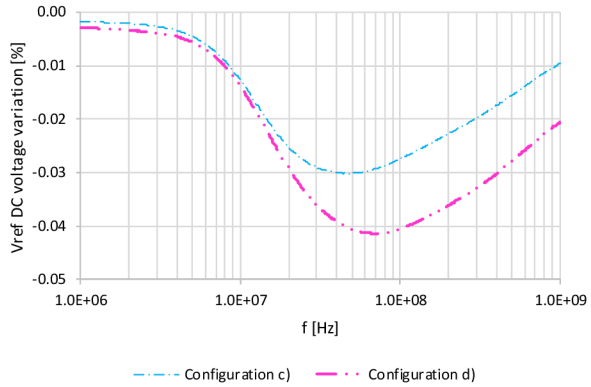


Fig. 39: Detail of basic VDD EMI susceptibility: V_{ref} DC voltage variations for the bandgap core configurations c) and d) with $V_{DD\_EMIpeak}$ of 0.632 V.

The basic bandgap core P-substrate EMI susceptibility simulations were performed with a small change in simulation schematics (Fig. 34, Fig. 35, Fig. 36, and Fig. 37) which is shown in Fig. 40.

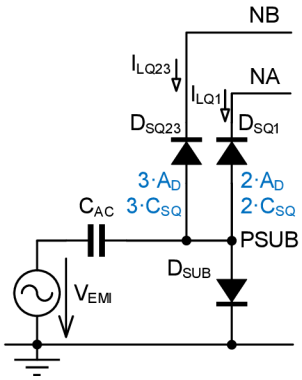
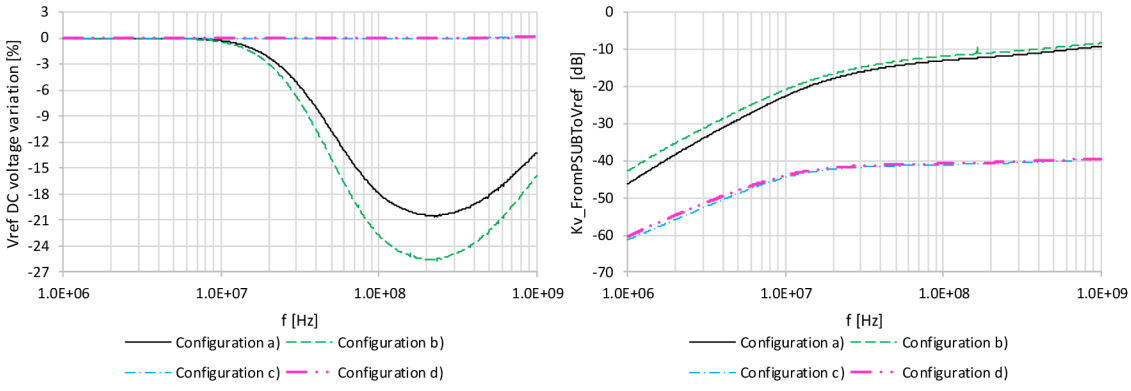


Fig. 40: Detail of simulation schematics of the bandgap core susceptibility to EMI coming from the IC substrate (in the figure is part of the configuration b)).

The change is that the EMI is coupled via a coupling capacitor C_{AC} to the PSUB node simulating the P-substrate of the bandgap core. The capacity of the coupling capacitor was chosen 1 nF as a compromise between the PSUB node capacitive load (circuit settling time) and signal transfer to this node. This coupling capacitor has a 159.2 Ω impedance according to equation (47) at the beginning frequency 1 MHz of the EMI analysis, which can be neglected relative to the PSUB node impedance.

$$|Z_{C_{AC}}| = \frac{1}{2\pi f C_{AC}}. \tag{47}$$

The basic bandgap core substrate EMI susceptibility simulation results of all described bandgap core configurations are shown in Fig. 41.



a) b)

Fig. 41: Basic PSUB (P-substrate) EMI susceptibility of the bandgap core various configurations: a) V_{ref} DC voltage variations and b) AC voltage transmissions with $V_{PSUB\_EMIpeak}$ of 0.632 V.

From these results, it is evident that adding a leakage compensation transistor (Q3 in Fig. 35, Configuration b)) causes higher substrate EMI susceptibility than the basic voltage reference core. It is due to the EMI coupling change in the voltage reference core that causes a higher EMI differential signal which is rectified by bipolar transistors in the bandgap core. But adding filtration capacitors (C_A and C_B in Fig. 36, Configuration c)) for the effective symmetrical filtration EMI signal on both branches in the bandgap core has proven its benefit to improve bandgap core EMI sensitivity. Even more, the common mode regulator (M1 and M2 in Fig. 37, final Configuration d)) doesn't degrade significantly the substrate EMI susceptibility of the bandgap core. The detail of the IC substrate EMI susceptibility simulation results for DC reference voltage variation of bandgap core configurations c) and d) are shown in Fig. 42, where configuration d) is the final configuration implemented in the test chip.

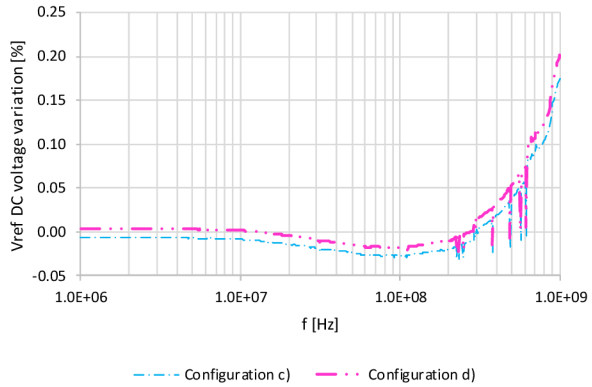


Fig. 42: Detail of basic PSUB (P-substrate) EMI susceptibility: V_{ref} DC voltage variations for the bandgap core configurations c) and d) with $V_{PSUB\_EMIpeak}$ of 0.632 V.

Through these simulations was verified that the fully symmetrical filtration method with the same time constants and the capacity ratio of both branches in the bandgap core is valid. The summary worst-case results of the EMI susceptibility simulations for all bandgap core configurations are presented in the following Tab. 7.

Tab. 7: The bandgap core overall EMI susceptibility simulation results.

Parameter	Conf. a)	Conf. b)	Conf. c)	Conf. d)
V_{ref} DC variation for VDD EMI [%]	max. 19.5	max. 26.0	< 0.1	< 0.1
V_{ref} DC variation for PSUB EMI [%]	max. 18.0	max. 26.0	< 0.2	max. 0.2
V_{ref} ripple rejection for VDD EMI [dB]	min. 11.0	min. 10.0	min. 37.0	min. 36.0
V_{ref} ripple rejection for PSUB EMI [dB]	min. 9.0	min. 8.0	min. 40.0	min. 39.0

4.2.2. EMI Susceptibility of the OPA

A used OPA is strongly impacting the EMI susceptibility of the complete bandgap voltage reference [11], [16]. From these literature sources, it can be formulated that if the OPA is fully symmetrical and the rectification effects are also symmetrical, then these effects will be suppressed. It is worth to note, that the symmetrical rectification is very hard to achieve.

The proposed one-stage folded cascode OPA with frequency compensation by a capacitor towards VSS (C_{DP} in Fig. 43 a)) and source follower output stage is used in the voltage reference, see Fig. 43 a). This OPA is designed to tolerate a high common mode input voltage range and keep all transistors in the desired operating region (strong inversion) when EMI disturbances create a common mode voltage shift in the bandgap core. For comparison EMI susceptibility of the folded cascode, a basic two stages Miller OPA, see Fig. 43 b), is designed with approximately the same open loop gain A_{OL} and unity-gain bandwidth GBW as the folded cascode OPA. Both types of circuit schematics of OPAs are shown in Fig. 43.

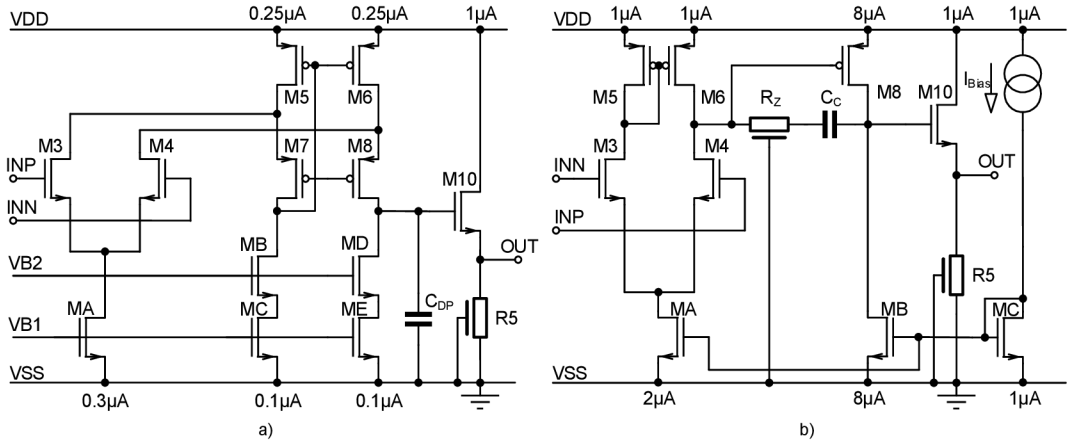


Fig. 43: The OPAs for Brokaw bandgap: a) folded cascode and b) basic Miller OPA.

Each of these OPAs was analyzed for small AC signal open loop characteristics. A simulation schematic is based on the general OPA simulation notes in [51]. The used open loop gain simulation schematic is shown in the following Fig. 44.

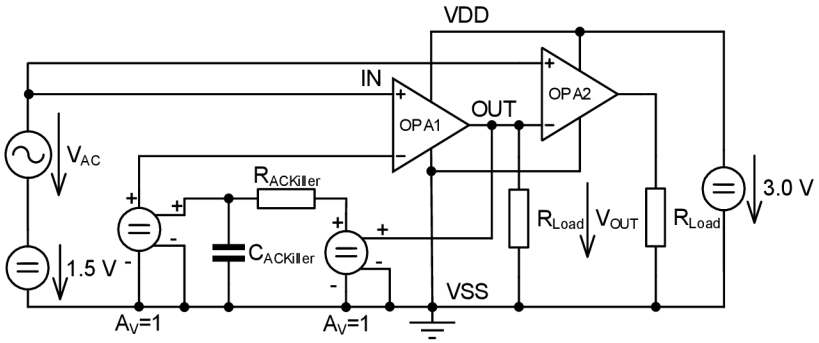


Fig. 44: The simulation schematic diagram for the OPA AC open loop gain analysis.

Both OPAs (OPA1 and OPA2) in the simulation schematic are identical. This circuit connection with an AC killer formed by two voltage-controlled voltage sources (VCVS) with $R_{ACKiller}$ resistor and $C_{ACKiller}$ capacitor in the negative feedback is used for simple operating point setting and input offset effect removal. The trick is that for the DC signal (0 Hz), the OPA1 works as a voltage follower with a small native offset caused by e.g. mismatches in current mirrors, and for the AC signal, the OPA1 works as a non-inverting amplifier with open feedback loop gain. The identical OPA2 with the same input amplifier operating point as OPA1 simulates a correct load of the analyzed OPA1. It must be noted that the $R_{ACKiller}C_{ACKiller}$ product shall be as large as possible, but very big value causes simulation problems with number range. For example, this time constant 10 seconds can be enough for simulation purpose [51]. The results of this simulation are shown in Fig. 45.

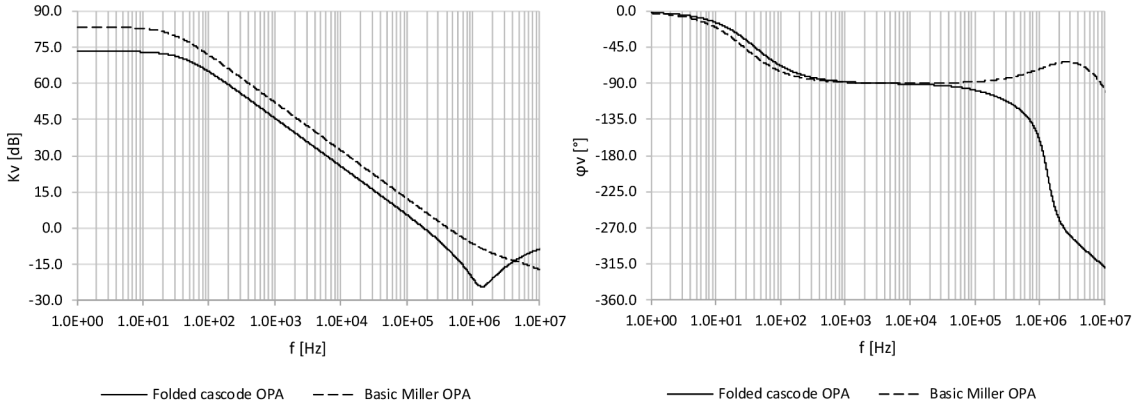


Fig. 45: The AC open loop characteristics of the folded cascode and the basic Miller OPA (the open loop gain magnitude and phase).

According to the simulation results, both OPAs are frequency-stable with a great open loop gain. Even the basic Miller OPA is a little bit frequency overcompensated, but for the comparison it is sufficient. Each of these OPAs was also analyzed for the input common-mode range (ICMR) according to [51]. The used ICMR simulation schematic is shown in the following Fig. 46.

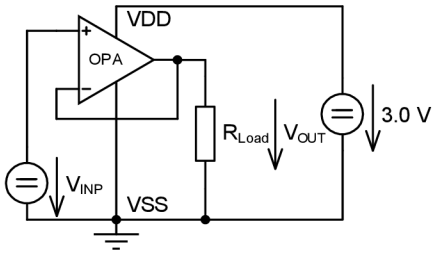


Fig. 46: The OPA ICMR simulation schematic [51].

The OPA is connected as the voltage follower and the input voltage V_{INP} is swept from zero to VDD supply voltage, which is 3 V in this case. The ICMR is defined as a linear part of the OPA output voltage [51]. The results of both OPAs ICMR simulations are shown in Fig. 47.

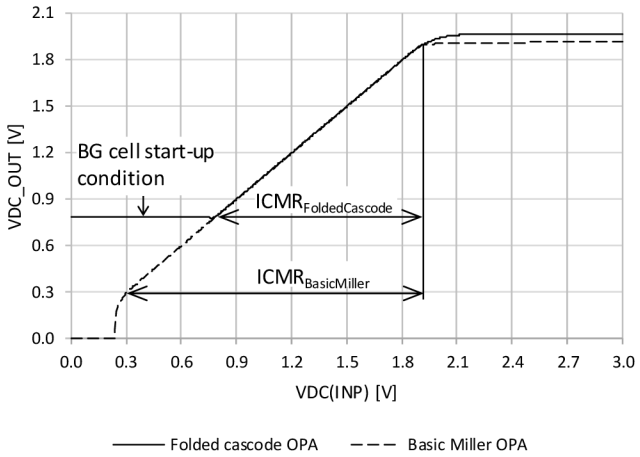


Fig. 47: The DC voltage ICMR of the folded cascode and the basic Miller OPA.

The ICMR simulation results show that the biasing circuit (not shown for simplicity) of the folded cascode OPA works as a bandgap start-up circuit. The bandgap core has two stable operating points, the zero and desired reference output voltage at the common base of bipolar transistors (e.g. Q1, Q2, and Q3 in Fig. 37). Therefore, there is the sophisticated start-up circuit, which makes a start-up condition as the lowest reference output voltage after switch-on power supply. This bandgap start-up condition is approximately 0.8 V output voltage when the input common-mode voltage is lower than 0.8 V. The basic Miller OPA doesn't have this start-up circuit and therefore its ICMR is larger than the ICMR of the folded cascode OPA. Even more, the differential input amplifier "switch-on" of the basic Miller OPA can be seen as an initial jump in ICMR sweep if the input voltage is greater than 0.3 V. Both OPA's output voltage saturation regions begin at about 1.9 V input common mode voltage. The output saturation voltage of the folded cascode OPA is about 1.96 V and 1.91 V for the basic Miller OPA.

The impact of the operational amplifier EMI susceptibility on the bandgap reference was verified by transient simulations where the proposed folded cascode OPA was compared with the basic Miller OPA (see Fig. 43). The first EMI simulation schematic is used for an OPA input differential EMI susceptibility analysis. The OPA works as a non-inverting voltage follower with resistive load R_{Load} as in the original bandgap reference. The simulation schematic is shown in Fig. 48.

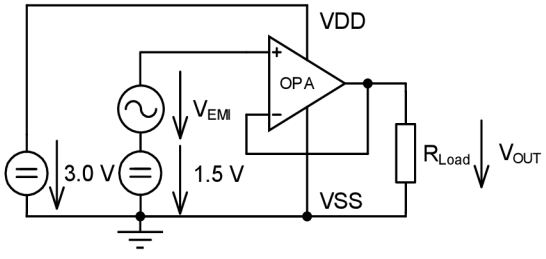


Fig. 48: The input differential EMI susceptibility simulation schematic of the OPA in voltage follower mode.

The second EMI simulation schematic is used for an OPA power supply EMI susceptibility analysis. The OPA works as a non-inverting voltage follower with resistive load R_{Load} as in the original bandgap reference. The simulation schematic is shown in Fig. 49.

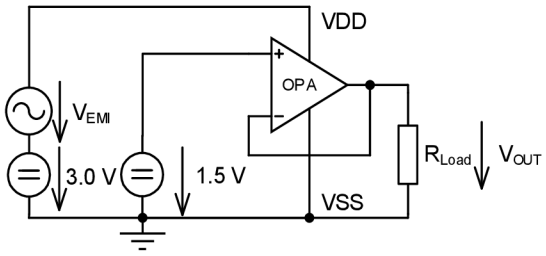


Fig. 49: The VDD EMI susceptibility simulation schematic of the OPA in voltage follower mode.

The third EMI simulation schematic is used for an OPA input common mode EMI susceptibility analysis. Fig. 50 shows a simple ideal simulation configuration with shorted OPA inputs for the common mode EMI susceptibility analysis. This configuration cannot be used because there is an input native voltage offset of the OPA causing an output voltage saturation (the output voltage is not in the linear region).

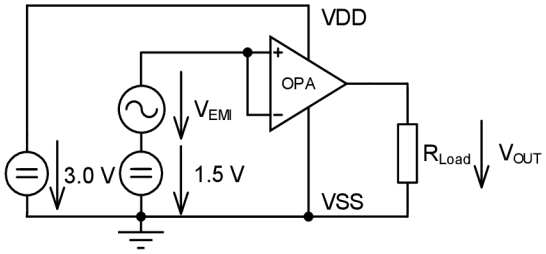


Fig. 50: The EMI susceptibility of the ideal OPA in the ideal common mode.

To overcome OPA AC common mode analysis issues from Fig. 50, the following modified simulation schematic for CMRR simulation from [51] shown in Fig. 51 can be considered.

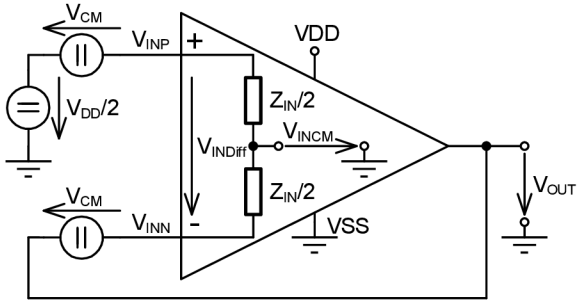


Fig. 51: Simulation of an OPA CMRR (taken and edited from [51]).

This simulation circuit uses the OPA in the non-inverting voltage follower mode similar to the AC open loop gain analyzed in Fig. 44. The trick is in a common mode voltage sources V_{CM} at the OPA inputs, which are identical. For a deeper understanding of the AC OPA common mode analysis, the differential mode and the common mode signal will be elaborated on in more detail. For an OPA input differential voltage V_{INDiff} from the circuit in Fig. 51 can be written the following equation

$$V_{INDiff} = V_{INP} - V_{INN} = V_{CM} + \frac{V_{DD}}{2} - V_{CM} - V_{OUT}, \tag{48}$$

and for an OPA input common-mode voltage V_{INCM} after the circuit superposition analysis method application can be expressed

$$V_{INCM} = \frac{V_{INP} + V_{INN}}{2} = \frac{V_{CM} + \frac{V_{DD}}{2} + V_{CM} + V_{OUT}}{2}, \tag{49}$$

where V_{INP} is an OPA input positive voltage, V_{INN} is an OPA input negative voltage, V_{CM} is the common mode source voltage, V_{DD} is the power supply voltage and V_{OUT} is the OPA output voltage. Further, for the output voltage is valid the following equation (50) according to [51]

$$V_{OUT} = A_{Diff} V_{INDiff} \pm A_{CM} V_{INCM}, \tag{50}$$

where A_{Diff} is an OPA differential mode gain and A_{CM} is an OPA common mode gain. The overall OPA output voltage equation (51) is obtained by substituting equations (48) and (49) into equation (50).

$$V_{OUT} = \frac{A_{Diff}}{1 + A_{Diff} \mp \frac{A_{CM}}{2}} \frac{VDD}{2} \pm \frac{A_{Diff}}{1 + A_{Diff} \mp \frac{A_{CM}}{2}} \left(V_{CM} + \frac{V_{DD}}{4} \right). \tag{51}$$

The above overall output voltage equation seems to be difficult to use. Therefore, assuming that the OPA output voltage will be equal to $V_{DD}/2$ while neglecting the OPA input offset, then the OPA input common-mode voltage can be written

$$V_{INCM} = V_{CM} + \frac{V_{DD}}{2}. \tag{52}$$

After substituting equation (52) into equation (50) with assuming that the OPA input differential voltage V_{INDiff} is zero, the simple overall OPA output voltage equation is obtained

$$V_{OUT} = \pm A_{CM} \left(V_{CM} + \frac{V_{DD}}{2} \right). \tag{53}$$

Then the OPA common mode gain can be derived from the following relationship

$$A_{CM} = \frac{V_{OUT}}{V_{CM} + \frac{V_{DD}}{2}}. \tag{54}$$

Considering the first harmonic components of the OPA overall output voltage and common mode voltage, the AC common mode gain can be calculated by the following equation

$$A_{CM\_AC} = \frac{V_{OUT\_1stHarm}}{V_{CM\_1stHarm}}, \tag{55}$$

where the $V_{OUT\_1stHarm}$ is the first harmonic component of the overall output voltage and $V_{CM\_1stHarm}$ is the first harmonic component of the AC common mode voltage source (V_{CM} in Fig. 51). The used simulation schematic for the OPA input common mode EMI susceptibility simulation is shown in Fig. 52.

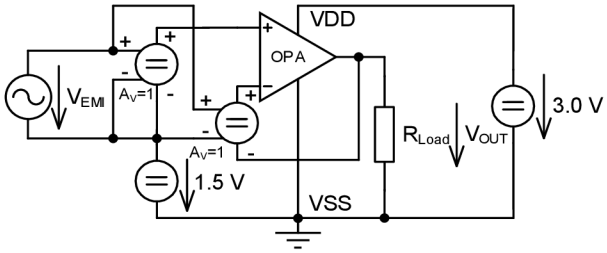
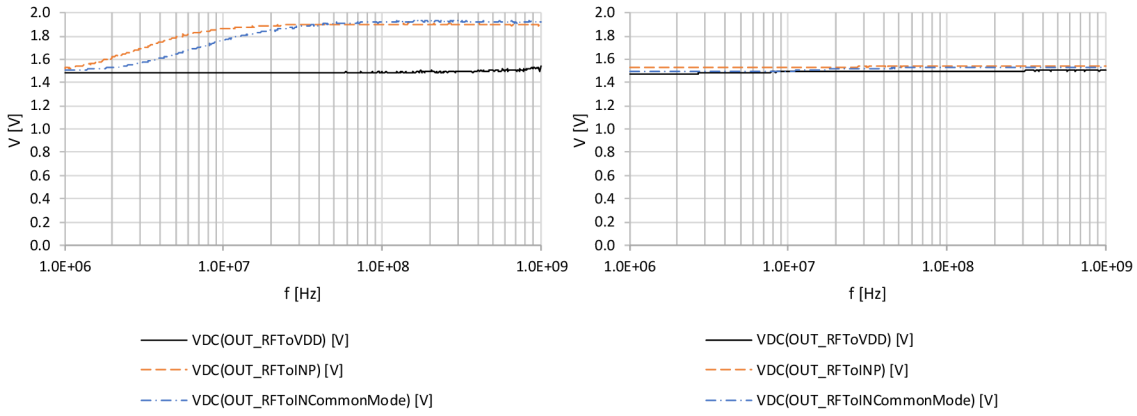


Fig. 52: Simulation schematic for the EMI common mode susceptibility of the OPA.

Transient simulations were performed with 3 V VDD supply voltage. The HF EMI signal was simulated by a V_{EMI} sinusoidal voltage source with variable frequency and chosen 0.632 V amplitude which is large in comparison with the 3 V supply voltage. The 0.632 V amplitude of the V_{EMI} source is approximately equal to 1 mW (0 dBm) power of the DPI method according to IEC 62132-4 [26] when driving high impedance load [27] as the worst-case situation. The EMI susceptibility simulations were performed as the envelope simulation with fifteen harmonics using Cadence Spectre RF® simulator with postprocessing of the V_{OUT} average and the first harmonic voltage values after circuit settling time. The basic EMI susceptibility simulation results as the output voltage characteristics of all described OPA configurations for both OPAs, the folded cascode, and the basic Miller OPA, are shown in Fig. 53.



a) b)

Fig. 53: The EMI (RF) susceptibility simulations of a) folded cascode and b) basic Miller OPA with $V_{EMIpeak}$ of 0.632 V.

The basic EMI susceptibility simulation results as the HF signal transfer characteristics of all described OPA configurations for both OPAs, the folded cascode, and the basic Miller OPA, are shown in Fig. 54.

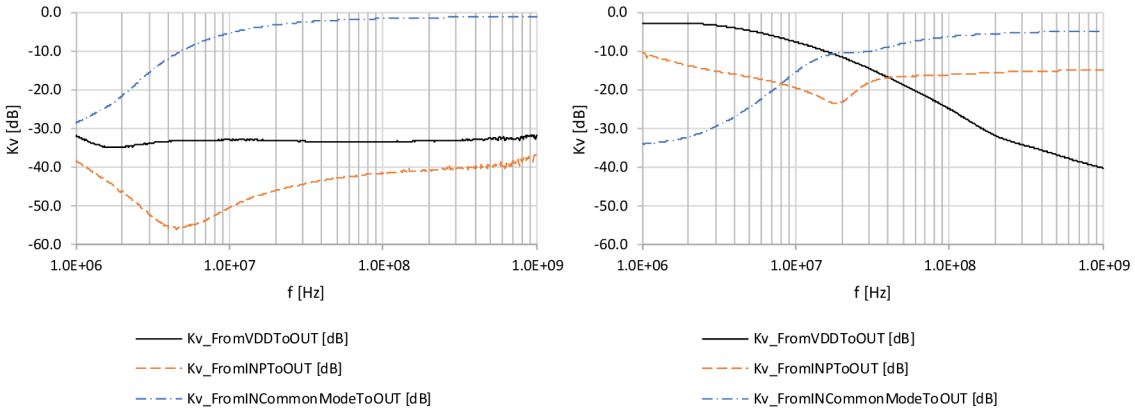


Fig. 54: The HF signal transfers (the first harmonic) of a) folded cascode and b) basic Miller OPA with $V_{EMIpeak}$ of 0.632 V.

These simulations verified that the used folded cascode OPA has a great power supply EMI susceptibility with high PSRR (low HF signal transfer from VDD power supply to V_{OUT}) but not sufficient input common mode EMI susceptibility. This input common mode EMI susceptibility is improved by the filtration capacitors at the OPA inputs in the final bandgap voltage reference. The basic Miller OPA has very good overall DC output voltage shifts induced by the EMI but not sufficient PSRR. The summary worst-case results of the EMI susceptibility simulations for all OPA configurations of both OPAs, the folded cascode, and the basic Miller OPA are presented in the following Tab. 8.

Tab. 8: The comparison of the folded cascode and the basic Miller OPA performance.

Parameter	Folded cascode	Basic Miller
DC open loop gain	73.4 dB	83.4 dB
f_{DP}	~40 Hz	~30 Hz
GBW	~200 kHz	~400 kHz
ICMR	1.1 V	1.6 V
$V_{OUT\_DCSaturation}$	1.96 V	1.91 V
$f_{VOUT\_DCSaturation\_RFToVDD}$	> 1 GHz	> 1 GHz
$f_{VOUT\_DCSaturation\_RFToINP}$	~20 MHz	> 1 GHz
$f_{VOUT\_DCSaturation\_RFToINCM}$	~40 MHz	> 1 GHz
$V_{OUT\_DCVariation\_RFToVDD}$	max ~2.5 %	max ~1.3 %
$V_{OUT\_DCVariation\_RFToINP}$	max ~27.1 %	max ~2.8 %
$V_{OUT\_DCVariation\_RFToINCM}$	max ~28.6 %	max ~2.5 %
PSRR	min ~31.6 dB	min ~2.7 dB
Current consumption	typ 1.5 µA	typ 12.0 µA

4.2.3. EMI Susceptibility of the Overall Voltage Reference

To verify the performance of the overall bandgap voltage reference, the basic EMI susceptibility transient simulations were performed with the final version of the bandgap core and the one-stage folded cascode OPA used in the original voltage reference design. The folded cascode OPA with frequency compensation by the C_{DP} capacitor towards VSS and source follower output is shown in Fig. 43 a), chapter 4.2.2. The final bandgap core configuration is with leakage compensation bipolar transistor Q3, filtration capacitors C_A and C_B, and common mode transistors M1 and M2 as is shown in the simulation schematic in Fig. 55. For more information about the final bandgap core configuration see chapter 4.1.

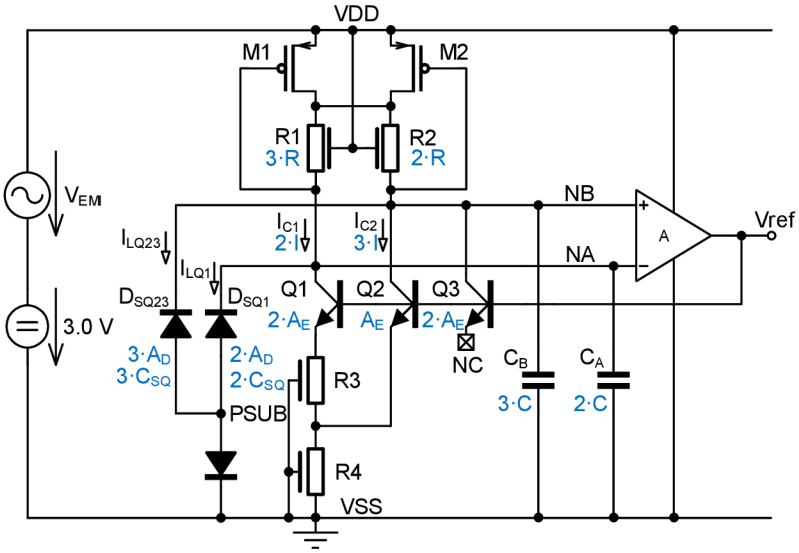
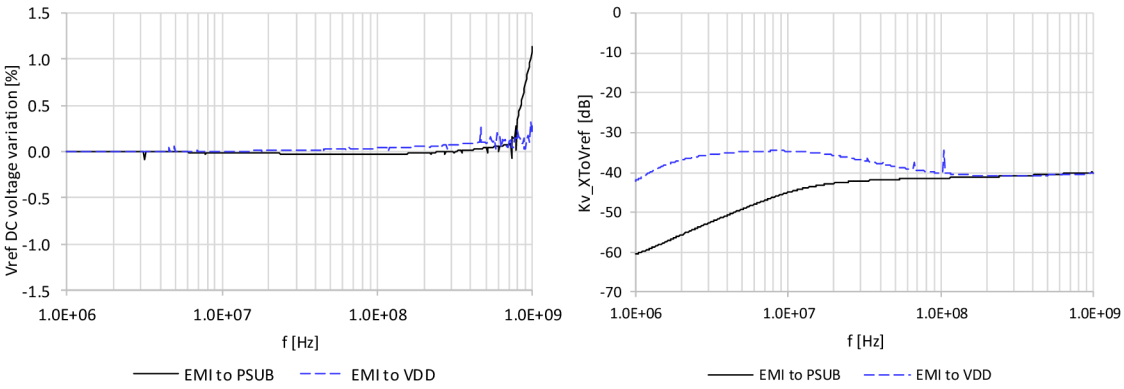


Fig. 55: The basic VDD EMI susceptibility simulation schematic of the overall voltage reference.

Transient simulations were performed with 3 V VDD supply voltage. The HF EMI signal was simulated by a V_{EMI} sinusoidal voltage source with variable frequency and chosen 0.632 V amplitude which is large in comparison with the 3 V supply voltage. The 0.632 V amplitude of the V_{EMI} source is approximately equal to 1 mW (0 dBm) power of the DPI method according to IEC 62132-4 [26] when driving high impedance load [27] as the worst-case situation.

The basic bandgap core P-substrate (PSUB) EMI susceptibility simulations were performed with a small change in simulation schematics which is shown in Fig. 40 (for more information see chapter 4.2.1). The EMI susceptibility simulations were performed as the envelope simulation with fifteen harmonics in the Cadence Spectre RF® simulator with postprocessing of the V_{ref} average and the first harmonic voltage values after circuit settling time. The basic VDD and PSUB EMI susceptibility simulation results of the overall bandgap reference are shown in Fig. 56.



a) b)

Fig. 56: The a) V_{ref} DC voltage variations and b) HF signal transmissions from coupling point to V_{ref} (first harmonic) within basic EMI susceptibility simulations of the overall bandgap with $V_{EMIpeak}$ of 0.632 V.

These results show the overall superior VDD EMI susceptibility of the described bandgap voltage reference. The V_{ref} DC voltage variation is less than 0.25 % and PSRR is higher than 35 dB for EMI superimposed to VDD power supply in the frequency range from 1 MHz to 1 GHz. The bandgap EMI susceptibility to P-substrate noises is also very good. For this situation, the V_{ref} DC voltage variation is no more than 1.1 % and the V_{ref} ripple rejection of PSUB EMI is higher than 40 dB. The simulation results also demonstrate the validity of the EMC robust design methodology which consists of the following general recommendations:

a) Using a fully symmetrical and differential topology everywhere where it is possible for high CMRR and PSRR.

b) Keep all possible nodes in a low impedance state at high frequencies.

c) Make symmetrical filtering of all differential signals and keep the same time constants.

d) Count with hidden structures of the IC.

4.2.4. EMI Susceptibility Measurement Results

The complete schematic of the EMC robust and low power voltage reference is shown in Fig. 32 in chapter 4.1. This bandgap was processed in onsemi I3T50 technology as a part of the test chip and a die photo is shown in Fig. 57.

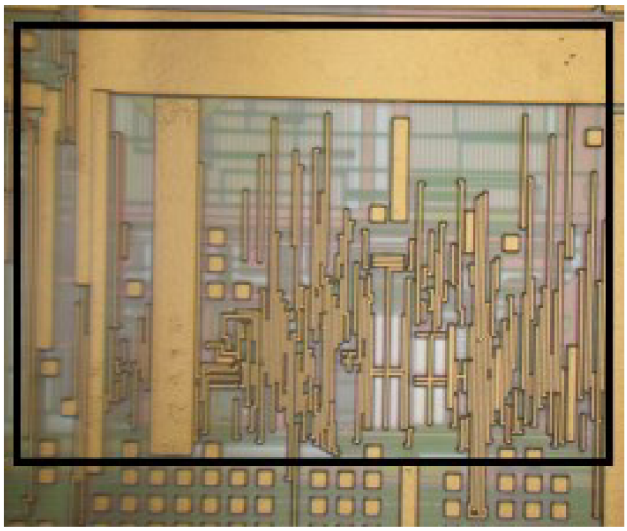


Fig. 57: Die photo of the realized voltage reference with marked bandgap area.

The DPI method, as per IEC 62132-4 [26], is used to test the EMI susceptibility of the bandgap. A deterministic interfering signal is added to a pin of the device under test (DUT), and its functionality is monitored for malfunctions while the signal is applied. The DPI measurement setup is shown in Fig. 58.

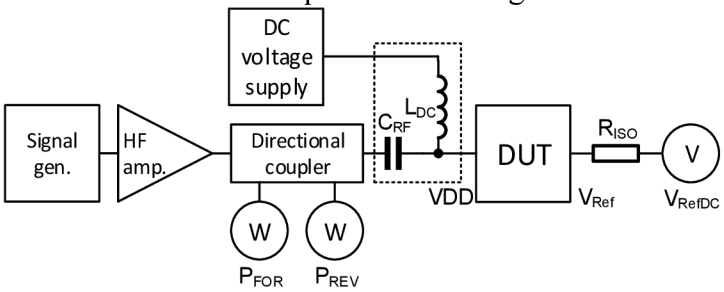


Fig. 58: The DPI measurement setup for supply pin according to IEC 62132-4 [26].

The EMI disturbance signal was superimposed to the VDD supply voltage line through a coupling capacitor C_{RF} (4.7 nF typical value). It is important to note that there was no decoupling capacitor on the supply line from an external source. To isolate the voltage supply from the HF signal, an L_{DC} coil of 5 µH and a ferrite bead, which form the bias-Tee circuit (see Fig. 24 in chapter 3.2.3), have been used. In order to prevent the capacitance impact of the coaxial line and the connected digital voltmeter, an external 100 kΩ resistor R_{ISO} is used to decouple the measured V_{ref} output. The VDD EMI susceptibility measurement results for two constant P_{For} powers of the realized bandgap on the test chip are shown in Fig. 59.

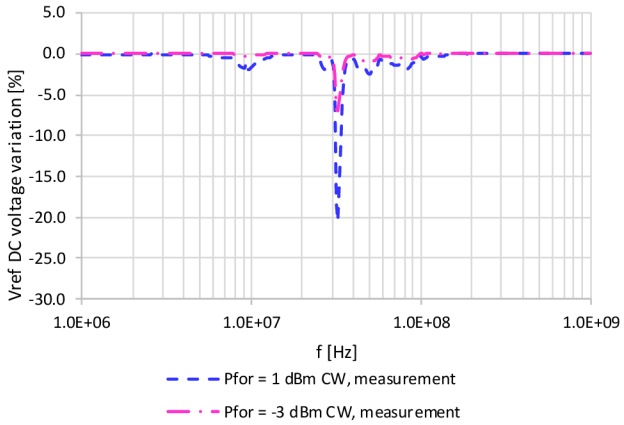


Fig. 59: The power supply EMI DPI measurement results for -3 and 1 dBm P_{For} constant power.

These measurement results show the overall good VDD EMI susceptibility of the described bandgap voltage reference. The V_{ref} DC voltage variation is at most 7.0 % for -3 dBm ($V_{VDD\_EMIpeak}$ of 0.448 V for driving high impedance load) and 20.0 % for 1 dBm ($V_{VDD\_EMIpeak}$ of 0.710 V) to the power line. The DC voltage variation looks like a narrow band resonance characteristic with resonance at 31 MHz. This issue will be deeper analyzed in the next chapter 4.2.5. The summary performance of the realized voltage reference compared with other voltage references from available literature with the power supply EMI susceptibility measurement results are presented in the following Tab. 9.

Tab. 9: The comparison of voltage reference performance with power supply EMI susceptibility measurements from the available literature.

Reference	[12]	[21]	[23]	ADR512 [52]	LT1460 [52]	This work, 1st BG **[48]**
Technology	0.7 µm	0.7 µm	0.35 µm	Not specified	Not specified	0.35 µm
Topology	Kuijk	Brokaw	Brokaw	Shunt ref.	Series ref.	Brokaw
Supply voltage	3.3 V	3.0 V	3.3 V	5.0 V	5.0 V	3.0 V
Output voltage	1.140 V	1.170 V	1.247 V	1.200 V	2.500 V	1.205 V
Temp. range	-40 to 125 °C	-40 to 125 °C	-10 to 180 °C	-40 to 85 °C	-40 to 85 °C	-40 to 160 °C
Current cons.	110 µA	46 µA	50 µA	min. 100 µA	100 µA	3.5 µA
EMI DPI level	-1 dBm	-13 dBm	-5 dBm	4 dBm	4 dBm	-3 dBm
V_{ref} DC variation	max. 3.5 %	max. 12.0 %	max. 7.8 %	max. 16.7 %	max. 4.0 %	max. 7.0 %

The comparison of the achieved EMI results with other voltage references is a little bit difficult because some presented measurement results are provided with different test setups and RF powers. For example, EMI DPI susceptibility with a 50 Ω termination resistor at the EMI coupled pin was measured in [52], which gives better-measured results due to impedance matching and resonance damping. This situation is not realistic as the 50 Ω resistor (e.g., at the power supply pin) is usually not used in the real application of the IC. Nevertheless, the EMI results of the described bandgap reference with the lowest current consumption from all presented are good.

4.2.5. New EMI DPI Simulation Method

The hidden issue of the DPI measurement setup and the IC that creates the significant V_{ref} DC voltage variation is revealed and explained in this chapter.

As it was written in chapter 4.2.4, the measured DC voltage variation looks like a narrow band resonance characteristic with resonance at 31 MHz. If it will be assumed that the DPI measurement setup consists of the non-ideal bias-Tee filter (Fig. 24 in chapter 3.2.3), the coaxial transmission line, and a simple probe to the VDD power line of the IC, then there must be resonance effects. Further, it can be assumed that the serial resonance of the VDD power line can cause a high RF current which also flows through the IC's external and internal capacities. Then a VDD voltage ripple caused by the RF current flowing through these capacities can be higher than the V_{EMI} amplitude. To verify this consideration, a VDD EMI DPI simulation schematic based on the VDD DPI measurement setup and bias-Tee filter modeling (see chapter 3.2.3) was created. The VDD EMI susceptibility simulation schematic with the related DPI measurement setup model is shown in the following Fig. 60.

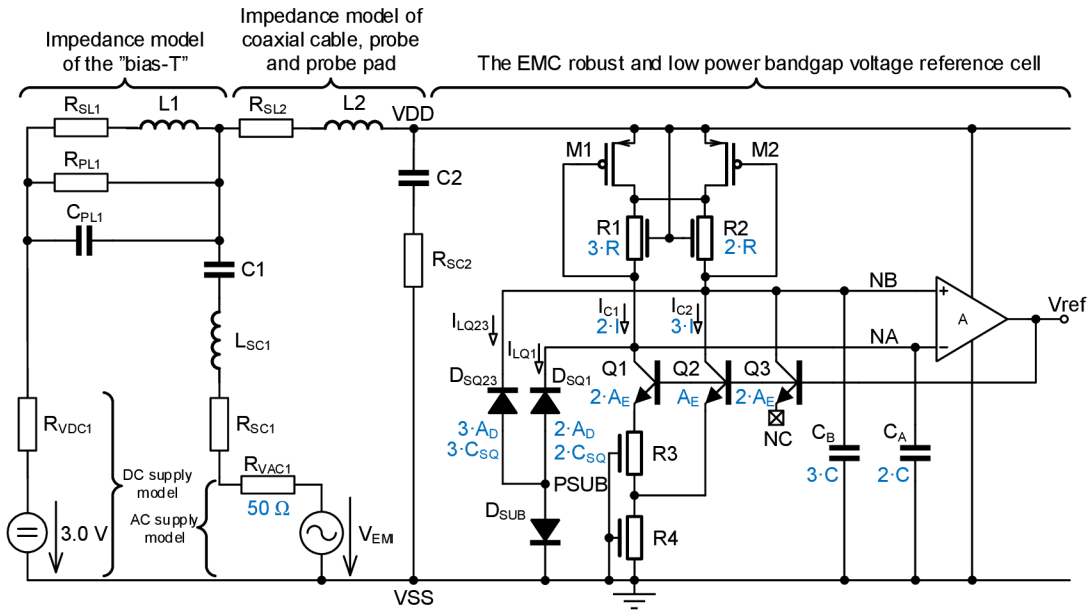


Fig. 60: The VDD EMI susceptibility simulation of the bandgap voltage reference with the DPI measurement setup model.

The values for the circuit components used in the bias-Tee filter were taken from chapter 3.2.3, which deals with passive network synthesis. $L2$ and $C2$ values were calculated and simulated to adjust the resonance frequency based on the VDD DPI susceptibility measurement results. The main objective of this method is to gain a better understanding of the observed effect. A summary of the DPI simulation circuit model elements with their descriptions is in Tab. 10.

Tab. 10: The DPI simulation circuit model elements (rounded to one decimal place).

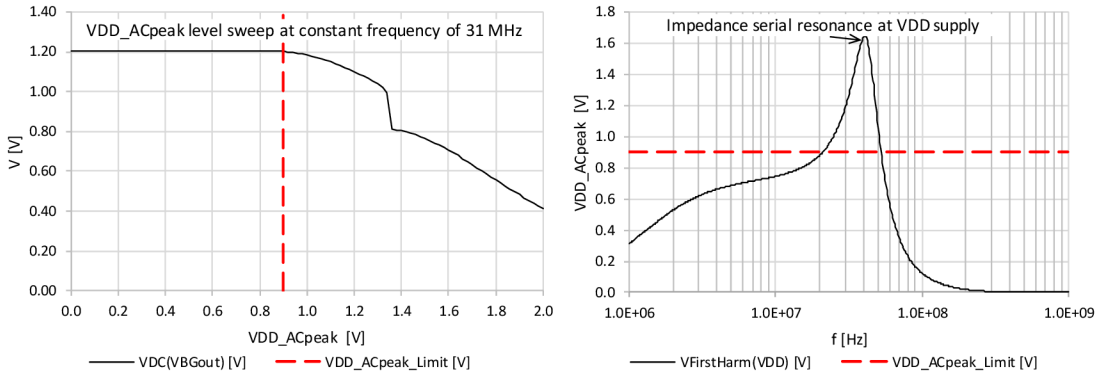
Model element	Value	Description
$C1$	4.5 nF	The bias-T coupling capacitor capacity (verified by the LCR meter).
L_{SC1}	13.4 nH	The total inductance of the bias-T BNC connector, PCB track, and coupling capacitor.
R_{SC1}	1.3 Ω	The total DC resistance of the bias-T BNC connector, PCB track, and coupling capacitor.
$L1$	4.0 μH	The inductance of the bias-T DC coil (verified by the LCR meter).
R_{SL1}	1.0 Ω	The winding resistance of the bias-T DC coil.
R_{PL1}	7.9 kΩ	The ferrite core loss resistance of the bias-T DC coil.
C_{PL1}	20.9 pF	The inter-turn capacity of the bias-T DC coil with the PCB track capacity (to the ground).
$L2$	484.8 nH	The inductance of the coaxial cable and a probe connected to the IC VDD supply line.
R_{SL2}	50.0 mΩ	The serial resistance of the L2.
$C2$	52.7 pF	The capacity of the coaxial cable, the probe, and a probe pad of the IC VDD supply line.
R_{SC2}	50.0 mΩ	The serial resistance of the C2.
R_{VAC1}	50.0 Ω	The internal resistance of the AC voltage source (simulates the EMI generator).
R_{VDC1}	10.0 Ω	The internal resistance of the DC low power voltage source.

The values of the circuit components for the coaxial cable, the probe, and the probe pad impedance model were derived by the following process. In the first step, the 500 nH inductance of the $L2$ coil and the 28.4 pF capacity of the $C2$ capacity were chosen. Then auxiliary EMI simulations were performed:

a) with the simple overall bandgap voltage reference for V_{DD_ACpeak} voltage estimation when the V_{ref} voltage goes to the measured value at problematic frequency 31 MHz (V_{ref} decreases about 20 % for 1 dBm in Fig. 59).

b) with the overall bandgap DPI measurement setup circuit model for serial resonance frequency estimation ($L2$ inductance value recalculation to desired resonance frequency according to Fig. 59).

The auxiliary EMI susceptibility simulation results of the described bandgap reference setups are shown in Fig. 61.



a) b)

Fig. 61: Auxiliary VDD EMI susceptibility simulations for DPI model elements estimation: a) basic EMI susceptibility at constant frequency and b) AC voltage at internal VDD supply with $V_{EMIpeak}$ = 0.710 V (1 dBm P_{For}).

The total VDD net capacity is calculated by the following equation from the known serial resonance frequency of the first approach of the $L2$ and $C2$ components.

$$C_{VDDtotal} = \frac{1}{\left(2\pi f_{ser\_res\_aux}\right)^2 L2}. \tag{56}$$

The $f_{ser\_res\_aux}$ is VDD impedance serial resonance frequency which is 41 MHz according to auxiliary basic EMI susceptibility simulation shown in Fig. 61 b). Further, the total VDD capacity is equal to the sum a VDD native capacity of the bandgap circuit $C_{VDDnative}$ with additional capacity $C2$ as is described in the following equation

$$C_{VDDtotal} = C_{VDDnative} + C2. \tag{57}$$

The VDD native capacity of the bandgap circuit's $C_{VDDnative}$ value is 1.7 pF and it was calculated from the following equation

$$C_{VDDnative} = C_{VDDtotal} - C2, \tag{58}$$

where the calculated total VDD net capacity $C_{VDDtotal}$ value is 30.1 pF according to (56) and the chosen added capacity $C2$ is 28.4 pF. The calculation continues with the VDD supply net impedance approximate estimation. The VDD impedance can be calculated according to equation (59)

$$|Z_{VDD}| = \frac{V_{DD\_ACpeak}}{I_{C2\_ACpeak}}, \tag{59}$$

where V_{DD_ACpeak} is a voltage obtained from the auxiliary EMI susceptibility simulation at the problematic frequency and I_{C2_ACpeak} current is approximately the maximum current from the V_{EMI} generator, which occurs at the serial impedance resonance. This current can be calculated according to equation (19) for Z_L = 0 Ω in chapter 3.1. From the VDD impedance at VDD serial resonance, the total new VDD capacity $C_{VDDtotalNew}$ can be calculated as follows

$$C_{VDDtotalNew} = \frac{1}{2\pi f_{ser\_res}|Z_{VDD}|}. \tag{60}$$

The total new VDD capacity $C_{\mathrm{VDDtotalNew}}$ value is 54.4 pF and from this value is calculated $L2$ new inductance value according to the following equation

$$L2_{New} = \frac{1}{\left(2\pi f_{ser\_res}\right)^2 C_{VDDtotalNew}}, \tag{61}$$

where $f_{\mathrm{ser\_res}}$ is the VDD impedance serial resonance frequency, which is 31 MHz. Finally, the newly added capacity $C2_{\mathrm{New}}$ can be calculated as follows

$$C2_{New} = C_{VDDtotalNew} - C_{VDDnative}. \tag{62}$$

The newly added capacity $C2_{\mathrm{New}}$ value is 52.7 pF and the $C_{\mathrm{VDDnative}}$ capacity value is 1.7 pF. After the C2 and L2 values estimation, the VDD EMI susceptibility simulation of the overall bandgap reference with the DPI measurement setup circuit model was performed. It must be noted that the EMI susceptibility simulations were performed as the envelope simulation with fifteen harmonics in the Cadence Spectre RF® simulator with postprocessing of the V_{ref} average and the V_{DD} first harmonic voltage values after circuit settling time. The EMI susceptibility simulation results of the described simulation schematic (Fig. 60) compared with the EMI DPI susceptibility measurement of the test chip bandgap are shown in Fig. 62.

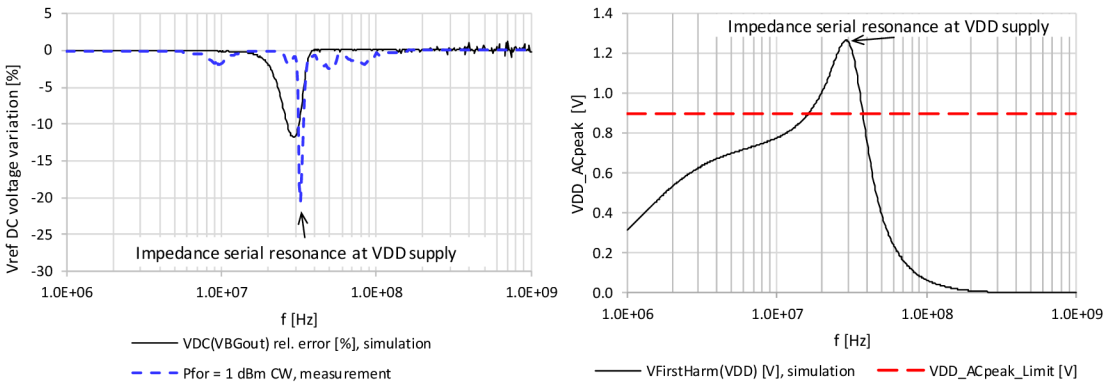


Fig. 62: The a) V_{ref} DC voltage variation and b) AC voltage at VDD supply of the bandgap DPI setup model simulation with V_{EMIpeak} = 0.710 V (1 dBm P_{For}).

The presented EMI susceptibility simulation results show that the VDD EMI signal is higher than the allowable limit, which is 0.9 V in peaks (for more information see chapter 4.1). The described low power and EMC robust bandgap voltage reference is designed for an EMI with 0.9 V amplitude and for a higher V_{EMI} amplitude at VDD supply is not guaranteed correct functionality. The measurement and simulation results confirm this hypothesis and for further bandgap VDD EMI susceptibility improvement VDD impedance serial resonances must be taken into account.

The described bandgap voltage reference and achieved results were published in the "An Automotive Low-Power EMC Robust Brokaw Bandgap Voltage Reference" paper [48].

4.3. Possibilities of the Power Supply EMI Susceptibility Reduction

From all the achieved results in chapter 4.2.5 about power supply EMI susceptibility of the low power Brokaw bandgap voltage reference in this work, it is evident, that the main issue is the resonances on the power supply line. These resonances can create a higher voltage supply ripple than the EMI generator can produce when it drives a high impedance load in the ideal case. Therefore, it is important to pay more attention to this phenomenon and consider here some compensation for this effect by, e.g., using the discussed following techniques:

a) Using a fast rectifier at the supply line for the bandgap reference.

b) Using a passive VDD supply net resonance damping circuit.

c) Using an active VDD supply net resonance damping circuit.

d) Using a fast VDD supply switch controlled by the internal VDD supply voltage value, which cannot be very low or very high.

e) Using an EMC robust voltage pre-regulator for the bandgap supply.

The presented techniques for EMC robust design are listed from the simplest to more complex and more expensive. The following text discusses the pros and cons of each mentioned technique.

Ad a) Pro is a high-frequency EMI translation to an ideal DC value of the voltage supply in case of appropriate supply filtration. Cons are reverse voltage stress when rectified voltage increases up to a given limit value by high EMI peaks and the finite speed of the rectifier due to its reverse recovery time. The unwanted capacity between input and output reduces the upper limit of the frequency range as well.

Ad b) Pro is resonance voltage peak damping, ideally in a wide frequency range. Con is higher power dissipation of a damping element, e.g., resistor, which causes resonance energy loss. This unpredictable loss causes a temperature increase in the element, which may lead to the element's destruction.

Ad c) Pros are resonance voltage peak damping, ideally in a wide frequency range, and lower power dissipation of the damping element. Cons are the finite speed of active damping and increased complexity. The active damping realization is very difficult at higher frequencies.

Ad d) Pros are voltage supply values in the required range and ideally zero power dissipation of the switch. Cons are the finite speed of the switch control, unwanted capacity between input and output of high voltage switch, and increased complexity.

Ad e) Pros are increased overall PSRR and regulated bandgap voltage supply in the required range with a higher dynamic range of a higher external supply domain. Cons are controlled startup procedure (first egg or chicken issue), higher requirements for higher external supply voltage (e.g., undervoltage/overvoltage transients with internal supply discharging/charging effects), and increased complexity.

From the mentioned resonance compensation techniques, the voltage pre-regulator for the bandgap supply is practically the most used. This voltage regulator has mostly a built-in unprecise voltage reference due to supplying the precise voltage reference during the startup phase. When the precise reference voltage is up to a given value (e.g., 80% of nominal value), then the voltage regulator is switched to this precise reference voltage in order to parametric regulation of the output voltage. The description of the EMC robust voltage pre-regulator is not intended in this work. The voltage reference only will be examined and improved for EMI susceptibility in case of low PSRR of the integrated voltage pre-regulator, which is externally supplied from the pin. The voltage regulator will be bypassed by a direct connection to the internal voltage reference supply during measurements.

For further work, an effort will be taken to find new techniques and principles for EMI susceptibility improvement of the new voltage reference. Before finding new techniques for susceptibility reduction, systematic studies of commonly used voltage reference core and OTA topologies will be conducted in the next chapters. From the achieved results, a suitable basic topology of the voltage reference will be selected for further improvements and investigations.

4.4. Study of Different Integrated Basic Bandgap Cores

Systematically analysis of existing and commonly used bandgap core topologies of voltage references was published in the "An EMC Susceptibility Study of Integrated Basic Bandgap Voltage Reference Cores" paper [53]. The paper includes temperature drift, sensitivity to OPA amplifier input offset, line regulation, and EMC susceptibility comparisons for Kuijk, Brokaw, and Tsividis concepts with a reduced count of BJTs.

Many articles focus on the temperature dependence of voltage references usually within a limited temperature range from -50 °C to 125 °C [54]-[59]. With this temperature range, the reachable temperature coefficients (TCs) are tens of ppm/°C and even 2 ppm/°C with some more advanced techniques. However, higher current consumption and higher supply voltage requirements are the costs of these very low-temperature variations [60]. In the automotive industry, the maximum junction temperature can go up to 200 °C during operation. Voltage references designed to handle such high temperatures often use advanced curvature correction techniques based on measurement of temperature characteristics and trimming [60], [61].

The automotive voltage references in sub-micron technologies are also limited by supply voltage, where the reference has to be parametric, e.g., from 2 V, to support fluctuating supplies [60]. The current consumption from this onboard power supply can be around 10 µA for a complete system on chip, including voltage reference, regulators, wakeup blocks, etc. [60].

From the above-mentioned requirements, the following criteria for the analysis of the basic bandgap cores are considered: temperature drift over a wide temperature range from -50 °C to 200 °C, line regulation for supply voltage from 2 V to 4 V, and low EMI susceptibility over wide high frequency (HF) range from 100 kHz to 1 GHz. The current consumption of the bandgap shall be less than 5 µA. It is worth noting that MOS transistors in a sub-threshold region can be used instead of BJTs, but they are usually not used in automotive bandgap designs due to their weakness in noise immunity [60]. To compare bandgap core topologies and not BJT properties, only NPN bandgap cores will be used further [53].

4.4.1. Integrated Basic Bandgap Core Topologies

There are several well-known basic topologies of bandgap voltage reference cores. The first chosen one is the Kuijk, the second one is the Brokaw, and the third one is the Tsividis bandgap core [62]. These cores are shown in Fig. 63.

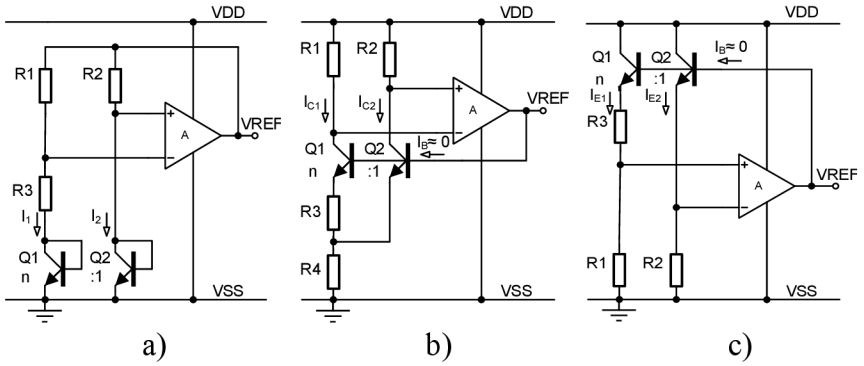


Fig. 63: The a) Kuijk, b) Brokaw and c) Tsividis bandgap core topologies [53].

The Kuijk core usually employs two bipolar transistors, Q1 and Q2, with the same currents, I_1 and I_2 [57]. This means that the resistors $R1$ and $R2$ have the same value and a ratio n:1 of bipolar transistor emitter areas A_{E1}/A_{E2} (also as the bipolar transistor units' ratio) is, in most cases, 8:1 in order to get a common centroid layout with Q2 in the middle. In the case of ideal BJTs without base currents, the output reference voltage is described by the following equation

$$V_{REF} = mV_T\, ln\left(\frac{I_2}{I_1}n\right)\left(\frac{R1}{R3}+1\right)+V_{BE1}, \tag{63}$$

where m is an emission coefficient with a value between 1 to 2, V_T is a temperature voltage $k(T_j+273.15)/q$, and V_{BE1} is the base-emitter voltage of the Q1 BJT.

The Brokaw core employs two BJTs, Q1 and Q2, with the same collector currents, I_{C1} and I_{C2}, similar to the Kuijk bandgap core. In the case of ideal BJTs without base currents I_B, the output reference voltage is described by the following equation

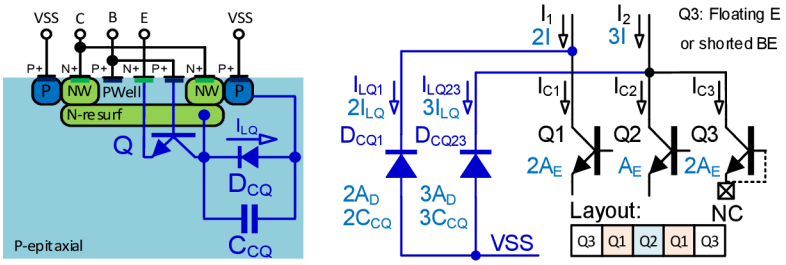
$$V_{REF} = V_{BE2}+\frac{R4}{R3}mV_T\, ln\left(\frac{I_{C2}}{I_{C1}}n\right)\left(1+\frac{R1}{R2}\right). \tag{64}$$

The Tsividis core employs two BJTs, Q1 and Q2, with the same emitter currents, I_{E1} and I_{E2}. This means that the resistors $R1$ and $R2$ have the same value, and the ratio n:1 of bipolar transistor emitter areas A_{E1}/A_{E2} is, in most cases, 8:1. In the case of ideal BJTs without base currents I_B, the output reference voltage is described by the following equation

$$V_{REF} = V_{BE1}+mV_T\, ln\left(\frac{I_{E2}}{I_{E1}}n\right)\left(1+\frac{R1}{R3}\right). \tag{65}$$

4.4.2. Collector Leakage Current Compensation

The collector of the vertical NPN type BJT is often isolated from the IC substrate only by a reverse polarized junction diode. The leakage current of this diode influences the accuracy of the bandgap, especially when working with small collector currents (about 1 µA) at temperatures higher than 150 °C [49].



a) b)

Fig. 64: a) NPN BJT cross-section in the IC and b) the collector leakage current compensation principle [53].

Fig. 64 a) shows a simplified cross-section of a vertical NPN-type BJT, which is processed in 180 nm BCD technology. The leakage current of the BJT's collector diode D_{CQ} can cause an error in the collector current. This effect mainly impacts Kuijk and Brokaw bandgap cores [53].

Collector leakages can be compensated by adding n - 1 dummy BJTs in parallel to Q2 in the case $I_{C1} = I_{C2}$, having the same ratio of leakage currents as the ratio of collector working currents [49]. This means adding seven BJTs when n is eight for the well-known Brokaw 8:1 core. For this case, it is very difficult to reach full symmetry for 16 BJTs, and the area is significantly increased. To reduce the area and have a symmetrical layout of the BJTs, n equal to two was chosen and the collector currents I_{C1} and I_{C2} in the ratio of 2:3. The chosen BJT's ratio requires only two dummy BJTs connected in parallel to Q2 for the compensation of leakages as was used in [48]. Fig. 64 b) shows the symmetrical layout of five BJTs in one row.

From the chosen ratio of collector currents 2:3, in the presented bandgap BJT configuration, the PTAT voltage as the difference between two base-emitter voltages of Q2 and Q1 BJTs is simplified to the following form

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = mV_T \, ln\left(\frac{I_{C2}A_{E1}}{I_{C1}A_{E2}}\right), \tag{66}$$

$$\Delta V_{BE} = mV_T \, ln\left(\frac{3I2A_E}{2IA_E}\right) \approx V_T. \tag{67}$$

This means no basic amplification of the temperature voltage. The BJT collector leakage currents compensation is described by the following equations where collector current is assumed as a difference between the input current and the BJT leakage current like for Q1: $I_{C1} = I_1 - I_{LQ1}$.

$$\Delta V_{BE} = mV_T \, ln\left[\frac{(I_2 - I_{LQ23})A_{E1}}{(I_1 - I_{LQ1})A_{E2}}\right] = mV_T \, ln\left[\frac{3(I - I_{LQ})2A_E}{2(I - I_{LQ})A_E}\right] \approx V_T, \tag{68}$$

where I is a unit bias current and I_{LQ} is a unit leakage current. Equation (68) shows that the additional dummy BJTs add leakage currents in the required ratio, and the collector currents ratio ideally stays the same. Therefore, the difference between the two base-emitter voltages is not impacted by the collector leakage currents [53].

4.4.3. Investigated Bandgap Cores

This study proposes nine simple bandgap cores from the three chosen basic bandgap core topologies with two methods of collector leakage current compensation. The compensation BJT Q3 (see Fig. 64 b)) with a floating emitter [48] and a shorted base-emitter (BE) junction connected to an emitter of Q2 [49] as two different versions for the leakage compensation were chosen. With the floating emitter, the impact of the collector substrate junction leakage is mainly expected. With the shorted BE junction connected to the emitter of Q2, a leakage current of closed bipolar to the circuit in emitters of BJTs is added. Fig. 65 shows the proposed bandgap cores.

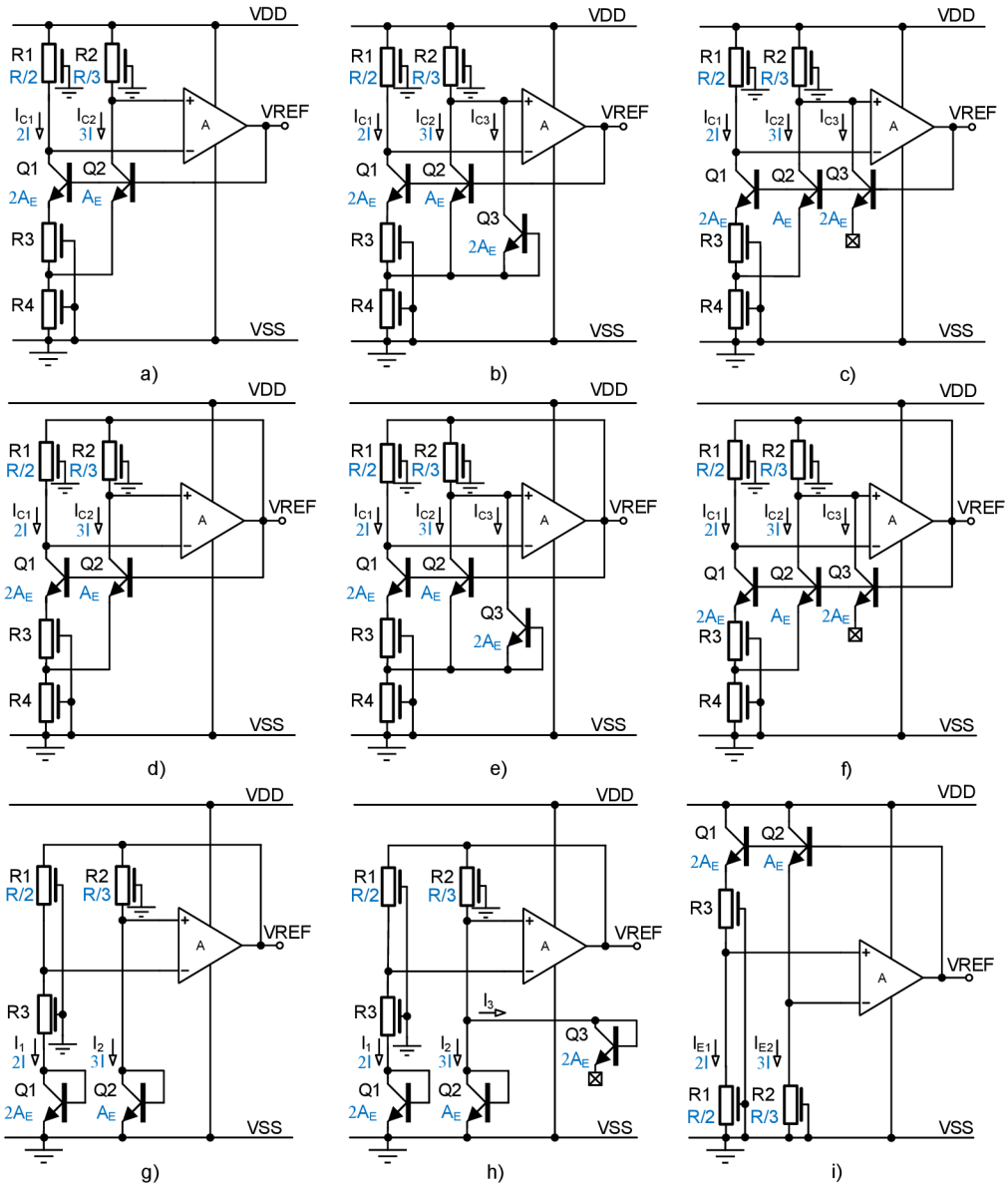


Fig. 65: The proposed bandgap cores for investigations [53].

The chosen bandgap cores are:

a) Brokaw bandgap 2:1,

b) Brokaw bandgap 2:1 with the collector leakage current compensation where the compensation BJT has shorted BE junction,

c) Brokaw bandgap 2:1 with the collector leakage current compensation where the compensation BJT has a floating emitter,

d) Self-supplied Brokaw bandgap 2:1,

e) Self-supplied Brokaw bandgap 2:1 with the collector leakage current compensation where the compensation BJT has shorted BE junction,

f) Self-supplied Brokaw bandgap 2:1 with the collector leakage current compensation where the compensation BJT has a floating emitter,

g) Kuijk bandgap 2:1,

h) Kuijk bandgap 2:1 with the collector leakage current compensation where the compensation BJT has a floating emitter, and

i) Tsividis bandgap 2:1.

The well-known Brokaw 8:1 bandgap core as a reference is also included. All proposed bandgap cores are designed to have the same operating point, such as bias currents of the cores and the same ratio of currents and BJTs. The current consumption of each bandgap core is around 1.3 μA. The one collector current compensation is chosen only for the Kuijk bandgap core due to the connection of the BJTs like diodes. Only BJT's intrinsic reverse polarized diodes between collectors and VSS ground keep collector leakage currents in the same ratio as the ratio of working currents I_1:I_2 (Fig. 65 h)). In general, the Tsividis core does not need leakage current compensation in collectors because it uses the emitter currents. Therefore, this core without compensation transistors (Fig. 65 i)) is first analyzed [53].

4.4.4. OPA Model

To be able to investigate the impact of the bandgap cores only, the OPA is modeled by a simple idealized model with one frequency pole and output resistance. The OPA model is shown in Fig. 66.

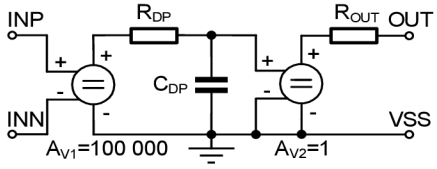


Fig. 66: The OPA circuit simulation model [53].

The INP pin is a noninverting (positive) input, and the INN pin is an inverting (negative) input of the OPA. The OPA consists of two voltage-controlled voltage sources (VCVSes) with a voltage gain A_V. Between these sources is an RC network defining the frequency of the dominant pole. The OPA simulation model has a DC open loop gain of 100 dB, a dominant pole frequency of 10 Hz, a unity gain bandwidth of 1 MHz, and an output resistance of 1 kΩ. These chosen parameters are very close to a real bandgap OPA. It must be noted that the OPA model is independent of the supply voltage variations [53].

4.4.5. Simulation Setup

All proposed bandgap cores are analyzed one by one in the same simulation setup within the Cadence Virtuoso analog design environment. The common simulation setup schematic diagram is shown in Fig. 67.

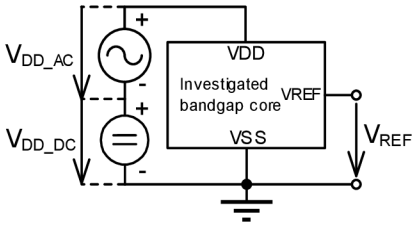


Fig. 67: The common simulation setup for investigated bandgap cores [53].

The V_{DD_DC} is 3 V as a DC supply voltage source. The V_{DD_AC} is 0 V or 1 V peak with a sweeping frequency *f* as a common AC sine wave voltage source for EMC susceptibility investigations. The analytical tools of the Cadence Spectre RF simulator were used for all simulations, especially an envelope analysis for the EMC susceptibility simulations [53].

4.4.6. Temperature Drifts

The reference voltage temperature drifts of all proposed bandgap cores were simulated for junction temperature from -50 °C to 200 °C. The reference voltage of each proposed bandgap core was normalized to the reference voltage at a room temperature of 27 °C. The resulting temperature drifts are shown in Fig. 68.

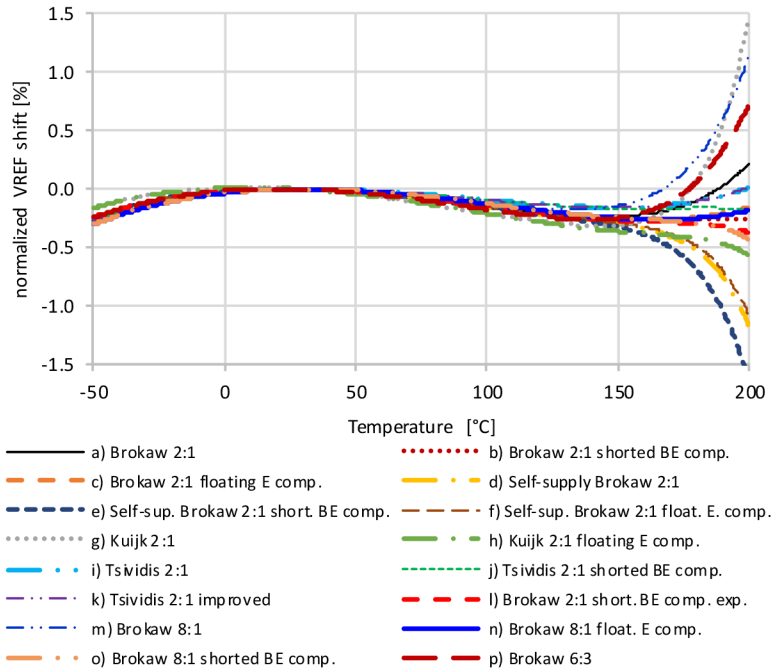


Fig. 68: The temperature drifts of all proposed bandgap cores [53].

From the overall temperature drifts, it can be seen that Kuijk 2:1 and Brokaw 8:1 cores have the highest sensitivity to unbalanced collector leakage currents. The mentioned collector leakage current effect is seen as a higher voltage tail in the range from 150 °C to 200 °C. The self-supplied Brokaw 2:1 core also has a high sensitivity to unbalanced leakage currents, and balancing leakages does not help much due to the saturation effect of BJTs. The saturation of BJTs is caused by voltage drops on the collector resistors. The increased voltages on the collector resistors push the BJTs to the unwanted deep saturation mode, which results in a decrease in the reference voltage. The voltage drops on collector resistors cannot be very small because decreasing the voltage drop reduces the operating range at the OPA input and increases unwanted sensitivity to the OPA input offset.

The Brokaw 2:1 bandgap core has medium sensitivity to unbalanced leakage currents, and balancing collector leakage currents shows its essence for both leakage compensations. For compensation comparison and more investigation of each version, additional experimental leakage compensation setups were prepared. The additional experimental simulation setups are shown in Fig. 69.

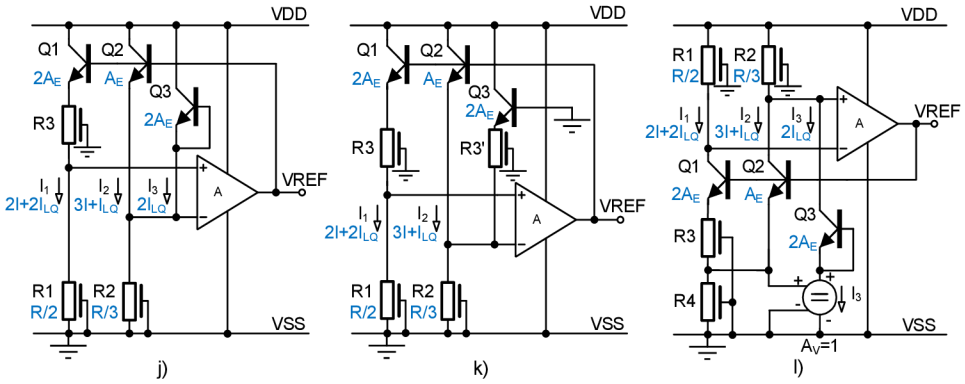


Fig. 69: Tsividis 2:1 j), k) and Brokaw 2:1 l) experiments [53].

These experiments include the shorted BE leakage compensation in the Tsividis 2:1 bandgap core (Fig. 69 j)) and improved capacity balance at OPA inputs (Fig. 69 k)) in the same core as well. The shorted BE compensation BJT connected through a VCVS to the ground in the Brokaw 2:1 bandgap core cancels the influence on the resistive divider *R*3 and *R*4 and keeps the leakage current from the collector to the base/emitter (Fig. 69 l)).

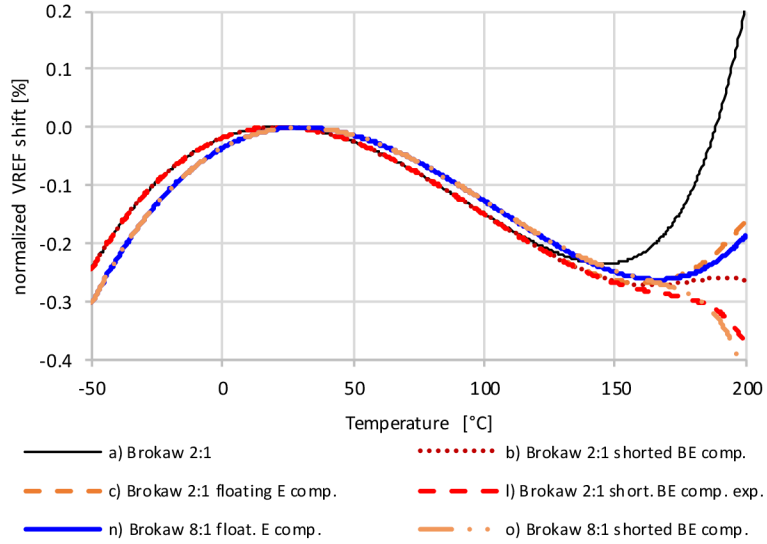


Fig. 70: Comparison of different collector leakage compensations [53].

Fig. 70 shows the resulting temperature drifts of Brokaw cores with different leakage compensations. The leakage compensation for the Brokaw 2:1 core (marked as the "Brokaw 2:1 short. BE comp.") shows a higher effect on the temperature drift than the version marked as the "Brokaw 2:1 float. E comp." due to the higher effect of a collector-base (CB) junction leakage. The CB leakage in the shorted BE compensation version flows directly to the emitter due to the shorted BE junction. When this emitter is connected to the emitter voltage divider, then the leakage influences the voltage ratio in the desired way resulting in a smaller temperature drift for temperatures above 150 °C. This effect was proven by a simulation where the emitter of the compensation BJTs was decoupled from the divider and maintained the same voltage conditions by the VCVS (Fig. 69 l)). The resulting temperate drift is marked as the

"Brokaw 2:1 short. BE comp. exp." and shows only one part of the collector leakage compensation effect, which is not sufficient. The experiment proved that the leakage also causes unwanted influence of voltages in the emitter circuit of the Brokaw bandgap core.

The CB leakage in the Brokaw 2:1 core with floating emitter compensation (see Fig. 65 f)) flows only to the base of the BJTs and impacts the voltage on the positive input of the OPA. This compensation method shows a little bit of temperature drift improvement, and it can be said that it does not completely compensate for the leakage effect. Both leakage compensation methods of the Brokaw 8:1 core also show their essence, especially for the compensation method marked as the "float. E comp.". Nevertheless, this method significantly increases the layout area to 16 BJTs, and they are very difficult to lay out fully symmetrically. The detailed temperature drifts of the Tsividis 2:1 bandgap core experiments are shown in Fig. 71.

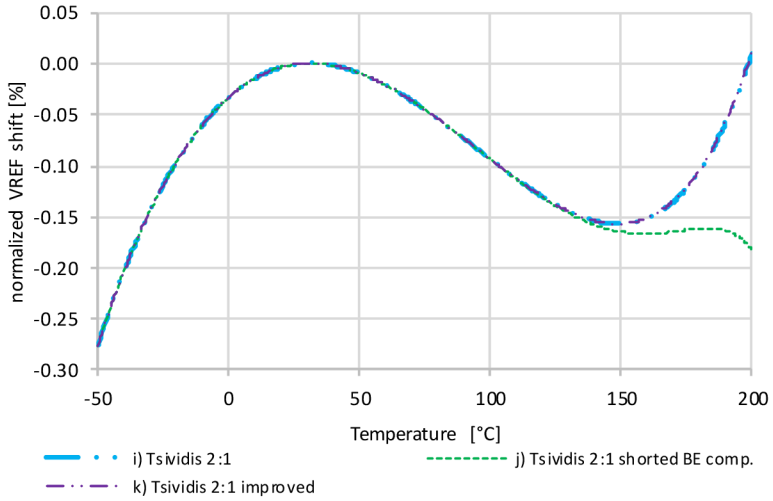


Fig. 71: The temperature drifts of Tsividis 2:1 cores [53].

It must be noted that the proposed Tsividis 2:1 bandgap core has a little leakage current effect caused by unbalanced CB junction leakage currents. These currents flow into the emitter circuit through BJT bases and influence the PTAT voltage. This effect can be minimized by the shorted BE leakage compensation (Fig. 69 j)). The Tsividis 2:1 core has low-temperature drift and an even smaller drift with the proposed leakage compensation [53].

4.4.7. Sensitivity to the OPA Input Offset

The reference voltage sensitivity to the OPA input offset is investigated by adding a voltage source in series to the OPA noninverting input. The voltage source models the input offset. The input offset from 0 to 10 mV is chosen, close to real values. The relative reference voltage sensitivities to the OPA input offset of proposed bandgap cores without leakage current compensations were analyzed at room temperature 27 °C. The resulting sensitivities are shown in Fig. 72.

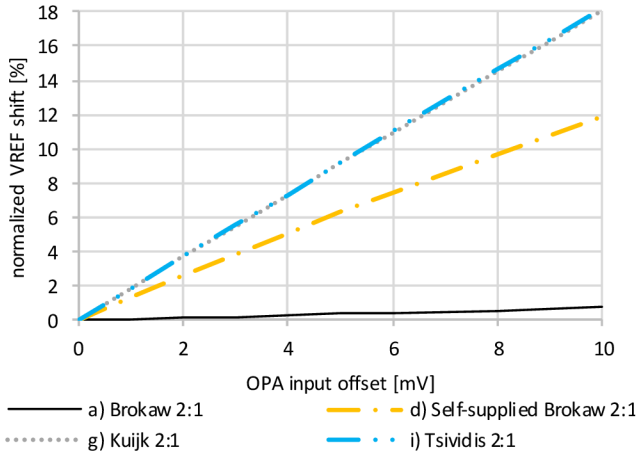


Fig. 72: The OPA input offset sensitivity of proposed bandgap cores at 27 °C temperature [53].

The Kuijk and Tsividis cores show high sensitivity to the OPA input offset. This behavior is expected due to the direct influence of the PTAT voltage. The self-supplied Brokaw 2:1 core shows medium sensitivity with a small nonlinearity caused by the saturation effect of the BJTs due to influenced voltage drops on collector resistors. For these bandgap cores, an OPA offset cancellation technique is recommended, e.g., chopping [64]. The Brokaw 2:1 core has low sensitivity to the OPA offset because there is a higher voltage drop across the collector resistors than in the self-supplied Brokaw, which means that a low offset has less impact on collector current errors.

4.4.8. Line Regulation

The supply line regulation simulation of proposed bandgap cores, using the OPA model from section 4.4.4, was done for a supply range from 2 V to 4 V and a temperature of 27 °C. The output voltage of each proposed bandgap core was normalized to its reference value at a 3 V supply. However, it should be noted that the resulting line regulations are worse in the case of a real OPA. Here, only bandgap core contributors are visible. The line regulations with the OPA model are shown in Fig. 73.

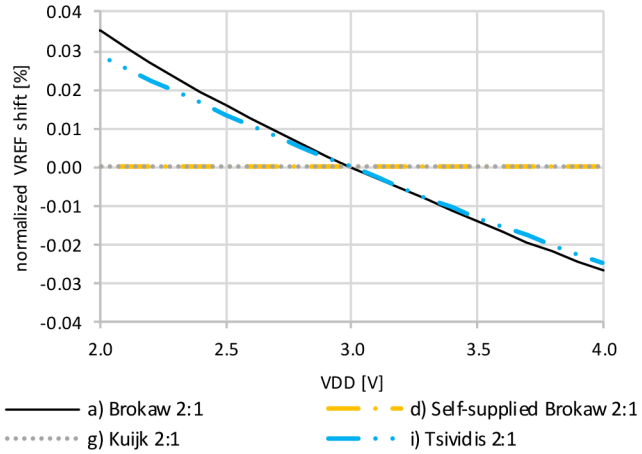


Fig. 73: Line regulations of VREFs at 27 °C temperature [53].

The Kuijk and the self-supplied Brokaw cores show ideal results with no VREF change as expected. Line regulations of these cores depend on the chosen OPA circuit, which supplies the mentioned cores. In this case, there is the OPA model without VDD supply coupling. The Brokaw and Tsividis cores, which they have VDD supply, have almost the same line regulation below 0.04 %. The Tsividis core has lower regulation than the Brokaw core.

4.4.9. Reference Voltage Noise

Fig. 74 shows output voltage noises for each proposed bandgap core. The Brokaw 6:3 with Brokaw 8:1 have the lowest noise from proposed cores. The Brokaw 2:1 has medium noise. Kuijk 2:1 and Tsividis 2:1 have the highest output noise. The 1/*f* noise is given by collector current densities of BJTs. If a higher count of BJTs in each branch of the core is used, the output 1/*f* noise is lower [53].

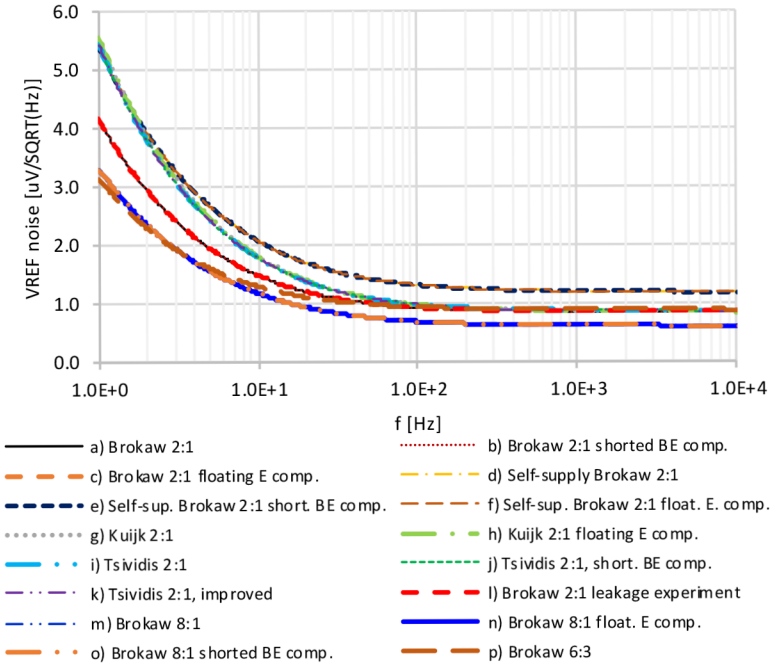


Fig. 74: The voltage noises of proposed bandgap cores [53].

4.4.10. EMI Susceptibility

The EMI susceptibility simulation was performed as transient envelope analysis with fifteen harmonics by Cadence Spectre RF simulator. The simulation results are post-processed after the circuit settles for the VREF DC and the first harmonic for each selected bandgap core. The Brokaw cores with both leakage current compensations and the Tsividis bandgap cores were compared [53]. The EMI susceptibility results as relative VREF DC voltage shifts are shown in Fig. 75.

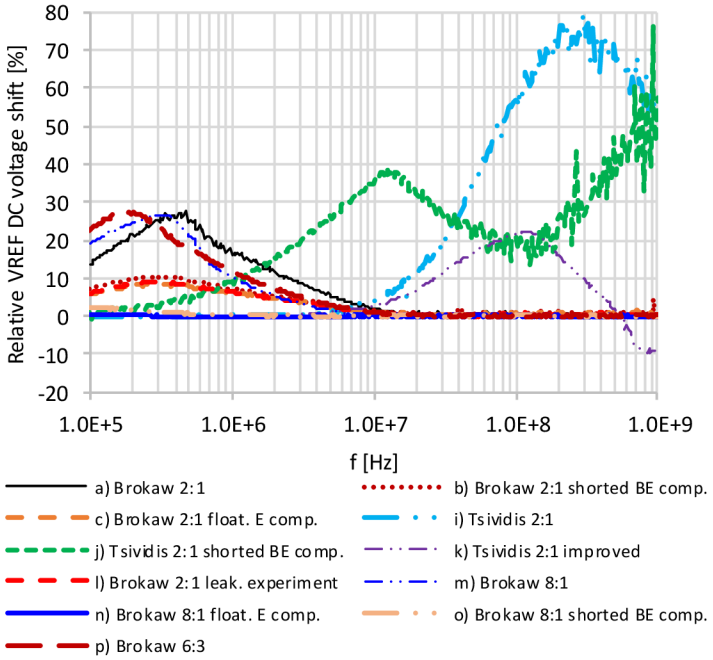


Fig. 75: Relative VREF DC voltage shifts of the selected bandgap cores induced by the 1 V peak sinusoidal HF EMI on the VDD supply with 3 V DC [53].

The Brokaw 2:1 and 8:1 cores without leakage current compensation have medium EMI susceptibility due to unbalanced time constants defined by the collector resistors and BJT collector to VSS capacitances. When the floating emitter leakage current compensation (marked as the "float. E comp.") is used, the collector RC time constants are balanced for Brokaw cores. The leakage current compensation with shorted BE (marked as the "shorted BE comp.") also shows influence by the CB junction capacitance. While this version is good for low-temperature drift, the EMI susceptibility shows slightly unbalanced collector time constants resulting in a slightly higher voltage shift. Both leakage compensations show a low rectification effect, which causes reference voltage shifts due to collector capacitances balancing at the OPA inputs. An effect of different collector resistors for Brokaw 2:1 with balanced BJT capacitors (Fig. 75 c)) can be seen in a frequency range from 100 kHz to 10 MHz. This is caused by the resistor's parasitic capacitance between its poly layer and the well below, which is connected to VSS. When the collector resistors are the same, they have the same parasitic capacitance. These resistors with balanced BJT capacitors cause a very low reference voltage shift, as can be seen for Brokaw 8:1 core with floating emitter leakage compensation (Brokaw 8:1 float. E comp. in Fig. 75 n)) [53].

The Tsividis 2:1 cores have high EMI susceptibility caused by the CB junction capacities. These capacities are effective at a higher frequency than 1 MHz. These capacities, together with the BJT capacities and emitter resistances, create unbalanced RC networks, which result in pass band rectification of the HF interference on the VDD supply. The Tsividis 2:1 improved core by approximately balanced RC networks shows lower EMI susceptibility (Fig. 75 k)) as was expected. A power supply rejection ratio (PSRR) of selected bandgap cores within EMC susceptibility analyses was investigated as well. The reference voltage PSRR of each selected core is calculated from the first harmonic voltage amplitude using the following equation

$$VREF\_PSRR = 10\,log\left(\frac{\Delta V_{VDD}^2}{\Delta V_{ref}^2}\right) = 20\,log\left(\frac{\Delta V_{VDD}}{\Delta V_{ref}}\right), \tag{69}$$

where ΔV_{VDD} is a change in the VDD supply, and ΔV_{ref} is a change in the reference voltage. The changes as first harmonic voltage amplitudes were considered [53]. The VREF PSRRs of selected bandgap cores are shown in Fig. 76.

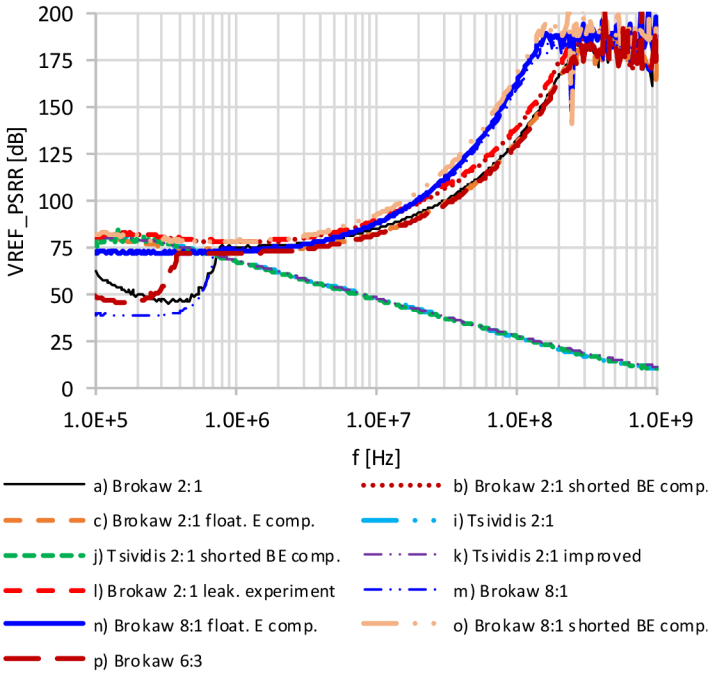


Fig. 76: The PSRR of the selected bandgap cores induced by the 1 V peak sinusoidal HF EMI [53].

The VREF PSRRs of the selected bandgap cores reflect behaviors of relative VREF DC voltage shifts from Fig. 75. The unbalanced collector RC time constants of the Brokaw cores without leakage current compensation cause a small OPA input differential voltage that is amplified by the OPA. This amplified AC voltage is added to the voltage reference resulting in lower PSRR. It must be noted that the OPA model has a 1 MHz unity gain bandwidth. The leakage current compensation balances the collector RC time constants and results in higher PSRR in a frequency range from 100 kHz to 1 MHz. The Tsividis cores have low PSRR at higher frequencies above 1 MHz due to VDD coupling to the output through CB junction capacities [53].

Study results of proposed bandgap cores include temperature coefficients calculated from temperature drifts, relative sensitivities to OPA offset, relative line regulations in VDD range from 2 V to 4 V, output voltage noise, mismatch, and relative voltage DC shifts with PSRRs within EMI susceptibility analyzes. It must be noted that the self-supplied Brokaw and Kuijk cores were supplied from the ideal OPA model (see Fig. 66), which is not dependent on VDD supply like a real OPA. For this reason, the line regulation and EMI susceptibility with PSRR results are not included in this table because the results are dependent on the parameters of the used OPA. These results are in the following summary table Tab. 11.

Tab. 11. Comparison of proposed bandgap cores [53].

Proposed bandgap cores	Parameters							
	No. of BJTs [-]	TC [ppm/°C]	Sensitivity to OPA offset [%/mV]	Line regulation [%]	Voltage noise at 1 Hz [µV/√Hz]	mismatch 6 sigma [mV]	DC shift induced by HF EMI on VDD max. [%]	PSRR min. [dB]
a) Brokaw 2:1	3	18.3	0.07	0.06	4.2	28.5	27.8	44.8
b) Brokaw 2:1, shorted BE comp.	5	10.9	0.07	0.06	4.2	28.5	10.6	77.7
c) Brokaw 2:1, floating E comp.	5	10.7	0.07	0.06	4.2	28.5	8.7	73.2
d) Self-supplied Brokaw 2:1	3	46.5	1.19	NA*	5.4	31.6	NA*	NA*
e) Self-sup. Brokaw 2:1, short. BE comp.	5	66.0	1.19	NA*	5.4	31.6	NA*	NA*
f) Self-sup. Brokaw 2:1, float. E comp.	5	43.2	1.19	NA*	5.4	31.6	NA*	NA*
g) Kuijk 2:1	3	71.8	1.81	NA*	5.6	27.1	NA*	NA*
h) Kuijk 2:1, float. E compensation	5	23.1	1.81	NA*	5.6	27.1	NA*	NA*
i) Tsividis 2:1	3	11.5	1.82	0.05	5.4	28.5	79.9	10.3
j) Tsividis 2:1, shorted BE comp.	5	11.1	1.82	0.05	5.4	28.5	76.8	9.8
k) Tsividis 2:1 with improvements	5	11.5	1.82	0.05	5.4	28.5	22.3	11.1
l) Brokaw 2:1 leakage experiment	5	15.1	0.07	0.06	4.2	28.5	9.0	78.3
m) Brokaw 8:1	9	57.5	0.05	0.06	3.3	15.7	26.7	38.3
n) Brokaw 8:1, float. E compensation	16	12.1	0.05	0.06	3.3	15.7	0.4	71.4
o) Brokaw 8:1, shorted BE comp.	16	17.4	0.05	0.06	3.3	15.7	2.2	77.5
p) Brokaw 6:3	9	39.1	0.08	0.06	3.1	18.2	27.3	45.4

Note that the NA* means not available due to using the ideal OPA model.

4.5. Study of Different Integrated OTA Topologies

Systematical analysis of existing and commonly used integrated OTA topologies was published in the "An EMI Susceptibility Study of Different Integrated Operational Transconductance Amplifiers" paper [65].

Many analog or mixed-signal ICs use integrated OTAs, such as the Miller OTA for example. The OTA transfers differential input voltage to output current and suppresses input common-mode voltage ideally independent of power supply, loading, temperature, and process variations. As an interesting fact, the abbreviation operational amplifier was first published in 1947 within electronic circuits for analysis of problems in the flight dynamics of the airplane [66].

The smaller size, lower power consumption, and higher density when combined with the increasing advent of high-speed mixed-signal and RF devices may result in serious EMC issues. For example, in electromagnetic emission (EME) and electromagnetic susceptibility (EMS), more attention needs to be paid [67]. In most cases, the main Achilles heel in an analog circuit could be the OTA from this perspective. Therefore, the influence analysis of EMI susceptibility on basic OTA topologies is considered a vital task [65].

Many articles focus on fully differential and symmetrical OTA topologies within different types of RF disturbances [68] - [72]. From these references, it can be formulated that if the OTA is fully symmetrical and rectification effects are also symmetrical, then EMI effects will be suppressed. In this study, symmetrical input to single-ended output OTA topologies will be analyzed.

Within the automotive requirements, the following criteria were selected for the analysis of the basic OTA topologies: open-loop gain with circuit stability over a wide temperature range from -50 °C to 200 °C and low EMI susceptibility over wide high frequency (HF) range from 100 kHz to 1 GHz [65].

The main principle of OTAs is to transfer input differential voltage to the output current. The input common-mode voltage is ideally completely suppressed. The following basic equation describes the OTA output current

$$i_{OUT} = (v_{INP} - v_{INN})gm_{Diff} + \frac{v_{INP} + v_{INN}}{2} gm_{CM}, \tag{70}$$

here gm_{Diff} is a differential transconductance, and gm_{CM} is a common mode transconductance that should be equal to zero in the ideal case. At the output of the OTA, here can be seen an output voltage due to the OTA output resistance r_{OUT} as follows

$$v_{OUT} = i_{OUT} r_{OUT}. \tag{71}$$

The OTA output resistance has an ideally infinite value. In reality, the value is defined by the output resistance of the output transistors, which forms an OTA output stage. From the above, the OTA has differential voltage amplification A_{Diff} and common mode voltage amplification A_{CM} which are described by the following equations

$$A_{Diff} = r_{OUT} gm_{Diff}, \tag{72}$$

$$A_{CM} = r_{OUT} gm_{CM}. \tag{73}$$

From the above-mentioned equations, it would be good to maximize the gm_{Diff} and minimize gm_{CM} to obtain a nearly ideal OTA with high A_{Diff} gain in the design. It can be achieved by maximizing the intrinsic output resistance of a MOS transistor, which is given by the following equation

$$r_{OUT\_Mx} = \frac{1}{\lambda I_{D\_Mx}}, \tag{74}$$

where $I_{\mathrm{D\_Mx}}$ is the drain pinch-off current, and λ is the channel length modulation factor. Within weak inversion, the following equation for MOS drain current can be written

$$I_{D\_Mx} = \frac{W}{L} I_0 e^{\frac{V_{GS\_Mx}}{nV_T}}. \tag{75}$$

In (75), W and L are the width and length of the MOS channel. The I_0 is a DC current when the aspect ratio W/L is equal to one and the gate-source voltage $V_{\mathrm{GS\_Mx}}$ is equal to zero volts. The n is the subthreshold slope factor given by $1 + C_{\mathrm{D}}/C_{\mathrm{OX}}$, where C_{D} is the channel-bulk depletion capacitance, and C_{OX} is the gate-oxide capacitance. Typical values of n are in the range from 1.3 to 1.5. The V_{T} is the well-known thermal voltage that is directly proportional to temperature T, $V_{\mathrm{T}} = kT/q$. From these equations, the drain current $I_{\mathrm{D\_Mx}}$ is not dependent on the threshold voltage V_{TH} of the MOS transistor, and temperature is an important design parameter in weak or moderate inversion circuits. Moderate inversion occurs when the effective voltage $V_{\mathrm{GS}} - V_{\mathrm{TH}}$ is approximately less than 80 mV. Weak inversion occurs when the effective voltage is less than 20 mV. These two regions offer a high gain with low power consumption, but they are not generally used due to low speed [73].

The bandgap voltage reference does not need high-speed OTAs, and therefore the study is focusing on low-speed, for all practical purposes, DC operation OTAs. A bias current of 100 nA is chosen with respect to the leakage current that rises from 1 nA to tens of nA in the temperature range from 150 °C up to 200 °C. All proposed OTAs are designed in 180 nm BCD technology.

4.5.1. Simple NMOS OTA

There are several well-known basic topologies for OTAs. The first chosen basic topology is a simple OTA with an NMOS differential pair, which is shown in Fig. 77.

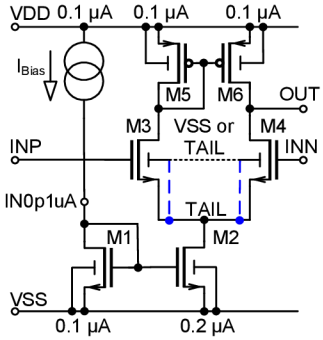


Fig. 77: Simple NMOS OTA [65].

This simple OTA consists of an NMOS differential pair, M3 and M4, based on the topology known since 1947 [74] with a PMOS current mirror, M5, and M6, which acts as an active load. The NMOS differential pair is supplied by an NMOS current mirror, M1 and M2, that sets an OTA operating point. This study includes a connection effect analysis of input differential pair bulks (back-gates) where influence on the EMI susceptibility is expected. Therefore, classical connections of back-gates are depicted by a pointed line and connections to a TAIL node by a dashed line in OTA circuits [65].

4.5.2. Simple PMOS OTA

The second chosen topology is the simple OTA with PMOS differential pair as opposite topology to the simple NMOS OTA. The OTA is shown in Fig. 78.

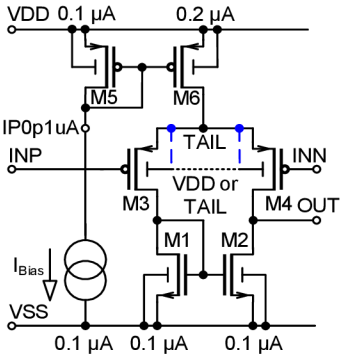


Fig. 78: Simple PMOS OTA [65].

This simple PMOS OTA consists of PMOS differential pair M3 and M4 with the NMOS current mirror M1 and M2, which acts as the active load. The PMOS differential pair is supplied by the PMOS current mirror M5 and M6, which sets the OTA operating point [65].

4.5.3. Miller PPDAL OTA

The third chosen topology is the well-known Miller OTA with an output PMOS pass device loaded by active load (PPDAL). This OTA is shown in Fig. 79.

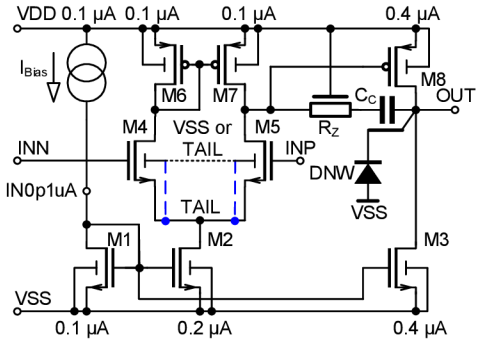


Fig. 79: Miller PPDAL OTA [65].

This Miller PPDAL OTA consists of two stages. The first stage is the NMOS differential pair M4 and M5 with the PMOS active load M6 and M7. The second stage consists of PMOS pass device M8 with active load M3 which is a part of the NMOS current mirror M1, M2, and M3. This current mirror sets the operating points of both stages.

Due to the two stages' topology, there is a frequency compensation by an internal dominant pole. The dominant internal pole is set by a Miller capacitance, whose value includes the OTA second stage gain with a C_C MOS type compensation capacitor placed in an N-type well. This well is depicted as a *DNW* diode. The same effect, which was first published by John M. Miller in 1920 [75], is used there. The C_C capacity is amplified by M8 and is part of an input impedance of the OTA second stage. Additionally, there is an R_Z resistor with a higher value than $1/gm_{M8}$ to maintain a frequency zero position on the left side of the Laplace complex plane, which would result in a wanted signal phase [65].

4.5.4. Miller NPDAL OTA

The fourth chosen topology is Miller OTA with an output NMOS pass device loaded by active load (NPDAL) as the opposite topology to the Miller PPDAL OTA. The Miller NPDAL OTA is shown in Fig. 80.

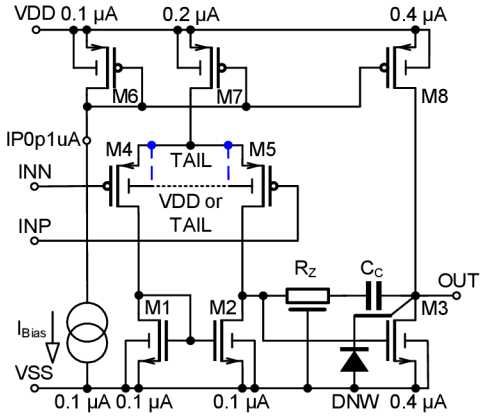


Fig. 80: Miller NPDAL OTA [65].

This Miller NPDAL OTA consists of two stages. The first stage is the PMOS differential pair M4 and M5 with the NMOS active load M1 and M2. The second stage consists of NMOS pass device M3 with active load M8 which is a part of the PMOS current mirror M6, M7, and M8. This current mirror sets the operating points of both stages. There is the same internal frequency compensation as for the Miller PPDAL OTA in chapter 4.5.3.

4.5.5. Folded NMOS Cascode OTA

The fifth chosen topology is a well-known folded NMOS cascode OTA with an NMOS input differential pair. This OTA is shown in Fig. 81.

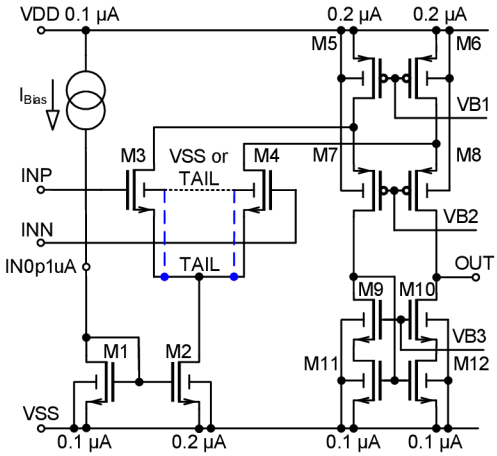


Fig. 81: Folded NMOS cascode OTA [65].

This folded cascode OTA consists of one stage, even though it appears that there are two stages. The one stage includes the NMOS differential pair M3 and M4 with the PMOS active load M5 and M6 and cascode transistors M7 and M8 with its active load M9 – M12 as a cascoded current mirror. The NMOS differential pair is supplied by an NMOS current mirror M1 and M2 that sets an OTA operating point. The main advantages of this topology, besides high voltage gain, are frequency stability over a wide frequency range without internal frequency compensation and symmetrical loading of the differential pair [65].

4.5.6. Folded PMOS Cascode OTA

Finally, the sixth chosen topology is folded PMOS cascode OTA with PMOS input differential pair as opposite topology to Folded NMOS cascode OTA. The folded PMOS cascode OTA is shown in Fig. 82.

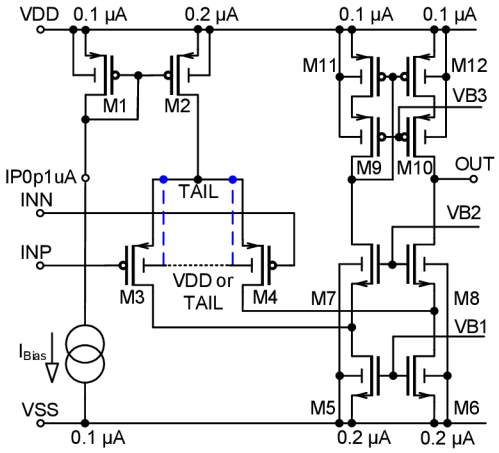


Fig. 82: Folded PMOS cascode OTA [65].

This one-stage folded PMOS cascode OTA includes the PMOS differential pair M3 and M4 with the NMOS active load M5 and M6 and cascode transistors M7 and M8 with its active load M9 – M12 as the cascoded current mirror. The PMOS differential pair is supplied by the PMOS current mirror M1 and M2, which sets the OTA operating point [65].

4.5.7. OTA Parameters

Each of the chosen OTA structures was analyzed for its AC open loop gain characteristic and input random offset. A C_{Load} load capacitor was chosen 1 pF representing on-chip load only. According to the OTA open loop gain simulation results, all OTAs are frequency-stable with sufficient open loop gains. The following tables show the basic parameters of all proposed OTAs under typical conditions: VDD = 3.1 V, temperature = 27 °C.

Tab. 12. Typical parameters of all proposed OTAs [65].

OTA topology	Offset 6σ [mV]	A_{Diff_OL} [dB]	f_{DP} [Hz]	UGBW [kHz]	PM [deg]
a) Simple NMOS	8.6	58.0	457.2	360.2	85.4
b) Simple PMOS	7.5	63.4	188.8	271.3	81.4
c) Miller PPDAL	7.8	121.9	0.1	132.7	61.8
d) Miller NPDAL	7.4	122.4	0.2	237.0	64.2
e) Folded NMOS cascode	8.4	111.7	0.9	360.7	71.5
f) Folded PMOS cascode	8.9	109.2	1.0	277.6	71.1

Tab. 13. Variations of parameters of proposed OTAs within 512 Monte-Carlo runs with mismatch and process variations [65].

OTA topology	A_{Diff_OL} 6σ [dB]	f_{DP} 6σ [%]	UGBW 6σ [%]	PM 6σ [%]
a) Simple NMOS	0.2	8.1	7.9	0.7
b) Simple PMOS	0.3	5.0	3.8	1.1
c) Miller PPDAL	0.4	17.9	14.7	10.6
d) Miller NPDAL	0.4	17.4	14.1	6.7
e) Folded NMOS cascode	0.7	5.8	7.2	2.3
f) Folded PMOS cascode	0.4	4.1	2.8	1.5

All presented OTAs have acceptable random input offsets less than 10 mV and UGBW higher than 100 kHz. Additionally, the mismatch and process Monte-Carlo simulation with 512 runs shows low variations. The simple NMOS and PMOS OTAs have small open-loop gains, which impact a systematic input offset. The Miller PPDAL, Miller NPDAL, folded NMOS, and PMOS cascode have much higher open loop gains, which results in a low input differential voltage and better linearity. If the considered input differential voltage can be 1 mV for 1.5 V output voltage within OTA as the voltage follower, then the open loop gain shall be higher than

$$A_{Diff\_OL} = 20\,log\frac{V_{OUT}}{V_{DiffIN}} = 20\,log\frac{1.5}{0.001} = 63.5\,dB. \tag{76}$$

The parameters for all proposed OTAs were also investigated in the junction temperature range from -50 to 200 °C. Tab. 14 shows temperature variations.

Tab. 14. Variations of parameters for proposed OTAs within junction temperature from -50 to 200 °C [65].

OTA topology	ΔA_{Diff_OL} [dB]	Δf_{DP} [%]	ΔUGBW [%]	ΔPM [%]
a) Simple NMOS	5.6	2.9	61.8	1.4
b) Simple PMOS	3.7	8.6	48.1	0.4
c) Miller PPDAL	7.4	16.6	63.7	2.7
d) Miller NPDAL	9.9	76.2	44.7	21.6
e) Folded NMOS cascode	9.0	43.3	62.3	4.6
f) Folded PMOS cascode	7.9	48.7	47.9	1.4

The temperature variation of open loop gain is higher than its mismatch and process variation because the weak inversion of a MOS transistor is more temperature-dependent than the strong inversion, which is generally more sensitive to process variation. The resulting temperature dependencies are not critical for a DC application.

4.5.8. Supply EMI Susceptibility

The OTA supply EMI susceptibility was analyzed by using the following simulation schematic shown in Fig. 83.

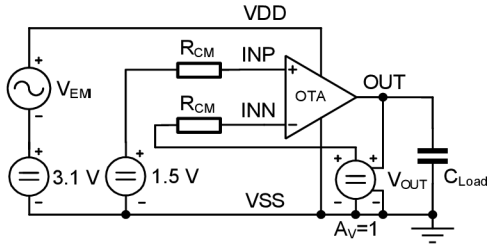


Fig. 83: The OTA supply EMI susceptibility simulation schematic with the isolated output [65].

The OTA connection as a non-inverting voltage follower was chosen with a 1.5 V DC input voltage and 3.1 V DC supply voltage. The V_{EMI} is a sine wave voltage source with a sweeping frequency f for EMI susceptibility investigations. The R_{CM} input common mode resistors are chosen with a value of 100 kOhm as ideal internal impedance without unwanted capacity to its well. It must be noted that the C_{Load} load capacitor is chosen 1 pF representing the on-chip load like for the simulations of the OTA basic parameters. EMI susceptibility simulations were performed with a 1 V peak sine wave as transient envelope analysis with the Cadence Spectre RF simulator. After the circuit settling, all simulation results are post-processed for the DC shift and the first AC harmonic for each OTA version. Standard small-signal AC simulation was performed as well.

The large and small signal PSRRs of each OTA version were extracted within the supply EMI susceptibility simulations. The output PSRR of each OTA was calculated from the first harmonic voltage amplitude using the following equation

$$PSRR = 10\,log\frac{\Delta V_{VDD}^2}{\Delta V_{OUT}^2} = 20\,log\frac{\Delta V_{VDD}}{\Delta V_{OUT}}, \tag{77}$$

Where ΔV_{VDD} is a voltage change in the VDD supply, and ΔV_{OUT} is a change in the output voltage. These changes are the first harmonic voltage amplitudes as in [53]. It is worth noting that the large signal PSRR is from transient simulation, and the small signal PSRR is from linearized AC simulation. The summary results will be shown later in chapter 4.5.10.

4.5.9. Common Mode EMI Susceptibility

The OTA input common mode (ICM) EMI susceptibility was analyzed by using the following simulation schematic shown in Fig. 84.

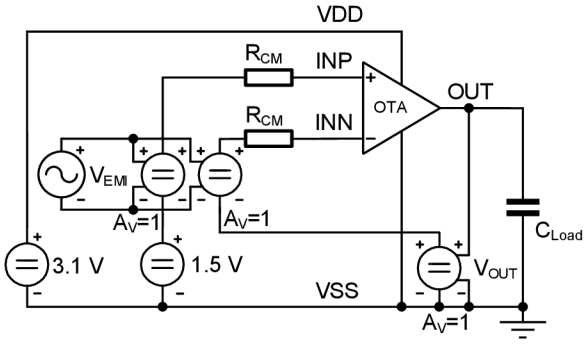


Fig. 84: The OTA ICM EMI simulation schematic with the isolated output [65].

The OTA connection used in the supply EMI susceptibility analysis (see chapter 4.5.8) was also used here, with an input common mode AC excitation as in [51]. The excitation and simulations are identical to those used in the previous chapter 4.5.8.

The large and small signal input CMRRs of each OTA version were extracted within ICM EMI susceptibility simulations. The CMRR of each OTA was calculated from the first harmonic voltage amplitudes using the following equation

$$CMRR = 10\,log\frac{\Delta V_{INCM}^2}{\Delta V_{OUT}^2} = 20\,log\frac{\Delta V_{INCM}}{\Delta V_{OUT}}, \tag{78}$$

where ΔV_{INCM} is a change of the input common-mode voltage, and ΔV_{OUT} is a change of the output voltage. These changes are the first harmonic voltage amplitudes, as in chapter 4.5.8. It is worth noting that the large signal CMRR is from transient simulation, and the small signal CMRR is from linearized AC simulation. The summary results will be shown next in chapter 4.5.10.

4.5.10. Summary of OTA EMI Susceptibility Results

The achieved results of OTA EMI susceptibility simulations are shown as graphs (Fig. 85 to Fig. 96) on the following pages. These graph arrangements were chosen for clear comparison reasons. It is possible to easily compare the simple NMOS OTA with the simple PMOS OTA, the Miller PPDAL OTA with the Miller NPDAL OTA, and the folded NMOS cascode OTA with the folded PMOS cascode OTA.

The simple NMOS OTA and the simple PMOS OTA graphs (Fig. 85 to Fig. 88) show that the simple NMOS OTA with classically connected back-gates of the input differential NMOS pair has lower supply EMI susceptibility. On the other hand, the simple PMOS OTA with back-gates connected to the differential TAIL node of the input differential PMOS pair has lower supply EMI susceptibility as well. The classical back-gate connection of the PMOS input differential pair to the VDD supply shows higher supply EMI susceptibility due to supply EMI coupling to the simple PMOS OTA input stage. The classical back-gate connection of the NMOS input differential pair to VSS ground shows lower supply and input common-mode EMI susceptibilities due to the higher EMI decoupling effect in the simple NMOS OTA input stage. The small and large signal PSRRs of the simple NMOS OTA are nearly identical, but the small and large signal CMRRs are different, especially in the lower frequency range of up to 100 MHz. The small and large signal PSRRs of the simple PMOS OTA are different due to input stage operating point change which is not seen for the AC small signal analysis within the frequency domain, but the change can be seen for analysis in the time domain with a large signal. The changes in OTA operation points, such as changes in bias currents, are not shown due to the intended scope of this study [65].

The Miller PPDAL OTA and the Miller NPDAL OTA graphs (Fig. 89 to Fig. 92) show supply EMI susceptibility weakness of the Miller PPDAL OTA due to the coupling effect of the C_C compensation capacitor with R_Z resistor (see Fig. 79) of the output PMOS pass device. There is partial coupling supply EMI via a well of R_Z resistor and partially via C_C capacitor. Even more, the C_C capacitor makes an AC short between the output and input of the PMOS pass device, which acts like a diode in a dedicated frequency range. If the well of the R_Z resistor is put from the VDD supply to the VSS ground, then the supply EMI susceptibility is slightly lower, and the maximum DC output shift decreases from 99 % to 25 %, for example. On the other hand, the Miller NPDAL OTA with back-gates of the PMOS input differential pair connected to the differential TAIL node has excellent supply EMI susceptibility. Nevertheless, the Miller NPDAL OTA with classically connected back-gates of the input differential pair has lower input common mode EMI susceptibility. Small and large signal PSRRs and CMRRs are similar to the simple NMOS OTA.

The folded NMOS cascode OTA and the folded PMOS cascode OTA graphs (Fig. 93 to Fig. 96) show that the folded PMOS cascode OTA with classically connected back-gates of the input PMOS differential pair has low supply EMI susceptibility. On the other hand, the folded NMOS cascode OTA with classically connected back-gates of the input NMOS differential pair has low input common mode EMI susceptibility. Small and large signal PSRRs and CMRRs are like simple OTAs [65].

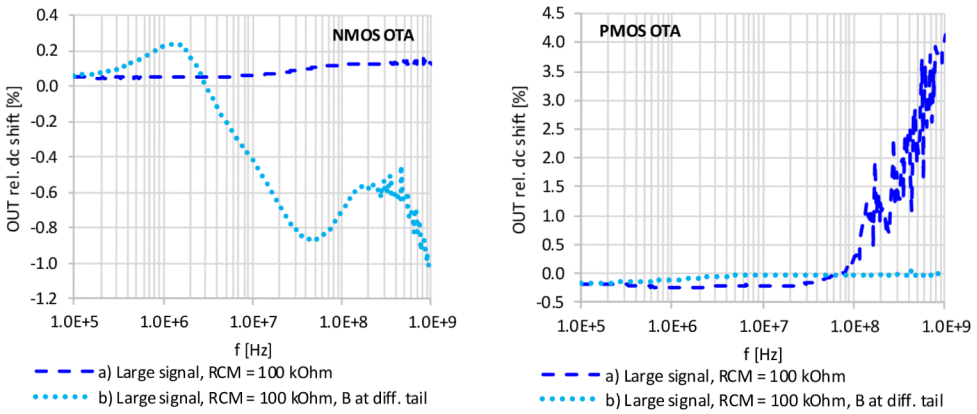


Fig. 85: Simple OTA VDD EMI susceptibilities [65].

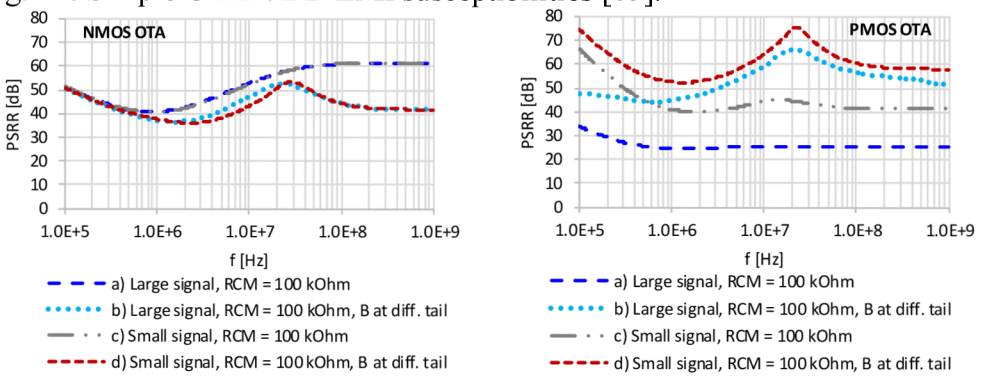


Fig. 86: Simple OTA PSRRs [65].

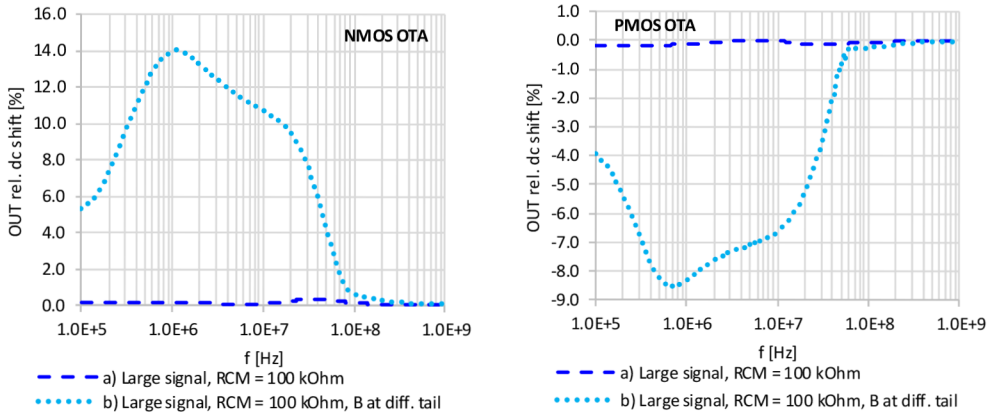


Fig. 87: Simple OTA INCM EMI susceptibilities [65].

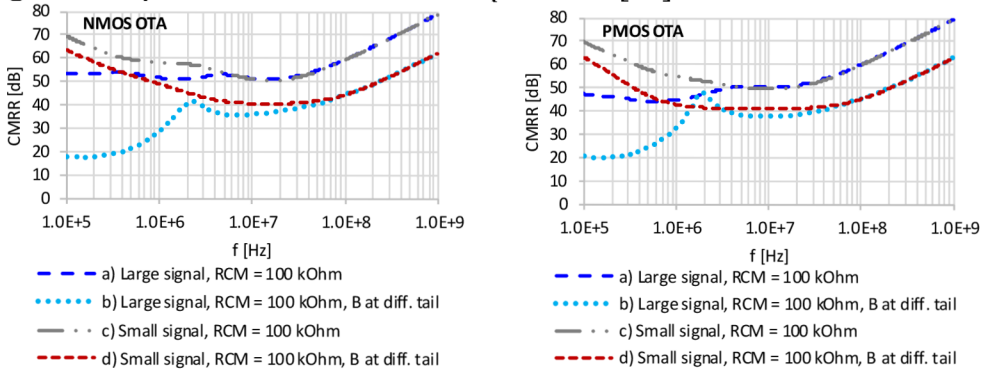


Fig. 88: Simple OTA CMRRs [65].

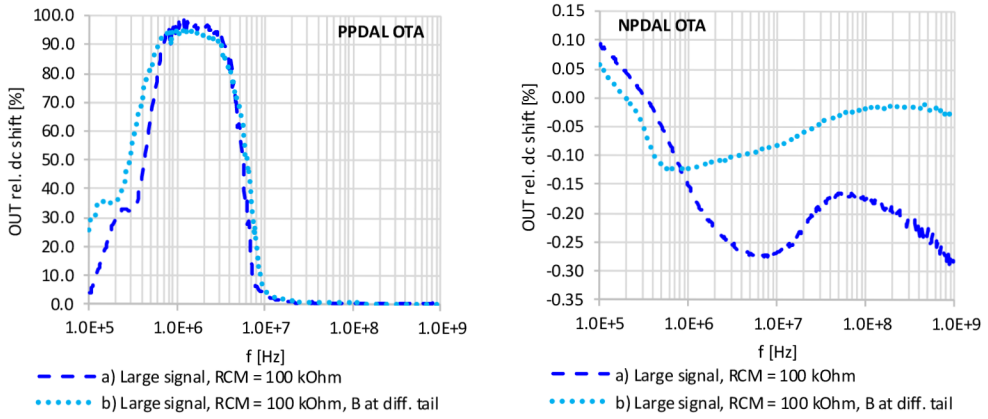


Fig. 89: Miller OTA VDD EMI susceptibilities [65].

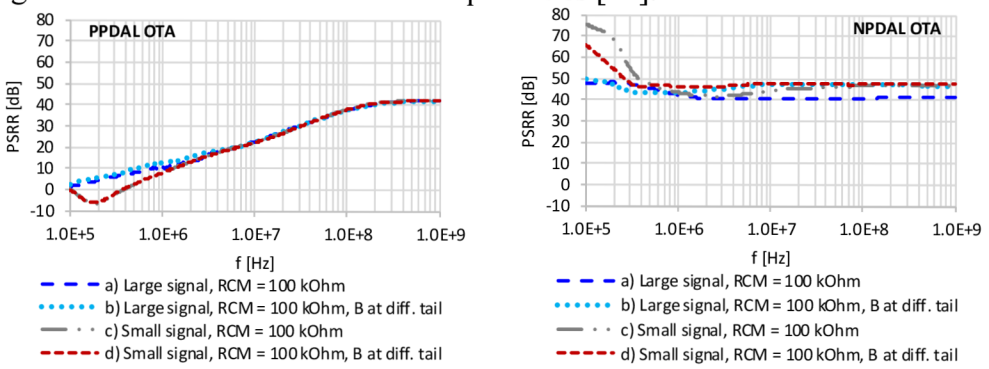


Fig. 90: Miller OTA PSRRs [65].

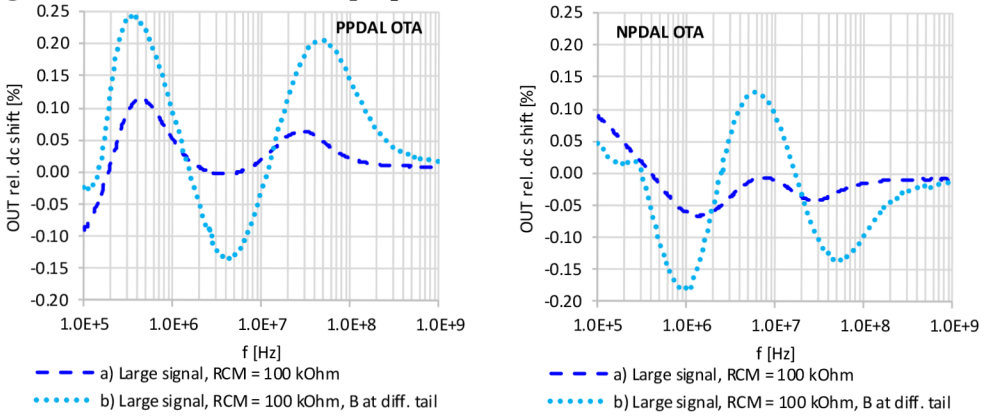


Fig. 91: Miller OTA INCM EMI susceptibilities [65].

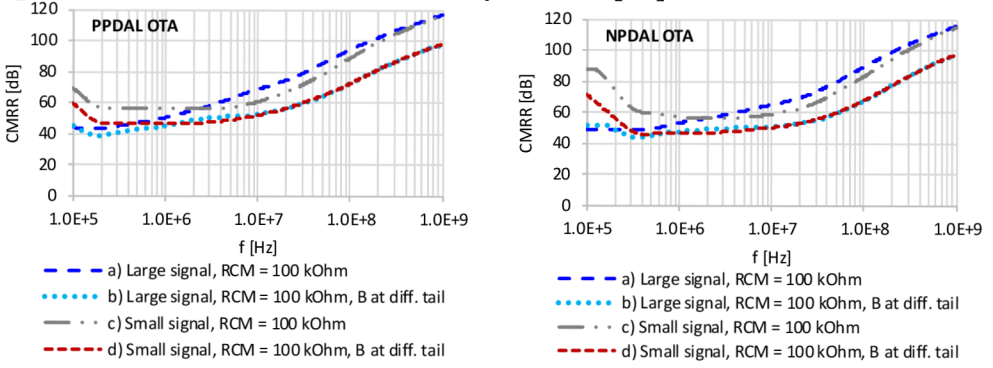


Fig. 92: Miller OTA CMRRs [65].

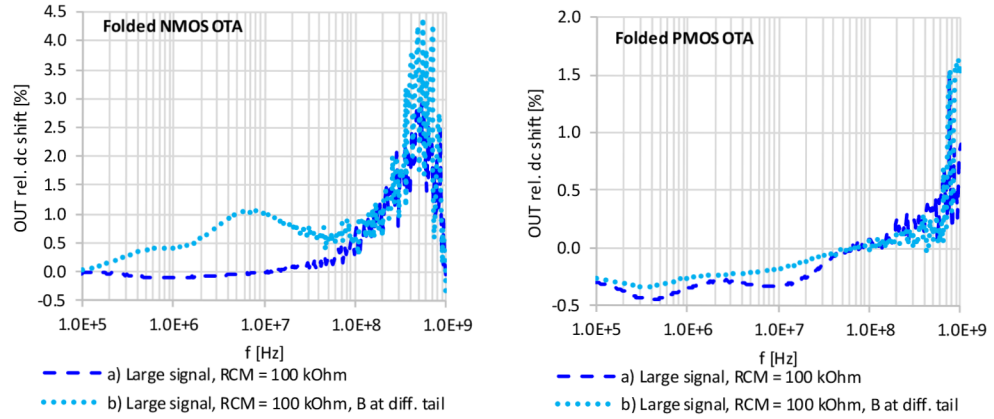


Fig. 93: Folded cascode OTA VDD EMI susceptibilities [65].

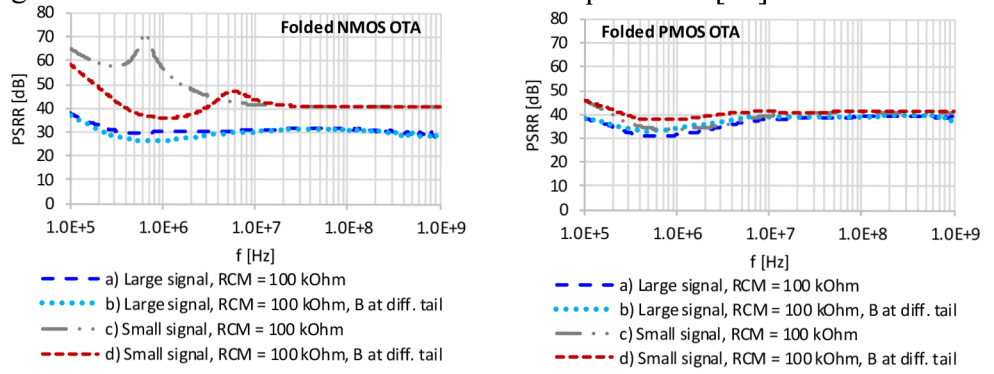


Fig. 94: Folded cascode OTA PSRRs [65].

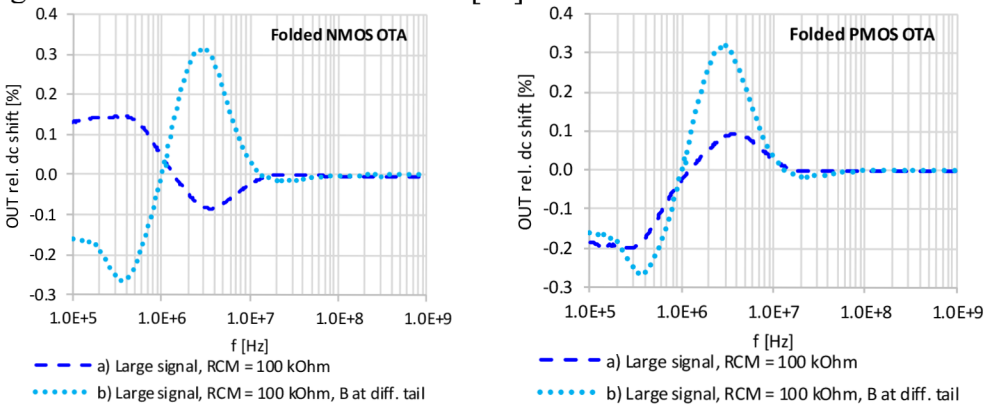


Fig. 95: Folded cascode OTA INCM EMI susceptibilities [65].

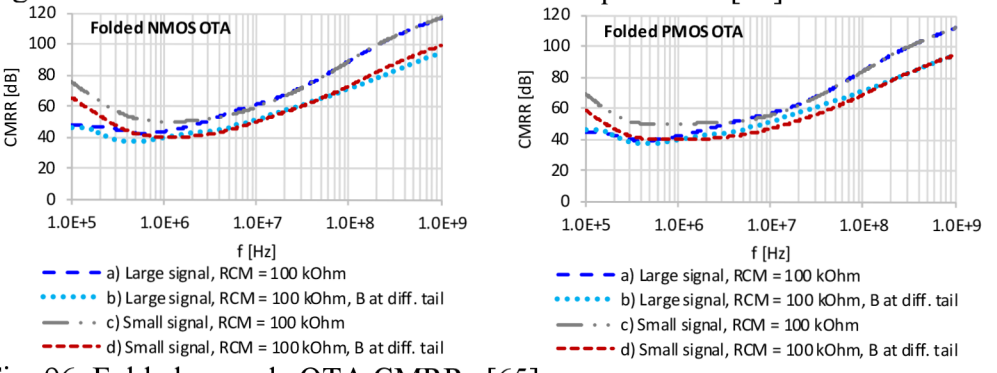


Fig. 96: Folded cascode OTA CMRRs [65].

Tab. 15. EMI susceptibility of the proposed OTAs [65].

EMI signal	Small (AC)				Large (1 V peak)			
EMI for	VDD supply		Input CM		VDD supply		Input CM	
OTA topology	OUT max. DC rel. shift [%]	PSRR min. [dB]	OUT max. DC rel. shift [%]	CMRR min. [dB]	OUT max. DC rel. shift [%]	PSRR min. [dB]	OUT max. DC rel. shift [%]	CMRR min. [dB]
a) Simple NMOS	NA*	40.8	NA*	50.6	0.2	40.8	0.4	51.1
b) Simple PMOS	NA*	40.1	NA*	49.6	4.1	24.9	0.2	44.3
c) Miller PPDAL	NA*	0.0	NA*	55.8	98.6	1.5	0.1	43.0
d) Miller NPDAL	NA*	41.8	NA*	56.0	0.3	40.4	0.1	48.6
e) Folded NMOS cascode	NA*	41.1	NA*	50.1	2.9	28.3	0.1	42.5
f) Folded PMOS cascode	NA*	34.0	NA*	49.9	1.5	30.8	0.2	39.1

Tab. 16. EMI susceptibility of the proposed OTAs with back-gates of input MOS pairs at the TAIL node [65].

EMI signal	Small (AC)				Large (1 V peak)			
EMI for	VDD supply		Input CM		VDD supply		Input CM	
OTA topology (back-gates at the TAIL node)	OUT max. DC rel. shift [%]	PSRR min. [dB]	OUT max. DC rel. shift [%]	CMRR min. [dB]	OUT max. DC rel. shift [%]	PSRR min. [dB]	OUT max. DC rel. shift [%]	CMRR min. [dB]
a) Simple NMOS	NA*	36.5	NA*	40.6	1.0	36.1	14.0	17.4
b) Simple PMOS	NA*	52.3	NA*	41.0	0.2	44.3	8.6	20.0
c) Miller PPDAL	NA*	0.1	NA*	46.4	95.4	2.7	0.2	38.9
d) Miller NPDAL	NA*	46.0	NA*	46.0	0.1	43.2	0.2	44.1
e) Folded NMOS cascode	NA*	36.1	NA*	40.1	4.4	26.3	0.3	37.0
f) Folded PMOS cascode	NA*	37.9	NA*	39.9	1.6	33.2	0.3	37.0

Note that the NA* means not available due to the AC (small signal) analysis.

All results within the EMI susceptibility analysis of the proposed OTAs are in the summary tables Tab. 15 and Tab. 16. Tab. 15 shows the EMI susceptibility results of the OTAs with classically connected back-gates of the input differential MOS pair. Tab. 16 shows the EMI susceptibility results of the OTAs with back-gates of the input differential MOS pair connected to the differential TAIL node. Large differences between small and large signal simulations for some cases in both tables lead to a recommendation for PSRR and CMRR simulations. If a large disturbance signal is considered, then one should use the time domain analysis rather than the AC frequency domain analysis in order to avoid skewed results because, for example, the AC analysis does not take into account nonlinearity effects.

This study presented a comparative study of six different integrated OTA topologies. In addition to the presented and discussed EMI susceptibility comparison results, the study also contains new supply and new ICM EMI susceptibility simulation setups with defined input common-mode impedances. The EMI simulation results within large and small excitation signals in time and frequency domains were discussed, as well as the impact of back-gate connections of the input differential MOS pair in the proposed low-power OTAs. The back-gate connection can help to decrease OTA EMI susceptibility in some cases (see Tab. 15 and Tab. 16) [65].

4.6. EMI Susceptibility Improved Voltage Reference

Chapter 4.6 presents the new proposed EMC robust voltage reference with the new EMC robust design methodology based on the outcome of previous analyses.

4.6.1. Selection of the Bandgap Reference Core

Based on the bandgap core EMI susceptibility comparison results in chapter 4.4, the Brokaw 2:1 with floating E leakage compensation was chosen with a 3:2 collector current ratio. This bandgap core has a low-temperature coefficient of about 10.7 ppm/°C in the temperature range from -50 °C to 200 °C with well-basic EMC robustness. The chosen bandgap reference core is shown in the following Fig. 97.

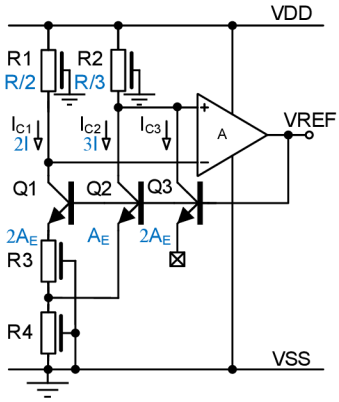


Fig. 97: The chosen bandgap reference core.

4.6.2. OTA Improvements

The OTA, which is a part of the bandgap, highly impacts the EMI susceptibility of the complete voltage reference [17], [76]. In general, the common mode EMI plays an important role there. This type of EMI can be suppressed when the amplifier has a symmetrical input stage with a fully symmetrical load in case of the symmetrical rectification effects [65]. For this reason, a folded cascode OTA was chosen.

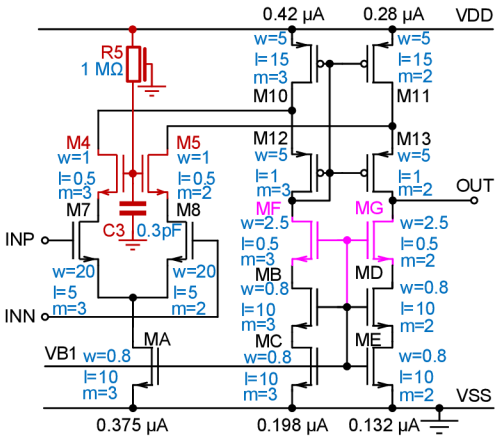


Fig. 98: The proposed one-stage folded cascode OTA.

Fig. 98 shows a circuit diagram of the improved one-stage folded cascode OTA with PMOS and NMOS pseudo-cascode current mirror structures described in [59]. The proposed folded cascode OTA denotes a wide input common mode range (ICMR) from 0.5 to 2.9 V within linearity error below 1 mV, an open loop gain of 85 dB, a unity gain bandwidth of 95.5 kHz with a phase margin of 84° and current consumption of the amplifier is only 0.7 μA. From these parameters, it is evident that the amplifier is designed to tolerate high common mode input voltage, which can be created by EMI in the bandgap core. The wide ICMR is achieved by the M7 and M8 input differential pair with a weak inversion operating point due to high transconductance with low bias current, as was stated in [48] and [65].

Because the bandgap core has asymmetrical collector impedances within the 3:2 collector current ratio, the comparison between a 1:1 fully symmetrical and a novel 3:2 asymmetrical OTA will be investigated. The introduced 3:2 ratio respects the impedance ratio of the bandgap core at the amplifier differential input. The basic folded cascode OTA topology presented in [48] was used as an initial topology. The topology will be improved so the following configurations will be analyzed, refer to Fig. 98:

a) The basic version with simple bias (MB – ME only) and the 1:1 ratio (the same m-factors),

b) The basic version with simple bias and the 3:2 ratio,

c) Bias pseudo-cascodes (MB – MG) within the 3:2 ratio, and

d) Bias pseudo-cascodes with additional input NMOS cascode (M4 and M5) within the 3:2 ratio.

The small signal open loop gains across the different folded cascode OTA configurations are shown in the following Tab. 17.

Tab. 17. Open loop gains of proposed OTA configurations.

OTA configuration	A_{OL} [dB]	UGBW [kHz]	PM [°]
a) Simple bias, 1:1	73.3	117.3	80.8
b) Simple bias, 3:2	71.5	95.5	84.6
c) Bias pseudo-cascodes, 3:2	84.9	95.5	84.4
d) Input cascode added, 3:2	85.0	95.5	84.3

The gain between the fully symmetrical and asymmetrical topologies differs by about 1.8 dB. This is the expected change due to transconductance changes caused by the different bias currents. The configuration with bias pseudo-cascodes brings its benefit, besides the OTA gain increase, in a wider VDD supply voltage room. Finally, the additional input NMOS cascode (M4 and M5 in Fig. 98), whose advantage is in decreasing unwanted coupling capacitances between differential outputs and inputs (described in the next chapter), does not change the gain as expected. The M4 and M5 NMOS cascode ensures operating point invariance of the M7 and M8 differential pair as the M12 and M13 PMOS cascode in previous configurations.

4.6.3. EMI Susceptibility of the OTA

A VDD EMI susceptibility impact on the output voltage of the proposed OTA configurations was investigated by simulations. These simulations were done as transient envelope analyses by the Cadence Spectre RF simulator. The results were post-processed for DC and the first harmonic voltages after circuit settling. A test bench schematic is in Fig. 99, and the achieved results are shown in Fig. 100 a) and b).

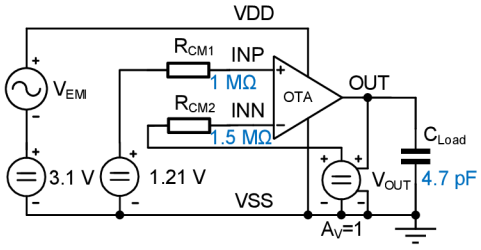
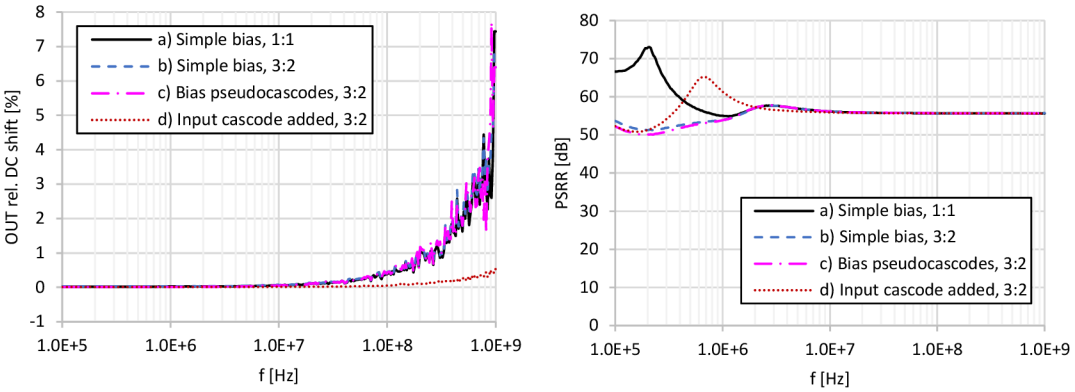


Fig. 99: The VDD EMI susceptibility simulation schematic of the OTA.



a) b)

Fig. 100: The a) DC output voltage relative shifts and b) PSRRs of the OTA configurations with 1 V peak EMI at VDD supply from transient simulation.

The common mode resistors, which are R_{CM1} = 1 MΩ and R_{CM2} = 1.5 MΩ (the same for all test cases), respect the collector impedances of BJTs in the bandgap core. The topology ratio does not affect the dc output voltage shift caused by VDD disturbance because the symmetry ratio between the differential pair and the subsequent cascoding current mirrors is kept in both cases. The best results are achieved for the OTA configuration with the additional input cascode with filtered gate voltage ($R5$, $C3$, M4, and M5 in Fig. 98), which helps to shield the circuit from disturbances on the VDD supply at higher frequencies. From the PSRR point of view, the 1:1 topology causes symmetrical coupling with the result of higher PSRR in the frequency range from 100 kHz to 1 MHz versus the 3:2 topology. For higher frequencies, an output capacitive voltage divider consisting of PMOS, NMOS cascode capacities, and C_{Load} capacity, which is 4.7 pF due to a dominant pole position, is dominant and dictates the final PSRR across all presented configurations. It is clear from the results that additional cascoding of the input differential pair using filtered gate voltage helps to minimize the output DC shift.

The next input common mode (ICM) EMI susceptibility analyses were performed as transient envelope simulations by the Cadence Spectre RF simulator with the result post-processing as well as the VDD EMI susceptibility simulations for each OTA configuration. The simulation schematic of the ICM EMI susceptibility is in Fig. 101, and the achieved results are shown in Fig. 102 a) and b).

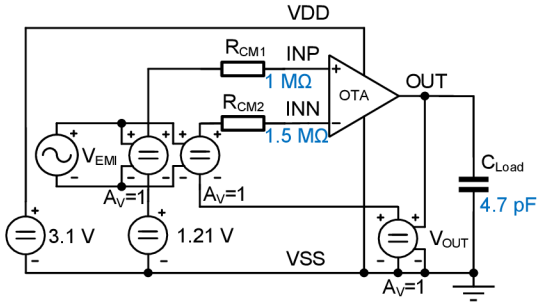
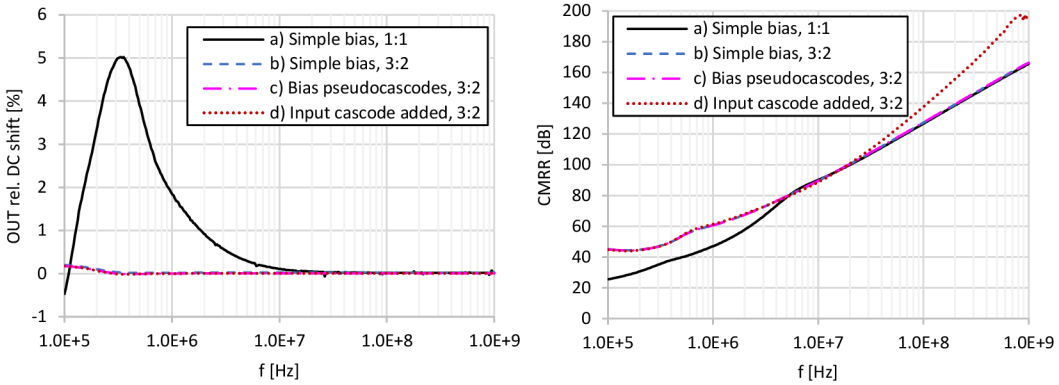


Fig. 101: The ICM EMI susceptibility simulation schematic of the OTA.



a) b)

Fig. 102: The a) DC output voltage relative shifts and b) CMRRs of the OTA configurations with 1 V peak ICM EMI from transient simulation.

The common mode resistors R_{CM1} and R_{CM2} are 1 MΩ and 1.5 MΩ, respectively, representing the bipolar collector impedances. For the 1:1 ratio, a significant DC output voltage shift appears in the lower frequency range because the amplifier input capacitances are not matched with input common mode resistances representing bipolar impedances. The asymmetrical ratio 3:2 of transistors in the amplifier significantly decreases DC output voltage shift and improves CMRR. The additional input cascode further increases CMRR in the higher frequency range.

4.6.4. Bandgap Reference Improvements

Fig. 103 shows the circuit schematic of the proposed voltage reference. The circuit consists of the bandgap core (*R*1–*R*4, *C*1, *C*2, and Q1–Q3), a BJT anti-saturation circuit (M1–M3, M6, and M9), a part of bias circuits (MF–MH), and the asymmetrical OTA (*R*5, *C*3, *C*4, M4, M5, M7, M8, M10–M14 and MA–ME). A startup circuit was omitted for simplification.

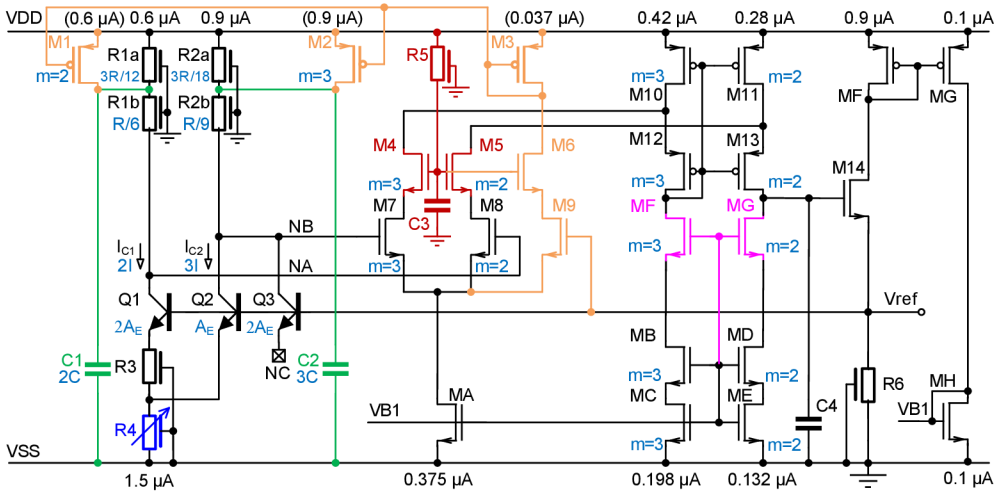


Fig. 103: Simplified circuit schematic of the new proposed bandgap.

The improvements of the voltage reference are discussed as follows. As shown in Fig. 103, *C*1 and *C*2 are used as additional filtration capacitors to minimize the coupling of the VDD supply EMI to the bandgap core. It is more effective to split the collector resistors into two parts and create a second-order filter than just connecting additional capacitors to the collectors. To lower the conversion of the common mode disturbances to differential OTA input signal, it is crucial to match well time constants between the two collector branches. *R*1a, *R*1b, *R*2a and *R*2b resistors together with *C*1, *C*2, C_{CQ1}, C_{CQ23}, C_{GM7} and C_{GM8} capacitors form two second order low-pass filters with time constants τ_{1a}, τ_{2a} and τ_{1b}, τ_{2b}. These time constants can be roughly estimated from node impedances by considering the validity that $C1 > (C_{CQ1} + C_{GM8})$ and $C2 > (C_{CQ23} + C_{GM7})$ as follows:

$$\tau_{1a} \approx R1a \cdot C1 = \frac{3}{12} \cdot R \cdot 2 \cdot C = \frac{1}{2} \cdot R \cdot C, \tag{79}$$

$$\tau_{2a} \approx R2a \cdot C2 = \frac{3}{18} \cdot R \cdot 3 \cdot C = \frac{1}{2} \cdot R \cdot C, \tag{80}$$

$$\tau_{1b} \approx R1b \cdot \left(C_{CQ1} + C_{GM8}\right) = \frac{1}{3} \cdot R \cdot \left(C_{CQ} + C_G\right), and \tag{81}$$

$$\tau_{2b} \approx R2b \cdot \left(C_{CQ23} + C_{GM7}\right) = \frac{1}{3} \cdot R \cdot \left(C_{CQ} + C_G\right). \tag{82}$$

Where C is a design unity capacity, C_{CQ} is an intrinsic unity capacity of the Q1 – Q3 BJT collectors and C_G is an intrinsic unity capacity of the M7 and M8 NMOS transistor gates. The design unity capacity was chosen in the order of a picofarad. To be able to well match the time constants the new asymmetrical OTA mentioned above was proposed. In [48] impact of the mismatch of these capacitances was neglected compared to the values of filtering capacitors. In the case of splitting sensing resistors and placing filtering capacitors between the split resistors, this matching is more important.

It is worth noting that the time constants can be estimated by Bode asymptotic approximation within the magnitude plot as well. In this way, the Bode plot can be approximated by an ideally cascaded transfer function with two real poles as follows:

$$K_{V\_VDDtoCOL1} = \frac{1}{\boldsymbol{s}^2 R1aC1R1b(C_{CQ1}+C_{GM8}) + \boldsymbol{s}[R1aC1 + R1a(C_{CQ1}+C_{GM8}) + R1b(C_{CQ1}+C_{GM8})] + 1}, \quad (83)$$

$$K_{V\_VDDtoCOL2} = \frac{1}{\boldsymbol{s}^2 R2aC2R2b(C_{CQ23}+C_{GM7}) + \boldsymbol{s}[R2aC2 + R2a(C_{CQ23}+C_{GM7}) + R2b(C_{CQ23}+C_{GM7})] + 1}. \quad (84)$$

These transfer functions can be written with substitutions of the time constants:

$$K_{V\_VDDtoCOL1} = \frac{1}{\boldsymbol{s}^2 \cdot \tau_{1a} \cdot \tau_{1b} + \boldsymbol{s} \cdot (\tau_{1a} + \tau_1^* + \tau_{1b}) + 1}, and \quad (85)$$

$$K_{V\_VDDtoCOL2} = \frac{1}{\boldsymbol{s}^2 \cdot \tau_{2a} \cdot \tau_{2b} + \boldsymbol{s} \cdot (\tau_{2a} + \tau_2^* + \tau_{2b}) + 1}. \quad (86)$$

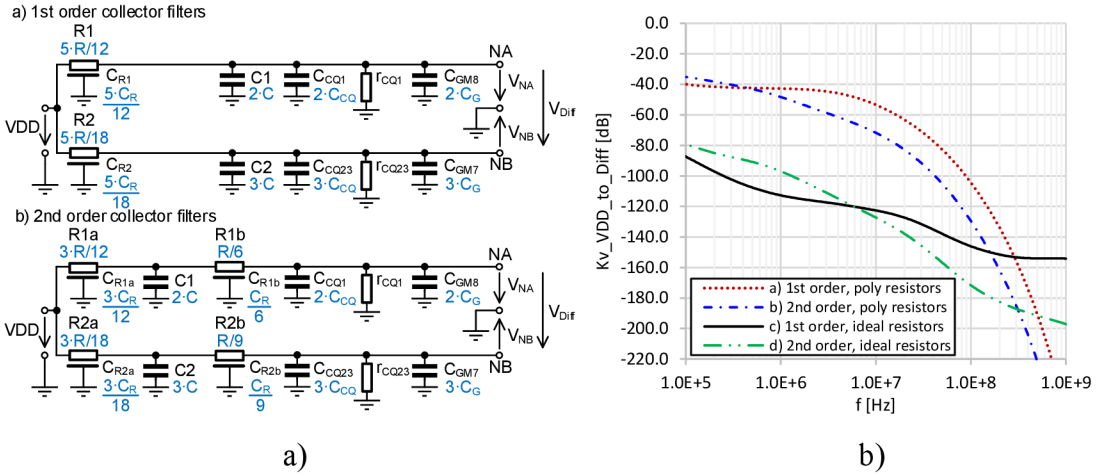
Neglecting the time constants τ_1^* and τ_2^* and put $\boldsymbol{s} = j\omega$, the approximated Bode magnitude plots with two poles are:

$$K_{V\_VDDtoCOL1\_dB} \approx 20 \cdot log \frac{1}{\sqrt{[1 + (\omega \cdot \tau_{1a})^2] \cdot [1 + (\omega \cdot \tau_{1b})^2]}}, \quad (87)$$

$$K_{V\_VDDtoCOL2\_dB} \approx 20 \cdot log \frac{1}{\sqrt{[1 + (\omega \cdot \tau_{2a})^2] \cdot [1 + (\omega \cdot \tau_{2b})^2]}}. \quad (88)$$

Here are the searched time constants (the substitution can be found in the first complex transfer functions) that create different positions of poles. The estimated time constants are the same as for calculations from the node impedances.

R1a – R2b are polysilicon resistors that are placed above a P-well diffusion. The diffusion is connected to the VSS ground, and therefore, the resistors have intrinsic capacitance to the ground. A simplified simulation circuit schematic with two types of collector filters was introduced in order to determine how resistor intrinsic capacitances C_{Rx} influence the matching of time constants and demonstrate the effectiveness of VDD decoupling by second-order filters. The schematic and achieved AC simulation results are shown in Fig. 104.



a) b)

Fig. 104: The a) simplified circuit schematic of collector filters and b) their common mode to differential voltage conversion.

The second-order filters with polysilicon resistors have a lower common mode to differential voltage conversion than the first-order filters in the frequency range from 1 MHz to 1 GHz, and the difference is around 20 dB. Note that this range is mostly used for EMI susceptibility tests. As a reference, filters with ideal resistors (without C_{Rx}) show low common mode to differential conversions impacted only by different BJT resistances r_{CQ1} and r_{CQ23}. It is evident from simulation results that the common mode conversion is negatively impacted by resistor intrinsic capacitances, which are opposite to the required capacity ratio. Within the same occupied area, the second-order filter gives higher common mode rejection.

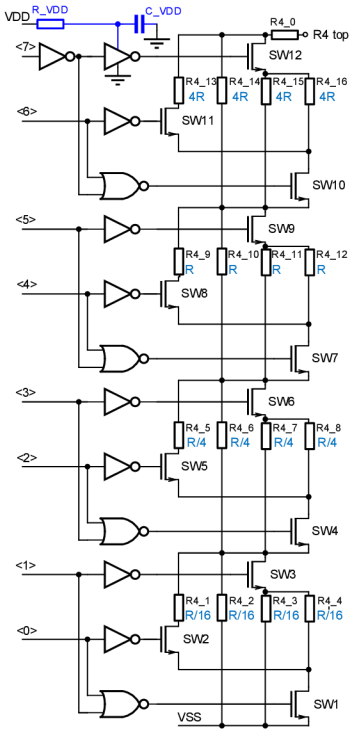


Fig. 105: A resistor *R*4 trimming circuit with filtered VDD supply.

The minimum supply voltage of the bandgap is 3.1 V, and the circuit was designed to work with only a 2.1 V supply to ensure good EMI robustness. By doing this, the circuit has the benefit of approximately 1 V margin for disturbances on VDD.

Voltage drop on *R*1 and *R*2 resistors was set to 0.9 V. For larger EMI levels, the bandgap core BJTs are pushed to unwanted saturation, which strongly influences the reference voltage. Therefore, a simple BJT anti-saturation circuit (M1–M3, M6, and M9 in Fig. 103) was added to maintain bandgap core BJTs in the linear region. This circuit consists of a detection transistor M9, which is cascoded by M6, and a forcing current mirror M1–M3. When BJTs collector to base voltage decreases close to 0 V, transistor M9 starts to conduct and delivers current to the forcing current mirror M1–M3. This current mirror decreases voltage drop on *R*1a and *R*1b and pulls up BJTs collectors as well.

The proposed bandgap employs digitally variable resistor *R*4 (Fig. 105) to trim the reference voltage due to process variations. An 8-bit trimming allows approx. 1 mV/LSB trimming step. Switched resistors are grouped into two-bit sections and using special topology decreases requirements for switch resistances yielding a smaller layout area. A one-temperature trimming at 150 °C was used.

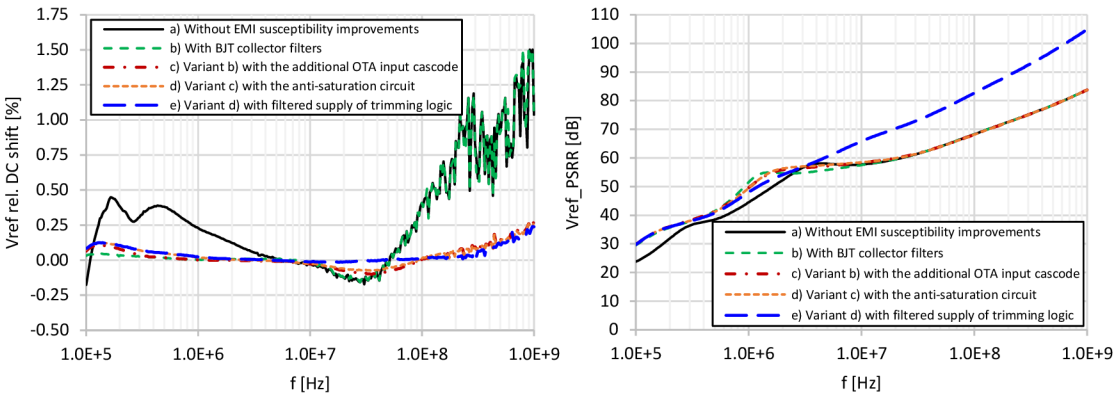
Because resistor *R*4 is in the emitter circuit of the bandgap core, there is a high sensitivity to disturbances coming from supply through digital gates and intrinsic capacities of trimming NMOS switches. Therefore, the trimming logic was supplied, which has almost zero static current consumption, by a first-order low-pass RC filter. In this design, the cutoff frequency of the filter is approximately 5 MHz.

4.6.5. EMI Susceptibility of the Bandgap Reference

To verify the proposed EMI susceptibility improvements, EMI simulations were performed with the following configurations of the overall bandgap, refer to Fig. 103:

a) Without EMI susceptibility improvements,
b) With BJT collector filters ($C1$ and $C2$ added),
c) Variant b) with the additional cascode of the differential input pair ($R5$, $C3$, M4, and M5 added),
d) Variant c) with the anti-saturation circuit (M1–M3, M6 and M9 added), and
e) Variant d) with the filtered supply of trimming logic.

The transient envelope analyses by the Cadence Spectre RF simulator for each bandgap configuration were performed. The 1 V amplitude EMC signal was superimposed on the supply voltage. Achieved results are shown in Fig. 106 a) and b).

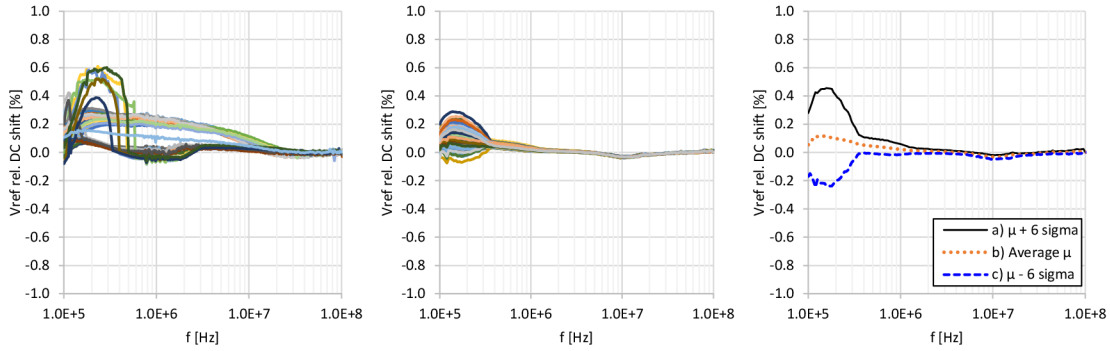


a) b)

Fig. 106: The a) relative DC voltage shifts and b) PSRRs of the new bandgap for 1 V peak EMI at VDD supply from transient simulation.

From these results, the added second-order collector filters show their essence in the lower frequency range from 100 kHz to 10 MHz. Further, the proposed additional cascode of the differential input pair reduces supply EMI susceptibility in the higher frequency range from approximately 50 MHz to 1 GHz. On the other hand, the susceptibility at the lower frequency range is slightly decreased, and the relative reference voltage shift is up to 0.1 %. The BJT anti-saturation circuit slightly decreases the susceptibility in the frequency range around 50 MHz. This contributor is the smallest of all improvements at a given disturbance level, and it helps with higher disturbances. Finally, the filtering of the logic supply of $R4$ trimming shows a reduced susceptibility in the middle-frequency range from 10 MHz to 100 MHz. The simulation results prove that all presented EMI improvements help to decrease the susceptibility of the proposed bandgap.

The corner and Monte Carlo simulations were performed to predict the variance of EMI susceptibility caused by the chip fabrication process and mismatch variances. The corner simulation includes 37 variations of process and nominal (typical) corners. Additionally, the mismatch Monte Carlo simulation with 255 runs was done. The simulations were performed for the proposed bandgap, which has all presented EMI improvements. Results from these simulations are shown in the following Fig. 107.



a) b) c)

Fig. 107: The relative DC voltage shifts for a) corner, b) mismatch Monte Carlo and c) 6 sigma mismatch extrapolation for 1 V peak EMI at VDD supply transient simulation.

The EMI corner simulation results show the worst-case process situations, which indicate circuit behavior with low probability. These results practically indicate circuit maximum limits without effects caused by random offsets. According to these results, the V_{ref} relative DC shift can be expected in the range of -0.1 % to 0.6 %.

The EMI mismatch Monte Carlo simulation (refer to Fig. 107 b)) with 255 runs was performed by the Cadence Spectre Monte Carlo simulator for temperature 27 °C. The results show the V_{ref} relative DC shifts within ± 3 sigma. The DC shift can be expected to range from -0.1 % to 0.3 %. The expected DC shift can be extrapolated to ± 6 sigma results (refer to Fig. 107 c)) within consideration of the statistical theory (see Appendix 4). The obtained ± 3 sigma results can be extrapolated to ± 6 sigma in an approximate way assuming the almost normal distribution of the circuit parameter x with equidistant multiplies of sigma. The one sigma can be calculated from Appendix 4 or in the MS Excel software by using the STDEV function on the data set from all the runs of the Monte Carlo simulation. The required number n of sigma result is easily obtained by integer multiplication of this calculated one sigma with the addition of mean as follows.

$$x_{\pm n\cdot\sigma} = \mu \pm n \cdot \sigma. \tag{89}$$

The validity of n-sigma results can be checked against simulated m-sigma results via one-sigma calculation, as is shown in the following equation.

$$x_{\pm m\cdot\sigma\ simulated} \approx \mu \pm m \cdot \frac{\left|x_{\pm n\cdot\sigma} - \mu\right|}{\pm n}. \tag{90}$$

The extrapolated ± 6 sigma of V_{ref} relative DC shifts within mismatch Monte Carlo simulation are shown in Fig. 107 c). The shift can be expected to range from -0.25 % to 0.5 %. The validity check shows that rel. errors are less than 15 % in the overall frequency range and less than 1 % in DC shift peaks. The 15 % is caused by a higher sigma than 3 in the original simulation results and nonlinearity of the circuit.

A Solido Variation Designer, developed by Siemens company, is a software used for the process and mismatch Monte Carlo simulations. This software uses an improved Solido Monte Carlo algorithm that can achieve the same statistical results with a lower number of simulation runs as compared to brute-force simulation runs. For example, only 301 runs can show the same statistical result as the brute-force equivalent of 49.7 million runs. This reduction has benefits in terms of lower simulation run time and allowing for deep statistical verification. The Solido Monte Carlo results, including mismatch and process variations for the EMI susceptibility of the bandgap, are shown in Fig. 108.

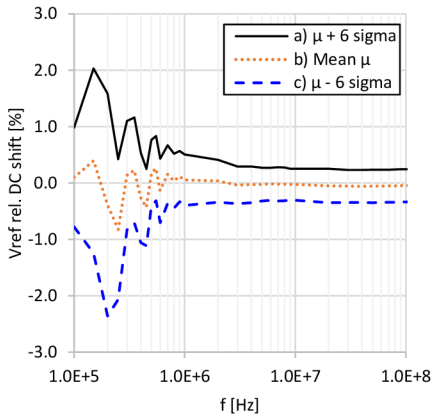
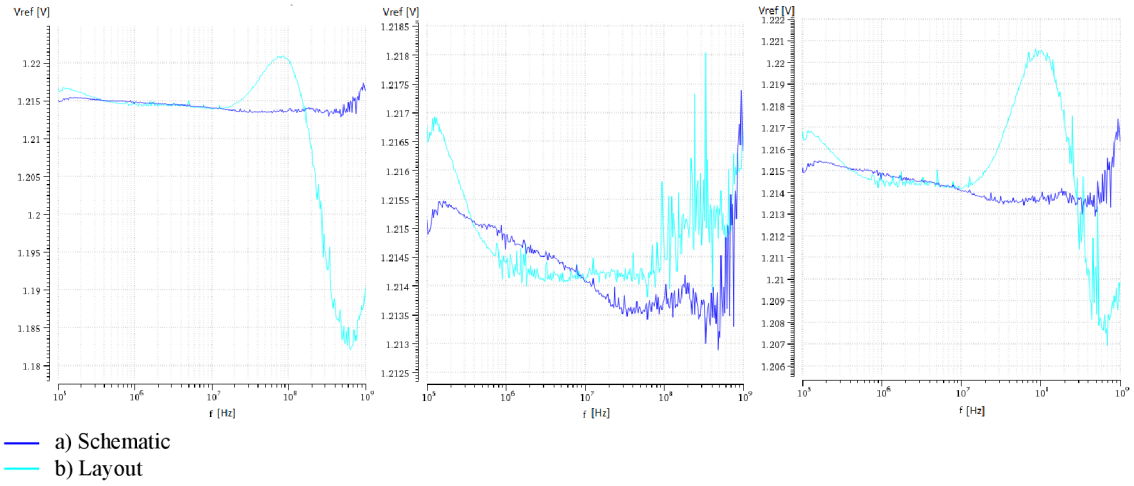


Fig. 108: The relative DC voltage shift for 1 V peak EMI at VDD supply from Solido Monte Carlo simulation.

The frequency range was considered from 100 kHz to 100 MHz due to the time requirement of these “large-scale” simulations. The range from 100 kHz to 10 MHz is interesting for process corners and Monte Carlo variation effects. For example, the mismatch of IC devices is negligible for higher frequencies because the IC behavior is dictated by a mismatch of parasitic elements, which are very difficult to estimate. The Solido Monte Carlo with process and mismatch variations shows that the DC shift can be expected to range from -2.2 % to 2.0 % at low frequencies.

The last verification step is a post-layout simulation with a back annotated schematic of the proposed bandgap by using a Siemens Calibre parasitic extraction (PEX). For this extraction, an xACT 3D method, which uses a field-solver modeling engine for metal-to-metal capacities, was used. The three most significant simulation results are shown in Fig. 109.

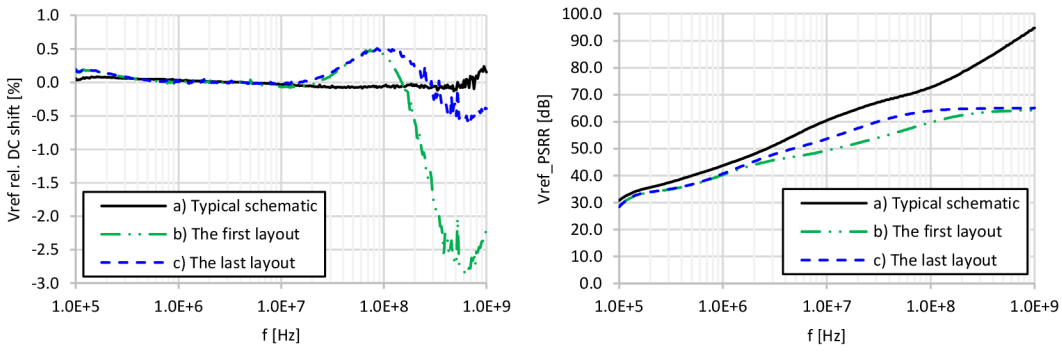


a) b) c)

Fig. 109: The comparison of DC voltage shift for a) the first layout, b) layout PEX netlist modification, and c) the final layout with 1 V peak EMI at VDD supply.

The first result (Fig. 109 a)) shows that the layout needs to be optimized. The optimization was performed by a PEX netlist investigation. In this netlist, the sensitive nets were first determined, and then the capacities between these nets higher than 1 fF were searched for and removed. This PEX netlist modification includes removing some unwanted high-sensitive coupling capacities in the emitter circuit of BJTs, in the differential pair to everything else than the ground, and small value capacities between VDD and BJT bases. The result is shown in Fig. 109 b).

After several attempts, the final version of the layout (shown as the result in Fig. 109 c)) indicates that it is impossible to reduce all unwanted capacities to negligible values. It is important to note that there is a limit to minimizing these capacities that cannot be exceeded. Moreover, the EMI signal is affected by various factors like inductances of pins, bond wires, capacities of pins, a lead frame, and inner metallization. Although these components can help to attenuate the EMI signal, there can be resonances that could cause issues. To summarize the results, the typical schematic and post-layout simulation results are shown in Fig. 110.



a) b)

Fig. 110: The summary of schematic versus layout a) relative DC voltage shifts and b) PSRR in transient simulations with 1 V peak EMI at VDD supply.

The final layout version of the proposed bandgap has the typical relative DC shift up to ± 0.5 %, and the PSRR is higher than 30 dB. The final DC shift is almost six times lower than the first layout version. The HF interference from the substrate was not analyzed because the 180 nm BCD (I4TE) technology offers a very well-contacting P-type epitaxial (PEPI) layer to the ground. The cross-section of used BJTs is shown in Fig. 111.

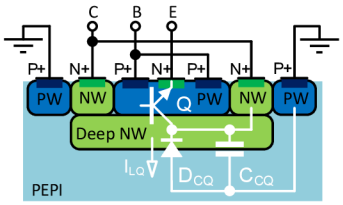
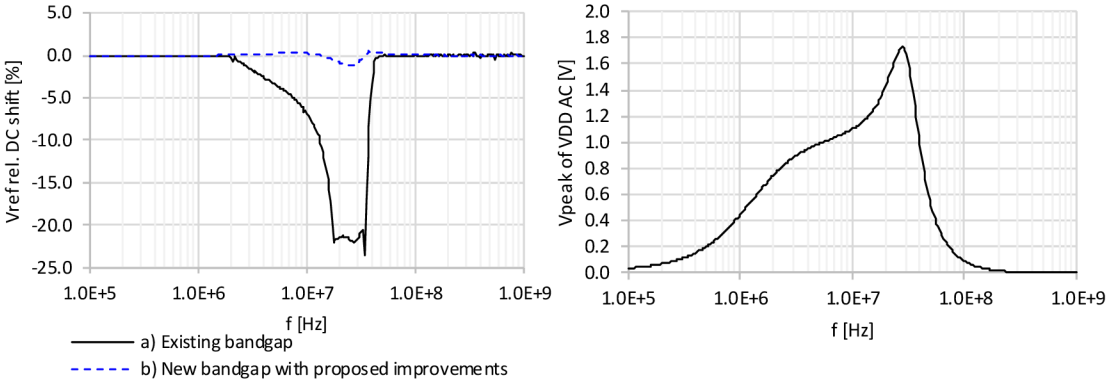


Fig. 111: The cross-section of an I4TE vertical NPN BJT in the IC.

It is worth note that the new EMI DPI simulation method (chapter 4.2.5) for the proposed bandgap with similar setup as for the existing bandgap (see Fig. 60) shows improvement of the susceptibility with the resulting dc shift less than 1 %. The results are shown in Fig. 112.



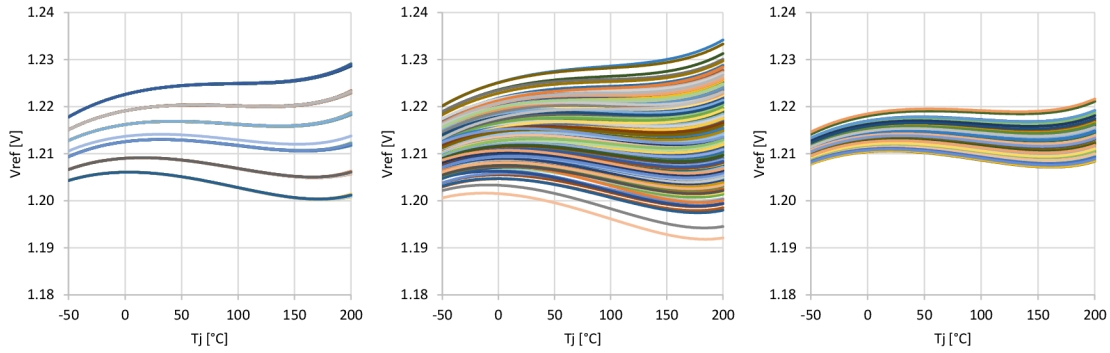
a) b)

Fig. 112: The a) *V*ref DC voltage variations and b) AC voltage at VDD supply from the new EMI DPI simulation method with $V_{EMIpeak}$ = 1 V (P_{For} = 4 dBm).

4.6.6. Achieved Results of the Realized Voltage Reference

This chapter presents the achieved results within temperature characteristics and practically measured EMI susceptibility of the proposed bandgap. The first part is dedicated to examining the results of the reference voltage over the temperature range from -50 to 200 °C.

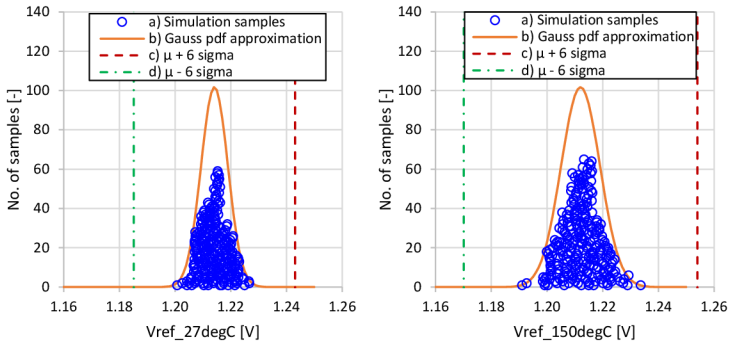
The corner and Monte Carlo simulations with swept temperature were performed to check the variance of reference voltage by the chip fabrication process and mis-match variances. The corner simulation includes 37 variations of process and nominal (typical) corners. Additionally, the mismatch and process Monte Carlo simulations with 255 runs were done. The simulations were performed for the proposed bandgap, which has all presented EMI improvements. Results from these simulations with one typical V_{ref} trimming code are shown in the following Fig. 113.



a) b) c)

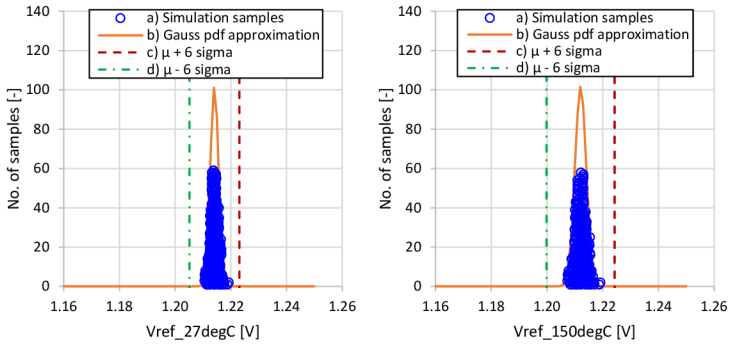
Fig. 113: The V_{ref} vs. temperature for a) corner, b) mismatch Monte Carlo, and c) process Monte Carlo simulations without trimming.

The results show higher sensitivity to mismatch. The Monte Carlo results are valid within approximately ± 3 sigma for maximum and minimum values. This is also evident from approximations by pdf (Appendix 4), which are shown in histograms Fig. 114 and Fig. 115. There are also shown limit lines for ± 6 sigma extrapolations.



a) b)

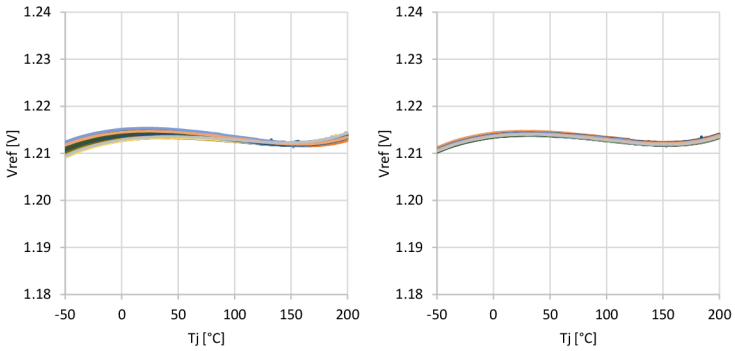
Fig. 114: Mismatch Monte Carlo histograms of V_{ref} without trimming for a) 27 °C and b) 150 °C.



a) b)

Fig. 115: Process Monte Carlo histograms of V_{ref} without trimming for a) 27 °C and b) 150 °C.

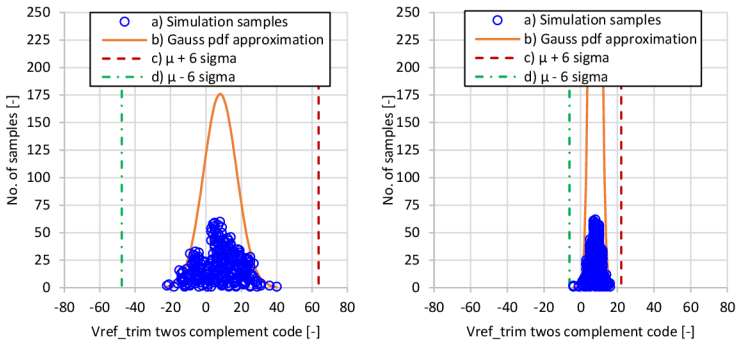
Results from the mismatch and process Monte Carlo simulations, including the V_{ref} trimming procedure at 150 °C, are shown in the following Fig. 116.



a) b)

Fig. 116: The trimmed V_{ref} vs. temperature for a) mismatch and b) process Monte Carlo simulations.

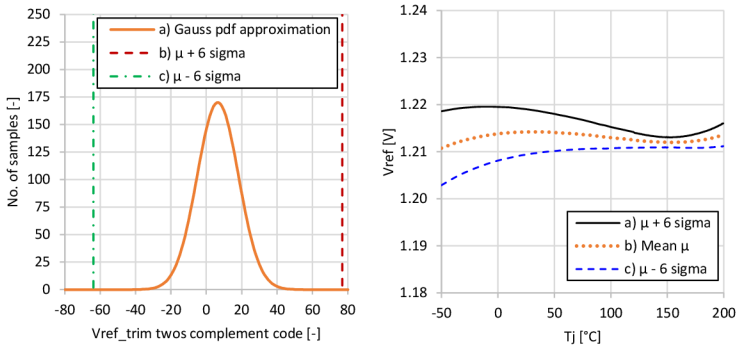
The Monte Carlo results show a voltage-trimming benefit. The resulting V_{ref} variance is very low. The histograms of corresponding trim codes with approximations by pdf function (Appendix 4) and limit lines for ± 6 sigma extrapolation are shown in Fig. 117.



a) b)

Fig. 117: The trim codes of the proposed bandgap for a) mismatch and b) process Monte Carlo simulations.

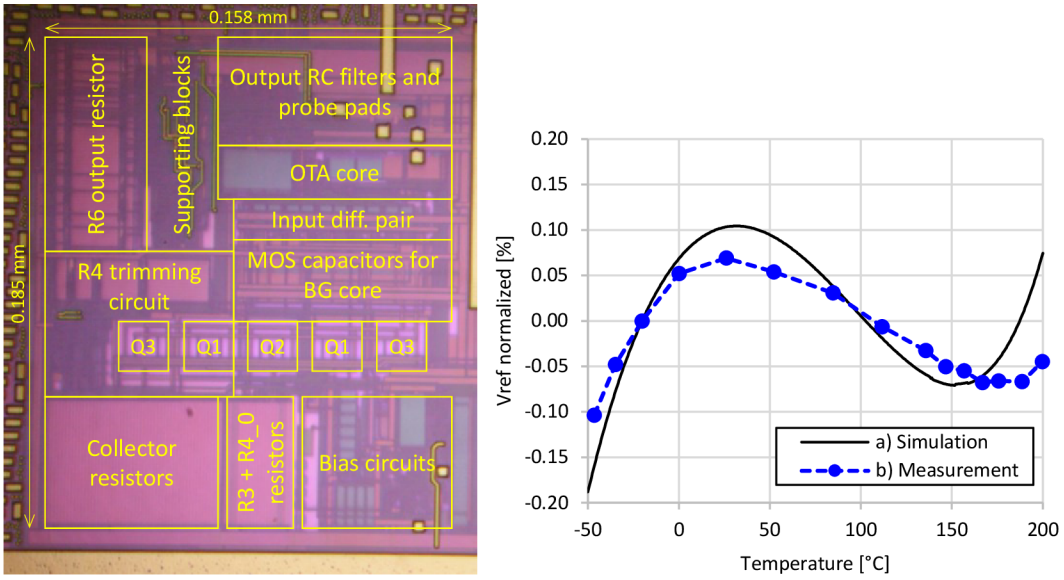
The Solido Monte Carlo results including mismatch and process variations show higher V_{ref} variance at a cold temperature of -50 °C and expected minimum variance at a trimming temperature of 150 °C. The resulting histogram of trim codes with limit lines for ± 6 sigma and related V_{ref} temperature characteristics are shown in Fig. 118.



a) b)

Fig. 118: The trim codes a) and temperature characteristics b) from Solido Monte Carlo simulation with process and mismatch variations.

The proposed bandgap voltage reference was realized in the onsemi 180 nm smart power BCD process as a part of a System on Chip (SoC). A die micro-photo of the realized voltage reference with the active silicon area of about 0.03 mm^2 and temperature dependency of measured and simulated reference voltages after trimming are shown in Fig. 119.



a) b)

Fig. 119: The a) die micro-photo and b) temperature characteristics after trimming.

For both simulation and measurement, the trimming code was firstly determined at a temperature of 150 °C by finding a target voltage of 1.215 V. Subsequently, the temperature sweep was performed, and the resulting output voltage was measured. The measured temperature coefficient of V_{ref} is about 7 ppm/°C. The simulation and measurement results are roughly correlating. Achieved statistical results for trimming temperature are summarized in Tab. 18.

Tab. 18. Statistical results for 150 °C after trimming.

Type of results	V_{ref}			Vref_trim code		
	-6·σ [V]	μ [V]	6·σ [V]	-6·σ [-]	μ [-]	6·σ [-]
a) Mismatch MC	1.211	1.212	1.213	-48	8	64
b) Process MC	1.211	1.212	1.213	-6	8	22
c) Solido P&M MC	1.211	1.212	1.213	-64	7	77

The second part is dedicated to presenting practically measured EMI susceptibility results. The susceptibility of the proposed bandgap was validated by the DPI method according to IEC 62132-4:2006 [26] in the frequency range from 100 kHz to 1 GHz. According to this method, a sinusoidal interfering signal with a known frequency and power was injected via an AC coupling capacitor to the VDD supply of the SoC since the output reference voltage was monitored by a DC voltmeter. The DPI test setup is shown in Fig. 120.

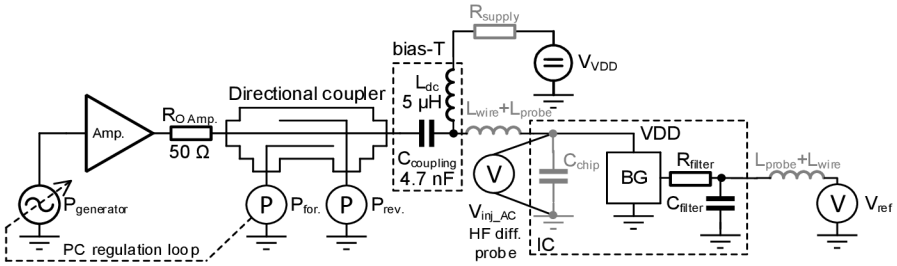
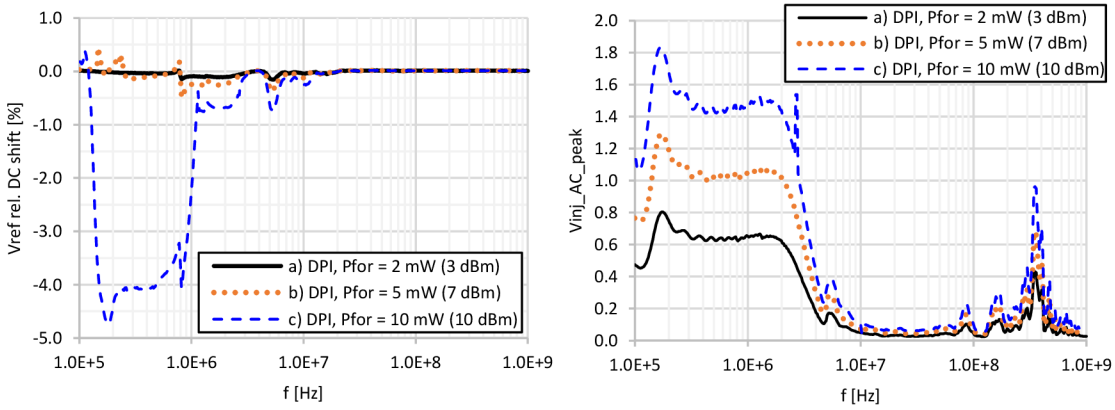


Fig. 120: The simplified circuit diagram of the DPI test setup.

This test setup does not have any external decoupling capacitor on the VDD supply to cover the worst case. For this case, there is native chip capacity C_{chip} with a value of about 10 nF as the VDD supply decoupling. The DC voltage supply source is isolated from AC by a choke L_{DC} which forms with the AC coupling capacitor $C_{coupling}$ a "bias-T" circuit. The parameters of this circuit were published in [28]. The DPI measurement results are shown in Fig. 121.



a) b)

Fig. 121: The DPI measurement results: a) V_{ref} relative DC shift and b) VDD AC voltage in the chip.

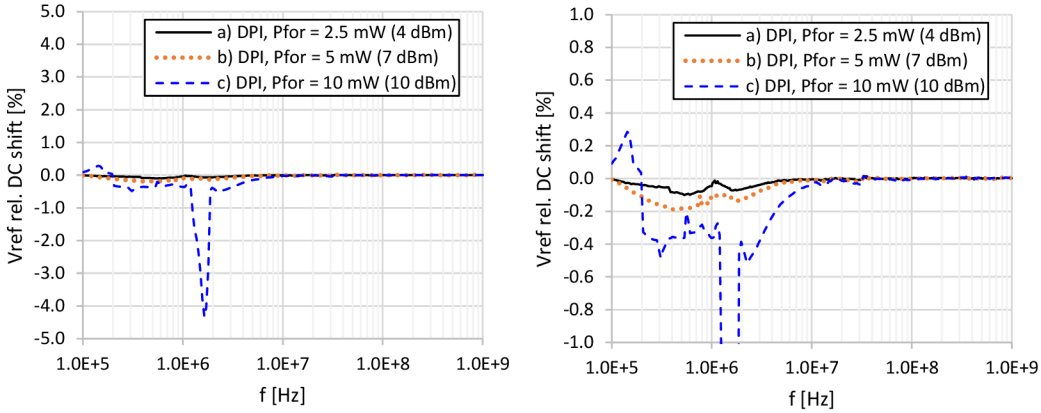
In the frequency range from 100 kHz to 1 GHz, the measured DC shifts are below 0.5 % for 5 mW (7 dBm) forward power. For the 10 mW (10 dBm), the maximum DC shift is lower than 5 % without damage of the bandgap. The high AC amplitudes of supply resonances create the peaks of DC shift. These resonances are caused by the "bias-T" circuit with coaxial wire and micro-probe inductances and the C_{chip} capacity. The internal resistor of the VDD voltage supply, R_{supply} in Fig. 120, partially dampens the resonances.

The DPI method involves a regulation loop of the average forward power using a personal computer (PC) with measurement software. The power meter measures the forward power through a directional coupler in this loop. The regulation loop behaves like negative feedback, which means that the amplifier output resistance, $R_{O\ Amp.}$ in Fig. 120, does not play a dominant role within the resonance damping. Therefore, more than one dominant resonance is seen in Fig. 121 b).

To measure the VDD voltage, a HF differential probe with 3 GHz bandwidth (Rohde & Schwarz RT-ZD30) was connected to a digital storage oscilloscope with 2 GHz bandwidth and 10 GSa/s sampling rate (Rohde & Schwarz RTO 1024). This voltage, marked as V_{inj_AC} in Fig. 120, was measured between microprobes connected to the internal VDD and GND of the IC.

The AC voltage in Fig. 121 b) shows the transmission of the “bias-T” filter and the attenuation caused by C_{chip} capacity, including resonances from parasitic circuit elements. The first dominant resonance is caused by the AC coupling capacitor and the inductance of the “bias-T” with the DC power supply. The other resonances are the results of the above-mentioned circuit interactions. An interesting dominant resonance occurs at 350 MHz. It is caused by inductances of coaxial wire and micro-probe with the input capacitance of the differential probe, which is less than 1 pF.

Fig. 122 shows the measurement results of the standard DPI to an external VDD pin of the test chip. This pin was added only for measurements and not used for normal functions.



a) Overview b) Detail

Fig. 122: The measurement results for DPI to external VDD pin via socket.

The internal supply is typically not connected to the external pin. However, the DPI measurements show a lower relative DC shift than previous tests. This effect is because the test chip was placed in a socket that has an inductance and capacitance in its wiring, and the external pin that attenuates the AC signal. Due to the different impedances in the DPI path, two effects are observed when comparing Fig. 122 a) to Fig. 121 a). Firstly, there is a higher AC attenuation (lower DC shift). Secondly, the dominant resonance has moved to a higher frequency according to the DC shift peaks.

In general, measured results show significantly lower supply EMI susceptibility of the proposed bandgap than other similar published bandgaps. The comparison of the bandgaps is in Tab. 19.

Tab. 19. Comparison of published Brokaw bandgaps with power supply EMI susceptibility measurements.

Reference	**[21]**	**[23]**	**This work, 1st BG [48]**	**This work, new BG**
Technology	0.7 µm	0.32 µm	0.35 µm	0.18 µm
Active area	0.160 mm^2	N/A	0.040 mm^2	0.029 mm^2
Supply voltage	3.0 V	3.3 V	3.0 V	3.1 V
Output voltage	1.170 V	1.247 V	1.205 V	1.215 V
Temperature range	-40 to 125 °C	-50 to 180 °C	-40 to 160 °C	-50 to 200 °C
Temperature coefficient	50 ppm/°C	3 ppm/°C	100 ppm/°C	7 ppm/°C
Current consumption	46 µA	50 µA	3.5 µA	3.2 µA
Power consumption	138 µW	165 µW	10.5 µW	9.9 µW
EMI DPI level	-13 dBm	-5 dBm	-3 dBm	7 dBm
V_{ref} rel. DC shift with DPI	max. 12.0 %	max. 7.8 %	max. 7.0 %	max. 0.5 %

Note that the output stage of the proposed bandgap is not designed for driving an external pin due to on-chip use only. Therefore, the output is connected to an output RC first-order low-pass filter (R_{filter} and C_{filter} in Fig. 120) with a cutoff frequency of 0.6 MHz. Then the filtered reference voltage is distributed around the overall chip, where each reference voltage input of IC blocks has an input RC low-pass filter. Since a very low EMI at the internal bandgap reference output is expected, the output EMI susceptibility of the proposed voltage reference was not analyzed.

4.6.7. An EMI Susceptibility Measurement with A Constant Voltage Amplitude on the Tested Pin

During EMI susceptibility measurements, a new interesting experimental test method was considered. The method was called a direct voltage injection (DVI) and it is based on the idea of maintaining a constant peak value of the alternating voltage. This voltage was injected into the internal supply of the tested bandgap in this case. In general, the voltage can be injected into the IC pin or port of the electronic system. The test setup is the same as for the DPI shown in Fig. 120. The only difference is in the digital HF generator regulation, whose amplitude is now regulated according to sensed $V_{\text{inj\_AC}}$ RMS voltage. The sensed value by the digital storage oscilloscope is compared with the required RMS value calculated from the chosen peak value in the measurement software on the PC. According to the comparison result, the software increases or decreases the $P_{\text{generator}}$ amplitude in Fig. 120. There is also a limiting meter function that limits the amplitude to protect the amplifier and the DUT from destruction. The DVI measurement results are shown in Fig. 123.

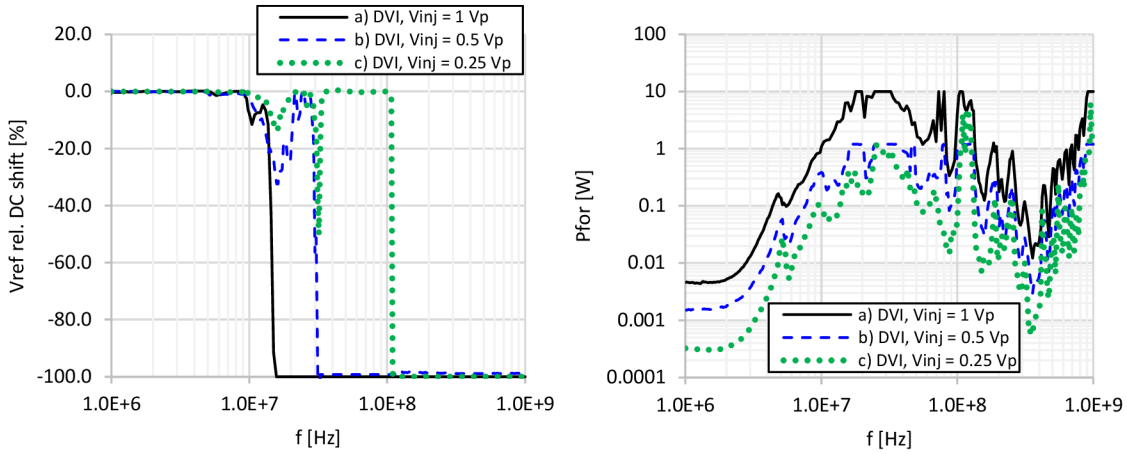
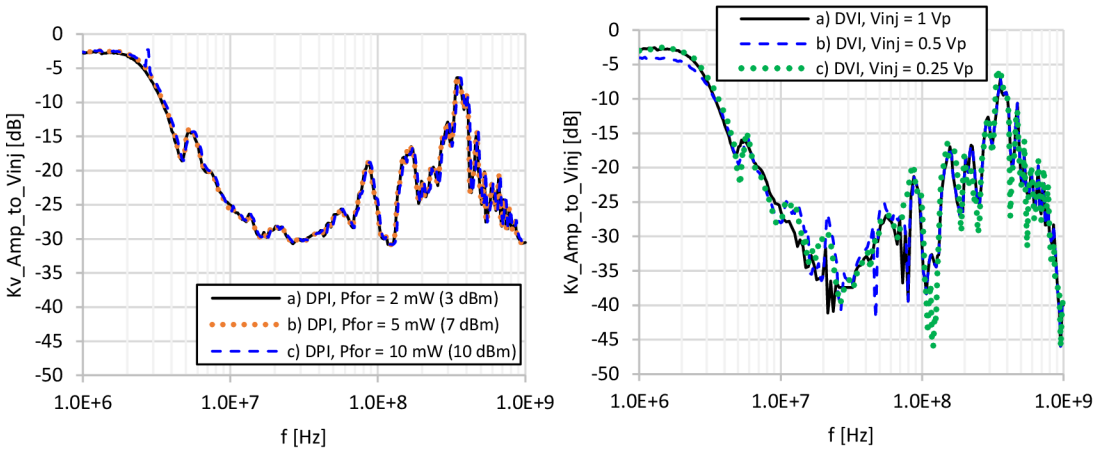


Fig. 123: The DVI measurement results: a) V_{ref} relative DC shift and b) regulated forward power P_{for}.

The results show that the constant peak value is possible to maintain in the frequency range from 1 MHz to 1 GHz, but the DUT may be destroyed. The destruction occurred due to a high alternating current indicated by high forward power. The limit value of the power was 10 W. For 1 V peak, the bandgap stops working at 14 MHz due to IC metallization damage. These thin conductive paths in the bandgap act as fuses. In case of high current peaks through internal capacities, thin metal paths are interrupted, and the DUT goes to malfunction or unsupplied state (supply net broken). For a 0.5 V peak, the bandgap stops working at 30 MHz and for a 0.25 V peak stops at 110 MHz. The goal of this method was to approach the same alternating voltage as for the EMI simulation. However, this is not possible due to internal impedance and physical limitations of nets in the IC. The DC relative shift correlates with EMI simulations in the frequency range from 1 MHz to 9 MHz.

The voltage transmission from the HF amplifier output to the internal VDD of the IC can be a correlation parameter between DPI and DVI methods. This transmission can be calculated from the measured alternating voltage at the VDD and known forward power at the amplifier output. The transmissions for different injected powers and voltages within both test methods are shown in Fig. 124.



a) b)

Fig. 124: The voltage transmissions from the HF amplifier to the internal VDD for a) DPI and b) DVI methods.

It is evident from the results that the voltage transmissions of both methods are almost exactly correlated. The difference is in a dynamic range of acquired alternating voltage. For the DPI, the VDD HF voltage is directly measured by the differential probe with the fixed oscilloscope setting. On the other hand, the VDD HF voltage of the DVI is regulated to the required peak value with a tolerance of up to 1 dB. In both cases, the HF amplifier output voltage is calculated from the measured forward power at the directional coupler. Additionally, the attenuator was used at directional coupler input to obtain higher accuracy of forward power regulation with noise reduction for the DPI. This attenuator is not possible to use for the DVI due to the required high range of power, but the whole dynamic range of the power sensor is fully used with auto-ranging effects that mostly increase accuracy and measurement time.

The DVI was evaluated as an aggressive EMI susceptibility test method like a closed-loop bulk current injection (BCI) method where HF current is inductively injected into wires. The forward power of the DVI method correlates with the DPI method in the low-frequency range from 1 MHz to 2 MHz due to the DUT impedance. The DVI can be used with small values of HF voltage in the frequency range of up to 100 MHz for local EMI coupling, e.g., in the IC, where the BCI method is not possible as the worst-case and aggressive EMI test.

4.6.8. Summary of Recommendations for Robust EMC Design

This chapter summarizes recommendations for IC design with low EMI susceptibility. The simulation and measurement results from previous chapters demonstrate the validity of the EMC robust design methodology which consists of the following general recommendations. These can be summarized into four points:

a) Using a fully symmetrical and differential topology everywhere where it is possible for high CMRR and PSRR.

b) Keep all possible circuit nodes in a low impedance state at high frequencies.

c) Make symmetrical filtering of all differential signals and keep the same time constants.

d) Count with hidden structures of the IC.

Six more points based on the summarizing of this work can be added to these basic methodological recommendations, and these are:

e) Count with hidden impedance resonances, especially impedance serial resonances, which can create very high voltage ripple at an internal IC capacity.

f) Reduce AC coupling from supply to sensitive inputs or nodes by cascoding and/or filtrations.

g) Use perfect time constant matching for differential signals, e.g., OPA input capacities with respect to bandgap core outputs.

h) Consider sufficient voltage room for EMI disturbances and design the circuit to operate at a significantly lower supply voltage than the nominal one.

i) Consider supply filtration of logic circuits, which control switches in highly sensitive analog circuits.

j) Post-layout simulation of a complete block, e.g., the voltage reference for checking unwanted coupling effects.

The following steps are recommended to ensure that analog design is robust against EMI. Firstly, the relationship between the IC and its EMI environment needs to be understood. It is crucial to identify the location of interference, the affected IC pins, and the impact of the PCB on coupling. From the PCB perspective, conductive paths with external parts act as an antenna, which can receive EMI from the radio environment or local current loops. From the IC perspective, an internal impedance, such as distributed spread capacitances and resistances from other nodes, determines the unwanted signal propagation and its effect. The IC pin capacitance affects the propagation from the PCB to the IC.

The second step is to analyze the EMC properties of each system part. For the IC block, it can help to investigate factors such as voltage dc shift, PSRR, and CMRR. During this investigation, it is crucial to identify the most susceptible block of the entire circuit or system. High impedance and sensitive nodes can be found, which need to be improved by decreasing high-frequency impedance and increasing voltage or current static stability. After circuit modifications, the EMC properties should be rechecked to establish the impact of the changes.

For the PCB, a vital step is estimating an external impedance circuit model for the dedicated IC pin. The IC block connected to the pin with the model can be investigated for voltage dc shift, PSRR, and CMRR. Experiments such as moving unwanted resonances away by detuning from the frequency range of interest by changes of PCB and external parts can be considered. Finally, experimental simulations and measurements of the entire circuit are needed to verify the validity of all changes.

5 CONCLUSIONS

The EMC is a crucial performance measure for any electronic device, particularly in the automotive where high standards are required for new applications. Standardized compliance tests for EMC of the entire car are performed, but these tests are often too late for IC development. Identifying and solving EMC issues at an early stage reduces development costs and time to market. Therefore, it is vital to verify the EMC performance during the development of a new IC to ensure EMC robust circuit design and avoid the complexities that come with later detection of EMC issues.

This dissertation work focuses on techniques for designing more robust bandgap voltage references through EMC-resistant analog IC design. This work presents several recommendations for improving the EMI robustness of the voltage references. The EMI susceptibility simulations and measurements of two test chips were used to validate the effectiveness of these recommendations.

The first existing voltage reference, manufactured in 0.35 µm BCD process, has a current consumption of 3.5 µA and operates in a wide temperature range from -40 °C to 160 °C. It can withstand -3 dBm EMI DPI power coupled to the supply pin, and the maximum output DC voltage variation is 7 %. The comparison of this bandgap with other publications is summarized in Tab. 9.

The second proposed reference is manufactured in 0.18 µm BCD process and has a current consumption of 3.2 µA. It operates in a temperature range from -50 °C to 200 °C and can withstand 7 dBm DPI power to the internal supply line with a relative DC shift only below 0.5 %.

It is evident that the proposed new voltage reference has a lower current consumption, wide temperature range, and higher EMC robustness in comparison to the previous references discussed in Tab. 19. Additionally, the new EMC robust reference is capable of withstanding 10 dBm DPI RF power at the low voltage supply line without any damage and with a DC voltage deviation of up to 5 %. The validity of all recommendations and design methodology has been proven, and all dissertation aims have been successfully achieved.

There are several appendixes included in this work. The first one shows a flow chart of the proposed element-by-element extraction method related to chapter 3.2.1. The second appendix offers the impedance network model synthesizer software application. This software can be found on a CD or in an attached ZIP file in the case of the electronic version on the university web. The third appendix addresses the theoretical question of which of the two most used low-voltage semiconductor devices is more susceptible to EMI. The fourth appendix reminds normal distribution in statistics. The fifth appendix presents a Matlab script that was used for statistical and EMI susceptibility calculations of low-voltage devices. The sixth appendix shows a diagram of all systematically published papers relevant to this work. Finally, the seventh appendix provides photos of the fabricated test chip with the proposed bandgap.

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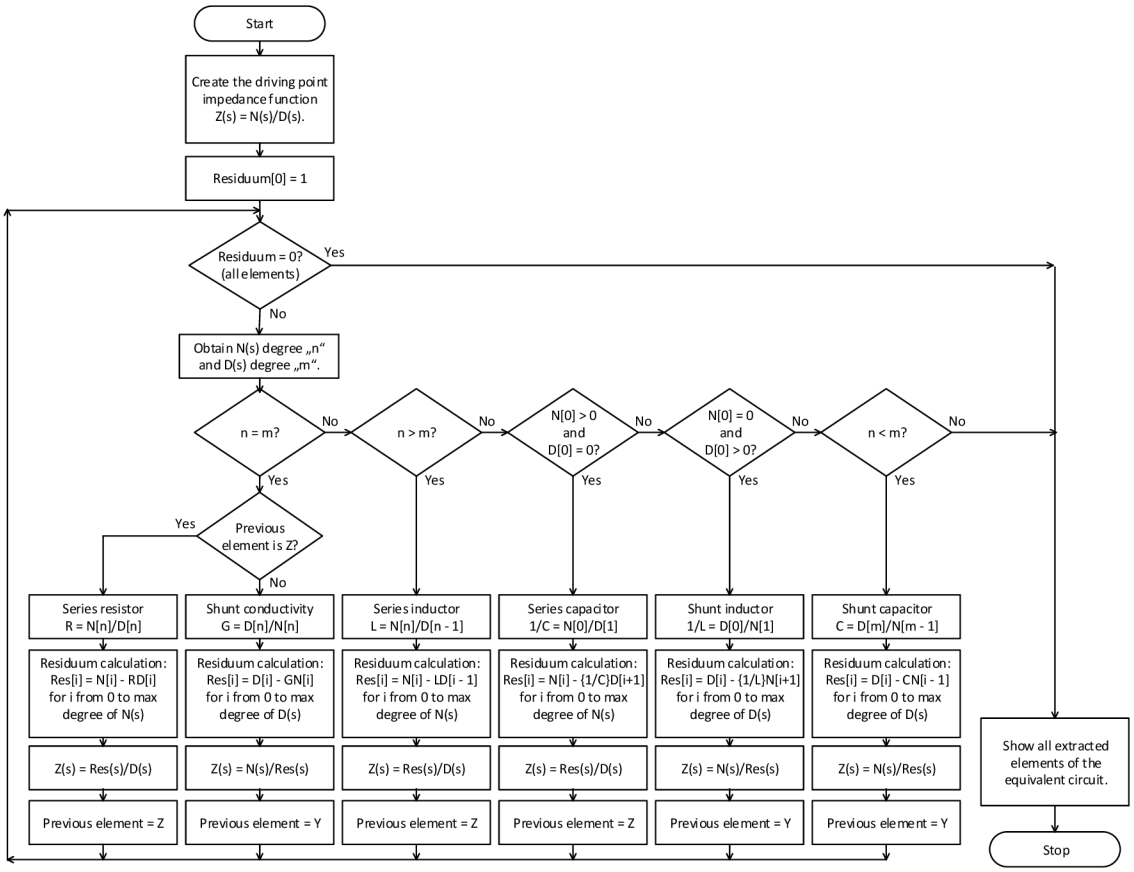
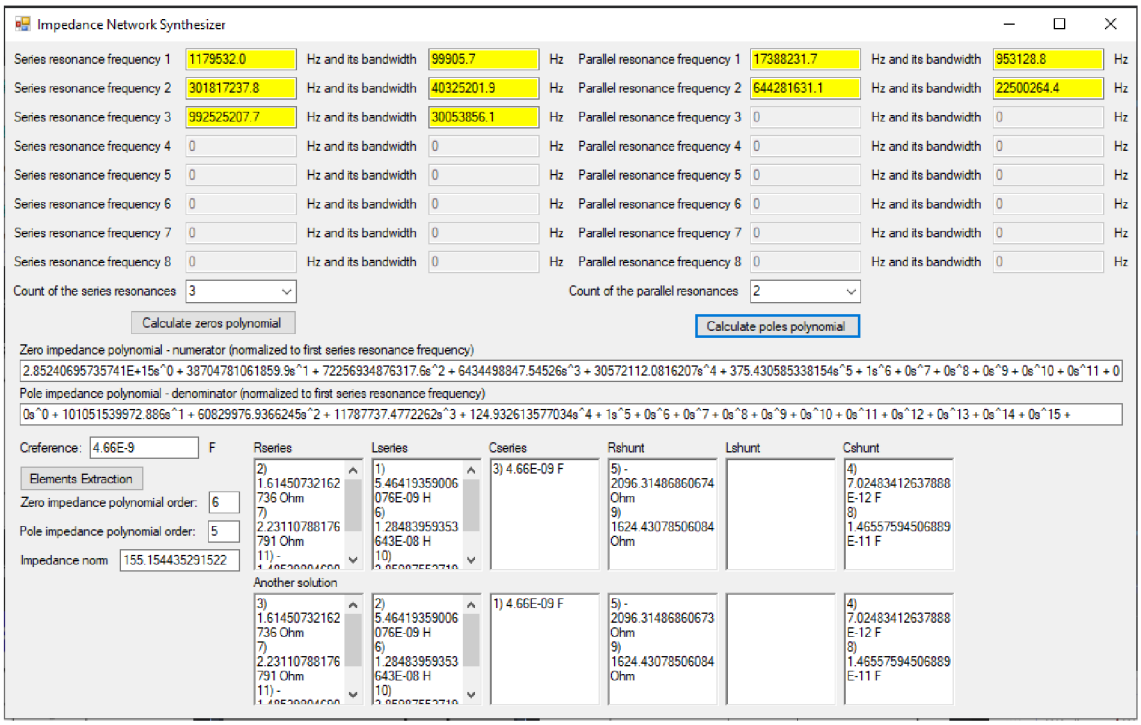
List of Appendixes

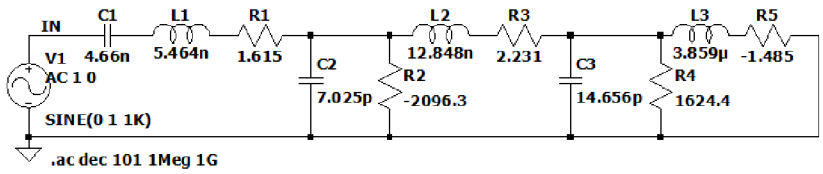
Appendix 1 Proposed Element-by-Element Extraction Method Flow Chart

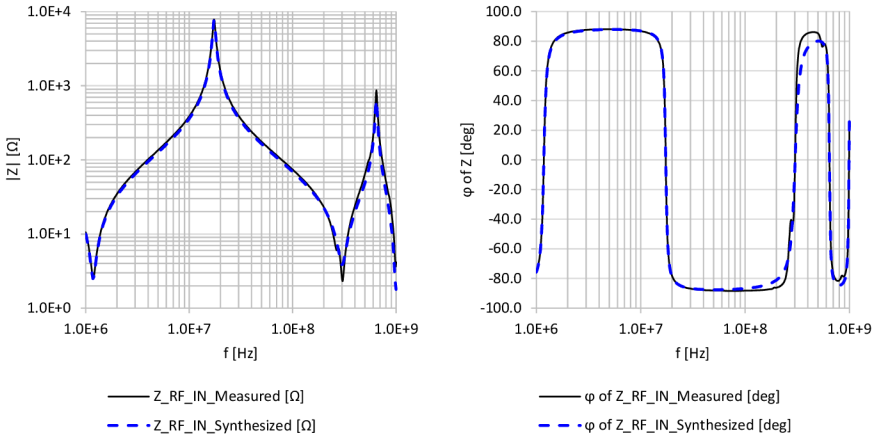


Appendix 2 The Impedance Network Synthesizer Software

The source code and the software of the impedance synthesizer application are saved on the enclosed CD or in the ZIP file for the case of the electronic version on the university web due to its size. The theoretical example of the software using two negative resistors in a synthesized network model is shown below.







Appendix 3 Theoretical EMI Sensitivity of Main Low-Voltage Semiconductor Devices

This appendix aims to find an answer to the following question: "Which one of the two following semiconductor devices, an NPN bipolar junction transistor and an NMOS transistor, is more sensitive to the EMI in their control electrode?"

To answer this question, start with the NPN BJT and consider the normal operating point. The BJT is in the linear region with a constant voltage between its collector and emitter. Its collector current is described by the following equation, where the very high current gain β is assumed, so the base current can be assumed as negligible for this case.

$$I_{C\_DC} = I_S \cdot A_E \cdot \left(e^{\frac{V_{BE\_DC}}{m \cdot V_T}} - 1 \right). \tag{91}$$

This is a collector DC current without an EMI signal. Now, a low EMI harmonic signal is considered, and the resulting DC collector current can be calculated from the definite integral over the one period of the harmonic signal.

$$I_{C\_DC\_EMI} = \frac{1}{T} \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} I_S \cdot A_E \cdot \left(e^{\cdot \frac{V_{BE\_DC} + V_{pk} \cdot sin\frac{2 \cdot \pi \cdot t}{T}}{m \cdot V_T}} - 1 \right) dt. \tag{92}$$

A method of expanding to stand-alone integrals was used to solve this integral.

$$I_{C\_DC\_EMI} = \frac{1}{T} \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} I_S \cdot A_E \cdot e^{\frac{V_{BE\_DC}}{V_T}} \cdot e^{\frac{V_{pk} \cdot sin\frac{2 \cdot \pi \cdot t}{T}}{m \cdot V_T}} dt - \frac{1}{T} \cdot A_E \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} I_S dt. \tag{93}$$

Solving all known integral functions leads to

$$I_{C\_DC\_EMI} = I_S \cdot A_E \cdot e^{\frac{V_{BE\_DC}}{V_T}} \cdot \frac{1}{T} \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} e^{\frac{V_{pk} \cdot sin\frac{2 \cdot \pi \cdot t}{T}}{m \cdot V_T}} dt - A_E \cdot I_S. \tag{94}$$

This result contains a nonintegrable function, which means that another analytical step doesn't exist. So, let's try the following mathematical trick: the *sin* function can be replaced by the *cos* function, and the integration interval can be changed to an interval from *0* to $2 \cdot \pi$ that still includes the entire period of the harmonic *cos* function. The modified definite integral is

$$I_{C\_DC\_EMI} = \frac{1}{2 \cdot \pi} \cdot A_E \cdot \int_0^{2 \cdot \pi} I_S \cdot \left(e^{\frac{V_{BE\_DC} + V_{pk} \cdot cos\, x}{m \cdot V_T}} - 1 \right) dx. \tag{95}$$

Again, expand the above definite integral equation to the following form.

$$I_{C\_DC\_EMI} = \frac{1}{2 \cdot \pi} \cdot A_E \cdot \int_0^{2 \cdot \pi} I_S \cdot e^{\frac{V_{BE\_DC}}{m \cdot V_T}} \cdot e^{\frac{V_{pk} \cdot cos\, x}{m \cdot V_T}} dx - \frac{1}{2 \cdot \pi} \cdot A_E \cdot \int_0^{2 \cdot \pi} I_S dx. \tag{96}$$

Solving all known integral functions using the MATLAB R2023a software shows a possible analytical solution.

$$I_{C\_DC\_EMI} = I_S \cdot A_E \cdot \left[e^{\frac{V_{BE\_DC}}{m \cdot V_T}} \cdot J_0\left(0 + j\frac{V_{pk}}{m \cdot V_T}\right) - 1 \right], \tag{97}$$

where J_0 is the first-order Bessel function of the first kind. These functions $J_\nu(x)$ are defined as the solutions to the Bessel differential equation, which are nonsingular at the origin. An example of this differential equation is shown below.

$$x^2 \cdot \frac{d^2y}{dx^2} + x \cdot \frac{dy}{dx} + (x^2 - \nu^2) \cdot y = 0. \tag{98}$$

The validity of the equation $I_{\mathrm{C\_DC\_EMI}}$ is for EMI peak voltage V_{pk} in the range

$$0 \leq V_{pk} < V_{BE\_DC}. \tag{99}$$

The $I_{\mathrm{C\_DC\_EMI}}$ can be calculated by using (97) with the following Tab. 20, which contains needed J_0 Bessel function values precalculated in MATLAB R2023a.

Tab. 20. Values of the first order Bessel function of the first kind.

x	$J_0(x)$	x	$J_0(x)$	x	$J_0(x)$	x	$J_0(x)$	x	$J_0(x)$
0 + 0.0·j	1.0000	0 + 2.0·j	2.2796	0 + 4.0·j	11.301	0 + 6.0·j	67.234	0 + 8.0·j	427.56
0 + 0.1·j	1.0025	0 + 2.1·j	2.4463	0 + 4.1·j	12.324	0 + 6.1·j	73.663	0 + 8.1·j	469.50
0 + 0.2·j	1.0100	0 + 2.2·j	2.6291	0 + 4.2·j	13.442	0 + 6.2·j	80.718	0 + 8.2·j	515.59
0 + 0.3·j	1.0226	0 + 2.3·j	2.8296	0 + 4.3·j	14.668	0 + 6.3·j	88.462	0 + 8.3·j	566.26
0 + 0.4·j	1.0404	0 + 2.4·j	3.0493	0 + 4.4·j	16.010	0 + 6.4·j	96.962	0 + 8.4·j	621.94
0 + 0.5·j	1.0635	0 + 2.5·j	3.2898	0 + 4.5·j	17.481	0 + 6.5·j	106.29	0 + 8.5·j	683.16
0 + 0.6·j	1.0920	0 + 2.6·j	3.5533	0 + 4.6·j	19.093	0 + 6.6·j	116.54	0 + 8.6·j	750.46
0 + 0.7·j	1.1263	0 + 2.7·j	3.8417	0 + 4.7·j	20.858	0 + 6.7·j	127.79	0 + 8.7·j	824.45
0 + 0.8·j	1.1665	0 + 2.8·j	4.1573	0 + 4.8·j	22.794	0 + 6.8·j	140.14	0 + 8.8·j	905.80
0 + 0.9·j	1.2130	0 + 2.9·j	4.5027	0 + 4.9·j	24.915	0 + 6.9·j	153.70	0 + 8.9·j	995.24
0 + 1.0·j	1.2661	0 + 3.0·j	4.8808	0 + 5.0·j	27.240	0 + 7.0·j	168.59	0 + 9.0·j	1093.6
0 + 1.1·j	1.3262	0 + 3.1·j	5.2945	0 + 5.1·j	29.789	0 + 7.1·j	184.95	0 + 9.1·j	1201.7
0 + 1.2·j	1.3937	0 + 3.2·j	5.7472	0 + 5.2·j	32.584	0 + 7.2·j	202.92	0 + 9.2·j	1320.7
0 + 1.3·j	1.4693	0 + 3.3·j	6.2426	0 + 5.3·j	35.648	0 + 7.3·j	222.66	0 + 9.3·j	1451.4
0 + 1.4·j	1.5534	0 + 3.4·j	6.7848	0 + 5.4·j	39.009	0 + 7.4·j	244.34	0 + 9.4·j	1595.3
0 + 1.5·j	1.6467	0 + 3.5·j	7.3782	0 + 5.5·j	42.695	0 + 7.5·j	268.16	0 + 9.5·j	1753.5
0 + 1.6·j	1.7500	0 + 3.6·j	8.0277	0 + 5.6·j	46.738	0 + 7.6·j	294.33	0 + 9.6·j	1927.5
0 + 1.7·j	1.8640	0 + 3.7·j	8.7386	0 + 5.7·j	51.173	0 + 7.7·j	323.09	0 + 9.7·j	2118.9
0 + 1.8·j	1.9896	0 + 3.8·j	9.5169	0 + 5.8·j	56.038	0 + 7.8·j	354.68	0 + 9.8·j	2329.4
0 + 1.9·j	2.1277	0 + 3.9·j	10.369	0 + 5.9·j	61.377	0 + 7.9·j	389.41	0 + 9.9·j	2561.0

For a practical approach to this equation, the following NPN BJT parameters are considered: $I_{\mathrm{S}} = 1 \cdot 10^{-8}$ A, $A_{\mathrm{E}} = 4$ um^2, $m = 1$, $V_{\mathrm{T}} = 0.026$ V, $V_{\mathrm{BE\_DC}} = 0.8551$ V and $V_{\mathrm{pk}} = 0.1$ V. This leads to $I_{\mathrm{C\_DC}} = 7.68$ µA and $I_{\mathrm{C\_DC\_EMI}} = 76.032$ µA. The relative current DC shift is approximately 890.1 %. This result, in the same order, was confirmed by the transient simulation.

To finish the answer, continue with the NMOS transistor and consider the normal operating point as well as the NPN BJT. The NMOS is in saturation region with a constant voltage between its drain and source. Its drain current is described by the following equation.

$$I_{D\_DC} = \frac{K_p}{2} \cdot \frac{W}{L} \cdot \left(V_{GS\_DC} - V_{TH}\right)^2, \tag{100}$$

This is a drain DC current without an EMI signal. Now, a low EMI harmonic signal is considered, and the resulting DC drain current can be calculated from the definite integral over the one period of the harmonic signal.

$$I_{D\_DC\_EMI} = \frac{1}{T} \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} \frac{K_p}{2} \cdot \frac{W}{L} \cdot \left(V_{GS\_DC} + V_{pk}\, sin\frac{2 \cdot \pi \cdot t}{T} - V_{TH}\right)^2 dt. \tag{101}$$

The result of this definite integral is as follows.

$$I_{D\_DC\_EMI} = \frac{1}{T} \cdot \frac{K_p}{2} \cdot \frac{W}{L} \cdot \frac{T \cdot \left(2 \cdot V_{GS\_DC}^2 - 4 \cdot V_{GS\_DC} \cdot V_{TH} + 2 \cdot V_{TH}^2 + V_{pk}^2\right)}{2}. \tag{102}$$

After formal editing, the resulting equation is

$$I_{D\_DC\_EMI} = \frac{K_p}{2} \cdot \frac{W}{L} \cdot \left(V_{GS\_DC} - V_{TH}\right)^2 + V_{pk}^2 \cdot \frac{K_p}{4} \cdot \frac{W}{L}. \tag{103}$$

The original DC drain current is seen with an additional drain current caused by an EMI signal. This equation is valid for EMI peak voltage V_{pk} and V_{GS_DC} DC operating voltage in the following ranges.

$$V_{GS\_DC} > V_{TH} \bigwedge V_{pk} < V_{GS\_DC} - V_{TH}. \tag{104}$$

For the practical approach to the $I_{D\_DC\_EMI}$ equation, the following NMOS parameters are considered: $K_P = 100\ \mu A \cdot V^{-2}$, $V_{TH} = 0.8$ V, $W = 8\ \mu m$, $L = 2\ \mu m$, $V_{GS\_DC} = 0.996$ V and $V_{pk} = 0.1$ V like for the NPN BJT. The calculation leads to $I_{D\_DC} = 7.683\ \mu A$ and $I_{D\_DC\_EMI} = 8.683\ \mu A$ in strong inversion (up-threshold region). The relative current DC shift is approximately 13.0 %. This result, in the same order, was confirmed by the transient simulation.

The conclusion is that the NPN BJT is more sensitive to EMI than the NMOS transistor. This is why the BJTs in bandgap voltage reference need to pay more attention. On the other hand, it must be noted that MOS transistors in subthreshold regions similarly behave like BJTs. In some cases, MOSes need to pay attention as well. MOS transistors in the sub-threshold region can be used instead of BJTs but are usually not used in automotive bandgap designs due to their weakness in noise immunity [60].

Tab. 21. Comparison of theoretical calculations vs. simulation results.

EMI V_{pk} [mV]	Theoretical calculation				Simulation			
	I_{C_DC} [µA]	$I_{C\_DC\_EMI}$ shift [%]	I_{D_DC} [µA]	$I_{D\_DC\_EMI}$ shift [%]	I_{C_DC} [µA]	$I_{C\_DC\_EMI}$ shift [%]	I_{D_DC} [µA]	$I_{D\_DC\_EMI}$ shift [%]
25	7.680	24.5	7.683	0.8	7.685	20.4	7.682	0.9
50		116.2		3.3		89.0		3.8
100		890.1		13.0		444.6		15.2
250		195475.0		81.3		3518.0		91.2
500		$2.1 \cdot 10^9$		325.4		11440.0		326.0

Note that the BJT base current and intrinsic resistances were neglected for the $I_{C\_DC\_EMI}$ calculation, so higher EMI V_{pk} leads to higher error between calculation and simulation results. The MOS transistor is in strong saturation region.

Appendix 4 The Normal Distribution in Statistics

The normal (Gaussian) distribution according to [77], which is important in statistics and often used in the natural sciences, is generally described by a probability density function (pdf) of x values. The function is presented in following equations.

$$f_{pdf}(x) = \frac{1}{\sigma \cdot \sqrt{2 \cdot \pi}} \cdot e^{-\frac{(x-\mu)^2}{2 \cdot \sigma^2}}, \tag{105}$$

$$\mu = \frac{1}{n} \cdot \sum_{k=1}^{n} x_k, \tag{106}$$

$$\sigma = \sqrt{\frac{1}{n-1} \cdot \sum_{k=1}^{n} (x_k - \mu)^2}, \tag{107}$$

where σ is a standard deviation (sigma), and μ is an average or mean value. The average value can be classically calculated according to (106). The standard deviation can be calculated, in this case, by (107) suitable for a sample of the whole population. The probability that the x value will be within a required limit can be calculated by definite integration of the pdf. The definite integral of the pdf for x in the whole real range is equal to one, which means a 100 % probability that x is in this range [77].

$$P(-\infty < x < \infty) = \int_{-\infty}^{\infty} \frac{1}{\sigma \cdot \sqrt{2 \cdot \pi}} \cdot e^{-\frac{(x-\mu)^2}{2 \cdot \sigma^2}} dx = 1, \mu = 0 \tag{108}$$

Similarly, the probability that the x value will be in six sigma limits can be calculated as follows.

$$P(\mu - 6 \cdot \sigma < x < \mu + 6 \cdot \sigma) = \int_{\mu-6\cdot\sigma}^{\mu+6\cdot\sigma} \frac{1}{\sigma \cdot \sqrt{2 \cdot \pi}} \cdot e^{-\frac{(x-\mu)^2}{2 \cdot \sigma^2}} dx \approx 1, \tag{109}$$

The result leads to answering the question of what is beneficial for six sigma's designing. It is almost 100 % probability that circuit parameters will be within the required limits for a huge production, e.g., one million ICs. The Monte Carlo simulation with a modified algorithm is one of the design tools for a very high yield. The probabilities and numbers of fails per one million samples for x values with the normal distribution in required limits are summarized in Tab. 22.

Tab. 22. Probabilities that x values with normal distribution will be within limits.

Considered limit	P(x in limit) [%]	No of fails [pm]
$\mu \pm 1 \cdot \sigma$	68.2689	$317.311 \cdot 10^3$
$\mu \pm 2 \cdot \sigma$	95.4500	$45.500 \cdot 10^3$
$\mu \pm 3 \cdot \sigma$	99.7300	$2.700 \cdot 10^3$
$\mu \pm 4 \cdot \sigma$	99.9937	63.343
$\mu \pm 5 \cdot \sigma$	99.9999	0.573
$\mu \pm 6 \cdot \sigma$	~100.0000	$1.973 \cdot 10^{-3}$

Appendix 5 Matlab Script

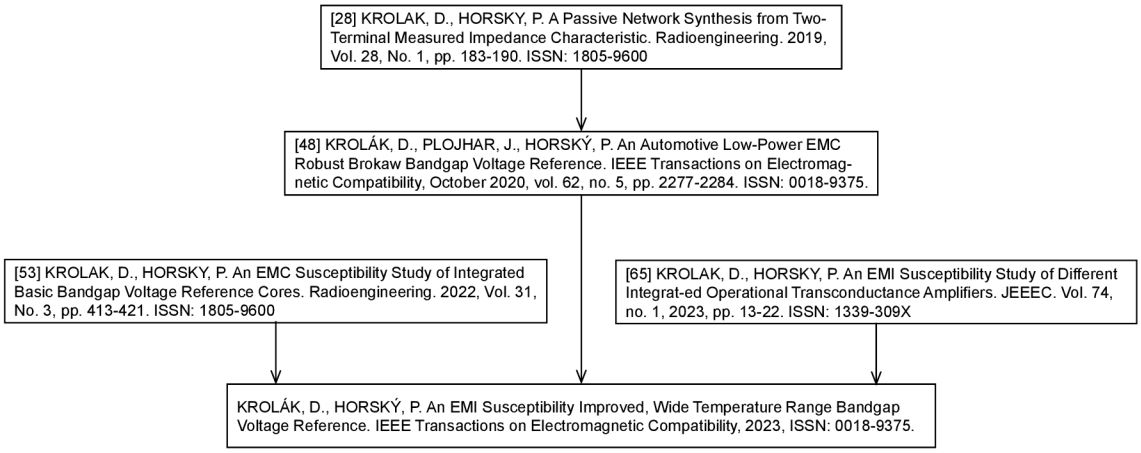
The executable Matlab script is saved on the enclosed CD or in the ZIP file for the case of the electronic version on the university web. The script was used for calculations of theoretical EMI sensitivity of main low-voltage semiconductor devices and statistical probabilities within normal distribution. The script is shown below.

```
% Close all figures, clear memory, and clear command window
close all
clear
clc

% Set output display format to the short engineering format with 4 decimal
% places and compact line spacing
format shortEng
format compact

% Define symbolic expression Ic_BJT(Vbe_dc + Vpk*sin(w*t)) and perform
% symbolic integration
syms Is Vbe_dc Vpk Vt T t x
expr = Is*(exp( ( Vbe_dc + Vpk*sin(2*pi*t/T) ) / Vt ) - 1 );
F = int(expr,t,-T/2,T/2)

% Mathematical trick for solving integral of previous symbolic expression
% in another way
expr = exp( ( Vpk*cos(x) ) / Vt );
F = int(expr,x,0,2.0*pi)

% Plot the Bessel functions of the first kind obtained in the integral result
% Jv(0 + j*x), v is order of function: 0..2, results for imaginary x values
x = -10:0.01:10;
J = zeros(3,2001);
for j = 0:2
    J(j+1,:) = besselj(j,0+x*1i);
end

figure(1)
plot(x,J)

grid on
legend('J_0','J_1','J_2','Location','Best')
title('Bessel Functions of the First Kind for $\nu \in [0, 2]$','interpret-
er','latex')
xlabel('x*1i','interpreter','latex')
ylabel('$J_\nu(0+x*1i)$','interpreter','latex')

% Plot in semilog the first order Bessel function of the first kind
% J0(0 + j*x), results for imaginary x values
figure(2)
semilogy(x,J(1,:))

grid on
```

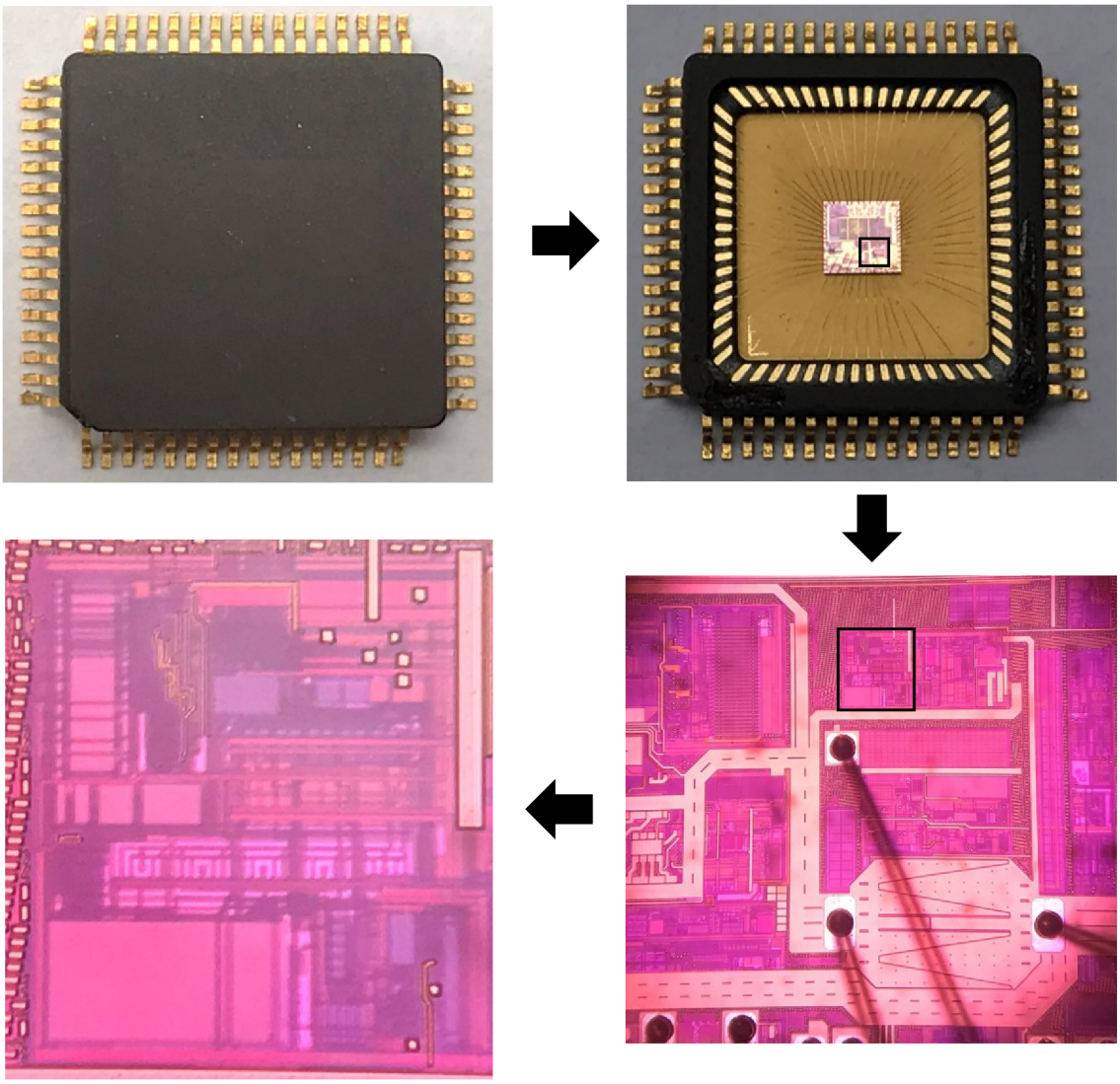
```
legend('J_0','Location','Best')
title('Bessel Functions of the First Kind for $\nu \in [0]$','interpret-
er','latex')
xlabel('x*1i','interpreter','latex')
ylabel('$J_\nu(0+x*1i)$','interpreter','latex')

% Clear memory and plot 3D graphs of the first-order Bessel function of the
% first kind
clear

x = -10:0.1:10;
y = x';
z = x + 1i*y;
Jnew = besselj(0, z);

% Imaginary part in 3D
figure(3)
surf(x,y,imag(Jnew))

title('Bessel Function of the First Kind - Imaginary Part of J0','interpret-
er','latex')
xlabel('real(z)','interpreter','latex')
ylabel('imag(z)','interpreter','latex')

% Real part in 3D
figure(4)
surf(x,y,real(Jnew))

title('Bessel Function of the First Kind - Real Part of J0','interpret-
er','latex')
xlabel('real(z)','interpreter','latex')
ylabel('imag(z)','interpreter','latex')

% Clear memory, define symbolic expression Id_NMOS(Vgs_dc + Vpk*sin(w*t))
% and perform symbolic integration
clear

syms Kp W L Vgs_dc Vpk Vth T t
expr = (Kp/2.0)*(W/L)*(Vgs_dc + Vpk*sin(2*pi*t/T) - Vth)^2;
F = int(expr,t,-T/2,T/2)

expr = (Vgs_dc + Vpk*sin(2*pi*t/T) - Vth)^2;
F = int(expr,t,-T/2,T/2)

% Clear memory, calculate BJT collector current without and with 0.1 Vpk EMI
clear

Is = 1.0E-8;        % A
Vt = 0.026;         % V at 27 degC
Vbe_dc = 0.8551;    % V
Ae = 4.0E-12;       % m^2
Vpk = 0.1;          % V

Ic_dc = Is*Ae*(exp(Vbe_dc/Vt) - 1)                              % A
Ic_dc_EMI = Is*Ae*(exp(Vbe_dc/Vt)*besselj(0,(Vpk*1i)/Vt) - 1)   % A
```

```
Ic_dc_rel_shift = (Ic_dc_EMI/Ic_dc - 1)*100                    % %

% Clear memory, calculate NMOS drain current without and with 0.1 Vpk EMI
clear

Kp = 100E-6;        % A/V^2
Vth = 0.8;          % V
Vgs_dc = 0.996;     % V
W = 8.0E-6;         % m
L = 2.0E-6;         % m
Vpk = 0.1;          % V

Id_dc = Kp/2.0*W/L*(Vgs_dc - Vth)^2                                % A
Id_dc_EMI = Kp*W*(2*Vgs_dc^2 - 4*Vgs_dc*Vth + Vpk^2 + 2*Vth^2)/(4*L) % A
Id_dc_rel_shift = (Id_dc_EMI/Id_dc - 1)*100                        % %

% Clear memory, calculate probability of x value in 1 to 6 sigma limits
% within the normal distribution
clear

u = 0; % average value
s = 1; % 1 sigma value
fpd = @(x) 1/(s.*sqrt(2.*pi)).*exp(-(x-u).^2/(2*s.^2));

P_x_in_1s_limit = integral(fpd,-1,1)*100.0  % %
P_x_in_2s_limit = integral(fpd,-2,2)*100.0  % %
P_x_in_3s_limit = integral(fpd,-3,3)*100.0  % %

P_x_in_4s_limit = integral(fpd,-4,4)*100.0  % %
P_x_in_5s_limit = integral(fpd,-5,5)*100.0  % %
P_x_in_6s_limit = integral(fpd,-6,6)*100.0  % %

% Calculate the fail probability of x value out of 1 to 6 sigma limits
% within the normal distribution
Fails_pm_1s = (100.0 - P_x_in_1s_limit)*1.0E6/100.0  % per one million
Fails_pm_2s = (100.0 - P_x_in_2s_limit)*1.0E6/100.0  % per one million
Fails_pm_3s = (100.0 - P_x_in_3s_limit)*1.0E6/100.0  % per one million

Fails_pm_4s = (100.0 - P_x_in_4s_limit)*1.0E6/100.0  % per one million
Fails_pm_5s = (100.0 - P_x_in_5s_limit)*1.0E6/100.0  % per one million
Fails_pm_6s = (100.0 - P_x_in_6s_limit)*1.0E6/100.0  % per one million

% Calculation of values for the first order Bessel function of the first
% kind with imaginary parameter
for j = 1:100
    Bessel_1st_order(j) = besselj(0,0+j*0.1*1i)
    x = j*0.1*1i
end
```

Appendix 6 The Diagram of Science Publications



Appendix 7 The Second Test Chip Photos



On the bottom left is the proposed EMC robust voltage reference as a die micro-photograph after gradual zooming in.

Appendix 8 CURRICULUM VITAE

Name:	David KROLÁK
Born:	July 12th 1991 in Frýdek-Místek
Contact:	David.Krolak@vutbr.cz

Education

2011-2014	Brno University of Technology / Department of Radio Electronics The Bachelor's Degree in the field Electronics and Communication, full-time study The final state examination passed in June 2014 Bachelor thesis: *Mixing board with class-AB output amplifier*
2014-2016	Brno University of Technology / Department of Radio Electronics The Master's Degree in the field Electronics and Communication, full-time study The final state examination passed in June 2016 Diploma thesis: *Module for verification of rotational position sensors*
2016-2023	Brno University of Technology / Department of Radio Electronics The Ph.D. Degree in the field Electronics and Communication Technologies, distance study Doctoral thesis: *An EMC robust precise voltage reference for automotive applications*

Courses

2017	Tomas Bata University in Zlín / Faculty of Applied Informatics Electromagnetic Compatibility for Industrial Practice
2018	H Test / Keysight Technologies in Prague Signal Integrity Measurement Insights
2019	University of Pardubice / Faculty of Electrical Engineering and Informatics / Rohde & Schwarz – Vector Network Analysis
2020	Tomas Bata University in Zlín / Rohde & Schwarz EMC Seminar – Discover the Secrets in EMI Debugging
2021	onsemi in Brno, Siemens – Solido Design Environment
2023	Škoda in Mladá Boleslav / Rohde & Schwarz Seminar – Innovation in Automotive Testing

Additional

Languages	Czech – mother language English – upper intermediate (B2) German – elementary (A2) Spanish – elementary (A2)
Skills	Analog circuit design, electrical mixed-mode simulations, electrical measurements, programming (C, C++, C#, VB, Python, VHDL), embedded systems programming (AVR, ARM), LabVIEW, Matlab, Altium, and Eagle PCB design.