BRNO UNIVERSITY OF TECHNOLOGY

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF MICROELECTRONICS

ÚSTAV MIKROELEKTRONIKY

SOLAR POWER INVERTER

MĚNIČ PRO FOTOVOLTAICKÉ PANELY

MASTER'S THESIS

DIPLOMOVÁ PRÁCE

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VEDOUCÍ PRÁCE

BRNO 2016

BRNO FACULTY OF ELECTRICAL
UNIVERSITY ENGINEERING
OF TECHNOLOGY AND COMMUNICATION

Master's Thesis

Master's study field **Microelectronics**
Department of Microelectronics

Student: Bc. Petr Gottwald   **ID:** 145997

Year of study: 2   **Academic year:** 2015/16

TITLE OF THESIS:

Solar power inverter

INSTRUCTION:

The aim of the work is to design and realize inverter for power convertion. The DC current from photovoltaic panels will be converted to alternating with the effective value of the output voltage 230V. Based on a study the most appropriate topology will be selected and reached parameters will be verified by measurements. To control system use FPGA.

RECOMMENDED READING:

Podle pokynů vedoucího práce

Date of project specification: 8.2.2016   **Deadline for submission:** 26.5.2016

Leader: Ing. Michal Pavlík, Ph.D.
Consultant Master's Thesis:

doc. Ing. Lukáš Fujcik, Ph.D., *Subject Council chairman*

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Diplomová práce

magisterský navazující studijní obor **Mikroelektronika**

Ústav mikroelektroniky

Student: Bc. Petr Gottwald   *ID:* 145997

Ročník: 2   *Akademický rok:* 2015/16

NÁZEV TÉMATU:

Měnič pro fotovoltaické panely

POKYNY PRO VYPRACOVÁNÍ:

Navrhněte a realizujte měnič pro konverzi stejnosměrného proudu z fotovoltaických panelů na střídavý s efektivní hodnotou výstupního napětí 230V. Na základě studie vyberte nejvhodnější topologii, jejíž parametry ověřte měřeními. Pro řízení využijte obvod FPGA.

DOPORUČENÁ LITERATURA:

Podle pokynů vedoucího práce

Termín zadání: 8.2.2016   *Termín odevzdání:* 26.5.2016

Vedoucí práce: Ing. Michal Pavlík, Ph.D.

Konzultant diplomové práce:

doc. Ing. Lukáš Fujcik, Ph.D., *předseda oborové rady*

ABSTRAKT

Tato práce se zabývá návrhem výkonového měniče určeného pro použití ve fotovoltaických systémech. Klíčovým je použití programovatelného hradlového pole (FPGA) pro realizaci řídicích funkcí. Do detailu jsou diskutovány aspekty návrhu spínaných měničů a na základě takto získaných poznatků je zkonstruován funkční vzorek měniče.

KLÍČOVÁ SLOVA

FPGA, VHDL, zvyšující měnič, můstkový měnič, MPPT, fotovoltaický panel

ABSTRACT

This thesis deals with design of a power converter intended for use in photovoltaic systems. The main feature is the use of Field-Programmable-Gate-Array as the main control block. The aspects of power converter design are discussed in detail. Based on gathered knowledge, a working prototype of the solar power inverter is designed.

KEYWORDS

FPGA, VHDL, boost converter, full-bridge converter, MPPT, photovoltaic panel

PROHLÁŠENÍ

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V Brně dne ....

                                                              (podpis autora)

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Introduction

In the modern world, renewable, clean sources of electrical power are becoming increasingly important. Traditionally, the biggest proportion of electricity produced worldwide has been produced in coal-fired power plants, followed by energy from nuclear power plants during the last few decades.

However, coal reserves are getting smaller over the time, burning of coal in power plants is considered to be one of the most important sources of greenhouse gases and other potentially hazardous substances. Further, damage to the nature as result of coal mining in mining areas is a well known issue.

Solar power is considered clean, although building of these power plants in the nature is sometimes disputed. Nevertheless, solar power is strongly benefited in the last few years.[1] On the other hand, in contrary to more traditional methods where electricity is produced by alternators (which produce AC sinusoidal output voltage), more sophisticated methods and additional circuits are needed in PV systems to produce AC voltages usable in a supply network.

Usually these power converter circuits are MCU/DSP-controlled. Efficiency is mostly higher than 90 % (e.g. Sunny Boy product series from SMA company has highest specified efficiency in excess of 95 % at full output power). The purpose of this master's thesis is to introduce an alternative approach that utilizes Field programmable gate array (FPGA) circuit instead of MCU for performing control functions. FPGAs provide compared to MCUs additional design flexibility and parallel signal processing capabilities.

This thesis is divided into following sections. In the first section, power conversion process is discussed in detail. A detailed overview of converter topologies is carried out in the first section. In the second section, the most suitable converter topology is selected and circuits are simulated. Originally, there was an intent to build a converter with 1 kW output power capability. However, the cost of such a solution turned out to be excessively high. Thus, practical realization has been limited to output power of 250 W[1].

In the third section, the required converter and control circuits are designed. Printed circuit boards are designed and design steps are explained. Photographs of assembled boards are provided in this section. CAD software EAGLE 5.6.0. and OrCAD Capture 16.5. were used to draft the design schematics. Boards were designed in EAGLE 5.6.0. and Cadence Allegro PCB Designer.

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[1] Unit Watt (W) is used throughout this thesis. Unit VA (Voltampere) could be used as well, since the output voltage and currents are AC. Therefore, purely resistive load is assumed.

In the fourth section of the thesis, VHDL description is created based on requirements of the final circuit. The respective blocks of the design are described and in some cases, block diagrams are present to improve the readers' understanding of the presented solution.

Finally, assembled circuit boards were tested and measurement results were processed. Oscillographs are provided as they were found to be more interesting for the reader than raw numerical data.

1 Power Conversion process

Solar panels described in the previous chapter typically produce DC voltage in the range of tens of volts to few hundred volts. This voltage has to be converted to AC voltage in order to make it available for the supply network. Value of the AC voltage and its frequency is usually given by standards in the respective country. Moreover, power converters have to be designed in such a way that maximal output power available for a given illumination level is always utilized. This feature of power converters is called MPPT, which stands for Maximum Power Point Tracking. MPPT is, more precisely said, measurement of I-V characteristics. [2],[3]

Furthermore, AC output voltage must be very carefully synchronized with supply voltage network voltage - it must have the same frequency and no phase shift.

Nowadays, power converters for solar panels are offered by many companies worldwide. Power levels are in the range of few hundred watts for low power converters to hundreds of kilowatts for high power solar systems. Higher output power levels are usually obtained by series- or parallel connecting of solar panels. Topologies utilized in these converters are boost converter (as the DC-DC stage) and full-bridge topology as the DC-AC stage, even though some isolated push-pull designs of DC-DC stage and even resonant LLC stage for output DC-AC inverter have been reported in the literature.[4] In this thesis, few topologies are compared based on expected output power, desired efficiency and power semiconductor requirements.
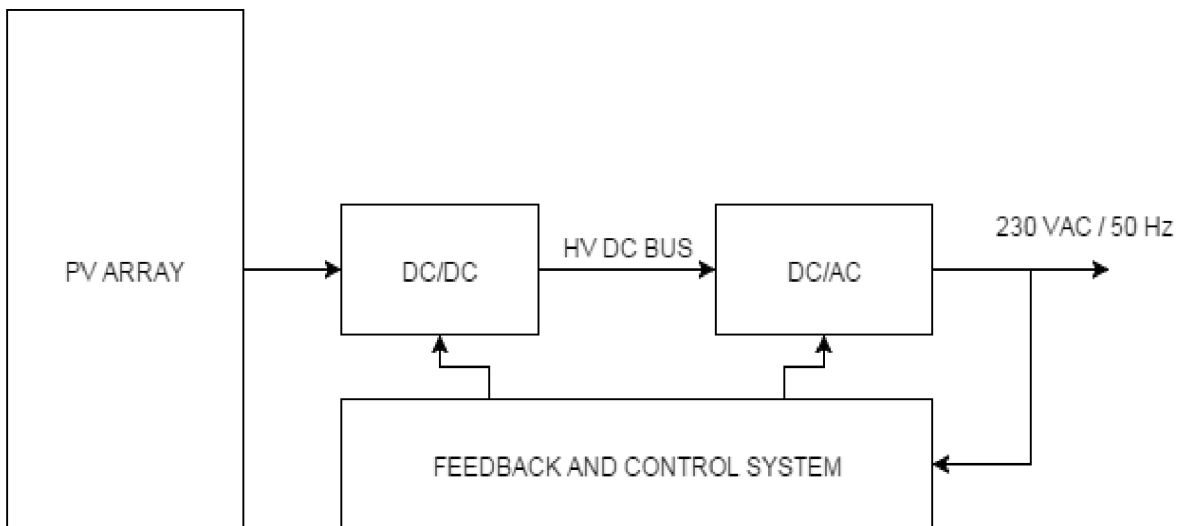
Figure 1: Solar power conversion system block diagram [1][2][3][4]

1.1   DC-DC stage theoretical analysis

The main task of the DC-DC converter stage is to step up the input voltage supplied by PV panel to a higher voltage. Few topologies can be used in this stage:

- Boost converter,

- forward converter,

- push-pull converter,

- half-bridge converter,

- full-bridge converter.

1.1.1   Power semiconductors

Basically, any device capable of controlled switching can be used in this stage, like SCR, GTO, IGBT, bipolar transistor or MOSFET.

1.1.2   Boost converter

Boost converter is an example of a non-isolated, transformer-less topology. The basic circuit consists of an inductor L, a switch SW (a transistor in most cases), a boost diode D and of an output filter capacitor C.
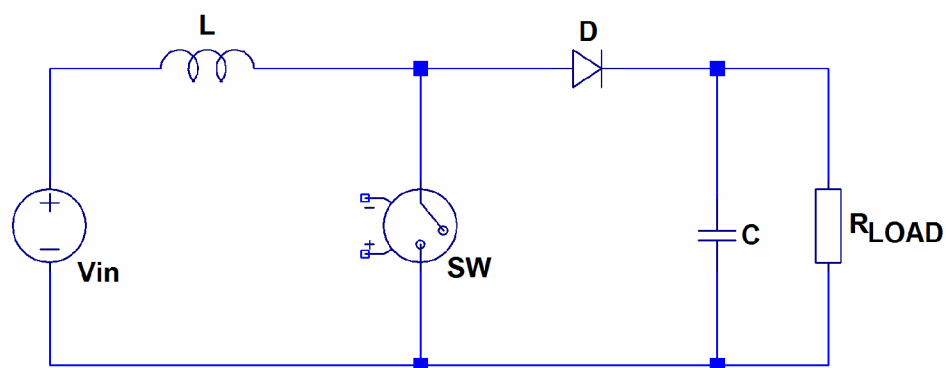
Figure 2: Boost converter simplified schematic diagram[5][6]

Assuming steady state operation (output voltage at its nominal value and constant load and inductor current never falls to a zero value), operation principle can be explained as follows:

During the t_1 period (fraction of total period T) the switch SW is in the on-state, the input voltage is applied to the inductor L and the inductor L is thus being charged by linearly rising

current i_L. Boost diode is in the cut-off state and the load current is being supplied solely from the output capacitor C. After the t_1 period has elapsed, switch SW is turned-off. Following equations can be written:

$$t_1 = D \cdot T \tag{1}$$

$$V_L = L \cdot \frac{di}{dt} \Rightarrow di = \frac{V_L}{L} dt \tag{2}$$

$$i = \frac{V_L}{L} \int_0^{D \cdot T} dt = \frac{V_L}{L} \cdot D \cdot T \tag{3}$$

where t_1 is the on-time of the switch [s], D is duty cycle [-], i_L is the inductor current [A], V_L is the voltage across the inductor L [V], T is the whole switching period [s] and L is the inductor inductance [H].

After the switch SW has been turned-off, voltage of reversed polarity appears across the inductor. At the same time, current through inductor is decreasing linearly to its initial value at the beginning of the first phase. Hence, to satisfy this condition, the average current change through the inductor is essentially zero as well as the average voltage across the inductor is zero. The equation (3) can be rewritten to apply to the time interval t_2, assuming that t_2 is:

$$T - D \cdot T = D \cdot T \tag{4}$$

$$i_{L,t2} = \frac{V_L}{L} \int_{D \cdot T}^{T} dt = \frac{V_{OUT} - V_{IN}}{L} \cdot (1 - D) \cdot T \tag{5}$$

If the average inductor current change during period is zero, then the following applies:

$$\Delta I_{L,t1} = \Delta I_{L,t2} \tag{6}$$

$$\frac{V_{OUT} - V_{IN}}{L} \cdot (1 - D) \cdot T = \frac{V_{IN}}{L} \cdot D \cdot T \tag{7}$$

Which yields the output voltage as a function of the input voltage V_{IN}:

$$V_{OUT} = V_{IN} \cdot \frac{1}{1 - D} \tag{8}$$

This DC input-to-output transfer function can be visualized as shown in the Figure 3:
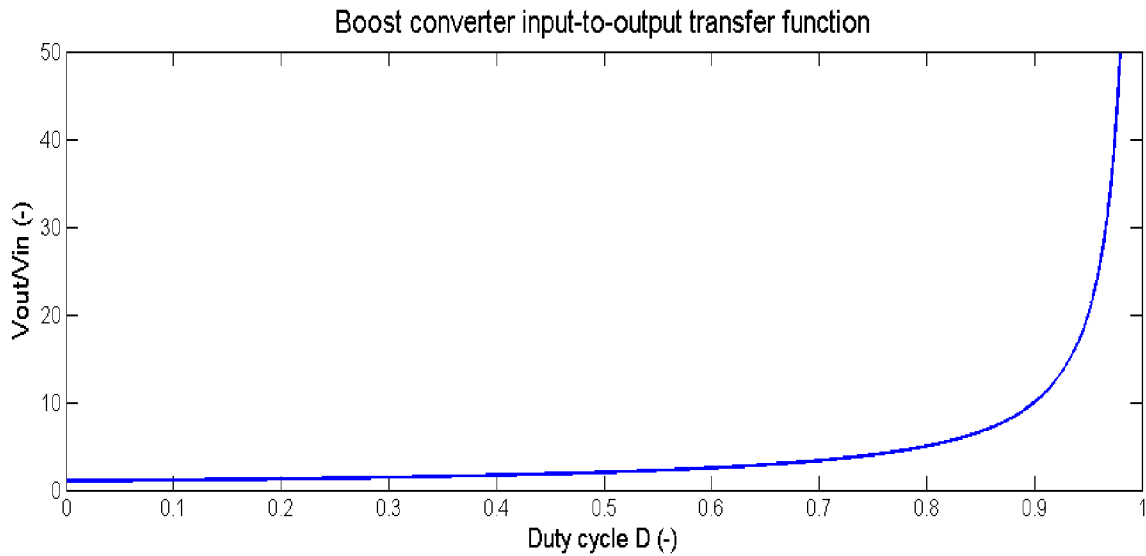
Figure 3: Boost converter input-to-output transfer function

The above described case is called Continuous conduction mode, or CCM for short.

As can be clearly seen, in CCM, the lower boundary for the output voltage is the input voltage when D = 0, whilst the higher boundary is theoretically infinite. Nonetheless, some practical limits do exist. Switch breakdown voltage (like for example collector-to-emitter voltage of a bipolar transistor) as well as boost diode reverse breakdown voltage are two main constraints.

The second case is called discontinuous conduction mode, or DCM for short. In DCM, the output voltage is not only dependent on duty cycle, it also depends on switching period, load resistance and boost inductor inductance. However, in practical circuits, constant output of these circuits is usually maintained by utilizing negative feedback, which is in turn used to alter duty cycle depending on instantaneous load current. DCM may be desirable, when output power is low and/or low value boost inductor has to be used. Main disadvantage is that RMS current is generally higher than in the CCM since the peak boost inductor current must be more then twice the value of the average current. On the other hand, there is practically no turn-on loss in the main switch - the main switch turns-on while no current is flowing through it.[5][6]
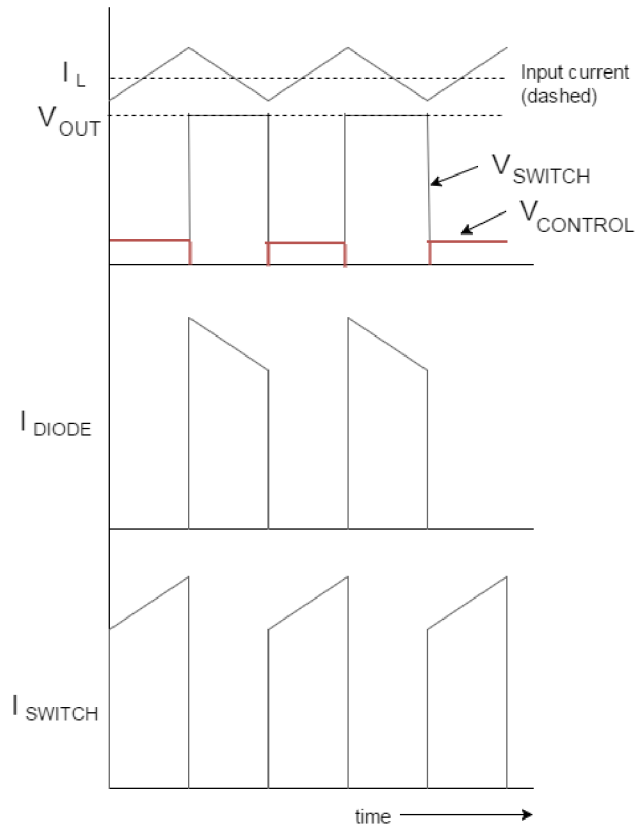
Figure 4: Boost converter steady state voltage and current waveforms (CCM)

1.1.3 Parasitic effects in passive and semiconductor devices

Parasitic effects are caused by circuit parasitic elements. These include parasitic resistances of the PCB, of the boost inductor, of the equivalent series resistance of capacitors, semiconductor switches' voltage drops. These parasitic elements cause reduction of efficiency or, in the case of parasitic inductances and capacitances, EMC issues.
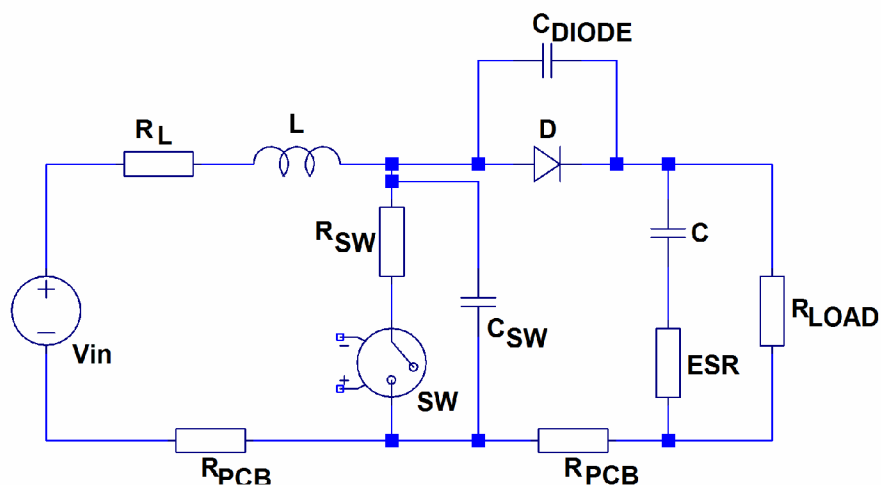
Figure 5: Boost converter schematic including parasitic circuit elements

Since these effects occur generally in all switching converter topologies, the previously described boost converter is used to demonstrate these effects, rather than doing this for each topology separately.

The power losses in all types of power converters can be divided into following groups:

- Conduction and leakage losses,

- switching losses.

Instantaneous conduction losses can be calculated as:

$$p(t) = v(t) \cdot i(t) \tag{9}$$

Where $p(t)$ is power loss [W], $v(t)$ is voltage drop [V] and $i(t)$ is current flowing through the circuit [A]. All values are instantaneous, which means, for a given time t.

Leakage losses are caused by leakage currents flowing through switching devices, when they are in the off-state. Unlike an ideal switch, a small amount of current is flowing during the off-period, possibly generating significant loss.

Switching losses arise from three reasons. First, parasitic capacitances of circuit elements are being charged during every switching period to a certain voltage value. In the previously discussed boost converter example, this voltage across the switch equals the output voltage V_{OUT}. Parasitic capacitors are denoted C_{SW} and C_{DIODE}, respectively. Capacitive switching loss can be calculated as energy stored in a capacitor times switching frequency (or divided by switching period):

$$P = \frac{C \cdot V_c^2}{2 \cdot T} \tag{10}$$

Where P is the power loss [W], C is the capacitance of parasitic capacitor [F], V_C is voltage across parasitic capacitor [V] and T is switching period [s].

Second, parasitic and leakage inductances are being charged every switching period by the current flowing through them. Analogously to previous capacitive switching loss example, inductive switching loss can be calculated as energy stored in parasitic inductance times switching frequency (or divided by switching period):

$$P = \frac{L_{PAR} \cdot I^2}{2 \cdot T} \tag{11}$$

Where P is the power loss [W], L_{PAR} is parasitic inductance [H], I is current flowing through the circuit [A] and T is the switching period [s].

It is important to note that leakage inductance is the biggest problem in switching converters that use coupled inductances - or transformers for transferring energy. For example in boost converter, if there was a PCB trace inductance in series with boost inductor, the parasitic inductance would have been added to the inductance of the boost inductor.

Semiconductor switching losses are the third reason. When switching devices are changing state from conducting to non-conducting and vice versa, there is, for a short time period, current flowing through the device while the voltage across the device is rising very rapidly, thus causing power loss. This switching mode is called "hard switching". There is a different mode, called "soft switching" or resonant switching.[7][8][9] Figure 6 shows the difference.
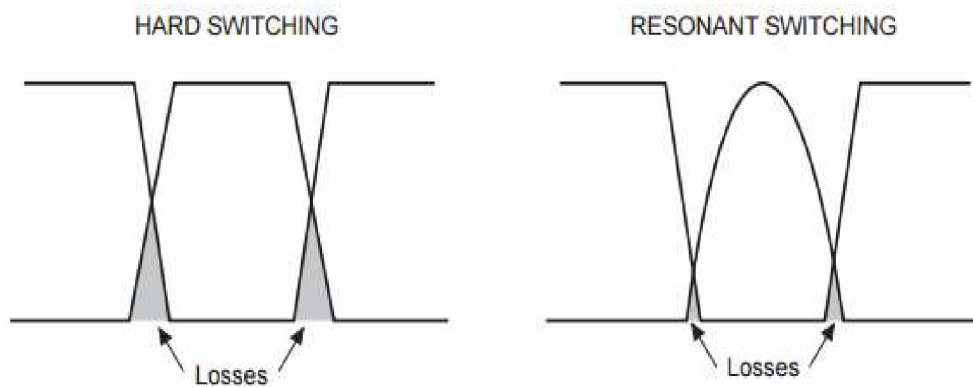
Figure 6: Difference between hard and soft switching. Current and voltage waveforms and the resulting power loss (grey-shaded). Source:[10]

In the following paragraph, a short overview of power semiconductors (bipolar transistors, IGBT, MOSFETs and GTOs) is shown.

- bipolar transistor - needs a current supplied to the base, which is proportional to the collector current. Breakdown voltage is in the range of >1 kV for some devices, collector current in the range of tens of Amperes. High switching loss, caused by minority carrier recombination, slow rise and fall times. Moreover, it exhibits storage time and tail current. Low conduction loss, when enough base current is supplied,

- IGBT - does not need current supplied to the gate during steady state operation, it is voltage-driven. Breakdown voltage exceeds 1 kV for many devices, devices with maximal collector current up to few hundred Amperes are available. However, it is a minority carrier device, thus exhibits rather high switching losses.

Low conduction loss. High switching losses can be decreased by using soft switching techniques,

- MOSFET - voltage-driven just like IGBT. On-resistance increases proportional to rated voltage, thus increasing conduction losses at high voltage. Low switching losses,

- GTO - or Gate Turn-Off Thyristor - turned-on by current pulse supplied to the gate, turned-off by negative gate current pulse. Very low conduction losses, very slow switching, thus high switching losses, mainly intended for high current, high voltage applications like for instance traction, seldom used in power converters.

Based on these properties and due to their availability, only MOSFETs and IGBTs will be considered in further discussion. In the following subsections the other most widely used topologies are briefly discussed.

1.1.4 Push-pull converter

Push-pull converter is a power converter topology that utilizes power transformer to transfer energy from the input to the output. Energy is transformed to the load during the switches' on-time. Transformer has a center-tapped primary winding (that means, having two separate primary windings with exactly the same number of turns, however wound in such a fashion that magnetic flux excited by one winding during the first operational phase is cancelled-out during the second operational phase, thus ensuring transformer core reset) and a secondary winding, which can also be center-tapped, although this is not necessary. Block diagram is shown in Figure 7.[5][6]
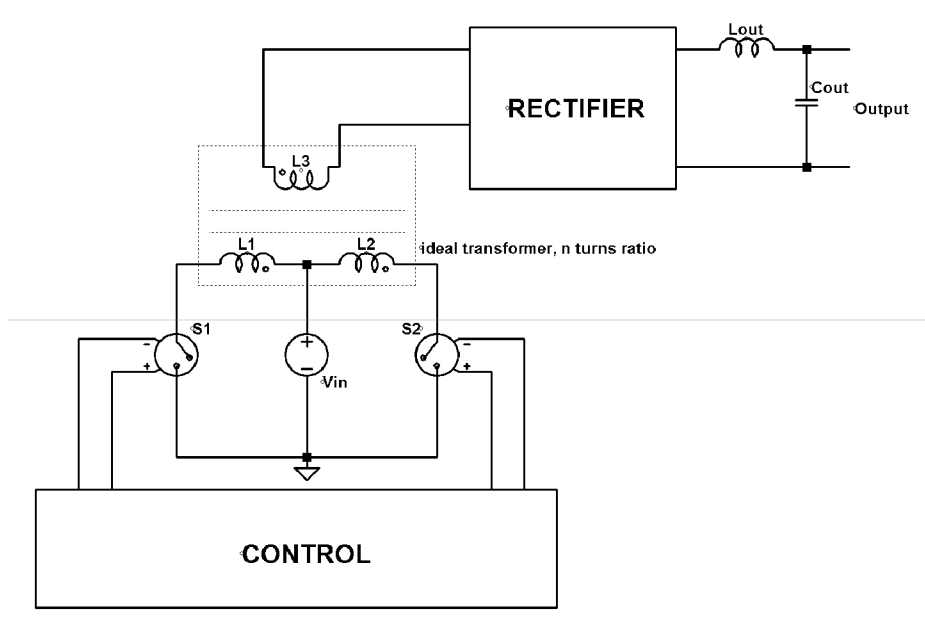
Figure 7: Push-pull converter block diagram. Note the phase dots in the transformer schematic symbol

Compared to boost converter, push-pull converter provides galvanic insulation between primary and secondary windings. Switches may be rated at lower voltage, because the higher output voltage is achieved by means of adjusting primary to secondary turns ratio. Penalty for this is higher circuit complexity and risk of transformer core saturation when the transformer is not properly designed or wound. Furthermore, the leakage inductance causes undesired energy storage and voltage spikes across switches. Note that the output filter consisting of capacitor C_{OUT} and L_{OUT} is mandatory. If there was no inductor in the output path, the capacitor C_{OUT} would be charged by rectangular shaped voltage from the transformer secondary winding, with current rate-of-rise limited only by capacitor equivalent series resistance and transformer leakage inductance.

Having an ideal transformer without leakage inductance, the output voltage is given by:

$$V_{OUT} = 2 \cdot n \cdot V_{IN} \cdot D \tag{12}$$

Where n is primary and secondary windings turns ratio [-], V_{IN} is the input voltage [V] and D is the duty cycle [-].

This equation is multiplied by two, because each transistor can be turned-on only for one half of the switching period T, thus D is dimensionless number smaller than 0,5. (D < 0,5). Furthermore, the equation is multiplied by duty cycle D, since the output filter acts as a low-pass filter, whose output voltage equals to the average value of the input voltage. This

assumption can be made in the case of other topologies using this type of output filter (half- and full-bridge and forward converter) as well.

It is interesting to note that the input voltage, when applied to one of the transformer primary windings, is reflected back to the second primary winding. Thus, the switches used in this converter must withstand voltage of at least twice the value of the input voltage.

The rectifier block shown in Figure 7 may consist either of Graetz bridge rectifier (when the secondary winging is single) or a center-tapped rectifier consisting of two diodes can be used.

1.1.5 Half-bridge converter

Another power converter topology utilizing power transformer is half-bridge converter. Similarly to push-pull converter, two switches are used. Similarly to the push-pull converter, these switches are never turned-on simultaneously. Supply voltage is divided by two by a capacitive voltage divider and then applied to the primary winding of the transformer. However, there are two drawbacks, namely:

- Since the voltage applied to the primary winding is halved, the secondary winding number of turns must be doubled to achieve the desired output voltage. This may increase winding conduction loss,

- likewise, the average current flowing through primary winding is two times greater than in push-pull converter, because the same output power is supplied at one half of the input voltage. This in turn increases conduction loss in primary winding and switches. It also requires high quality, low-ESR capacitors to be used in the capacitive voltage divider.
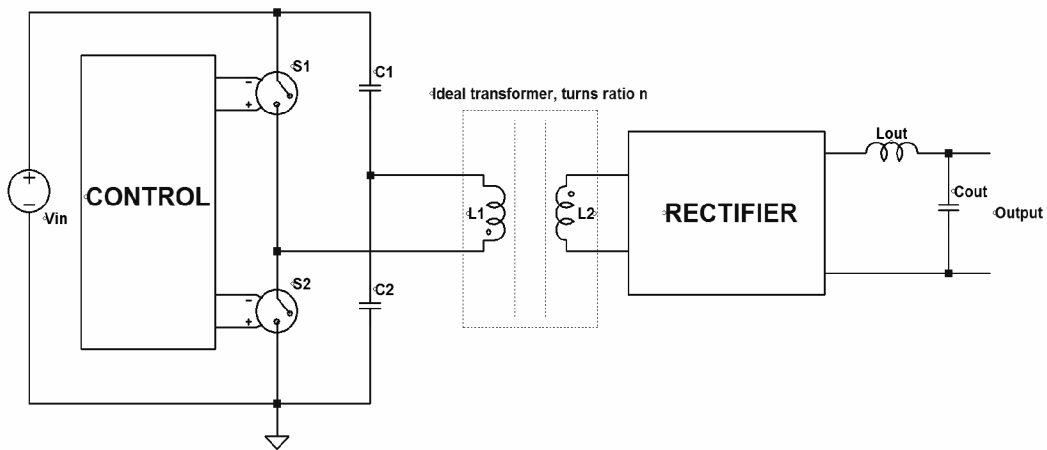
Figure 8: Half-bridge converter block diagram [5][6]

Again, when an ideal transformer having no leakage inductance and having turns ratio n is considered, the steady state output voltage is given by:

$$V_{OUT} = 2 \cdot n \cdot \frac{V_{IN}}{2} \cdot D = V_{IN} \cdot D \cdot n \tag{13}$$

This topology will not be further considered.

1.1.6   Full-bridge converter

By replacing voltage divider capacitors (C_1 and C_2 in Figure 8) with switches, the full bridge topology (or sometimes called H-bridge) has been created. Just like in the half-bridge topology, the switches S_1 and S_2 must not be turned-on simultaneously - this would cause short circuit of the input power supply and eventual damage to switches, PCB copper traces etc. The same applies for switches S_3 and S_4.
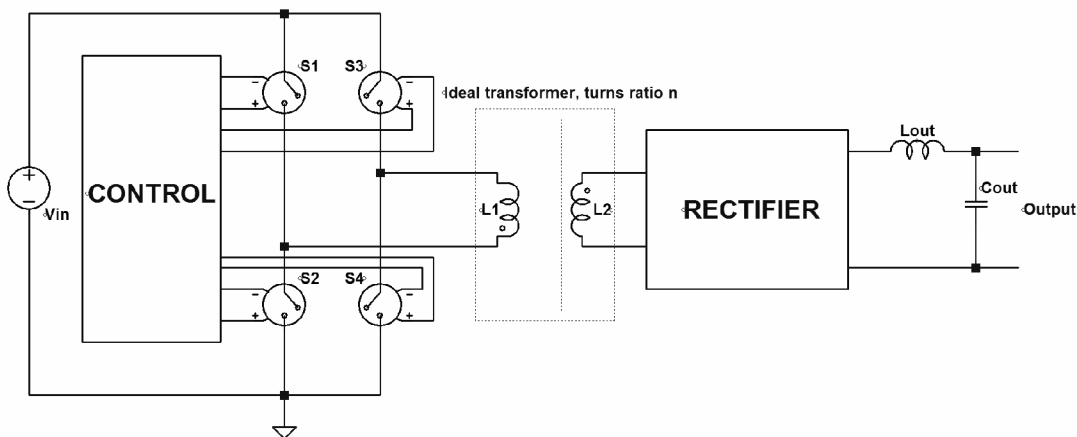
Figure 9: Full-bridge converter block diagram [5][6]

It can be seen that half- and full-bridge topologies have their upper switches, or more precisely said, their gates not referenced to ground. Thus, to drive these switches correctly a gate (or base when bipolar transistor is utilized) drive transformer or bootstrap circuit must be used. This poses a disadvantage over the push-pull or single-switch topologies like for example boost, forward or flyback converter.

2 DC-DC and DC-AC stage design

Particularly attractive is boost topology due to its inherent simplicity. However, switching losses can be high, because the main switch sees the full output voltage - that is at least 390 V_{DC}. Push-pull topology is also attractive, since it has ground referenced switches. Furthermore, low voltage, high current MOSFETs with low $R_{DS(On)}$ can be used. However, leakage inductance will most likely cause voltage spikes. Half- and full bridge topology are rather complex and therefore are not considered for this stage. In the following section, component values of a 1 kW boost an push-pull converter and calculated and resulting circuits simulated using LTspice IV simulator.

2.1 Example boost converter design

These parameters are known or given:

- Output power 1 kW

- Input voltage < 90 V_{DC}

- switching frequency 20 kHz

By rearranging equation   (8)
the duty cycle can be determined (at lowest input voltage):

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{40}{390} = 0{,}88 \qquad (14)$$

V_{IN} is considered 40 V_{DC} [2] and V_{OUT} is 390 V_{DC}, which yields D = 0,88. This in turn yields switch on-time of 44 µs. Then, the average input current at lowest input voltage of 40 V_{DC} can be determined, assuming efficiency of 95 %:

$$I_{IN(MAX)} = \frac{P_{OUT}}{V_{IN} \cdot \eta} = \frac{1000\,W}{40\,V \cdot 0.95} = 26{,}3\,A \qquad (15)$$

Where P_{OUT} is the output power [W], V_{IN} is the input voltage [V] and η is the efficiency [-].

Now, the inductor current ripple has to be determined. Albeit the value can be chosen arbitrarily, the lower the current ripple is, the lower is the maximal current flowing through

---

[2] The value of 40 V was selected based on typical output voltage values of solar panels available on the market. It is likely that PV panel array would output higher voltage at 1 kW power levels. Thus, the value of 40 V should represent an extreme case, because current stresses are highest at lowest supply voltage (higher average input current).

the inductor and the switch and through the boost diode. The value has been chosen to be 10 A or ±5 A. Thus, the maximal inductor current at full load is (26,3 + 5 = 31,3) A.

The required inductance can be calculated as follows:

$$L = \frac{V_{IN} \cdot t_{ON}}{\Delta I_L} = \frac{40\,V \cdot 44\,us}{10A} = 190uH \tag{16}$$

Where L is the inductance of the inductor [H], V_{IN} is the input voltage [V] and t_{ON} is the switch on-time [s].

Thus, taking into account that an inductor may begin to saturate at lower currents, when its temperature increases, an inductor with inductance value of at least 220 μH is required. The same applies for current rating - a safety margin must be taken into account. Thus, an 220 μH inductor rated at current of 40 A has to be used. For instance, EK55246-221M-50AH inductor from Coil Winding Specialist, Inc. could be used. The initial inductance value of 220 μH reduces to 157 μH at 35 A DC bias current. Alternatively, a multiphase boost topology [9] can be used.

Assuming four phases operating in parallel gives approximately (24 A / 4), that is 6 A average current per one phase. The current ripple remains still the same. For the purpose of the simulation, an 220 μH, 15 A inductor PCV-2-224-08L having series resistance of 37,5 mΩ from Coilcraft has been chosen for each phase.

However, the switching frequency is relatively low. As a result, the converter will enter the Discontinuous conduction mode at either higher input voltage or lighter load (because the average input current decreases). As has already been mentioned, in DCM, the voltage input-to-output transfer function is dependent not only upon duty cycle, it depends also on output current, switching frequency and inductance. This transition could be avoided either by increasing converter switching frequency or by increasing inductor inductance. The latter case is rather unfeasible, as high inductance value inductors get bulky and expensive and manufacturers of inductors usually do not supply inductance versus frequency characteristics of their products (for instance, the inductor PCV-2-224-08L mentioned earlier is characterized only at frequency of 18,5 kHz). Thus, the converter will run in DCM.

2.1.1 Boost switch selection

The switch used must be selected to withstand voltage of at least:

$$V_{MAX} = V_{OUT} + V_{MARGIN} \tag{17}$$

Where V_{OUT} is the output voltage and V_{MARGIN} is safety margin to ensure that switch breakdown voltage is never exceeded.

Moreover, the switch must be able to conduct current of at least:

$$I_{MAX} = I_{PK} + I_{MARGIN} \tag{18}$$

Where I_{PK} is the peak current flowing through one converter phase [A] and I_{MARGIN} is safety margin to ensure that maximal rated current of the switch is never exceeded [A].

Suitable MOSFET is SPA11N60C3 from Infineon, which has On-state resistance of 0,34Ω. To further reduce the resistance, four transistors are connected in parallel in each converter phase. Boost diode is MUR460, ultra-fast recovery diode rated at 600 V and average forward current of 4 A. Resulting waveforms are shown in Figure 10. Average input current is 14,096 A at input voltage of 75 V, resulting in input power of 1057 W. Output power is 995 W, which yields converter efficiency of 94,6 %. Detailed simulation schematic is placed in Appendix A.

Alternatively, IGBT IKW75N65ES5 can be used. It features saturation voltage of 1,42 V at collector current of 75 A. However, SPICE model in a suitable file format is not available, hence no simulation can be carried out. Another option is to use STGB15H60DF from STM. SPICE model of this IGBT is available, but there have been convergence errors during simulation.
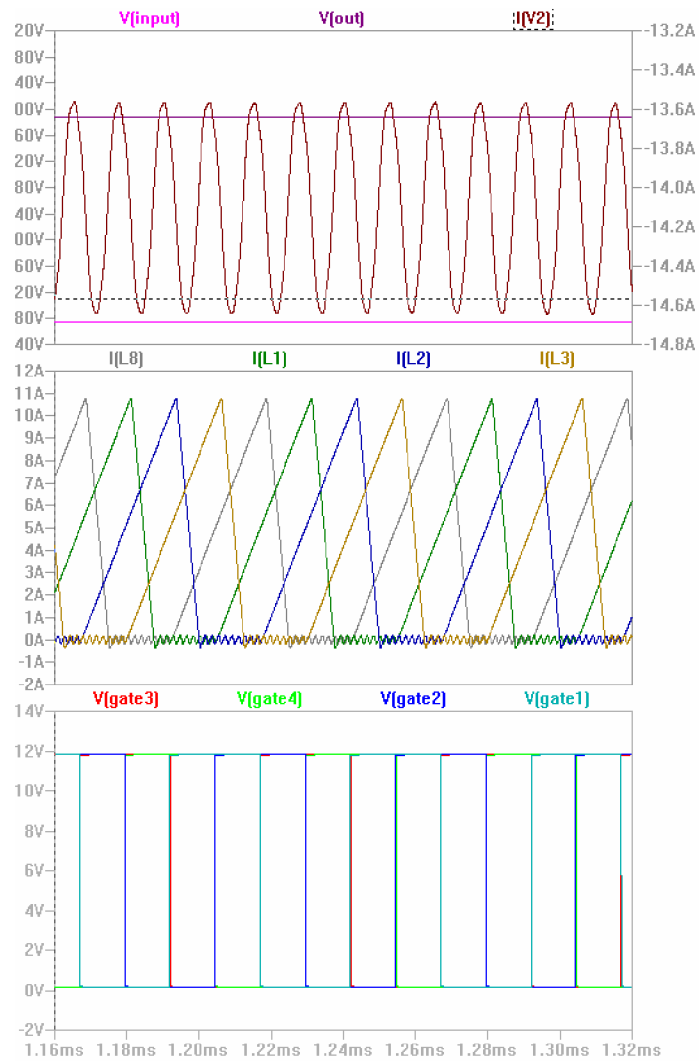
Figure 10: Waveforms of simulated boost converter circuit

Possible way to reduce switching losses is to utilize some of many soft-switching boost topologies. For instance, these have been presented in literature[7][8].
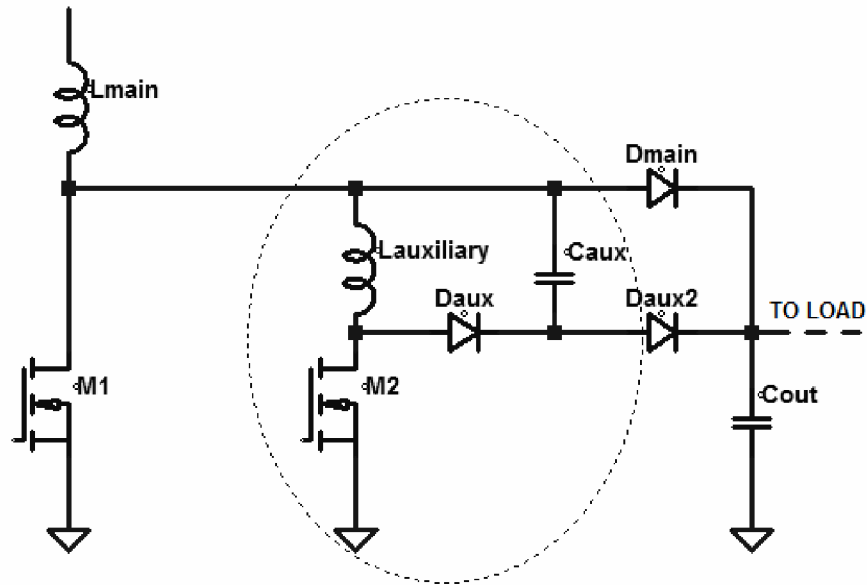
Figure 11: Boost converter with auxiliary active turn-off snubber

The circuit shown in Figure 11 was presented in 2002 in [12] . It reduces turn-on and turn-off stresses in Continuous conduction mode (and to a less extent in Discontinuous conduction mode). During the off-time of the main switch M_1, auxiliary switch M_2 is turned-on by a short gate pulse and auxiliary inductor is being charged by current, which is the sum of main inductor current and reverse recovery charge of boost diode D_{main}. Then, M_2 is turned-off and magnetic field of auxiliary inductor begins to collapse - diode D_{aux} is now forward-biased and capacitor C_{aux} is charging to a negative voltage, which equals - in the ideal case - the output voltage. After this time interval the main switch is turned-on, while the auxiliary capacitor is still being charged. Then, M_1 turns-off and current starts flowing to the negatively charged capacitor C_{aux} and through diode D_{aux2} to the load. Thus, voltage on the main switch is rising very slowly at this moment. This in turn reduces turn-off losses significantly.
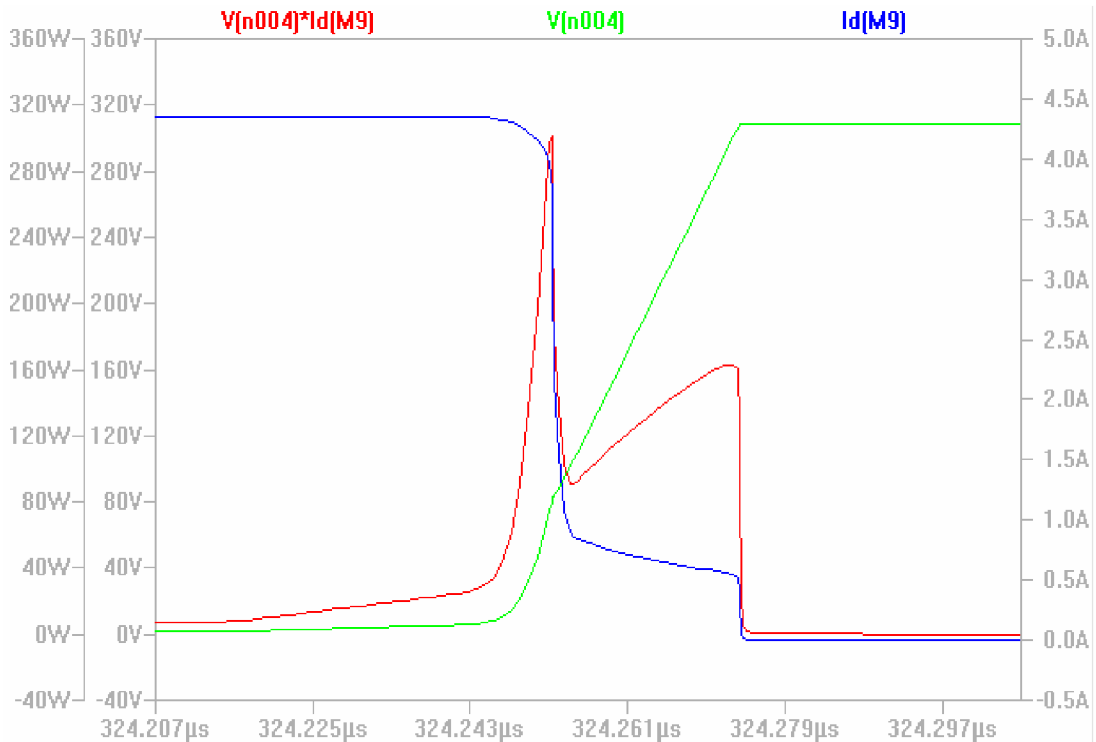
Figure 12: Turn-off waveforms at the switching node (circuit shown in Figure 11). Green color - voltage, blue - current and red is the resulting power loss

From the Figure 12, one observation can be made. Current through the switch is flowing, while the switch (in other words, drain-source voltage of the used MOSFETs) voltage is rising almost linearly - at this moment the output capacitance of the MOSFETs is charging to the output voltage. Thus, this power loss cannot be avoided - or more precisely said, can be only decreased by utilizing switching devices with lower output capacitance, e.g. utilize the aforementioned IGBTs instead of parallel connected MOSFETs. SPA11N60C3 has typical output capacitance of 390 pF, which yields total output capacitance of 6,24 nF when 16 devices are connected in parallel. For example, IKW75N65ES5 has output capacitance of 130 pF, resulting in total capacitance of 520 pF (one IGBT in each phase).

The circuit shown in Figure 11 has been simulated with the following component values: $L_{AUXILIARY}$ = 22 µH, C_{AUX} = 1 nF, and the diodes MUR460. Auxiliary transistor is triggered by a 5 µs long gate pulse. Output voltage is 395 V, average input current 13,91 A at input voltage of 75 V. Thus, total input power is 1043 W and the output power is 1026 W and the resulting efficiency is therefore 98,4 %.

2.2   Push-pull stage design

The design input parameters are exactly the same as in the boost converter section. Main difference between transformer-less boost converter and push-pull converter is that unlike

inductors, no "of-the-shelf" transformers that fit the particular design are usually available. Therefore, a suitable transformer has to be designed. First of all, the proper size of the transformer core has to be determined, based on transferred power, operating frequency, magnetic flux density and so on. Core size can be expressed as area product AP[13]:

$$AP = \left(\frac{P_{OUT}}{0.014 \cdot f \cdot \Delta B}\right)^{\frac{4}{3}} \qquad (19)$$

Where P_{OUT} is the output power [W], ΔB is the flux density swing [T] and f is the operating frequency [Hz]. It is important to note that this is a empirical equation only.

Assuming the output power of 1000 W, flux density swing of 200 mT and operating frequency of 50 kHz, the required AP is:

$$AP = \left(\frac{1000}{0,014 \cdot 100000 \cdot 0,2}\right)^{\frac{4}{3}} = 3,57 cm^4 \qquad (20)$$

For example, the core ETD49 meets this criterion, having AP of 5,76 cm^4. Next step is to determine a suitable core material. One has to be aware of the fact that it can be very difficult and time-consuming to find the best material for this application because of many variables involved. Now, the N87 material is considered.

Once the core material has been found, number of primary turns can be determined. By applying Faraday's law, number of turns can be found based on input voltage, duty cycle, operating frequency and flux density swing:

$$N_P = \left(\frac{V_{IN(MIN)} \cdot D_{MAX}}{\Delta B \cdot f \cdot A_{core(eff)}}\right) = \frac{40 \cdot 0,95}{0,2 \cdot 100000 \cdot 0,00021} = 10,17 \Rightarrow 11\, turns \qquad (21)$$

Where N_P is the number of primary turns, $V_{IN(MIN)}$ [V] is the minimal input voltage, D_{MAX} is the maximal duty cycle [-], f is the operating frequency [Hz], ΔB is the flux density swing [T] and $A_{CORE(EFF)}$ is the effective area of the transformer [m^2].

N87 material has inductance constant A_L of 1680 nH/turn^2. Thus, 11 turns produce primary inductance of 203 µH. The primary-to-secondary turns ratio n can be calculated (while neglecting diode and switch drops):

$$n = \left(\frac{V_{OUT}}{D \cdot V_{IN(MIN)}}\right) = \frac{390}{0,95 \cdot 40} = 9,2 \qquad (22)$$

Where V_{OUT} [V] is the output voltage, D is the duty cycle [-], $V_{IN(MIN)}$ is the minimal input voltage. [V]

Hence, the required number of secondary turns is 11 turns times 9,2, which yields after rounding up 102 turns. The circuit has been simulated just like the boost converter in the previous example. Simulation schematic diagram is shown in Figure 13.
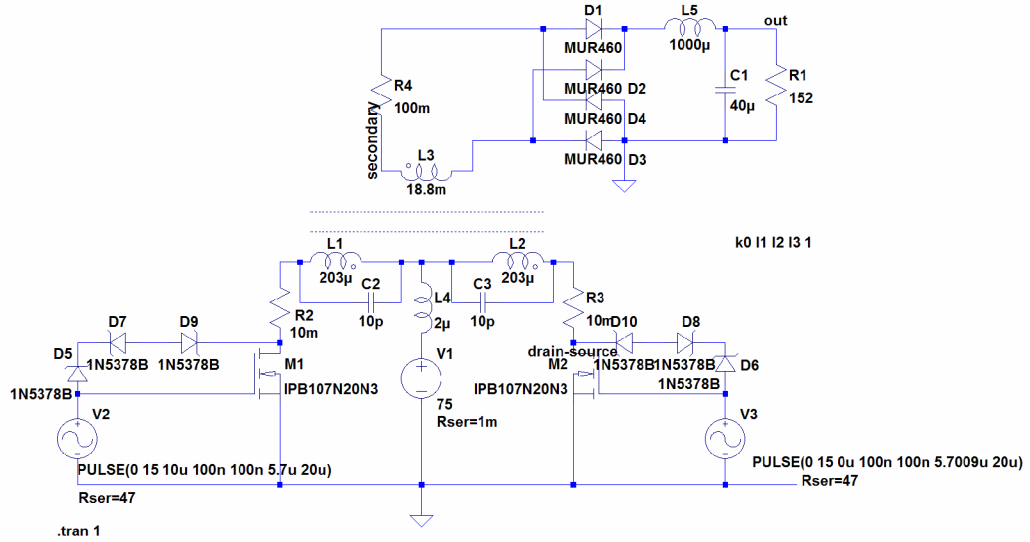
Figure 13: Push-pull converter simulation schematic diagram

A 10 mΩ, 250 V MOSFETs IPB107N20N3 are employed as switches. Their drain-source voltage at turn-off is clamped at 200 V + $V_{GS(TH)}$ by clamping circuits consisting of Zeners D_5, D_7, D_9 and D_{10}, D_8, D_6, respectively. Resistors R_2 and R_3 represent DC-losses of the transformer primary winding, inductance L_4 represents leakage inductance of the transformer (1 % of magnetizing inductance of 203 µH), capacitors C_2 and C_3 are transformer inter-winding capacitances and resistor R_4 is parasitic resistance of transformer secondary winding. Resulting waveforms are shown in Figure 14. It can be clearly seen that there is severe ringing caused probably by reactive circuit components. For this reason, boost stage will be used for the final realization.
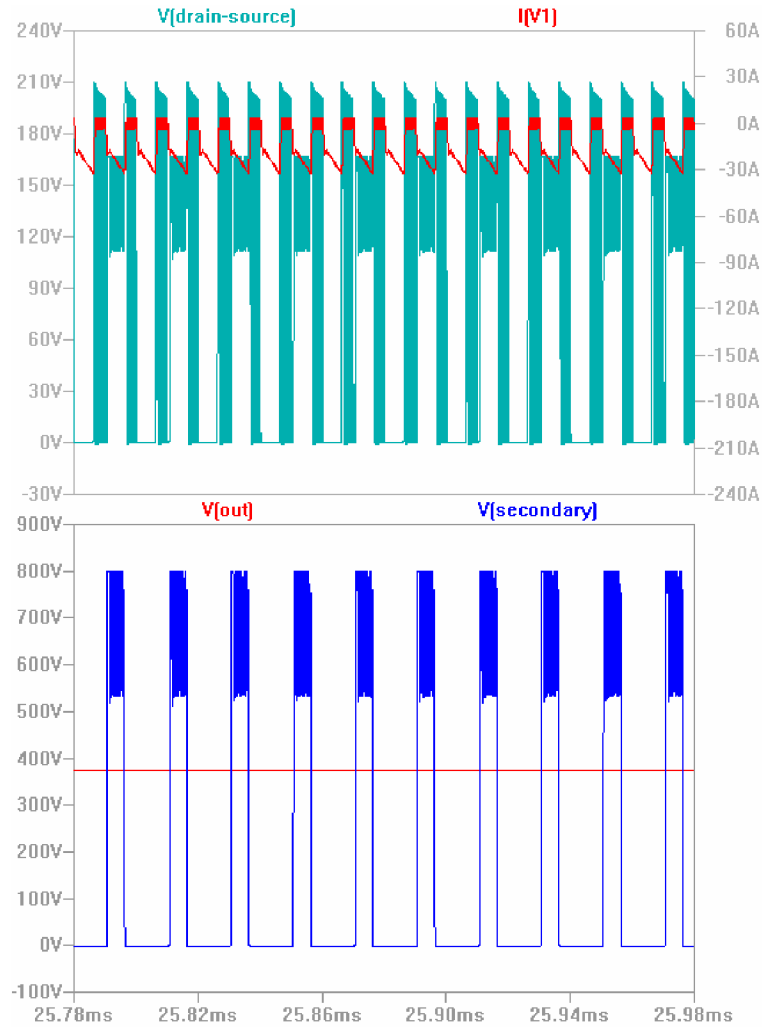
Figure 14: Push-pull converter waveforms

One conclusion can be drawn from the above simulations - boost converter has performed better in terms of efficiency and voltage stresses of rectifier diodes have been smaller than in push-pull converter. Voltage imposed on MOSFETs and rectifier diodes and wasted power have decreased after the leakage inductance was made smaller. The simulated circuit has average input current of 14,866 A at input voltage of 75 V, that is input power of 1114 W. Output voltage is 375 V at output current of 2,47 A, which means output power of 926 W. This yields efficiency of 83 %.

2.3   DC-AC stage

A full-bridge output stage has been designed to be utilized as DC-AC inverter stage. Eight switching transistors are switched by a PWM signal. The PWM signal is produced by comparing sine wave signal to a reference saw-tooth signal. For the purpose of simulations, two MOSFETs SPA11N60C3 have been chosen for each converter leg. The switching

frequency has been chosen to be 10 kHz. A 4-th order LC filter consisting of two 4,7 mH inductors and 20 μF capacitors filters the square-wave output voltage of the switching stage.
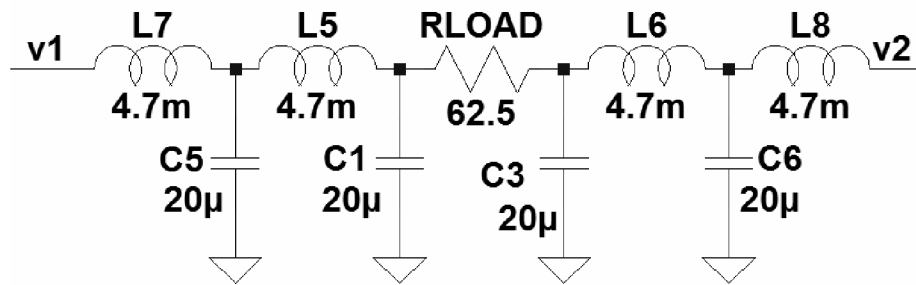
Figure 15: Output filter schematic diagram

Gates of high-side MOSFETs (which are not ground-referenced) are driven by a transformer. When the high-side MOSFET is in the On-state, the driver circuit is supplying a 500 kHz, 50 % duty cycle signal to the transformer primary winding. A Graetz bridge rectifier is connected to the transformer secondary winding to rectify this signal. After the primary driver circuit has been turned-off, the gate capacitance is discharging through a small-signal PNP transistor. This gate drive technique offers, in contrary to a simple capacitor-coupled transformer gate drive, a very wide duty cycle range[14]. The gate drive circuit is shown in Figure 16.
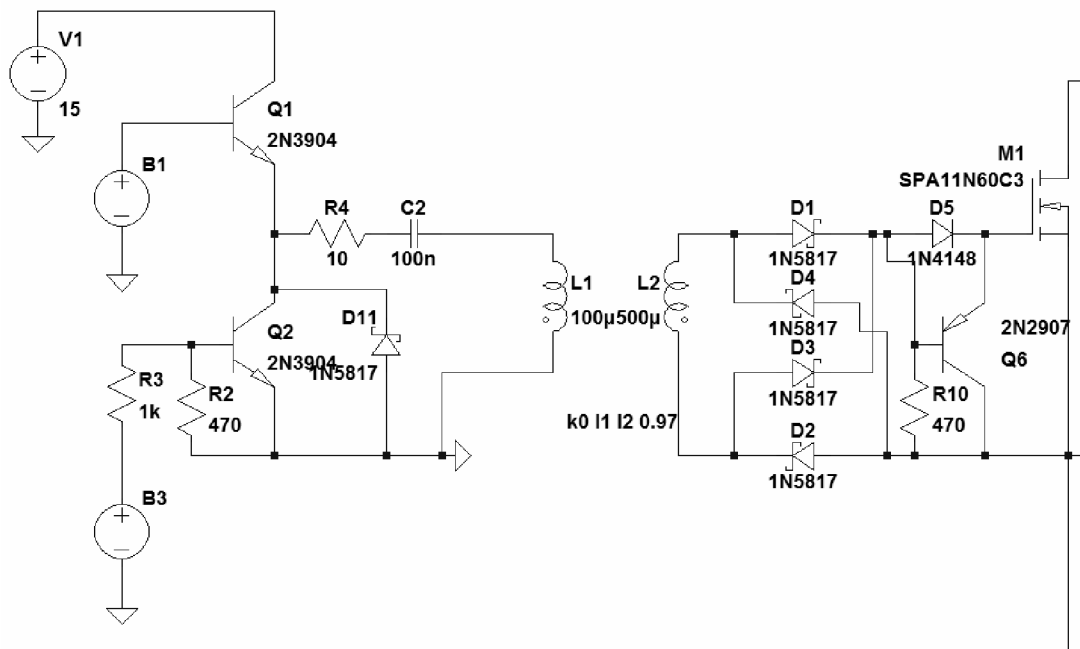
Figure 16: High-side MOSFET gate drive circuit

The complete schematic diagram of the simulated DC-AC stage is placed in the Appendix A. The output load is simulated by a 62,5 Ω resistor as shown in Figure 15. The simulation yields total harmonic distortion of the output signal of approximately 1,6 %. The FFT of the output voltage is shown in Figure 17.
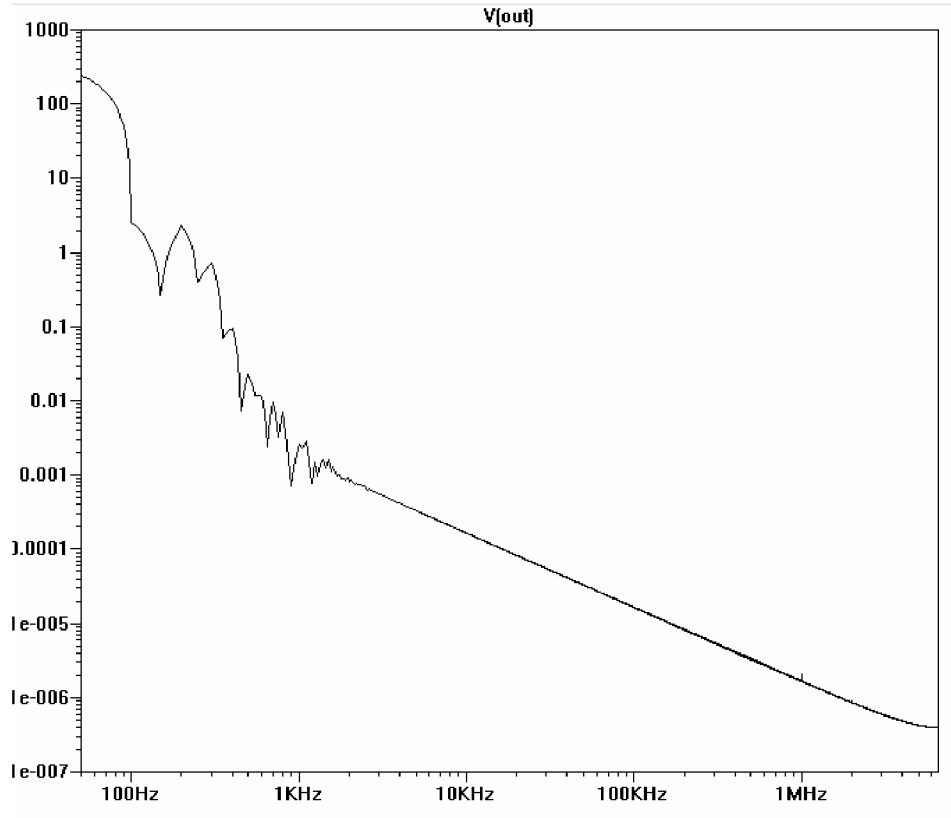
Figure 17: FFT of the output voltage. 1st harmonic has RMS value of 214V, 2nd and 3rd harmonics have both RMS value of approximately 2,5V

Knowing two most dominant higher-order harmonics, the THD can be calculated as[15]:

$$THD = \frac{\sqrt{V_2^2 + V_3^2}}{V_1} = \frac{\sqrt{2,5^2 + 2,5^2}}{214} = 1,6\ \% \tag{23}$$

Where V_1, V_2, V_3 are RMS-values of the respective harmonics [V].

In Figure 18 gate drive signals are displayed. The quickly changing signals are the high-side drive signals - this waveform is caused by loading the Graetz bridge rectifier output by gate discharging resistors.

Another possible option is to use integrated power module, or IPM for short as the full-bridge driver. For example, circuit STGIPL14K60 from ST Microelectronics offers six integrated IGBT transistors along with analog signal conditioning circuits. Thus, possible

time consuming experiments with gate-drive transformer are avoided. This will be discussed later.
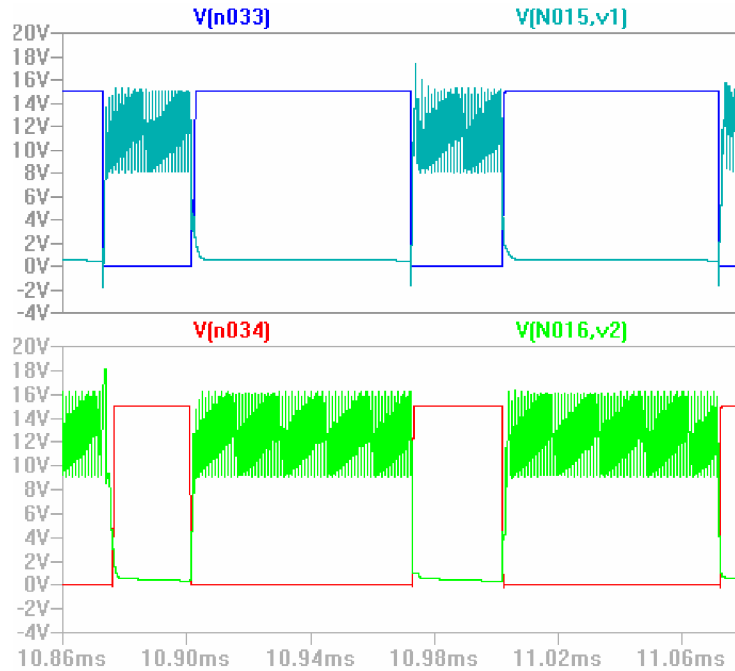
Figure 18: Gate drive signals. Pulsed signals are high-side drive signals

The DC-AC stage outputs 217 V_{RMS} into 62,5 Ω load at input voltage of 400 V_{DC}, which means output power of 736 W. Input power calculated by LTspice IV simulator is 754 W. That is efficiency of 97,6 %. Output power lower than expected is caused by switching and conduction losses and low duty cycle. Increasing maximal duty cycle too much to a higher value is not a good choice, because problems during turning-on and turning-off of the high-side MOSFETs will likely occur (due to limited speed of driver circuit). Therefore, the input voltage of the DC-AC stage needs to be increased. Increasing to 410 V_{DC} and increasing maximal duty cycle to 97 % results into RMS output voltage of 242 V_{RMS}. This gives output power of 952 W, input power is 988 W and resulting efficiency is 96,3 %.

3 Practical implementation

For the purpose of prototyping and debugging, physical design has been implemented on three separate boards - one board for FPGA and sensing circuits, one for one phase of interleaved boost stage and one for full-bridge stage. Firstly, boost board will be described in detail. Then, the FPGA board will be described as the last one, since the requirements on control and sensing circuit are dictated solely by problems arising in these two aforementioned stages.

Some of schematic diagrams are placed in this chapter, board schematics as well as bill of material are placed in appendices for the sake of better readability. All components used for the practical implementation were bought at company Farnell element14.

3.1 Boost board design

The boost board has been designed with the following parameters:

- output power of 250 W + margin[3]
- input voltage < 90 V
- output voltage of 390 V_{DC}
- soft-start circuit to avoid large inrush current
- simple over-current and over-voltage protection

Soft-start circuit has been implemented by means of thermistor-diode string connected from the input to the output. This circuit ensures that the current through boost inductor never increases too rapidly, which would lead inductor into saturation. Additionally, a circuit which prevents boost stage from starting when the output is shorted has been added. This circuit is formed by a PNP transistor, 15 V zener diode and a high voltage PN diode. When the output is lower then input voltage minus zener voltage and base-emitter junction of the PNP transistor becomes forward biased, the transistor is switched-on and a fault signal appears in the collector. The circuit is shown in Figure 19.

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[3] Assuming losses in the last (full-bridge) stage
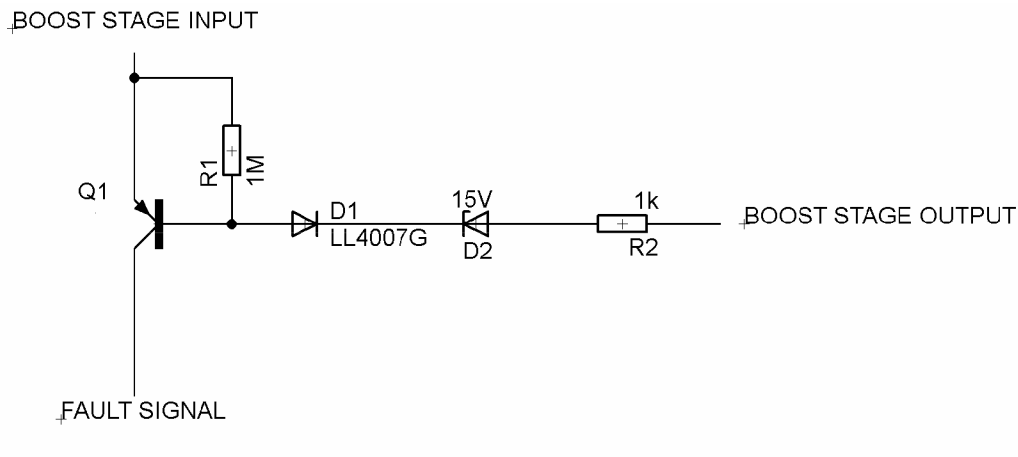
Figure 19: Basic overload protection circuit

Inductor selection was done in Section 2.1. Inductor PCV-2-224-08L was chosen. On the other hand, transistor selection has been iterated. The solution using parallel connected MOSFETs has been abandoned due to:

- High input and output capacitances,

- multiple gate drivers are required,

- layout is harder to optimize in terms of EMI

Instead, single IGBT IKP10N60T from Infineon has been chosen. It features collector-to-emitter breakdown voltage of 600 V at collector current of 18 A. IGBT driver TC1411 from Microchip was selected as the gate driver. Approximate value of switching and conduction losses at maximal output power of the boost stage can be calculated from values given in the device's datasheet. As stated earlier, the peak collector current can be calculated as twice the value of average input current. To simplify calculations, average input current is assumed to be 6 A, which would give input power of 264 W (250 W output power + 14 W loss). Switching energy at turning-off 12 A of collector current is 0,45 mJ. Thus, switching power can be calculated by multiplying switching energy and switching frequency.

$$P_{SW} = E_{SW} \cdot f_{SW} = 4,5 \cdot 10^{-4} \cdot 20000 = 9\ W \tag{24}$$

Where P_{SW} is switching power [W], E_{SW} switching energy [J] and f_{SW} switching frequency [Hz].

Conduction loss can be calculated by assuming saturation voltage of 1,8 V at 12 A of DC collector current. Conduction loss in IGBTs is generally more difficult to calculate than in MOSFETs, since the collector-to-emitter saturation voltage drop is non-linear function of collector current. [16] However, to obtain some reasonable value and to enable proper cooling design, RMS current and saturation voltage can be multiplied to obtain the power loss due to

conduction. RMS current has been calculated by numerical integration in LTspice IV simulator.

$$P_{LOSS} = U_{CE(SAT)} \cdot I_{RMS} = 1,8 \cdot 6,9 = 12,4 \, W \qquad (25)$$

Where P_{LOSS} is the switching loss [P], $U_{CE(SAT)}$ is the collector-to-emitter saturation voltage [V] and I_{RMS} is the collector current RMS value [A].

This accounts to total power loss of 21,4 W in switching transistor. The temperature of IGBT chip must be kept lower than 175 °C. Assuming maximal ambient temperature of 40 °C, there is 135 °C temperature margin. The heatsink can be designed using the following equivalent schematic of the thermal circuit in Figure 20:
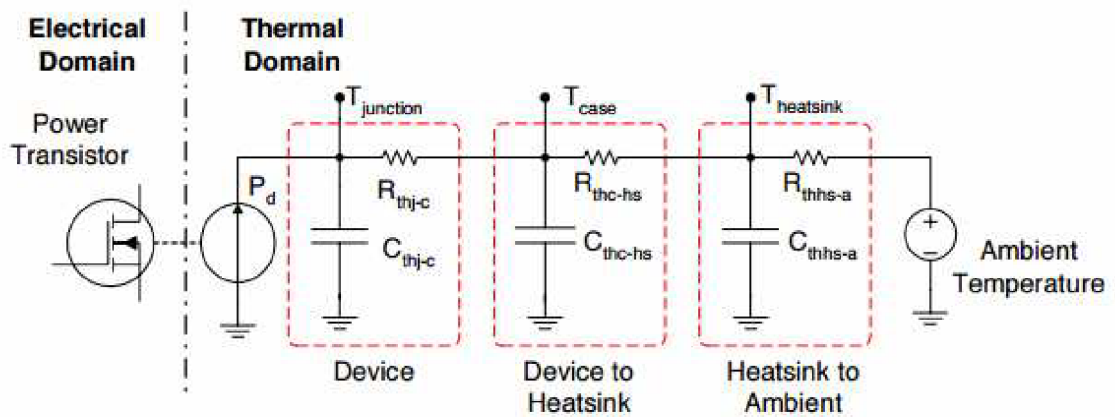
Figure 20: Equivalent thermal circuit [17]

The Pd source sources 21,4 W of power into load consisting of three resistors - junction-to-case, case-to-heatsink and heatsink-to-ambient. Junction-to-case resistance of TO-220 package is 0,9 °C/W. Thus, thermal flow of 21,4 W causes 19,3 °C temperature drop across this resistance. Hence, the thermal resistance of heatsink must be smaller than:

$$R_{HEATSINK} < \frac{175 - 40 - 19,3}{P_d} = \frac{115,7}{21,4} = 5,4°C/W \qquad (26)$$

Where $R_{HEATSINK}$ is the thermal resistance of the heatsink [°C/W] and P_d [W] is the dissipated power.

Having thermal resistance of 5,2 °C/W, heatsink SK129 from Fischer Elektronik has been selected. Next step is to determine input and output capacitor value and current ratings as well as suitable boost diode. Boost diode can be selected based on two requirements. First, it has to block voltage of at least 390 V_{DC} + safety margin. Second, it has to have reverse recovery time as short as possible. Silicon-carbid diode STPSC10H065G has been selected for this purpose.

Input capacitor RMS current rating can be calculated by subtracting maximal RMS inductor current and maximal input average current (non-corellated):

$$I_{CIN} = \sqrt{I_{LRMS}{}^2 - I_{LN}{}^2} = \sqrt{6,9^2 - 6^2} = 3,4 \; A \tag{27}$$

Where I_{CIN} is the input capacitor RMS current [A], I_{LRMS} is the RMS current of the boost inductor [A] and I_{IN} is the input average current [A].

This result has been confirmed by simulation. The value of the input capacitors can be estimated by using the equivalent schematic of a real capacitor as shown in Figure 21
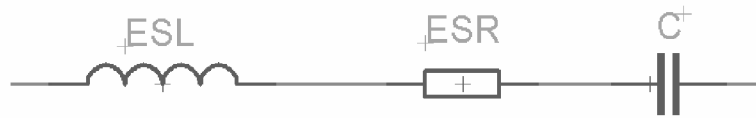
Figure 21: Physical capacitor equivalent schematic

The equivalent series inductance (ESL) is usually in the range of nanohenries and could be neglected for the purpose of these calculations, as the switching frequency is relatively low. However, the ripple current - the inductor current - creates voltage drop across equivalent series resistance as well as capacitive ripple when charging capacitance C. Thus, the AC voltage across capacitor can be expressed by following formula:

$$u_C = ESR \cdot i_C(t) + \frac{1}{C} \int i_C(t) dt \tag{28}$$

Where u_C is the ripple voltage across the capacitor [V], ESR is the equivalent series resistance [Ω] and C is the capacitance [F] and i_C is the current flowing into the capacitor [A].

Next task is to determine, how exactly the ripple voltage depends on time and inductor current. As can be seen in Figure 22, the current is flowing out of the capacitor when the inductor current is greater than input current (assuming input current source). Hence, the voltage ripple is dependent upon half of the inductor ripple current, or $\Delta I_L/2$. Further can be seen that the whole switching period can be divided into two parts - current is flowing out of the capacitor and into the capacitor. The capacitor charge must remain the same at the end of each cycle. Thus, seeing that the part of the period when the charge is positive or negative can be further divided into two sections - in the first section current is increasing and in the second the current is decreasing, the capacitive ripple voltage can be expressed as:

$$u_C = \frac{\Delta I_L}{C \cdot 8 \cdot f} \tag{29}$$

Where u_C is the ripple voltage across the capacitor [V], $\Delta I_L/2$ is the inductor ripple current [A], C is capacitance of the capacitor [F] and f is frequency [Hz].
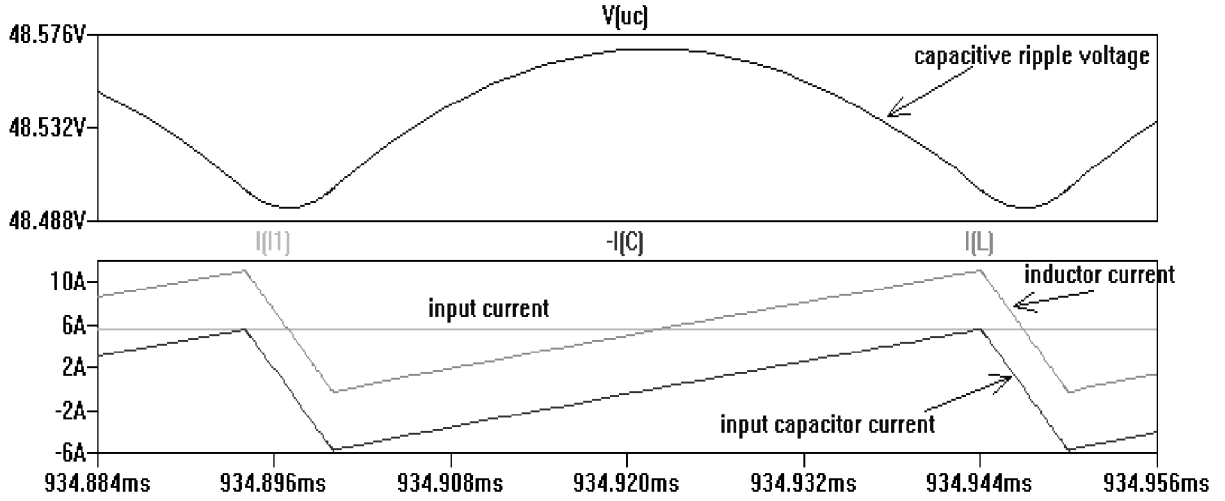
Figure 22: Waveforms of input capacitor and inductor currents and capacitor voltage ripple, capacitor ESR = 75 nΩ (capacitor with negligible ESR)

Hence, it can be clearly seen that two ripple components exist - the higher the capacitance, the smaller the capacitive ripple component is. For very high capacitance values, the ripple is created virtually only by equivalent series resistance. Paralleling two capacitors ELG477M200AR2AA gives 940 µF capacitance and 75 mΩ equivalent series resistance. This in turn yields capacitive ripple voltage of

$$u_{C(CAP)} = \frac{\Delta I_L}{C \cdot 8 \cdot f} = \frac{12}{940 \cdot 10^{-6} \cdot 8 \cdot 20000} = 79\,mV \tag{30}$$

Where I_L is the inductor ripple current [A], C is the capacitance of the capacitor [F] and f is the switching frequency [Hz].

This calculation result corresponds very well to the result of simulation shown in Figure 22. Resistive drop due to ESR can be achieved by multiplying ESR and inductor current, which yields 0,9 V.

Output capacitor is loaded by two currents - charged by triangular inductor current and discharged by sine-shaped current at twice the output AC voltage frequency. Thus, there is a ripple component caused by ESR of the capacitor and capacitive ripple, caused by reactive component of capacitor impedance. Absolute value of this reactive component can be calculated:

$$\left| X_C \right| = \frac{1}{2\pi \cdot f \cdot C} \tag{31}$$

Where X_C is reactive component of capacitor impedance[Ω], f is frequency [Hz] and C is capacitance [F].

To clarify this, a simulation has been done. Boost stage is supplied by current source, which sources current of 6,15 A. Output capacitor has been selected PEH532YBF3220M2 from KEMET, having capacitance of 220 µF and ESR of 0,43 Ω (capacitor C1 in Figure 23). Output is loaded by full-bridge stage, which delivers power of 250 W.
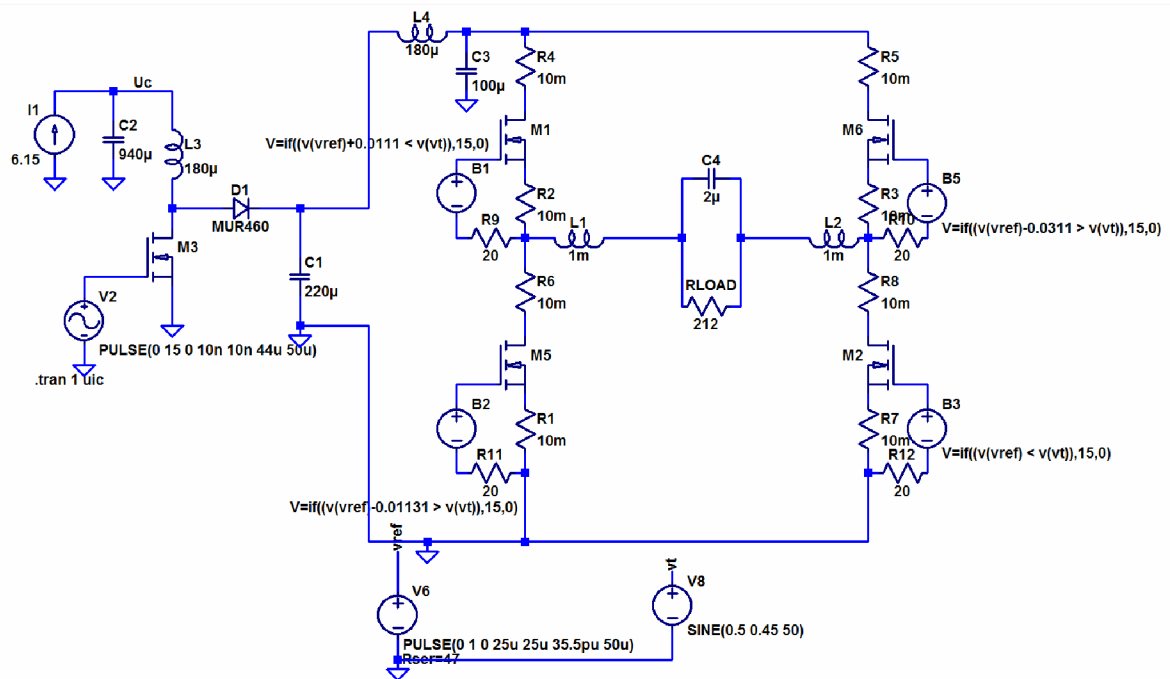
Figure 23: Simulation schematic of boost stage loaded by full-bridge stage for current and voltage calculation

Resulting waveforms of chosen current and voltages are shown in Figure 24.
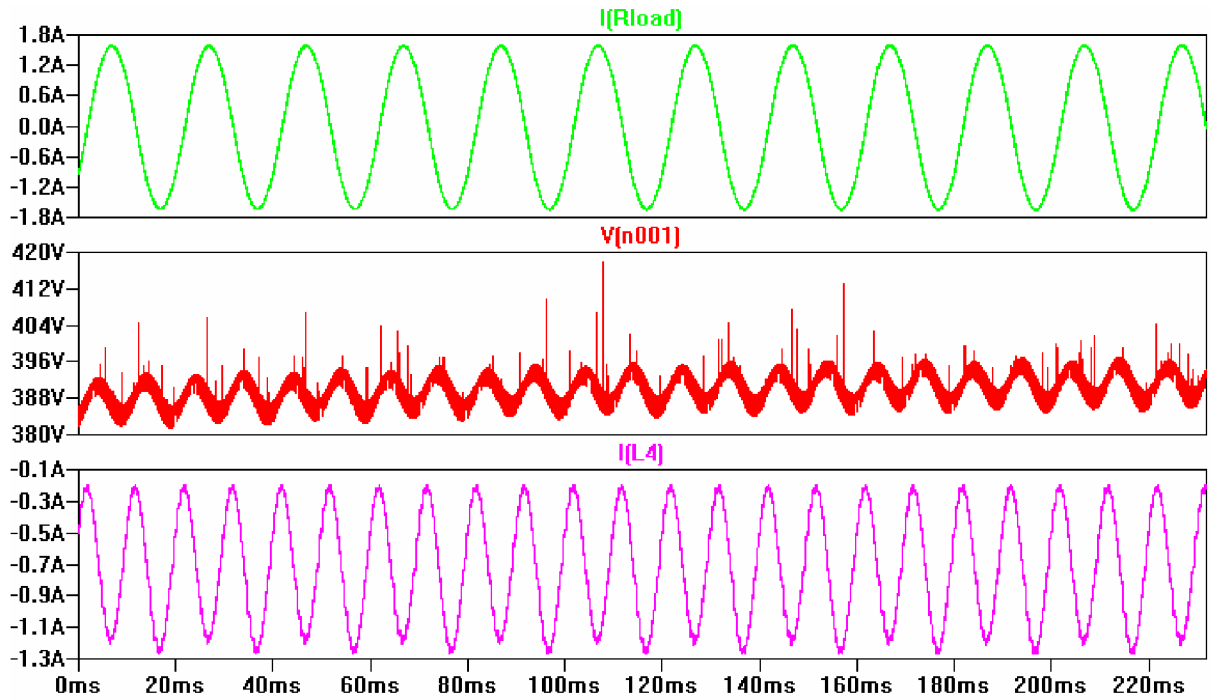
Figure 24: Waveforms of boost and full-bridge stage with boost capacitor 220 µF, full-bridge input current (bottom, pink), boost output voltage (middle, red), AC output current (top, green)

As can be seen in Figure 24, boost stage output voltage has ripple of approximately 6 Vp-p caused by the full-bridge load. This ripple could be reduced by utilizing negative feedback. However, the advantage is that the input source is loaded by constant current.

3.1.1   Boost board layout design

Most of the effort has been spent on identifying and minimizing current loops as these loops create parasitic inductances. There are two high-frequency loops in a typical boost converter. First loop is: input capacitor - inductor - power transistor back to the input capacitor. Second loop is created after the transistor has turned-off: Input capacitor - inductor - boost diode - output capacitor back to the input capacitor. This is visualized in Figure 25.
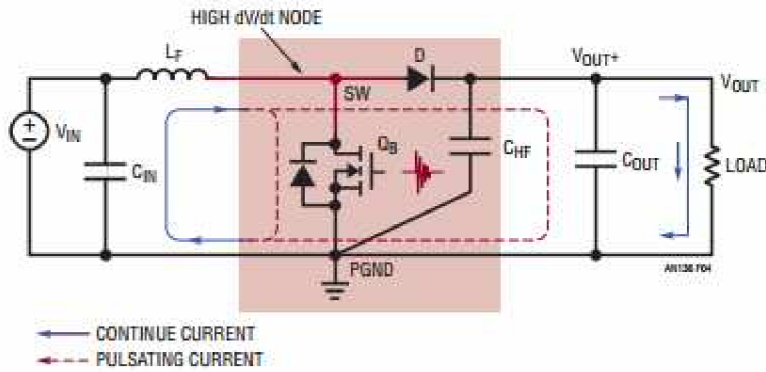
Figure 4. Continuous and Pulsating Current Paths of a Boost Converter

Figure 25: Continuous and pulsating current paths in a boost converter [18]

As shown in Figure 25, the second loop can be minimized by placing high-frequency ceramic capacitor directly to the cathode of boost diode and source/emitter of the power transistor. This is exactly what has been done in this case. High slew rate current as seen during boost diode turn-on is flowing through this high-frequency capacitor, instead of creating voltage drops in parasitic inductances.
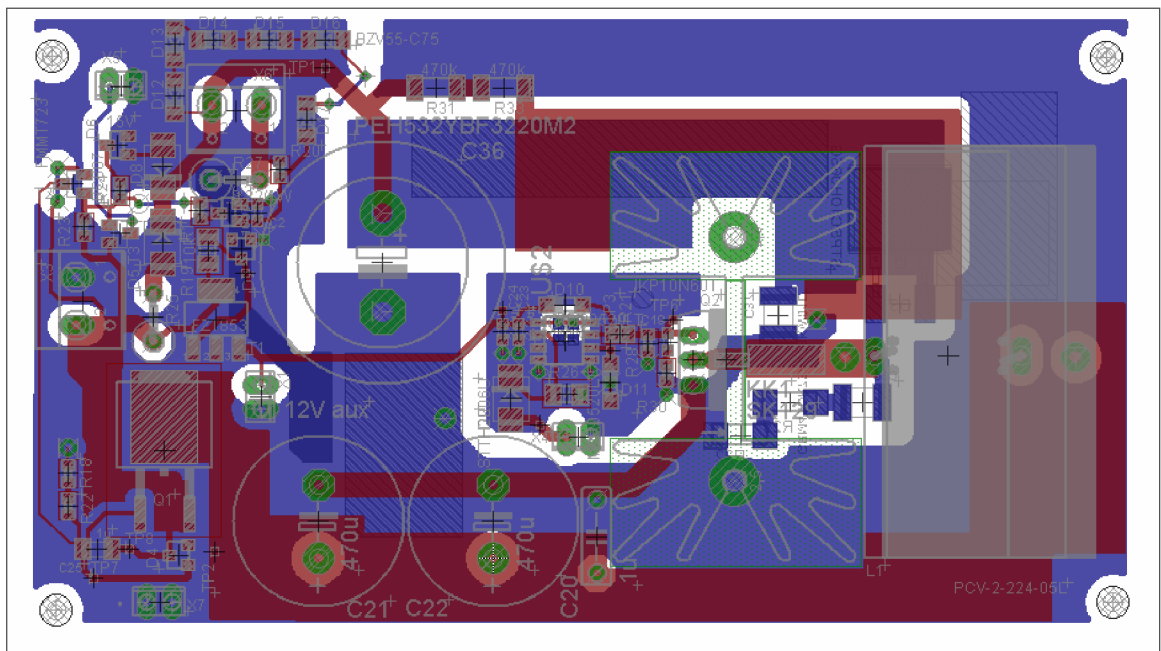
Figure 26: Boost board layout. Bottom layer = blue, top layer = red

Boost board layout is shown in Figure 26. As can be seen, ground plane (blue color) cut-outs (white spaces) were created to isolate high switching currents from the signal current (i.e. IGBT driver ground island connected to the power ground at the emitter of IGBT).

3.1.2   Boost board testing

Boost board was hand soldered and tested by connecting laboratory power supply sourcing voltage of 26,5 V to the input and a resistive load having resistance of 1400 Ω to the output. IGBT driver was driven by signal generator, which was generating 20 kHz, and 3,3 Vp-p square wave signal in order to simulate conditions in the final system. One difficulty with such approach is that extreme care must be taken to avoid accidental removing of the output load as the converter operates in open-loop mode and load disconnecting would cause output capacitor overcharging.

After 10 minutes of operation and 100 W load, heatsink temperature rose to 62 °C. Boost diode heated to 30 °C. Output capacitor did not heat up at all. It is clear that IGBT is the major contributor to power losses in the circuit. IGBT driver supply voltage during the experiment was swept from 10,5 V to 15 V but without any significant effect on losses.

3.2   Full-bridge board design

Options regarding DC-AC stage design from the electrical point of view were discussed in chapter 2.3. To speed up the design process, hybrid power integrated circuit (intelligent power module - IPM) STGIPL14K60 from ST Microelectronics has been chosen. Not only does this circuit integrate six power IGBT transistors, but it also integrates six op-amps (three comparators and three op-amps with designer-configurable feedback) for voltage and current sensing purpose.

The circuit has been originally intended for use in AC motor drives (frequency converters), thus the recommended application schematic provided by the manufacturer in the datasheet has been modified significantly. Out of three phases available, only two are actually used. One op-amp is used as voltage feedback amplifier, it senses the DC-AC stage input voltage and its output is connected to the ADC input on the FPGA board. Second op amp is used to sense the DC-AC stage output voltage and the third one is used for AC-line voltage sensing.

Comparators are used for simple over-current, over-voltage and temperature protection (connected with internal NTC thermistor). Because of complexity of the complete board

schematic, it is placed in appendix. Output filter has been optimized both in terms of performance and cost by using two 1 mH inductors in series for each full-bridge leg output and two 1 μF capacitors in parallel.
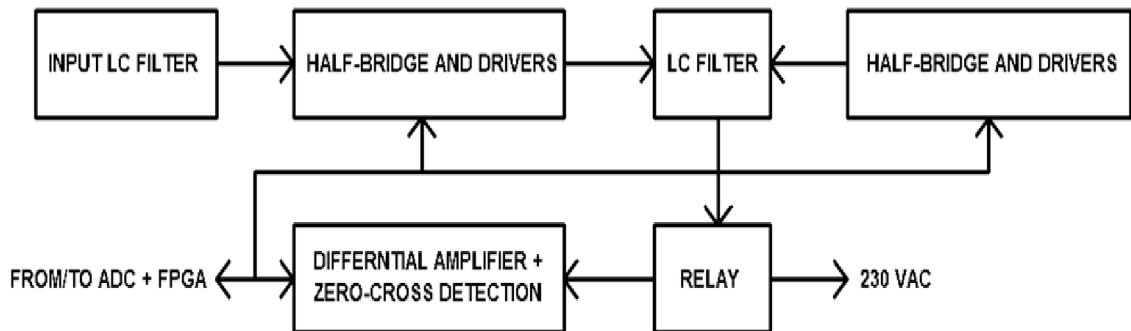
Figure 27: Full-bridge board block diagram

3.2.1 Full-bridge layout

This part of the design was the most complex and time consuming. Even though the design was slightly simplified by using integrated power module, critical aspects still exist. To minimize parasitic inductances of PCB traces, high frequency current tracks have been routed on opposite layers in opposite directions (which means that magnetic fields cancel each other out). The same applies as in the previous case. Board layout as well as board schematic are placed in appendix.

3.3 Full-bridge board testing

The full-bridge board was tested in a situation similar to the final application - by connecting the input to the output of the boost board. FPGA board supplied the PWM signal for both the IPM module and the boost transistor. For the purpose of testing, a 90 W soldering iron having resistance of 720 Ω was connected to the full-bridge output.
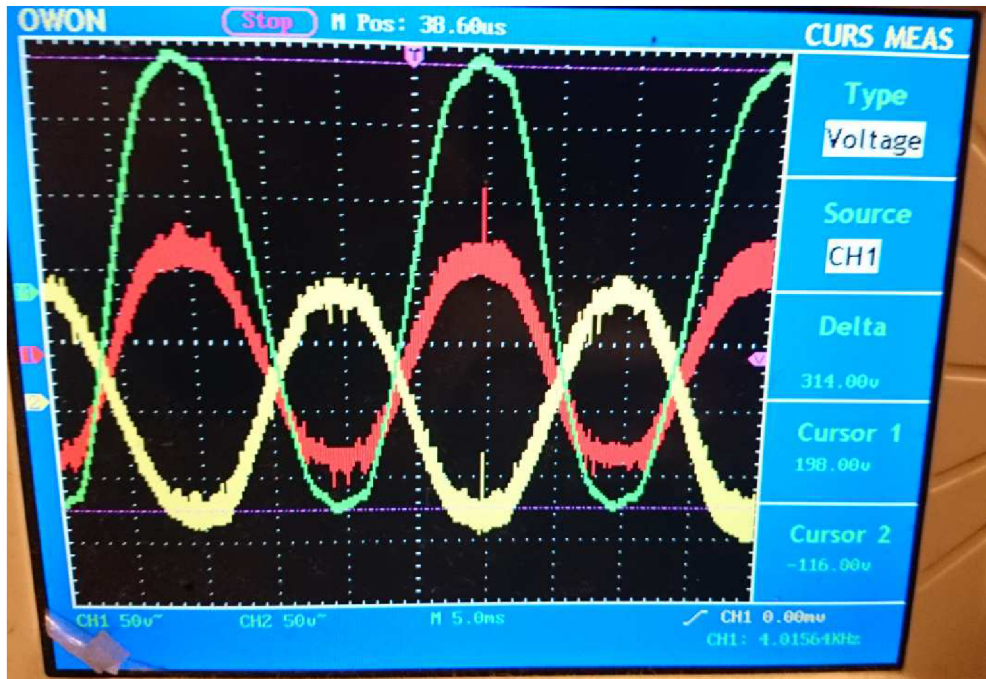
Figure 28: Voltage waveforms on the full-bridge output during initial testing. Generated voltage 112 V_{AC}.

3.4 FPGA board

The FPGA board has been designed based on the following requirements:

- Input voltage up to 90 V

- high conversion efficiency of voltage regulators for powering FPGA

- FPGA programmable via JTAG interface

- optional communication capability with PC via USB

- capability to drive four gate drivers in each phase of boost converter

- capability to drive IPM on full-bridge board

- current and voltage sensing capabilities: input voltage, boost stage output voltage

- output voltage, mains voltage, input current

Based on these requirements, the input voltage is first decreased by zener diode-based linear regulator (zener diode followed by NPN transistor). This stage then feeds DC-DC converters, which are used for powering FPGA and I/O circuits and analog-to-digital converter. FPGA XC3S200A from Xilinx operating at 25 MHz clock has been chosen. Rather low clock frequency of 25 MHz has been chosen in order to decrease dynamic power consumption of the FPGA as well as losses in input linear regulator. FPGA I/O and core voltages are supplied by DC-DC step-down converters based upon TPS62040 chips from

Texas Instruments. These ICs have been chosen because they are endorsed by Xilinx for having optimal start up characteristics (output voltage slope during start up), which are essential for correct start up behavior of FPGA.

Analog-to-digital converter has been chosen MCP3208 from Microchip, which offers 8 multiplexed analog input channels and SPI-based communication interface. This communication interface has been implemented in VHDL language - this will be discussed later.

There has been implemented a USB communication interface as well - by utilizing FT232 UART-to-USB bridge. This can be used for instance for displaying measured values of voltages and currents in a user application on a PC. In order to increase safety in such a situation, the UART interface is isolated from USB interface by optocouplers. Simplified block diagram of FPGA board is shown in Figure 29
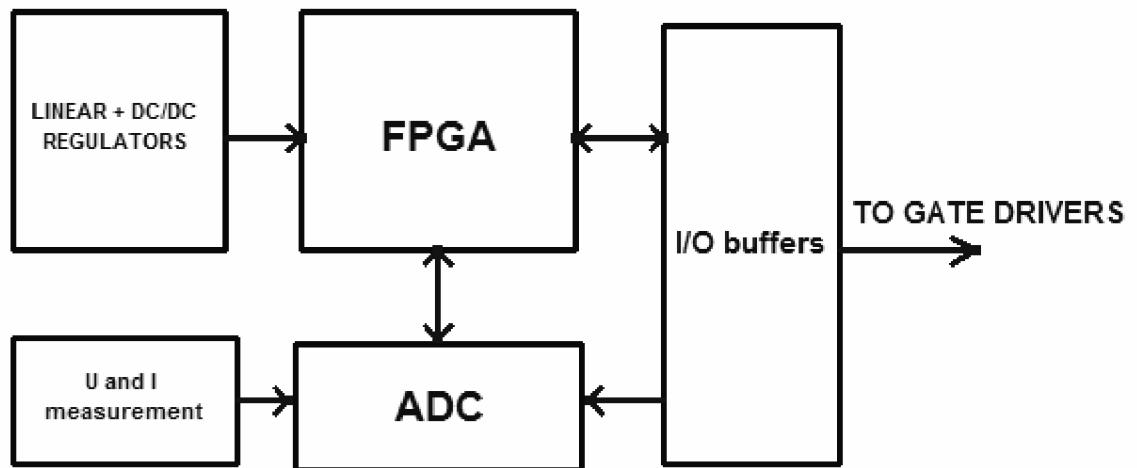
Figure 29: FPGA board block diagram

Finally, photographs of assembled circuit boards are shown in the following three pictures. Only the top side of the FPGA was soldered in IR furnace, the rest of components was soldered manually. Empty pads are intended for optional components which were not assembled.
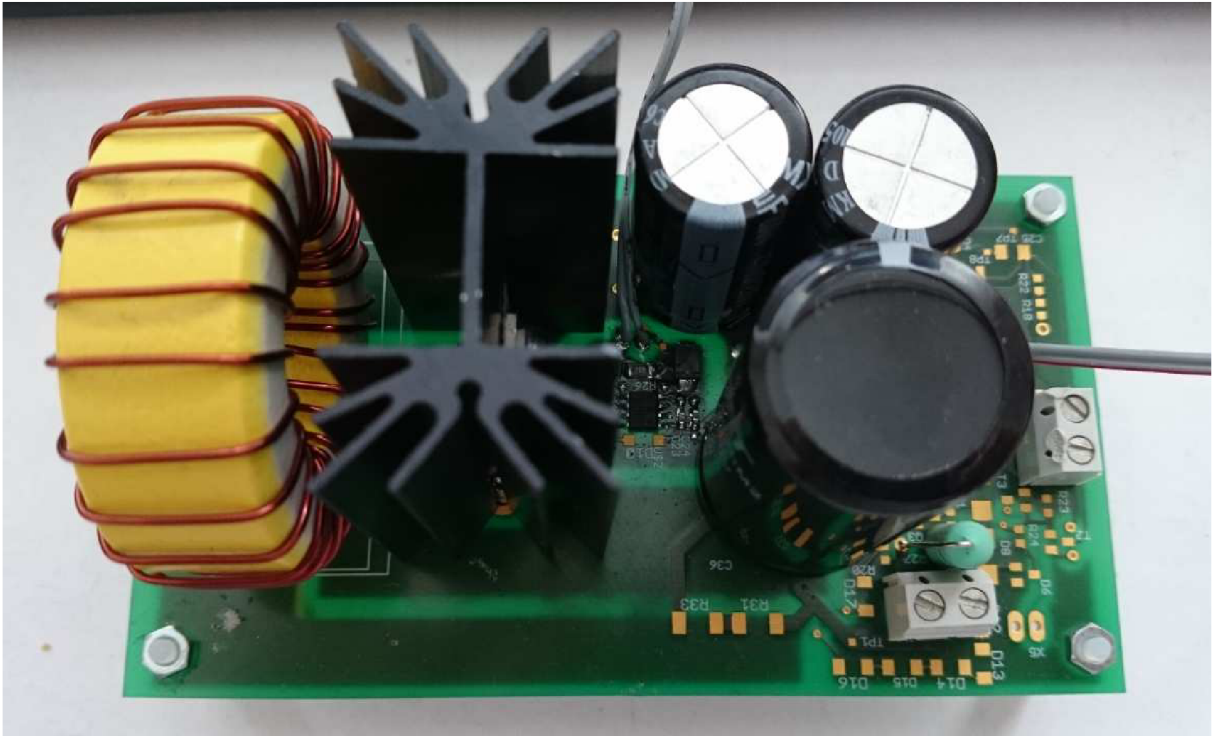
Figure 30: Assembled boost board

Figure 31: Assembled FPGA board
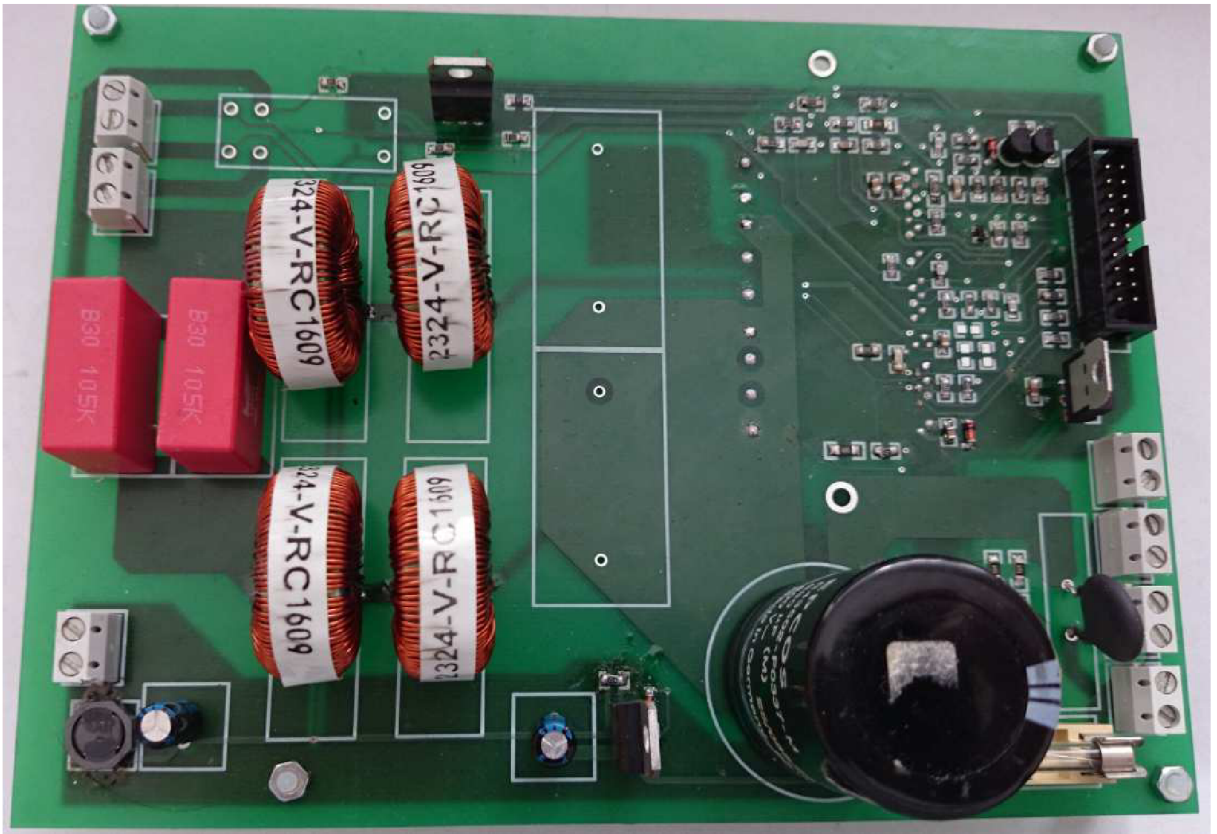
Figure 32: Assembled full-bridge board

4 VHDL description

There are five blocks needed for basic, open-loop operation of the converter. These are:

- Boost converter PWM modulator,

- sine wave PWM modulator for full-bridge stage,

- sine wave ROM, which stores digital sine wave samples,

- soft-start circuits to avoid damage to power components during start-up

- duty cycle limiters.

To maintain good readability of this work, the respective blocks described by VHDL language are described here on a block level only. The VHDL codes are placed in appendix.

4.1   Boost converter PWM modulator

This block has been implemented as a 10-bit counter clocked by 25 MHz system clock

Counter value is then compared with input 10-bit signal. As the IGBT gate drivers have active low inputs, the resulting PWM signal is inverted as well. Furthermore, since there are four in parallel operating boost stages intended, the gate drive signal for three remaining boost stages is delayed by 90 degrees.
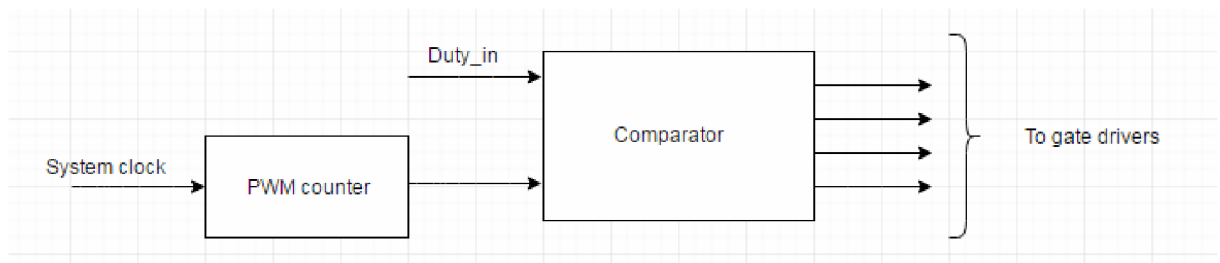
Figure 33: PWM modulator block diagram. Signal Duty_in is 10-bit wide as well as the PWM counter output. OUT = H when PWM counter is greater than Duty_in, else OUT = L
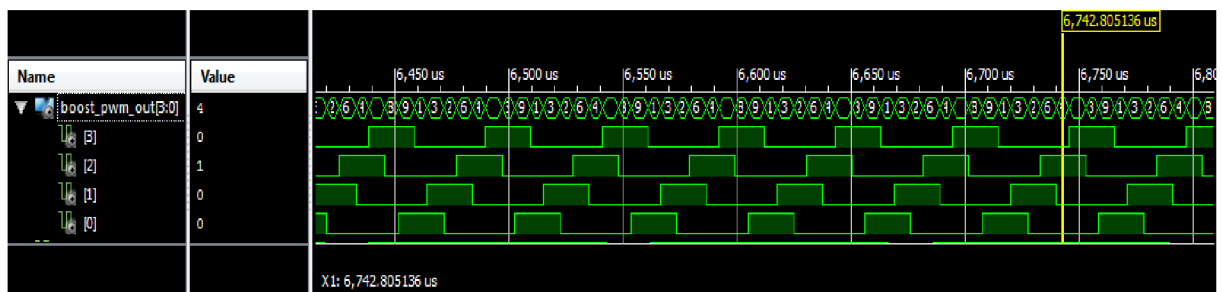
Figure 34: Phase-shifted gate driving signals shown in ISim simulation

4.2　Sine wave PWM modulator

For the purpose of sine wave generation, principle similar to the direct digital synthesis has been adopted. In contrary to the original DDS, sine samples loaded from the memory are not sent to a DAC, but they are used as a reference for a PWM counter. A 32-bit wide phase accumulators have been implemented. First phase accumulator calculates the address, at which the sine sample to be loaded is stored. Second phase accumulator's output serves as a reference signal. More on DDS can be found in [19].

First phase accumulator needs 20 ms to complete one sine-wave period. The second phase accumulator is used to generate the high-frequency PWM carrier signal, it runs thus at 200-times higher frequency, which yields frequency of 10 kHz. Both PWM and sine-wave frequency can be optionally fine-tuned by modifying phase accumulator phase increment values. In [19] it was shown that signal frequency obtainable from the phase accumulator is given by:

$$f_{OUT} = \frac{f_{CLK}}{2^n} FCW \tag{32}$$

Where f_{OUT} is the output signal frequency [Hz], f_{CLK} is the system clock frequency [Hz], n is the bit depth of the phase accumulator [-] and *FCW* (Frequency control word) is the phase increment [-].

By evaluating the previously given equation with FCW = 1, f_{CLK} = 25 MHz and n = 32 bits, elementary frequency step (i.e. the smallest frequency change) is.

$$f_{OUT} = \frac{25 \cdot 10^6}{2^{32}} = 5mHz \tag{33}$$

This tuning capability can be exploited when trying to synchronize the generated AC voltage with mains voltage. However, because of problems during circuit debugging, this option was not implemented.
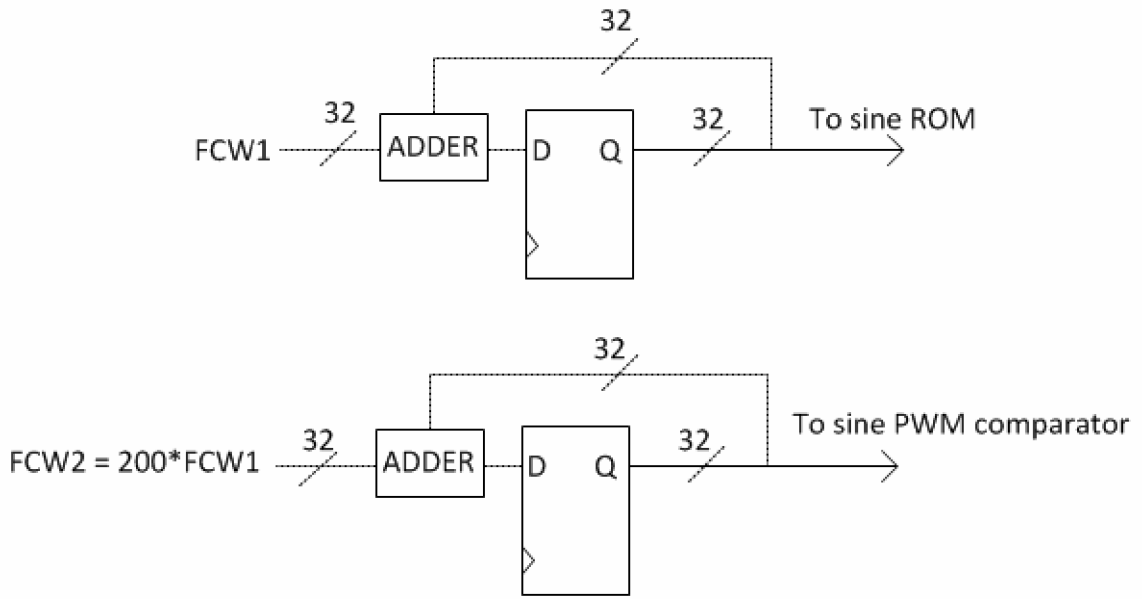
Figure 35: Block diagram of phase accumulators and their inputs and outputs

4.3   Sine-wave ROM memory

This memory has been implemented by utilizing Block RAM available on Xilinx FPGAs. Signal samples are stored in RAM memory cells during configuration of the FPGA at start-up. To save some memory space for possible additional features, only one half-wave is stored in the memory - second half is then calculated based on phase - as a difference between offset value and the corresponding sine-function value. This can be expressed as:

$$y[n] = \frac{FS}{2} - \frac{FS}{2} \cdot \sin\left(2\pi \frac{n}{N}\right) \tag{34}$$

Where *y[n]* is the discrete-time domain sample value[-], *FS* is full-scale value of signal[-], *n* is sample number (discrete time)[-] and *N* total number of samples (discrete period). n < N/2.

Assuming 10-bit resolution, equation 34 gives:

$$y[n] = \frac{1024}{2} - \frac{1024}{2} \cdot \sin\left(2\pi \frac{n}{1024}\right) \tag{35}$$

Where *y[n]* is the discrete-time domain sample value[-] and *n* is the sample number[-].

4.4   Sine-wave sample limiter

To avoid too large or too small duty cycles of the full-bridge stage, sine samples are digitally attenuated in this block. Extreme values of duty cycle might cause higher losses due to limited switching speed of output transistors, since the output PNP transistor of the IGBT may stay in active region of its output characteristics. Samples are multiplied by factor of 0,8, that is, multiplied by factor of 800 and then shifted by 10 bits to the right.

4.5   Soft-start circuit

This circuit is implemented as a 10 bit counter, incremented by 1 every 40 μs. The actual value of the duty cycle is limited by the value of soft-start counter. This circuit has been implemented to hinder excessive rate-of-rise of the inductor current at the start-up. After the start-up is complete (zero value of the counter is reached), counter is blocked. In Figure 36, block schematic diagram of basic open-loop circuit implemented in FPGA is shown.
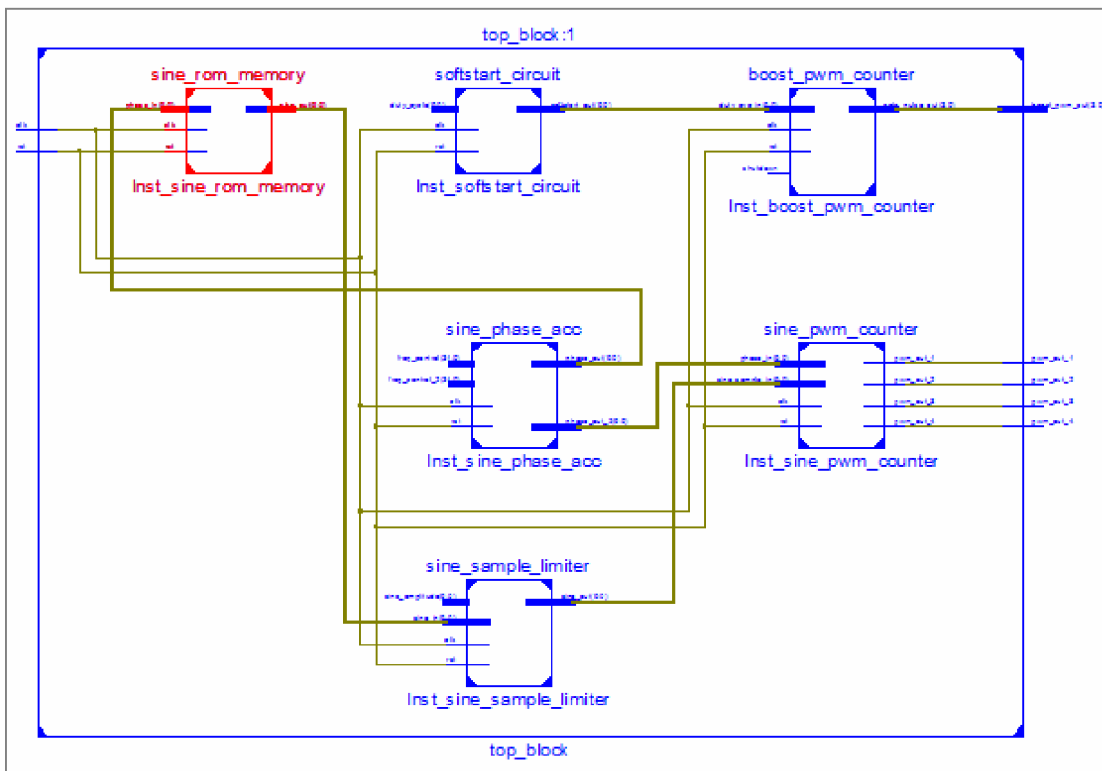
Figure 36: Schematic of top level block generated by Xilinx ISE 14.6 IDE

4.6 Design of the control loop

In order to harvest full power available from the PV panel (array), maximum power point tracking has to be employed. One of the algorithms can be summarized as follows:

- When the input power available is increasing, duty cycle has to be increased,

- when the input power begins to decrease, even though the duty cycle is increasing, duty cycle must change in opposite direction and vice versa.

This is usually called Perturb and Observe algorithm, when referring to MPPT. Another possible solution to the problem can be described as follows:

- Duty cycle is swept from some fixed initial value,

- as soon as the input power ceases to increase, duty cycle increasing is stopped,

- the process is repeated at fixed time intervals.

These algorithms are usually referred to as current sweep algorithms. It has been implemented by a finite state machine, whose state diagram is shown in Figure 37. Process is repeated every ten seconds.
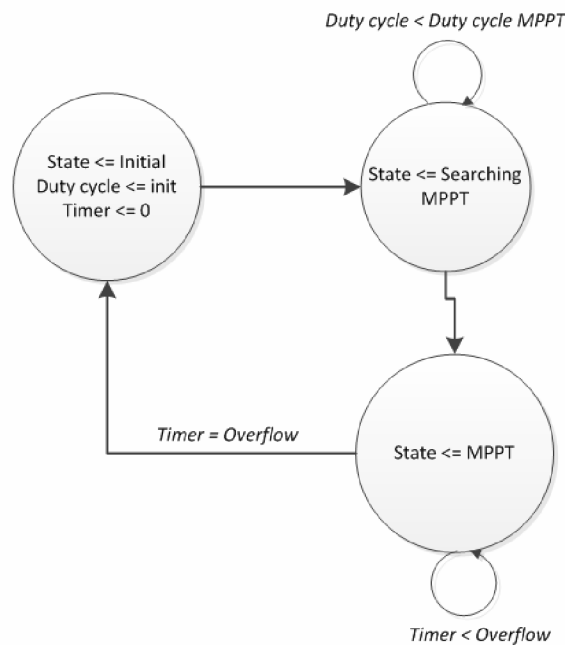
Figure 37: Current sweep method state diagram

4.6.1 MPPT P&O algorithm implemented in hardware

As has been mentioned earlier, the algorithm is based on comparing two consecutive values of input power and adjusting duty cycle to achieve maximal power output from the PV panel. Thus, a discrete-time differentiator has to be employed. A simple differentiator can be built using two D flip-flops. A comparator then compares the two consecutive values of the signal. If the unit delayed value of the input signal is higher than the current value, it means that the input signal has negative slope and vice versa. Then, the duty cycle is incremented or decremented based on difference sign.
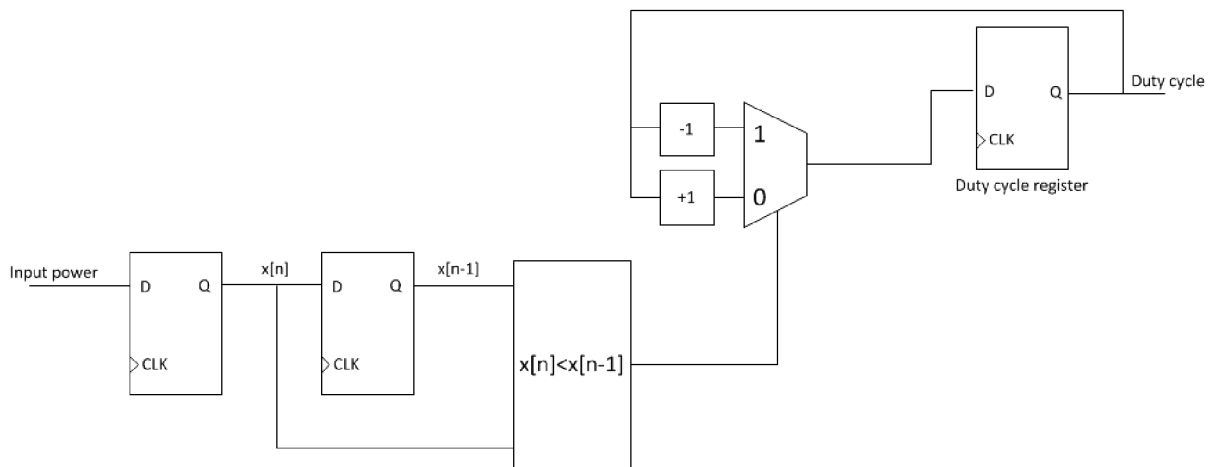
Figure 38: Perturb and observe method simplified block diagram on RTL level

The algorithm is continuously trying to find maximum power point of the PV panel array. After the maximum power point has been found, the difference changes its sign and the process is repeated. That means that the operating point of the PV array oscillates around the maximum power point.

Finally, to protect the entire circuit from overvoltage in case of output load is disconnected, a shutdown function has been implemented. When the boost stage output voltage reaches 410 V, a shutdown circuit is activated.

4.7 Current and voltage measurement

Analog signal conditioning circuit is placed on FPGA board. It consists of MCP3208, a 12-bit serial ADC communicating over SPI interface with FPGA. There are also two current measurement inputs. Two 5 mΩ shunt resistors are used to convert current to voltage. Input voltage is measured by circuit shown in Figure 39
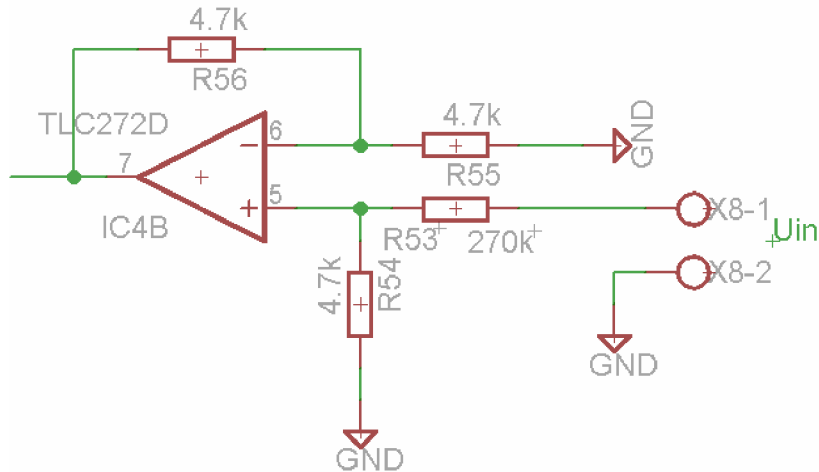
Figure 39: Input voltage measurement circuit

The circuit shown in Figure 39 is designed to produce 3,15 V on its output at full-scale input voltage of 90 V. However, standard 0805 and 0603 resistors having 5 % tolerances have been used. This is because these devices are available in reasonable quantities. The current measurement circuit schematic is placed in Appendix C.

4.7.1 Analog-to-digital converter MCP3208 SPI interface

SPI interface has been implemented in VHDL language based on waveforms provided by device manufacturer. Source code is provided in a separate *.zip file.

4.8   FPGA utilization

HDL synthesis report from Xilinx ISE IDE is given in this subchapter. It shows how many logic resources within FPGA is actually used for the implementation.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	179	704	25%
Number of Slice Flip Flops	184	1408	13%
Number of 4 input LUTs	347	1408	24%
Number of bonded IOBs	11	68	16%
Number of BRAMs	1	3	33%
Number of MULT18X18SIOs	1	3	33%
Number of GCLKs	1	24	4%

Figure 40: FPGA utilization report

5 Measurement results

Even though the inverter has originally been intended to be designed for 1 kW output power, it was tested only at output power below 100 W. The decision has been made due to the lack of adequate power sources, since the PV panels arrays are too costly at such a high output power ratings. In other words, there have been limited financial resources.

First, the circuit was tested supplied by two power supplies connected in series. Then, two PV panels connected in series with output open-circuit voltage of 42 V were used as the input power source

The following equipment has been used to test the final circuit:

- Laboratory power source STATRON Typ 2224.1

- Laboratory power source DELTA ELEKTRONIKA ES015-10

- Oscilloscope OWON PDS7102T

- DMM EXTECH INSTRUMENTS TRUE RMS MULTIMETER 430

- DMM VOREL 81780

- DMM ProsKit MT-1233D

Measurement result displayed on oscilloscope were acquired by PC Oscilloscope Suite application from OWON, the manufacturer of the oscilloscope. First, a lower voltage of 130 V_{AC} was generated in order to identify potential weak spots in the circuit. A 90 W solder iron was used as the test load. For safety reasons (there are lethal voltages present on the PCB) and to avoid possible damages to the equipment, measurement was conducted on output of one inverter leg only (or more precisely, output of the first LC filter). Full output voltage of 230 V_{AC} was measured using additional 2:1 voltage divider.
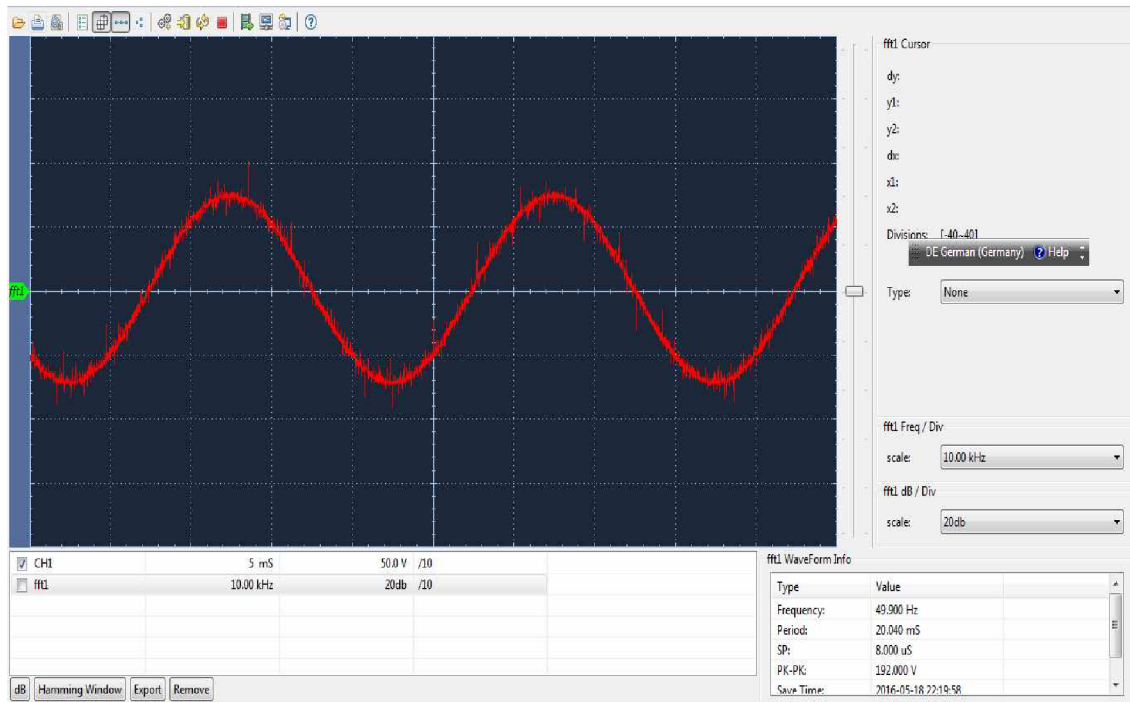
Figure 41: Waveforms of generated output voltage of 130 V$_{AC}$

Waveform of generated output voltage of is shown in Figure 41. As can be seen, there is no visible distortion of the sine shape. However, with different time scale, some details can be revealed, as shown in Figure 42.
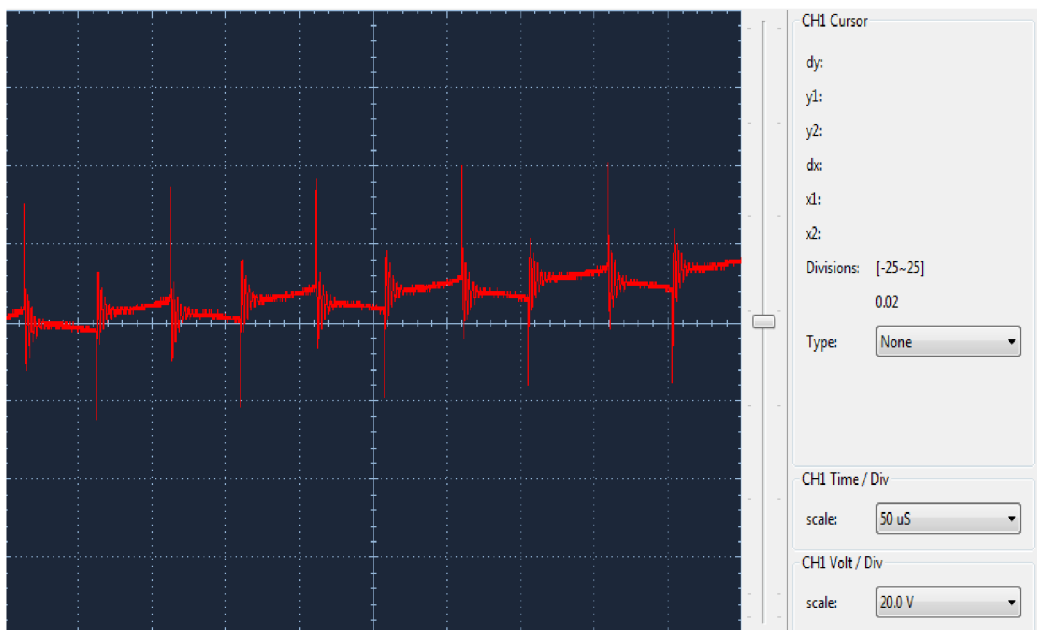
Figure 42: Detail of the waveform on the output of the LC filter

In Figure 42 can be seen that the switching waveform at 10 kHz is still present as well as high-frequency ringing. This can be caused by parasitic inductances in the output node or by non-optimal characteristics of the oscilloscope. Fast Fourier Transform was done by the PC Oscilloscope Suite and is shown in Figure 43.
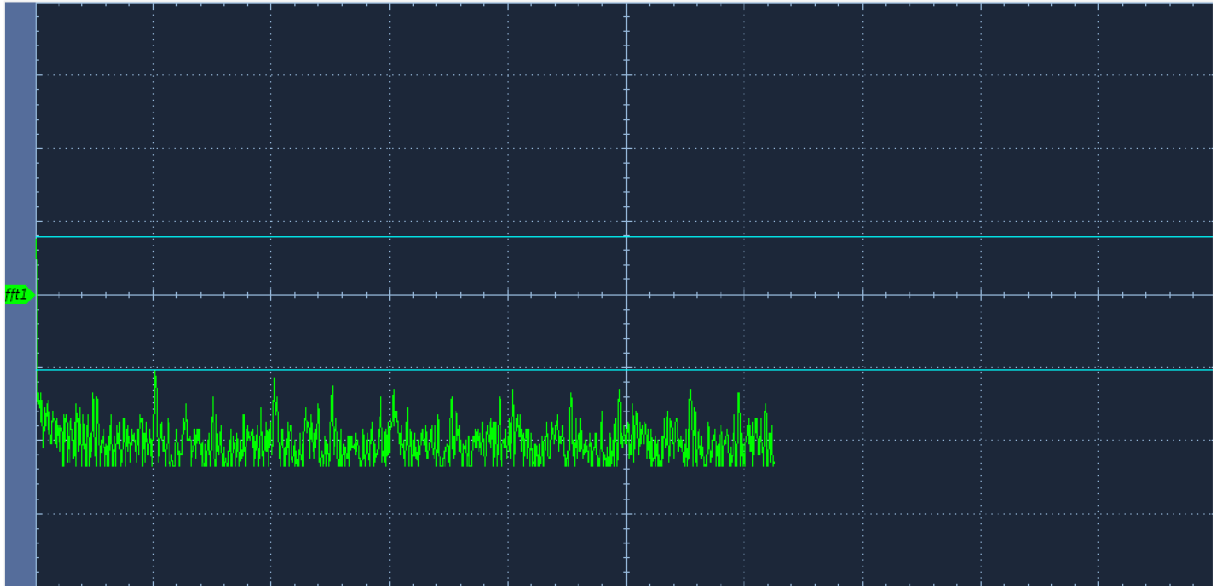
Figure 43: FFT of the output waveform at 130 V_{AC}, 10 kHz/div, 20 dB/div

As could be expected, there is a spectral line at 50 Hz and spectral lines at 10 kHz, 20 kHz and so on. The 10 kHz and 20 kHz spectral lines are caused by the switching waveform. It has to be said, however, that the oscilloscope used during this measurement has 8-bit sampling ADC resolution, which may contribute significantly to the noise and distortion level.
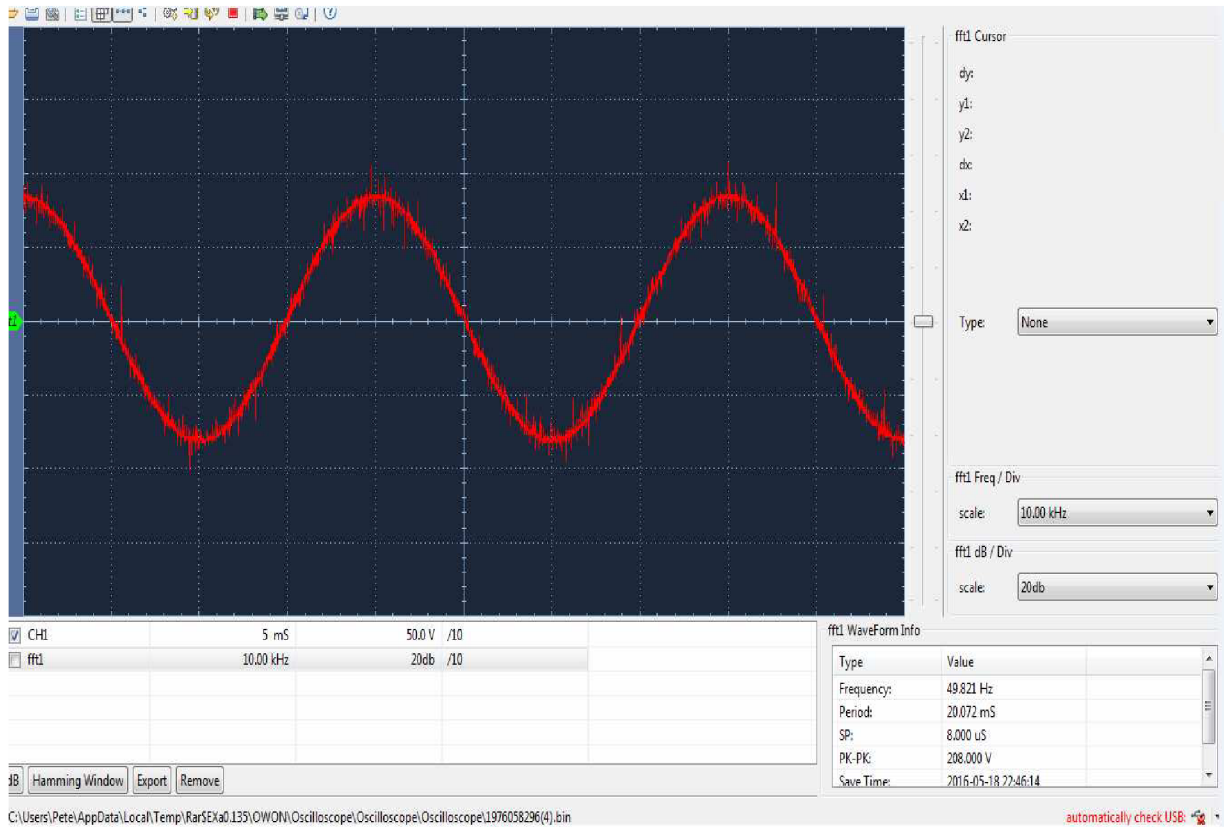
Figure 44: Output voltage waveform at 231 V_{AC}, 90 W (purely resistive) load

Inverter was supplied by laboratory voltage sources with supply voltage of 41,5 V. At load, the input current reached 2,35 A. This yields input power of 97,5 W and efficiency of 92 %. Idle current consumption (FPGA board + full-bridge) board was approximately 60 mA. Two weak spots were identified, where most of power losses seem to occur - boost IGBT and full-bridge output inductors. After five minutes of operation, temperature of output inductors as well as boost IGBT rose to approximately 40 °C. IPM remained almost cold, even though it was run without additional heatsink.

In Figure 45 is shown FFT of the output voltage waveform. High frequency spectral components are attenuated by 36 dB with respect to 50 Hz spectral line. Neglecting spectral lines above 20 kHz, this accounts for THD of approximately -35 dB or 1,8 %
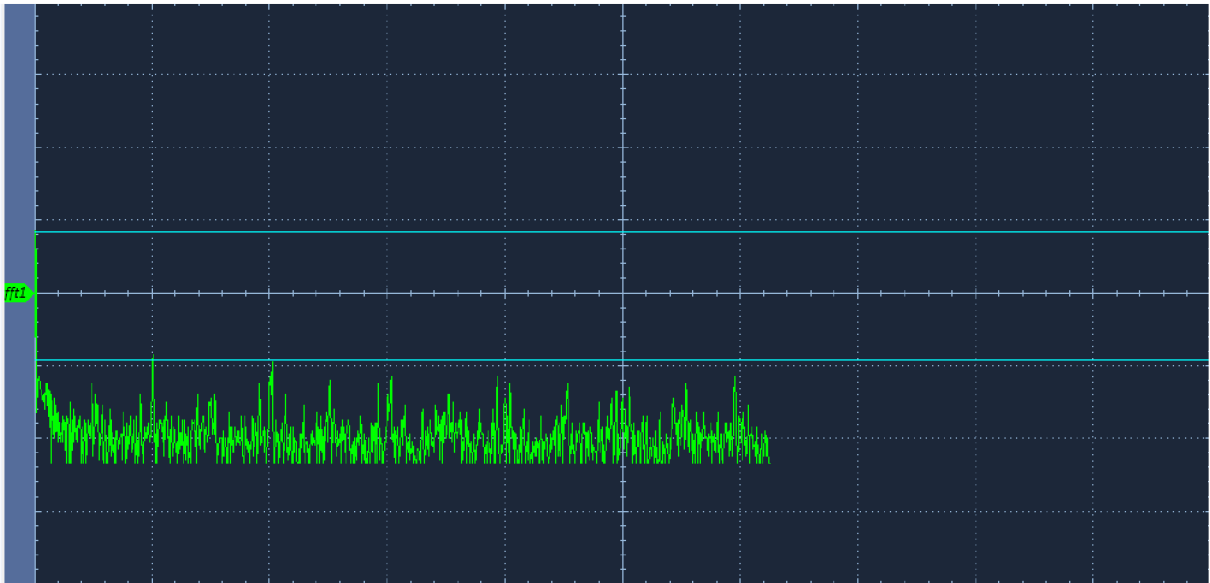
Figure 45: FFT of output waveform at 90 W load and 231 V$_{AC}$ output voltage, horizontal 10 kHz/div, vertical 20 dB/div

5.1 Measurement results with PV panels as the input source

To verify MPPT algorithm, two PV panels SFM30W connected in series were used as the input source. Open circuit voltage was 42,3 V and dropped to MPP value of 29,9 V at current of 1,24 A. These are rather low values compared to values provided by the manufacturer (18 V and 1,67 A from single panel - this would mean 36 V when connected in series). Reason for that may be insufficient irradiation/less than optimal angle between panel surface and sunlight or elevated temperature of the panel. The current and voltage values yield input power of 37 W. Again, a resistive load - soldering iron having heating element resistance of 1,5 kΩ was used as the test load. Output voltage reached 217 V$_{AC}$.

The last photograph in Figure 46 shows the test setup used during the measurements (power supplied from laboratory sources).
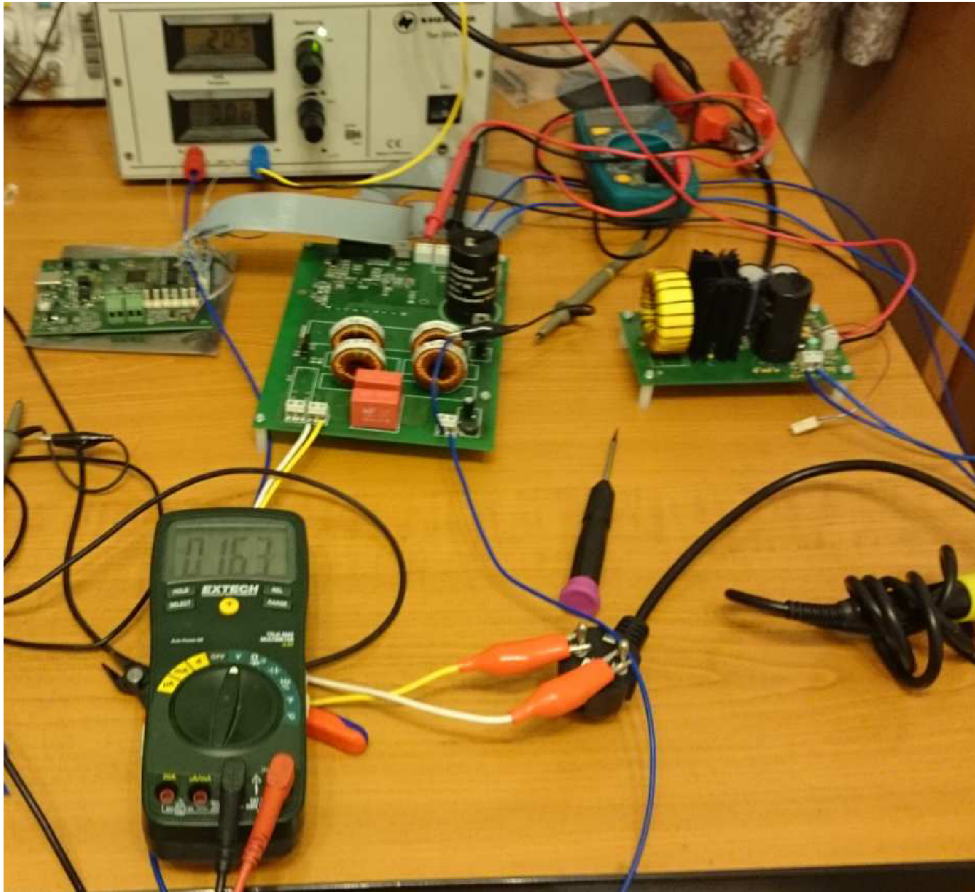
Figure 46: Test setup during the testing of the final circuit

Parameters of the final circuit can be summarized as shown below:

- Input voltage 17,5 V - 90 V [4]

- Standby current 60 mA

- THD 1,8 %

- Conversion efficiency > 90 %

---

[4] Below 17,5 V, UVLO protection of IPM is active.

6 Conclusion

Firstly, a brief description of power conversion process used in photovoltaic systems was done in this thesis. The reader has to be aware of the fact that small differences may exist among different power converters depending on manufacturer and output power.

A power converter design of a photovoltaic system was proposed. Two different approaches, first approach utilizing transformer-less, multiphase boost converter and second approach utilizing transformer-isolated push-pull converter, were demonstrated and simulated using LTspice IV simulator. Boost topology performed better in terms of efficiency and voltage stress of components. This can be considered critical, when the converter is delivering high output power, because cooling and components rated at higher voltage may increase resulting weight and cost significantly. Boost converter efficiency according to simulation was 98,4 %, while efficiency of push-pull converter was 83 %. Therefore, boost stage was chosen for the final realization.

Full-bridge DC-AC inverter stage was proposed. Simulation shown total harmonic distortion of the output signal of 1,6 % and efficiency of the stage is 96,3 %. Therefore, the efficiency of the entire converter system (the boost stage connected in series to the DC-AC inverter) can be calculated by multiplying the efficiency of boost stage by efficiency of DC-AC stage, which yields 94,7 %.

In the next section, boost converter and full-bridge converter stages were designed. Despite the initial intent, converter was designed only for output power of 250 W, for financial reasons. Expensive (especially power) components were replaced by their cheaper alternatives with decreased current ratings.

In the 4th section, VHDL model of the converter controller was described and appropriate FPGA device selected. Two different implemented MPPT algorithms were presented. Finally, in the last section, waveforms of generated sine signal were examined. THD of the signal was found to be 1,8 % - a value very similar to simulation results.

The main goal was accomplished, an alternative to the more common DSP-based solutions was proposed and presented. But one has to admit that DSP-based solutions provide some advantages, like for example rich amount of analog peripherals (ADCs, DACs and so on) integrated on the chip, whereas most FPGAs do not provide such functions. The solution is rather expensive.

Some of the design steps might have been performed better, for example insufficient trace clearances in bootstrap section of the IPM. These problems were revealed too late in the design phase. They did not cause any trouble during the testing, albeit the long-term reliability

might be impaired. The solution utilizing IPM (or any other solution with integrated bootstrap drivers) can be considered as one of the cheapest solutions, as it makes possible to connect low-voltage logic circuits directly to high-power, high-voltage devices without any special interface circuits. However, from the safety point of view, solutions using gate-drive transformer provide inherent safety barrier in case of failure. For example, in case of IGBT transistor breakdown, the insulation barrier of a gate-drive transformer may at least protect low-voltage circuit from damage. This is not guaranteed in case of IPM, where a galvanic path exists.

Boost converter was chosen for its inherent simplicity and absence of inductive coupling. Push-pull designs may profit from using low-voltage MOSFETs, which feature very low conduction and switching losses. The broad input voltage range in this project caused that these advantages of low-voltage MOSFETs almost disappeared. If the input voltage was in a lower range, then the push-pull solution would probably prevail.

7 References

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8 List of abbreviations

AC	-	Alternating Current
ADC	-	Analog-to-Digital Converter
DAC	-	Digital-to-Analog Converter
DC	-	Direct Current
DDS	-	Direct Digital Synthesis
DSP	-	Digital Signal Processor
EEPROM	-	Electrically Erasable Programmable Read-Only Memory
ESR	-	Equivalent Series Resistance
FFT	-	Fast Fourier Transform
FPGA	-	Field-Programmable Gate Array
GTO	-	Gate Turn-off Thyristor
IDE	-	Integrated Development Environment
IPM	-	Intelligent Power Module
IGBT	-	Insulated Gate Bipolar Transistor
JTAG	-	Joint Test Action Group
MCU	-	Microcontroller Unit
MOSFET	-	Metal-Oxid-Semiconductor Field-effect Transistor
MPP	-	Maximum Power Point
MPPT	-	Maximum Power Point Tracking
NTC	-	Negative Temperature Coefficient
P&O	-	Perturb and Observe
P-P	-	Peak-to-Peak
PV	-	Photovoltaic
PWM	-	Pulse-Width-Modulation
RMS	-	Root-Mean-Square
RTL	-	Register-Transfer-Level

SCR	-	Silicon-Controlled Rectifier
SPI	-	Serial Peripheral Interface
THD	-	Total Harmonic Distortion
USB	-	Universal Serial Bus
UVLO	-	Under-Voltage Lock-Out
VHDL	-	VHSIC Description Language
VHSIC	-	Very High Speed Integrated Circuit

A Simulations

A.1   Appendix - Simulation of multi-phase boost converter
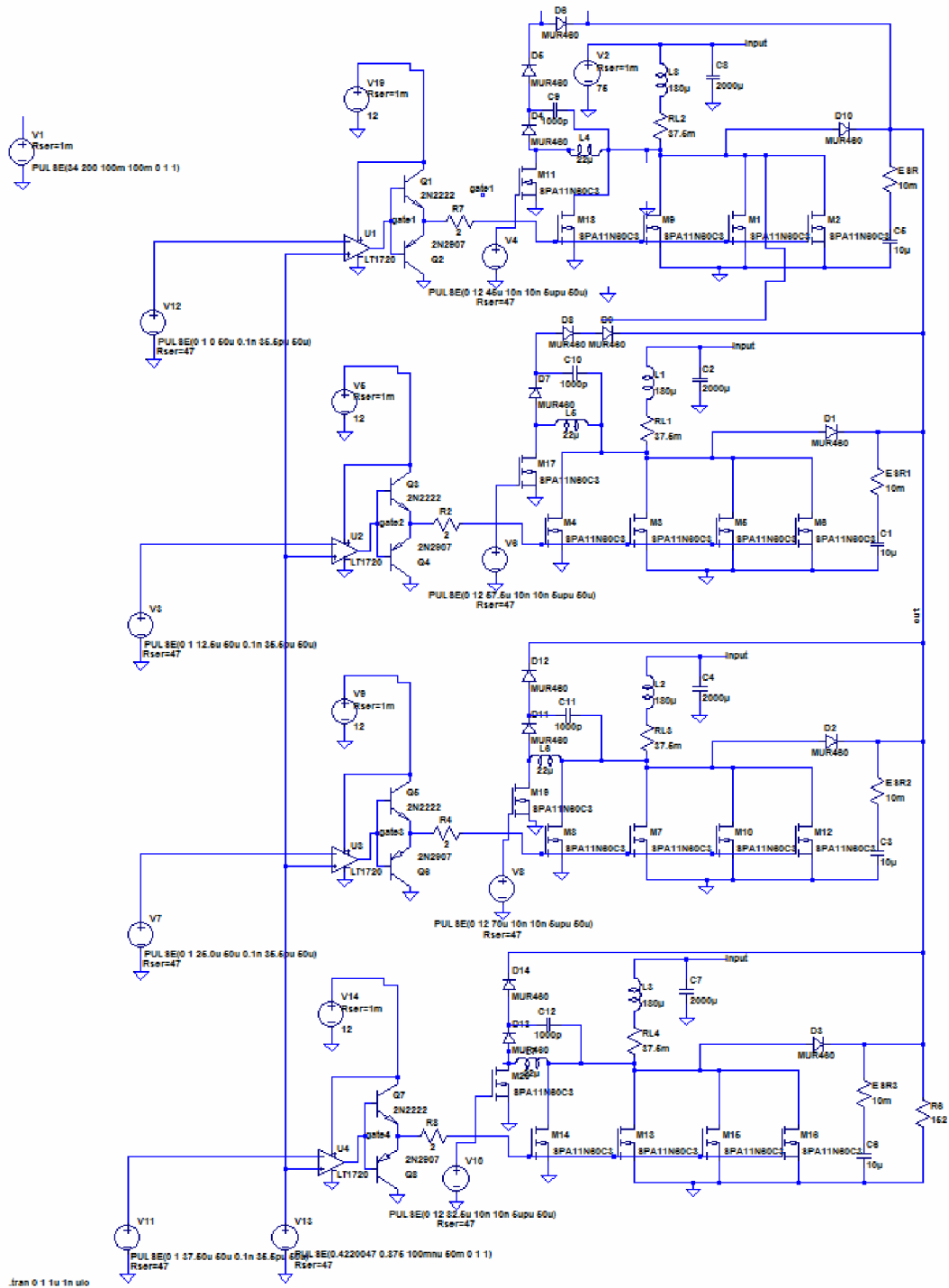
A.2 Appendix - Simulation of full-bridge inverter stage
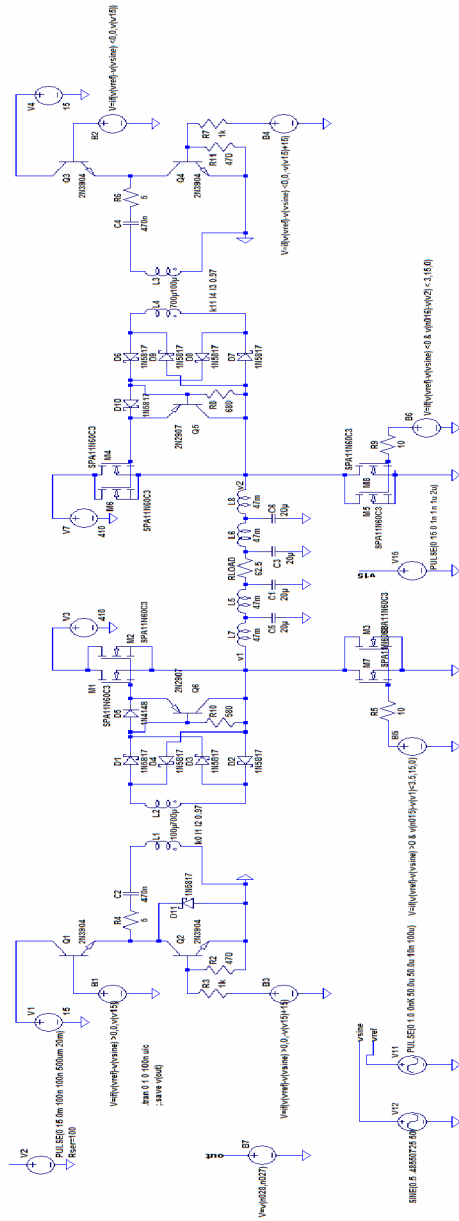
B Printed Circuit Boards

B.1   Appendix - FPGA board, TOP layer, Not To Scale
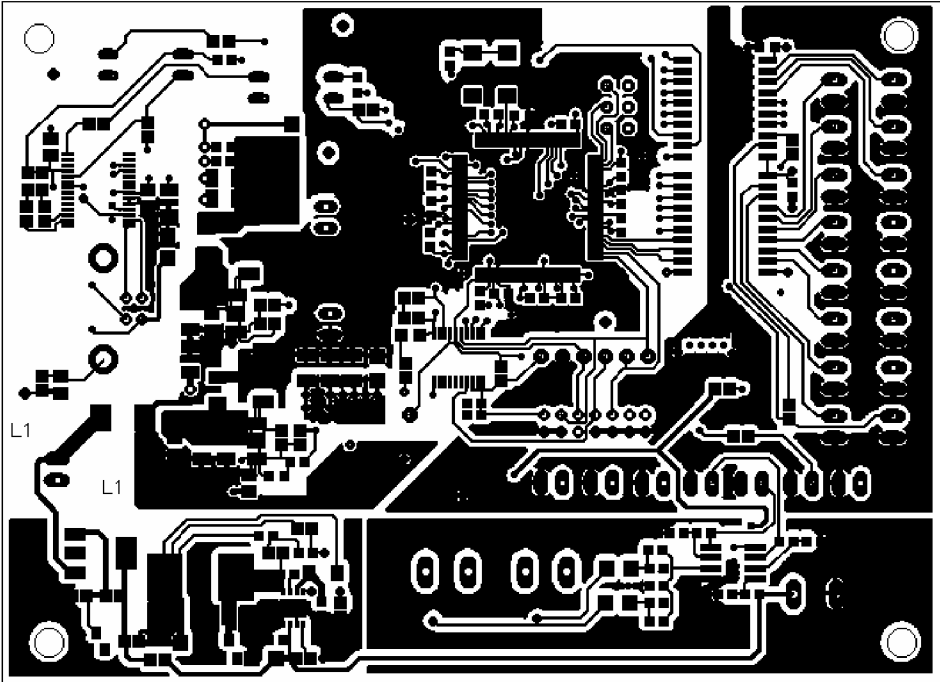
B.2   Appendix - FPGA board, BOTTOM layer, Not To Scale
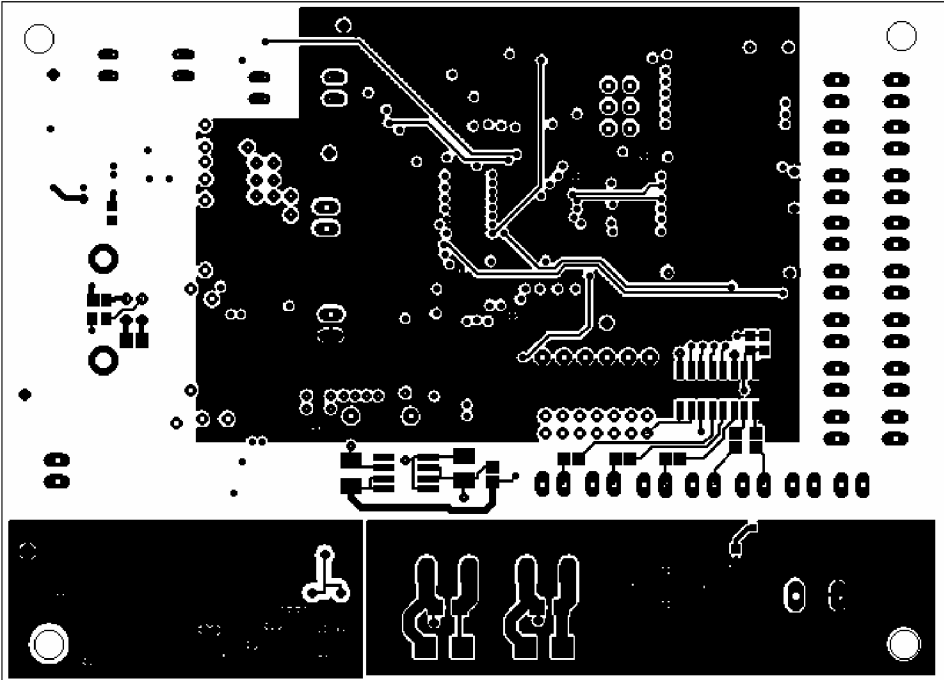
B.3   Appendix - Boost board, TOP layer, Not To Scale
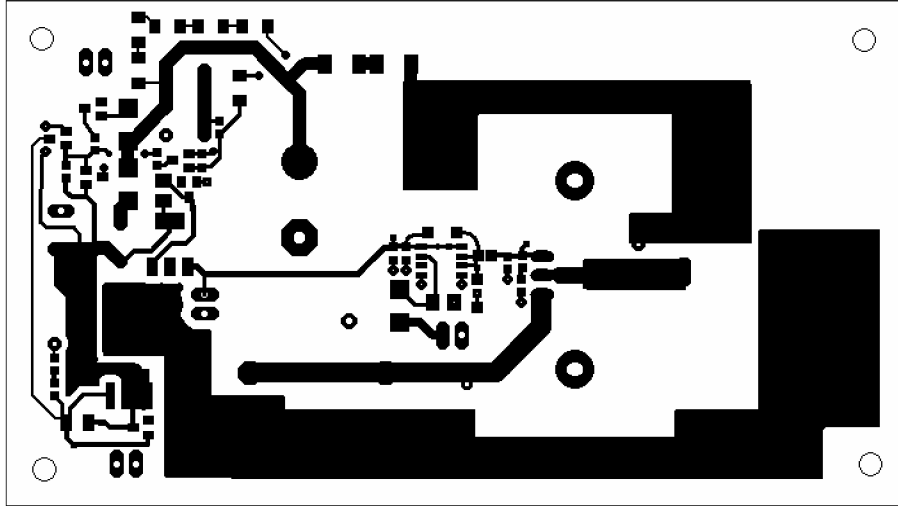
B.4   Appendix - Boost board, BOTTOM layer, Not To Scale
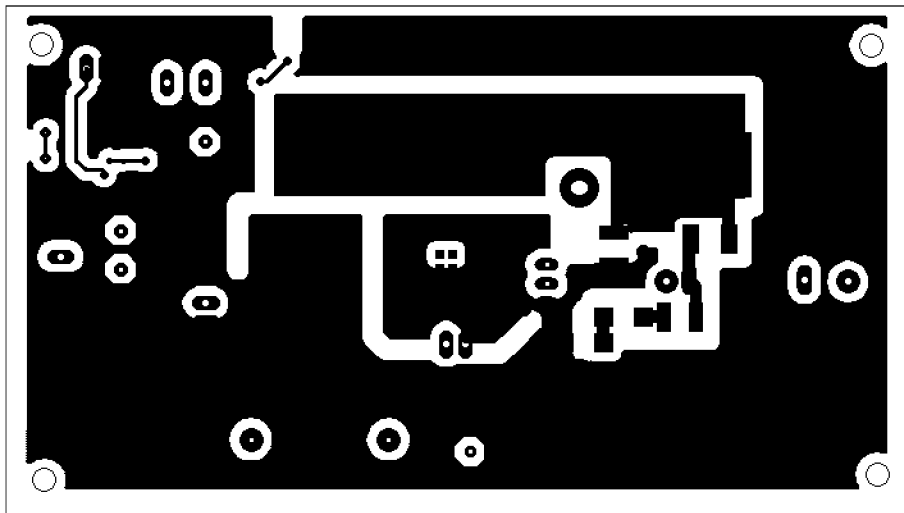
B.5 Appendix - Full-bridge board, TOP layer, Not To Scale
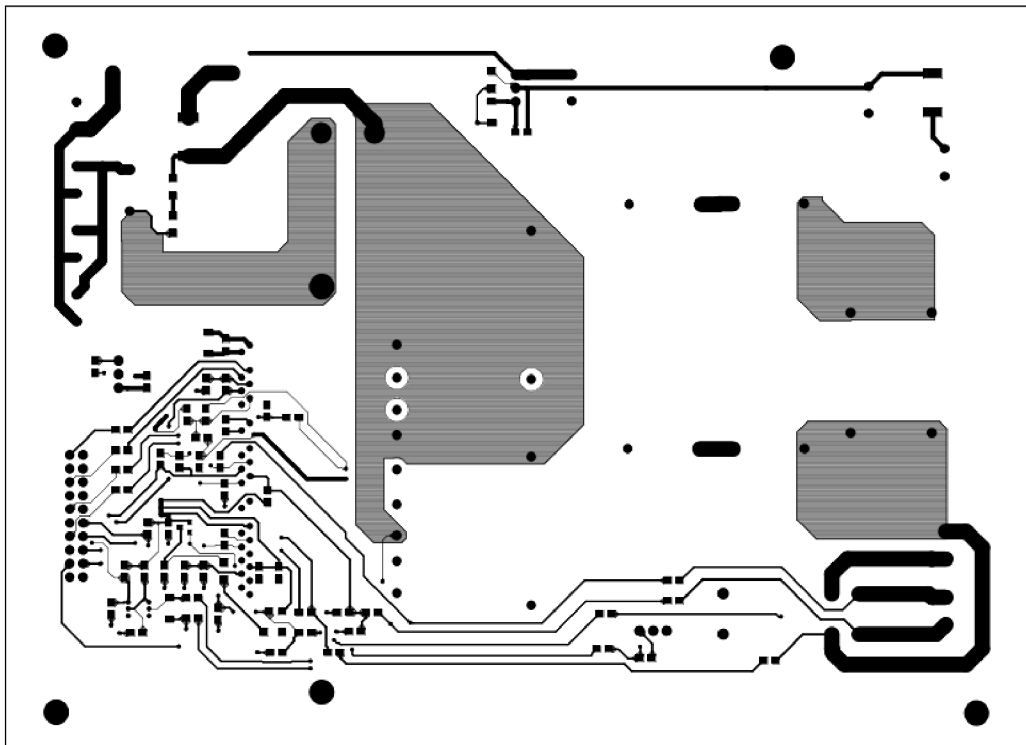
B.6 Appendix - Full-bridge board, BOTTOM layer, Not To Scale
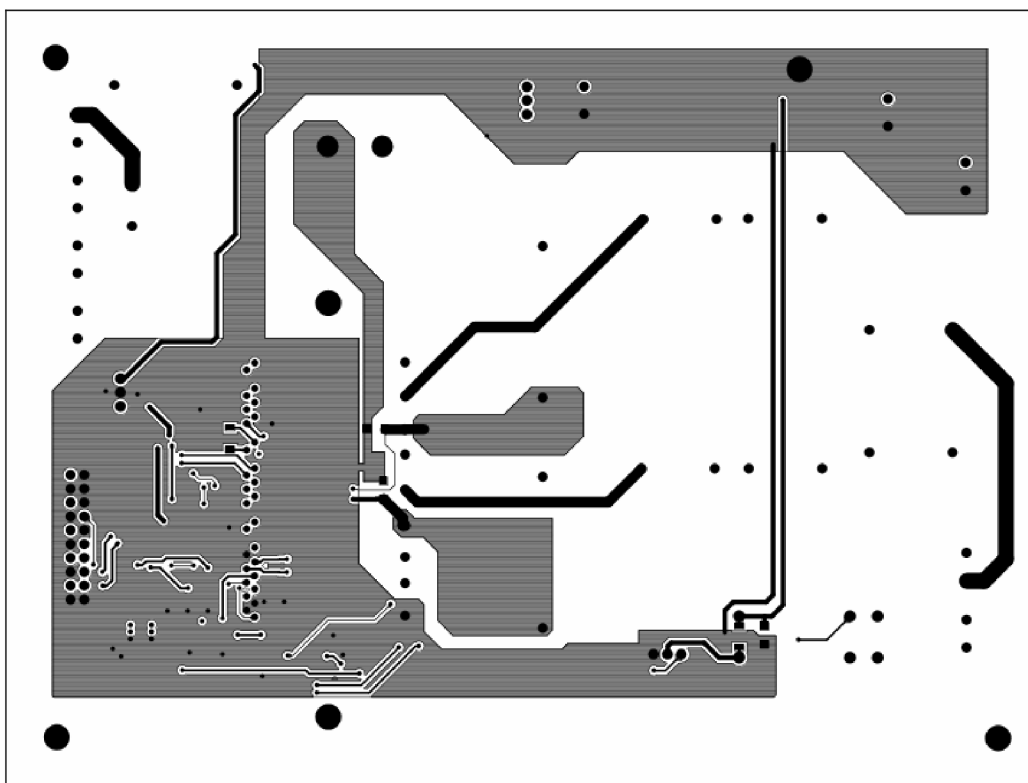
C Schematics

C.1   Appendix - Full-bridge board schematic
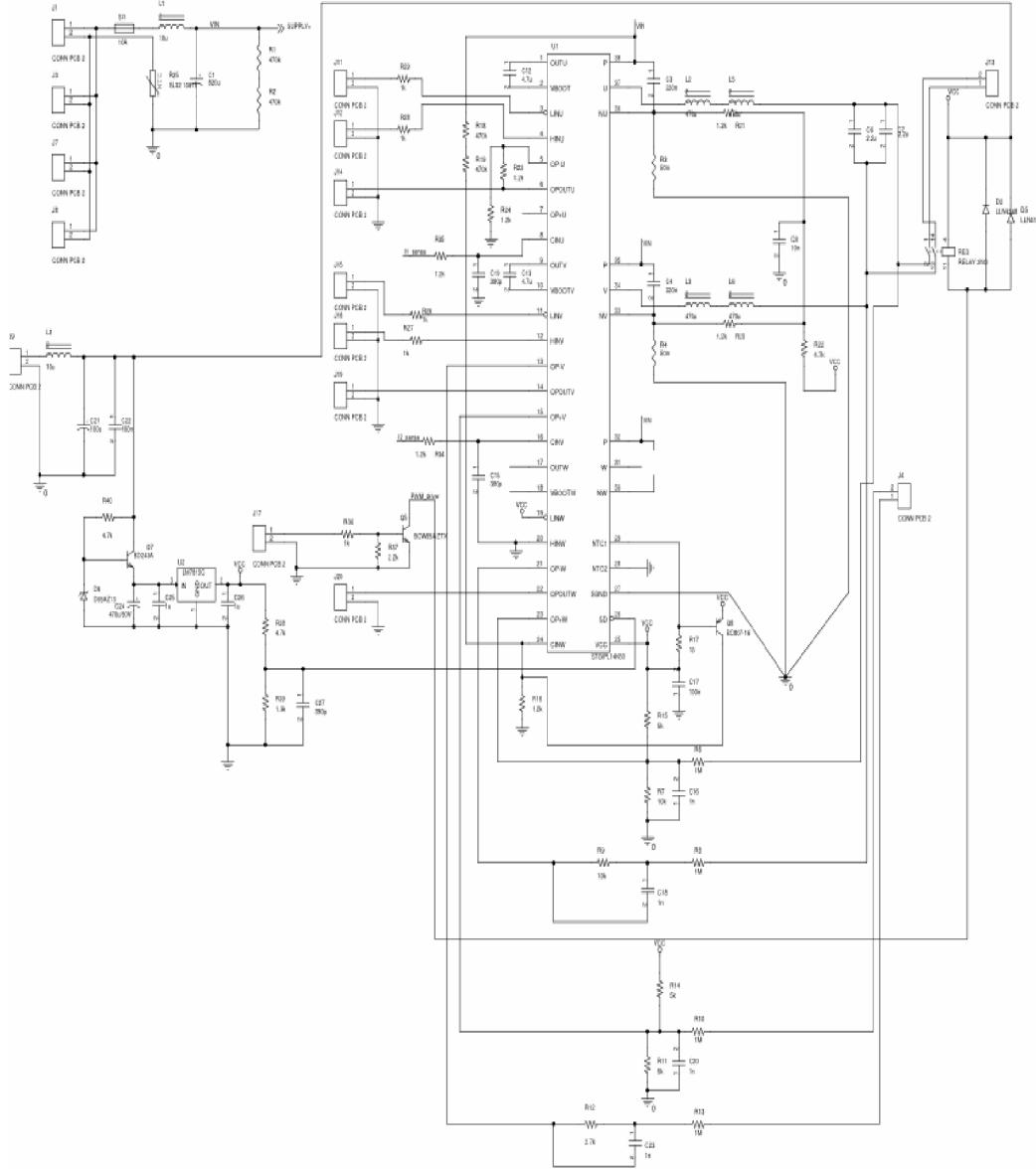
C.2 Appendix - FPGA board schematics
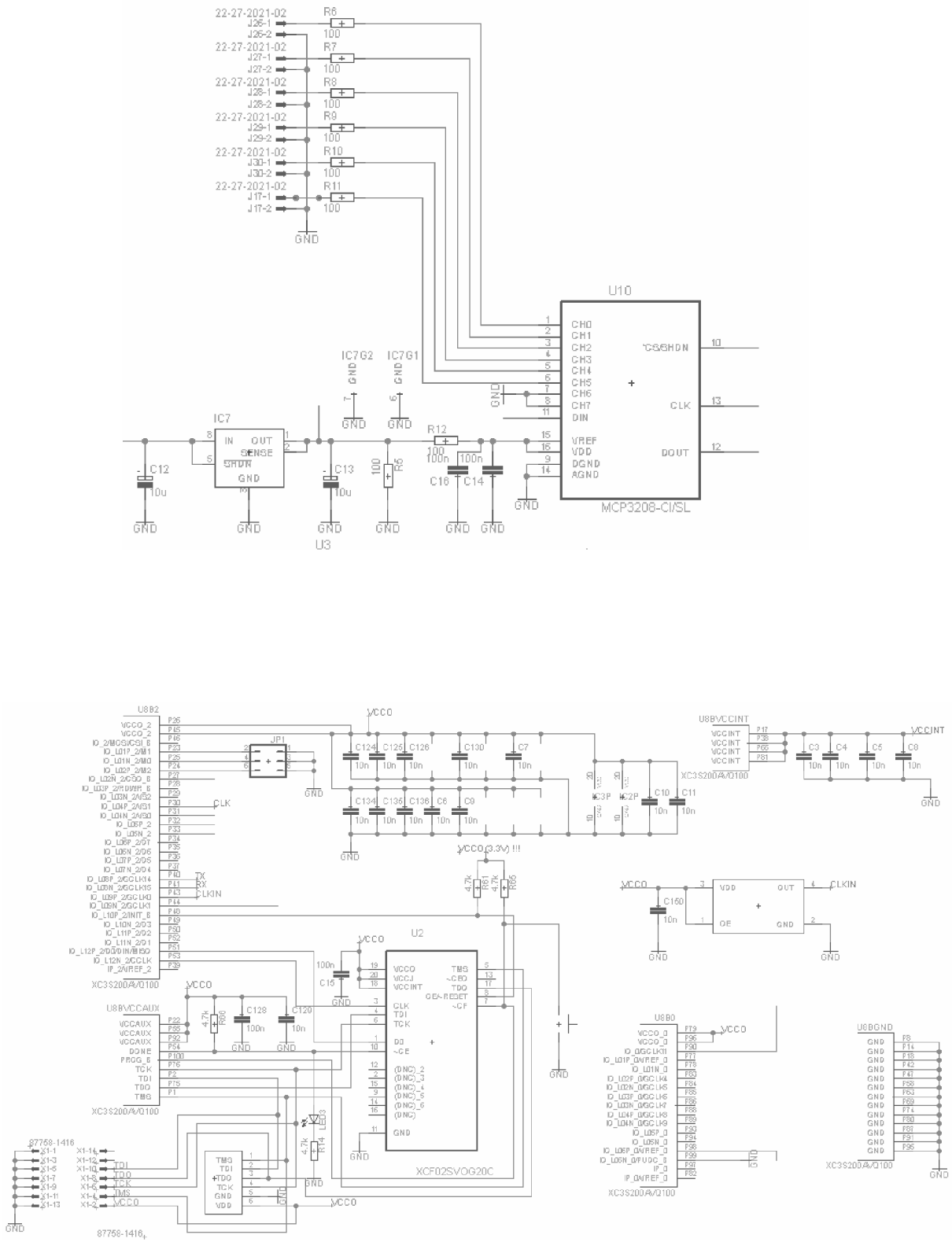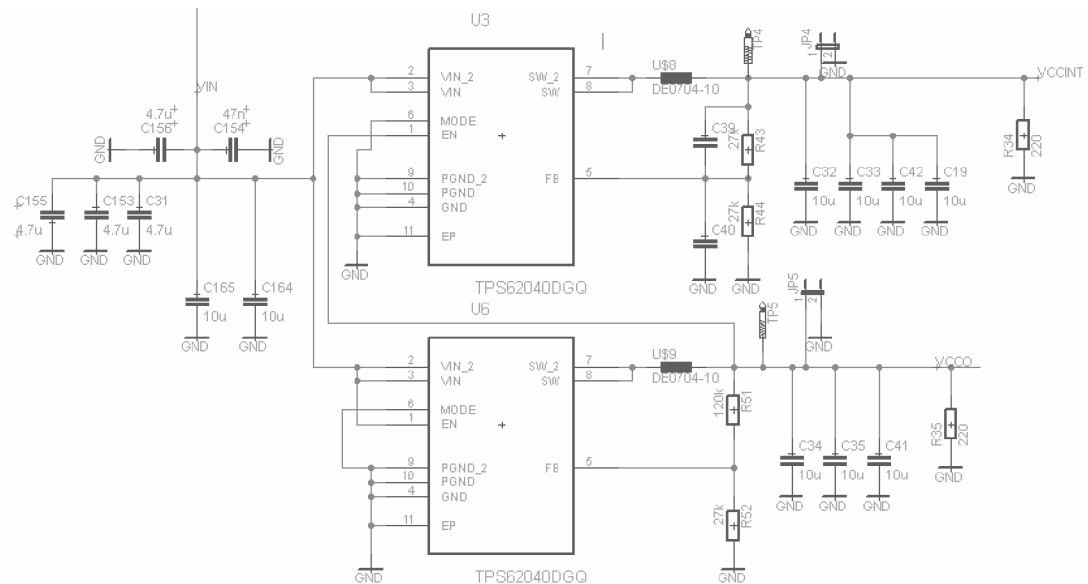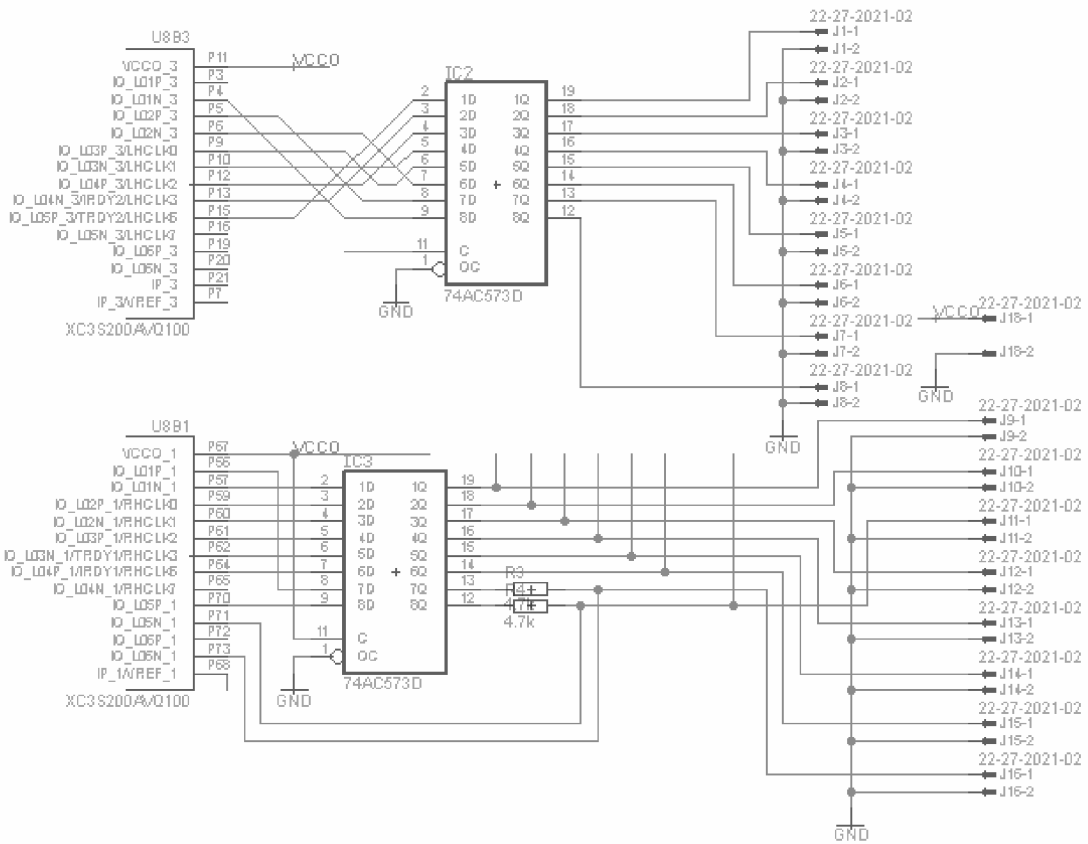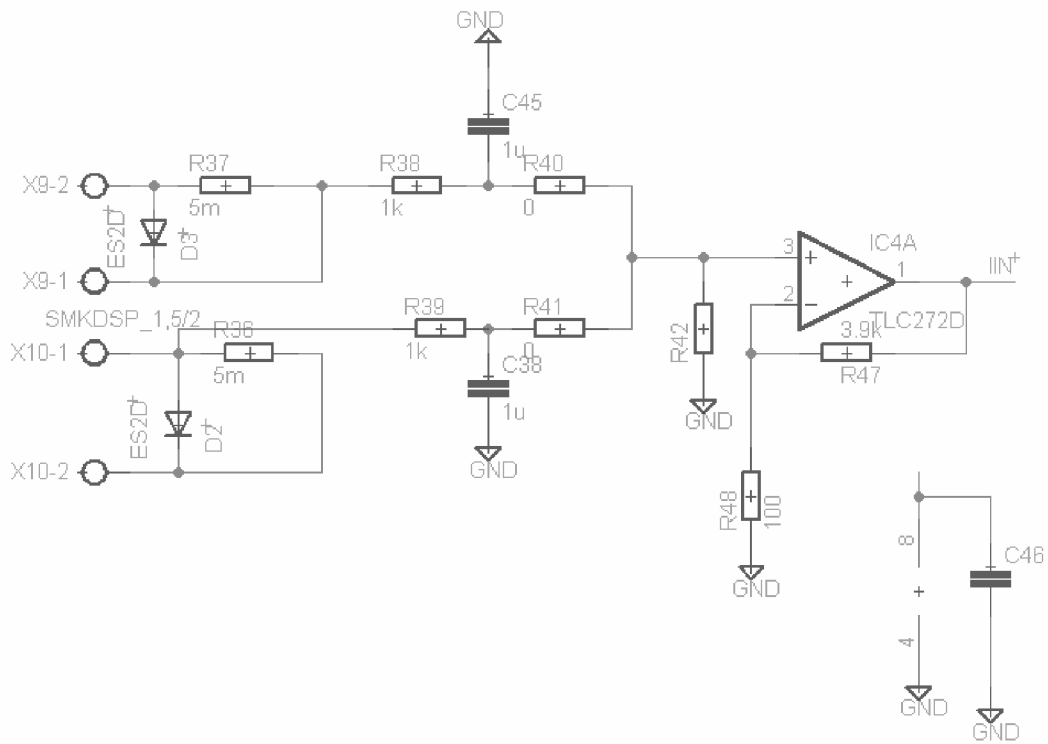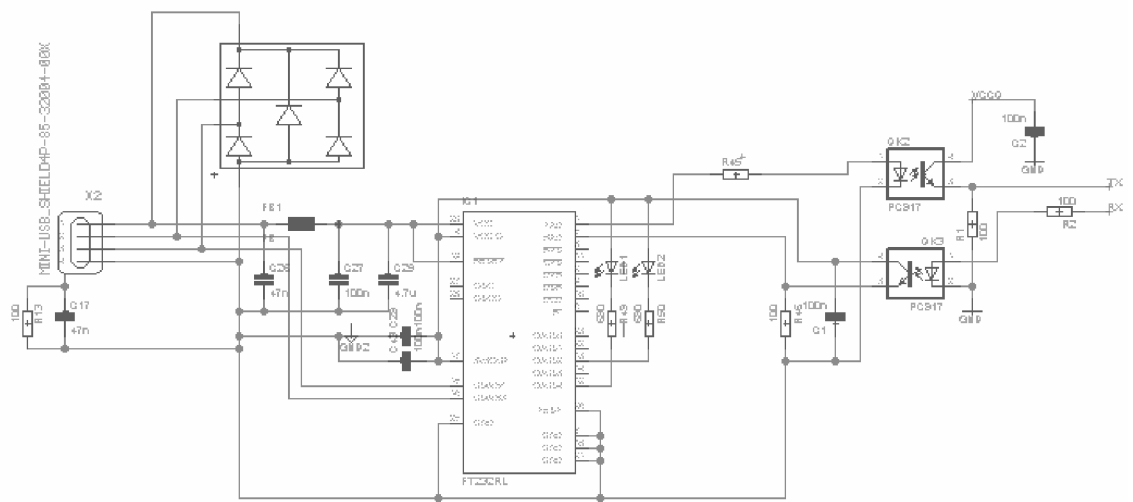
C.3   Appendix - Boost board schematic
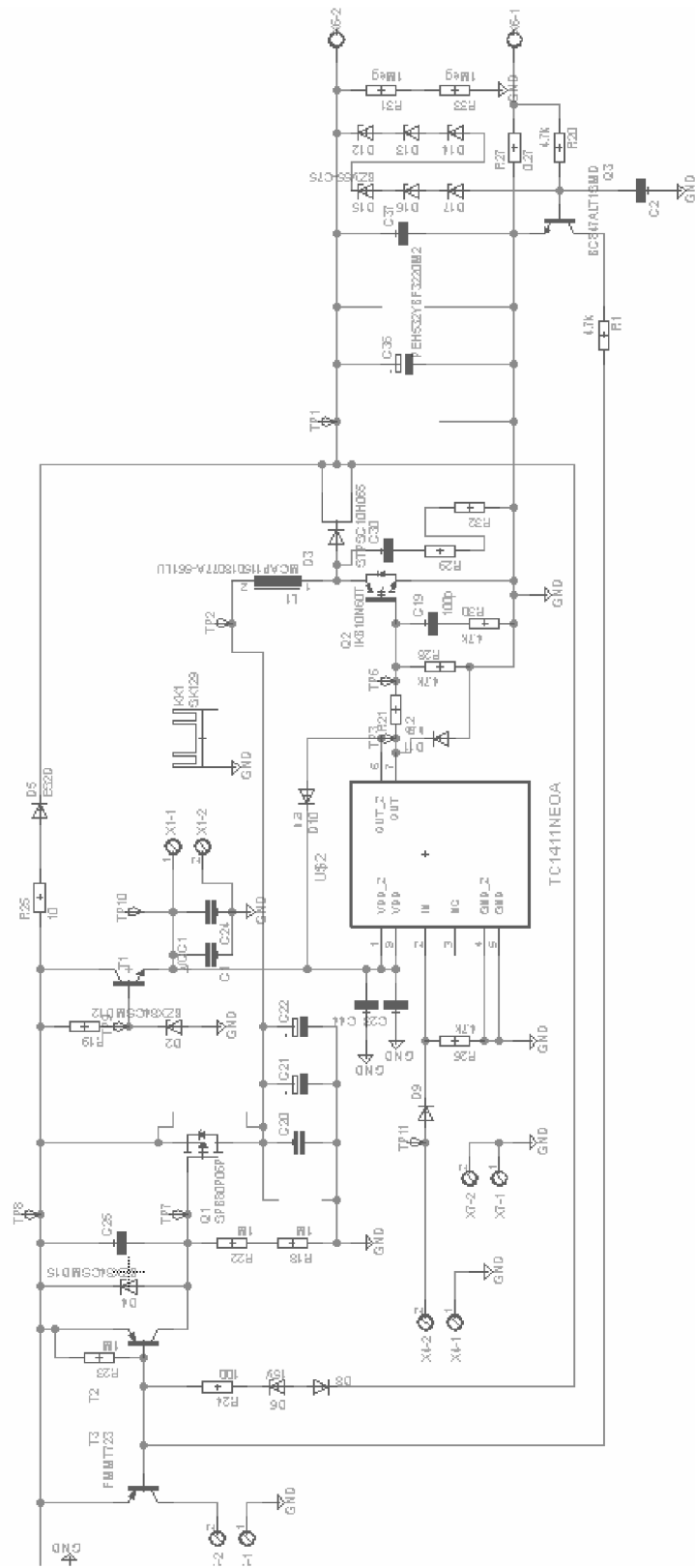
D   Bill of Material

D.1   Appendix - Bill of Material

Revised: Saturday, March 26, 2016
Revision:

Bill Of Materials   May 24,2016   21:40:15 Page1

Item	Quantity	Reference	Part
1	1	C1	820u
2	2	C3,C4	220n
3	2	C6,C7	2.2u
4	1	C8	10n
5	2	C12,C13	4.7u
6	3	C15,C19,C27	390p
7	4	C16,C18,C20,C23	1n
8	2	C17,C22	100n
9	1	C21	100u
10	1	C24	470u/50V
11	2	C25,C26	1u
12	2	D2,D5	LLN4148
13	1	D6	D05AZ13
14	15	J1,J3,J4,J7,J8,J9,J11, J12,J13,J14,J15,J17,J18, J19,J20	CONN PCB 2
15	2	L1,L8	10u
16	4	L2,L3,L5,L6	470u
17	1	Q5	BCW65A/ZTX
18	1	Q7	BD243A
19	1	Q8	BC807-16
20	1	RE3	RELAY 2NO
21	4	R1,R2,R18,R19	470k
22	2	R3,R4	50m
23	4	R6,R8,R10,R13	1M
24	2	R7,R9	10k
25	3	R11,R14,R15	5k
26	1	R12	2.7k
27	7	R16,R20,R21,R23,R24,R34, R35	1.2k
28	1	R17	10
29	3	R22,R38,R40	4.7k
30	1	R25	SL32 10015
31	5	R26,R27,R28,R29,R36	1k
32	1	R37	2.2k
33	1	R39	1.3k
34	1	SI1	10A
35	1	U1	STGIPL14K60
36	1	U2	LM7815C

Partlist

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Assembly variant:

Part	Value	Device	Package	Library	Sheet
C1	100n	C-EUC0603K	C0603K	resistor	1
C2	100n	C-EUC0603K	C0603K	resistor	1
C3	10n	C-EUC0603K	C0603K	resistor	1
C4	10n	C-EUC0603K	C0603K	resistor	1
C5	10n	C-EUC0603K	C0603K	resistor	1
C6	10n	C-EUC0603K	C0603K	resistor	1
C7	10n	C-EUC0603K	C0603K	resistor	1
C8	10n	C-EUC0603K	C0603K	resistor	1
C9	10n	C-EUC0603K	C0603K	resistor	1
C10	10n	C-EUC0603K	C0603K	resistor	1
C11	10n	C-EUC0603K	C0603K	resistor	1
C12	10u	CPOL-EUSMCB	SMC_B	resistor	1
C13	10u	CPOL-EUSMCB	SMC_B	resistor	1
C14	100n	C-EUC0603K	C0603K	resistor	1
C15	100n	C-EUC0603K	C0603K	resistor	1
C16	100n	C-EUC0603K	C0603K	resistor	1
C17	47n	C-EUC0805K	C0805K	resistor	1
C18	n,a	C-EUC0603	C0603	resistor	1
C19	10u	C-EUC1206K	C1206K	resistor	1
C26	47n	C-EUC0805K	C0805K	resistor	1
C27	100n	C-EUC0805K	C0805K	resistor	1
C28	100n	C-EUC0805K	C0805K	resistor	1
C29	4.7u	C-EUC1206K	C1206K	resistor	1
C31	4.7u	C-EUC1206K	C1206K	resistor	1
C32	10u	C-EUC1206K	C1206K	resistor	1
C33	10u	C-EUC1206K	C1206K	resistor	1
C34	10u	C-EUC1206K	C1206K	resistor	1
C35	10u	C-EUC1206K	C1206K	resistor	1
C38	1u	C-EUC0603	C0603	resistor	2
C39		C-EUC0603K	C0603K	resistor	1
C40		C-EUC0603K	C0603K	resistor	1
C41	10u	C-EUC1206K	C1206K	resistor	1
C42	10u	C-EUC1206K	C1206K	resistor	1
C43	100n	C-EUC0603K	C0603K	resistor	1
C45	1u	C-EUC0603	C0603	resistor	2
C46		C-EUC0603	C0603	resistor	2
C47	10n	C-EUC0603	C0603	resistor	1
C48	10n	C-EUC1206	C1206	resistor	1
C49	10n	C-EUC0603	C0603	resistor	1
C50	10n	C-EUC0603	C0603	resistor	1
C51	10n	C-EUC0603	C0603	resistor	1
C52	10n	C-EUC1206	C1206	resistor	1
C124	10n	C-EUC0603K	C0603K	resistor	1
C125	10n	C-EUC0603K	C0603K	resistor	1
C126	10n	C-EUC0603	C0603	resistor	1
C128	100n	C-EUC0603K	C0603K	resistor	1
C129	10n	C-EUC0603K	C0603K	resistor	1
C130	10n	C-EUC0603K	C0603K	resistor	1
C134	10n	C-EUC0603K	C0603K	resistor	1
C135	10n	C-EUC0603K	C0603K	resistor	1
C136	10n	C-EUC0603K	C0603K	resistor	1
C150	10n	C-EUC0603K	C0603K	resistor	1

Part	Value	Device	Package	Library	Qty
C153	4.7u	C-EUC1206K	C1206K	resistor	1
C154	47n	C-EUC0805K	C0805K	resistor	1
C155	4.7u	C-EUC0805K	C0805K	resistor	1
C156	4.7u	C-EUC0805K	C0805K	resistor	1
C164	10u	C-EUC1206K	C1206K	resistor	1
C165	10u	C-EUC1206K	C1206K	resistor	1
D1		DIODE-MELF-MLL41	MELF-MLL41	diode	1
D2	ES2D	ES2D	SMB	diode	2
D3	ES2D	ES2D	SMB	diode	2
D7		DIODE-SOD80C	SOD80C	diode	1
D18	BAS40	BAS40	SOT23	diode	1
D19	BZX84CSMD5v6	BZX84CSMD	TO236	diode	1
FB1	FB	FB	R1206	resistor	1
IC1	FT232RL	FT232RL	SSOP28	ftdichip	1
IC2	74AC573D	74AC573D	SO20W	74xx-eu	1
IC3	74AC573D	74AC573D	SO20W	74xx-eu	1
IC4	TLC272D	TLC272D	SO08	linear	2
IC7		LT1129CS8	SOIC8	linear-technology	1
J1	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J2	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J3	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J4	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J5	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J6	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J7	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J8	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J9	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J10	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J11	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J12	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J13	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J14	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J15	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J16	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J17	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J18	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J25	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J26	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J27	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J28	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J29	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
J30	22-27-2021-02	22-27-2021-02	6410-02	con-molex	1
JP1		JP3Q	JP3Q	jumper	1
JP4		JP1E	JP1	jumper	1
JP5		JP1E	JP1	jumper	1
L3		DO3316PAA	AAA	inductor-coilcraft - Copy	1
LED1		LEDCHIPLED_0805	CHIPLED_0805	led	1
LED2		LEDCHIPLED_0805	CHIPLED_0805	led	1
LED3		LEDCHIPLED_0805	CHIPLED_0805	led	1
OK2	PC817	PC817	DIL04	optocoupler	1
OK3	PC817	PC817	DIL04	optocoupler	1
R1	100	R-EU_R0805	R0805	resistor	1
R2	100	R-EU_R0805	R0805	resistor	1
R3	4.7k	R-EU_R0805	R0805	resistor	1
R4	4.7k	R-EU_R0805	R0805	resistor	1
R5	100	R-EU_R0805	R0805	resistor	1
R6	100	R-EU_R0805	R0805	resistor	1
R7	100	R-EU_R0805	R0805	resistor	1
R8	100	R-EU_R0805	R0805	resistor	1
R9	100	R-EU_R0805	R0805	resistor	1
R10	100	R-EU_R0805	R0805	resistor	1
R11	100	R-EU_R0805	R0805	resistor	1
R12	100	R-EU_R0805	R0805	resistor	1
R13	100	R-EU_R0805	R0805	resistor	1
R14	4.7k	R-EU_R0805	R0805	resistor	1
R15	100	R-EU_R0805	R0805	resistor	1
R16	n,a	R-EU_R0805	R0805	resistor	1
R17	100	R-EU_R0805	R0805	resistor	1
R34	220	R-EU_R1206	R1206	resistor	1
R35	220	R-EU_R1206	R1206	resistor	1
R36	5m	R-EU_R1206	R1206	resistor	2
R37	5m	R-EU_R1206	R1206	resistor	2

Part	Value	Device	Package	Library	Sheet
R38	1k	R-EU_R1206	R1206	resistor	2
R39	1k	R-EU_R1206	R1206	resistor	2
R40	0	R-EU_R0603	R0603	resistor	2
R41	0	R-EU_R0603	R0603	resistor	2
R42		R-EU_R0603	R0603	resistor	2
R43	27k	R-EU_R0805	R0805	resistor	1
R44	27k	R-EU_R0805	R0805	resistor	1
R45	100	R-EU_R0805	R0805	resistor	1
R46	100	R-EU_R0805	R0805	resistor	1
R47	3.9k	R-EU_R0603	R0603	resistor	2
R48	100	R-EU_R0603	R0603	resistor	2
R49	680	R-EU_R0805	R0805	resistor	1
R50	680	R-EU_R0805	R0805	resistor	1
R51	120k	R-EU_R0805	R0805	resistor	1
R52	27k	R-EU_R0805	R0805	resistor	1
R53	270k	R-EU_R0603	R0603	resistor	2
R54	4.7k	R-EU_R0603	R0603	resistor	2
R55	4.7k	R-EU_R0603	R0603	resistor	2
R56	4.7k	R-EU_R0603	R0603	resistor	2
R57	100	R-EU_R0805	R0805	resistor	1
R58	100	R-EU_R0805	R0805	resistor	1
R59	100	R-EU_R0805	R0805	resistor	1
R60	100	R-EU_R0805	R0805	resistor	1
R61	4.7k	R-EU_R0805	R0805	resistor	1
R62	1	R-EU_R0805	R0805	resistor	1
R65	4.7k	R-EU_R0805	R0805	resistor	1
R66	4.7k	R-EU_R0805	R0805	resistor	1
T4		-NPN-SOT223	SOT223	transistor-neu-to92	1
TP4	PTR1B1,27	PTR1B1,27	B1,27	testpad	1
TP5	PTR1B1,27	PTR1B1,27	B1,27	testpad	1
U$1	PRTR5VOU2X	PRTR5VOU2X	AAA	diode	1
U$3	SIGNLE_POLE_SW	SIGNLE_POLE_SW	SINGLE_SW	switch	1
U$4	JTAG-HEADER	JTAG-HEADER	JTAG	con-commcon	1
U$5	ASV	ASV	ASV-LCC	crystal	1
U$8	DE0704-10	DE0704-10	DE0704-10	inductors	1
U$9	DE0704-10	DE0704-10	DE0704-10	inductors	1
U1	LM5017SD/NOPB	LM5017SD/NOPB	DFN400X400X80-9N	74xx-little-de	1
U2	XCF02SVOG20C	XCF02SVOG20C	SOP65P640X119-20N	xilinx-xcv	1
U3	TPS62040DGQ	TPS62040DGQ	SOP50P490X110-11N	resistor	1
U6	TPS62040DGQ	TPS62040DGQ	SOP50P490X110-11N	resistor	1
U8	XC3S200AVQ100	XC3S200AVQ100	VQ100	xilinx_devices	1
U10	MCP3208-CI/SL	MCP3208-CI/SL	SOIC127P600X175-16N	74xx-eu	1
X1	87758-1416	87758-1416	87758-1416	con-molex	1
X2	MINI-USB_SHIELD4P-85-32004-00X	MINI-USB_SHIELD4P-85-32004-00X	85-32004-00X	con-cypressindustries	1
X8		W237-02P	W237-132	con-wago-508	2
X9		SMKDSP_1,5/2	SMKDSP_1,5/2	con-phoenix-smkdsp	2
X10	SMKDSP_1,5/2	SMKDSP_1,5/2	SMKDSP_1,5/2	con-phoenix-smkdsp	2

Partlist

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Assembly variant:

Part	Value	Device	Package	Library	Sheet
C1		C-EUC0603K	C0603K	resistor	2
C2		C-EUC0603K	C0603K	resistor	2
C19		C-EUC0603K	C0603K	resistor	2
C20	1u	C-EU075-032X103	C075-032X103	resistor	2
C21	470u	CPOL-EUE7.5-18	E7,5-18	resistor	2
C22	470u	CPOL-EUE7.5-18	E7,5-18	resistor	2
C23		C-EUC0603K	C0603K	resistor	2
C24		C-EUC0603K	C0603K	resistor	2
C25		C-EUC1206K	C1206K	resistor	2
C30		C-EUC1812K	C1812K	resistor	2
C36	PEH532YBF3220M2	CPOL-EUE10-25	EB25D	resistor	2
C37		C-EUC1812K	C1812K	resistor	2

Part	Value	Device	Package	Description	Qty
C44	4x 1u	C-EUC0603K	C0603K	resistor	2
D2	BZX84CSMD12	BZX84CSMD	TO236	diode	2
D3	STPSC10H065	BY229B	TO263AB	diode	2
D4	BZX84CSMD15	BZX84CSMD	TO236	diode	2
D5	ES2D	ES2D	SMB	diode	2
D6	15V	ZENER-DIODESOT23	SOT23	diode	2
D8		ES2D	SMB	diode	2
D9	mur460	ES2D	SMB	diode	2
D10		MBR0520LT	SOD123	diode	2
D11		MBR0520LT	SOD123	diode	2
D12		ZENER-DIODESOD80C	SOD80C	diode	2
D13		ZENER-DIODESOD80C	SOD80C	diode	2
D14		ZENER-DIODESOD80C	SOD80C	diode	2
D15	BZV55-C75	ZENER-DIODESOD80C	SOD80C	diode	2
D16		ZENER-DIODESOD80C	SOD80C	diode	2
D17		ZENER-DIODESOD80C	SOD80C	diode	2
KK1	SK129	SK129-PAD	SK129	heatsink	2
L1	MCAP115018077A-561LU	SFT1240	SFT1240	inductors	2
Q1	SPB80P06P	SPB80P06P	TO263	transistor-fet	2
Q2	IKP10N60T	IRG4BC15UD--L	TO262-V	transistor-power	2
Q3	BC847ALT1SMD	BC847ALT1SMD	SOT23	transistor-npn	2
R1	4.7k	R-EU_R0603	R0603	resistor	2
R18	1M	R-EU_R0603	R0603	resistor	2
R19		R-EU_M1206	M1206	resistor	2
R20	4.7k	R-EU_R0603	R0603	resistor	2
R21	2.2	R-EU_R0805	R0805	resistor	2
R22	1M	R-EU_R0603	R0603	resistor	2
R23	1M	R-EU_R0603	R0603	resistor	2
R24	100	R-EU_R0603	R0603	resistor	2
R25	10	R-EU_0414/5V	0414V	resistor	2
R26	4.7k	R-EU_M1206	M1206	resistor	2
R27	0.27	R-EU_0414/5V	0414V	resistor	2
R28	4.7k	R-EU_R0603	R0603	resistor	2
R29		R-EU_MELF0207W	MINI_MELF-0207W	resistor	2
R30	4.7k	R-EU_R0603	R0603	resistor	2
R31	1Meg	R-EU_MELF0207R	MINI_MELF-0207R	resistor	2
R32		R-EU_MELF0207W	MINI_MELF-0207W	resistor	2
R33	1Meg	R-EU_MELF0207R	MINI_MELF-0207R	resistor	2
T1		PZT2222A-NPN-SOT223	SOT223	transistor-neu-to92	2
T2		BC807-16-PNP-SOT23-BEC	SOT23-BEC	transistor-neu-to92	2
T3	FMMT723	BC807-16-PNP-SOT23-BEC	SOT23-BEC	transistor-neu-to92	2
TP1	TPSTP07SQ	TPSTP07SQ	TP07SQ	testpad	2
TP2	TPSTP07SQ	TPSTP07SQ	TP07SQ	testpad	2
TP3	TPSTP07SQ	TPSTP07SQ	TP07SQ	testpad	2
TP6	TPSTP07SQ	TPSTP07SQ	TP07SQ	testpad	2
TP7	TPSTP07SQ	TPSTP07SQ	TP07SQ	testpad	2
TP8	TPSTP07SQ	TPSTP07SQ	TP07SQ	testpad	2
TP9	TPSTP07SQ	TPSTP07SQ	TP07SQ	testpad	2
TP10	TPSTP07SQ	TPSTP07SQ	TP07SQ	testpad	2
TP11	TPSTP07SQ	TPSTP07SQ	TP07SQ	testpad	2
U$2	TC1411NEOA	TC1411NEOA	SOIC127P600X175-8N	40xx	2
X1		MPT2	2POL254	con-phoenix-254	2
X3		W237-02P	W237-132	con-wago-508	2
X4		MPT2	2POL254	con-phoenix-254	2
X5		MPT2	2POL254	con-phoenix-254	2
X6		W237-02P	W237-132	con-wago-508	2
X7		MPT2	2POL254	con-phoenix-254	2