

BRNO UNIVERSITY OF TECHNOLOGY

Faculty of Electrical Engineering  
and Communication

MASTER'S THESIS

Brno, 2016

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# BRNO UNIVERSITY OF TECHNOLOGY

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

## FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY  
A KOMUNIKAČNÍCH TECHNOLOGIÍ

## DEPARTMENT OF MICROELECTRONICS

ÚSTAV MIKROELEKTRONIKY

## STEP-UP SWITCHED POWER SOURCE

ZVYŠUJÍCÍ MĚNIČ NAPĚTÍ

### MASTER'S THESIS

DIPLOMOVÁ PRÁCE

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BRNO 2016

# Diplomová práce

magisterský navazující studijní obor **Mikroelektronika**

Ústav mikroelektroniky

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**ID:** 147009

**Ročník:** 2

**Akademický rok:** 2015/16

**NÁZEV TÉMATU:**

## Zvyšující měnič napětí

**POKyny PRO VYPRACOVÁNÍ:**

Navrhněte a realizujte zvyšující měnič napětí s galvanickým oddělením. Měnič by měl pracovat v rozsahu napětí 40-80V na vstupu s nastavitelným výstupem až 1000V s přenášeným výkonem 20VA.

**DOPORUČENÁ LITERATURA:**

According to recommendations of supervisor

**Termín zadání:** 8.2.2016

**Termín odevzdání:** 26.5.2016

**Vedoucí práce:** Ing. Michal Pavlík, Ph.D.

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## **Abstract**

This work focuses on describing different voltage regulators with a specific focus on the isolated topologies. Then there is a discussion about the best choice for anodic bonding, which means high voltage, low current requirements.

Next part explores difficulties faced when designing such a converter and what and how needs to be taken care of.

Afterwards, there is the own design of the regulator with described steps of optimization, followed by the simulation results. Two different approaches are compared and the best solution is then selected. Way of making the output bipolar is shown.

Final parts focuses on the hardware implementation of such a design and measurement of its performance.

## **Keywords**

Anodic bonding, switch mode power supply, flyback regulator, snubber

ŽAMBERSKÝ, J. Zvyšující měnič napětí. Brno: Vysoké učení technické v Brně, Fakulta elektrotechniky a komunikačních technologií, 2016. 80 s. Vedoucí diplomové práce Ing. Michal Pavlík, Ph.D..

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V Brně dne

I would like to thank my supervisor Ing. Michal Pavlík, Ph.D., who despite his much more important task at that moment was always able to point me the right direction, when I went astray. And in the first place for making this work even possible.



Výzkum popsáný v této diplomové práci byl realizován v laboratořích podpořených z projektu SIX; registrační číslo CZ.1.05/2.1.00/03.0072, operační program Výzkum a vývoj pro inovace.



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pro inovace**

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# 1 INTRODUCTION

Anodic bonding, also referred to as a field assisted glass-silicon sealing or electrostatic sealing is a process of connecting a glass and a silicon wafer under the influence of increased temperature and an external electric field. Typical temperature is around 500°C and the applied voltage ranges from 50 to 1 000 V.

With both surfaces clean and maximal roughness of around 0.1  $\mu\text{m}$ , the glass and silicon are placed on top of each other and voltage is applied in such a way that the silicon wafer is connected to the positive terminal, glass to the negative. Kind of a capacitor with a glass as dielectric is formed. The exact mechanism is unknown, but due to the electromigration of sodium ions in the glass to the interface with a silicon and formation of a bond between these two elements, basically irreversible bond is created. [9]

The speed of the process can be controlled with both the temperature and the applied voltage. The usual time ranges from minutes up over quarter of an hour.

The subject of this thesis is design such a power source, which can provide the variable output voltage, so the speed of the process can be controlled as was mentioned above as well as compensate for different glass thickness.

## 2 POWER REGULATOR TOPOLOGIES

There is a big spectrum of voltage sources utilizing various methods to provide the regulated output voltage. Following chapter will give a quick overview.

### 2.1 Linear regulator

The most simple implementation of voltage regulator is using linear regulator. Function of this circuit, simplified in figure 2.2, is based on variable resistor adjusted in order to have a voltage drop just enough for the remaining voltage to be of a right value.

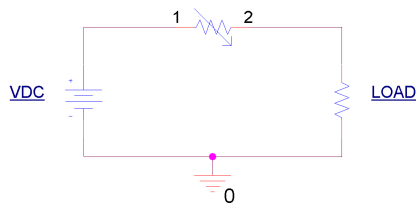


Fig. 2.1: Simplified schematic of linear regulator

Apart from the simplicity, advantage of this approach is basically no output ripple, no EMI, regulator mostly consists of just one integrated circuit and two bypass capacitors, giving a small PCB footprint.

However, there is a toll of poor efficiency when there is a big voltage drop across the regulator. Big portion of the energy supplied by the power source is transformed into a Joule heat instead of being delivered to a load. Another drawback is the circuit's inability to provide higher voltage than the one of a power source.

### 2.2 Switched power supplies

As opposed to the linear regulator, there is a family of switched power supplies. As the name suggests, they operate with a switch alternating between on- and off-state. With some additional components, mostly capacitors, inductors and diodes, it is possible to obtain a regulated DC voltage. Based on the arrangement of the circuitry around the switch, the output can be either lower, higher or both. Output voltage is mostly controlled by duty cycle of the switch.

Common property of switched power supplies is higher efficiency throughout various input and output voltages (ideally no voltage drop on the switch, purely complex inductance and capacitance). If using transformer, switched power supplies can be galvanically isolated. On the other hand, without an ideal output filtering, there will always be a voltage ripple and the switch generates some EMI. The circuits are generally more complex.

Divided based on galvanic isolation, the most basic topologies for non-isolated are:

- Buck (step-down)
- Boost (step-up)
- Buck-boost

Buck converter has output voltage lower than input, boost converter higher. Buck-boost converter combines two previously mentioned, hence the output can be both lower or higher.

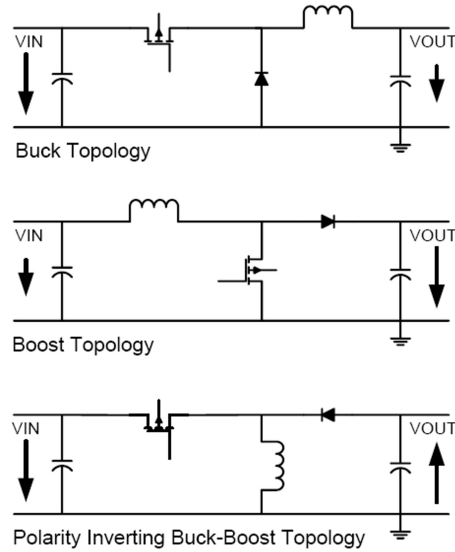


Fig. 2.2: Different non-isolated switching supply topologies [1]

The isolated converters can be further divided based on whether the transformer magnetization B-H curve goes in only one quadrant, called asymmetrical, or if magnetization curve goes through multiple quadrants. These are called symmetrical.

Most well known asymmetrical isolated converters are

- Flyback, shown in figure 2.3a
- Forward, figure 2.3b

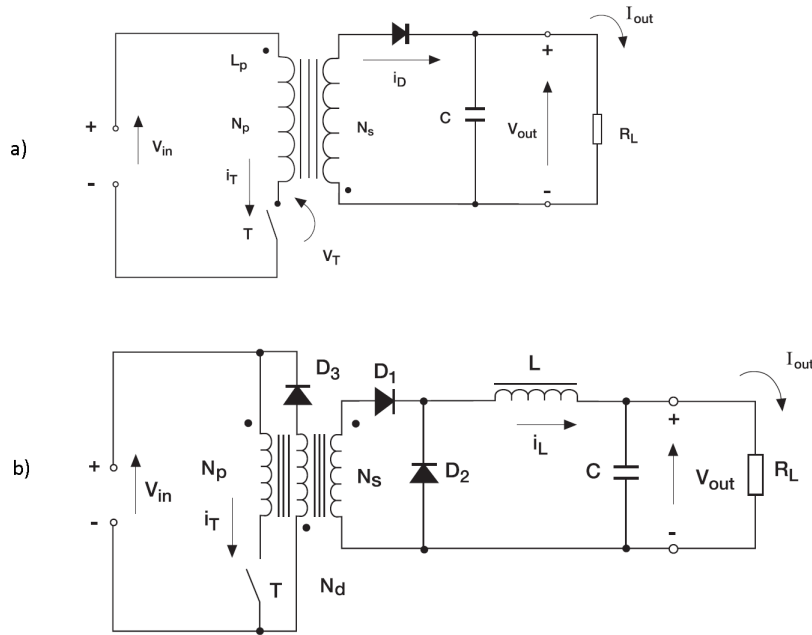


Fig. 2.3: Asymmetrical isolated converters, a) flyback, b) forward [17]

Symmetrical topologies on the other hand are

- Push-pull, shown in figure 2.4a
- Half bridge, figure 2.4b
- Full bridge, figure 2.4c

### 2.2.1 Flyback regulator

The biggest advantage of this regulator is its simplicity. The regulator features only one switch which is grounded and doesn't need additional inductor. The maximal output power of this type of regulator around 150 W. It's well suited for high output voltage, but not a good choice for high output current. [16]

### 2.2.2 Forward regulator

Even though the forward regulator looks similar to flyback, its function is fundamentally different. Compared to flyback, the forward regulator doesn't use the transformer as an energy storage, but just transforms the primary current into the secondary winding, where for the switch off-state, the current is supplied through inductor and the freewheeling diode.

This difference in function also defines its parameters. Because the output current is non-pulsating, it's more suitable for high output current applications. There is a need for third, reset winding in the transformer, also the regulator consists of greater number of components. On the other hand, there are no current spikes as in flyback regulator, so as was mentioned, the topology is well suited for high output currents. [16]

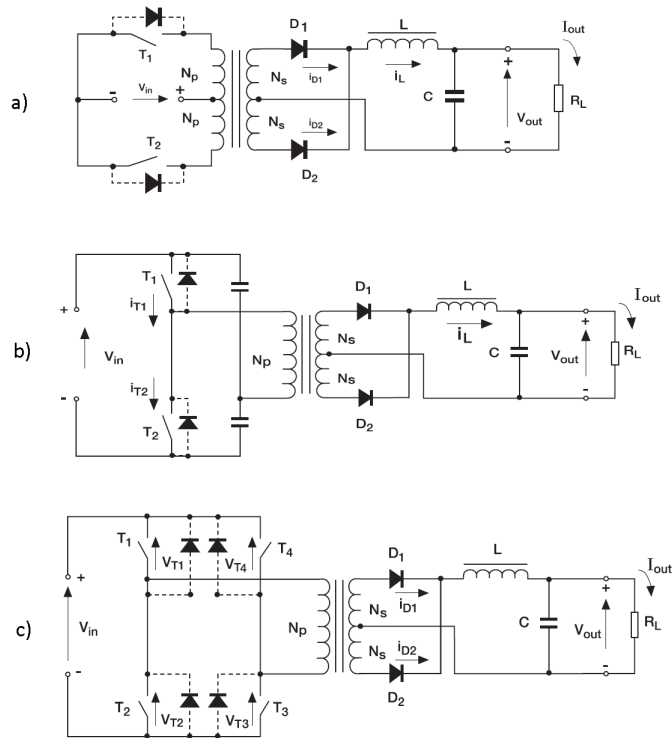


Fig. 2.4: Symmetrical power regulators, a) push-pull, b) half bridge c) full bridge [17]

### 2.2.3 Push-pull, half and full bridge regulators

All of these regulators are somewhat based on forward regulator. Due to higher complexity of transformer and its driving, they are capable of providing higher output power. Thanks to an alternated switching of the primary winding, the output filter for the same power can be smaller.

Common disadvantage of these topologies is both higher circuit and transformer complexity and more caution must be taken while driving the switches. [16]



## 3 DESIGN CONSIDERATION

In this chapter, the topology selection will be justified, followed by some of the most problematic parts of the selected design, especially focusing on the issues related to the high output voltage.

### 3.1 Topology selection

To pick up the right topology to fulfill the given requirements, the pros and cons for each has to be considered. Some of them can be crossed out right away pretty easily due to the fact that the power source has to be capable of both increasing and reducing the input voltage. Apart from a theoretical concept of transforming the input voltage to over 1 kV and then reducing, which would place high demand on breakdown voltage of the switching element, only isolated power sources and a buck-boost converter remain in the selection.

Another simple elimination is of the buck-boost converter. The output has to be bipolar, however the regulator is only unipolar and since it's not isolated, everything would have to be doubled and switching between polarities would mean switching the regulator connected to output.

All of the isolated converters however can fulfill the task given, and to choose the best one, also the output voltage and power has to be taken into account.

With respect to the required power supply parameters, which are rather low output power, all of the push-pull, half and full bridge make no sense to choose, since they are just variations of forward regulator designed to provide higher output power. There would be no merit, however the circuitry would be more complex.

Two reasonable options are flyback and forward regulator. The design is closer to the high voltage-low current, since the priority is for it to work well in the high-voltage region, where the currents are low, not vice versa. Another advantage of the flyback topology is that since there is no need to charge external inductance, faster transient response is achievable. Based on this, the best topology choice would be the flyback regulator.

### 3.2 Flyback regulator

In this section, the flyback regulator principle will be just briefly explained.

The circuit is switching between on-state and off-state, displayed in figure 3.1. When the switch is on, the input voltage is forced across the transformer primary which causes an increasing flow of current through it.

Note that the polarity of the voltage on the primary is dot-negative (more negative at the dotted end), causing a voltage with the same polarity to appear at the transformer

secondary (the magnitude of the secondary voltage is set by the transformer secondary-to-primary turns ratio).

The dot-negative voltage appearing across the secondary winding turns off the diode, preventing current flow in the secondary winding during the switch on time. During this time, the load current must be supplied by the output capacitor alone.

When the switch turns off, the decreasing current flow in the primary causes the voltage at the dot end to swing positive. At the same time, the primary voltage is reflected to the secondary with the same polarity. The dot-positive voltage occurring across the secondary winding turns on the diode, allowing current to flow into both the load and the output capacitor. The output capacitor charge lost to the load during the switch on time is replenished during the switch off time.

Flyback converters operate in either continuous conduction mode (CCM), when the secondary current is always greater than zero, or discontinuous mode (DCM), if the secondary current falls to zero on each cycle. [14]

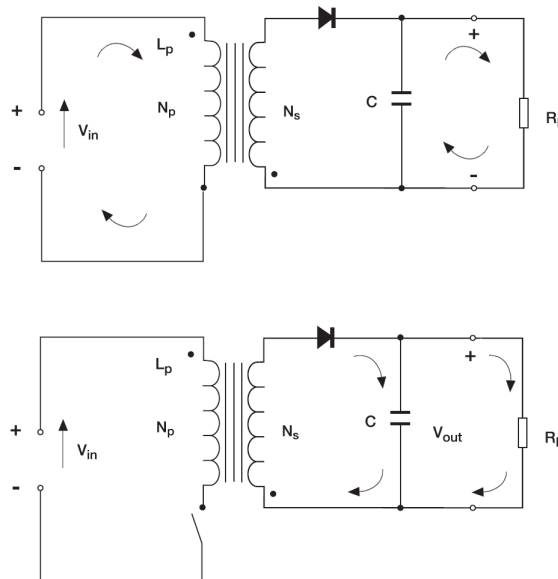


Fig. 3.1: On- and off-state currents in flyback regulator [14]

Typical waveforms of a flyback regulator working in a continuous mode are shown in figure 3.2.

Working in each mode has some advantages and drawbacks. Advantages of CCM are:

- Transistor and diode peak current requirements are approximately half compared to DCM of the same output
- Easier cross-regulation for multiple outputs
- Lower primary and secondary RMS current

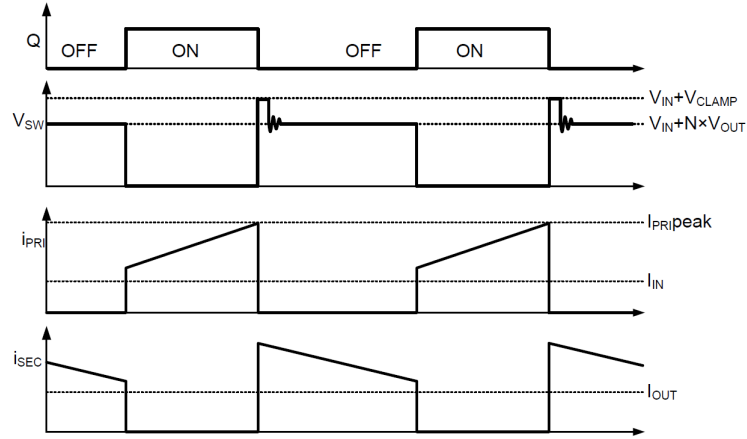


Fig. 3.2: Waveforms for continuous mode [2]

- Output capacitor ESR is not that critical [7] [10]

Advantages of DCM are:

- Smaller transformer can be used because the stored energy is lower
- Stability is easier to achieve
- Output rectifier operates at zero current prior to getting reverse biased, hence reverse recovery is not critical
- Faster transient response
- Transistor turns on at zero current, so turn on time is not critical
- Transistor turn-on to zero current results in low EMI [7] [10]

Because the DCM mode may allow a smaller transformer as well as provide a fast transient response and lower turn-on losses, it is usually the best choice for lower power or a Flyback with a high output voltage and low output current requirement.[10]

The regulator should be designed to operate in only one of these modes for best performance. Working in both modes is also possible, but such a converter must meet more strict feedback regulation requirements compared to one working only in DCM because of more complex transfer function.

### 3.3 Snubbing

In figure 3.2 can be seen, that during on-off transition, a voltage spike on the switch can be seen. This is a result of the parasitic properties of the components in real circuit, namely a leakage inductance of the transformer given by non-optimal coupling between primary and secondary winding.

When the transistor is turned off, the energy stored in the uncoupled inductance causes a voltage spike on the switch to rise. The excessive voltage on the drain pin may lead to an avalanche breakdown and eventually damage the MOSFET. Therefore, it is

necessary to add an extra circuit to clamp the voltage within the  $V_{DSmax}$ . [3]

The RCD snubber circuit is used to protect the switch, as shown in fig. 3.3. It absorbs the current in the leakage inductor by turning on the snubber diode when  $V_{ds}$  exceeds  $V_{in+nV_o}$  and the current flows into the  $C_{sn}$ . The energy stored in the capacitor is then discharged through the  $R_{sn}$  resistor.

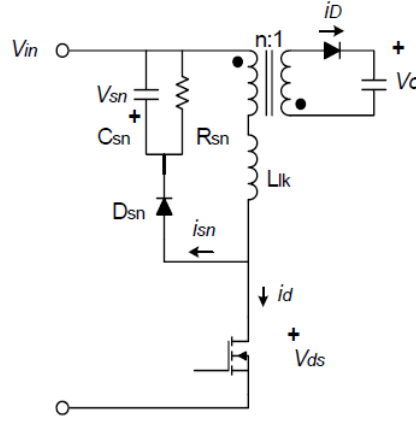


Fig. 3.3: DRC snubbing circuit [3]

### 3.4 Two switch flyback

Another approach to solving the leakage induced spikes is changing the topology using two switches in the primary side, as shown in figure 3.4. With the switches being driven in phase, the primary winding is either connected to the input voltage, or through the reverse polarized diodes to the input voltage. When switching to off-state, the energy of the spike is driven through the demagnetization diodes back to the input power supply, recovering the energy. This modification allows us to work at higher switching frequencies and with a better efficiency than the one of a single switch structure. However, the two switch structure requires driving a high side switch. This double switch flyback is also known as asymmetrical half bridge flyback. [16]

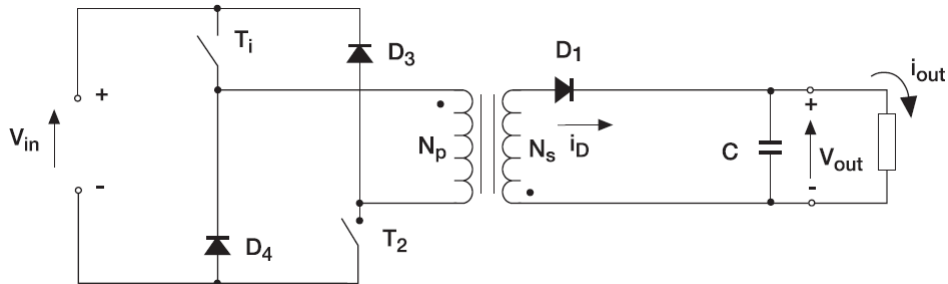


Fig. 3.4: Two switch flyback regulator [16]

### 3.5 Voltage stress

As the current is switched on and off, voltage over the transistor and the rectifying diode changes depending on the phase in which the regulator is. Following chapter will analyze voltage appearing on the transformer, which together with the input/output voltage defines the semiconductor elements voltage stress.

Simple simulation model shown in figure 3.5 will serve as a reference circuit to demonstrate all the occurring effects. Component values were chosen to work in stable DCM. In figure 3.6, the corresponding waveform for a close-to-full voltage state is shown. Note, that the transformer ratio  $n_{prim}/n_{sec} = 1$ . Also the two windings are ideally coupled, so no over-voltage spikes are observed.

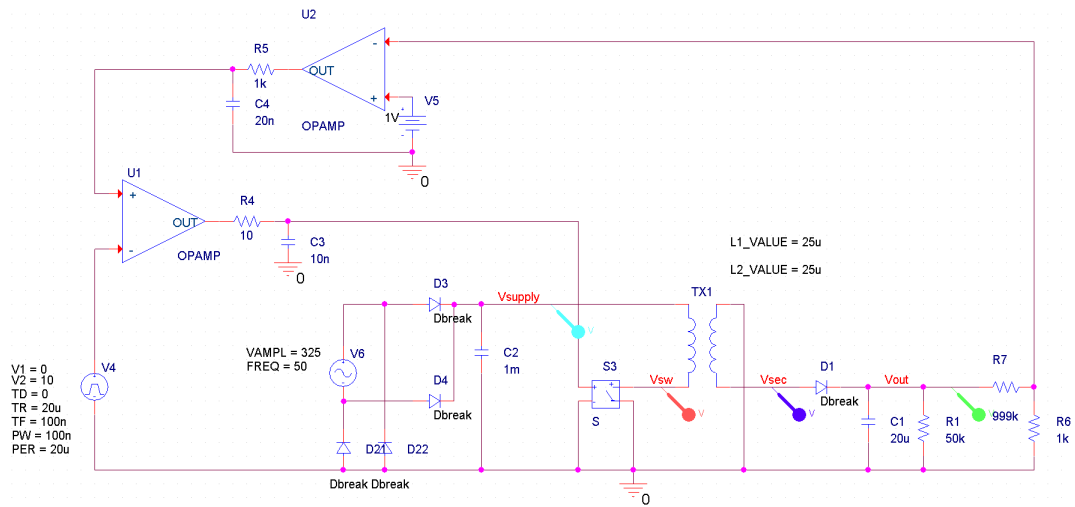


Fig. 3.5: One-switch flyback simulation model

Three phases can be seen, phase of charging the inductor from the input voltage (3.5 to 3.51 ms), phase of charging the output capacitor with energy stored and the third phase (3.51 to 3.513 ms), when the inductor is discharged with no current flow through it (3.513 to 3.520 ms).

In the first phase, as the switch is closed, the input voltage is reflected to the secondary side with the opposite polarity, multiplied by the transformer ratio, in this case equaling one. During this phase, the reverse voltage on the diode is the greatest and given by equation 3.7.

$$v_{diode} = v_{out} + n \cdot v_{in} \quad (3.7)$$

In the second phase, the diode is forward polarized, however the output voltage reflect itself to the primary winding, causing additional voltage stress to the switch. During this phase, the voltage stress of the switch is maximal and given by equation 3.8.

$$v_{switch} = v_{in} + \frac{1}{n} \cdot v_{out} \quad (3.8)$$

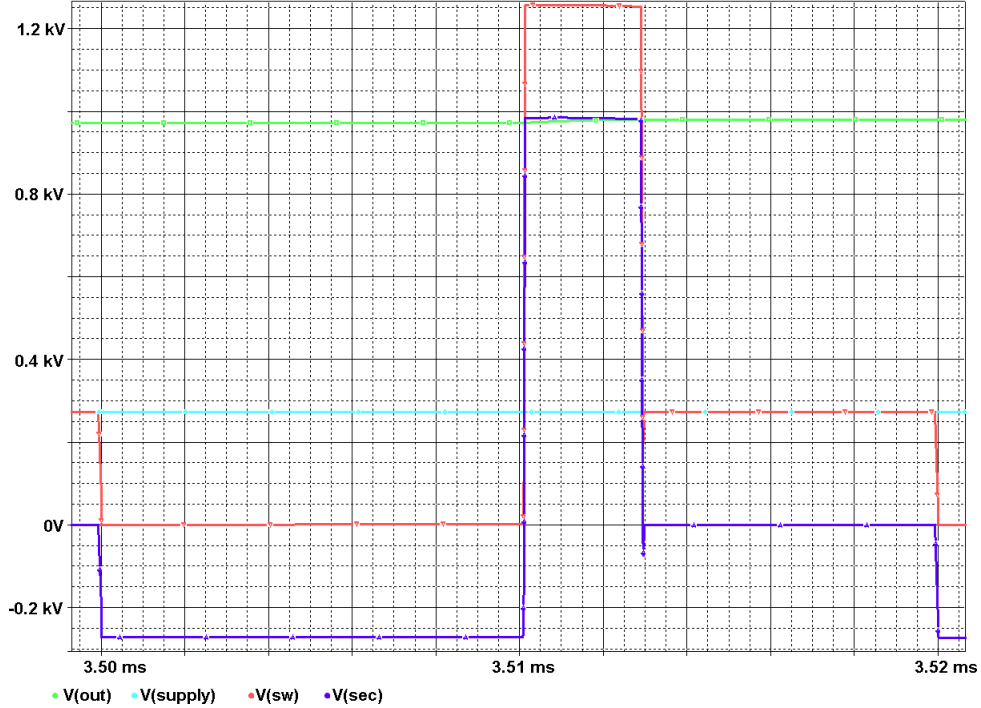


Fig. 3.6: Signal waveforms of one switch simulation. Cyan: supply voltage, green: output voltage, red: voltage on switch, blue: voltage on secondary

The third phase is somewhat the most component friendly one as no additional voltage applies to them.

Thing that needs to be considered when designing the two switch flyback regulator is the secondary voltage reflected to primary. As soon as the output voltage reaches the value of the input, the energy in the inductor is discharged through the diodes back to the input bypass capacitor instead of being transformed to the secondary side. For  $v_{out} > v_{in}$ , the transformer ratio has to be greater than one. This behavior was also proven in simulation, with the primary switching side connected as shown in fig. 3.10 with the rest of the circuit identical to the one in fig. 3.5. Corresponding waveform as soon as the output voltage reaches the input is shown in fig. 3.11. Majority of the energy accumulated in the inductor is transferred back through the diodes with only a small portion being transferred to the secondary side. For a two switch topology, the equation 3.9 must be valid.

$$v_{out} < v_{in} \cdot n \quad (3.9)$$

For non-ideally coupled transformer in a single switch topology without a snubber, additional voltage spike is defined only by the leakage inductance and the parasitic capacitances. With a snubbing circuit, it's a good safety assumption to give additional 30% breakdown voltage reserve for the switching element. [10].

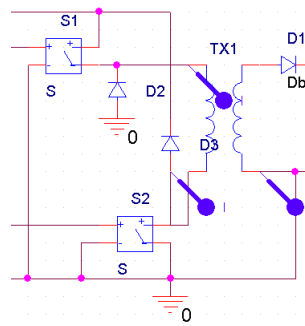


Fig. 3.10: Two-switch flyback simulation circuit

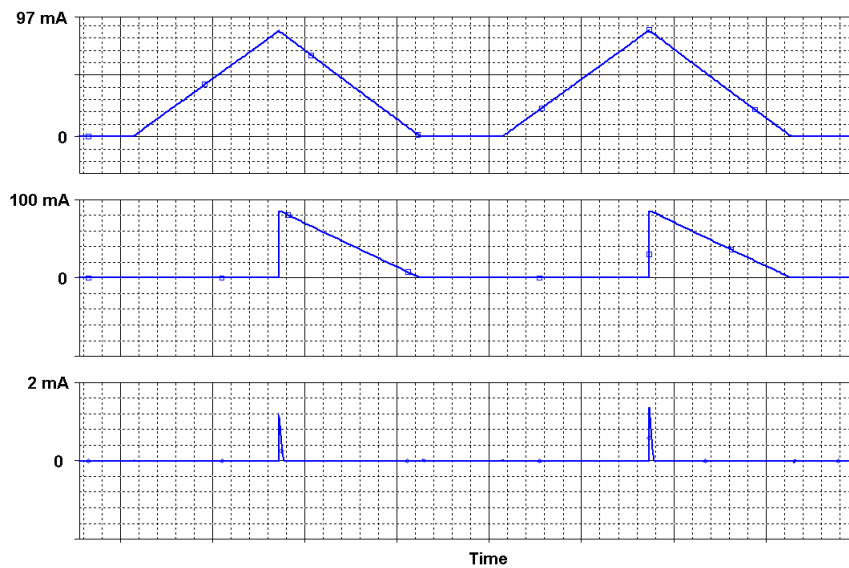


Fig. 3.11: Waveform of signals in two switch flyback when  $v_{in} = v_{out}$ . Top: inductor primary current, middle: diode current, bottom: inductor secondary

### 3.6 Transformer ratio

One of the most crucial decision that needs to be made is designing the transformer in order to fit below the breakdown voltage of semiconductor components. As shown by equations 3.7 and 3.8, both the diode and transistor maximal voltage is directly influenced by the transformer ratio. With output voltage 1 kV, if the design was to be supplied via e.g. 230 VAC mains, then the voltage over these components for various transformer ratio can be printed. It can be seen in fig. 3.12 that these voltages are pretty high for basic semiconductor components and there is rather narrow window, if any, where designing the reugulator would be feasible without using some special high voltage components (keep in mind that the leakage inductance spike is neglected). Taking into account the condition given by equation 3.9 for two switch topology, the options are even more limited.

The obvious solution for reducing the voltage stress on the components is reducing the input voltage, which plays role of a slope of  $V_{diode}$  curve and shift of the hyperbolic

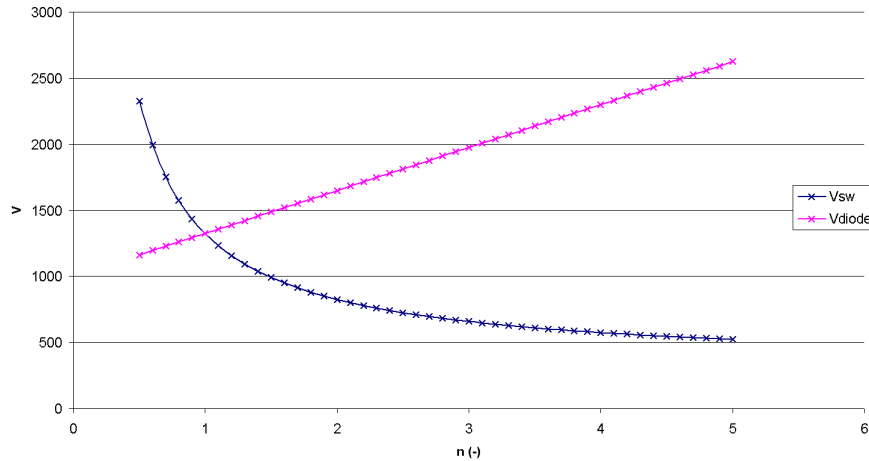


Fig. 3.12: Voltage over a diode and a switch on transformer ratio dependency

$V_{sw}$  curve. The plot 3.13 shows two different situation, one previously shown for 230 VAC (325  $V_P$ ) and 100 V.

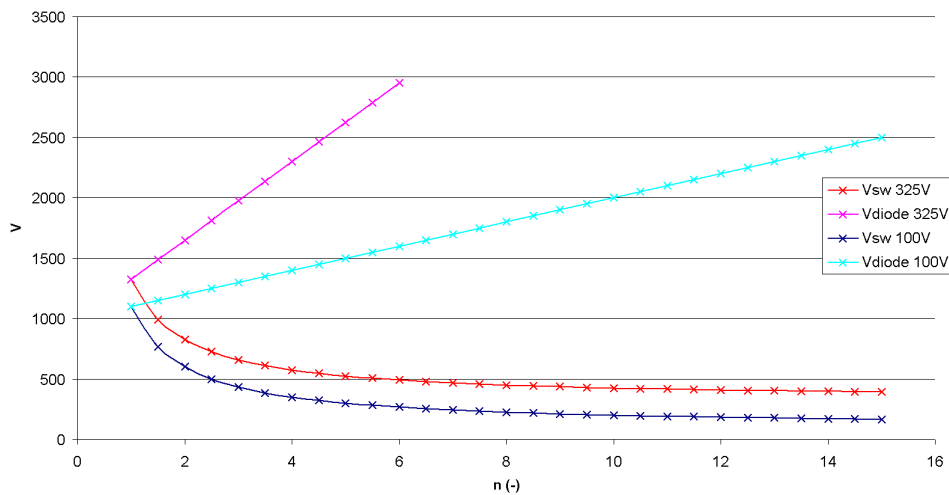


Fig. 3.13: Dependency of a diode and switch voltage on transformer ratio for different  $v_{in}$

In the setting with lower  $v_{in}$ , it's much easier to find a suitable operating point, where for example around the transformer ratio  $n = 4$ , maximal voltage over both semiconductor component is within reasonable boundaries. For two switch topology, the transformer ratio has to be correspondingly higher, giving greater stress on the diode, whereas the switching transistor can be anything for voltage over around  $250 V_{DSmax}$  with good enough current capability. For the input voltage of 24 V, as this design is to be, the situation is even better.



### 3.7 Transformer core

Transformer cores are made of ferromagnetic materials. Common unfortunate property of these materials is their B-H non-linearity, based on domain structure of such material. Every material has its typical magnetization curve, but all of them resembles the one in fig 3.14. When all domains in material are turned in the direction corresponding with the external field, no additional flux can be provided by the material. This state is called saturation. Since a permeability  $\mu$  is related to the slope of a B-H curve, and inductance is directly proportional to the permeability, behavior of an inductor with ferromagnetic core can be determined. If the hysteresis is omitted, the inductance of an inductor with a ferromagnetic core increases at first, reaching region with maximal inductance, and slowly approaches zero as a saturation takes place.

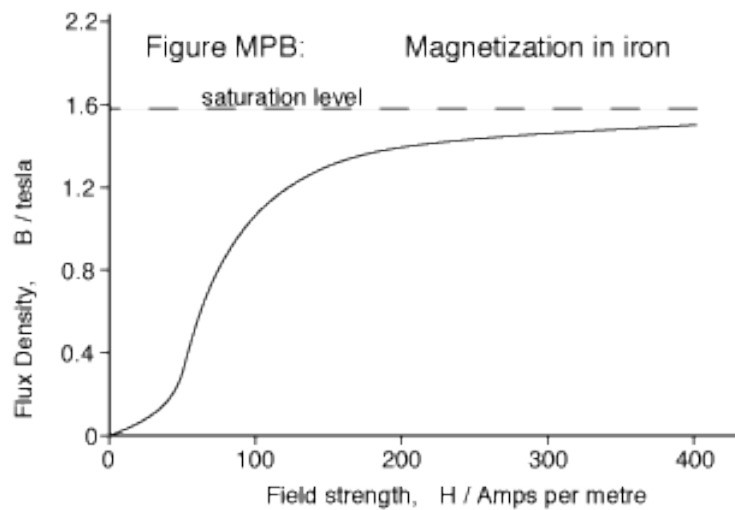


Fig. 3.14: B-H curve for ferromagnetic material [15]

From the equation 3.15 describing an inductor, if  $L \rightarrow 0$ , the  $di/dt \rightarrow inf$ , limited only by the series resistance of the inductor. So the drawback of using the ferromagnetic core is the risk of reaching the saturation, which would result in rapid increase of current, therefore probably destroying the switching device.

$$v = L \cdot \frac{di}{dt} \tag{3.15}$$

Solution to both the non-linearity and the saturation is using a gapped core, meaning the core is not "full circle", but a small section is replaced either by air or some saturation-resistant material. This way, total reluctance of the circuit is given by a series combination of the ferrite core and the air gap. Permeability of ferrites is in order of thousands (meaning reluctance really small), so its obvious that the total reluctance is given by the reluctance of the air gap, which is linear and can't reach saturation. The whole inductor with a gapped core of course can still reach saturation when the magnetizing current is big enough to put the ferromagnetic material in the saturation region. But due to the slope

of the B-H curve being much smaller, this corresponds with much higher current and can be controlled by the gap length. Difference between B-H curves of an ungapped and gapped core is displayed in figure 3.16

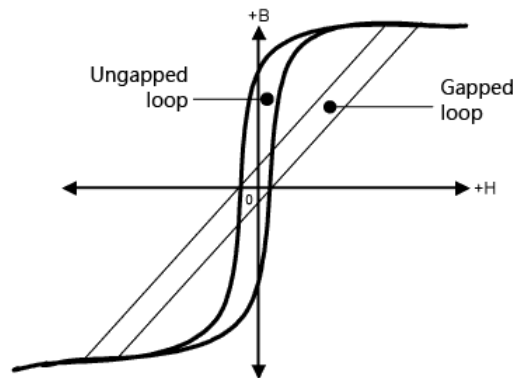


Fig. 3.16: B-H curve for gapped and ungapped core [4]

The transformer in the flyback regulator is working as a coupled choke, thus capability to store an energy is important. With the reduced inductance by the air gap, inductor can be subjected to a much larger current before reaching saturation. Energy in the inductor is proportional to current squared (eg. 3.17), logical outcome then is that gapped inductor can store much more energy, because of that higher current.

$$E = \frac{1}{2}LI^2 \quad (3.17)$$

Obvious downside is that the permeability of the core is reduced, so more turns in the winding are required for the same inductance. Another one is that the air gap increases the leakage inductance, leading to larger voltage spikes on switching. Leakage inductance is lowest with the winding placed over the air gap.

## 4 REGULATOR DESIGN

Two regulators, a single switch topology and also one with two switches will be designed. The first few steps are however the same for both of them. Some parameters have to be decided prior to the own design.

### 4.1 Switching frequency

The switching frequency is always a compromise. Using higher frequency results in smaller output filter components, smaller inductor, provides better load transient response. The tradeoff is in higher switching losses and higher EMI. The usual range is between 50 and 100 kHz, but latest trend is using higher frequencies, reaching order of MHz. As EMI is not much of a concern given the PSU is not to be placed in a direct proximity of any sensitive devices, whereas reducing the output filter components is favorable due to the high voltage value it needs to be designed to, the design is aiming towards higher frequencies, where 100 kHz seems to be a reasonable value.

### 4.2 Output capacitor

As soon as the switching frequency is given, the value of the output capacitor can be calculated. Even though the maximal output power of the power source is given as 20 VA, it is clear from the application that there is no risk of the current increasing while reducing output voltage. The maximal output current is then given by equation 4.1.

$$i_{max} = \frac{P_{outMax}}{V_{outMax}} = \frac{20 VA}{1000 V} = 20 mA \quad (4.1)$$

Apart from maximal current, the capacitor value is related to the ripple voltage and switching frequency. These values are related by equation 4.2, which is derived from the fundamental equation describing capacity.

$$C_{min} = \frac{i_{max}}{f_{sw} V_{ripple}} = \frac{20 mA}{100 kHz \cdot 1 V} = 200 nF \quad (4.2)$$

Of course a good design rule is to use a higher value, but considering the slew rate is also an issue, the margin shouldn't be too big.

### 4.3 Transformer inductance

Now this is where it gets a bit tricky. Two equations the optimization process is based on are the fundamental inductance equation 4.3 and the previously mentioned equation describing energy stored in the inductor 3.17.

$$v = L \frac{di}{dt} \quad (4.3)$$

While neglecting all the parasitic properties of the inductor the energy transferred over time is linearly dependent on the inductance of the transformer and a square of a current. The current flowing in the primary side of the transformer by the end of the on-phase is also a function of the inductance, inverse proportional. This means that the product of  $L * i$  is constant, but with higher current and lower inductance, the energy stored in an inductor (energy, which is transferred to the secondary) is higher.

For the sake of a switching element, it's preferred to keep the current as low as possible, but there is a certain amount of energy which needs to be transferred to the secondary side, defined by the output capacitance, output voltage and the drawn current. Counting the exact value is not relevant at the moment. What is important is that increasing inductance reduces the energy transferred per time unit, but also reduces the current. Then there must be some limit inductance, which is "just good enough" to charge the output capacitor in time, but keeping the current as low as possible. Even though it should be possible to do the math on the paper, much easier way is to make a simple circuit model and with a parametric analysis numerically find the solution.

## 4.4 Single switch topology

The model used for simulation of a single switch topology is displayed in figure 4.7. At the first glance, the feedback might look a bit complicated. This is because of the additional voltage comparator on the primary side winding, blocking next charging cycle if there is still some current flow in the secondary. This way, the converter is forced to work in DCM. Except for the low-pass filter after the U2 opamp, all of the others are just to help the simulation converge and have no circuit function due to their very high cutoff frequency.

Maximal duty cycle is set to 0.8 for  $V_{out} = 1000 V$  and is linear function of the target output voltage. This reduces the ripple while working with lower output voltage. Load is represented with a current source taking the maximal possible output current. Transformer is parametrically defined by a primary inductance and a turn ratio. The coupling is set to 0.95, which, if some basic design rules are obeyed, is an achievable value. Snubber circuit is also parametrized by the RC time constant and a capacity. Compared to the capacity counted in eq. 4.2, the output capacitor is increased by the factor of 2.5 to 500 nF. For correct function of CCM blocking, saturation voltage of opamps is crucial. For these limits, refer the netlist in appendix.

The values shown in simulation model came from a parametric stepping based optimization with a target to get the required transient response while holding the switch current as low as possible, though slight margin was included, leaving some room for poorer performance of real components.

The output voltage transition is shown in figure 4.4, based on simulation with  $v_{targ}$  stepping for 50, 100, 300, 600 and 1000 V. Figures 4.6 and 4.5 show the maximal voltage and current spikes which can be found on the waveform. Keep in mind, that the two

waveforms don't have to be at the same time.

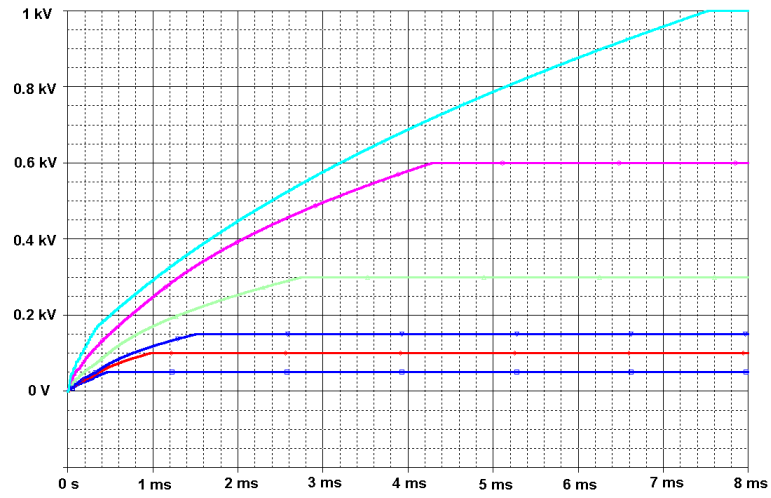


Fig. 4.4: Output voltage for target voltage set to 50, 100, 300, 600 and 1000 V

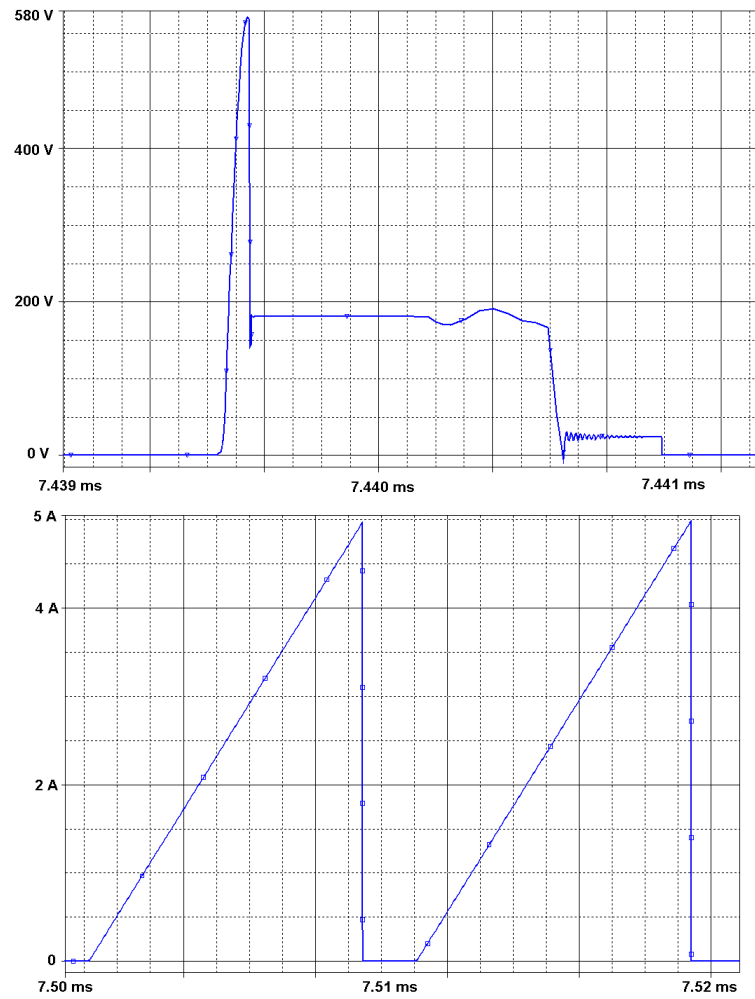


Fig. 4.5: Maximal switch voltage and current spike

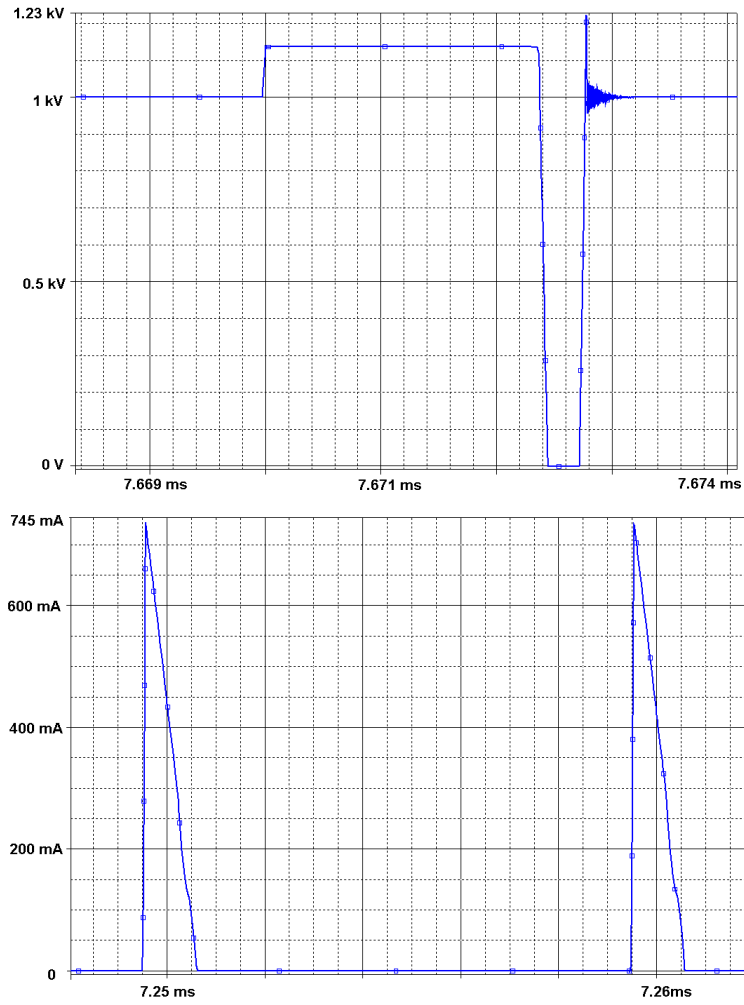


Fig. 4.6: Maximal diode voltage and current spikes

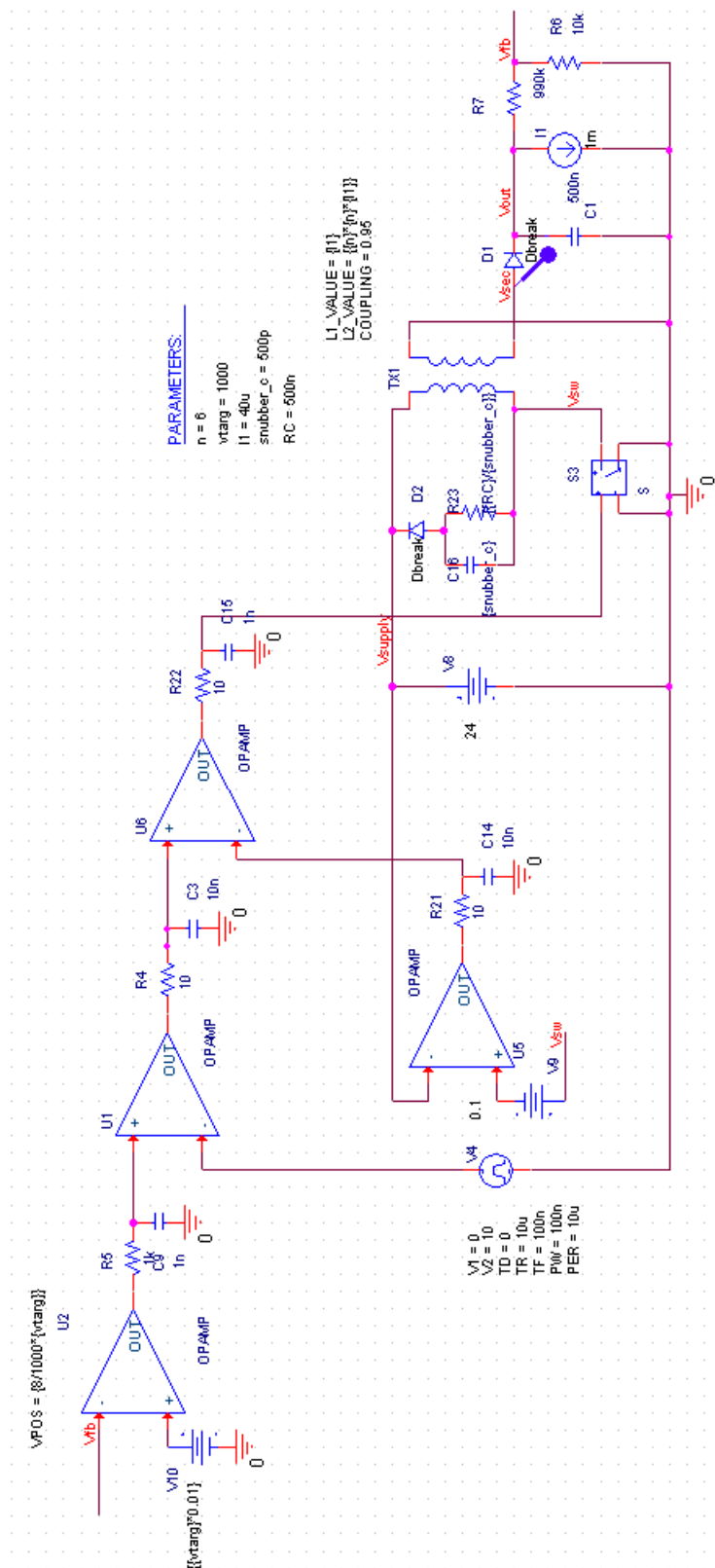


Fig. 4.7: Single switch model used for simulation

#### 4.4.1 Snubber circuit

Designing the inductor with a known capacitance is pretty straightforward and just a few iterations are sufficient to reach the goal. However when designing the snubber circuit, the application preference comes into play. The design can be either optimized for low voltage spikes with high Joule heat generated on the resistor, or with higher voltage spikes, though reducing the wasted energy. The goal was to manage the transistor spikes within 600 V range, where there is plenty of cheap models with good current rating.

For starters, it's a good empiric rule to set the RC constant to 1/10th of the switch on-time. [8]. For full load steady state, let's consider duty cycle 0.5, leading to the equation 4.8 for the time constant.

$$\tau_{snubber} = \frac{100 \text{ kHz}^{-1} \cdot 0.5}{10} = 500 \text{ ns} \quad (4.8)$$

The higher the capacity, the lower the voltage spikes. With the regard of keeping the goal of 600 V, capacity of 500 pF did the job. Then the snubber resistor is 1 k $\Omega$ . In maximal load steady state, the dissipated power is 2 W.

#### 4.4.2 Summary

With this topology, it was possible to achieve the desired parameters. The minimal voltage and current parameters for switching element and the diode are summed up in table 4.9.

Tab. 4.9: Minimal component parameters

Component	$V_{peak}$ (V)	$I_{peak}$ (A)
Diode	1.2k	0.75
Transistor	580	5

Even though some are higher than one would expect, both of them are not in any way extreme and basically can be bought off-the-shelf in any average shop. Trying to improve any of the following led to deterioration of some other parameter.

With more sophisticated DCM detection than the one used, faster charge time could be achieved due to eliminating some "dead time". This kind of feedback was chosen for the simulation purposes for its simplicity to reduce the runtime.

#### 4.5 Two switch topology

As was already mentioned, the minimal transformer ratio is limited by the discharge of the reflected voltage back to the input. In this case, around the  $n = 50$  is the limiting ratio, under which the maximal output voltage is unreachable. This high turn ratio together with already pretty high inductance would most likely be more problematic to make with a good coupling.



Multiple simulations were run to optimize the circuit. The best performing transformer ratio for this application proved to be around  $n = 60$ , the remaining parameters were obtained analogically to the single switch model. Both the final values and netlist can be found in appendix. In the following figures, the output voltage transition for different target voltage 4.10 and currents in the switching element and rectifying diode 4.11 are shown.

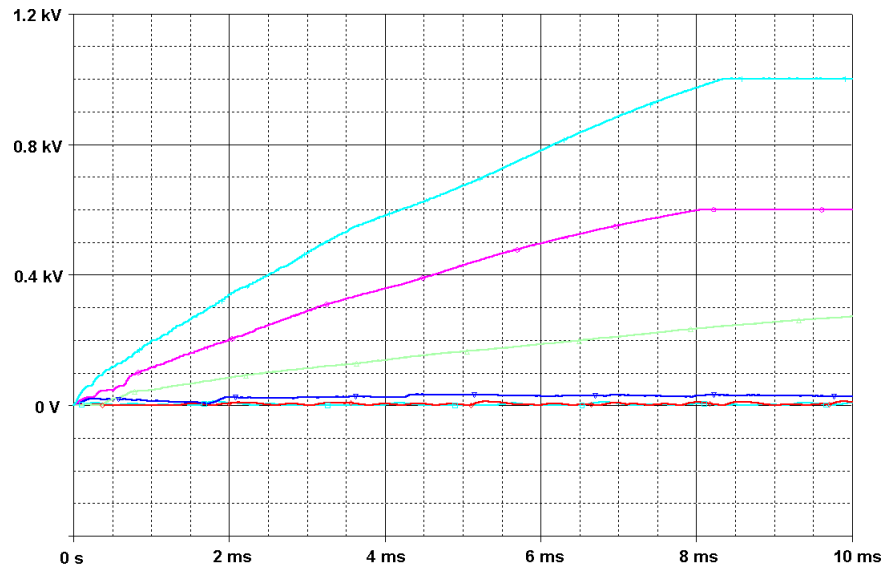


Fig. 4.10: Output voltage for target voltage set to 50, 100, 300, 600 and 1000 V, two switch topology

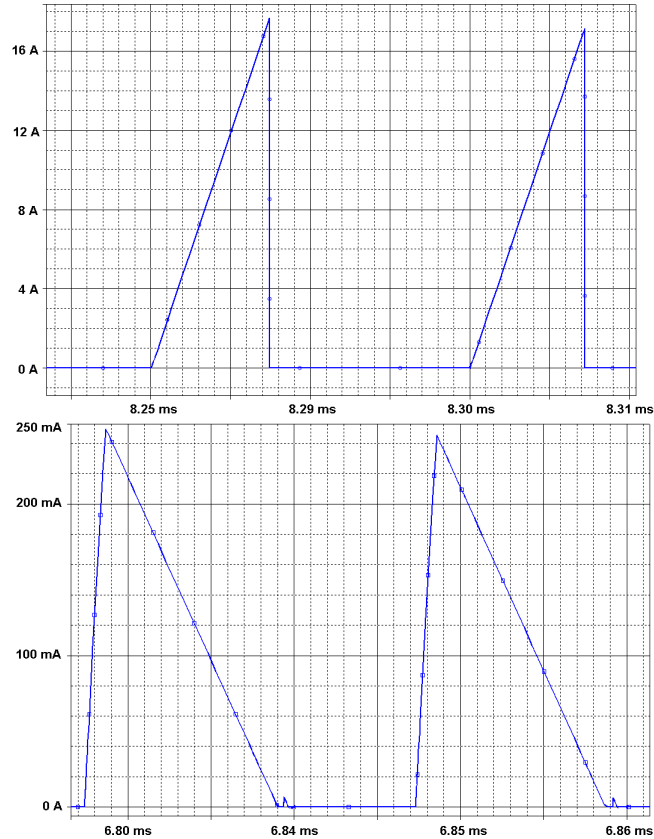


Fig. 4.11: Maximal switch and diode current, two switch topology

### 4.5.1 Summary

Even though the loss in the circuit was lower, around 400 mW in each demagnetizing diode, the overall performance suffers from worse output range and also the current spikes on the primary side are much higher. On the other hand, the voltage over the primary side switches can not exceed the  $V_{supply} + 2 \cdot v_{diode}$ , which is around 26 V.

## 4.6 Bipolarity

If the feedback is galvanically isolated, e.g. via linear optocoupler, the bipolarity of the power source can be easily achieved utilizing an H-bridge connecting the regulator to the output clamps. Two things needs to be considered:

1. High and low side switching, isolated from the control circuit
2. Current spike, caused by capacitance connected to the regulator

There are multiple solutions for driving the H-bridge. In any case, either two isolated power sources together with four isolated switches, or four isolated sources are needed. One approach would be using two DC-DC converters, which are all-in-one solution for providing the voltage together with optocouplers to control the gate driving.

Another, very simple solution is to use a pulse transformers. Since the transistors are always being driven in pairs, only two of them are needed, both with two secondary

windings. Using either just a capacity of the gate or charging parallel capacitor while having high resistance between gate and source, the pair of transistors would be closed if the pulse transformer was driven, otherwise the resistor would discharge the gate, opening the transistor. Schematic for one pair is shown in figure 4.12.

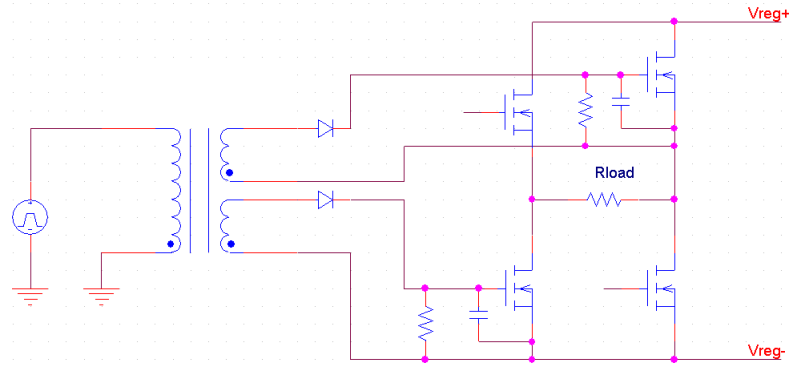


Fig. 4.12: H-bridge driving using pulse transformer

## 4.7 Simulation result summary

Some problematic steps while designing the switched regulators were discussed and were later applied to a simulated design. With the most suitable topology being a flyback regulator, two different models were tested. One of them more simple single switch topology, the second one more complex two switch flyback topology, which was theoretically promising better results.

After optimizing the circuit for minimal current load and fulfilling the requirement for 0 to 1 kV transition in 10 ms, the two circuits were compared. Even though the two switch converter exhibited lower losses, the overall current was higher, the regulation more difficult for a wide range output voltage and winding the transformer would be much more complicated because of its high transformer ratio as well as higher secondary inductance. On the other hand, the single switch topology was able to perform well over wider output voltage range with a rather simple regulation circuit. The only disadvantages were higher voltage on the transistor and higher losses. Though both of these were in an acceptable boundaries, the 2 W losses are of no big concern and transistor for 600 V is a common component.

Regarding the previously mentioned and also the fact that the single switch topology is a more simple circuit, especially thanks to no need for high side switching, the obvious choice for this application is a single switch topology flyback.

The bipolar output was also discussed with a suggested solution utilizing a pulse transformer driven H-bridge. This way there is no need for a stable voltage for high side and low side switching and all the control circuitry can be galvanically isolated from the output section.

## 5 HARDWARE IMPLEMENTATION

The simulations gave some idea of the basic elements, which had to be implemented into the design. Simplified regulator block diagram, omitting the auxiliary power sources, is in figure 5.1. The thick lines indicate power lines, thin lines signals, hollow line is a bus. The connections between separate blocks will be explained in the following sections, together with description of individual parts of the design.

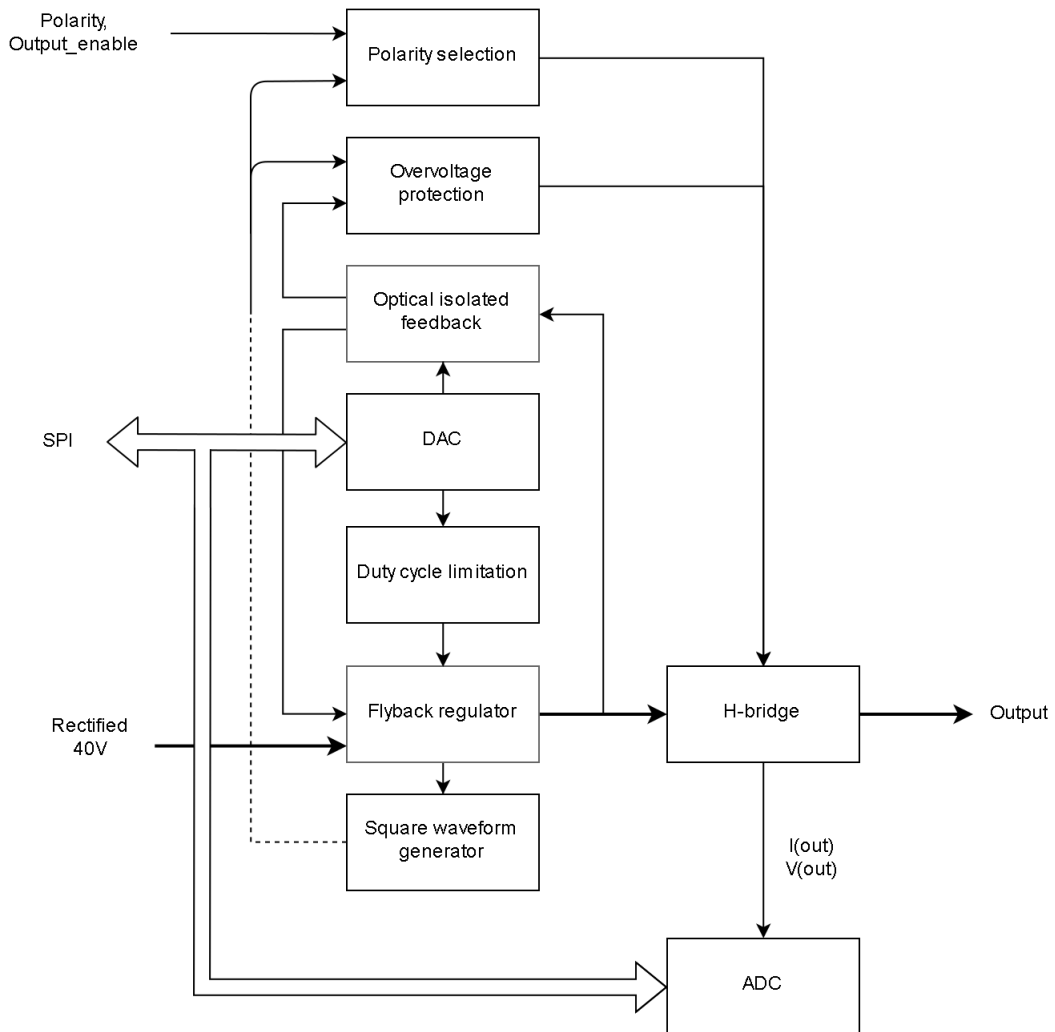


Fig. 5.1: Simplified block diagram

Note, that this chapter doesn't show full schematic, just mentions the important parts. For full schematic, refer to the appendix.

## 5.1 Flyback regulator

Flyback regulator consist of multiple components, each deserving deeper description.

### 5.1.1 PWM controller

Even though the design shown in simulation could be viable if made from individual components as simulated above, there are devices incorporating most of the features into a single device. One of those is UC184x family of PWM controllers from Texas instruments. Block diagram of such a device is shown in figure 5.2.

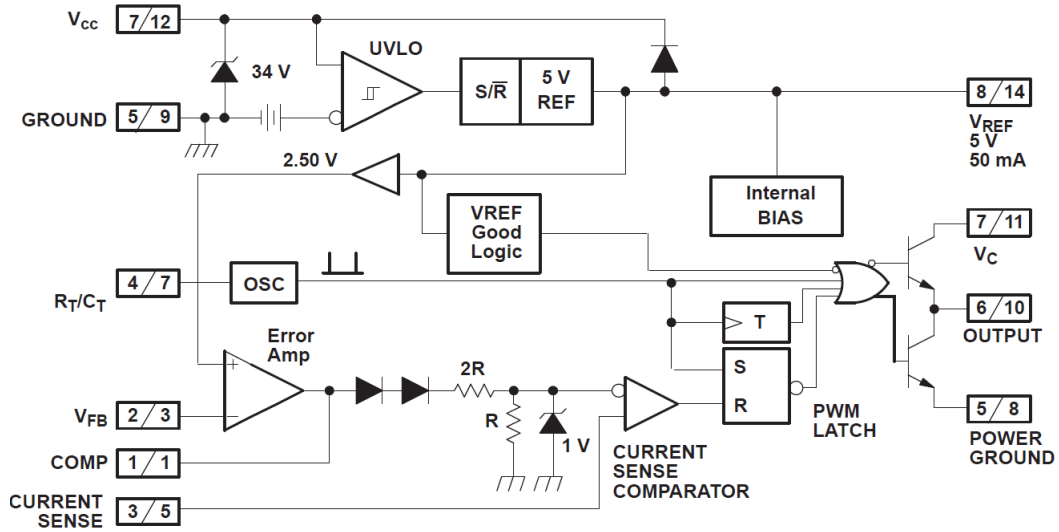


Fig. 5.2: Block diagram of UC182x family [12]

This device incorporates the chain of an error amplifier with 2.5 V threshold , current sense comparator with 1 V tripping value, oscillator adujstable with external RC circuit and a push-pull output driver. Additionally, there is a 5 V linear regulator providing 50 mA for extra circuitry, eliminating the need for additional components. Input voltage range from UVLO threshold to 30 V. For further details, refer to the datasheed in [12].

The model used for this application was UC2843, which has maximal duty cycle approaching 100% and UVLO of 8.4 and 7.6 V. Figure 5.5 shows the PWM controller with just the essential components. R35 and C11 are setting the oscillator frequency according to the equation 5.3.

$$f = \frac{1.72}{R \cdot C} \quad (5.3)$$

For the 100 kHz, the 8k2 resistor and 2.2n capacitor are values giving frequency close to 100 kHz, as shown in equation 5.4.

$$f = \frac{1.72}{8k2 \cdot 2.2n} = \frac{1.72}{1.804 \cdot 10^{-5}} = 95 \text{ kHz} \quad (5.4)$$

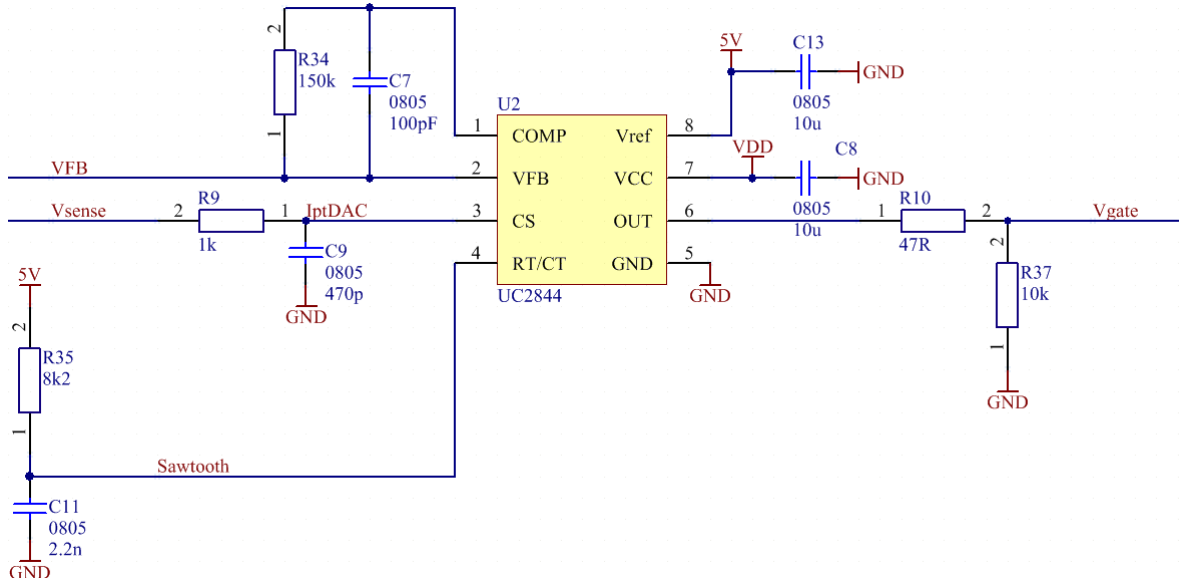


Fig. 5.5: UC2844 with typical circuitry

Compared to the simulated schematic, some supplementary circuits had to be modified in order to cooperate with this controller.

### 5.1.2 MOSFET

The switching transistor was selected as to have sufficient current and voltage capabilities, preferably in THT package to allow for heatsink mounting. Infineon IPP50R299 has  $V_{DSmax}$  550 V, continuous current 12 A and low on resistance on orders of hundreds of milliohms, promising low power dissipation. TO220 package is suitable for heatsink.

### 5.1.3 Rectification

Due to the higher input voltage in the final version (40 V AC), two rectifier diodes were connected in series to cover for slightly higher reverse voltage while still being in a SMT package and a "few bucks" device.

Diodes are 1 A, 1.3 kV fast diodes. The voltage stress was expected to be very close to the 1.3 kV. While fast diodes for higher voltage were unproportionally more expensive and the voltage stress is expected really close to one diode rating, simple connection of two diodes in series was chosen, with high resistor value divider for balancing.

### 5.1.4 Transformer

The transformer was wound on an RM12 core with 0.4 mm air gap, giving it inductance factor  $A_l$  400 nH. Since the supply current was increased, the inductance could

have been slightly increased to  $90 \mu H$ . Number of turns was calculated using equation 5.6.

$$n = \sqrt{\frac{L_{prim}}{A_L}} = \sqrt{\frac{90 \mu H}{400 nH}} = 15 \quad (5.6)$$

Fifteen primary side turns gives ninety turns on secondary side.

It is desirable to have as low leakage inductance as possible. Interleaving primary and secondary windings is an easy way to achieve it [5]. Interwinding capacitance increases, but that is not of a big concern in the design. The transformer was wound with a  $0.4mm$  copper wire, which allowed for 30 turns in one layer. Interleaving was done in a way that first layer was only secondary, second layer half primary half secondary, then one and half layer of secondary. This gave 15 turns of primary winding and 90 turns of secondary. Figure 5.7 shows the winding with red being the primary and blue secondary.

Isolation was made with Kapton tape with two layers between primary and secondary winding and one layer between third and fourth layer.

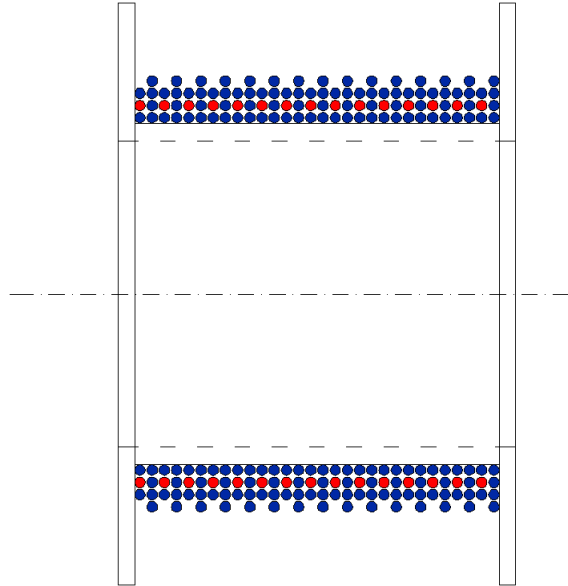


Fig. 5.7: Transformer winding

Schematic for the power section of the regulator is in figure 5.12. Voltage divider is composed of multiple resistors for both higher voltage capability and easier value trimming. Output capacitor is parallel combination of polypropylene capacitor with high capacity and a ceramic one for low ESR. Sensing resistor limits the current to 4 A.

## 5.2 Feedback

To make the circuit work with bipolar output, the secondary side has to be galvanically isolated. Some information of the output voltage has to be however transferred back

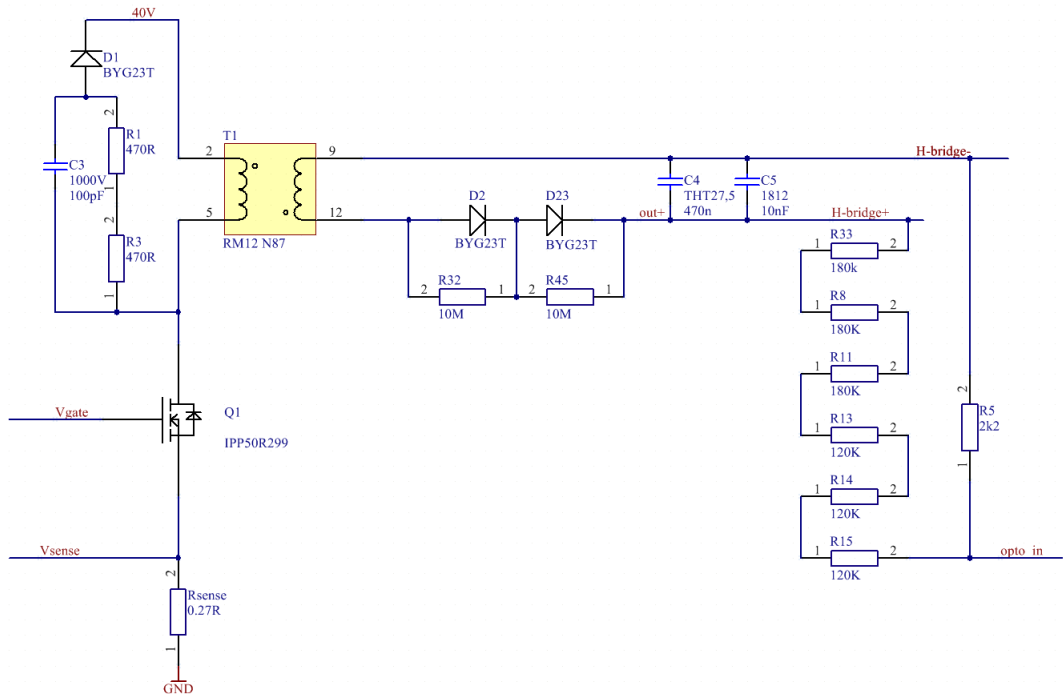


Fig. 5.8: Power section of primary side and secondary rectifier with capacitor

to close the control loop. There are different approaches, such as using TLV431 shunt regulator and an optocoupler [6]. In order to minimize to component count on the secondary side, linear optocoupler was considered as more suitable approach, since it has no DAC on the secondary side, greatly reducing the amount of isolated communication channels.

IL300 is a linear optocoupler using principle of two matched detectors and an emitter in a feedback loop with one detector. 5300 V isolation rating and 200 kHz bandwidth are both satisfactory by a large margin.

### 5.2.1 Output voltage settings

One fundamental difference is the fixed voltage on an error amplifier. The output voltage cannot be controlled via the value on its non-inverting input. Voltage shifting of the feedback voltage has to be used instead, which can actually be done pretty easily. Schematic diagram in figure 5.9 shows the feedback circuit.

emitting diode generates current in both detectors, which creates voltage drop over resistors R31 and R69 + R6. U6 amplifier controls the voltage to make it the same as the input voltage. Non-ideal coupling of the detectors has to be eliminated via R69 trimmer. Referencing the resistors on the secondary side to the DAC output instead of ground potential makes the desired voltage shift. PSU output voltage is then proportional to the supplement to 2.5 V. U4 amplifier is just a buffer. Both amplifiers should work with the bottom rail input. It's also important to keep in mind that the DAC has to have a



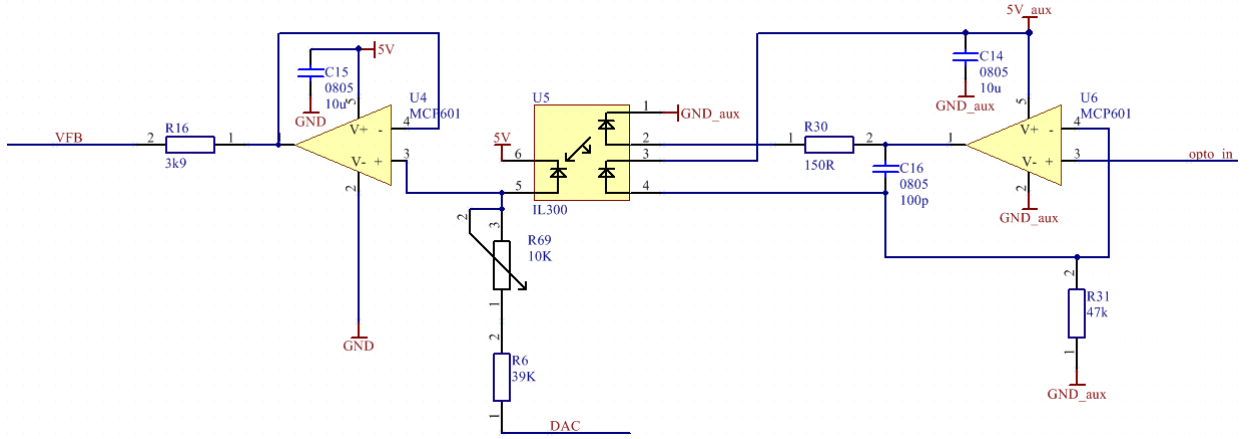


Fig. 5.9: Feedback schematic

rail-to-rail output buffer.

*opto.in* signal is output from a 1:400 resistor voltage divider placed on the output capacitor.

### 5.3 Duty cycle limitation

In the simulation, the maximal duty cycle was for the simplicity controlled by the maximal voltage of the error amplifier. This is also a principle which can't be incorporated into this design. It is possible to implement this feature via the current sense pin. In DCM operation, the current is proportional to the on-time of the switch. The principle of shifting the voltage on CS pin reduces the maximal current, which is basically the same thing as limiting the maximal duty cycle. This feature was implemented knowing the CS pin is a high-z and only negligible current should flow in/out. Resistor of the low-pass filter on the CS pin can bear this task (R9 in fig. 5.5). Constant current flowing through this resistor generates a voltage shift on the CS pin.

Simple resistor between DAC output and a CS pin is not suitable since the voltage on CS shifts during every switching cycle. Voltage controlled current source was used instead. Output voltage is increasing with a DAC voltage increasing. This means that higher DAC value means lower maximal duty cycle. This excluded the high-side source and additional current mirror had to be used. Figure 5.10 show schematics of the source. 2.5 V DAC value generates 640  $\mu A$  current, shifting the CS pin 640 mV higher. Some BJT mismatch is not crucial in this application.

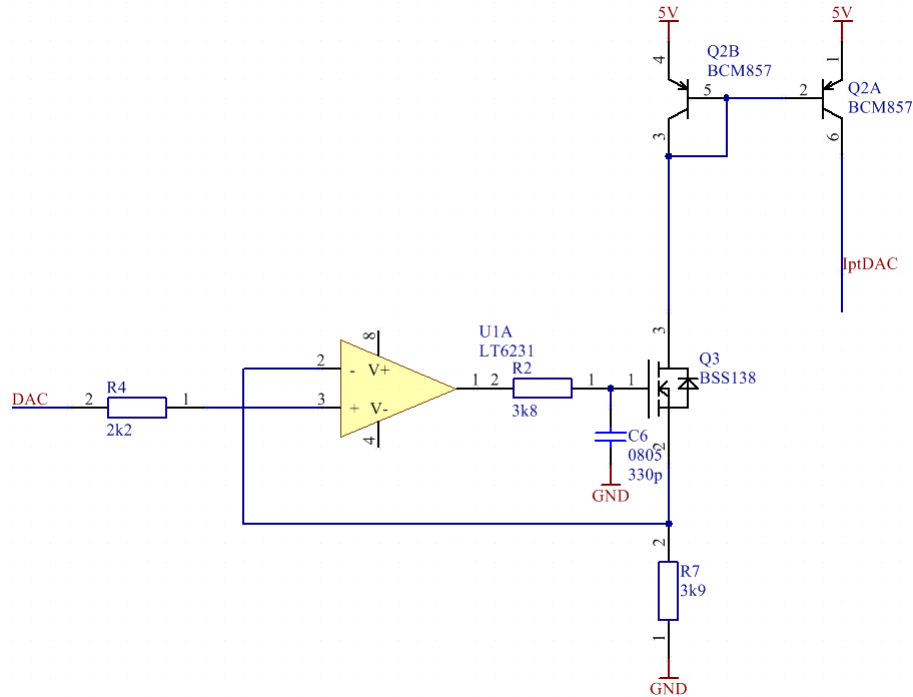


Fig. 5.10: Transconductance source

## 5.4 H-bridge

H-bridge schematic is shown in figure 5.11.

The output H-bridge is made of 4 IGBT transistors, 1.2 kV rated, 5 A continuous current. Two low side transistors are equipped with current limiting circuit, ensuring no fatal shoot-through. Furthermore, Zener diodes ensure maximal gate voltage of 5 V, which corresponds with around 5 A, so no higher surges should be possible.

While turning the transistors off can be as quick as possible, the turn-on time should take some time to allow potential load capacity to discharge through partially closed transistor and a free-wheeling diode. For this, there is R-C circuit with different time constant for charging and discharging, making discharge around seven times faster.

There are basically three stages, first are the pulse transformers with one primary and two secondary windings forming a simple flyback, each around 40 turns, each transformer corresponding with transistors for certain output polarity. Transistors are driven with a square waveform (will be described later).

Second stage, an RC circuit, consists of 1k resistor and 10n capacitor, giving very short time constant, meaning its almost instantly charged/discharged, depending on the transformer state.

Last stage is connected to the transistor gate and is charged via 22k resistor, whereas discharged through just a diode.

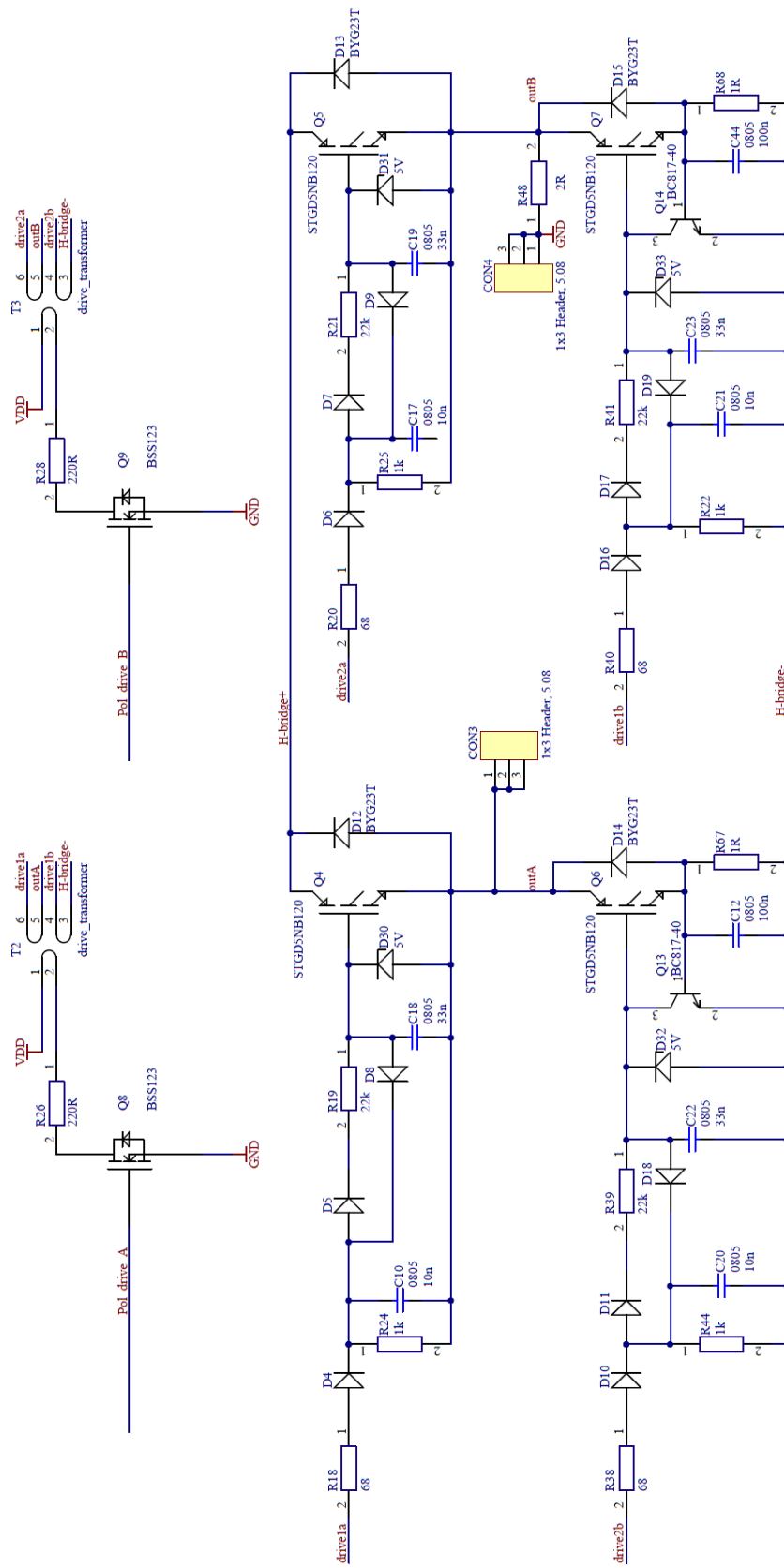


Fig. 5.11: H-bridge with gate driving circuitry

## 5.5 Square waveform generator

For driving the pulse transformers, square waveform has to be generated. External RC circuit of the PWM controller was used, where between the resistor and capacitor is roughly sawtooth waveform. Comparing it with a suitable voltage, 50% duty cycle square waveform can be generated. Second OPAMP in the package with transconductance source was used, reducing the component count.

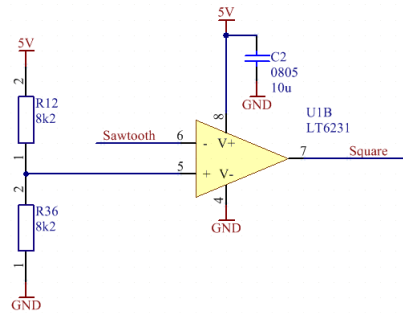


Fig. 5.12: square waveform generator

## 5.6 Pulse transformers driving

The pulse transformers are driven by two independent mechanisms. One is to ensure correct polarity on the output, the other one is discharging the output capacitor through the H-bridge in case of over-voltage condition.

### 5.6.1 Polarity and output enable control

Schematic for the polarity control circuit can be found in figure 5.13.

There are two input signals. *PSU\_OE* for output enable (active low) and *Polarity*. Output polarity is determined by which pulse transformer is active. The square waveform is driven into an 4051 analog demultiplexer, where the *Polarity* signal is a control signal switching between active outputs. *PSU\_OE* is INH (inhibit) signal, disconnecting all outputs into high-Z. *Polarity* has pull-down resistor, *PSU\_OE* pull-up so that the output is disabled with no low-impedance control signal connected.

Furthermore, there is a 4538 dual monostable flip-flop, where rising and falling edges of *Polarity* generates a 500 ns pulses. These output signals are also driven into control inputs of multiplexer, disconnecting the output and ensuring there is a small delay between changing a polarity, preventing any potential shoot-through.

Two signals are coming out of this multiplexer, which are either square waveform of high-Z. In high-Z condition, there is a pull-down resistor. In this point, the over-voltage signal is mixed in with a PMOS connected between either one of these two signals and a square waveform. When over-voltage signal is low (active), both lines are connected to

the square waveform, when the over-voltage is high, PMOS transistors are opened and do not influence the signals coming out of multiplexer.

If multiplexer is connecting the square waveform to one of the output signals and over-voltage occurs, both signals are in phase and no short-circuit occurs.

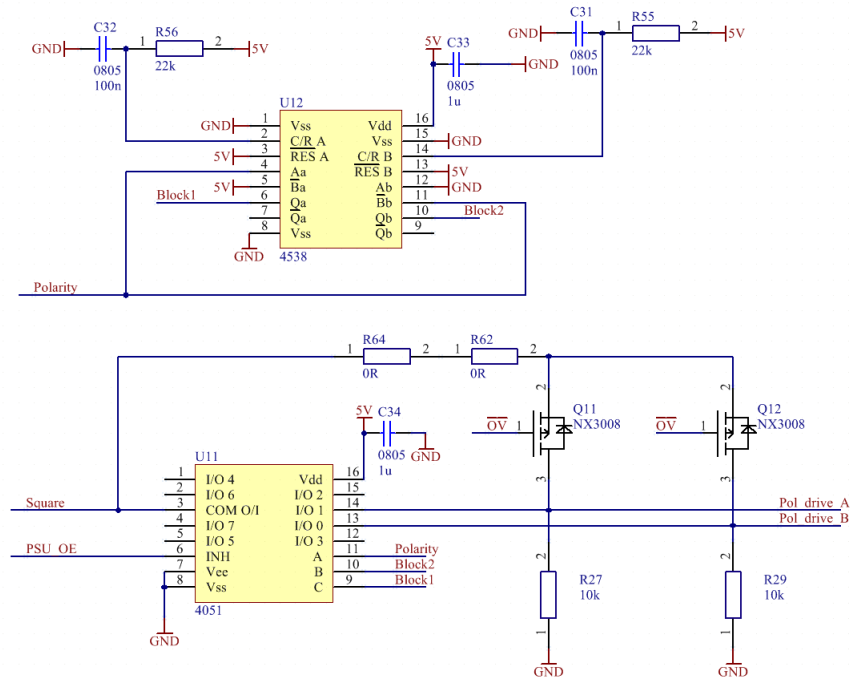


Fig. 5.13: Polarity, output enable and over-voltage discharge control circuit

## 5.6.2 Over-voltage protection

The feedback works in a way that voltage on the FB pin is stabilized to 2.5 V. If the value rises above that, there is higher voltage than desired on the output. Over-voltage signal is generated with a Schmitt trigger comparator, where one input is the FB pin and the other a trimmable voltage divider. Schematic is in figure 5.14.

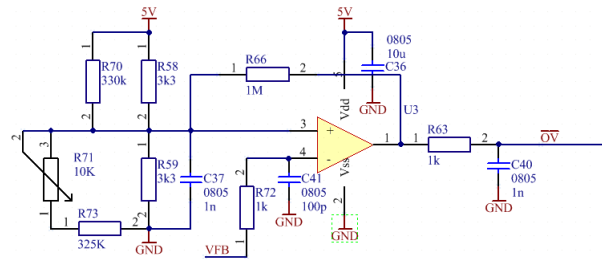


Fig. 5.14: Over-voltage signal generator

## 5.7 Voltage and current measurement

To measure voltage and current on the output, it has to be sampled after the H-bridge, which eliminates the error caused by voltage drop over the IGBTs. In figure 5.11, current sensing resistor R48 can be found between the *outB* and a *GND* output connector. Same voltage divider as the one in the optocoupler feedback is between the ground and the *outA* side of the H-bridge.

As the ADC, the ADS1120 was chosen, a 16-bit  $\Sigma\Delta$  converter from Texas instruments. The ADC features a programmable gain amplifier, which should be suitable especially for the current measurement, which can reach very low values. Except for the bypass capacitors, everything is integrated into the converter, so no external components, such as reference or oscillator are needed. The inputs are filtered to eliminate switching noise. Current sensing input is also clamped by two antiparallel Zener diodes to limit the voltage in case of high currents [11].

One drawback is that in order for the programmable gain amplifier to work correctly, input common mode voltage has to be between certain boundaries, ideally in the middle between  $V_{ss}$  and  $V_{dd}$ . Another isolated voltage had to be produced and also SPI interface isolator added to shift the signals to the ground reference, common for the DAC. Both ADC and isolator schematic is in figure 5.15, signal *Vout\_ADC* is coming from the above mentioned voltage divider.

Divided output voltage is between pins *AIN0* and *AIN1*, current sense resistor between *AIN2* and *AIN3*.

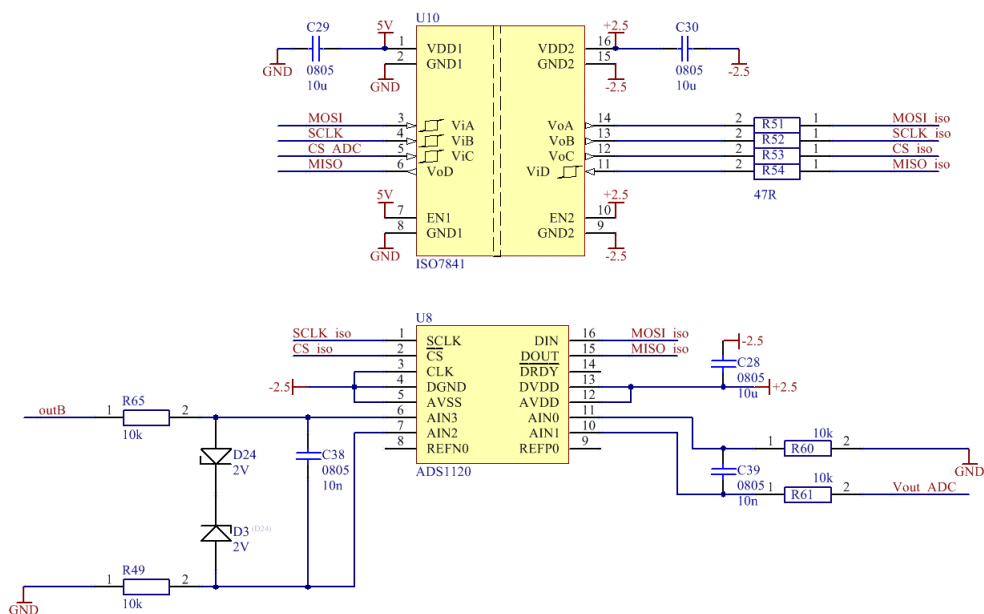


Fig. 5.15: ADC for voltage and current measurement, together with SPI isolator

## 5.8 Voltage sources

Some additional voltages had to be generated for different parts of circuit.

### 5.8.1 40 V DC

The input is 40 V AC transformer, so firstly it needs to be rectified and filtered with a capacitor. This part is simple two diode rectifier for center tap transformer and 1000  $\mu F$  electrolytic capacitor

### 5.8.2 18 V Vdd

The supply voltage for UC2843, pulse transformers as well as generating 5  $V_{AUX}$  and  $\pm 2.5 V$  for ADC. Made as N-MOS with 18 V Zener diode stabilizer connected to its gate.

### 5.8.3 5 V AUX, ADC supply

Figure 5.16 shows galvanically isolated power supply providing 5 V for secondary side of optocoupler as well as  $\pm 2.5 V$  with reference to the ground for the ADC converter and SPI isolator. Power source is made with ferrite cup transformer.

One primary winding with 40 turns is on one side driven with push-pull output stage of MOS-FET driver, which proves suitable for this application, on the other side tied between two balanced capacitors. As input waveform the square waveform signal is used.

Two secondary windings are both with center tap. Winding for powering the optocoupler is 40+40 turns, two diode rectification stabilized with Zener diode. Winding for ADC is 20+20 turns, generating both positive and negative voltage with reference to the center tap using bridge rectifier. Central tap is connected to the ground potential. Also stabilized with Zener diodes.

## 5.9 Digital to Analog Converter

The digital to analog converter sets the voltage value, on which is based output voltage and maximal duty cycle. To achieve decent output step, at least 12-bit converter has to be used, which means roughly 0,25 V per LSB. As was already mentioned in the feedback section, the DAC has to have a rail-rail output buffer (more precisely bottom rail). Texas instruments DAC7311 fulfills these requirements, provides SPI interface to keep just the one bus to communicate with the PSU and is also all-in-one solution with just a bypass capacitor as an extra component [13].

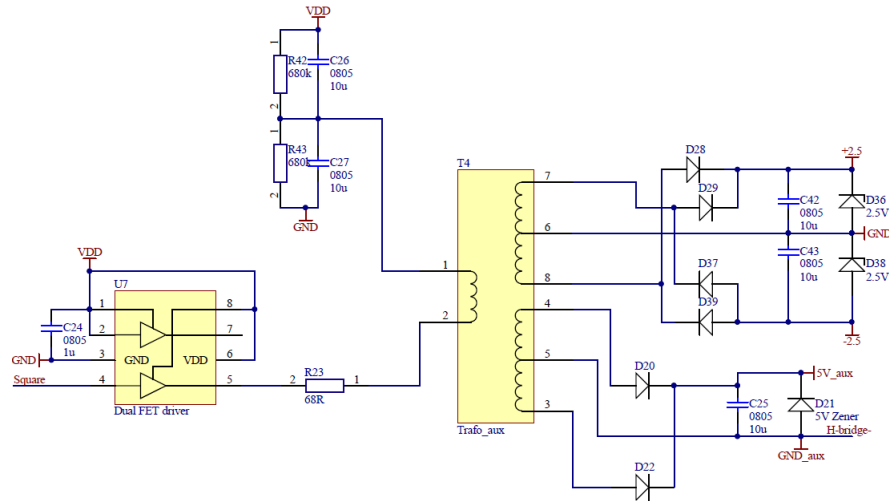


Fig. 5.16: Auxillary voltage power source

## 5.10 Interface

It was already indicated in previous sections that there are two signals, *PSU\_OE* which is active low and *Polarity*, where log.1 means positive with reference to the ground. *PSU\_OE* has a pull-up resistor, *Polarity* pull-down.

Both DAC for setting the output voltage and ADC for reading output voltage and current are connected on SPI bus. For communication protocol, refer to [11] and [13].

All of these signals are on the 2.54 mm spacing male header with pinout shown in figure 5.17.

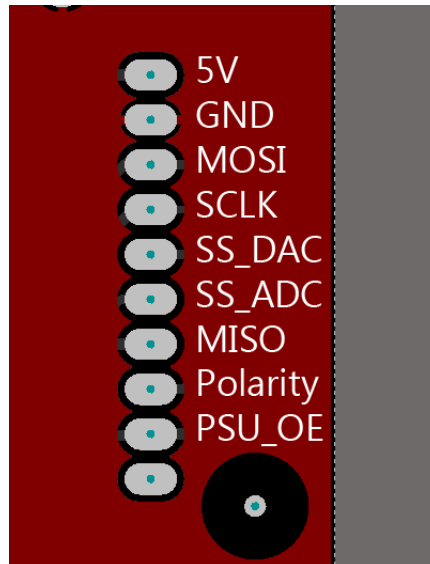


Fig. 5.17: Signal header pinout



## 5.11 PCB layout

Device was layouted on double-sided FR4 board. Special care had to be taken to keep sufficient clearance between primary and secondary circuits as well as cooling area for surface mount transistors. The board was designed to fit into computer PSU box, giving maximal dimensions of 145x145 mm. Layouted top and bottom layer can be found in appendix.

## 6 MEASUREMENT

After assembly and making sure all the primary and secondary side voltage sources work properly, individual parts were tested.

### 6.1 Main transformer

To verify the transformer inductances, it was connected in series with a 10R resistor, forming an RL circuit. The inductance was then measured as a cutoff frequency, meaning -3dB voltage transfer and 45 deg phase shift. Leakage inductance was measured the same way with the other winding short-circuited. Results are shown in tab. 6.1.

Tab. 6.1: Measured transformer inductances

	Primary	Secondary
Inductance / $\mu H$	88	3100
Leakage inductance / $\mu H$	0.5	34

Inductance corresponds with the calculations and leakage inductance under 1 % is an optimistic result.

### 6.2 Feedback

While feeding the optocoupler directly into the amplifier input, transfer characteristics of the amplifier was measured. With DAC set to 0 V and 1.25 V offset and amplitude sinusoidal wave as input, the waveform on figure 6.2 was obtained.

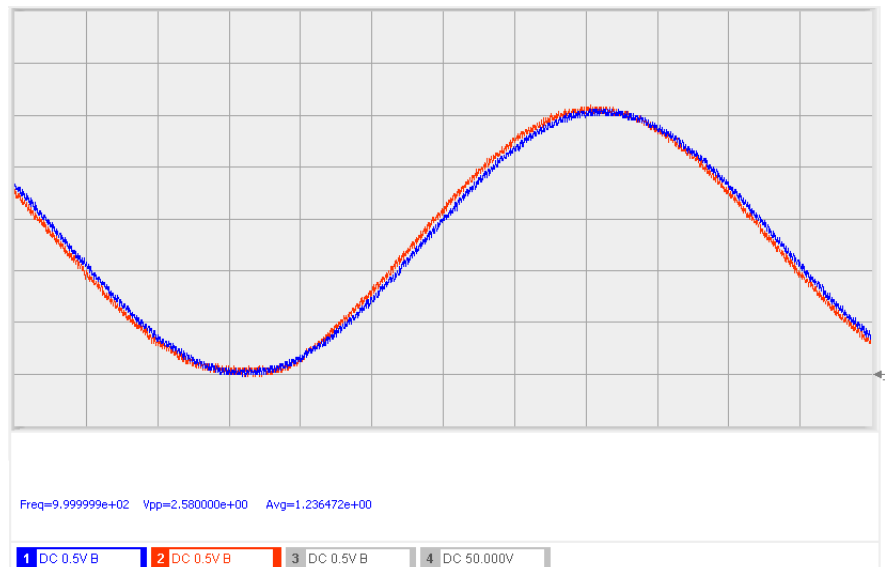


Fig. 6.2: Optoisolator transfer of 1 kHz sinusoidal wave over the full scale, red-input, blue-output.  $100 \mu s/div$

While the sinusoidal function seemed okay, measurement of a 0.5 V amplitude square wave showed more disturbing result (fig. 6.3). Even though the feedback on the signal source side worked properly, there were huge overshoots on the output side of the isolator. Additional capacitor of 33 pF parallel with the R6 load resistor limited the slew rate, but eliminated the overshoots, as shown in figure 6.4.

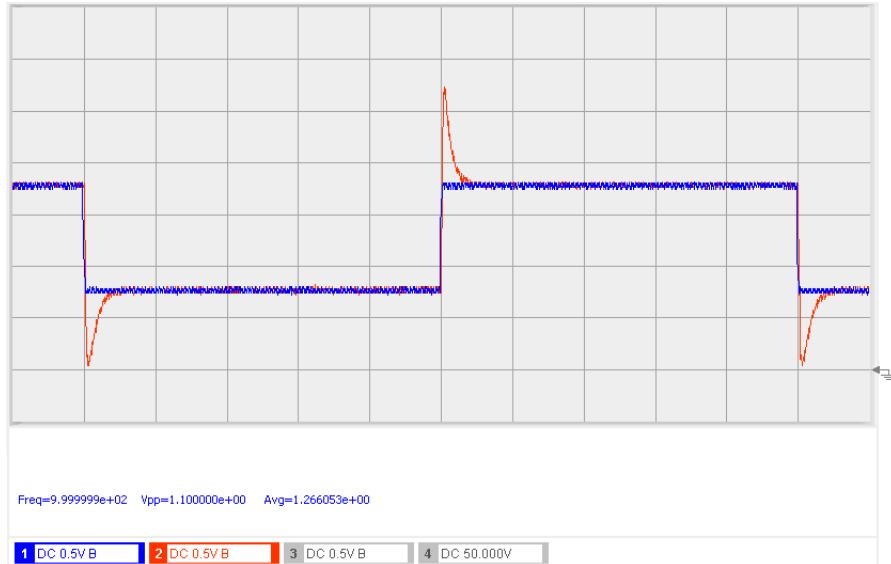


Fig. 6.3: Optoisolator transfer of 1 kHz square wave, showing some major overshoots, 1 V peak-peak, red-output, blue-input.  $100 \mu\text{s}/\text{div}$

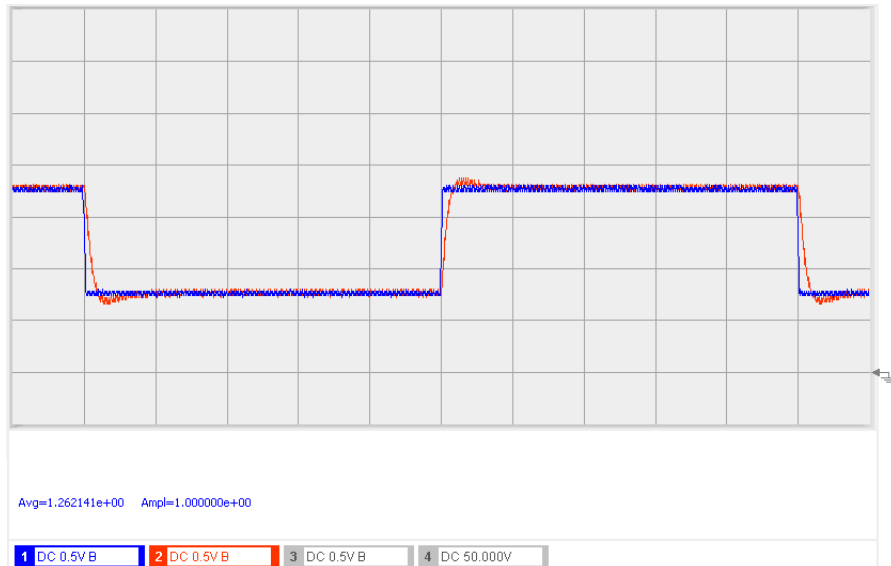


Fig. 6.4: Optoisolator transfer of 1 kHz square wave with capacity stabilized output, 1 V peak-peak, red-output, blue-input.  $100 \mu\text{s}/\text{div}$

This way, the optoisolator had bandwidth of 25 kHz, measured from the amplitude attenuation and phase shift, as shown in figure 6.5.

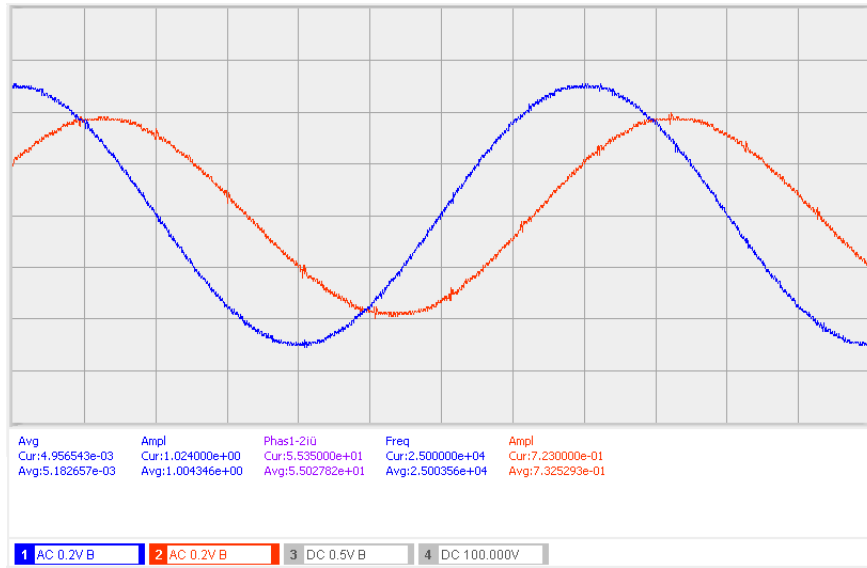


Fig. 6.5: Optoisolator bandwidth measurement, blue-input, red-output.  $5 \mu s/div$

Shifting the output voltage by the DAC is shown in figure 6.6. Output stage works correctly to slightly over 4 V.

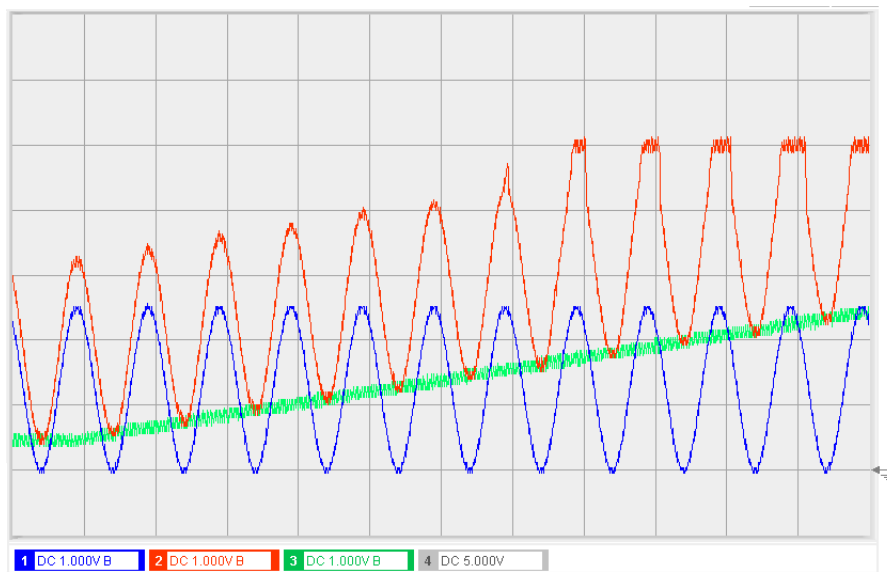


Fig. 6.6: Voltage shifting of optoisolator output, blue-input, red-output, green-DAC voltage.  $1 ms/div$

### 6.3 Duty cycle limitation

To verify the functionality of circuitry limiting the maximal duty cycle, voltage ramp was generated by the DAC while observing the voltage on CS. As shown in figure 6.7, circuit starts working from DAC voltage of around 500 mV, under this threshold, the operational amplifier is not able to drive the transistor correctly due to the lack of rail-rail input.

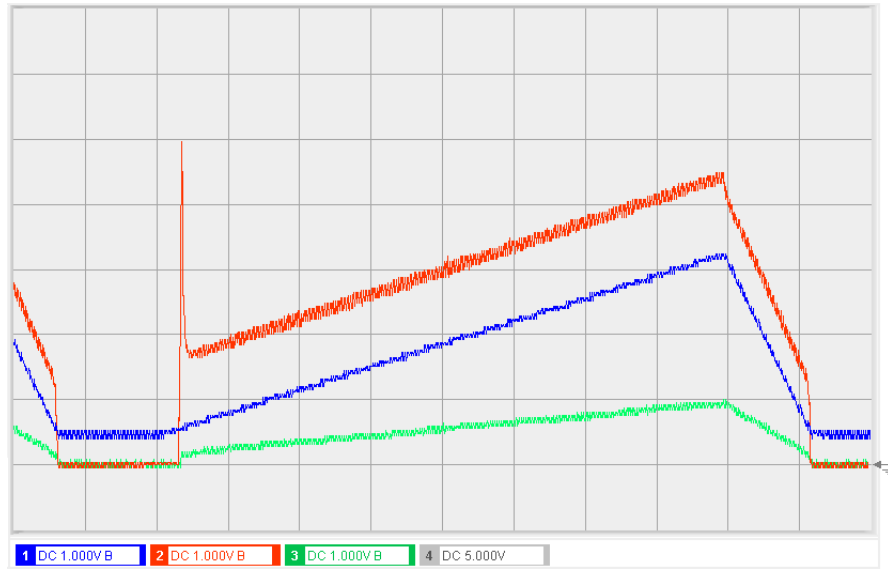


Fig. 6.7: Voltage shifting of *CS* pin, blue-DAC value, red-Q3 transistor gate voltage, green-CS pin voltage

### 6.4 H-bridge gate driving

First of all, the square waveform generation was verified. As can be seen in fig. 6.8, the sawtooth signal is neither full scale, nor oscillating around supply midpoint, so the comparing value had to be shifted to 2 V. Afterwards, the 94 kHz 48% duty cycle squares were generated.

Rectified voltage on the output of the pulse transformer and the transistor gate when enabling (fig. 6.9) and disabling (fig. 6.10) the observed transistor shows rise time of 0.7 ms, whereas fall time just 0.18 ms.

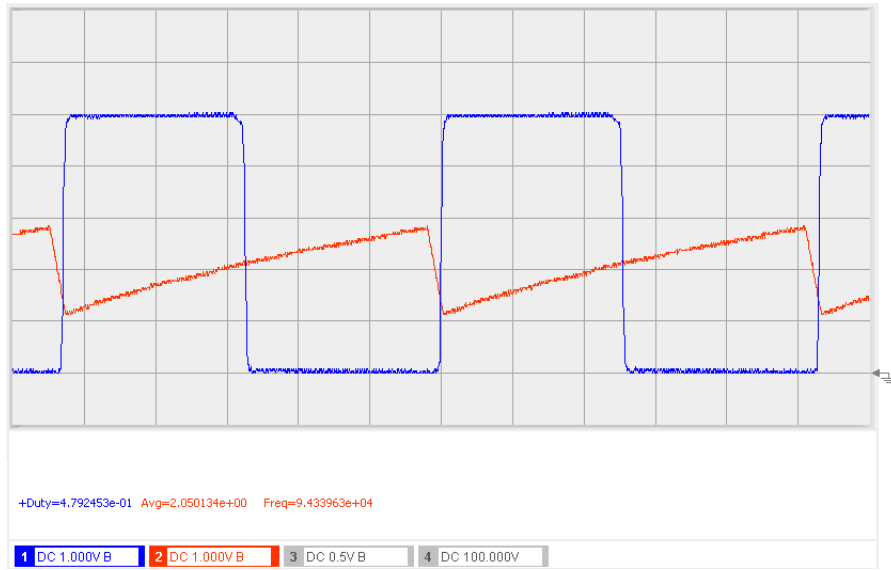


Fig. 6.8: Square waveform generator, red- $R_T/C_T$  pin voltage, blue-comparator output.  $2 \mu s/div$

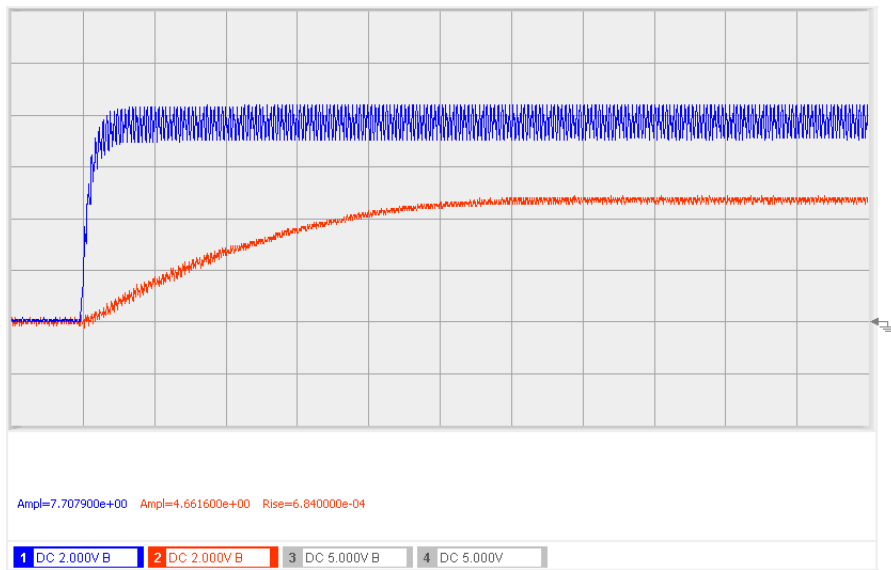


Fig. 6.9: Rectified pulse transformer output and IGBT gate voltage rise, blue-rectified transformer output, red-gate voltage.  $200 \mu s/div$

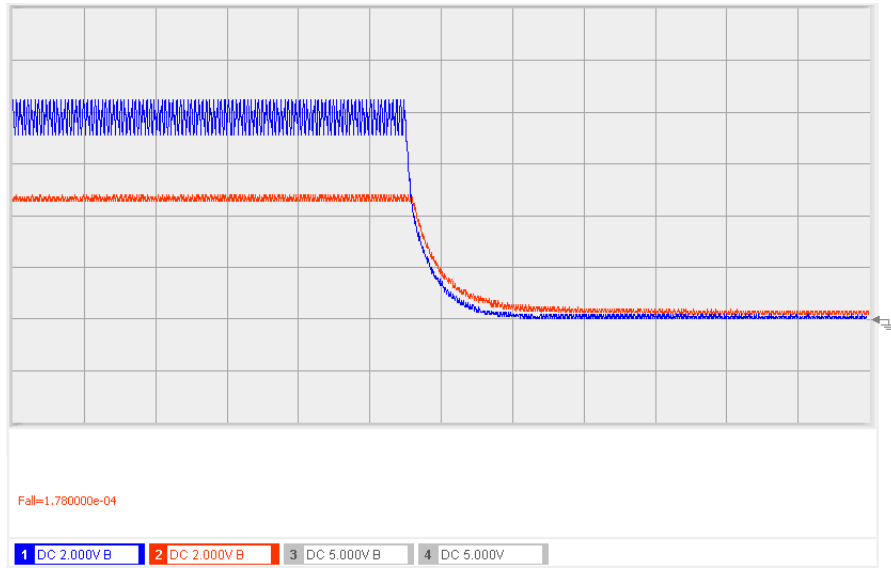


Fig. 6.10: Rectified pulse transformer output and IGBT gate voltage fall, blue-rectified transformer output, red-gate voltage.  $200 \mu s/div$

Figure 6.12 shows response to a polarity change. A gap of roughly 0.5 ms is visible.

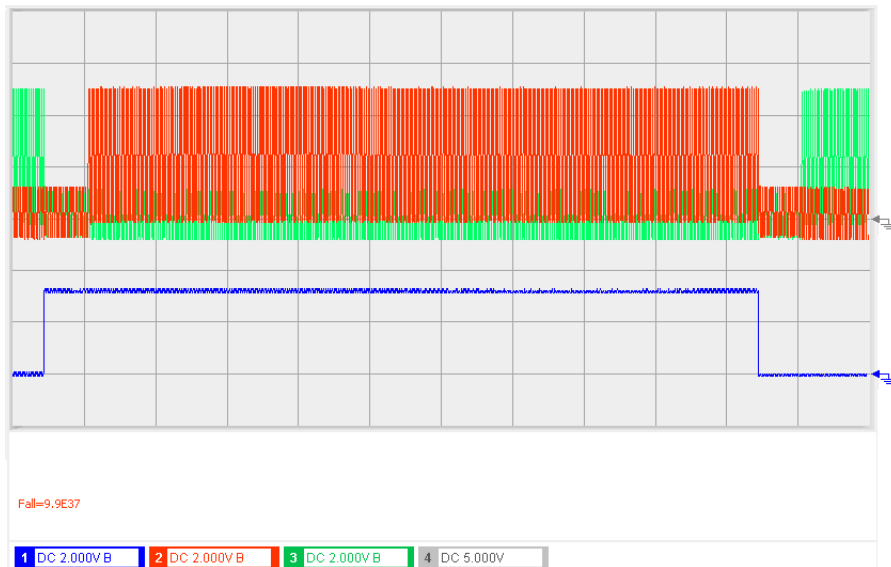


Fig. 6.11: Polarity change response, blue-*Polarity* signal, red and green-trwo pulse transformer drive signals.  $1 ms/div$

In case of over-voltage, the signals driving the pulse transformer MOSFETs are shown in figure 6.12. Both condition, demultiplexer closed and demultiplexer opened, are displayed.

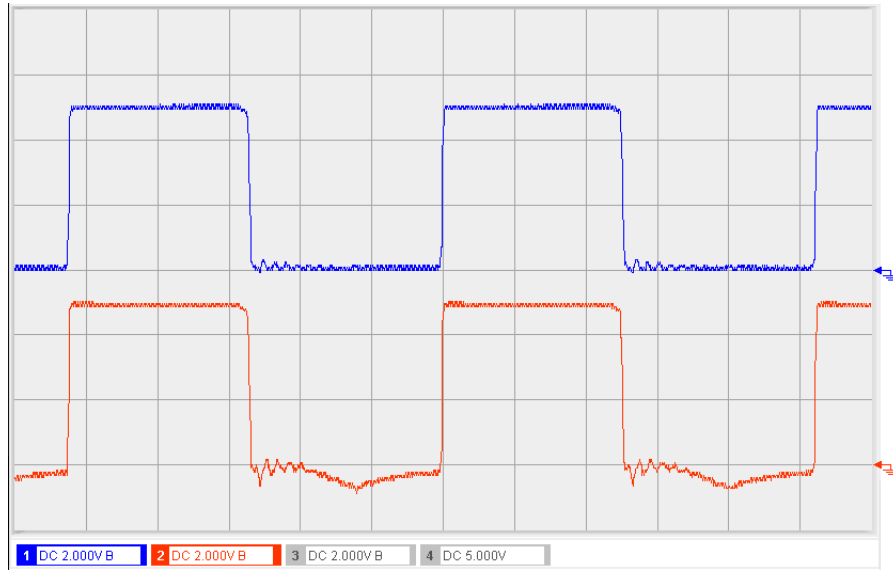


Fig. 6.12: Pulse transformer driving in overvoltage condition, red-mux in High-Z, blue-mux connected to the same pin.  $2 \mu s/div$



## 6.5 Flyback source

With all the auxillary circuitry working, the own power supply was tested.

### 6.5.1 Voltage transition

The voltage transitions are shown in figure 6.13. The circuit was loaded with a 47k resistor on the H-bridge output, which roughly corresponds to 20 W load with a 1 kV output voltage. All the transitions are under 5 ms and the duty cycle limitation is apparently working since the slope changes.

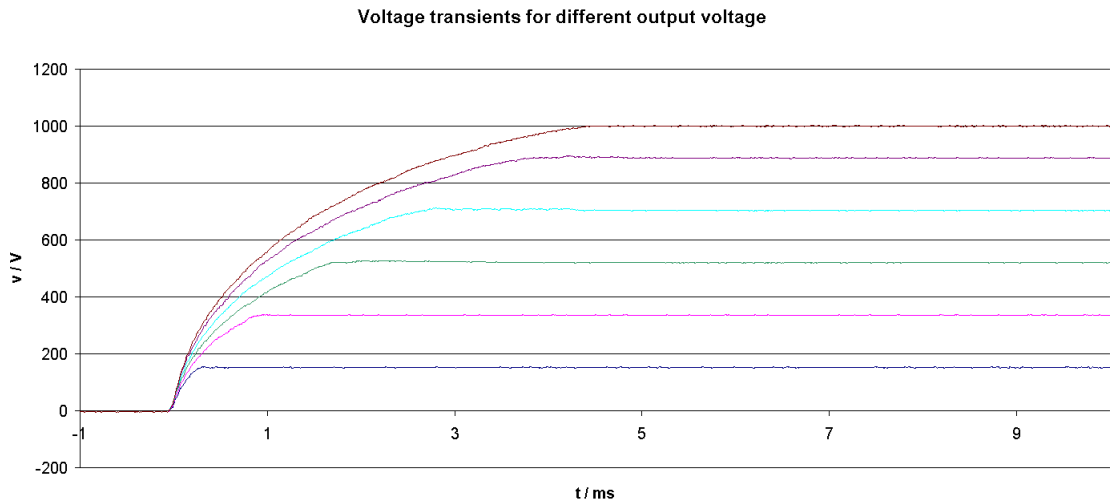


Fig. 6.13: Voltage transition for different output voltage

### 6.5.2 Ripple

Ripple voltage was measured also with 47k resistive load for three different output voltages. Figure 6.14 shows the ripple voltage being in a band of around 2 V with some extra switching generated spikes of 10 V amplitude, which were however just a measurement error, since no matter how big parallel capacity was connected, the peaks prevailed untouched.

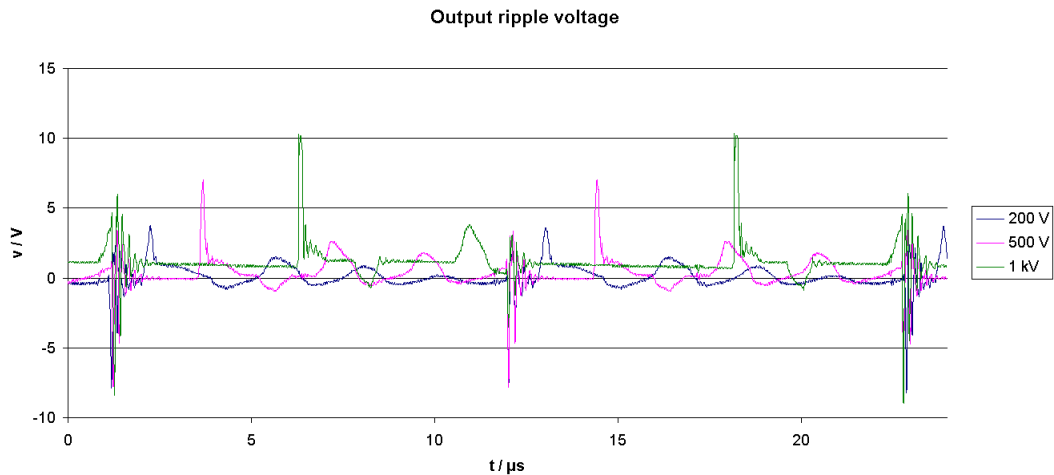


Fig. 6.14: Voltage ripple for 200, 500 and 1000 V

### 6.5.3 Capacitive load

Another thing to be verified is a capacitive load. Switching the polarity with high capacity connected to the output could potentially generate high current spikes, which should be minimized by the soft switching of the IGBT gates. In figure 6.15, three sections can be seen, firstly the discharge of the capacity when all the H-bridge transistors are opened, lasting around 0.5 ms. Afterwards, with the transistors partially opened, the capacity is being discharged through the high side of the bridge and the freewheeling diode, where the current is limited by the IGBT transconductance. The last part is when the load capacity is being charged with the current limited by the low side IGBT.

The discharge through the freewheeling diode has the highest slope, indicating the highest current. Detail of this section was measured and is shown in figure 6.16. The slope is a little under  $10 \text{ V}/\mu\text{s}$ , which for 220 nF capacity, using the equation 4.2 gives current of 2.2 A, well below the 18 A pulse rating of the diode.

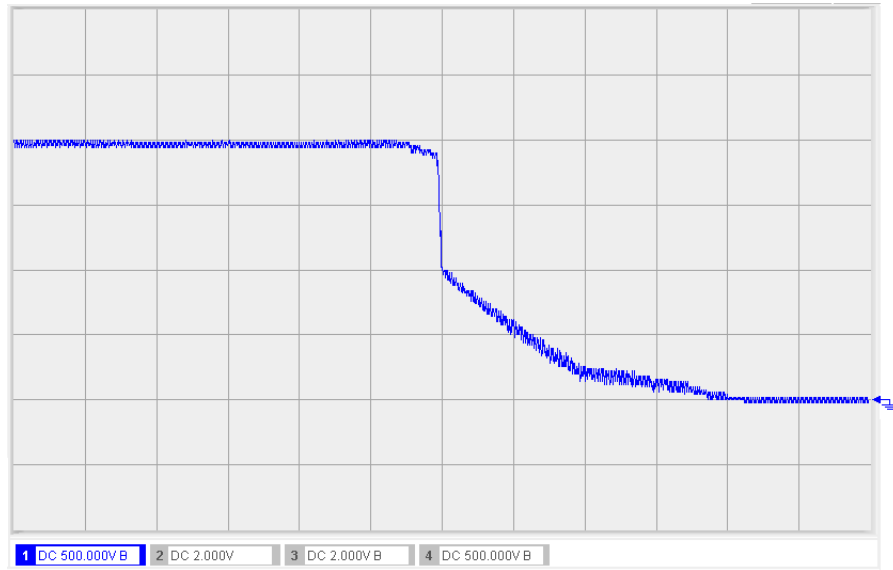


Fig. 6.15: Polarity switching transition with 220 nF capacitive load. 2 ms/div

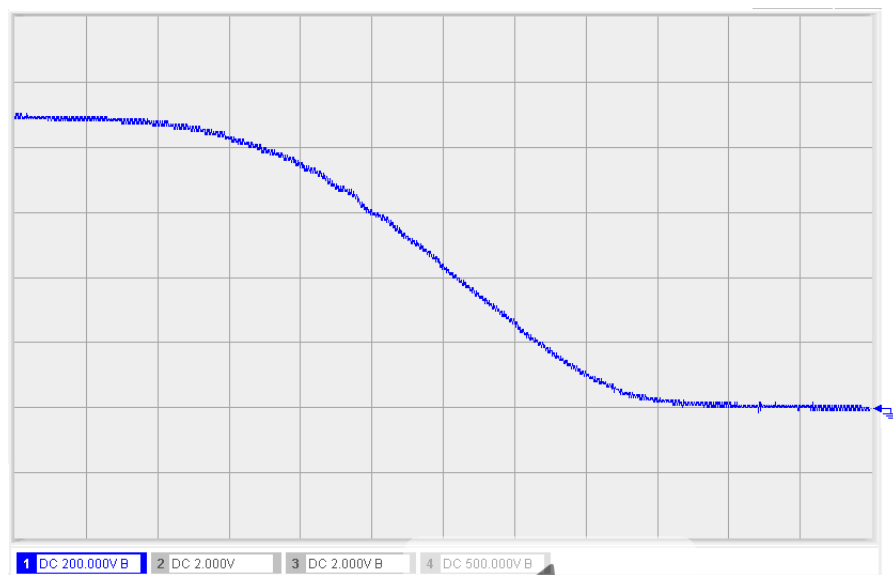


Fig. 6.16: Polarity switching transition, highest slope detail. 20  $\mu$ s/div

#### 6.5.4 Switching transistor

Drain-source voltage of the switching transistor was of a big concern during the simulation, therefore was also measured to ensure no excessive voltage stress takes place. The worst case, meaning 1 kV output voltage is in figure 6.17. Only negligible voltage overshoot is visible, placing only 200 V over the transistor. Some additional resonance occurs in the off-state, which is then cut by start of the next charging cycle. To reduce the power loss on in the snubber circuit, resistors were increased to 2 x 3k3 without any visible change in the waveform.

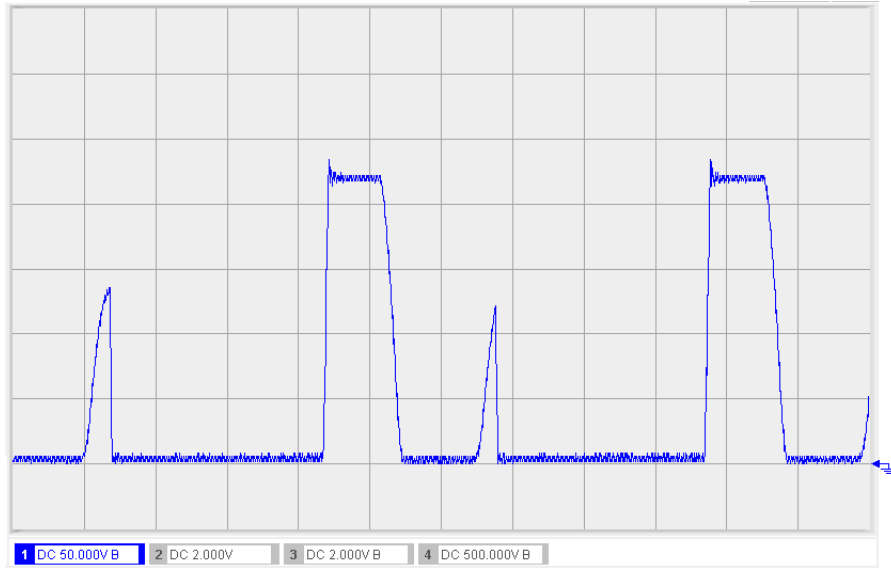


Fig. 6.17: Switching MOSFET  $V_{DS}$ .  $2 \mu s/div$

### 6.5.5 Transient load response

The supply unit was tested with a transition from zero load to full load (with already mentioned 47k resistor). The issue, which is shown in figure 6.18, occurred. When connecting or disconnecting load, the low-side transistor in the H-bridge opened for a period of 1 ms.

The issue originated in some interference inducing voltage in the current limiting BJT, which discharged the gate capacitor and opened the IGBT. The issue couldn't be eliminated even by soldering additional 100 nF capacitor directly on the base and emitter pins of the transistor.

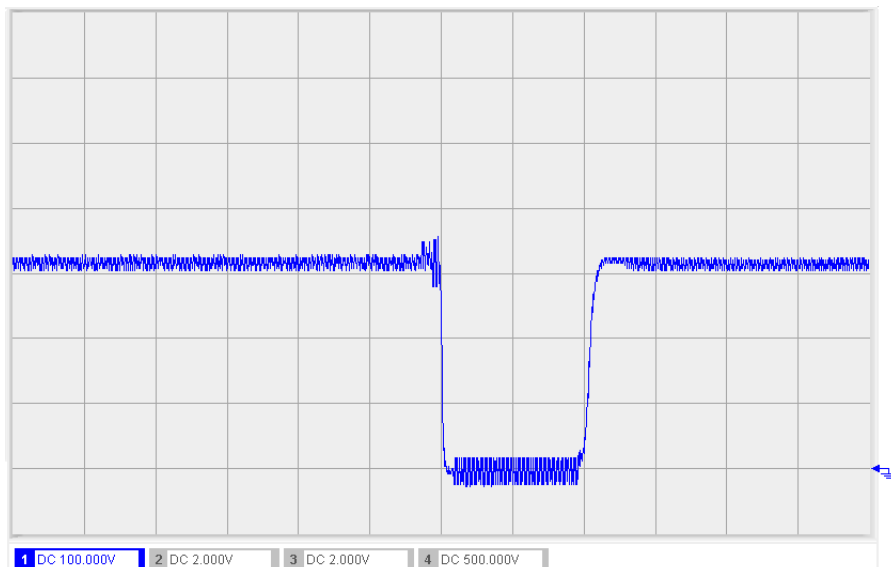


Fig. 6.18: Load transient response.  $500 \mu s/div$

### 6.5.6 Discharge

The voltage divider was experimentally trimmed to 2.53 V. This way the discharging worked as is shown in figure 6.19. Even though there is the voltage drop to zero volts, which seems inappropriate, it actually is a correct result considering both branches are closed with the low-side transistors limiting the current. All the output voltage is then over these transistors and the output potential is approaching zero.

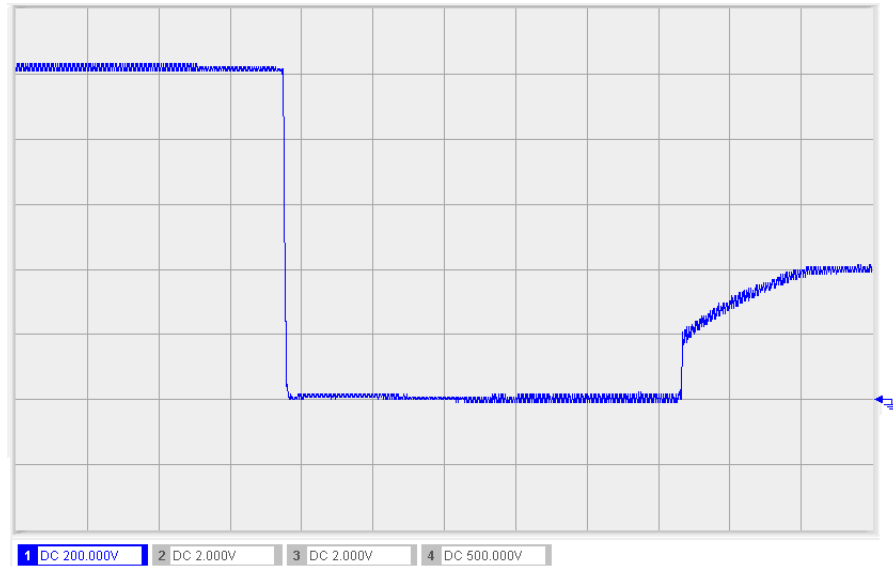


Fig. 6.19: Output voltage while discharging. 1 *ms/div*

To examine the behavior of the own discharging, the voltage over the capacitor before the H-bridge was measured. As can be seen in figure 6.20, the voltage decreases with a slope given by the current limitation of the low-side transistors, slightly undercharges and then the source increases the voltage to the desired level.

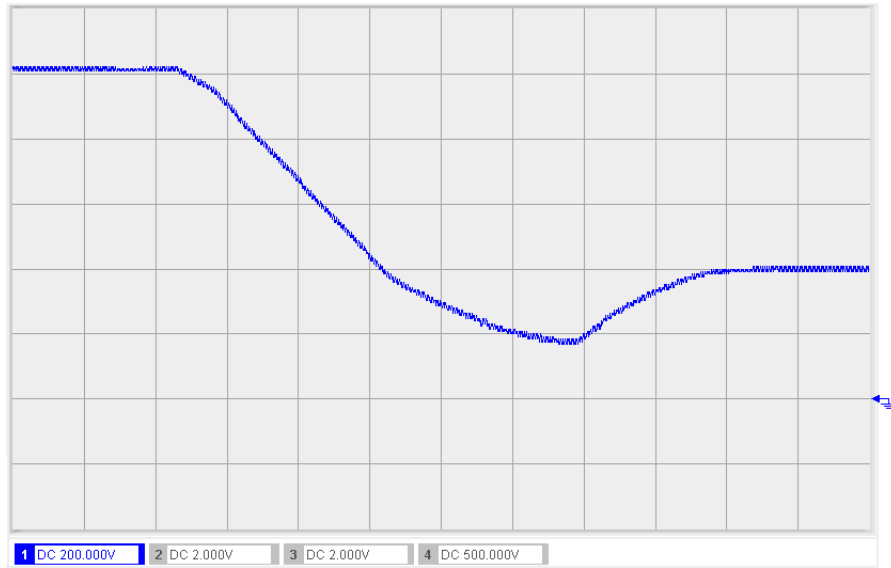


Fig. 6.20: Capacitor voltage while discharging. 1 ms/div

### 6.5.7 Load characteristics

The PSU was loaded with resistive load of 193k, 94k, 62k and 50k as well as measured without load, drawing approximately 0, 5, 10, 15 and 20 mA with a 1kV output voltage. Figure 6.21 shows dependency of output voltage on the current.

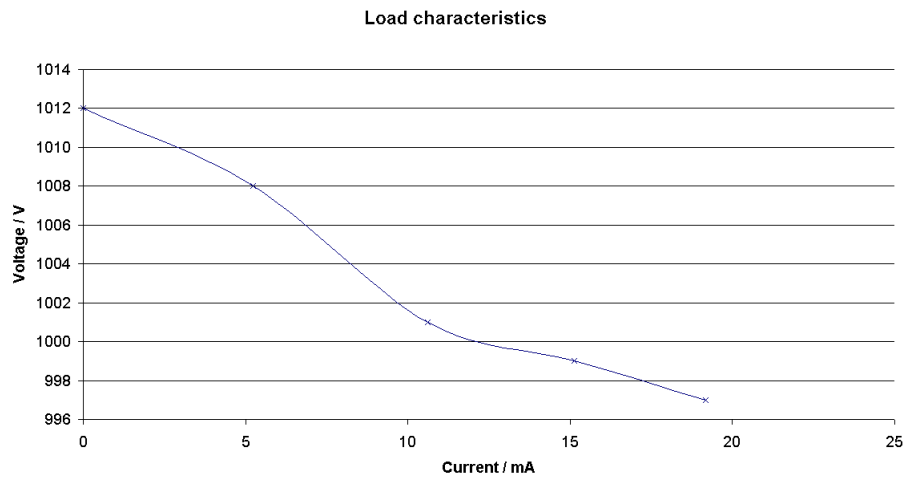


Fig. 6.21: PSU load characteristics

The load characteristics is approximately a straight line corresponding with an internal resistance of 800  $\Omega$

## 7 CONCLUSION

The designed flyback power supply unit was constructed and tested. The voltage transitions where the voltage was rising worked fine as well as switching the polarity. Decreasing the voltage was accompanied by the issue of the output voltage dropping to zero. When looking at this issue strictly from the point of view where the transition are supposed to be under 10 ms, the power supply passes, but more correct design would be with either additional transformers, allowing shoot-through on just one side of the bridge or one separate transistor with discharging being its sole purpose.

Issue was with a stability of the maximal current limiting loop, where induced  $V_{BE}$  voltage was closing the transistor and opening the low-side of the bridge. The issue occurred already in normal operation, but was solved with additional 100 nF capacitor between gate base and emitter, however the problem prevailed for transient load response and could not be eliminated by the H-bridge tuning. The result is disconnecting the load for around 1 ms, when both connected or disconnected.

This problem was additionally tested with extra 110 nF capacitor on the H-bridge output. Since it was proven that the power supply can withstand the capacitive load of this value easily while keeping the transition times in a given boundary, its possible to place it there as a part of a source. The load spike to the bridge was smoothed, H-bridge opening was eliminated with an additional bonus of filtering the output ripple voltage to a well below 1 V band. If transient load is expected, it is advised to place this capacitor between CON3 and CON4 pads.

Another potential solution could be placing a resistor to the base of the current limiting transistor and the capacitor after this resistor, as in figure , making a low-pass filter as shown in figure 7.2. In the implemented solution, the capacitor has to be over 10R resistor, making its function very limited. This potential remedy couldn't be tested due to the lack of space on the PCB.

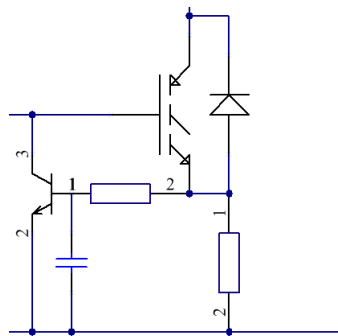


Fig. 7.1: Potential solution for H-bridge turn-offs

Another theoretical solution, at least partial, could be placing a resistor between the IGBT gate with the current limiting transistor and a gate capacitor. This way, the

capacitor couldn't be discharged instantly and the off-state would last just a tiny moment, if any.

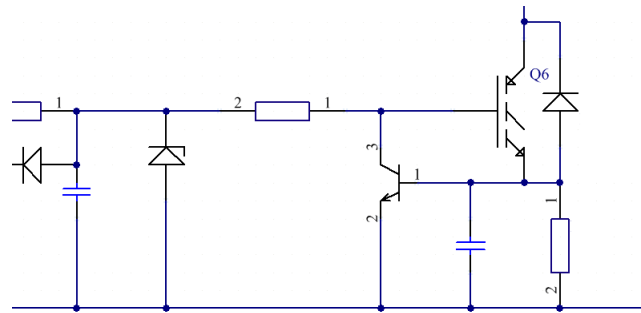


Fig. 7.2: Another potential solution for H-bridge turn-offs

As well as the previous suggestion, this method was not tested due to the lack of PCB space.

The transistor responsible for providing 18 V was only component dissipating any larger amount of heat and was actually provided with a small additional heatsink made of folded piece of copper metal plate. All the other components, including the main switching transistor were working close to a room temperature.

No device seemed to be working near its maximum electrical rating.

Design flaw, which was not fixed and can not be implemented on the current layout is lack of current limitation on 18 V source. Potential short-circuit may result in transistor breakthrough, forming low-resistance and letting 40V into the rest of the circuit, subsequently destroying the PWM controller as well as the rest of the circuits. Adding circuit similar the one on the low-side IGBT transistors would solve the issue.

Additional safety feature would be placing a fuse between the output clamp and the H-bridge. With short-circuited output, the current limitation of 50 mA and a 1 kV output generates 50 W of Joule heat on the IGBT. For a short duration, thanks to the thermal capacity of the transistor, it can withstand it, but for a longer duration, the PCB could not dissipate this amount of heat and the transistor would be destroyed.



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## ABBREVIATIONS AND ACRONYMS

ADC	Analog to Digital Converter
BJT	Bipolar Junction Transistor
CCM	Continuous Conduction Mode
DAC	Digital to Analog Converter
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PSU	Power Supply Unit
RMS	Root Mean Square
SPI	Serial Peripheral Interface

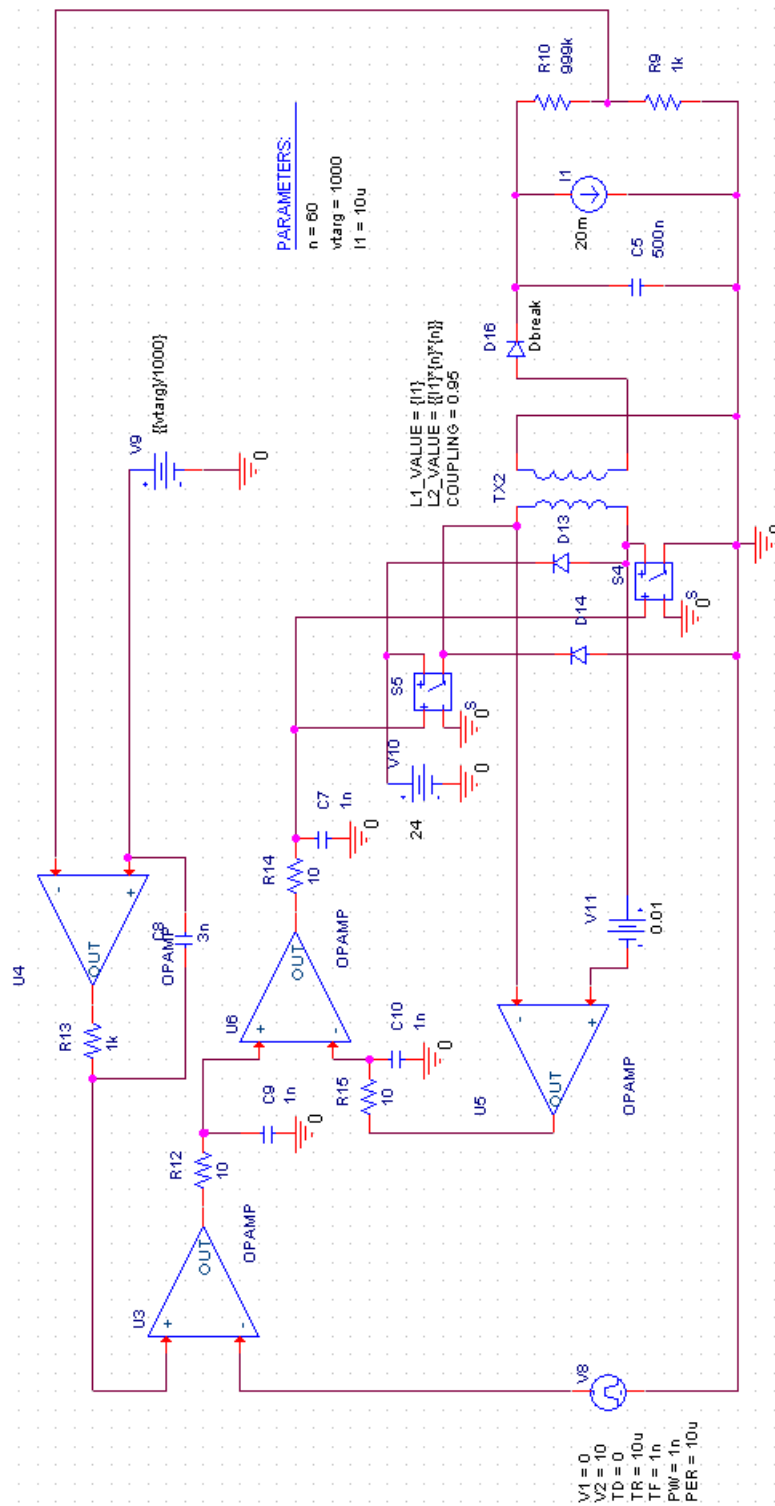
## APPENDIX

- A Single switch simulation model netlist
- B Two switch model schematic
- C Two switch simulation model netlist
- D PCB layout
- C Schematics

## A SINGLE SWITCH SIMULATION MODEL NETLIST

```
* source 1SWSIMULACNIMODEL
C_C1          0 VOUT 500n TC=0,0
X_TX1        VSUPPLY VSW 0 VSEC SCHEMATIC1.TX1
D_D1          VSEC VOUT Dbreak
V_V4          N09504 0
+PULSE 0 10 0 10u 100n 100n 10u
E_U1          N102442 0 VALUE {LIMIT(V(N14741,N09504)*1e6,0,2)}
R_R4          N102442 N10384 10 TC=0,0
C_C3          0 N10384 10n TC=0,0
E_U2          N107742 0 VALUE {LIMIT(V(N10915,VFB)*1000,0,{8/1000*{vtarg}})}
R_R5          N14741 N107742 1k TC=0,0
R_R6          0 VFB 10k TC=0,0
R_R7          VFB VOUT 990k TC=0,0
X_S3          N58557 0 VSW 0 SCHEMATIC1.S3
C_C9          0 N14741 1n TC=0,0
V_V8          VSUPPLY 0 24
E_U5          N581492 0 VALUE {LIMIT(V(N73235,VSUPPLY)*1e6,0,5)}
R_R21         N581492 N58953 10 TC=0,0
C_C14         0 N58953 10n TC=0,0
V_V9          VSW N73235 0.1
E_U6          N599072 0 VALUE {LIMIT(V(N10384,N58953)*1E6,-0,5)}
R_R22         N599072 N58557 10 TC=0,0
C_C15         0 N58557 1n TC=0,0
V_V10         N10915 0 {{vtarg}*0.01}
I_I1          VOUT 0 DC 1m
R_R23         VSW N64613 {{RC}}/{snubber_c} TC=0,0
C_C16         VSW N64613 {snubber_c} TC=0,0
D_D2          N64613 VSUPPLY Dbreak
.PARAM rc=500n vtarg=1000 n=6 l1=40u snubber_c=500p
.subckt SCHEMATIC1.TX1 1 2 3 4
K_TX1         L1_TX1 L2_TX1 0.95
L1_TX1        1 2 {l1}
L2_TX1        3 4 {{n}*{n}*{l1}}
.ends SCHEMATIC1.TX1
.subckt SCHEMATIC1.S3 1 2 3 4
S_S3          3 4 1 2 _S3
RS_S3         1 2 1G
.MODEL        _S3 VSWITCH Roff=1e6 Ron=10m Voff=0.0V Von=1.0V
.ends SCHEMATIC1.S3
```

## B TWO SWITCH MODEL SCHEMATIC



## C TWO SWITCH SIMULATION MODEL NETLIST

```
* source 2SW
C_C5          0 N52739  500n  TC=0,0
X_S5         N64559 0 N52971 N52959 SCHEMATIC1_S5
X_TX2        N52959 N52893 0 N66222 SCHEMATIC1_TX2
V_V10        N52971 0 24
D_D16        N66222 N52739 Dbreak
E_U3         N535452 0 VALUE {LIMIT(V(N53043,N53523)*1E6,0,2)}
R_R10        N53155 N52739  999k TC=0,0
X_S4         N64559 0 N52893 0 SCHEMATIC1_S4
V_V8         N53523 0
+PULSE 0 10 0 10u 1n 1n 10u
C_C8         N53043 N53747  3n  TC=0,0
R_R9         0 N53155  1k  TC=0,0
C_C7         0 N64559  1n  TC=0,0
D_D14        0 N52959 Dbreak
R_R12        N535452 N53235  10 TC=0,0
D_D13        N52893 N52971 Dbreak
V_V9         N53747 0 {{vtarg}/1000}
E_U4         N536172 0 VALUE
+{LIMIT(V(N53747,N53155)*200000,0,{7e-3*{vtarg}})}
R_R13        N53043 N536172  1k  TC=0,0
E_U5         N64677 0 VALUE {LIMIT(V(N64307,N52959)*1E6,0,5)}
V_V11        N52893 N64307 0.01
E_U6         N644222 0 VALUE {LIMIT(V(N53235,N68529)*1E6,0,+5)}
C_C9         0 N53235  1n  TC=0,0
R_R14        N644222 N64559  10 TC=0,0
R_R15        N64677 N68529  10 TC=0,0
C_C10        N68529 0  1n  TC=0,0
I_I1         N52739 0 DC 20m
.PARAM  vtarg=1000 n=60 l1=10u

.subckt SCHEMATIC1_S5 1 2 3 4
S_S5          3 4 1 2 _S5
RS_S5         1 2 1G
.MODEL        _S5 VSWITCH Roff=1e6 Ron=10m Voff=0.0V Von=1.0V
.ends SCHEMATIC1_S5

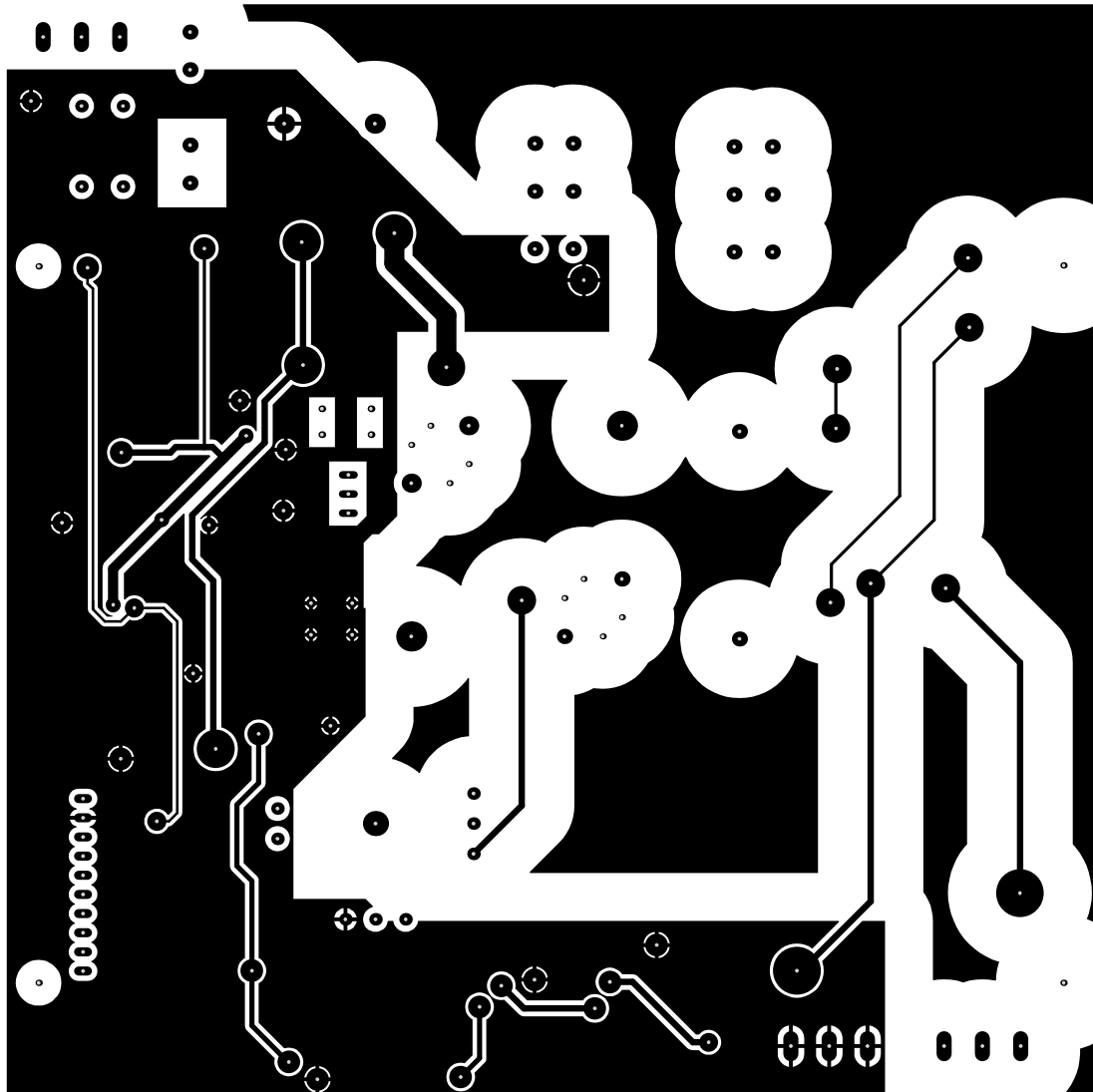
.subckt SCHEMATIC1_TX2 1 2 3 4
K_TX2         L1_TX2 L2_TX2 0.95
```

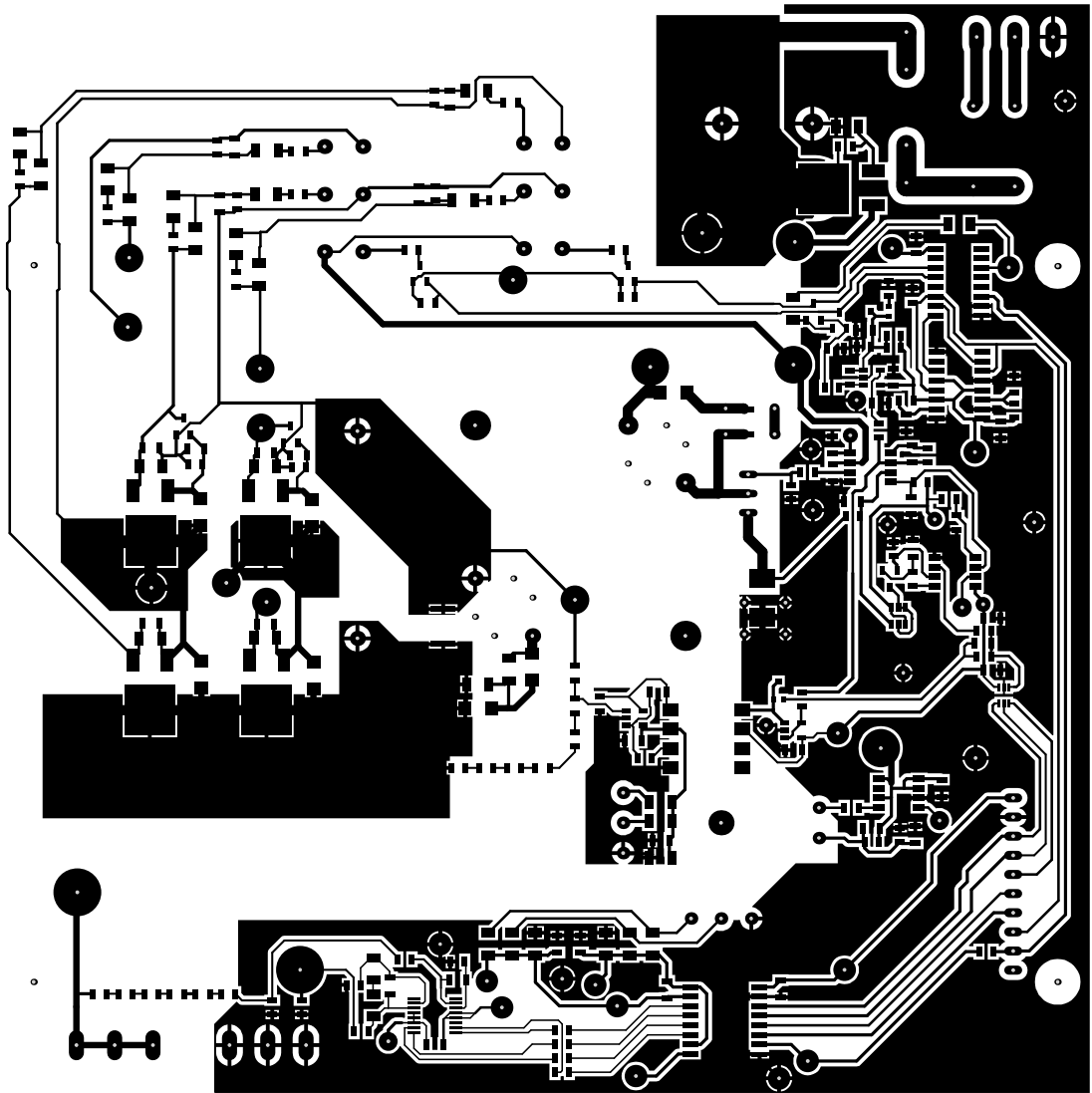
```
L1_TX2      1 2 {11}
L2_TX2      3 4 {{11})*{n})*{n}}
.ends SCHEMATIC1_TX2

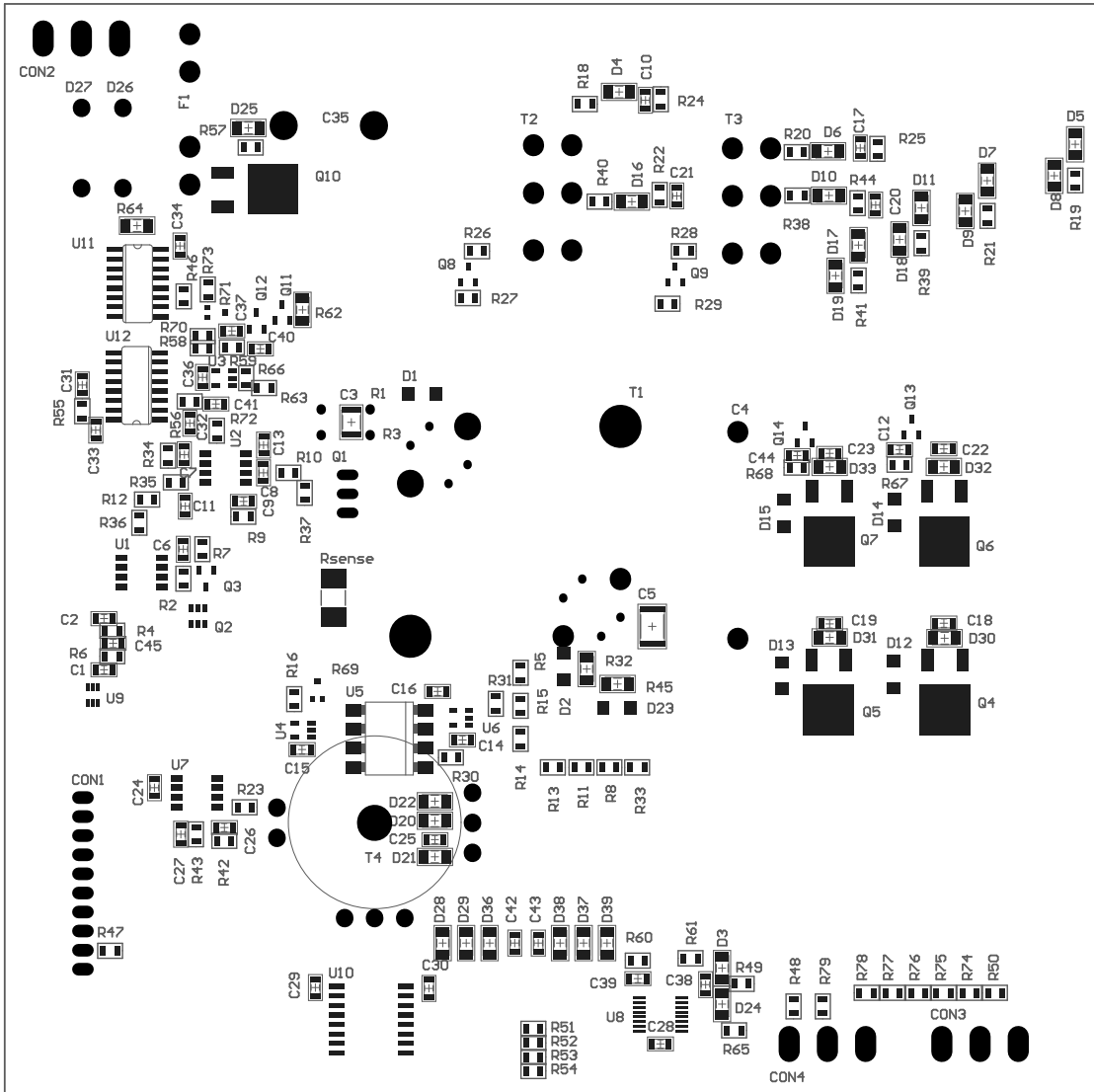
.subckt SCHEMATIC1_S4 1 2 3 4
S_S4        3 4 1 2 _S4
RS_S4       1 2 1G
.MODEL      _S4 VSWITCH Roff=1e6 Ron=10m Voff=0.0V Von=1.0V
.ends SCHEMATIC1_S4
```



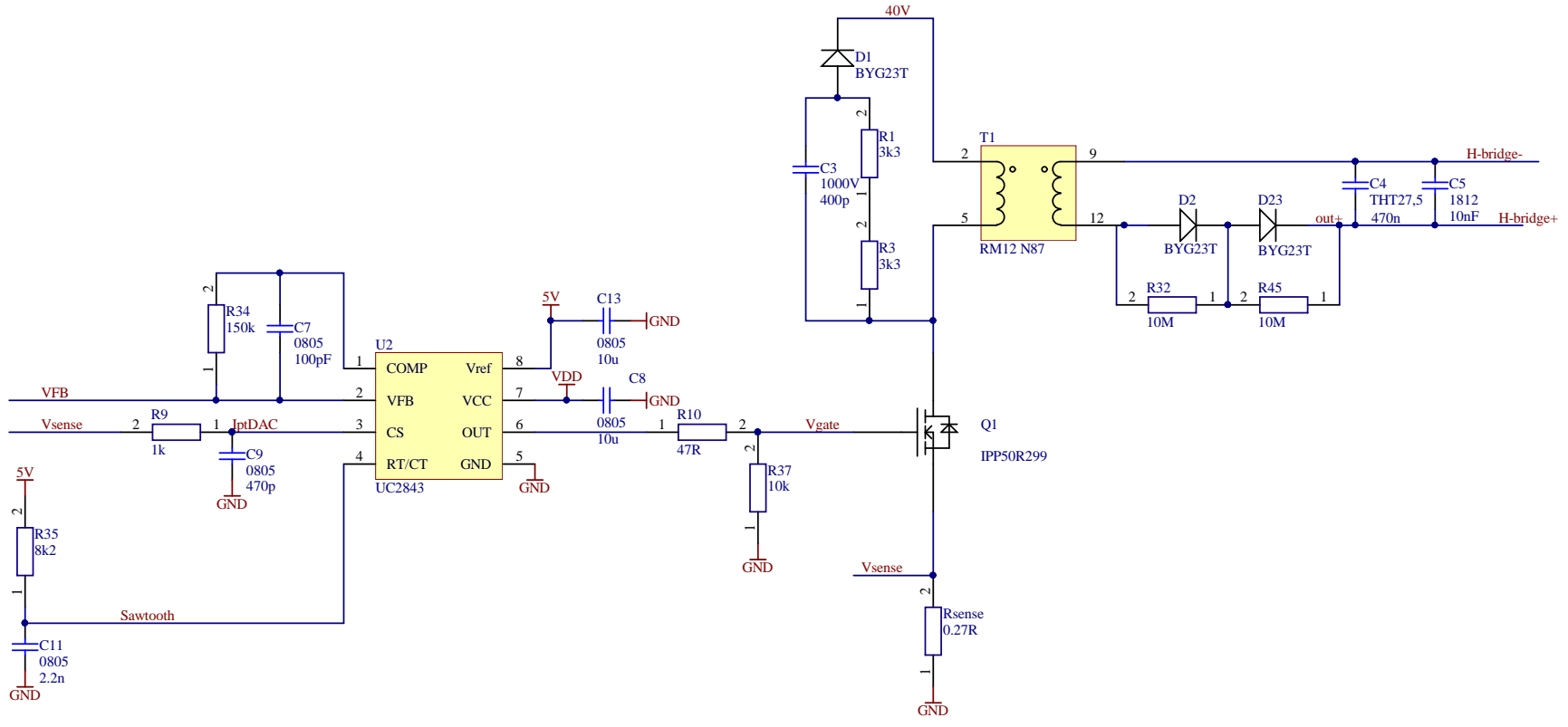
## D PCB LAYOUT

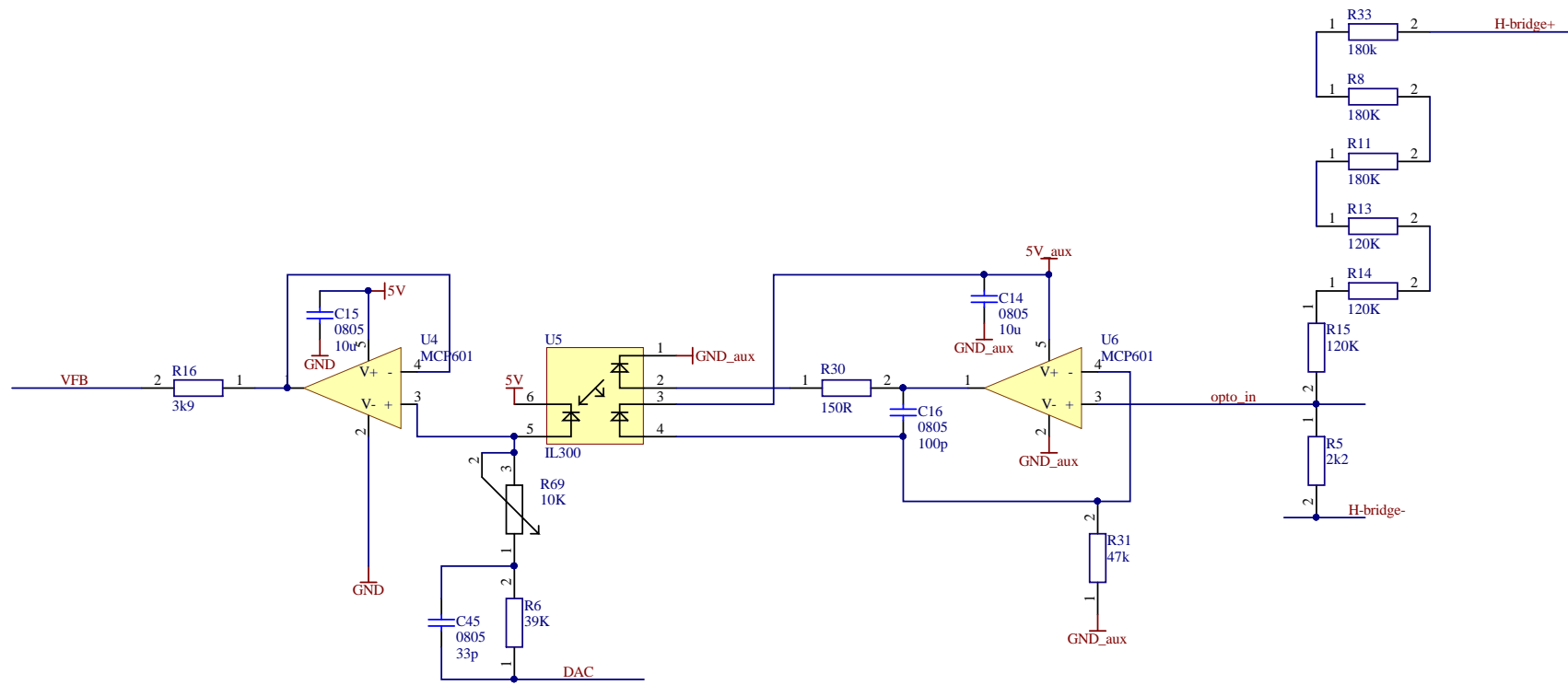


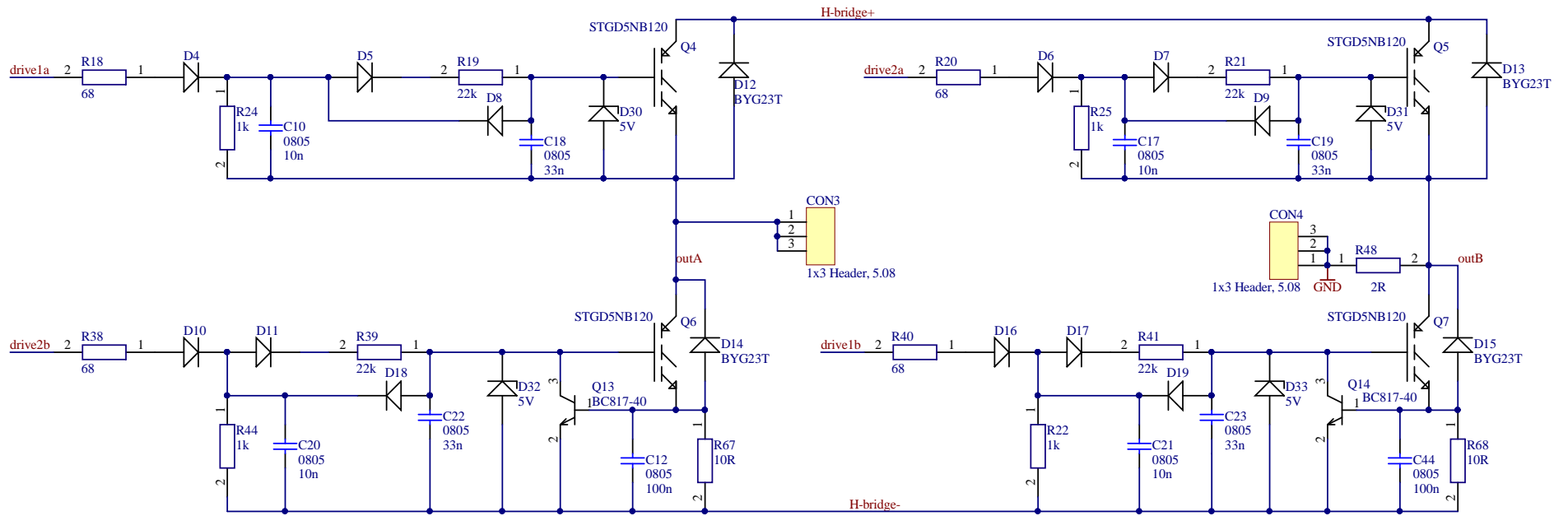
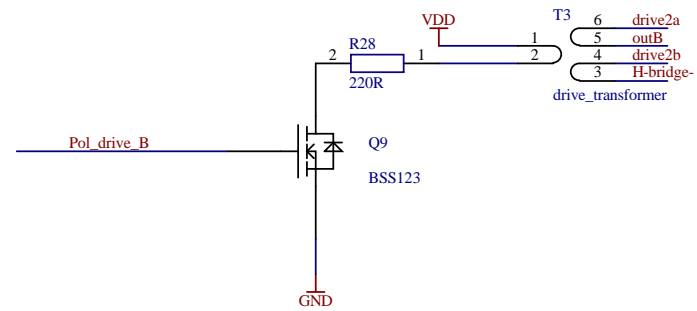
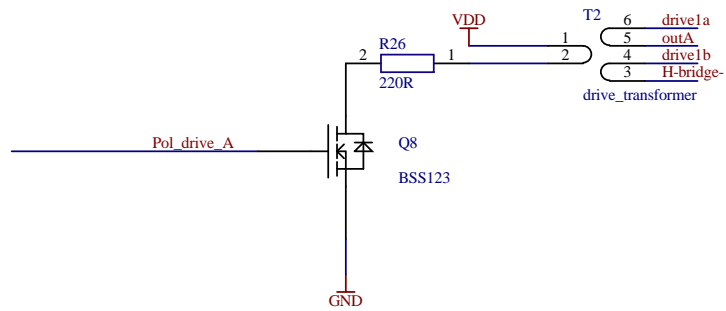




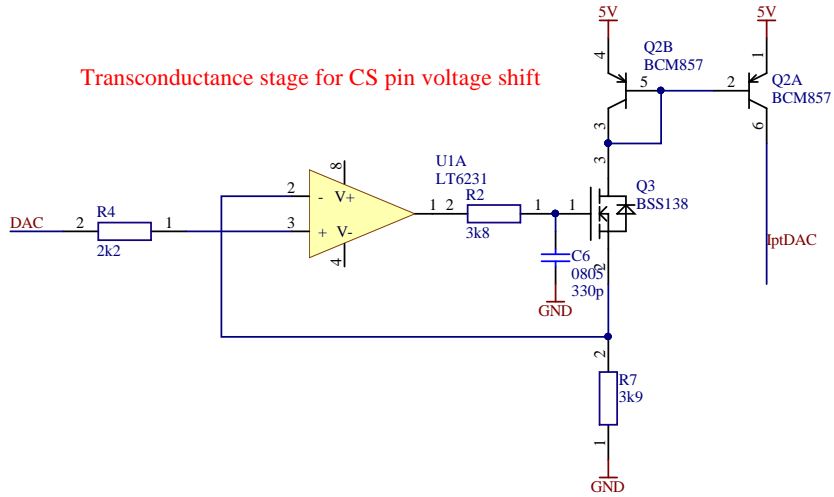
E SCHEMATICS



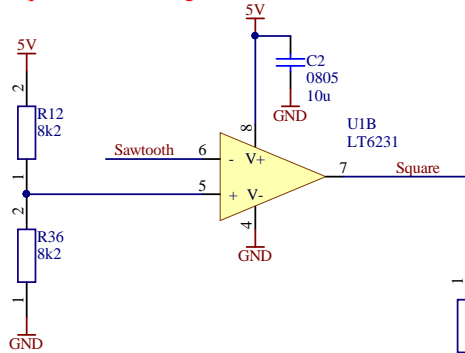




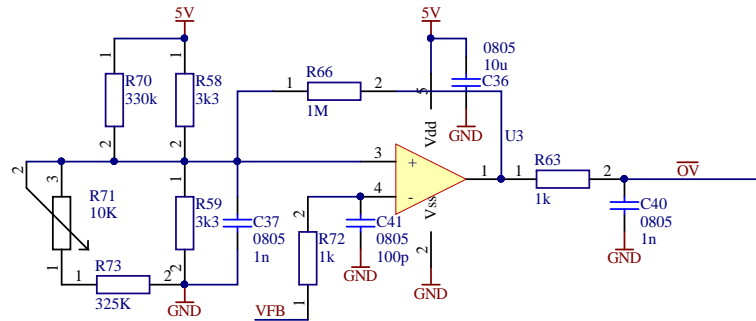
Transconductance stage for CS pin voltage shift



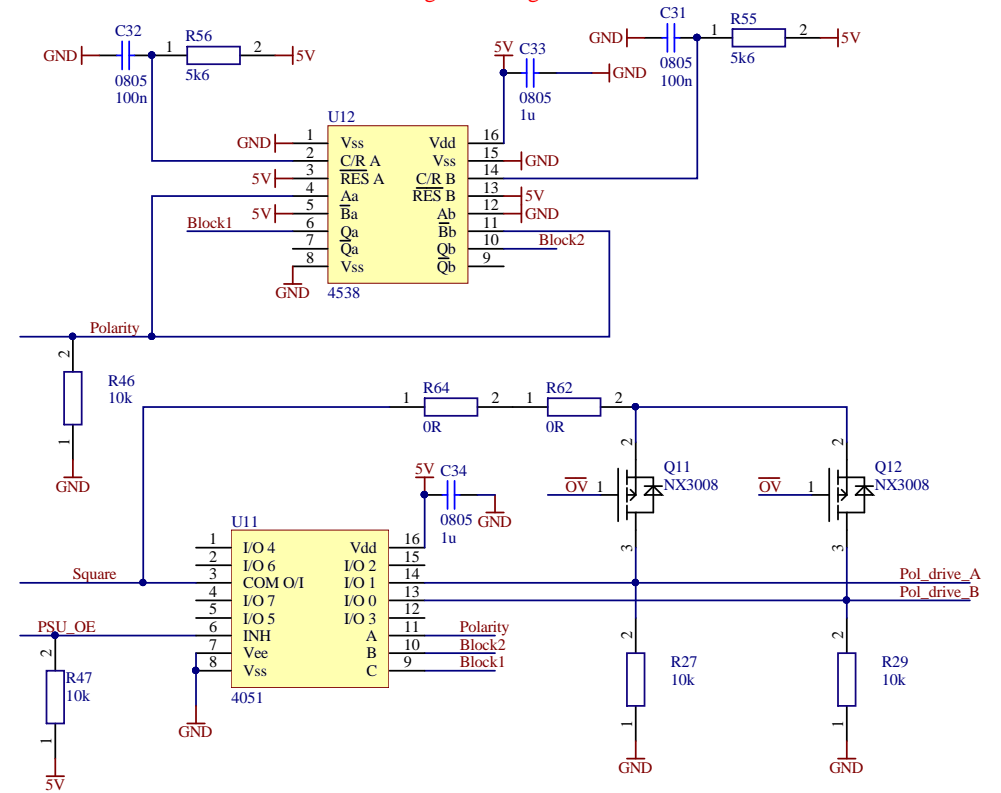
Square waveform generator



Over-voltage signal generator

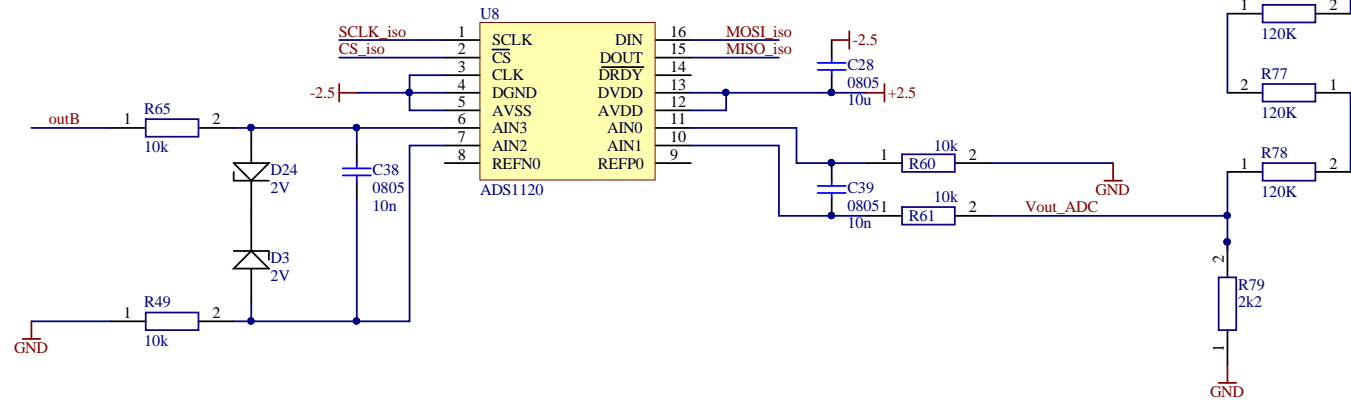
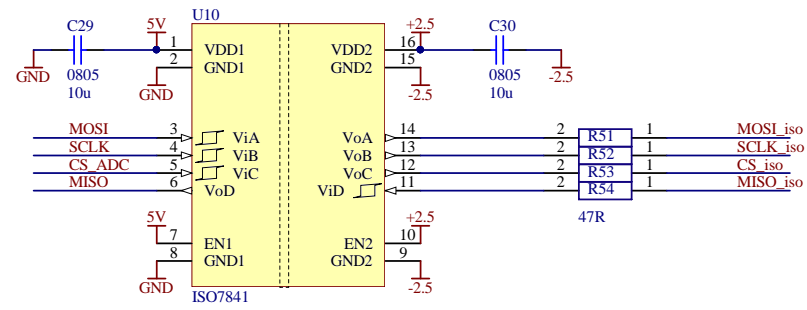
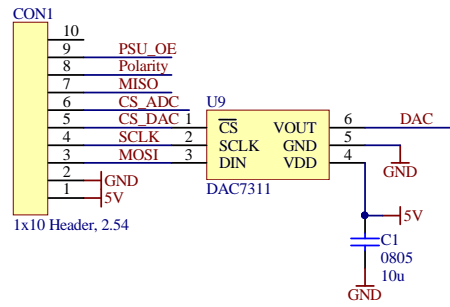


Pulse transformer gate driving



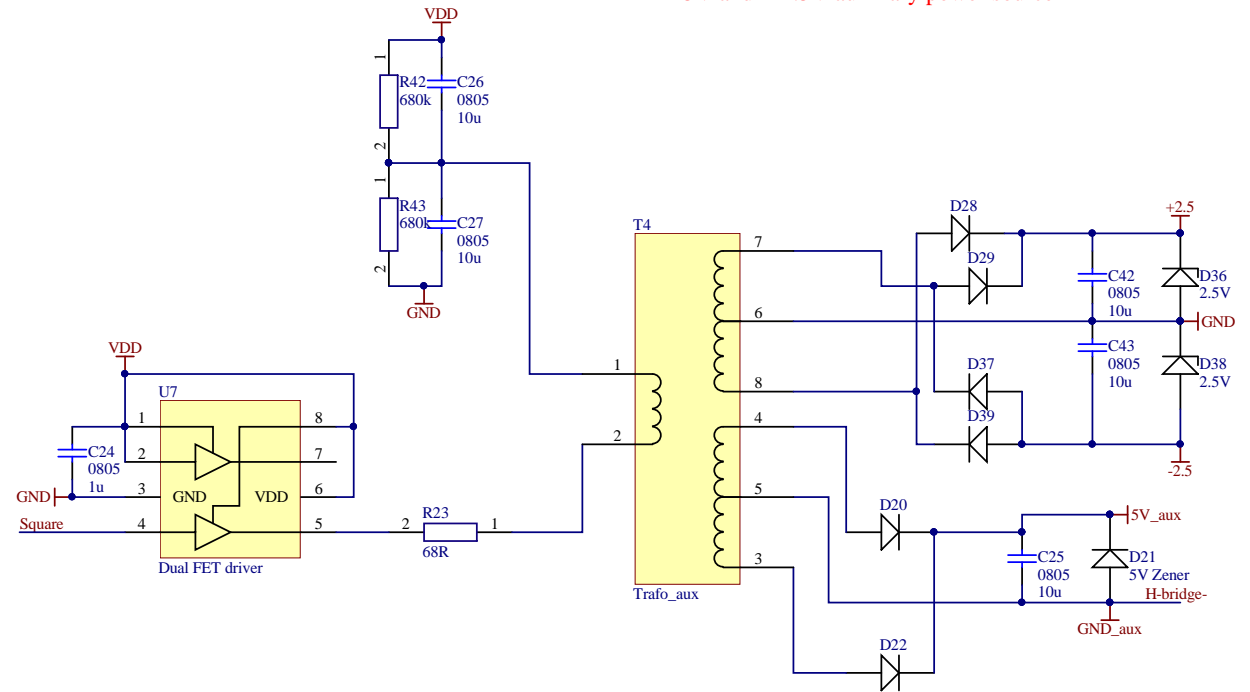
## DAC with isolator

### Header connector and DAC





+5V and +2.5V auxiliary power source



+18V power source

