BRNO UNIVERSITY OF TECHNOLOGY

Faculty of Electrical Engineering
and Communication

MASTER'S THESIS

Brno, 2024 Bc. Matyáš Sedláček

BRNO UNIVERSITY OF TECHNOLOGY

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF RADIO ELECTRONICS

ÚSTAV RADIOELEKTRONIKY

A SHORT-PULSE GENERATOR FOR UWB APPLICATIONS

GENERÁTOR KRÁTKÝCH PULSŮ PRO UWB APLIKACE

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

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BRNO 2024

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ

Diplomová práce

magisterský navazující studijní program **Elektronika a komunikační technologie**

Ústav radioelektroniky

Student: Bc. Matyáš Sedláček ***ID:*** 221069

Ročník: 2 ***Akademický rok:*** 2023/24

NÁZEV TÉMATU:

Generátor krátkých pulsů pro UWB aplikace

POKYNY PRO VYPRACOVÁNÍ:

Seznamte se s principy generování krátkých napěťových pulsů pro Ultra-Wide-Band (UWB) aplikace. Zaměřte se na generátory využívající step-recovery diody (SRD). Proveďte analýzu generátoru.

Vybraný koncept generátoru realizujte a experimentálně ověřte. Získané výsledky diskutujte.

DOPORUČENÁ LITERATURA:

[1] UWB Theory and Applications. Ed. I. OPPERMANN, M. HÄMÄLÄINEN, J. IINATTI. Chichester, UK: John Wiley, 2004. ISBN 0-470-86917-8.

[2] JEONGWOO HAN a C. NGUYEN. On the development of a compact sub-nanosecond tunable monocycle pulse transmitter for UWB applications. IEEE Transactions on Microwave Theory and Techniques. 2006, 54(1), 285-293 [cit. 2023-05-22]. ISSN 0018-9480.

Termín zadání: 16.2.2024 ***Termín odevzdání:*** 20.5.2024

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ABSTRACT

This master's thesis is concerned with the analysis and design of a short-pulse generator. It focuses on the utilization of step recovery diodes and reactance-based circuit elements. A model of the SRD for the use in simulation is tuned. A pulse shaping network (PSN) is designed, the properties of which are described via parametric analysis. Consequently, aiming at improving the output characteristics of the device, possible modifications to the circuit are explored, e.g., the inclusion of transmission line stubs. A PSN driver and supply circuits are designed. The pulse generator is powered by a battery, to comply with portability and energy self-sufficiency requirements. The properties of the manufactured generator are then tested via measurements.

KEYWORDS

impulse generator, ultra-short voltage pulses, dioda s krokovým zotavením, ultra-wide band, unipolar pulse

ABSTRAKT

Tato diplomová práce je zaměřena na analýzu a návrh generátoru krátkých pulsů. Při vypracování jsou pro tvarování pulsu využity step recovery diody a reaktanční prvky. Za účelem simulace je odladěn ekvivalentí model SRD. Je proveden návrh tvarovacího obvodu, jehož vlastnosti jsou popsány za pomoci parametrické analýzy. Dále jsou prověřeny možné úpravy zapojení, např. zahrnutí pahýlů přenosových vedení, za účelem zlepšení výstupních parametrů zařízení. Je navržen budící obvod tvarovače a obvod napájení. Aby zařízení vyhovělo požadavkům na přenosnost a energetickou soběstačnost, je napájeno z baterie. Vlastnosti vyrobeného generátoru jsou následně ověřeny měřením.

KLÍČOVÁ SLOVA

impulsní generátor, krátké napěťové pulsy, step-recovery diode, ultra-wide band, unipolární puls

SEDLÁČEK, Matyáš. *A short-pulse generator for UWB applications*. Brno: Brno University of Technology, Faculty of Electrical Engineering and Communication, Department of Radio Electronics, 2024, 84 p. Master's Thesis. Supervised by doc. Ing. Martin Štumpf, Ph.D.

Author's Declaration

Author:	Bc. Matyáš Sedláček
Author's ID:	221069
Paper type:	Master's Thesis
Academic year:	2023/24
Topic:	A short-pulse generator for UWB applications

I declare that I have written this paper independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the paper and listed in the comprehensive bibliography at the end of the paper.

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author's signature*

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ACKNOWLEDGMENT

I would like to thank the supervisor of my thesis, Dr. Martin Štumpf, for his valuable comments and advice.

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Introduction

This thesis concerns itself with the generation of wide band pulses. Its objective is to explore pulse generation using step recovery diodes and transmission lines. The outcomes of an initial feasibility study are used to design a pulse generator.

The device that will be developed within this research work is to be used as a standalone wide band pulse generator. The pulse generator is to be integrated in a measurement device that serves for non-invasive estimation of the electrical conductivity of tissue, a key parameter for designing on-body wireless interconnections. As such, the produced pulses should have a mathematically well definable shape for modeling and be distinctly separate, not interfering with each other. An important parameter is the pulse time width as it influences the physical dimensions of the measurement device. With the intended application in mind, we have set this parameter to 1 ns or more. Since the initial motivation for development is to replace an unwieldy and expensive piece of laboratory equipment, the device should be portable, energetically self-sufficient and reasonably low-cost.

The text that follows is divided into four chapters. The first chapter introduces the reader to the principles of generating wide band pulses. Here, a general structure of a pulse generator is described, including selected properties of step recovery diodes and their circuit models for transient analysis. Further, properties of pulse shaping networks utilizing these diodes are analyzed, including biasing, configurations, the inclusion of transmission lines and energy-storage elements. Finally, requirements on the driver are discussed. The second chapter specifies first how the diode model was tuned for its use in the chosen simulator. Subsequently, the results of simulation are used to provide a parametric study of the proposed generator. Finally, possible modifications based on the literature are tested and reviewed. The third chapter is a description of the design of the circuitry for the entire project and subsequent PCB design. The chapter is split into sections describing each module individually. The fourth chapter concerns itself with the measurement and analysis of the manufactured device, using the simulation results as a benchmark.

1 Principles of generating very short pulses

Very short electrical pulses are being utilized in many fields of engineering and science. As far as electrical engineering is concerned, one such field is the rather broad family of ultra-wide band (UWB) technologies. Applications of UWB stem from its key feature: a wide-band, noise-like spectrum in the frequency domain of a low power spectral density. From a communication standpoint, this enables UWB systems to co-exist with narrow-band ones in the shared frequency band without introducing mutual electromagnetic (EM) interference. In addition, the broad frequency spectrum of a short EM pulse plays an important role in inversion methods employing transient EM data, where the pulse distortion caused by its passing through an analyzed material sample provides the sample's EM properties in a wide band of frequencies. This is advantageous in radar technology, where shorter pulses lead to a higher spatial resolution. Accordingly, it follows that UWB technology relies on pulses with fast transition times and a low duration [1]. A method in this respect is described in the present chapter.

Pulse shapes

The Gaussian pulse with its first and second derivatives, which can be seen in Fig. 1.1 are the most commonly used pulse shapes in UWB-based communication systems, each with their own benefits. Given the fact that time-differentiated Gaussian pulses are mostly obtained by adding differentiators to a Gaussian-pulse generator, the generation of a Gaussian pulse requires the least complicated and most compact circuit.

Owing to its relatively low clutter level (meaning unwanted echoes due to multi-directional spreading) and high-resolution characteristics [2], the Gaussian pulse is also frequently employed in ground penetrating radar (GPR) applications.

Its first derivative, usually termed as monocycle, is very common in impulse radio or radar. It does not contain a DC component, which implies that less energy is wasted in converting it to a radiated EM wave at the antenna [3].

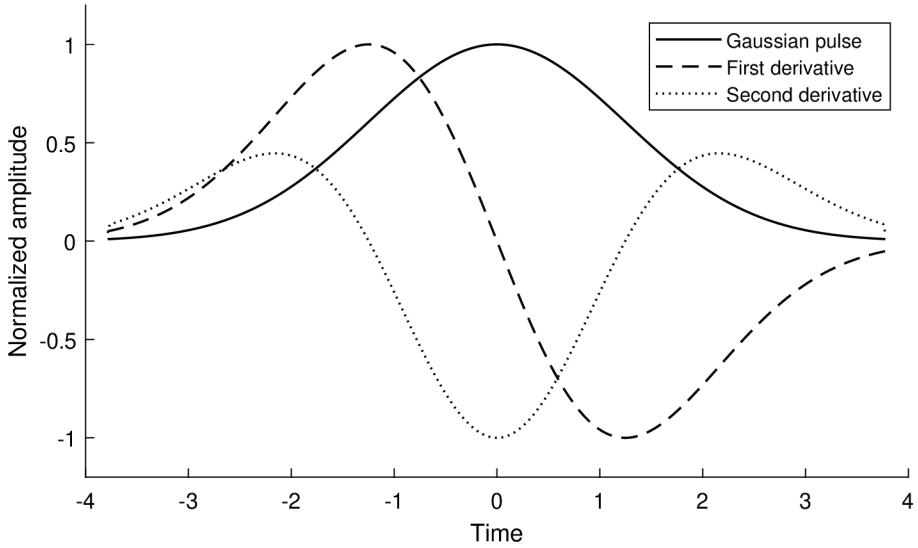


Fig. 1.1: Gaussian pulse and its first two derivatives

Pulse generator structure

A general pulse generator circuit consists of three main parts, which are depicted in Fig. 1.2. Here, for the sake of clarity, the differentiator is not a part of the pulse shaping network.

The first section is the **driver circuit**, which provides some form of time-varying voltage. In existing generator designs, the driver circuit dominantly generates a square wave produced by a clock oscillator (or a function generator if the design is not stand-alone) [4], a square wave with different rise and fall times [5] or a sine wave [6]. The driver should be able to handle sudden current draws from the following circuitry, otherwise it needs to be buffered.

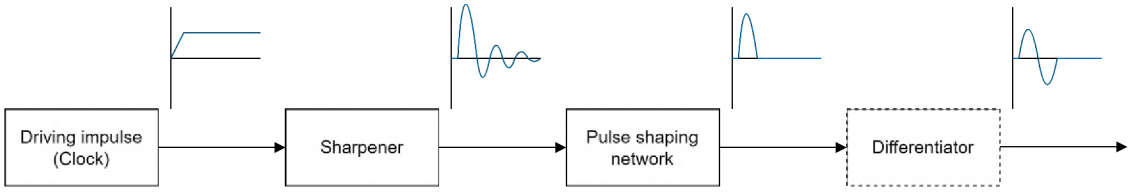


Fig. 1.2: Generalized structure of a Gaussian pulse (monocycle) generator

The next part is the **sharpener**, the purpose of which is to increase the slope of the rising/falling edge of the waveform coming from the driver. This is a crucial part of the generator, since the type of sharpener that is used determines a baseline for achievable output pulse properties, such as the pulse time width and its amplitude. The other blocks must be designed to be compatible with to the chosen type of sharpener. This is explored in more detail below, in the ensuing Sec. 1.1.

Obviously, devices which are used for sharpening the pulse edges are not ideal. Owing to parasitic effects due to surrounding circuit elements and the circuit board itself, the sharpener will produce pulses with undesirable traits. A typical unwanted effect is ringing that manifests itself by decaying oscillations of the pulse's trailing tail. It might also be the case that the pulse width or amplitude need to be modified to better fit the application at hand. The solution to both of these problems is the **pulse shaping network** (PSN).

1.1 Step recovery diodes

The pulse sharpener may be realized in various ways. Despite the existence of other options (e.g., vacuum tubes, mercury-wetted mechanical switches, non-linear transmission lines), we shall limit the scope of this work to designs based on semiconductor devices, the most common option in low power applications. The most popular semiconductor devices are: (a) tunnel diodes, that can achieve rise times of the order of tens of picoseconds with sub-volt amplitudes [7]; (b) avalanche transistors, with rise times in the range of hundreds of picoseconds and amplitudes in the range of tens of volts [7][8]. And, finally, (c) step recovery diodes (SRDs), which are capable of producing rise times in the range from high tens to low hundreds of picoseconds, with amplitudes of the order of volts and lower tens of volts [7][9]. This thesis focuses on the use of SRDs. For this reason, only SRD-based solutions are considered further.

The SRD (also known as the snap-off or charge storage diode) is a special type of silicon PIN diode, which finds its use in pulse sharpeners, comb generators, frequency multipliers and others. Static properties of SRDs are similar to those of a standard PN junction diode. The most important difference is in its dynamic behavior. Indeed, in contrast to standard diodes, it possesses the ability to very abruptly change its impedance on reversing the voltage bias. When the diode is forward biased and thus appears as a low impedance, charge is being stored inside the junction. This charge is in the form of minority carriers, that need a finite time to recombine. If the bias is reversed the diode still acts as a low impedance, thereby conducting electrical current. During this period, the stored charge starts to be depleted. Once the junction discharges completely, the diode will close abruptly, thus returning to its high impedance state. This causes the current to drop to zero in a very fast step [9].

Designing pulse sharpeners with SRDs relies on the knowledge of basic relations describing how the diode accumulates and releases charge. The two most important formulas, that have been presented in [9] and utilized in e.g. [3][10][11], state

$$\frac{t_S}{\tau} \simeq \ln\left[1 + \frac{I_F(1 - \exp(-t_F/\tau)}{I_R}\right] \tag{1.1}$$

where t_S is the time required to remove the charge stored by the forward current I_F, which has been previously applied for the duration t_F; I_R represents the constant reverse current, used to remove the charge. Furthermore, τ denotes the minority carrier lifetime, which is intrinsic to the diode. The other relation,

$$t_r = \sqrt{t_t^2 + (2.2R_{eq}C_{vr})^2}\,, \tag{1.2}$$

describes the dependencies between the transition rise time t_r, the intrinsic transition time of the diode t_t, and the circuit controlled rise time $(2.2R_{eq}C_{vr})^2$. This relation holds when the rise time is measured from 10%-90% of the edge. Next, R_{eq} represents the equivalent resistance of the surrounding circuit from the diode's perspective, and C_{vr} is the capacitance of the diode under reverse bias. Equation (1.2) therefore serves to isolate the effect that the external circuitry has on the pulse edge from what is contributed by the diode itself.

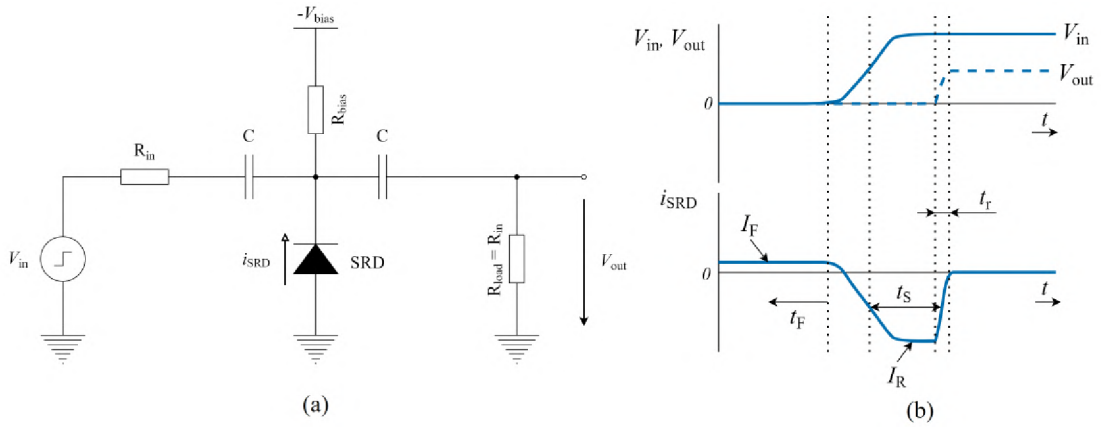


Fig. 1.3: Typical dynamic behavior of the SRD: (a) Demonstration circuit; (b) Current and voltage waveforms

The typical dynamic behavior of an SRD is represented in the waveforms of Fig. 1.3, corresponding to Eq. (1.1). In the given circuit, the fast transition of current through the diode also causes a corresponding transition of the output voltage. As far as the voltages are concerned, the effect appears like a shortening of the rising edge, as expected.

If the circuit design fulfills the condition $t_F >> \tau$, Eq. (1.1) can be simplified:

$$\frac{t_S}{\tau} \simeq \ln\left(1 + \frac{I_F}{I_R}\right)\,. \tag{1.3}$$

Equation (1.3) can be used to determine the maximum achievable pulse repetition frequency (PRF) of the generator. If the reverse-biasing voltage ends sooner than the charge is siphoned from the junction, the step transition cannot occur. Consequently, the generator will not produce an output. The equation is especially useful for simulations, since it allows for determining how to set the parameters of a model in order to match a real diode as specified by the manufacturer.

1.1.1 Modeling SRD behavior for transient analysis

The SRD is a non-linear device. While this makes it useful in the applications mentioned above, it also has an effect on how accurately can its behavior be represented in a SPICE based transient simulation. Traditionally, designs involving the diodes have relied on the iteration of manufactured prototypes. This has led to the development of several different ways to model SRDs in a computer-friendly manner [12].

Since the charge plays a key role in their behavior, the simplest way to model SRDs is by approximating their charge-voltage characteristic. The easiest solution would be to split the curve into two linear segments, thus describing the reverse and forward bias behavior separately. Then, the slope of each of the linear segments corresponds to a value of capacitance [13]. This way, unfortunately, presents problems in transient solvers, since the approximation is too crude. In particular, the piece-wise linear approximation is not continuously differentiable, which may lead to convergence difficulties. Another simple option is to use a model of the standard PN junction diode, but this approach does not account for the most important feature of the SRD – the step recovery. An improvement on the charge-voltage linearization technique, that makes it applicable in transient simulators, is described in [12]. While further possible improvements of the model have been suggested (see [21], for example), we shall employ the model implemented in ANSYS Designer, the numerical tool used in this thesis.

As mentioned in the previous paragraph, the idealized Q-V characteristic of the SRD can be represented by two capacitors, the values of which correspond to the slopes of the two linear segments: a large C_f for forward bias and C_r, that is smaller by several orders of magnitude. Here, C_r models the equivalent capacitance of the diode in reverse bias (not to be confused with C_vr, which is a parameter of the actual diode). The value of C_f for a given diode can be determined indirectly from measurement. A simple way of doing this is possible thanks to the following relation [13]:

$$\tau = C_\mathrm{f} R_\mathrm{f} \tag{1.4}$$

where τ is the minority carrier lifetime and is treated as the time constant of an RC circuit, where R_f denotes the resistance of the PN junction when forward biased. Its value is typically less than 1 Ω and can be determined from the V-A characteristic of the diode as its dynamic resistance [10][12]. If R_f is known beforehand (using a datasheet as provided by the manufacturer, for instance), then C_f could be determined via simulation of a test circuit.

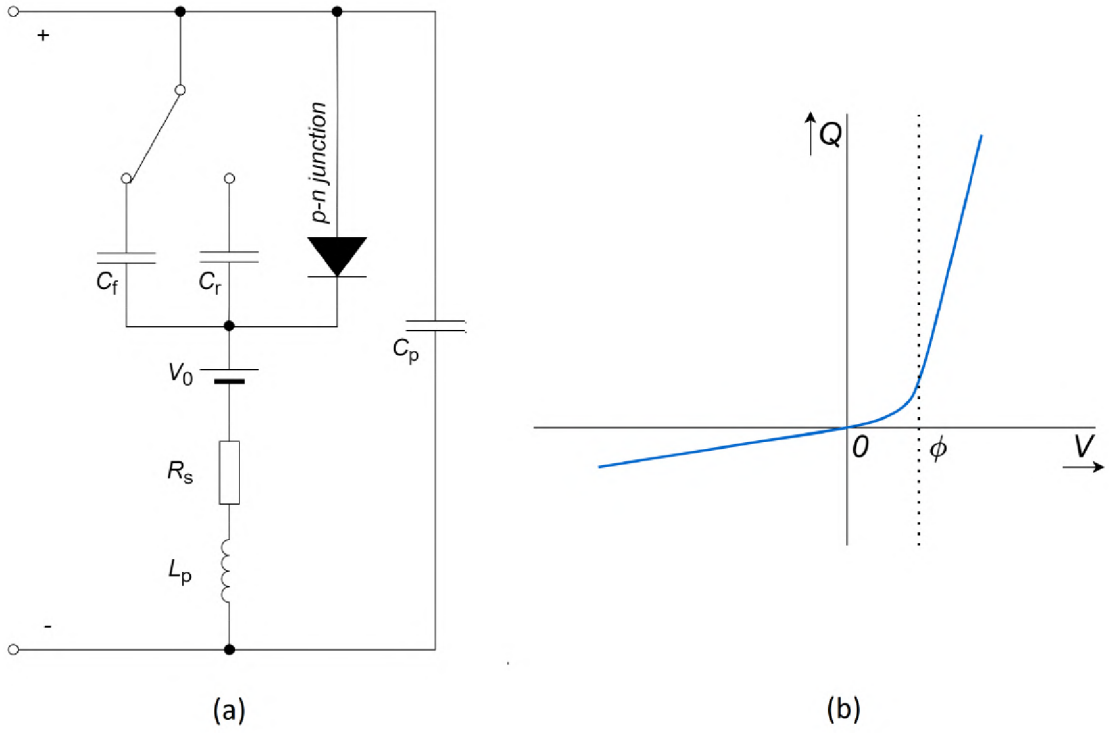


Fig. 1.4: The SRD model proposed in [12]: (a) Equivalent circuit; (b) Charge-voltage characteristic

An improvement of the linearised model comes in the form of a parabolic curve in the transition region that joins the two straight lines. The corresponding mathematical description reads as [12]:

$$Q(V) = \begin{cases} C_\mathrm{r} V, & \text{for } V \leq 0 \\ \dfrac{C_\mathrm{f} - C_\mathrm{r}}{2\phi}\left(V + \dfrac{C_\mathrm{r}\phi}{C_\mathrm{f} - C_\mathrm{r}}\right)^2 - \dfrac{C_\mathrm{r}^2 \phi}{2\left(C_\mathrm{f} - C_\mathrm{r}\right)}, & \text{for } 0 < V \leq \phi \\ C_\mathrm{f} V - \dfrac{\left(C_\mathrm{f} - C_\mathrm{r}\right)\phi}{2}, & \text{for } V \geq \phi \end{cases} \tag{1.5}$$

where ϕ represents the contact potential. The corresponding curve can be seen in Fig. 1.4 (b). In the same figure, part (a), we show the full equivalent model of the SRD proposed in the paper. It accounts for the behavior described above: the two

switched capacitances for the different bias modes and the corresponding PN junction. The model also includes additional parameters for a more accurate simulation: L_p and C_p, components representing the parasitic inductance and capacitance due to the package. Further, the resistor R_s represents the diode series resistance and V_0 models for the contact potential.

1.2 Pulse shaping network

The voltage impulse that is produced by the SRD might have undesired properties. When one aims for the generation of a single impulse, a typical unwanted effect is ringing. The pulse might have an unsuitable rise/fall time, duration or even shape. All of these pulse parameters depend on the intended application of the generator. Consequently, designs of PSNs vary across the available literature.

Biasing, diode configurations and removing ringing

The main requirement for a functional generator is to make the SRD undergo reverse recovery. There are several options to achieve this. The most straightforward way is to use a forward biasing DC voltage source, which also sets the current through the SRD. The diode then requires to be triggered by a unipolar input pulse, which has the opposite polarity. Let us consider, for example the circuit shown in Fig. 1.3. Here, the diode is forward biased by a negative voltage and, consequently, its reverse bias is achieved by a positive voltage pulse. A similar line of reasoning applies to the opposite case. Examples of such circuits can be found in [5][14][15].

Another option for biasing is to leave out the biasing DC source entirely. In this approach the diode is driven by a bipolar input waveform. The advantage lies in requiring less components and also not having to introduce an external DC voltage to the PSN. The disadvantage of this approach is the need for an extra (finely tuned) matching circuit at the diode input. The matching circuit has to be designed with regard to the minimization of the SRD's response to the opposite input slope and the pulse ringing. Another issue is that the currents through the diode in both bias regimes are, unlike with the DC bias option, not set separately. Consequently, the designer has less control over the diode's behavior than when using the traditional DC bias approach. This type of circuit has been shown and its properties explained in, [4], [16], for example.

In a circuit with a single diode, the rising edge of the pulse is directly driven by its transition. The falling edge occurs when the diode presents as a high impedance. Therefore, the voltage drop in the node of the diode experiences different conditions

from the voltage rise. For a case without ringing, this can manifest in a comparatively lower slope in the lower parts of the falling edge [17]. This is illustrated in Fig. 1.5 (c). One possible way to symmetrize or shorten the pulse is to use a combination of two diodes. The second one must be connected so that it will be able to speed up the drop of voltage in the node. For a PSN based around an SRD connected in parallel, this means connecting the secondary in series, as in 1.5. It also has to have a delayed step response relative to the first diode, otherwise it will only shorten and attenuate the pulse. An example circuit, inspired by [14][18] is shown in Fig. 1.5 (a), where R_d is used to limit the discharge current through the second diode, thus delaying its step recovery by a time t_d as shown in Fig. 1.5 (c). Note that pulse shaping in this way comes at the cost of amplitude.

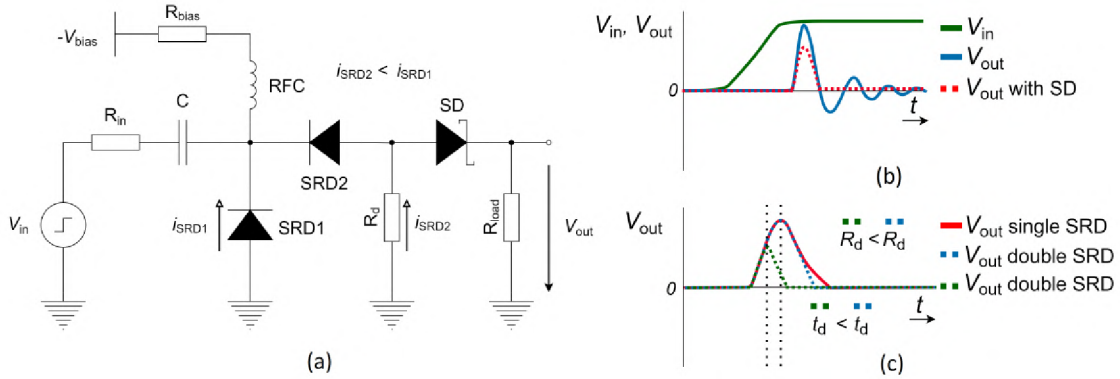


Fig. 1.5: (a) Example circuit utilizing two SRDs and a rectifier at the output; (b) Effects of the rectifier; (c) Output voltage waveforms for the double SRD circuit

Ringing is usually introduced to the output when the sharp transition of current and voltage due to the diode triggers dampened oscillations in the (parasitic or intentionally placed) inductances and capacitances in the circuit. When the amplitude of the ringing is relatively small compared to the main impulse, the most common way of suppressing the ringing effect involves the use of a rectifier, usually in the form of a series Schottky (sometimes PIN) diode as the last stage of the PSN. This is the reason why the Schottky diode is present in the circuit diagram in Fig. 1.5 (a). The rectifier approach is widely utilized (see [3][14][16][18], for example). This solution comes at the cost of amplitude, since the diode is set up to cut off the lowest part of the pulse, where the problem is most prevalent. This is illustrated in Fig. 1.5 (b). If the ringing has a comparatively large amplitude to the main pulse, the circuit design has to be modified with regard to the impedances of connections between the elements as well as particular L and C values. Then the output should

be rectified as well [3][5]. If the amplitude of the ringing is not reduced enough, it may occur in the output signal, even when the Schottky diode is applied [19].

Using stubs to manipulate pulse properties

Transmission line stubs are frequently employed to manipulate the pulse properties. The stubs are commonly terminated by a short circuit and used to delay and invert the reflected pulse, that is subsequently combined with the incident one. Concerning a PCB trace, the pulse propagates along the line at a wave speed that depends on the effective permittivity of the dielectric substrate. As far as the reflected pulse is concerned, it is necessary to account for its two-way travel time. Therefore for a given value of time delay t_{delay}, the length of the stub can be obtained from:

$$l_{\text{stub}} = \frac{t_{\text{delay}} c}{2\sqrt{\epsilon_{\text{reff}}}}. \tag{1.6}$$

The time delay has a strong impact on the output pulse shape. For very short delay times, which are half of the pulse duration, the effect is a sharpening of the falling edge of the output [16]. To minimize losses and pulse distortion, the stub should be placed as close as possible to the sharpener. Since the pulse that is produced in this way is a (slightly deformed) monocycle, this has to be combined with a rectifier for a unipolar output, as seen from the circuit shown in Fig. 1.6 (a). Therefore, a significant overshoot into negative voltage values is present (when the incident is negative, then the overshoot is positive) as illustrated in Fig. 1.6 (c). Since the rectification results in an amplitude decrease, the use of the rectifier is another reason to keep the sharpener and stub close together.

For longer time delays with duration of about the incident pulse time width, the stub effectively behaves as a differentiator (e.g., for a Gaussian incident pulse the output corresponds to a monocycle). As a general rule, the longer the pulse is, the worse does a distributed element solution work, since the reflection line needs to increase in its length. To minimize distortions caused by multiple reflections in the circuit [4][14], the differentiator is usually the end stage of the PSN (see Fig. 1.6 (a)). An example of the monocycle output voltage pulse is shown in Fig. 1.6 (c).

If the line is any longer than the spatial support of the incident pulse, the incident and reflection pulses will separate, which is not desirable. In addition, it is important to keep in mind that a longer travel time implies higher attenuation and stronger distortion of the signal. On top of these effects, a longer transmission line stub requires a larger PCB. As these unwanted effects depend on the type of transmission line, the use of a low-loss and high-quality substrate will lead to their mitigation. A purely planar design starts to become impractical for longer pulse lengths, and the stubs might have to be made from a shorted coaxial cable or replaced by discrete

elements. It is worth noting that for sub-nanosecond pulses, discrete elements would introduce stronger rising edge degradation (lengthening and distortion) compared to the distributed solution [11][16][18].

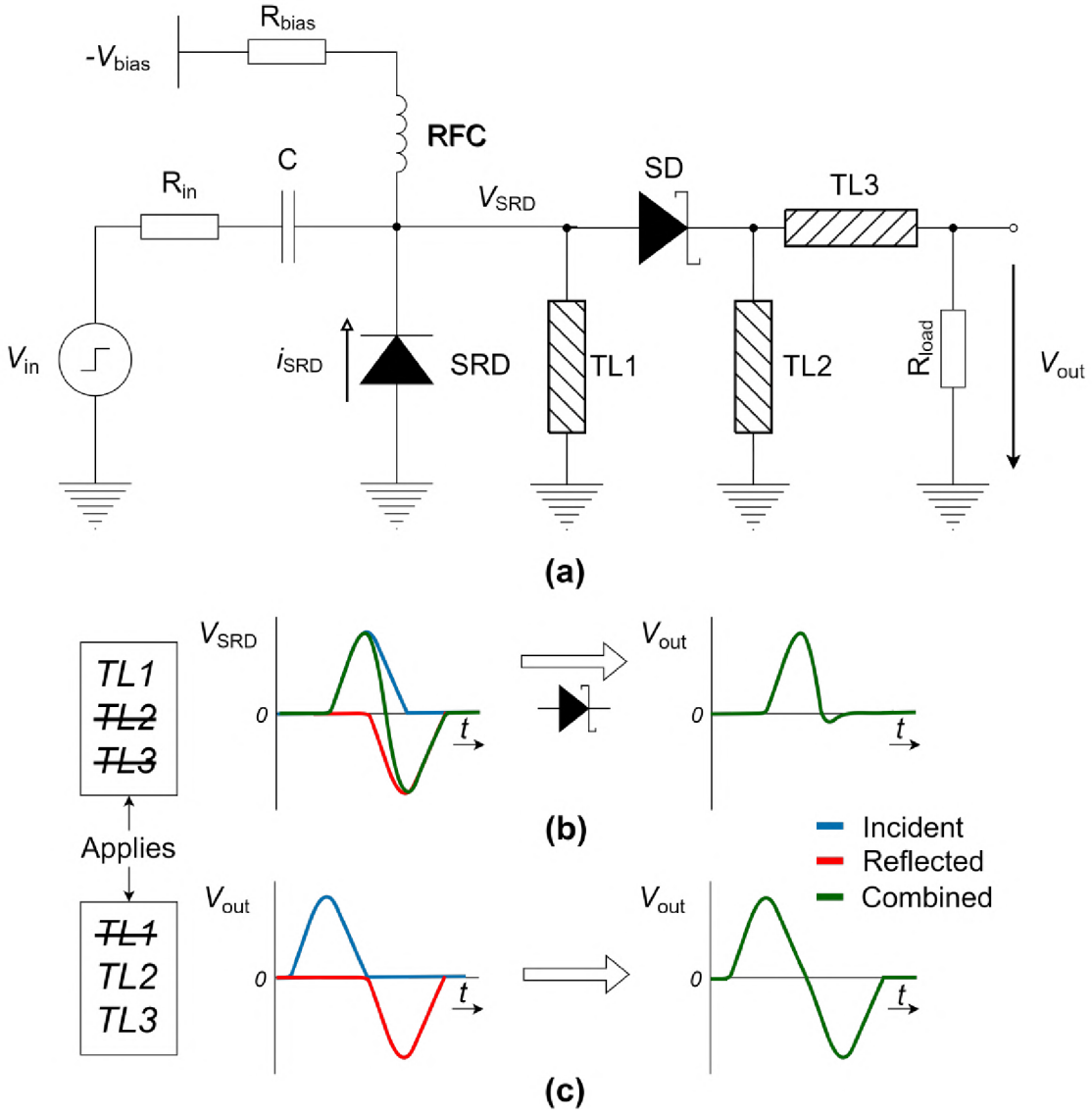


Fig. 1.6: Example circuit (a) for: (b) using a shorted stub to sharpen the falling edge or (c) differentiate the pulse

Multiple reflections within the PSN should be avoided. The undesired effects range from ripple and pulse distortions caused by shorter signal paths to a trail of separate pulses behind the initial one for longer paths. To minimize these unwanted phenomena, the impedance of the transmission lines can be optimized. Since the pulses are wide-band and the impedances in the network change during the generation of the pulse (the impedances variations are attributed to the SRD and to the rectifying Schottky diode, if present), this is not a straightforward process in a

common SRD based circuit. Most designs cited in this work opt for standard 50 Ω lines, but if necessary, optimization of individual segments can be achieved using computer assisted design (CAD) [5].

Energy-storage elements

It is possible to utilize capacitors and inductors to help in manipulating the width and amplitude of the pulse. Let us consider that the circuit shown in Fig. 1.3 would have a small inductor connected between the time-varying input and the SRD node. The abrupt change in the SRD's impedance will cause a cutoff in the current through the inductor, which will contribute to the voltage spike created at the diode node [3]. A similar principle applies to a small capacitor connected in parallel to the diode node. Its value will add to the SRD capacitance, which will slow down the rise time of the diode, thus increasing the width of the produced impulse. Since such a capacitance will be very small (comparable to C_r from Sec. 1.1.1) it can therefore be difficult to implement it properly on the actual PCB.

The value of energy-storage elements has to be tuned. Low values will tend to produce ripples in the pulse through interactions with parasitics in the circuit. On the other hand, relatively high values will effectively filter out the produced pulse [9].

1.3 Driver circuit

The rest of the circuit needs a voltage edge to act on. Ideally, it should be as short as possible and at the same time, the active voltage level should be held long enough for the SRD to discharge. This naturally leads to a square wave input being the most common choice, as in [4][14] or [15] and many others. However this does not mean that it is exclusively the case, and other approaches, like a sine wave input have been shown to work, for example [6].

Another important factor to be considered is that when the diode is conducting in reverse bias, the current draw will increase and this current will flow from the source of the highest voltage in the circuit at the time, the driver. This implies that a standard chip square wave clock oscillator is not sufficient for providing the needed power. An inclusion of a buffer in some form and a current limiting resistor is therefore necessary [14][16][17].

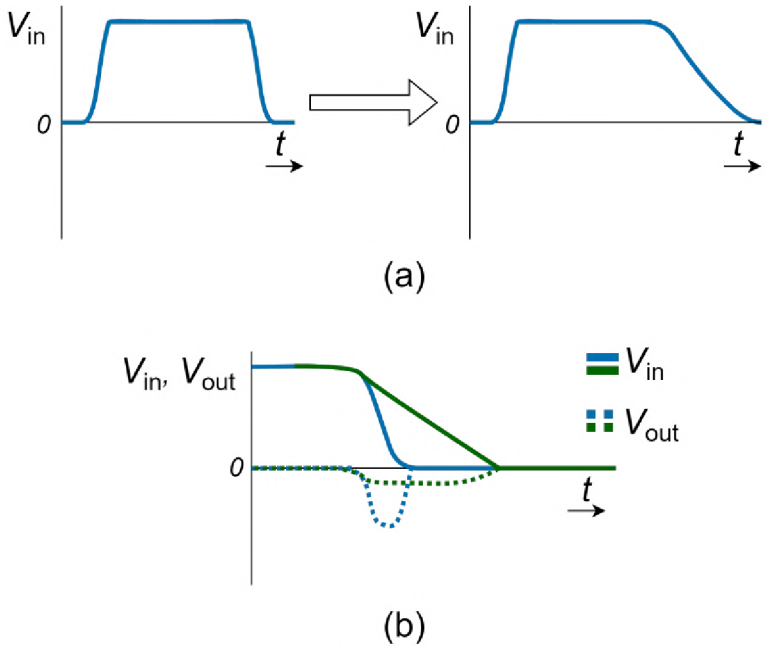


Fig. 1.7: (a) Change of the input pulse for decreasing output voltage overshoot at the falling edge (b) Effect of increasing the input fall time on the output

For the type of PSN that has been shown in Fig. 1.6 (a), a problem can occur at the falling edge of the input waveform. It produces a voltage inverse to the main pulse at the output, see Fig. 1.7 (b). The voltage level of this distortion is proportional to the falling edge slope, its width is inversely proportional to the same [14][20]. A possible improvement to the driver can therefore be made by stretching the falling edge of the square wave signal as shown in Fig. 1.7 (a). That can be done, for example, by driving a buffering stage of the driver with a mono-stable circuit triggered by the clock oscillator. This was the approach adopted in [14][20]. The fall time should not be increased to the point that the falling edge would stretch beyond a half of the period of the original square wave.

2 Simulations and analysis

In order to create an accurate setup for simulating the chosen generator structure, the concepts from the previous chapter are applied here. In this chapter we provide a description of how the design has been adapted in several iterations to best fit in the intended application. The simulations have been performed in ANSYS Designer.

2.1 Tuning the SRD model

To achieve reasonably accurate results when simulating the PSN design, an accurate model of the utilized SRD has to be used. The simulation tool of choice offers a framework for such a model, but its parameters have to be determined based on a specific diode. SRDs are not a particularly common component in modern designs, although there has been a resurgence in their use with the development of compact UWB devices. This makes finding commercially available options challenging and costly. Currently, only one manufacturer, MACOM, provides a selection of these devices. From a cost perspective, only one product presents a reasonable choice: the diode MA144769-287. All their other SRDs are presently priced five to six times higher, with availability being an issue.

The model framework included in ANSYS is a combination of the standard SPICE PN junction diode model, including breakdown voltage, and the charge-capacitance model as described in Sec. 1.1.1. Basic parameters from the provided datasheet [22] can be used directly (e.g. reverse breakdown voltage), while others (area junction grading coefficient M, emission coefficient N, for example) have been obtained from the manufacturer's web page, where parameters for a SPICE model along with package parasitics are provided [23].

The values of C_f and C_r have been set by simulating the circuit shown in Fig. 1.3 with $R_\mathrm{in} = R_\mathrm{load} = 50\,\Omega$ and tuning their values until τ and t_t matched the datasheet maximum values, which are given as 50 ns and 150 ps, respectively. In this approach, τ and t_t need to be calculated indirectly using Eqs. (1.3) and (1.2), respectively. The simulated waveforms used to determine the desired capacitance values can be seen in Fig. 2.1. After performing the calculations (for $t_\mathrm{S} = 34.18$ ns; $I_\mathrm{F} \simeq I_\mathrm{R} \simeq 40$ mA), from (a) we get $\tau = 49.31$ ns, which corresponds to $C_\mathrm{f} = 1.8$ nF in the model. Similarly from (b), the expected rise time for a diode with $t_\mathrm{t} = 150$ ps in this circuit ($R_\mathrm{eq} = 25\,\Omega$, $C_\mathrm{vr} = 0.9$ pF [23]) is around $t_\mathrm{r} = 160$ ps, which is reflected in the model with $C_\mathrm{r} = 3$ pF.

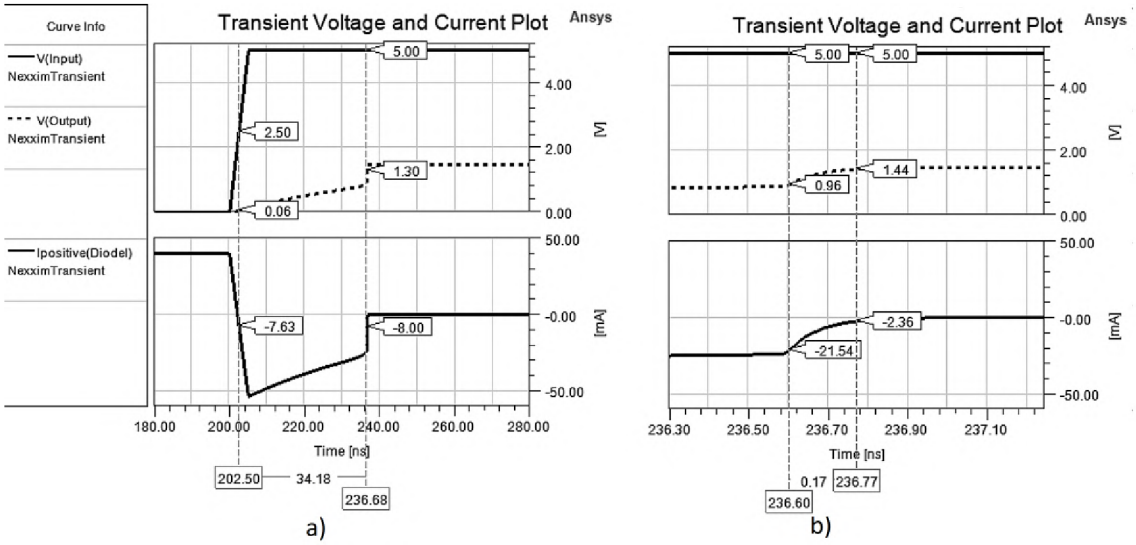


Fig. 2.1: Voltage and current waveforms used in tuning the model: a) time to discharge the diode junction t_S; b) rise time t_r

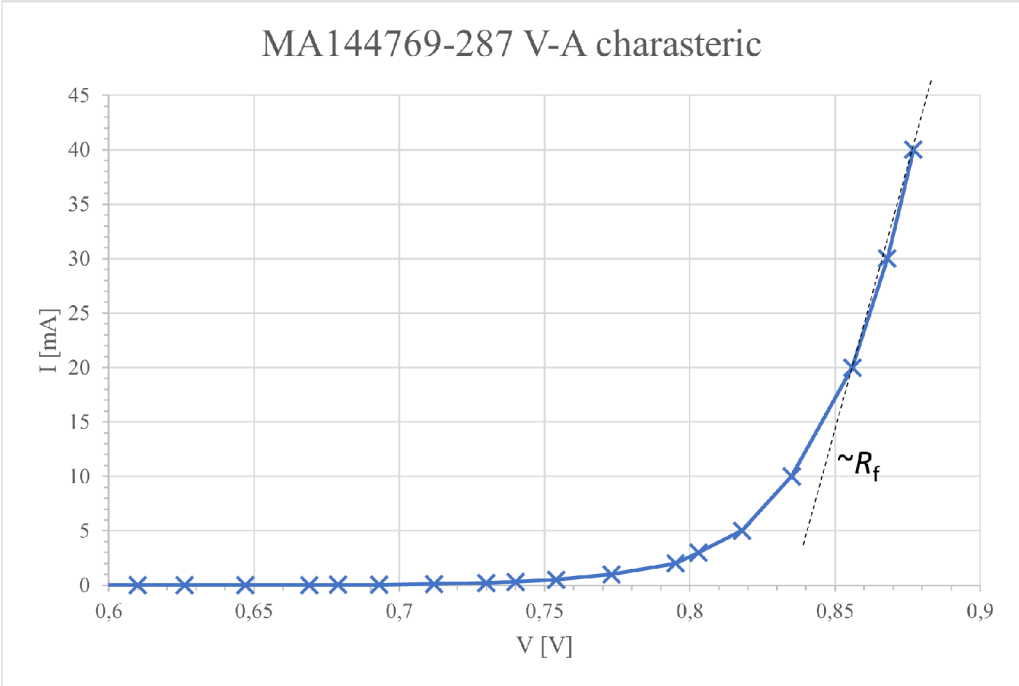


Fig. 2.2: Measured V-A characteristic of MA144769-287

The value of R_f was verified further by measuring the V-A characteristic of the used diode (see Fig. 2.2). The measurement was carried out using a TESLA BM529 transistor tester. The value of the diode forward resistance is the slope of the characteristic in forward bias, which for the actual diode is $R_\mathrm{f} \simeq 1.05\,\Omega$. The obtained value is comparable to $0.8\,\Omega$ provided by the manufacturer and is therefore acceptable for simulations.

Based on the above, the final model parameters are summarized in Table 2.1. Note that the table does not contain parameters influencing temperature dependent effects. That is because the presumed temperature for all simulations is $T_\mathrm{nom} = 25\,°C$.

Tab. 2.1: Relevant parameters for the model of the MA144769-287 SRD

Parameter	Name	Value	Unit
C_f	Forward bias capacitance	1.8	nF
C_r	Reverse bias capacitance	3	pF
R_s	Diode series resistance	0.8	Ω
I_s	Saturation current per unit area	2.3	fA
N	Emission coefficient	1.1	[-]
I_VB	Current at breakdown voltage	10	μA
V_B	Reverse breakdown voltage	30	V
FC	Forward bias depletion capacitance coefficient	0.5	[-]
V_0	Built-in junction potential	0.4	V
M	Area junction grading coefficient	0.2	[-]
EG	Energy gap for PN junction	1.11	eV

2.2 Analysis of the PSN

The analysis of the designed PSN starts from an idealized initial working solution and optimizing it for better performance, examining possible improvements based on Chapter 1 and then adding parasitic values as well as microstrip lines to better reflect real conditions.

2.2.1 The simulation setup & the ideal case

The simulations are performed using the transient solver as implemented in ANSYS Designer. The input pulse source is set to begin after a 50 μs delay and the traces are being observed after several hundred input signal periods, so that the transient effects can fade away and to ensure that the output is stable. To simulate for sub-optimal conditions with a possible cost reduction if feasible, the chosen substrate for the simulation is FR4. Its relative permittivity $\epsilon_{\mathrm{r}} = 4.4\,[-]$, and its thickness of 60 mil.

The initial ideal circuit used can be seen in Fig. 2.3, and the waveforms at the indicated voltage probes are shown in Fig. 2.4. It is based around a parallel SRD biased by a -5 V DC voltage source, which is separated from the rest of the circuit by an RF choke in the form of an inductor $L_{\mathrm{bias}} = 10\,\mu$H, and a bypass capacitor $C_{\mathrm{bias}} = 100\,$nF. The biasing current is set by the resistor $R_{\mathrm{bias}} = 170\,\Omega$ to roughly 30 mA. This value can be raised to make the SRD store charge faster and is in direct proportionality with the pulse amplitude.

The circuit is driven by a pulse voltage source, which represents a chip clock oscillator driving a current buffer (the specific ICs mentioned below are subject to change in a subsequent stage of the circuit's design). The oscillator is set to a square wave of frequency $f_{\mathrm{PRF}} = 10\,$MHz, which gives the diode enough time to recover. The maximum PRF can be determined from Eq. (1.3). For the present circuit with $I_{\mathrm{R}} \simeq 5I_{\mathrm{F}} \simeq 150\,$mA (see Fig. 2.7), which implies $t_{\mathrm{S}} = 9\,$ns, its value is about 55 MHz for a 50% duty cycle square wave. The input voltage levels are $V_{\mathrm{HIGH}} = 5$ V and $V_{\mathrm{LOW}} = 0$ V. The rise/fall time is $t_{\mathrm{r,f}} = 10\,$ns, respectively. The values are set this way to imitate the crystal clock oscillator 830202536501 from Wurth Elektronik [25].

The value of R_{buffer} comes from the datasheet value of the output impedance of the high-speed buffer BUF634A from Texas Instruments [26](for which we were unable to obtain a functioning model to use in simulations). It can provide a continuous output current of 250 mA, so it would be able to effortlessly supply the spikes in current draw of the PSN when the diode is conducting in reverse. It has a slew rate of 3.75 V/ns, so it should be able to reliably transfer the input voltage with its

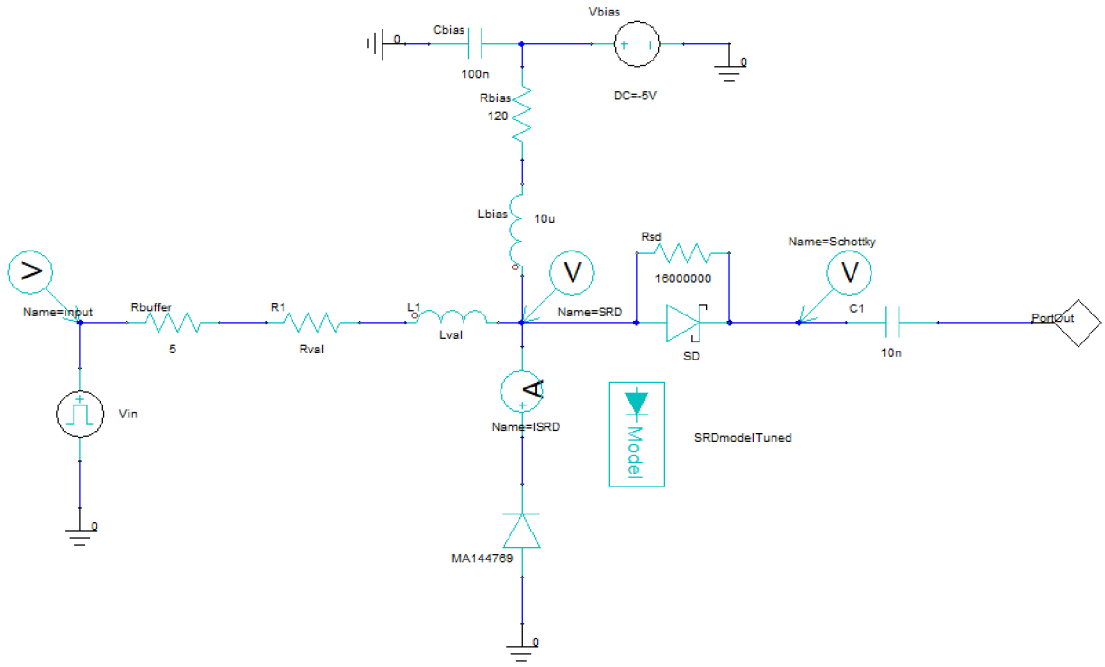


Fig. 2.3: The initial ideal circuit for the PSN used in simulations

0.5 V/ns. The only issue might lie in its gain bandwidth product (GBW), which is 240 MHz. The buffer's output headroom to supplies (the voltage difference between supply and output voltage) is 2.5 V at maximum current and this will have to be taken into account when designing the driver, even though the maximum current will only be a short peak, not a steady draw.

The output of the PSN has a DC blocking capacitor $C_1 = 10\,\text{nF}$, the purpose of which can be observed by comparing the voltage traces *V(Schottky)* and *V(PortOut)* from Fig. 2.4. The PSN is terminated by a 50 Ω load.

The most important components from the perspective of output pulse properties are: (a) R_1, which is a current limiting resistor that affects how fast the diode discharges. It has an impact dominantly on the pulse amplitude and t_S; (b) L_1 has a two-fold purpose. Firstly, it allows the low frequency components from the driver to pass to the SRD and prevents the high frequency components formed in the PSN from propagating backwards. It impacts pulse amplitude and pulse width, while simultaneously also influencing t_S; (c) SD is the Schottky diode used to rectify the pulse and thus remove ringing.

The Schottky diode SPICE model used in this simulation is based on the BAT15 family and is made by Infineon, who provide the model on their website [24]. The value of R_{SD} in Fig. 2.3 is based on the manufacturer's recommendation. Its impact

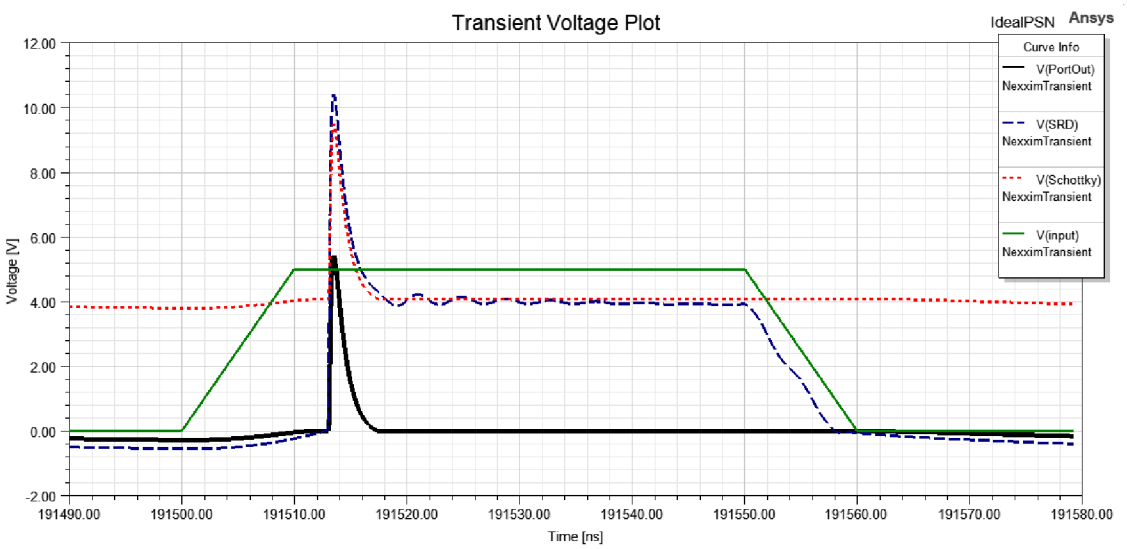


Fig. 2.4: The voltage waveforms present in the PSN design from Fig. 2.3 for a single repetition cycle

on ringing removal can be seen by comparing the traces *V(SRD)* and *V(Schottky)* in Fig. 2.4.

The impact of R_1 and L_1 can be demonstrated using the simulation tool. From Fig. 2.5 it can be seen that an increase to L_1 delays the step response of the SRD and increases the pulse amplitude. A key feature for the target application is that the pulse width is increased via an extension of the falling edge. This transforms the Gaussian pulse to the shape of a double exponential. At the same time, the higher the value of L_1, the higher is the negative output voltage dip due to the falling edge.

A value that seems to be a good compromise of all of the above is $L_1 = 100\,\text{nH}$, which is to be used further on. For this value, the full width at half maximum (FWHM) is 1.37 ns, a notable increase over f.e. 340 ps for $L_1 = 10\,\text{nH}$.

Concerning R_1, at first glance it might appear that the lowest value would be best, but Fig. 2.6 demonstrates, that for a value that is too low, here $R_1 = 5\,\Omega$ for example, the SRD triggers too early and this comes at the cost of a drop in pulse amplitude. Apart from that, an increase to R_1 leads to a reduction in amplitude as well. Since the diode can at most dissipate 250 mW of power, this might be necessary. A conservative value $R_1 = 20\,\Omega$ was chosen as a starting point for the purposes of keeping the simulation close to reality. This value will most likely have to be tuned on the actual circuit board.

Concerning currents in the circuit, for the given configuration, we expect a peak current through the SRD of 150 mA and a peak current drawn by the entire PSN of 200 mA, see Fig. 2.7.

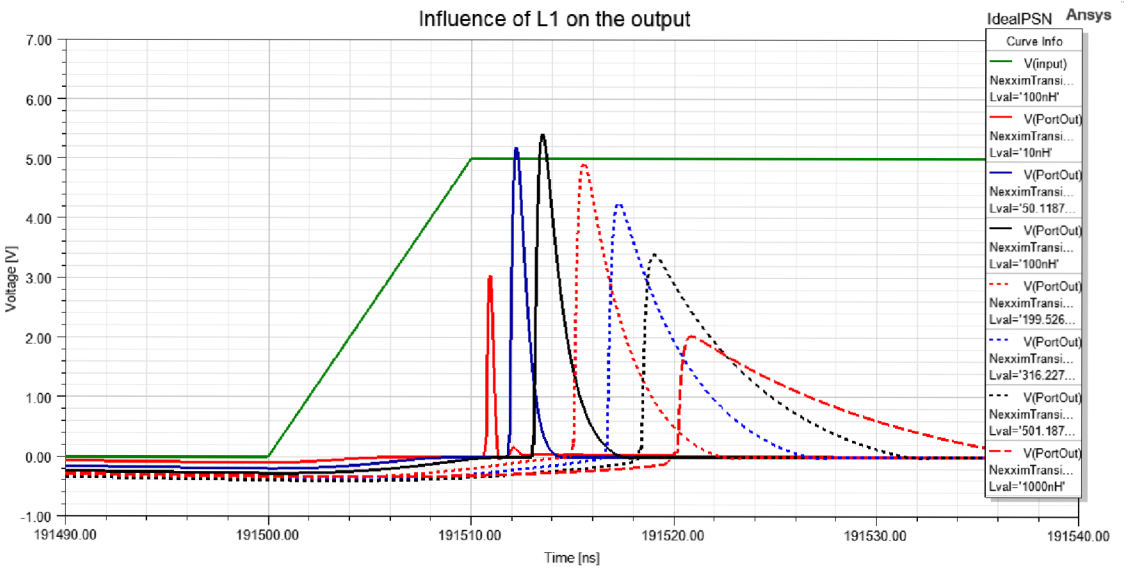


Fig. 2.5: The impact of the series inductance value L_1 on the output pulse in circuit from Fig. 2.3; $R_1 = 20\,\Omega$, all L_1 values in nH

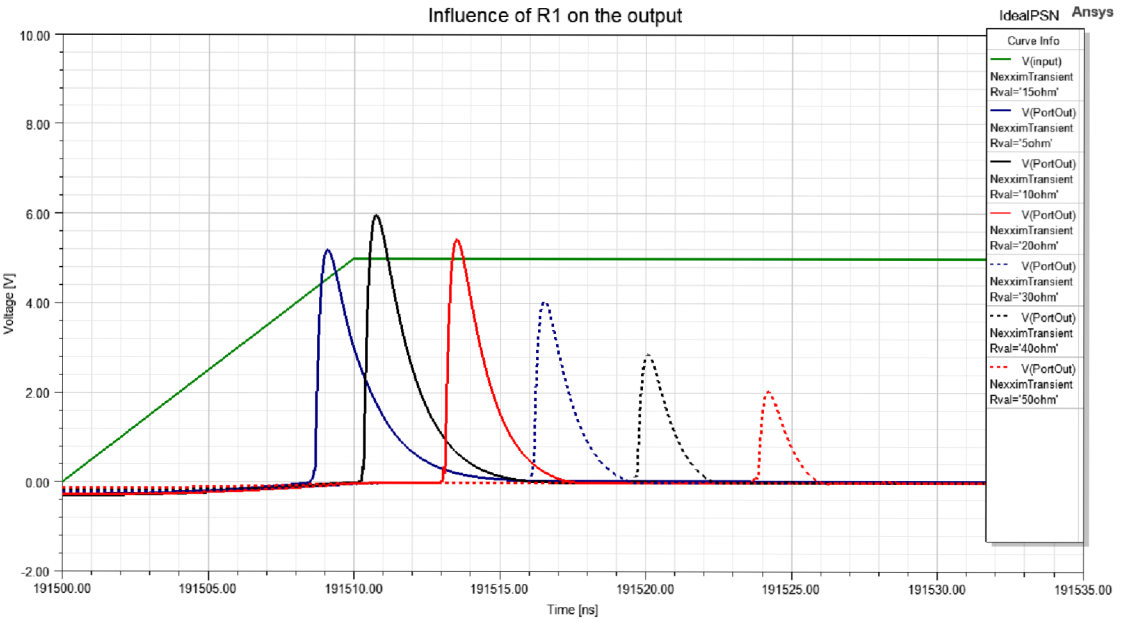


Fig. 2.6: The impact of the current limiting resistance value R_1 on the output pulse in circuit from Fig. 2.3; $L_1 = 100\,\text{nH}$, all R_1 values in Ω

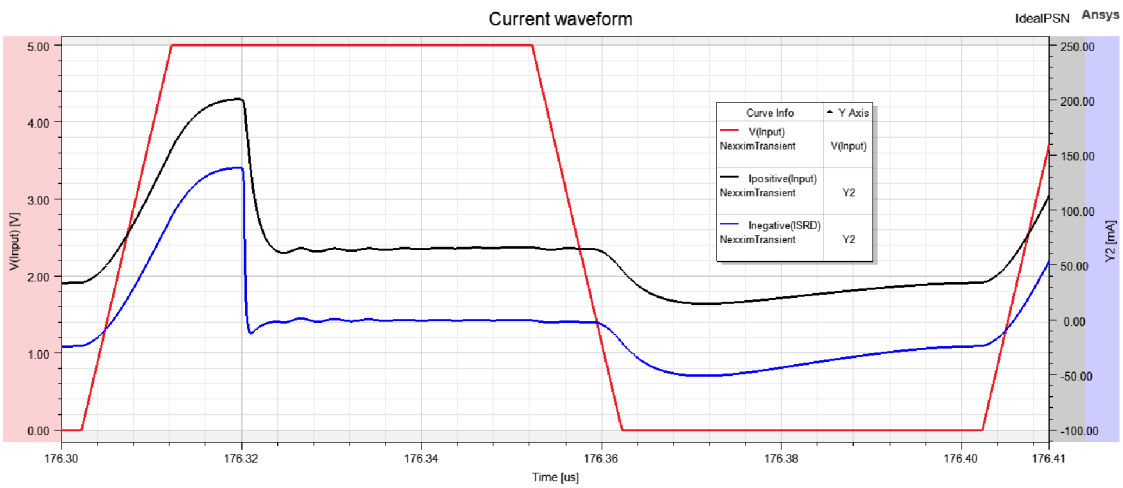


Fig. 2.7: Current drawn by the PSN over a single period

Accounting for real world influences

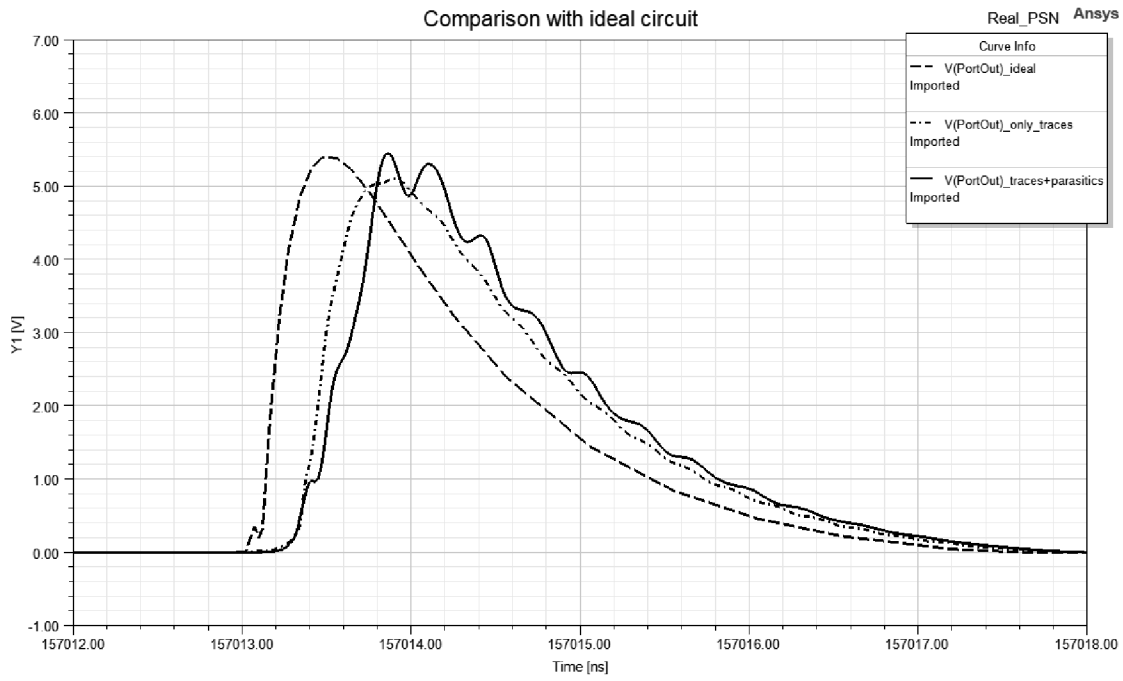


Fig. 2.8: Comparison of ideal and parasitic effects included output pulse

Transmission lines in the form of microstrips are added to the simulated circuit. The same applies to the package parasitics of the SRD as well as the Schottky diode. The full circuit used in simulations is shown in Fig. 2.9. The characteristic impedance of 50 Ω proved to be sufficient for the signal part of the circuit. The DC biasing part is connected by a very thin trace, 0.3 mm, since this will help it work as

an RF choke. At this stage of design, the lengths of microstrips were estimated to mimic typical distances in such layouts, but they may change later. The produced output pulse is affected by a superimposed parasitic oscillation (see Fig. 2.8). In the simulation model we used ideal inductances. Since package parasitics usually show a low quality factor, it is anticipated that the observed ripple will be reduced in the actual design.

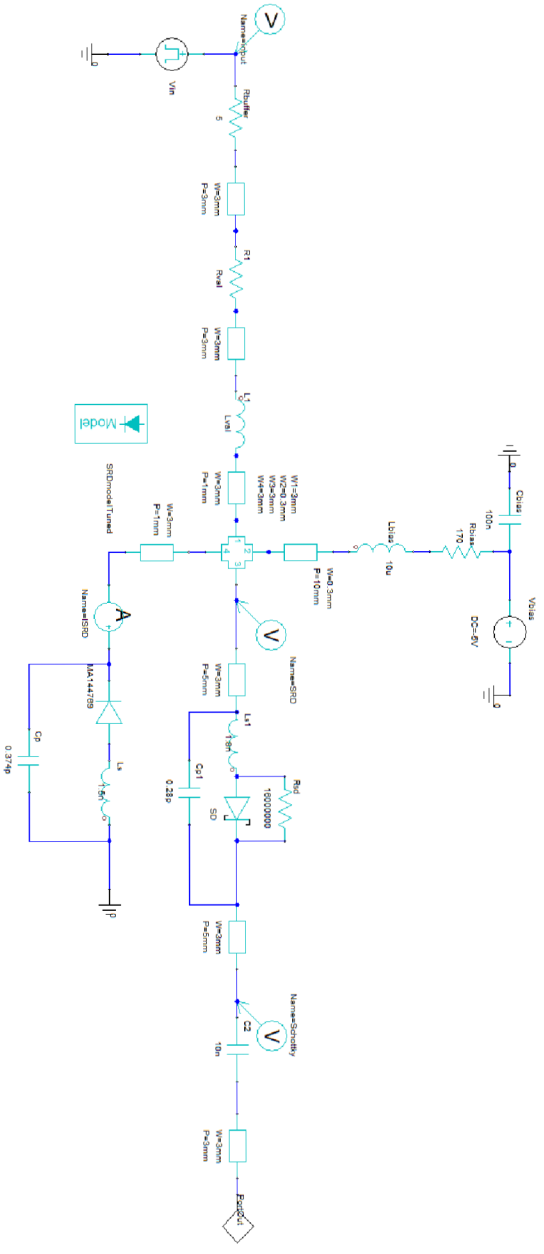


Fig. 2.9: Schematic of the PSN with transmission lines and package parasitics

2.3 Possible modifications and improvements

Based on the methods described in the available literature on the subject (see Chapter 1), this section focuses on examining the viability of modifications to the proposed circuit.

Shorted stubs realized via microstrip lines

As the intended application of the generator does not call for a monocycle pulse, we opt for a unipolar output. The reason being simply a less complex board layout and tuning process.

What is worth to investigate is the use of a shortened stub to manipulate the pulse length and its falling edge. To this end, the stub needs to be connected to the same node as the SRD. Consequently, we have to incorporate a blocking capacitor that prevents the stub from forming a short circuit to ground. Best results were obtained by using a combination of two capacitors, one directly on the signal path, and one in the reflecting branch, as seen in Fig. 2.10. The stub dimensions which produce the waveforms shown in Fig. 2.11 are $L = 42$ mm and $W = 3$ mm. Using Eq. (1.6) and accounting for the FR4 substrate ($\epsilon_\mathrm{r} = 4.4$), the corresponding round trip time is approximately $t_\mathrm{delay} = 0.52\,\mathrm{ns}$. This is the largest value of delay that was achievable without introducing spurious pulses of amplitude that is comparable to the main one. Since a longer delay line corresponds to a larger pulse width, this means that it would not be possible to achieve a clean pulse of the needed 1 ns duration in this PSN structure. The pulse had, indeed, been shortened when compared to the original from Fig. 2.8, from a FWHM of 1.37 ns to 0.47 ns. Furthermore, the amplitude has decreased substantially, from 5 V to 1 V in the ideal case and to only 0.5 V with the inclusion of transmission lines. Also, it has been shown that it is possible to increase the slope of the output falling edge in this way. Accordingly, this modification can be useful for a PSN that uses a sharpener with a longer transition time than used here.

The most obvious issue of this modification is that in order to not interfere, both added capacitors have to be set to 10 pF (see Sec. 1.2), which is a very small value for an accurate physical implementation. This is illustrated in Fig. 2.11 by comparing the traces with and without the inclusion of parasitic values. The capacitor values are low enough to produce oscillations when interacting with the parasitics. These oscillations are substantial enough that the intended pulse shape completely distorts.

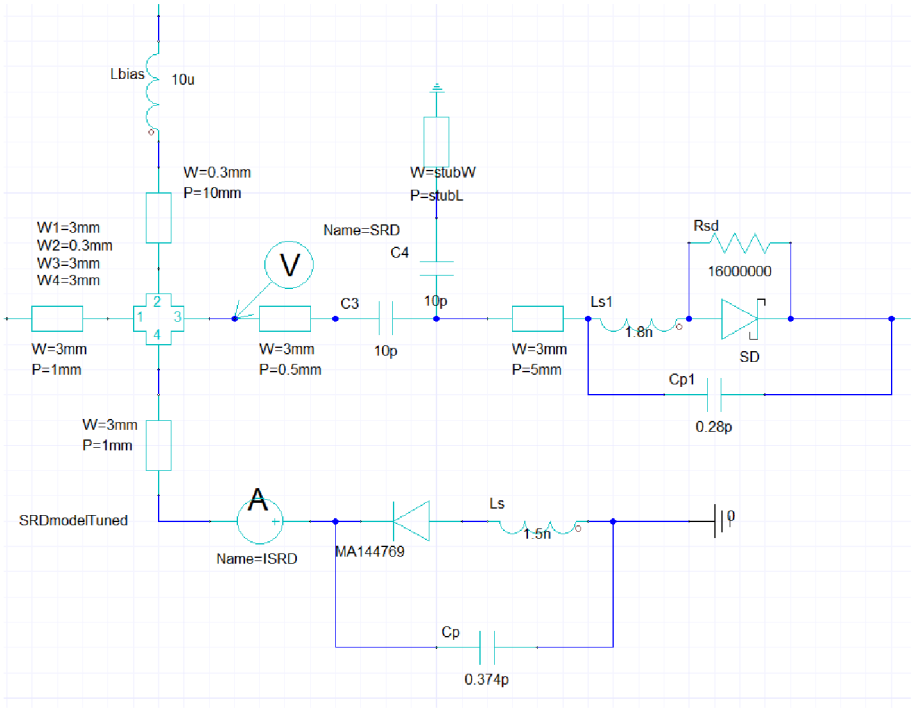


Fig. 2.10: Circuit for the simulation of the shorted stub

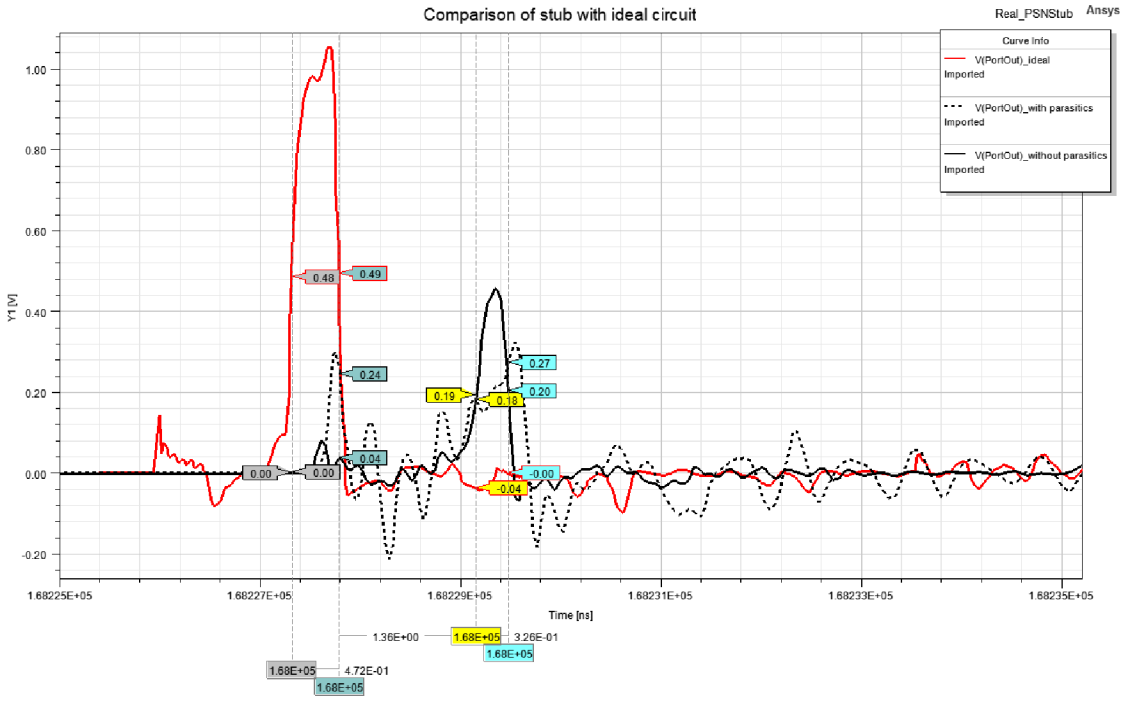


Fig. 2.11: Simulation results for the shorted stub; comparison between ideal, transmission lines included and parasitics included cases

Extending the input falling edge

We have observed that applying this modification to the proposed PSN does not produce the same behavior as presented in [14] and [20], which was explained in Sec. 1.3 using Fig. 1.7. For the design in Fig. 2.9, the extension of the input falling edge only modifies the negative voltage spike's duration, not its amplitude, as is illustrated in Fig. 2.12 (b). It even comes at a cost of reducing the output pulses amplitude (see Fig. 2.12 (a)). This occurs because the SRD's junction has less time to store the charge when the input is in V_{LOW}. That makes this modification unsuitable for the chosen design.

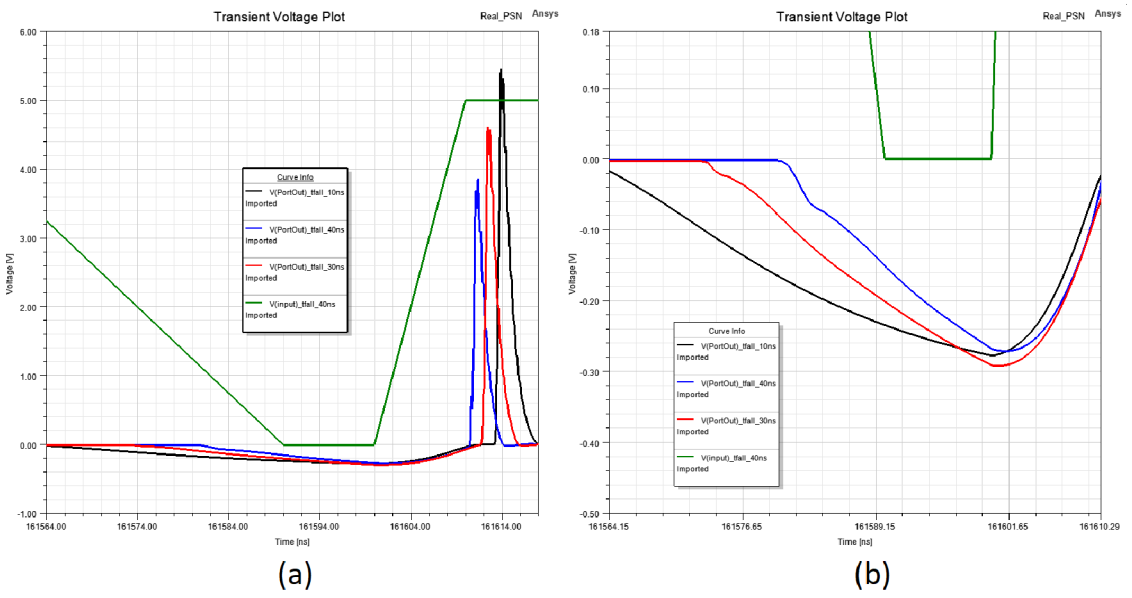


Fig. 2.12: (a) Comparison of the effects that different input falling edge durations have on the negative voltage swing at the output; (b) detail

It is possible to deal with these limitations to a degree by combining the falling edge extension with the addition of a blocking capacitor between the driver and PSN. It has to have a high enough value (the value of about 10 nF is sufficient), so that it only partially filters the DC component out of the input square wave. Since the value of V_{HIGH} which actually interacts with the SRD is decreased by this, it will cause a reduction to the pulse amplitude. And since for a lower voltage level the diode now discharges at a slower rate, this will also lead to an increase of t_{S}. Similar to the case without a blocking capacitor, the less time the SRD spends charging during V_{LOW}, the lower the amplitude of the output pulse is.

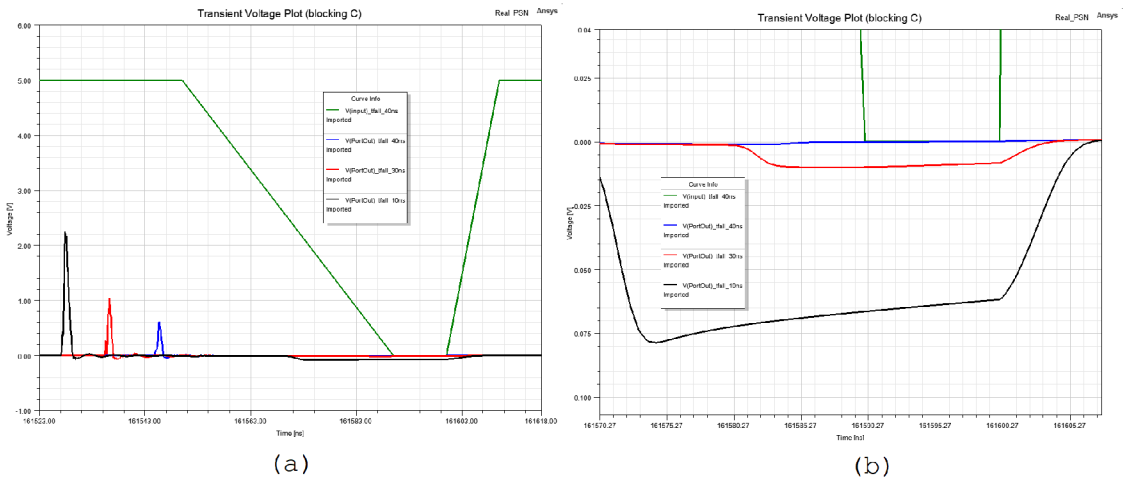


Fig. 2.13: (a) Output voltage with different input falling edge durations and an input blocking capacitor; (b) detail

In Fig. 2.13 (b) we see that compared to Fig. 2.12, the falling edge extension now minimizes the undesirable negative voltage swing. As discussed, this comes at the price of pulse magnitude (see the corresponding waveform in Fig. 2.13 (a)). A good compromise could be reached for t_{fall} values between 20 and 30 ns, but experimental confirmation is required.

Two SRDs

As was mentioned in Sec. 1.2, connecting the second SRD as shown in Fig. 2.14, with a delayed trigger relative to the first one can affect the output falling edge. It can remove the decrease in slope that is present in the output falling edge's lower part. While that is not necessary for the chosen application of this circuit, we will examine the possibility.

In Fig. 2.15 we see a comparison between the single and double SRD versions of the PSN. Unlike in the ideal theoretical case (see Fig. 1.5), it was not possible to preserve the pulse amplitude. Figure 2.15 shows the best result that was obtained for a value of $R_2 = 200\,\Omega$. For comparison, the output for $R_2 = 400\,\Omega$ is shown as well. The worst feature of this modification is an introduction of a negative voltage swing behind the initial pulse. This occurs because the voltage oscillation induced after the second diode triggers in the node between the SRDs has an exceedingly high amplitude. Thus, the output Schottky diode is not able to rectify it entirely. On the other hand, the pulse has been shortened and the slope of the falling edge increased. Since a decrease of the output pulse width is not desirable for the intended application, this modification will not be utilized unless a diode with a longer transition time has to be used as a replacement for the current SRD.

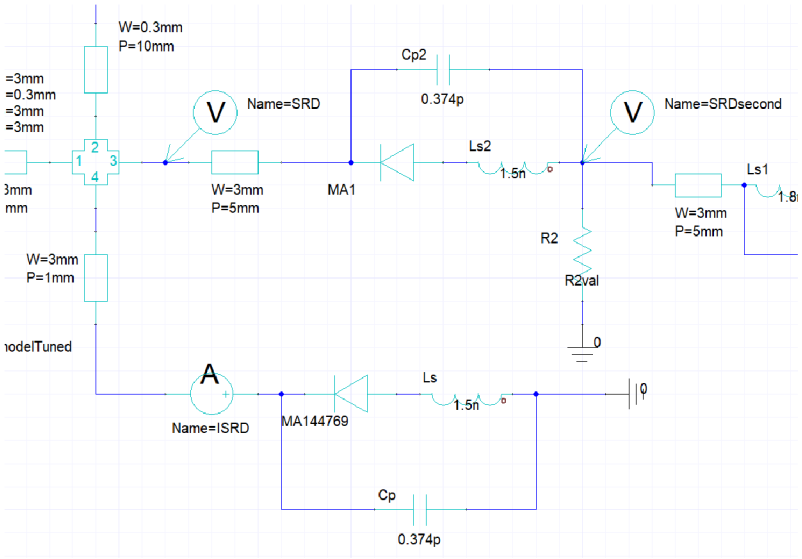


Fig. 2.14: Addition of the second SRD to the circuit from Fig. 2.9

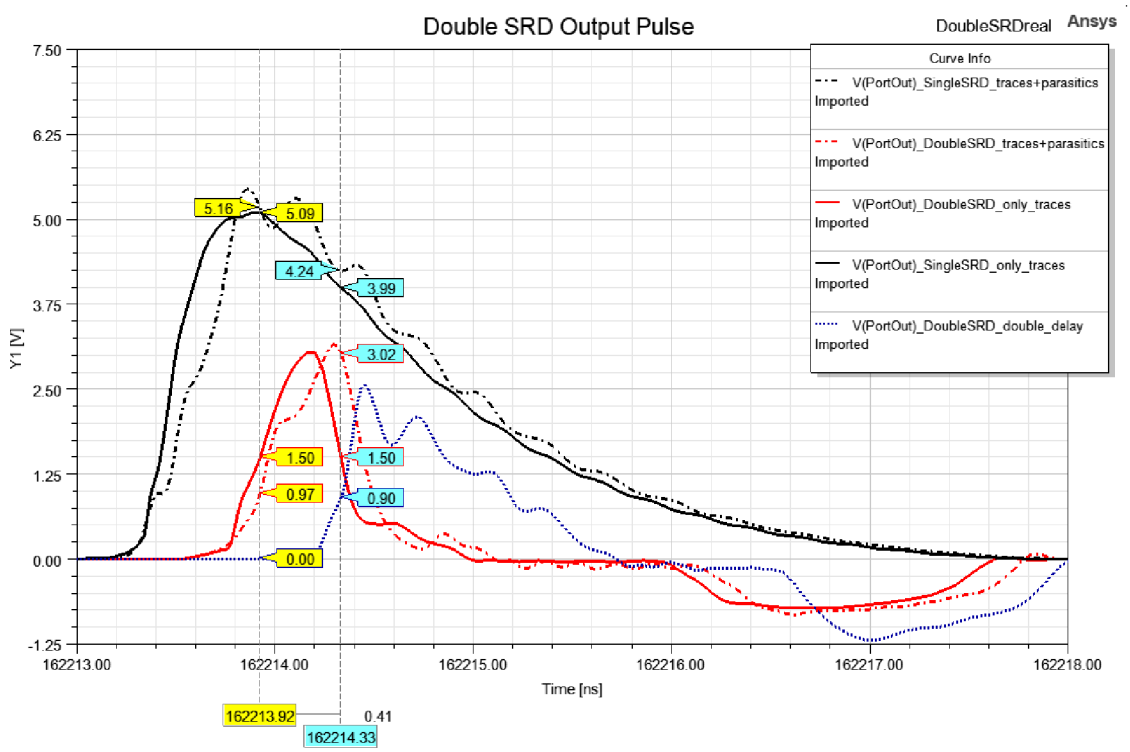


Fig. 2.15: Output waveforms (red: $R_2 = 200\,\Omega$; blue: $R_2 = 400\,\Omega$) for the circuit in Fig. 2.14, in comparison with the single SRD circuit from Fig. 2.9

3 Circuit & PCB design

This chapter outlines the design process of the two printed circuit boards that the final pulse generator consists of. The aim is to clarify the design choices made as they pertain to the design requirements.

3.1 General design requirements

Based on the results presented in Chapter 2, we have concluded that the unmodified circuit utilizing a parallel SRD and biasing tee, examined therein, complies best with the output pulse time width requirement. Furthermore, the pulse is not seriously distorted and due to a comparatively low amount of components and small required dimensions (as opposed to a PSN utilizing a shorted stub), this variant of the circuit best meets the requirements for portability and will preserve as much of the pulse amplitude as possible.

Another requirement placed on this project was to create a standalone pulse generator. Thus, the PSN discussed and simulated in Chapter 2, while by far the most important, is only a small subset of the circuitry required to create such a device.

The second most important part of the device is the PSN driver. Its necessary properties were briefly mentioned in Sec. 1.3, namely the ability to create a rising edge as steep as possible (from 0 to 5 V in 10 ns being the target value), while at the same time being able to deliver current peaks over 200 mA to the PSN. While a square wave oscillator is the best choice for this purpose, most integrated options can not fulfill the current requirement. The driver is therefore composed of two subcircuits: the oscillator and a current buffer.

All of the above mentioned circuit blocks of course have to be powered. To satisfy the requirement for portability, the power source has to be a (preferably rechargeable and high energy density) battery. Some types of batteries might necessitate the inclusion of auxiliary ICs.

The voltage from the battery has to be converted to the appropriate levels for powering the rest of the circuit. The required voltage is +5 V to power the oscillator and buffer blocks, with an expected current capability of at least 200 mA. More is preferable, to keep the voltage level as close to +5 V as possible when the load is switched. A voltage of -5 V is needed for the PSN bias. Due to the maximum forward current of the utilized SRD, no more than 50 mA current capability is necessary.

In the early stages of the design, a decision was made to split the entire circuit onto two separate PCBs. This was done for multiple reasons, the ease of troubleshooting, tuning and testing chief among them. One PCB would contain

circuitry for creating the necessary DC voltages and a generator of the rising edge required to trigger the SRD-based PSN. The other PCB would then contain only the aforementioned PSN, so as to keep it separated from the rest. This was done to minimize unwanted interference between the switched part of the power delivery board and the reactance-based components of the PSN one.

3.2 Pulse shaping network

Since this part of the project was mostly designed during the analysis in Chapter 2, including a choice of components, this section will only cover how the circuit was tuned and PCB specific parameters.

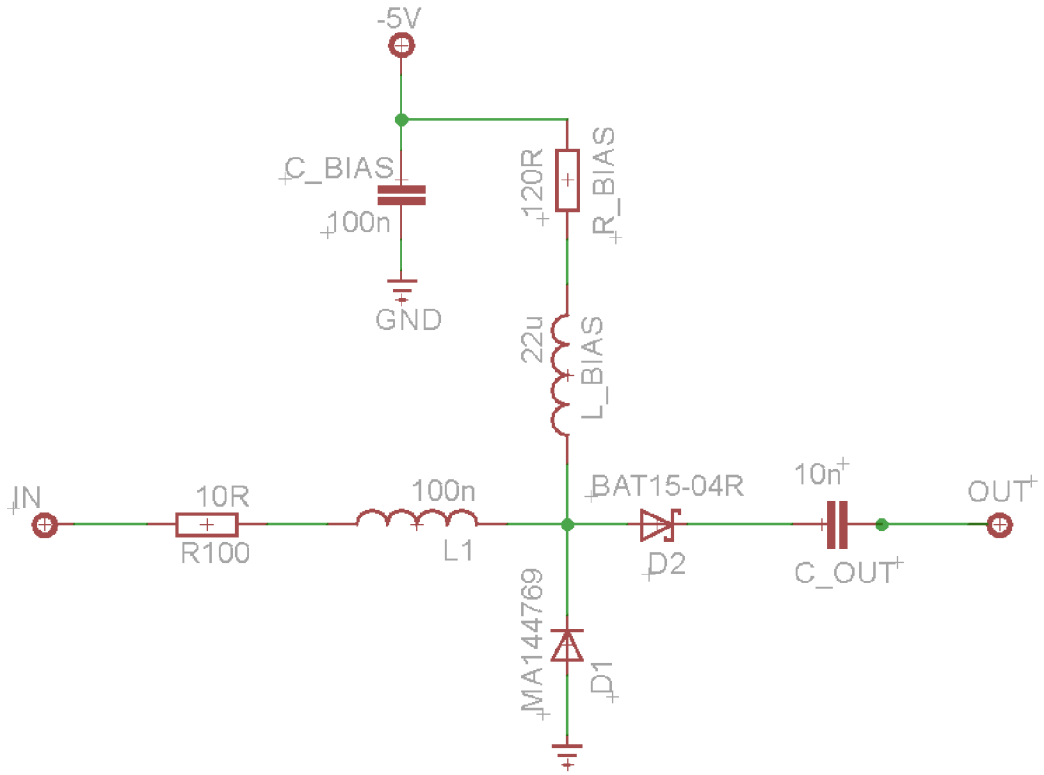


Fig. 3.1: The final schematic for the PSN

We examined the addition of an input series blocking capacitor. The idea was to block the DC current between the +5 V and -5 V voltage nodes of the circuit, which would prevent unnecessary load on the resistors between these nodes. As far as the output characteristics of the PSN are concerned, however, this addition has its drawbacks. The capacitor filtered the DC component from the input square wave ($V_{\text{HIGH}} = 5$ V; $V_{\text{LOW}} = 0$ V), which reduced the output amplitude roughly by half. Therefore, the blocking capacitor has not been included in the final design.

A minor change comes with the value of L_{bias}, which serves as an RF choke. Its value was increased from 10 to 22 μH, to provide better filtering characteristics at lower frequencies.

Finally, as to the Schottky diode used as a rectifier, two choices were considered: BAT15-04R from Infineon [27] and BAT54A from Nexperia [28]. The former one was used for simulations. This diode performs better with respect to BAT54A in terms of its lower forward voltage drop and a shorter transition time. On the other hand, BAT15-04R has a relatively low maximum reverse voltage, 4 V, which could cause damage. The output capacitor C_{OUT} is charged by the output pulses during operation (5 V peak in simulation) and when the input goes to 0 V, a reverse voltage could briefly appear before the capacitor discharges through the load. This issue did not manifest in the manufactured PCB, possibly due to the short duration of this state. Therefore, BAT15-04R is used in the final circuit board, since the pulse amplitude is higher and the trailing negative voltage overshoot greatly reduced compared to the alternative. Note however, that these two components are not pin compatible and the PCB layout was designed for BAT54A.

Tuning component values

After manufacturing the first version of the PCB, the values of R_1, L_1 and R_{bias} were tuned, to optimize the output pulse. The goal was to find a balance of high pulse amplitude ($\sim$5 V), large pulse width (>1 ns) and minimal distortion (ringing, overshoot etc.).

Using the results from Sec. 2.2, the values were adjusted from the initial simulated estimates to what can be seen in Fig. 3.1. R_1 was lowered to 10 Ω, since this would discharge the SRD junction faster, providing a sharper impedance transition, leading to an increase in amplitude. R_{bias} was lowered from 170 to 120 Ω as well, to increase the biasing current from 30 to 40 mA, as this increased the pulse width. Finally, after experimenting with different values, L1 was kept at 100 nH, since this provided the maximum amplitude and an acceptable pulse width.

During the design process, we also kept track of pulse distortions in response to changing component values. Two components play a key role. The first is R_1, where higher values cause the parasitic oscillation on the pulse to increase in amplitude, see Fig. 3.2 (a). Since this maximizes both amplitude and pulse width, it is therefore desirable to keep R_1 as low as possible (see Table 3.1). Note however, that values below $\sim$ 10 Ω cause a decrease in amplitude, as was explained using simulations in Sec.2.2.1 using Fig. 2.6. The second is L_1, the increase of which dampens the oscillation (see Fig. 3.2(b)). While this is beneficial for increasing the pulse width, this leads to losses in amplitude (see Table 3.1). Thus we keep $L_1 = 100$ nH.

Tab. 3.1: Output pulse parameter dependence on R_1, L_1 and R_{bias} values

Component	Value	V_{max} [V]	t_{FWHM} [ns]
R_1	10 Ω	5.6	2.3
	22 Ω	3.8	1.633
	33 Ω	2.2	1.426
L_1	330 nH	4.2	4.03
	560 nH	3.5	5.2
R_{bias}	220 Ω	5.5	1.611

Note: Default component values are $R_1 = 10\ \Omega$, $L_1 = 100$ nH *and* $R_{\text{bias}} = 120\ \Omega$

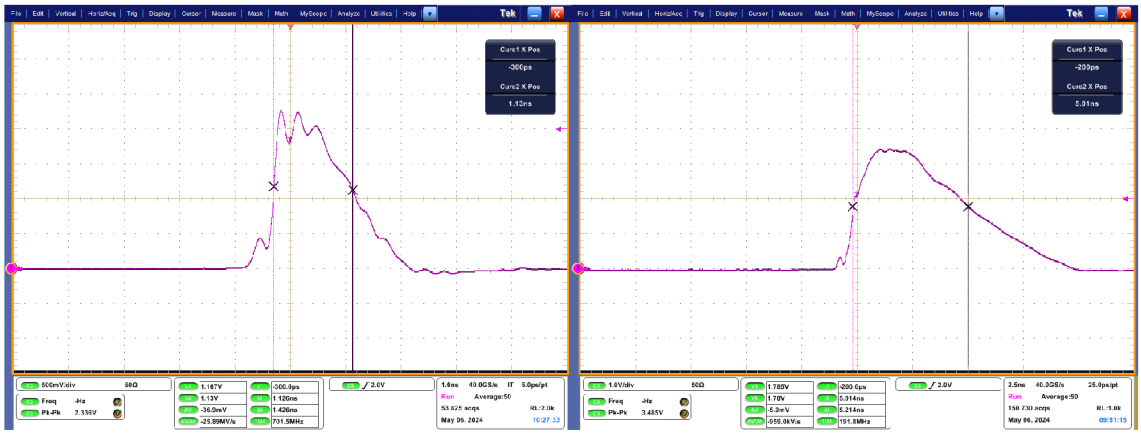


Fig. 3.2: Pulse distortions for: (a) $R_1 = 33\ \Omega$; (b) $L_1 = 560$ nH

PCB specific information & Troubleshooting

The simulations have shown that the circuit performed best when most lines were kept at a characteristic impedance of 50 Ω (excluding the DC biasing line). Originally, due to its low cost, the entire device was supposed to be designed on the FR4 substrate. To reduce losses and trace dimensions on the PSN board, the substrate Arlon 25N, $\varepsilon_{\text{r}} = 3.38$ [−], of height $h = 0.762$ mm was used. For example, consider the 50 Ω trace width, $w = 1.76$ mm, compared to the equivalent on FR4, $\varepsilon_{\text{r}} = 4.4$ [−], $h = 1.5$ mm, which is $w = 2.87$ mm. It also offers a significantly lower loss tangent, $\tan\delta = 0.0025$ [−], compared to FR4's $\tan\delta = 0.02$ [−], which should result in a more efficient device.

During the design of the PCB for the PSN, we chose not to include any vias between the ground plane on the top and bottom layers. The reasoning was that this would add a parasitic capacitance between the SRD and ground. The conductive

path would go through the legs of the SMA connectors on the edges of the board. This decision can be justified by the approach to grounding in e.g. [4],[6] and [14].

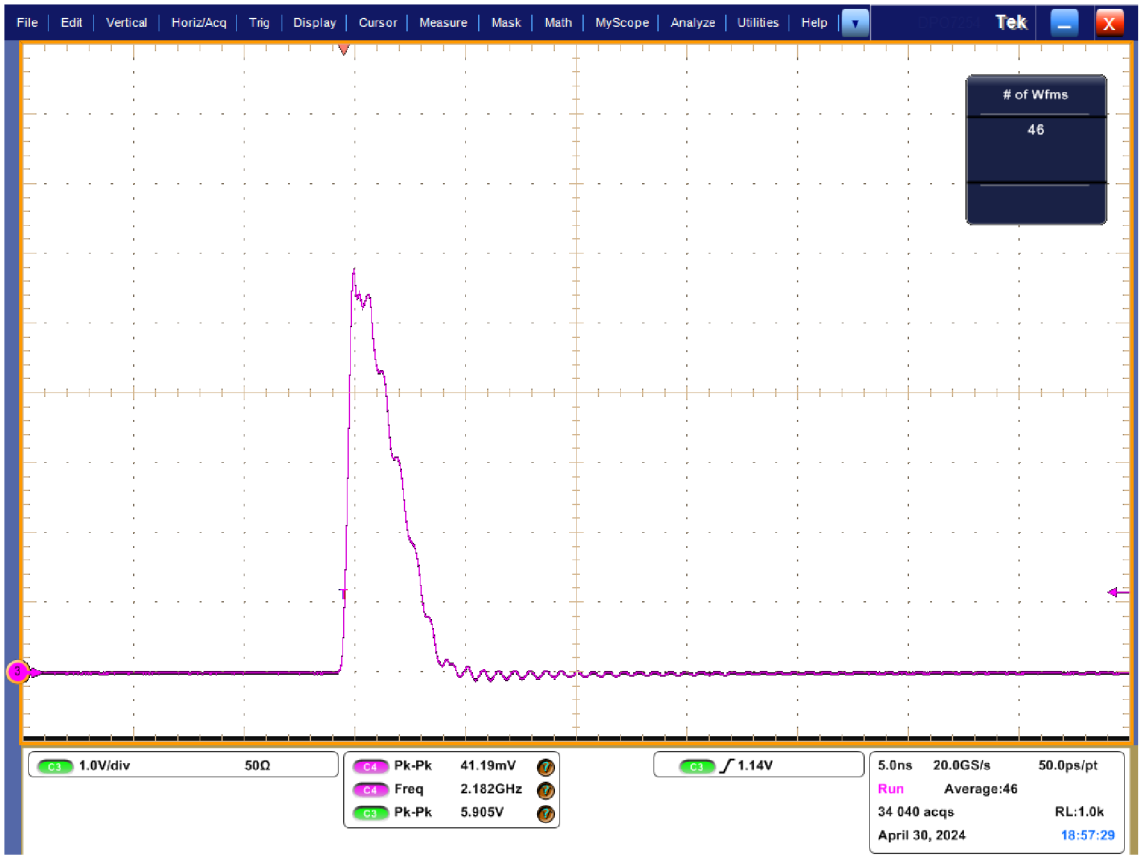


Fig. 3.3: Parasitic oscillations of the output pulse due to improper grounding

However, since the SRD is located in the middle of the 43 mm long board, this proved to be an issue that affected the output pulse, as seen in Fig. 3.3 (a). We have in essence added a parasitic inductance in series with the SRD, due to the improper grounding. The voltage oscillations in the node between the SRD and Schottky diode are not dampened sufficiently and thus are not rectified properly, which manifests itself through ringing. This is similar to the worst-case simulation including parasitics from Fig. 2.8. An addition of a copper strip over the edge of the board to connect the ground planes as a substitute for vias mitigates this issue. The pulses presented further in this work were produced on a board with this modification.

3.3 Power delivery & Driver circuit

This part of the device is comparatively more complicated, therefore its description is split into sections according to Fig. 3.4.

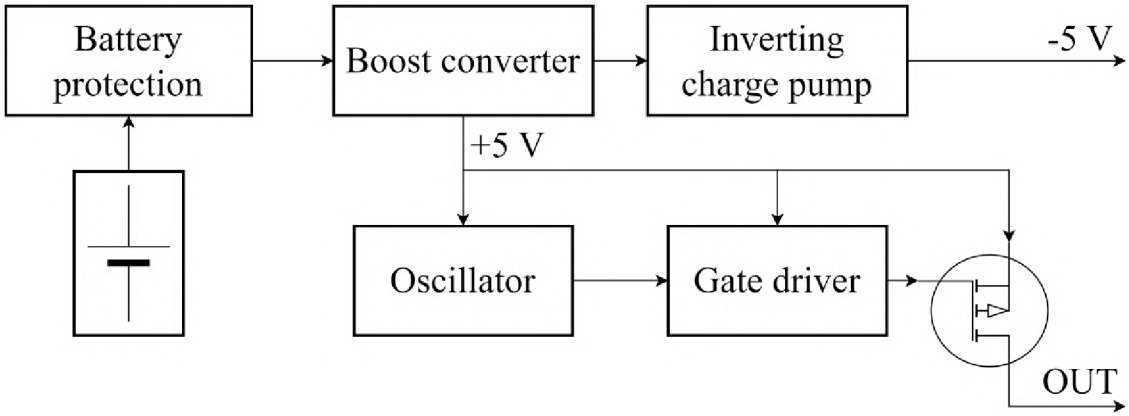


Fig. 3.4: The final block diagram for the power delivery and driver board

3.3.1 Power source and protection

Seeking to comply with requirements as they are stated in Sec. 3.1, the lithium-ion battery was chosen as the power source, specifically in the shape of a single common 18650 cell. This choice offers a high charge density value. They are easily removable and transferable, which enables external charging. Since there is no intention to have a charging function on the device, the latter properties are important aspects in our design. External charging of course requires that the battery be easily reachable and not fixed. To this end, an enclosure that is easy to disassemble without tools and an open battery holder were chosen.

The inclusion of a lithium based battery warrants extra protection, to prevent accidental over-discharge and mainly to insure that the battery stays above the minimum safe voltage. To this end a single cell protection IC, the S-8241(ABKMC-GBKT2G) from ABLIC Inc. [29], was chosen. This is a fairly common solution (usually under the name DW01-P from Fortune semiconductor), where the IC based on the voltage level and current draw from the cell controls the gates of two anti-series N-channel MOSFETs, which are connected between the battery cathode and circuit ground.

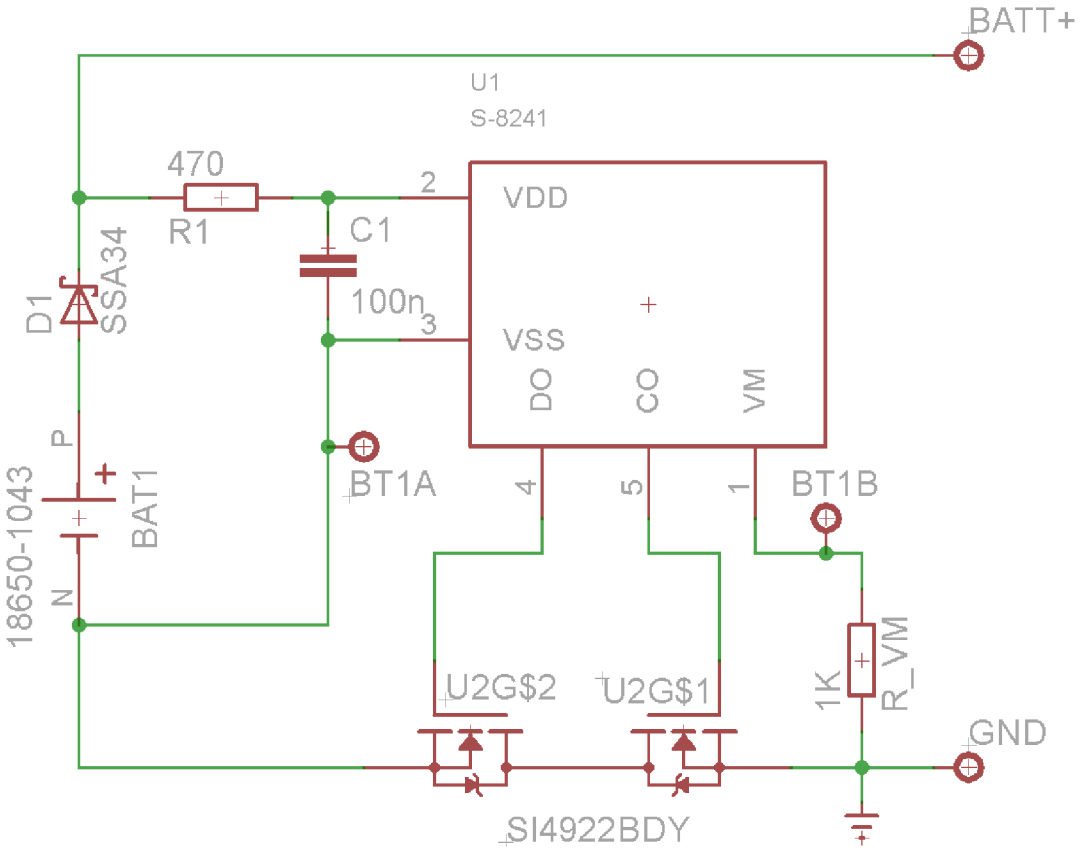


Fig. 3.5: Battery protection circuit

The limit values of the IC are set in manufacturing, the issue with this being that models available during the manufacturing of this project, have their lower discharge limit set to 2.5 V. This goes against the general recommendation of not discharging li-ion batteries below roughly 3 V, since this reduces their lifetime due to irreversible chemical changes inside the battery. Besides this major weakness of the IC, battery reverse polarity is an issue. While the diodes in the ground FETs protect the rest of the circuit, the S-8241 itself has no such protection and could potentially be destroyed. It is therefore necessary to introduce a separate reverse polarity protection element. Usually in a low voltage application such as this one, connecting a diode in series with the entire circuit would be considered brute-force and undesirable, due to introducing a voltage drop to an already low voltage budget. However, in our case, this can be turned into an advantage: the S-8241 IC has its lower discharge set too low (2.5 V), adding a rectifying diode would effectively raise this level, as well as provide the lacking reverse polarity protection. The SSA34 from Vishay [30] has a voltage drop of $V_\mathrm{f} = 0.49\ V$, which is perfect for this application, and it can also be utilized in other parts of the project (see Sec. 3.3.4).

Another issue to take care of is the so-called 'power down function'. After first connecting the battery, the IC will not activate the FETs, unless the voltage difference between the voltage sensing pin VM and VDD is higher than 1.3 V. This is solved by temporarily connecting the battery cathode to the VM pin directly. In our circuit we implement it by simply connecting a button between these nodes. Note that it is only required to press it after first inserting the battery, it has no effect in other situations.

The IC requires several external components to function properly (see Sec. 3.5). All the values are set as per the manufacturers recommendation, since there is no need to modify them for our purposes. Capacitor $C_1 = 100$ nF is a standard bypass capacitor, it also prevents the FET gates from oscillating during overcurrent or short circuit detection. $R_{\mathrm{VM}} = 1$ kΩ is used to limit the current through the IC to prevent damaging it, when sensing overcurrent via the voltage present at the VM pin, set to the threshold of 0.15 V. Similarly, $R_1 = 470\ \Omega$ limits current through the chip for added ESD protection.

The most important parameters of the two FETs is their gate threshold voltage and channel resistance in the on state, R_{DS} which has to be low to reduce power loss. To ensure that the IC can control them without issue, the FETs have to be reliably fully open between the voltages of 0.4 and 2.5 V. This is fulfilled by the Si4922BDY from Vishay [31], with a maximum value of $V_{\mathrm{GS(th)}} = 1.8$ V and a channel resistance of $R_{\mathrm{DS}} \leq 0.02\ \Omega$ above $V_{\mathrm{GS}} = 2.3$ V. It is also a dual package, thus saving space.

3.3.2 Buffer

In Chapter 2, we described a solution to the buffer issue in a single IC package, namely the BUF634A from Texas instruments. However, after practical experience with the type of circuit that is designed here, it became obvious that this option would introduce several issues that would complicate the design. Namely: 1) a dual supply of different level, ± 8 V, than what was otherwise present in the circuit; 2) Output slew-rate is dependent on input slew-rate, which puts an unnecessary demand on the oscillator and layout of that part of the board; 3) It provides a bipolar output, when we only require a unipolar one.

Another possible solution would be to replicate a buffer/driver composed of discrete components, as was done in [5] and [20], for example. Modifications would of course be required. Everything would need to be scaled down to 5 V, the BJT structure switched to PNP and inverted, since our design requires driving pulses of opposite polarity. The main advantage of this solution mentioned in the paper is a controllable falling edge duration, however we are using a different PSN structure and simulation results in Sec. 2.3 have shown this does not produce a benefit in

our case. In fact, we only require the rising edge of the pulse to be reliably driven. Thanks to the fact that the chosen PSN structure contains a negative voltage biasing line, we can let the buffer output node be driven in a high impedance state for the falling edge. In other words, we do not require a dual drive, since the biasing voltage will open and charge the SRD even without the buffer forcing 0 V to the PSN input. Therefore, we can massively simplify the buffer structure.

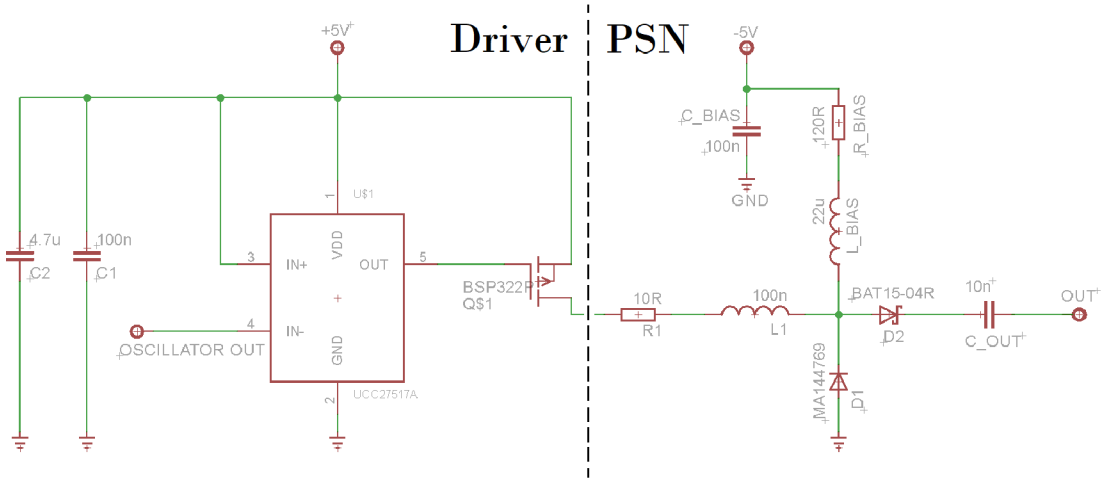


Fig. 3.6: Buffer structure schematic together with the PSN

The result of this approach is shown in Fig. 3.6. We chose a MOSFET, since they in general have faster rise/fall times compared to BJTs. It is a P-channel device and while an N-channel would be able to achieve faster rise times, we chose this option to ensure we drive the output rising edge without a pull-up, which would produce an undesirable voltage drop and reduce output amplitude as a result. To produce a reasonable rise time, it has to be driven by an appropriate gate driver IC. Simulations show that we require a rising edge of ∼10 ns. Driving a MOSFET's gate is essentially charging and discharging a capacitor, the value of which is usually quantified as gate charge in [C] (= coulombs). To provide fast rise times, this value has to be as low as possible. Another important parameter is the V_{GS} at which the MOSFET opens fully, which has to fall under -5 V considering the supply voltage.

We chose the BSP322P from Infineon [32]. Its gate charge is 16.5 nC, which is still comparatively high to even sub-nanocoulomb options on the market, but it has several advantages. Even with this value, the manufacturer claims an impressive maximum rise time of 6.5 ns for $V_{DD} = -50$ V, which is a lower value than many comparable options with lower gate charge values. This is especially favorable in combination with it being in SOT-223-4, a large leaded package, which allows more options for routing. Furthermore, the maximum threshold voltage is $V_{GS(th)} = -2$ V,

with the MOSFET being fully open between -3.5 and -3 V at operating temperature, which will result in efficient driving of the gate in the 5 V network of the board.

For the gate driver, we require a device that: 1) has a digital input, in order to not rely on the oscillators output rise time; 2) is in a leaded package; 3) can work with a 5 V supply; 4) can charge/discharge the gate of the MOSFET in around 10 ns or less. Since we care only about the P-channel MOSFET's rise time, we are interested in the driver fall time.

Requirements 1 through 3 are fulfilled by all the below considered ICs. The final decision was mainly influenced by requirement 4 and the amount of details provided by the manufacturer. The options are listed in Table 3.2. Note that the manufacturers usually list fall-times for a specified load and switching voltage. To make the comparison meaningful, the values shown are calculated for the actual loading capacitance $C_{\mathrm{LOAD}} = Q_{\mathrm{GATE}}/V_{\mathrm{DD}} = 16.5\mathrm{nC}/5\mathrm{V} =$ **3.3 nF**. Then the fall time is calculated as the time constant of this capacitance and the drivers internal resistance through which the current is sunk multiplied by 2.2 (this is because we calculate the fall time of an edge from 90 to 10 %). Note that the calculations consider the worst case scenario as per the datasheet values and serve only as a rough approximation to compare the devices.

Tab. 3.2: Gate driver options consideration

Name	Manufacturer	Adjusted fall-time [ns]
NCP3420 [33]	ON Semiconductor	18.2
MAX15070A [34]	Analog Devices	3.4
UCC27517A [35]	Texas instruments	8.7

We chose the UCC27517A-Q1 since it is sufficient for the purposes of the design, but mainly because the manufacturer provided extra information in the datasheet concerning layout and power dissipation issues. It can operate with a supply voltage as low as 4.5 V and is contained in an SOT-23 package. It has two TTL and CMOS compatible inputs, one inverting, which is the one used (see Fig. 3.6). This is done with the chosen oscillator in mind (see Sec. 3.3.3), since when disabled, its output is pulled low, thus pulling the driver's output high and closing the output MOSFET. The driver can handle a 4 A current peak, which is sufficient, since we will require approximately $I_{\mathrm{DRIVER}} = Q_{\mathrm{GATE}}/t_{\mathrm{fall}} = 16.5\mathrm{nC}/10\mathrm{ns} = 1.65$ A. The power during switching, P_{SW}, that will have to be dissipated is given by the manufacturer as:

$$P_{\mathrm{SW}} = Q_{\mathrm{GATE}} \cdot V_{\mathrm{DD}} \cdot f_{\mathrm{SW}} = 16.5 \cdot 10^{-9} \cdot 5 \cdot 100 \cdot 10^{3} = 8.25 \text{ mW}, \tag{3.1}$$

where Q_{GATE} is the gate charge, V_{DD} the supply voltage and f_{SW} the switching frequency. As the result of Eq. (3.1) shows, the package (SOT23) can dissipate the power easily, therefore there is no need for an external gate resistor. This is further supported by desiring the fastest edge possible. Another reason to omit this resistor is the need to limit the parasitic inductance in the junction between the driver output and MOSFET gate, so that it will not produce unwanted voltage spikes in response to the sharp changes in current during switching, as this could damage the driver. In the ideal case, where the full current capabilities of the chosen driver are utilized, we should be able to achieve an edge of $t_{\mathrm{fall}} = Q_{\mathrm{GATE}}/I_{\mathrm{DRIVER}} = 16.5\mathrm{nC}/4\mathrm{A} = 4.125$ ns.

3.3.3 Oscillator

Thanks to the chosen gate driver, the demands on the oscilator can be relaxed. Based on the available literature on the subject, in Chapter 2, an assumption was made concerning the frequency of the driving square wave, which was set to $f_{\mathrm{PRF}} = 10$ MHz.

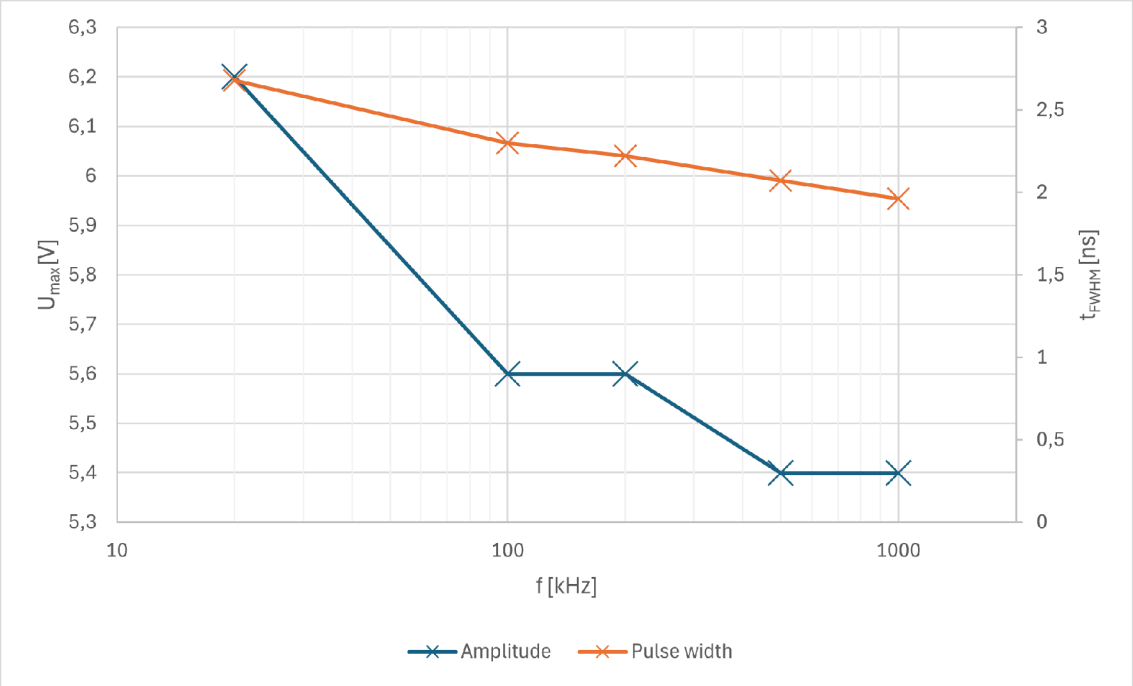


Fig. 3.7: Output amplitude and pulse width dependence on input frequency; measured on on the Tektronix DPO 7254 oscilloscope for PSN component values: $R_1 = 10\ \Omega$, $L_1 = 100$ nH, $R_{\mathrm{bias}} = 120\ \Omega$

After the first version of the PSN board was manufactured, it showed better results, namely in increased pulse width and less distortion, with lower frequencies, as

shown in Fig. 3.7. Therefore, we have decided to switch to frequencies in the neighborhood of $f_{\mathrm{PRF}} = 100$ kHz. Decreasing this value further results in a lengthening of the pulse tail (see Fig. 3.8(b)).

In accordance with the gate driver manufacturer's instructions, the oscillator should have sharp voltage transitions to drive the gate driver's input without difficulties, meaning the best choice is a square wave. Thus, the only functional requirement is, that the oscillator is tunable, preferably a voltage controlled oscillator (VCO). This is done so the user can fine tune the output frequency on the spot, if needed.

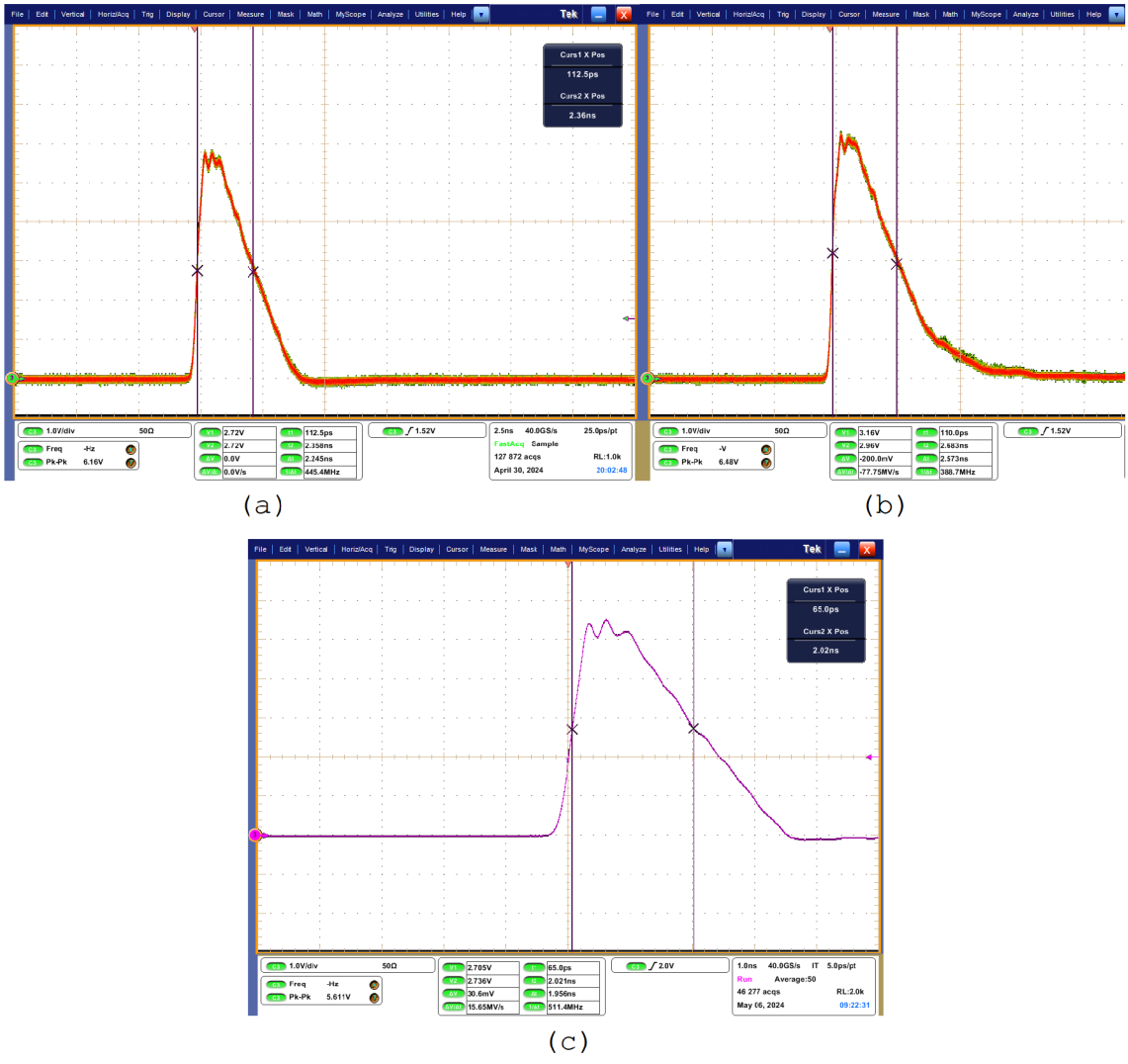


Fig. 3.8: Comparison of pulse shapes: (a) $f_{\mathrm{PRF}} = 100$ kHz; (b) $f_{\mathrm{PRF}} = 20$ kHz; (c) $f_{\mathrm{PRF}} = 1$ MHz

In this frequency range, there are two options: an oscillator built from discrete components and operational amplifiers or a chip oscillator. The IC would offer a

smaller necessary board space, less period jitter and more control options, with the only downside of being more costly. Therefore, we chose the LTC6990 from Analog devices [36], which is a low cost precision programmable silicon oscillator. It outputs a 50 % duty cycle square wave in the range of 488 Hz to 2 MHz with a period jitter of $\pm 0.22\ \%_{\mathrm{P-P}}$, can work on a 5 V supply and comes in a SOT-23 package. It can produce ~ 1 ns rise/fall times on a 5 pF load, which safely covers the requirements of the gate driver. It is also possible to set the output to go low without external pull-downs when the enable pin is pulled low, which is advantageous due to reasons described in Sec. 3.3.2.

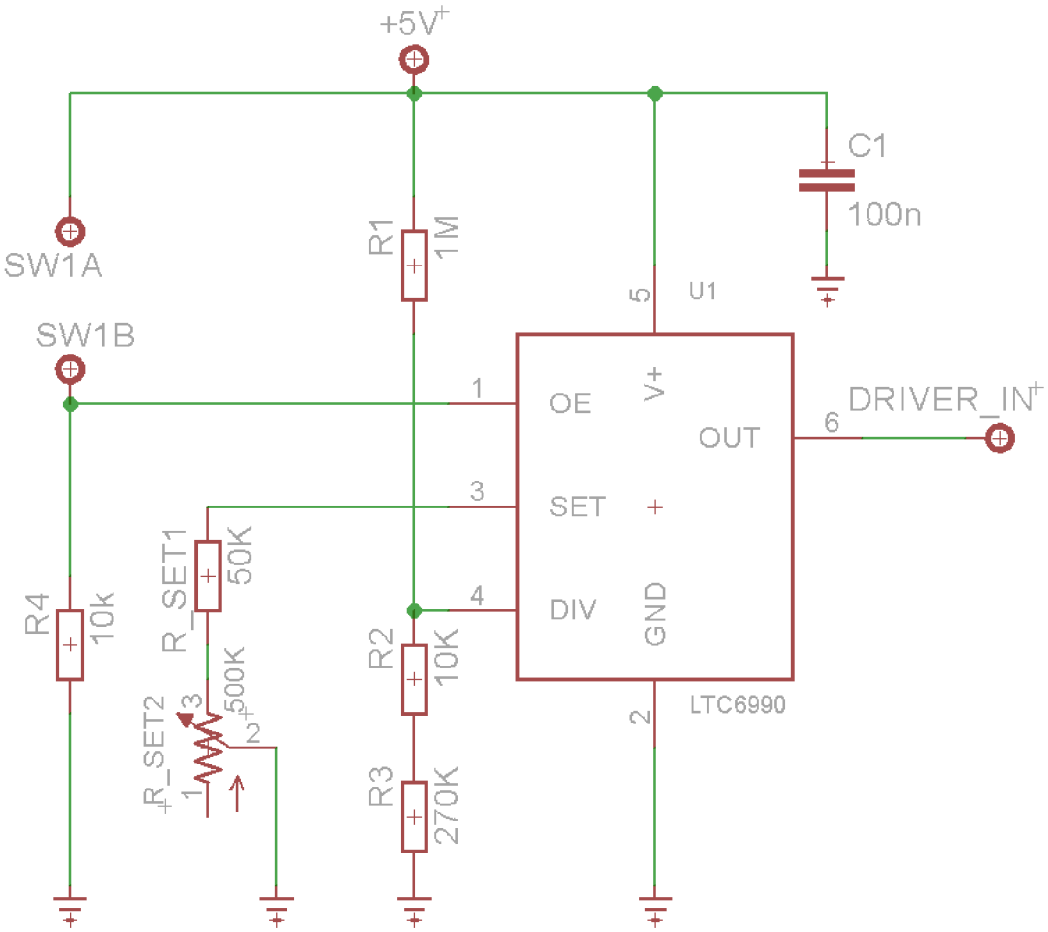


Fig. 3.9: Oscillator schematic with component values

The LTC6990 is controlled by external resistor values (see Fig. 3.9). The DIV pin, which is used to select the frequency range and output state when disabled, is set up as on output of a voltage divider from supply to ground. The manufacturer provides a table of value combinations, since we aim at $f_{\mathrm{PRF}} = 100$ kHz and a low output when disabled, we require $R_1 = 1\ \mathrm{M\Omega}$ and $R_2 + R_3 = 280\ \mathrm{k\Omega}$. This gives

us a frequency range from 7.8 to 125 kHz, setting the internal frequency divider to $N_{\mathrm{DIV}} = 8$.

The frequency itself is set by regulating the current draw from the SET pin. The lowest resistance value to achieve maximum frequency is $R_{\mathrm{SET1}} = 50$ kΩ. To be able to retune the oscillator, we add a series trimmer R_{SET2}, so that $R_{\mathrm{SET}} = R_{\mathrm{SET1}} + R_{\mathrm{SET2}}$. We do not need to use the full lower range of the oscillator, a lower bound of $f_{\mathrm{PRF}} = 10$ kHz is sufficient. Therefore, from a modified design equation provided by the manufacturer:

$$R_{\mathrm{SET2}} = R_{\mathrm{SET1}} \cdot \left(\frac{f_{\mathrm{MASTER}}}{f_{\mathrm{PRF}} \cdot N_{\mathrm{DIV}}} - 1 \right) = 50 \cdot 10^3 \cdot \left(\frac{10^6}{10^3 \cdot 8} - 1 \right) = 575 \ k\Omega \doteq 500 \ k\Omega, \tag{3.2}$$

where f_{MASTER} is the frequency of the master clock. Due to available trimmer values, the result is rounded down to 500 kΩ, which makes the actual lower bound $f_{\mathrm{PRF}} \approx 11.4$ kHz.

The enable pin, OE is connected to a switch, which allows manual disabling of the boards output.

3.3.4 DC voltage generation

The ICs which are used on the board require a +5 V voltage supply, with the output square wave's high level being the same. At the same time, we require -5 V for the biasing of the PSN board. Since the device is powered by a li-ion cell (including the protections described in Subsection 3.3.1, the effective input voltage range is 2.5 to 3.7 V), the voltage will obviously require stepping up. This means the inclusion of a boost converter. Since it has to be able to cover the current consumption of both the output and the biasing line, the requirement is the ability to reliably supply a peak of 200 mA, although more is better, as this will lead to a lower voltage drop when the converter output is under load. An exceedingly high voltage drop is undesirable mainly due to the UCC27517A driver, which has a minimum worst-case operating voltage of 4.35 V. Especially, since the load changes rapidly due to the output switching, the converter block should be able to respond to this transient without a prolonged drop in voltage. At the same time, since the device is portable, we aim for an efficient conversion to prolong battery life.

Initially, we considered a single package solution, in the form of the TPS65133 from Texas Instruments [37]. This device is a ±5 V dual rail supply with a maximum current capability of 250 mA. It claims a stable output voltage level over the whole load current range. It shows a spiked voltage drop of ~ 60 mV for an increase in loading current by 150 mA over 20 μs. It also has an enable function, thus allowing

for simple control. The only issue is its 12-pin WSON package, which does not fit within the layout tolerances of our chosen manufacturer.

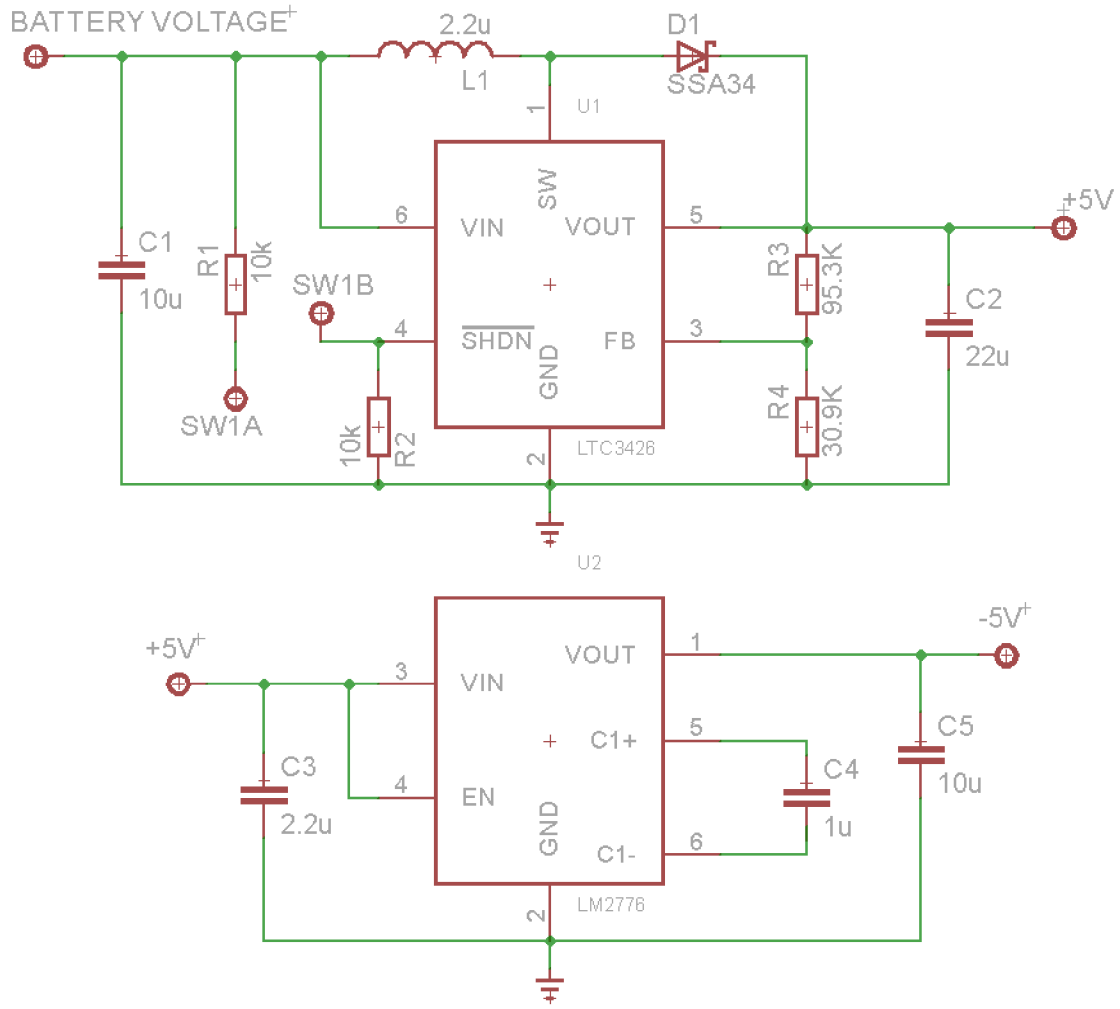


Fig. 3.10: DC supply network

We opted for a solution separated into two parts. For the up-conversion, we chose the LTC3426 from Analog Devices [38]. And as a separate inverting charge pump we choose the LM2776 by Texas Instruments [39]. The LTC3426 claims to deliver an output current up to 800 mA, while only requiring small external SMDs. In our input voltage range and chosen configuration (see Fig. 3.10), the device should have a conversion efficiency of 88-90 %. Furthermore, a voltage drop of only ∼50 mV is shown for 500 mA of output current. The response to a sharp load increase by 250 mA in ∼1 μs is a spiked voltage drop of 150 mV. All the above mentioned characteristics safely comply with the device requirements.

The component values of C_1, C_2, L_1 and D_1 are chosen as per manufacturer recommendation to maximize conversion efficiency for a 5 V output fed from a li-

ion battery. Capacitors C_1 and C_2 were chosen with a maximum voltage of 25 and 16 V, respectively. This is done to maximize the capacitance value at our operating voltage. The capacitors are ceramic to minimize their equivalent series resistance, which has an impact on output ripple. The inductor L_1 is chosen to handle the 2 A current peaks that LTC3426 can produce during switching, the diode D_1 is chosen with similar peak current considerations. Inductor L_1 was also chosen with its low DC series resistance of 31.3 mΩ in mind, to minimize power losses. The values of R_3 and R_4 determine the output voltage level according to:

$$V_{\text{SUPPLY}} = 1.22 \cdot (1 + \frac{R_3}{R_4}) = 1.22 \cdot (1 + \frac{95.3}{30.9}) = 4.98 \text{ V}. \tag{3.3}$$

The demands on the biasing source are not that high. While the LM2776 is not ideal, its parameters prove to be sufficient. The main issue is that at our operating current, $I_{\text{bias}} = 40$ mA, the output will have a ripple of ∼100 mV and should exhibit a voltage decrease of 150 mV compared to the input. However, both of these are not an actual problem for the given application, since the instability of I_{bias} does not have a major impact on the charging of the SRD's junction. With the given parameters and for the chosen external components (see Fig. 3.10), the IC should operate at 92 % efficiency. External component values are once again based on the manufacturer's recommendation. Similar to the boost converter, the external capacitors are selected with several multiples of the operating voltage in mind, to maximize capacitance. This will, together with them being ceramic and thus low equivalent series resistance, ensure a stable output and predictable current capability.

4 Testing & Measurement

Concerning primarily the output waveforms of both the PSN and the Power & Driver board, this chapter presents the results of the project. The outcomes of measurements are compared with the results of simulations. Since the materials/trace width has been changed, we refer to a simulation representing the new design configuration as well. The time-domain measurements were performed on the Tektronix DPO 7254 digital oscilloscope. It has a bandwidth of 2.5 GHz, which implies that its input rise time $t_{\text{rise(Osc.)}} = 0.35/BW = 0.35/2.5\text{GHz} = 140$ ps, is sufficient for our purposes. The measurement setup is shown in Fig. 4.1. The spectral measurement was captured on a Rohde & Schwarz FSL spectrum analyzer with a 3 GHz bandwidth.

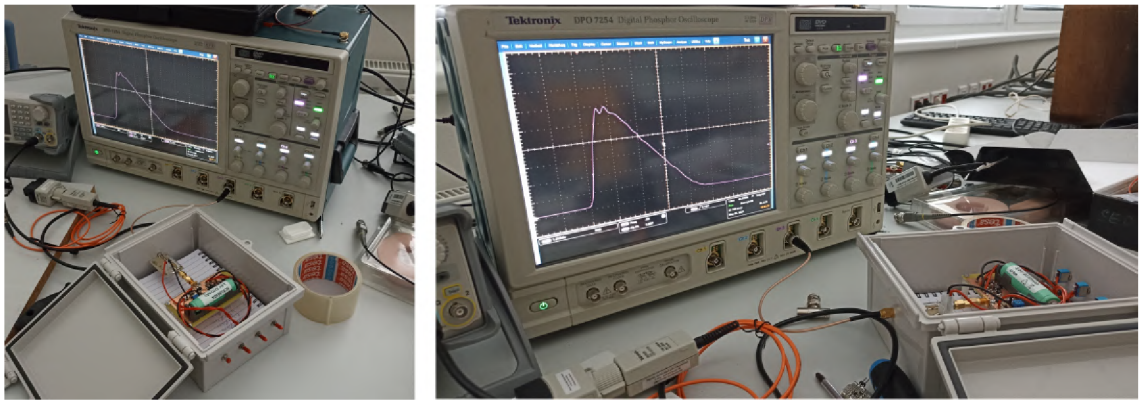


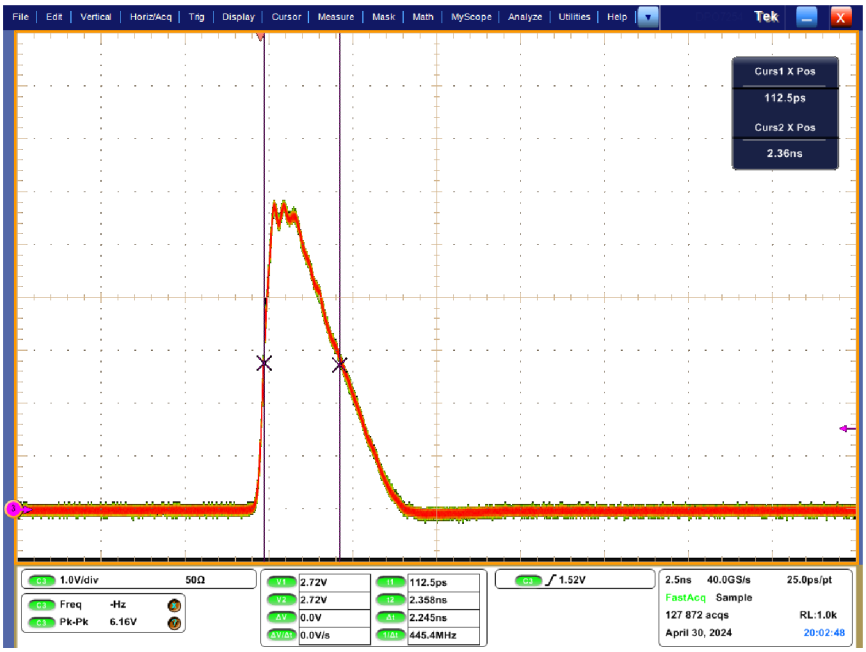
Fig. 4.1: Measurement setup (enclosure was later switched to aluminum)

4.1 PSN measurements

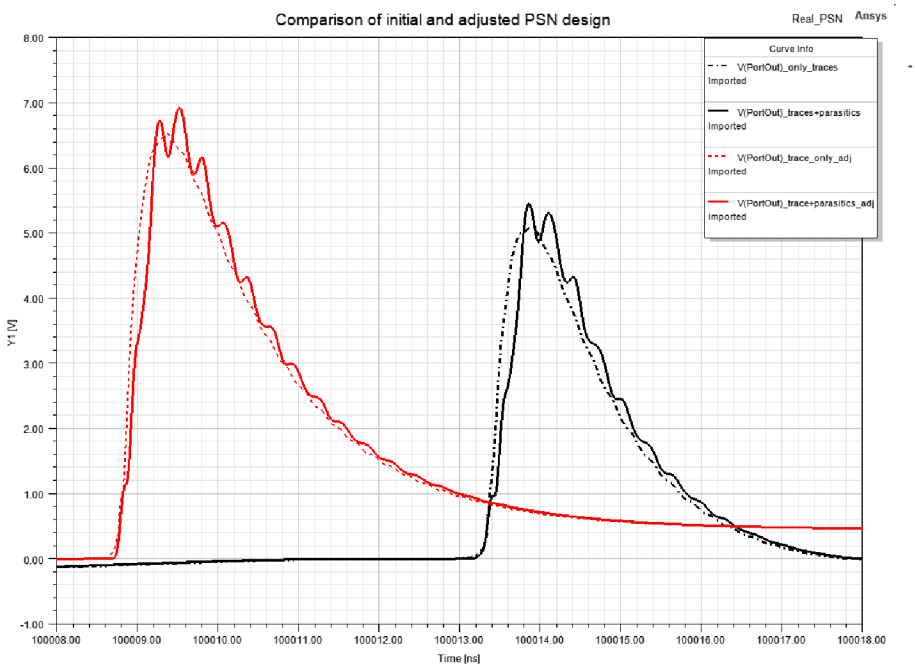
We performed another set of simulations with the updated PSN parameters (substrate, component values, driver rising edge etc.). We can therefore make comparisons of the achieved output pulse parameters to the initial and final versions of the design.

The final version of the project operates on a 50 Ω load and is capable of producing a pulse that reaches an amplitude of $V_{\text{max}} = 5.6$ V and has a FWHM of $t_{\text{FWHM}} = 2.245$ ns (see Fig. 4.2 (a)). In simulation (see Fig. 4.2 (b)), when accounting for the influence of trace and component parasitics, we got a pulse of $V_{\text{max(sim)}} = 5.4$ V and $t_{\text{FWHM}} = 1.4$ ns. By adjusting the design as described in Sec. 3.2 we have seemingly achieved approximately the same amplitude, while improving the pulse width by ∼800 ps with respect to the prediction. Note, however, that the updated simulation shows $V_{\text{max(adjSim)}} = 6.9$ V. This points to the fact that the

actual improvement in amplitude between manufactured boards would be at least 1.5 V, which correlates well with what was found during the PSN tuning (see Table 3.1).



(a)



(b)

Fig. 4.2: (a) Output pulse of the PSN in the configuration described in Sec. 3.2; (b) Simulation results for the original (black) and improved (red) PSN design

We observe several important differences between the measurement and simulation, in particular, in the pulse shape. The difference is most significant in the rising and falling edge regions. The falling edge of the measured pulse is essentially linear, while the simulations predict an exponential decay. We have demonstrated in Fig. 3.8 that the behavior at the falling edge depends on the chosen f_{PRF}. The linearization is present above 100 kHz. There is also a major difference in how pronounced the oscillations are in the simulation, where ideal inductances were used to imitate the worst case scenario. This resembles the output with improper grounding (see Fig. 3.3) and an increased $R_1 = 33\ \Omega$ (see Fig. 3.2). By solving these issues, we managed to mitigate the parasitic inductance of the PSN, thus dampening the ripple to the present state.

Figure 4.3 shows a zoom-in on the rising edge, which is composed of two regions that can be approximated by two straight lines of different slopes. The slope discontinuity of the rising edge is present due to the parasitic oscillations superimposed on the pulse. The total rise time, (see Fig. 4.3 (a)), is $t_{\mathrm{r}} = 372$ ps, whereas the first linear region extends over the first 214 ps. We can again compare this with the original prediction (see Fig. 4.2 (b)), where we see ∼400 ps (∼240 ps without parasitics from components). This shows that the SRD model used in simulation fits in well with the actual SRD. As far as the distortions of the pulse edge are concerned, notable differences have been observed. In the simulation the edge shows a more pronounced distortion and is broken into three separate steps for both the original and updated predictions. This difference can be attributed to the same causes as the falling edge in the above paragraph, *i.e.,* the parasitics.

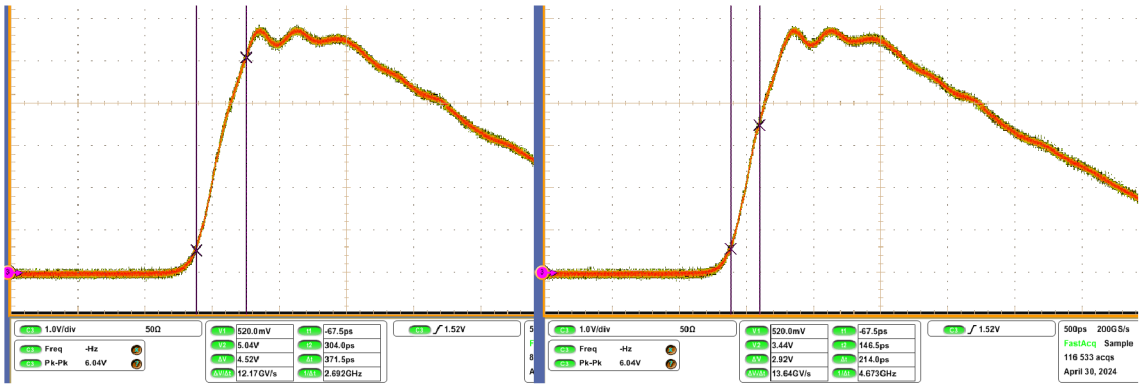


Fig. 4.3: Close-up of the rising edge of the PSN output pulse; (a) Total rise time; (b) Rise time of the first linear region

We can further examine and compare the oscillations (see Fig. 4.4 (a)). The measured period is 299 ps. This matches with the 320 ps in the case of the simulated

result in Fig. 4.2. Through comparing this value over measurements that included changes in f_{PRF} and component values (see Fig. 3.2 and Fig. 3.8) and accounting for its short period, we come to the conclusion that it must depend on the reaction of very small reactances to the pulse rising edge. This agrees with the simulation, where ∼1 nH inductances and sub-picofarad capacitances were used to emulate the package parasitics of components. In Fig. 4.4 (b)we show measurement results of the output PSD.

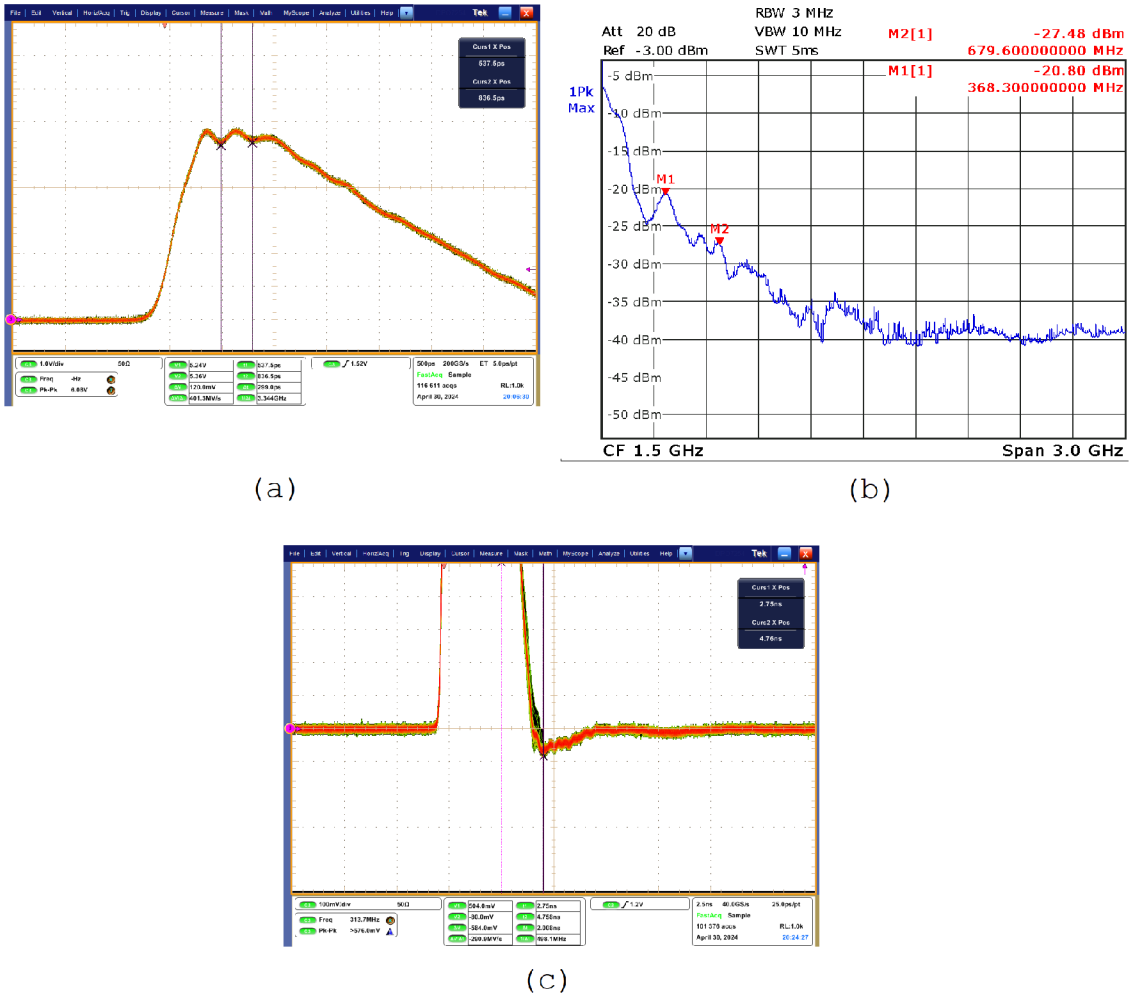


Fig. 4.4: Zoom-in on the undesirable traits of the output pulse; (a) Ripple in time; (b) Frequency spectrum of the output pulse; (c) Negative overshoot at the foot of the pulse

Overall, the parasitic ripple in the designed device is mostly present at the peak of the pulse and then sharply declines in amplitude to the degree that it is almost undetectable on the second half of the falling edge. It reaches a maximum of 0.5 V_{p-p} or 8.9 % of the pulse amplitude and therefore does not present a significant detriment.

In Sec. 1.2, the negative voltage overshoot of the output was described, as well as measures taken to mitigate it (rectifier). As the measured overshoot only has a peak value of -80 mV (see Fig. 4.4), we may conclude that the measures have proven to be effective. This is 1.43 % of the output amplitude and hence insignificant.

Another issue was discussed in both Chapters 1 and 2. The presence of a negative voltage swing of the output on the falling edge of the input square wave. As can be seen from Fig. 4.5, this issue is not present in the manufactured circuit. However, there is a dampened oscillation of 15 mV in amplitude on the output line 30 ns before the input shuts off. We were not able to identify the cause, nevertheless due to its weak amplitude and short duration, we anticipate that this will not have an effect on the intended application.

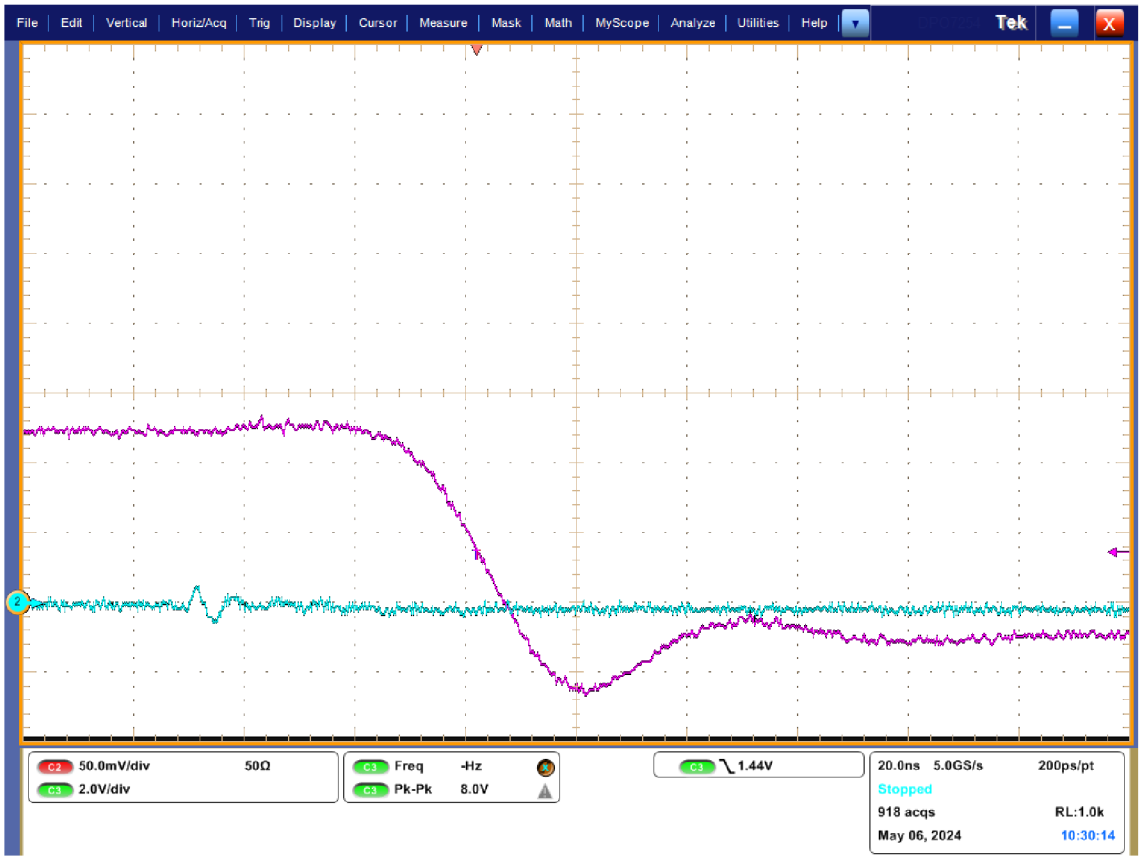


Fig. 4.5: Contrary to the outcomes of simulation, no negative voltage swing of the output during the falling edge was measured.

4.2 Power&Driver measurements

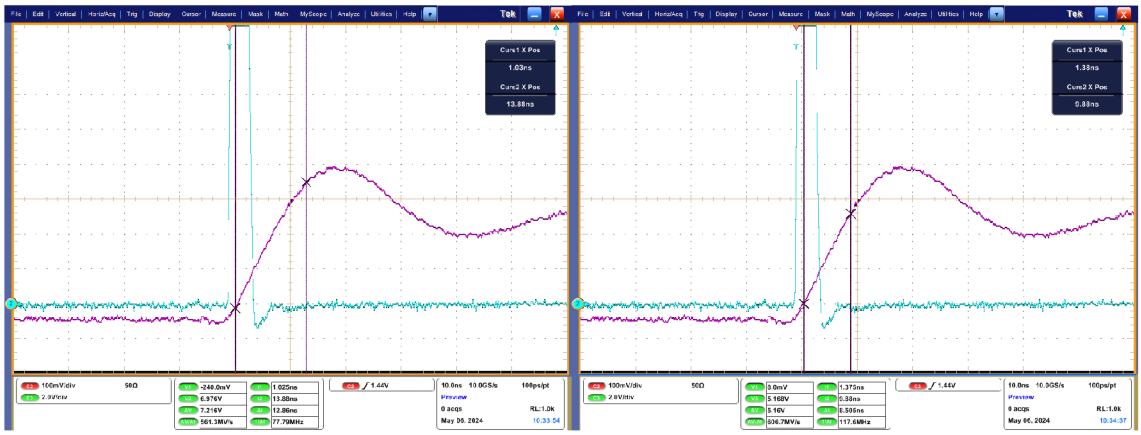
As far as this Power & Driver board is concerned, we are interested in the driver output and the power consumption of the entire device.

Fig. 4.6: Driver output waveform: (a) 50 Ω load; (b) PSN as the load

When the driver is connected directly to a 50 Ω load (e.g., oscilloscope input), it produces a rising edge as seen in Fig. 4.6 (a). Its rise time is $t_{\text{rise}(50\Omega)} = 3.576$ ns. We can compare this to the ideal case prediction for the MOSFET gate driver rise time, 4.125 ns. We see, that the MOSFET is able to open faster, which fits in with our predictions. However, due to the way the circuit is designed, this is dependent on the load. This is demonstrated in Fig. 4.6 (b), where the driver output is connected directly to the PSN. We note that the rise time has increased. Since the edge is now followed by a dampened ringing, we can distinguish between 0-5 V rise time and 10-90 % rise time. Consequently, the output reaches a peak of 8 V. Then the largest voltage drop is to 4 V. The most important factor as to their effect on the circuit is that the ringing has a very short duration. The maximum is well within the allowed voltage level in any case. As to the voltage drop, it is mentioned in Sec. 3.3.4 that a voltage drop below 4.35 V would negatively affect the gate driver. However, its duration is only ∼20 ns, so the bypass capacitors are able to compensate without any issue. The voltage level stabilizes to 5 V after 120 ns.

Regarding the rise times, as said above, if we take into account the full voltage range of the output, its duration is 12.86 ns (see Fig. 4.7 (a)). If we only consider the rise time between stable voltage levels, we obtain a value of $t_{\text{rise}(\text{PSN})} = 8.5$ ns (see Fig. 4.7 (b)), which fits the prediction from Tab. 3.2 of 8.7 ns. This fulfills our goal of 10 ns.

The DC voltage of the biasing line was measured at -4.8 V, which agrees with the prediction from Sec. 3.3.4 of having a decrease of $\sim$ 150 mV compared to the input voltage.



(a) (b)

Fig. 4.7: Driver output waveform: (a) 50 Ω load; (b) PSN as the load

Fig. 4.8: Measurement of current consumption via voltage drop on a 2.2 Ω resistor

The power consumption was measured by connecting a 2.2 Ω resistor in series with the battery and measuring the voltage drop with an oscilloscope. This was done to test if the consumption varies in time. Fig. 4.8 shows that consumption during full operation is constant and equates to $I_{\text{op}} = V_{\text{meas}}/R_{\text{meas}} = 0.12/2.2 = 54.5$ mA. If we

presume that the consumption stays mostly the same during the battery discharge, then for a cell with a capacity of 3070 mAh, we estimate ∼56 hours of fully activated operation per cell.

Conclusion

In this thesis we have designed and manufactured a standalone portable wide band pulse generator to be used for non-invasive estimation of the electrical conductivity of tissue. A special focus has been placed on the use of a step recovery diode (SRD) in the role of a sharpener and its properties. In particular, its dynamic behavior and simulation model have been described in detail.

Because of its relatively low price and availability, the MA144769 diode with its 150 ps transition time has been selected. A model of this diode was tuned in ANSYS Designer. The value of the diode's dynamic resistance was verified by measurement.

Owing to the possibility to control both the forward and reverse bias current values, a parallel SRD biased by a DC voltage source has been chosen as the topology for the PSN. Since the diode itself produces a pulse of below 340 ps FWHM, which is too narrow for the desired application, a series inductance was added to the signal path, which allows for an increase of FWHM. For example, $L_1 = 100$ nH widens the pulse to 1.37 ns in simulation.

Furthermore, the use of transmission line stubs for the pulse formation has been explored. Since a unipolar output is sufficient for the intended application, a shorted line as the end stage is not necessary. It has been shown that the use of a stub near the sharpener will potentially distort the pulse, or shorten it at best. Therefore, stubs have not been included in the final design.

We chose a modular design, keeping sub-circuits of the generator on separate PCBs, the driver with power supply on one and the PSN on the other. To allow for its portability, the device is powered by a removable 18650 li-ion cell. For a cell of 3070 mAh capacity, it can continuously operate for about ∼56 hours. The enclosure is made of aluminum and allows for easy disassembly to access the battery.

The designed PSN was tuned on the physical board to achieve a compromise between maximizing pulse amplitude width without deforming the pulse shape significantly. The result is a unipolar pulse which has an amplitude $U_{\mathrm{max}} = 5.6$ V and a FWHM of $t_{\mathrm{FWHM}} = 2.245$ ns, thus outperforming the initial simulated design with $U_{\mathrm{max}} = 5.4$ V and a FWHM of $t_{\mathrm{FWHM}} = 1.37$ ns. The pulse has a rise time of $t_{\mathrm{rise}} = 372$ ps, which is comparable to the simulated value of 400 ps. The circuit is designed to operate with a 50 Ω load, lower impedance loads will reduce pulse amplitude.

The designed Power & Driver board is capable of producing a rising edge of 8.5 ns from 0 to 5 V when driving the PSN. The other parts of the circuit are not compromised by the effects of the switching. Moreover, the PSN board does not produce a negative voltage swing at the output in response to the falling edge of the driver, thus keeping the output free of interfering pulses.

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Symbols and abbreviations

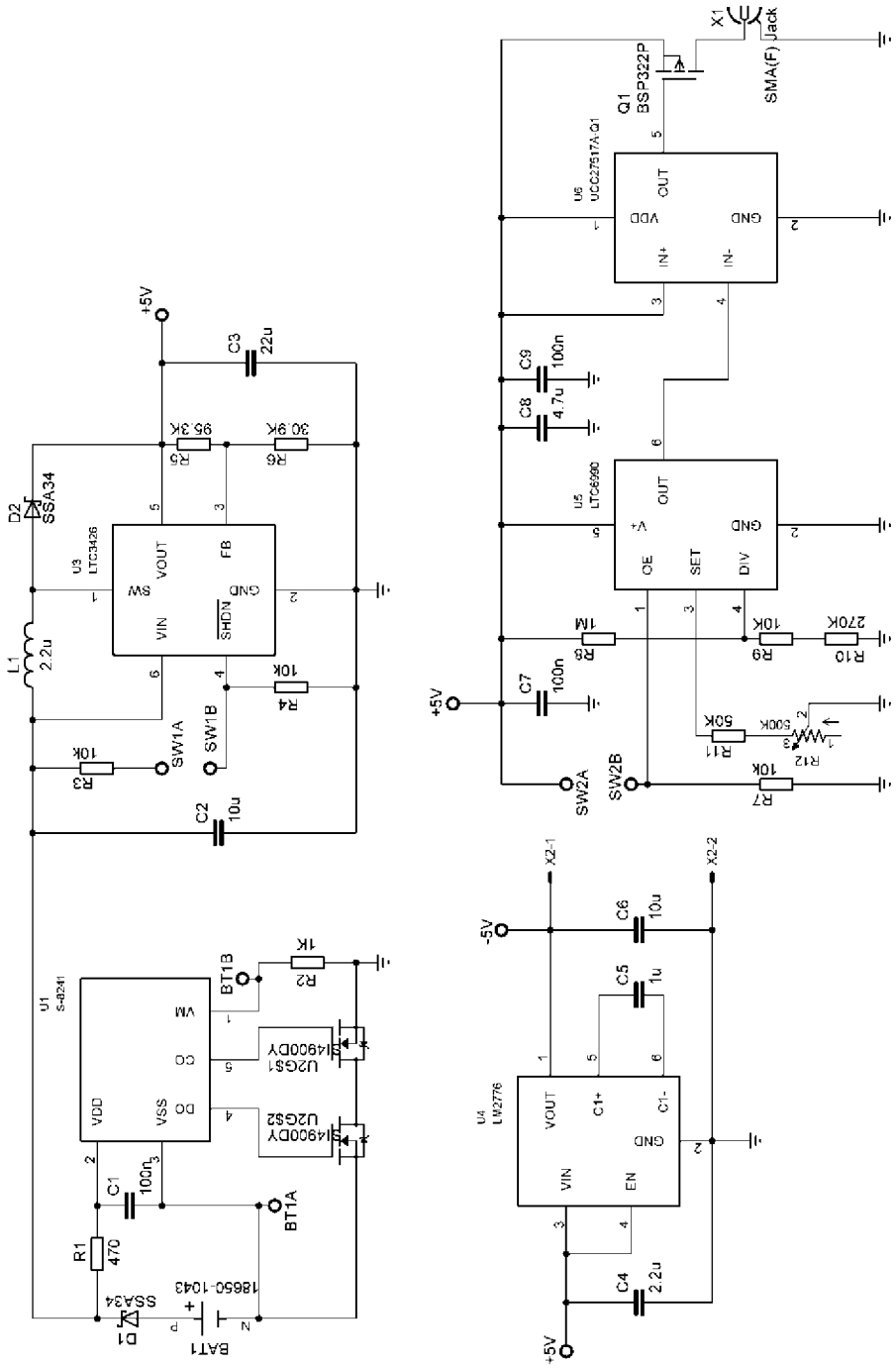
UWB	ultra-wide band
SRD	step recovery diode
PSN	pulse shaping network
GPR	ground penetrating radar
PRF	pulse repetition frequency
EM	electromagnetic
CAD	computer assisted design
FWHM	full width at half maximum
PCB	printed circuit board
IC	integrated circuit
FET	Field effect transistor
MOSFET	Metal oxide semiconductor field effect transistor
BJT	Bipolar junction transistor
VCO	Voltage controlled oscillator
V **[V]**	voltage
I **[A]**	current
$I_{\mathrm{F}}/I_{\mathrm{R}}$ **[A]**	SRD forward/reverse current
t_{S} **[s]**	time to remove charge stored in the SRD junction
τ **[s]**	minority carrier lifetime
t_{F} **[s]**	time to store charge in the SRD junction by I_{F}
t_{r} **[s]**	output rise time
t_{t} **[s]**	intrinsic diode rise time
C_{vr} **[F]**	capacitance of the SRD junction under reverse bias

$C_\mathrm{f}/C_\mathrm{r}$ [**F**]	capacitance of the SRD equivalent model under forward/reverse bias
R_f [Ω]	resistance of the SRD junction in forward bias
ϕ [**V**]	diode contact potential
ϵ_reff [**-**]	effective relative dielectric permittivity

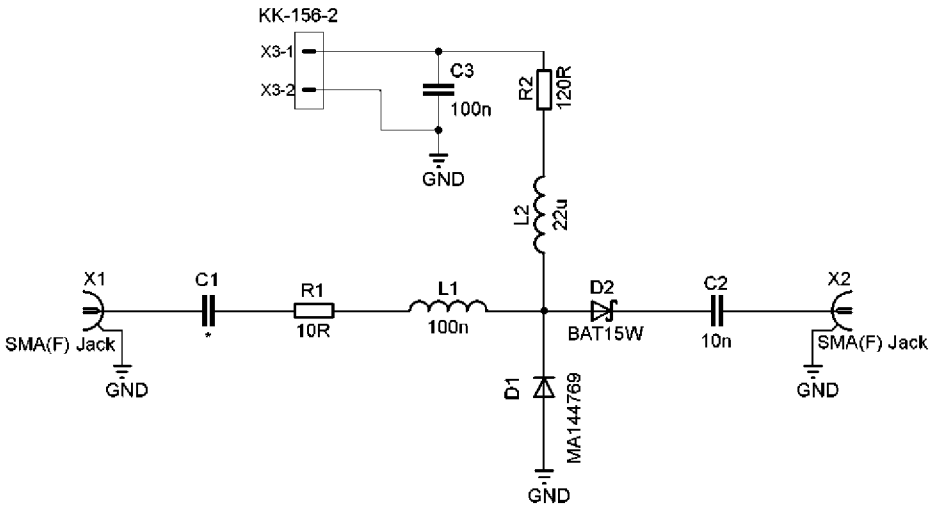
List of appendices

A Circuit schematics

A.1 Power & Driver



A.2 PSN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C3
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R2
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L2
22u
X1
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C1
*
R1
10R
L1
100n
D2
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D1
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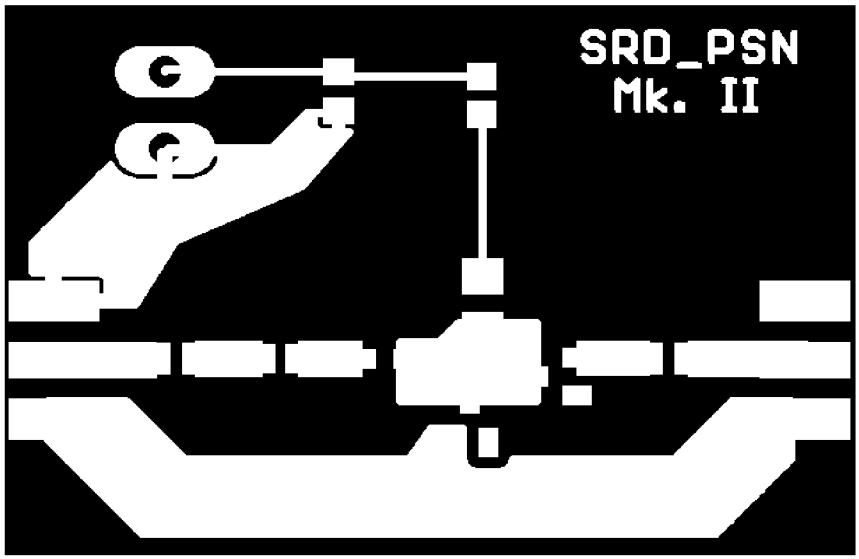
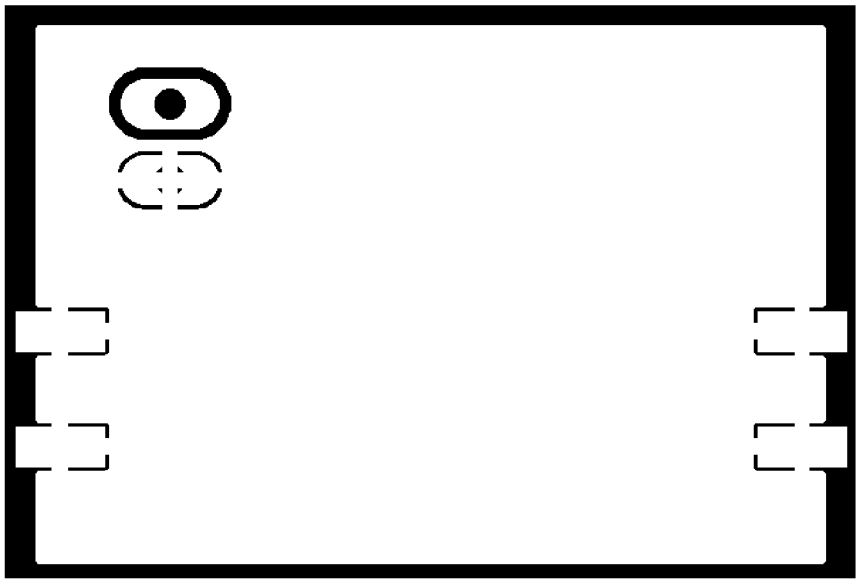
GND

B Printed circuit boards

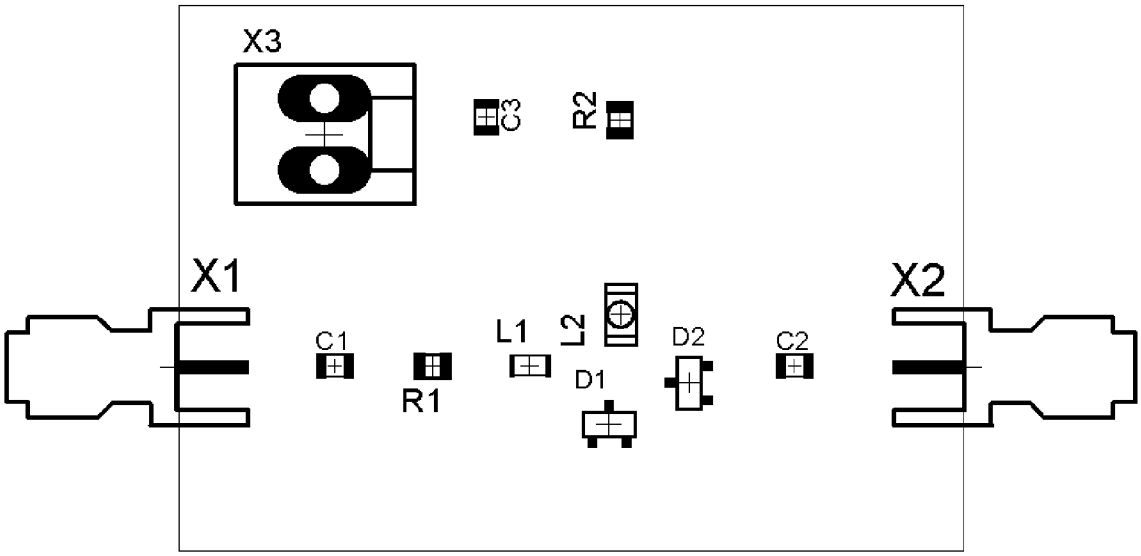
B.1 PSN - Top layer



B.2 PSN - Bottom layer

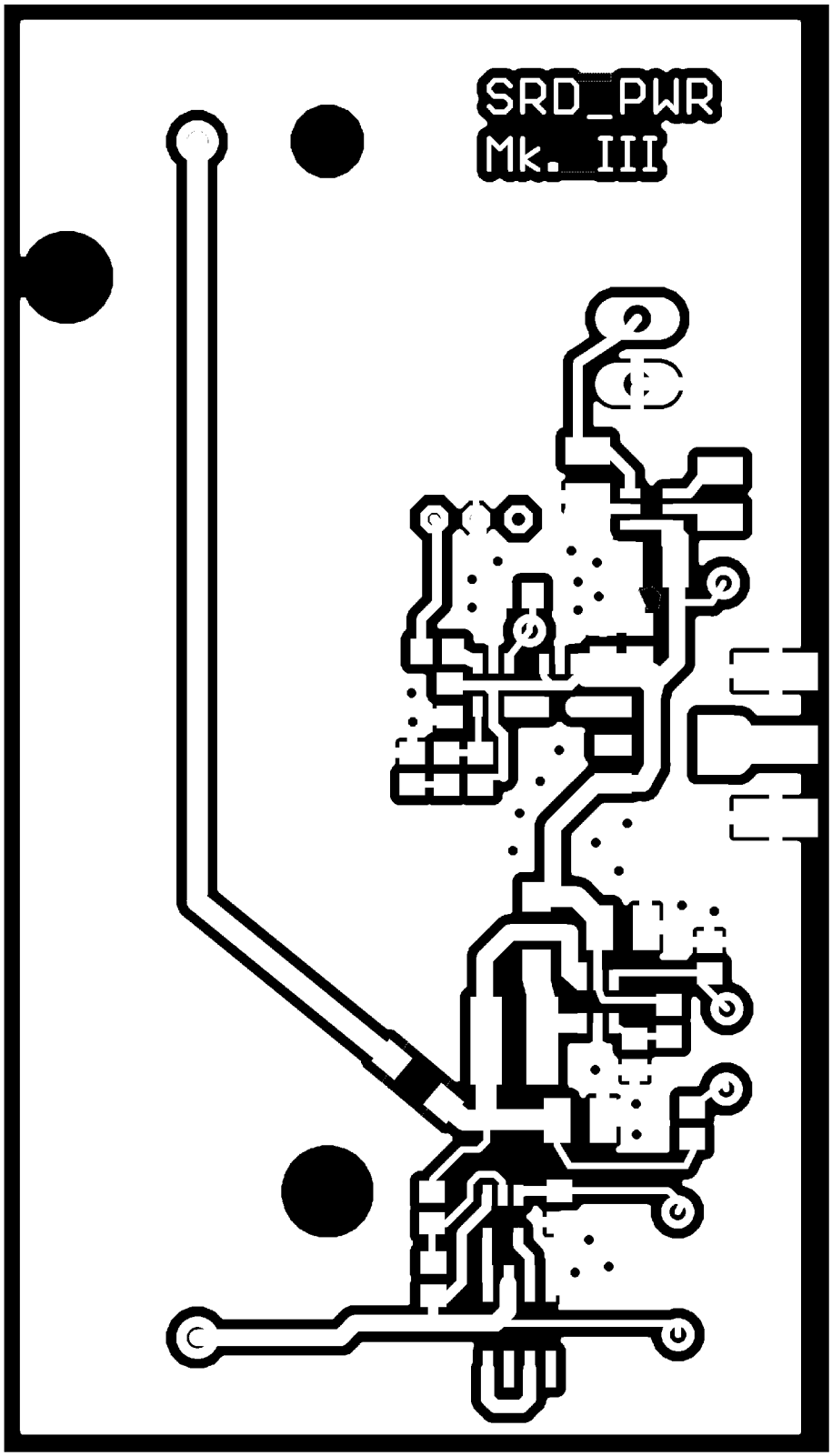


B.3 PSN - Component placement

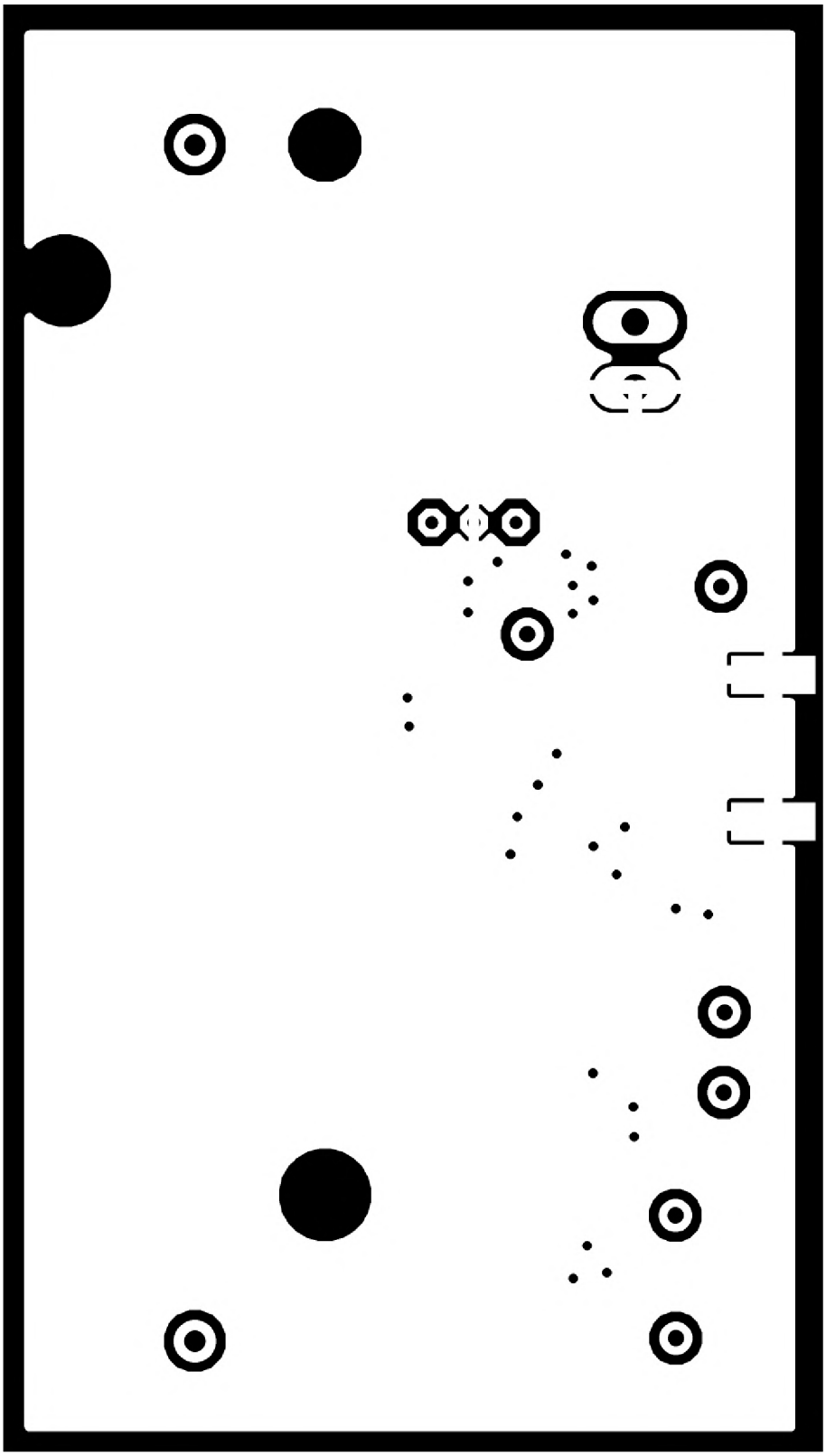


Board dimensions: 43 x 30 mm

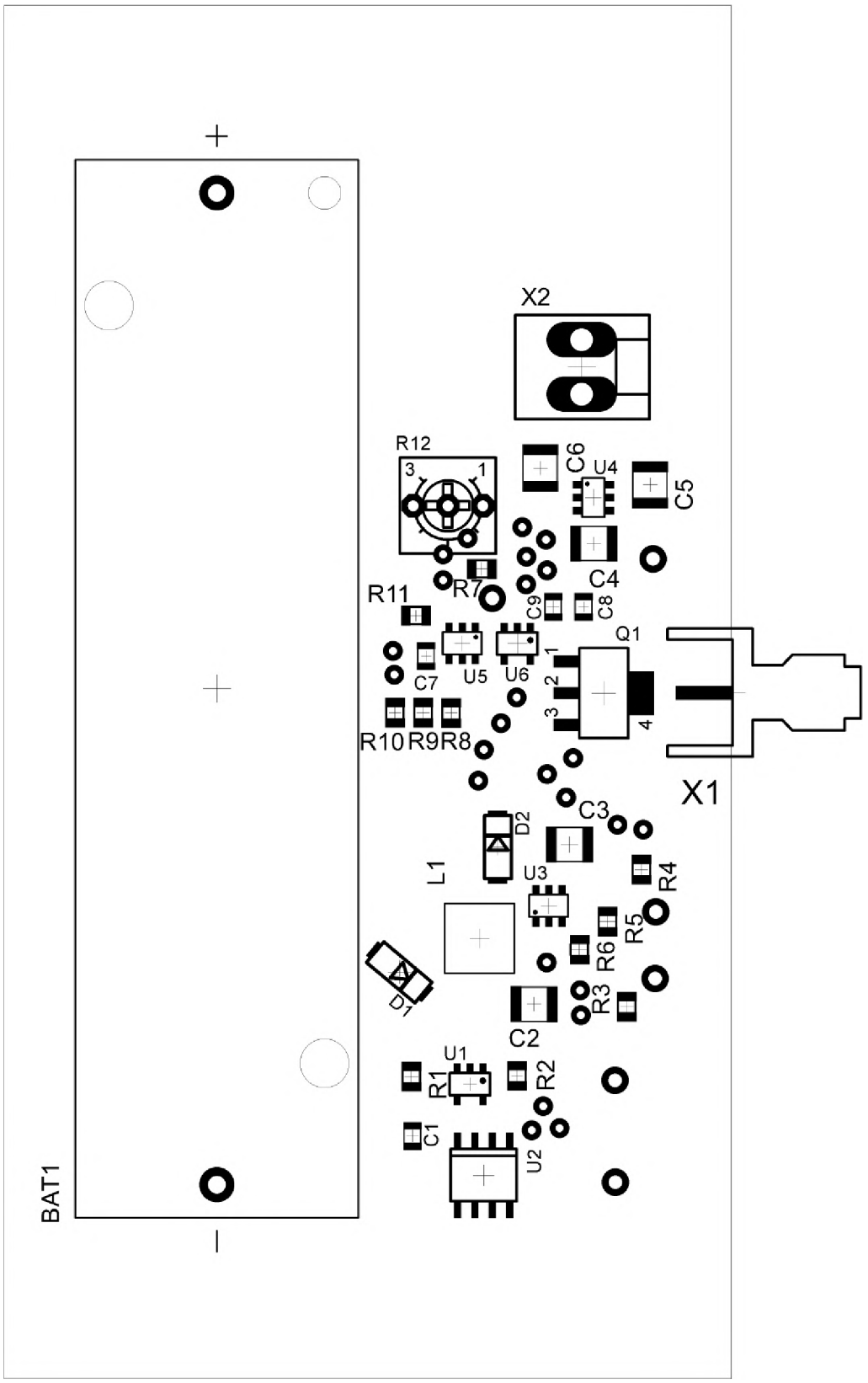
B.4 Power & Driver - Top layer



B.5 Power & Driver - Bottom layer



B.6 Power & Driver - Component placement



Board dimensions: 100 x 53 mm

C List of components

C.1 PSN

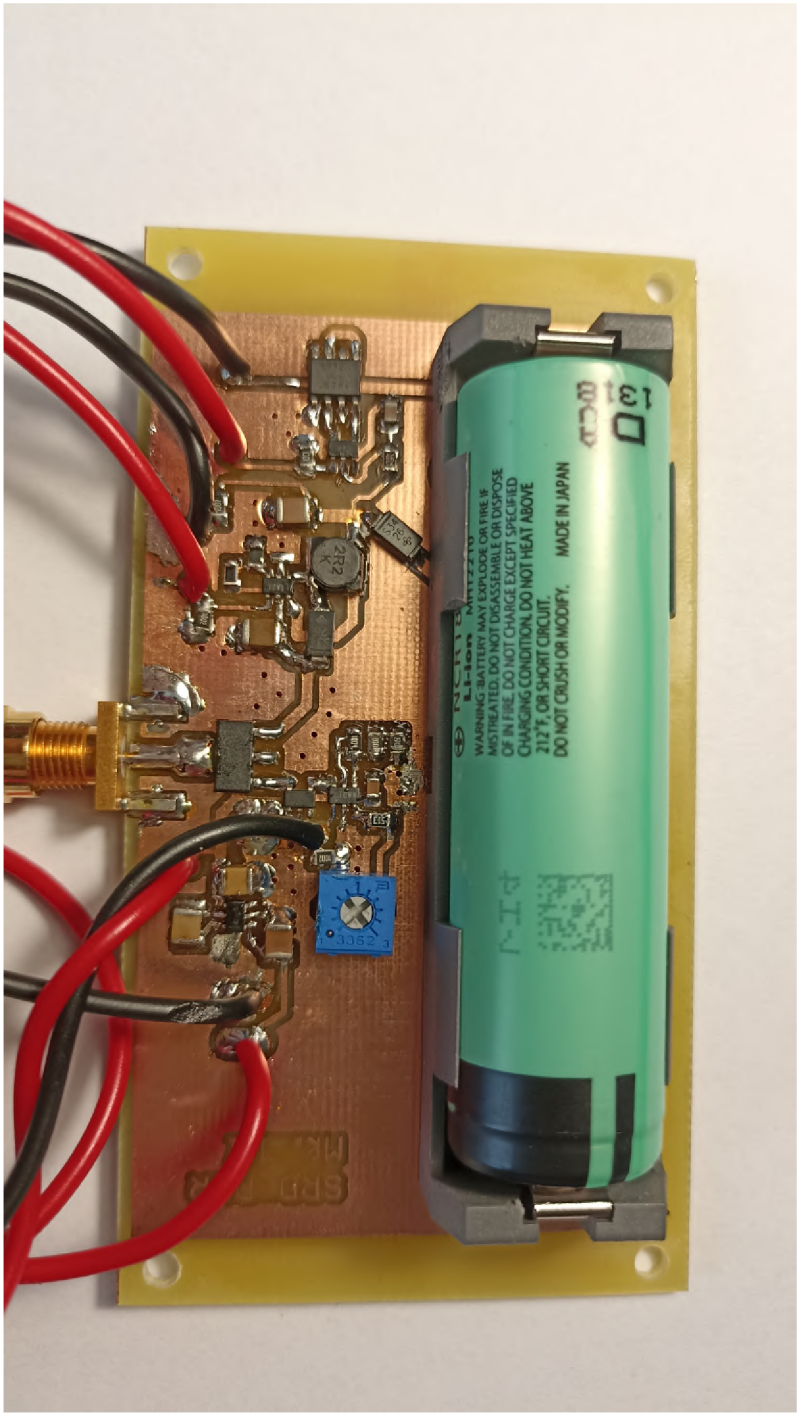
Parts	Value	Package
C1	*	C0805K
C3	100n	C0805K
L1	100n	L0805
R1	10R	R0805
C2	10n	C0805K
R2	120R	R0805
L2	22u	L3225P
D2	BAT15-04R	SOT23
X3		KK-156-2
D1	MA144769	SOT23
X1, X2	SMA(F) Jack	J502-ND-142-0701-801/806

C.2 Power & Driver

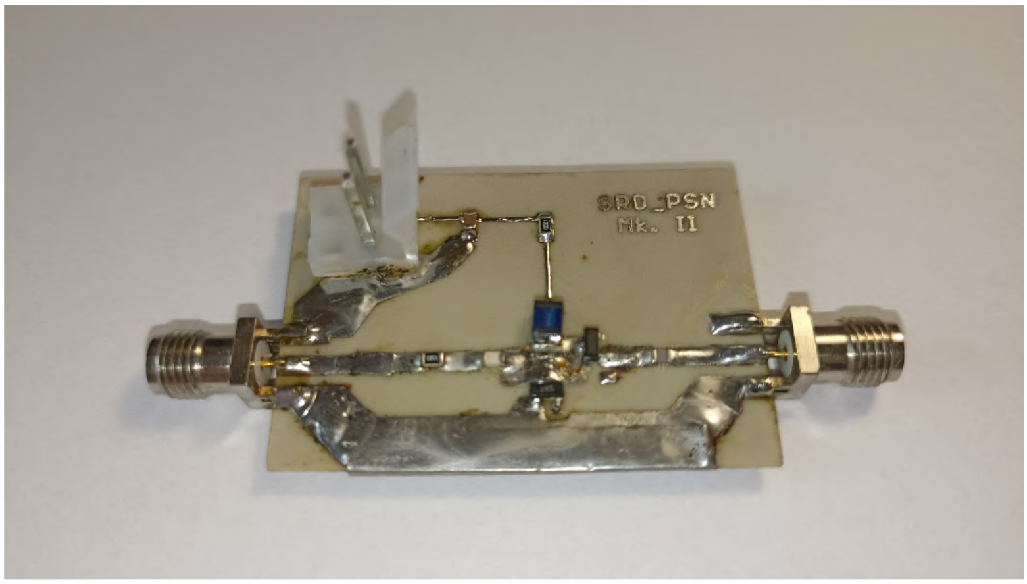
Parts	Value	Package
X2		KK-156-2
C1, C7, C9	100n	C0805K
R9	10K	R0805
R3, R4, R7	10k	R0805
C2, C6	10u	C1210
BAT1	18650-1043	18650-1043
R2	1K	R0805
R8	1M	R0805
C5	1u	C1210
C4	2.2u	C1210
L1	2.2u	L-5x5mm
C3	22u	C1210
R10	270K	R0805
R6	30.9K	R0805
C8	4.7u	C0805K
R1	470R	R0805
R12	500K	3362U
R11	50K	R0805
R5	95.3K	R0805
Q1	BSP322P	SOT223
U4	LM2776	SOT23-6L
U3	LTC3426	SOT23-6L
U5	LTC6990	SOT23-6L
U1	S-8241	SOT23-5L
U2	SI4900DY	SO8
X1	SMA(F) Jack	J502-ND-142-0701-801/806
D1, D2	SSA34	DO214AC
U6	UCC27517A-Q1	SOT23-5L

D Photos

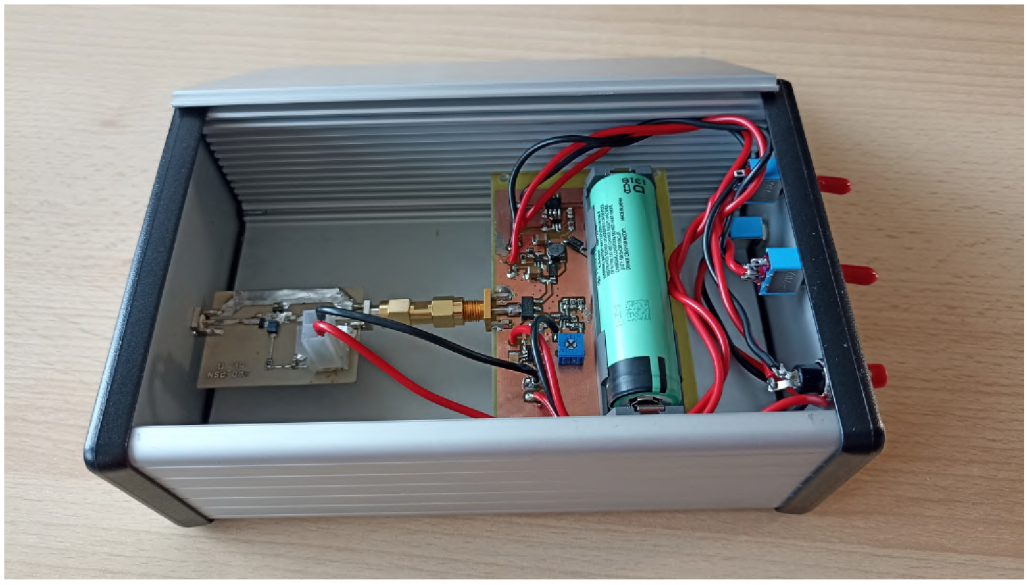
D.1 Power & Driver



D.2 PSN



D.3 Inside enclosure



E Instructions

BATT. SET - press after first inserting the battery
The switches should be activated in the order SUPPLY -> BIAS -> OUT.