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ANALOG SIGNAL PROCESSING WITH INTEGRATED CURRENT FEEDBACK AMPLIFIERS

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ABSTRACT

This dissertation thesis deals with the design of new functional blocks usable in area of analogue signal processing. The current feedback circuits (which in a suitable configuration can operate in voltage or current mode) are used here. This allows to achieve very promising results in the systems with a very low power supply. The versatility of the circuits will find applications in many areas. The current-feedback amplifier is chosen as the main building block for the detailed studies on the analog signal processing circuit design and realisation through various RC configurations. The thesis deals mainly with the study, synthesis, and design aspects of deriving new immittance functions covering inductive and supercapacitive admittances, current conveyors, voltage conveyors, high quality selective filters utilizing the transimpedance, integrators and differentiators, non-minimum phase allpass equalizers, and voltage controlled oscillators. The work deals in detail with these new particular blocks which are described theoretically and evaluated by simulations.

KEYWORDS

Analog signal processing, operational amplifier, current feedback amplifier, conveyor, integrator, differentiator, sensitivity

ANOTACE

Tato disertační práce pojednává o návrhu nových funkčních bloků použitelných v oblasti zpracování analogového signálu. Jde o obvody v proudové módu, které mohou ve vhodné konfiguraci pracovat v proudovém i v napěťovém módu. To umožnilo získat velmi nadějně výsledky v soustavách s nízkým napájecím napětím. Mnohostrannost těchto obvodů nalezne uplatnění v mnoha aplikacích. Zesilovač s proudovou zpětnou vazbou byl zvolen jako hlavní stavební blok pro detailní zkoumání funkce obvodů s RC operační sítí. Tato disertační práce pojednává o studiu, syntéze a návrhových aspektech realizace nových imitančních funkcí, jmenovitě induktivních a superkapacitních, proudových a napěťových konvejorech, kmitočtových filtrech s velkou jakostí, integrátorech a diferenciátorech, fázovacích členech s neminimální fází a napětím řízených oscilátorech. Disertační práce se detailně zabývá těmito novými bloky, které jsou popsány teoreticky a vyhodnoceny na základě simulací vlastností.

KLÍČOVÁ SLOVA

Zpracování analogového signálu, operační zesilovač, zesilovač s proudovou zpětnou vazbou, konvektor, integrátor, diferenciátor, citlivost

List of used shorts and symbols

<i>ASP</i>	Analog Signal Processing
<i>BP</i>	Band Pass
<i>CMOS</i>	Complementary Metal Oxide Semiconductor
<i>CCCS</i>	Current Controlled Current Source
<i>CFA</i>	Current Feedback Amplifier
<i>DAC</i>	Digital to Analog Converter
<i>DVCCS</i>	Differential Voltage Controlled Current Source
<i>DIL</i>	Double Integrator Loop
$F(p)$	Complex Variable (also s)
<i>FDNR</i>	Frequency Depend Negative Resistance
<i>FET</i>	Field Effect Transistor
<i>GB</i>	Gain Bandwidth
<i>HP</i>	High Pass
<i>LP</i>	Low Pass
<i>LSI</i>	Large Scale Integration
<i>MP</i>	Microprocessor
<i>IC</i>	Integrated Circuit
<i>OA</i>	Operation Amplifier
<i>OTA</i>	Operation Transconductance Amplifier
<i>PLL</i>	Phase Locked Loop
<i>PRA</i>	Programmable Resistor Array
<i>VCI</i>	Voltage Controlled Integrator
<i>VCO</i>	Voltage Controlled Oscillator
<i>VCD</i>	Voltage Controlled Differentiator
<i>VCSO</i>	Voltage Controlled Sinusoid Oscillator
<i>VLSI</i>	Very Large Scale Integration
<i>VCVS</i>	Voltage Controlled Voltage Source
V_1	voltage amplitude
<i>Z</i>	impedance

1. INTRODUCTION

During the years the analog, but also the digital designers began to think and calculate only in terms of voltages rather than currents, although many of the signals handled by the analog circuits are actually currents in their initial state. Examining the analog paths of the signal processing system in Fig. 1.1. shows that the output signals of the sensors, which are often currents or charge, were first converted to voltages by I/V converters, before they were processed in pure voltage signal processing circuits; see Fig. 1.2. The pre-processed voltage was input signal. A similar situation occurred at the output of the signal processing system, where the output current of the D/A converter was first converted to voltage, the post-processed and finally often converted back to current to drive a physical transducer.

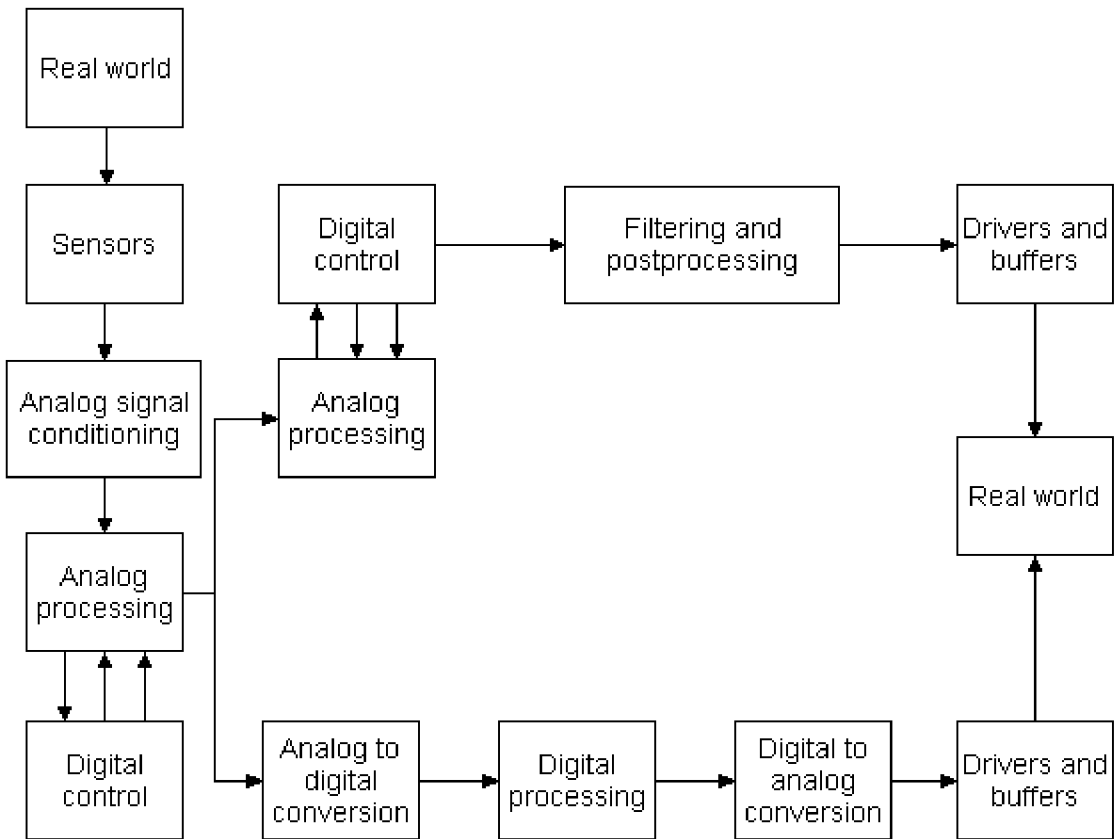


Fig. 1.1: General signal processing system [1]

A much simpler way here is to use analog circuits directly processing the signals in form of currents, like indicated in Fig. 1.3. This would skip the V/I and I/V converters necessary to adjust the input signal for voltage processing and for converting to digital signals. The chip area as well as the energy needed to drive the signal processing could be higher, because a possible sources of errors would be cancelled too.

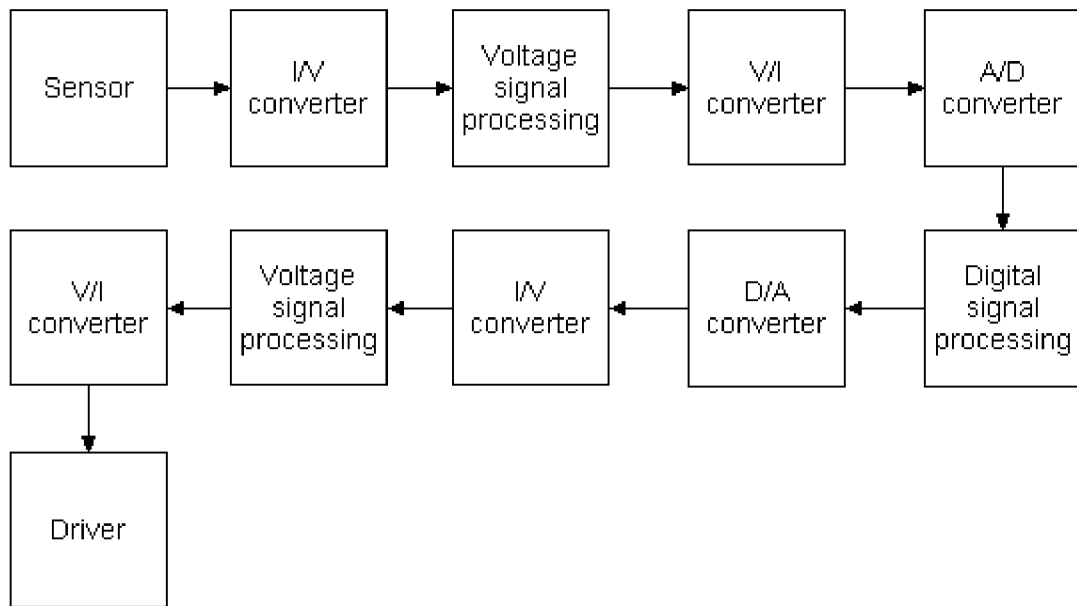


Fig. 1.2: Voltage signal processing system [1]

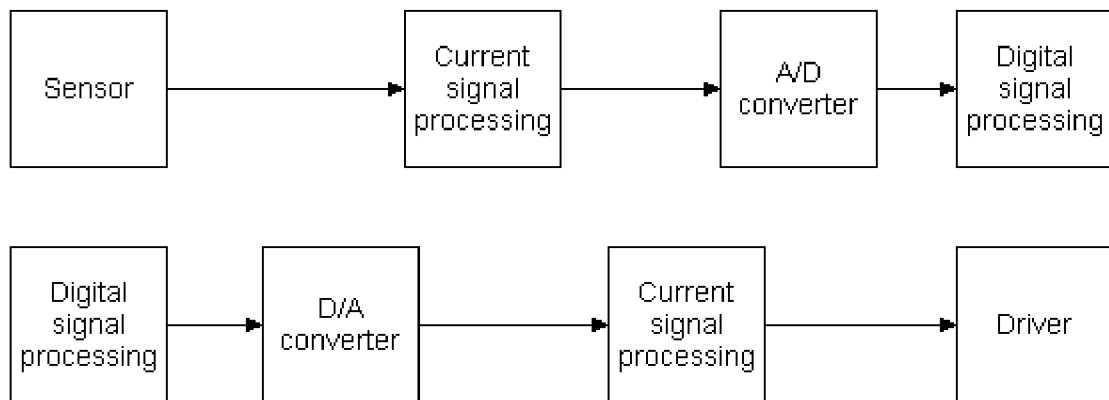


Fig. 1.3: Current signal processing system [1]

The reason, why current signal processing was not able to establish itself until now, was the missing high-performance current processing circuits. While there are number of well established building blocks for voltage processing ones, e.g. operational amplifiers, comparators, etc., there was not enough attention paid to the design of similar building blocks for current processing circuits.

A current conveyor belongs among those current processing blocks. It is very useful building block consisting of both voltage and current sub-blocks. Current conveyors were introduced in the late sixties, early seventies by Smith and Sedra. They were considered to be used as controlled voltage and current sources, impedance converters, etc., but also as function

generators, amplifiers, filters, etc., in current processing circuits mainly for instrumentation and measurement applications.

In the first years of their appearance the performance of current conveyors was severely limited by the available technologies, which didn't allow well-matched devices on fabricated chips. Since the technologies have improved, the current gained attention of many analog designers. Today the current conveyors have developed to very useful building blocks of analog electronics and their main application areas are in high-speed, high-frequency circuits for both voltage and current signal processing.

A conveyor is generally a three-port device (except special types) operating mostly in the current mode. It consists of two blocks, a voltage VF and a current CF follower. By the order of their arrangement, a voltage (Fig. 1.4) and a current (Fig. 1.5) conveyor can be recognized.

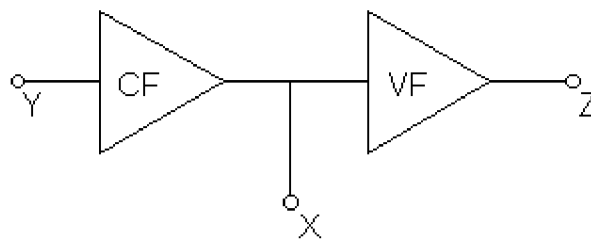


Fig. 1.4: Voltage conveyor

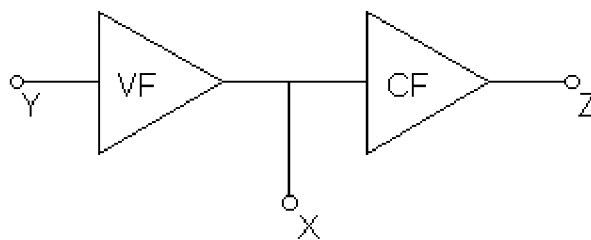


Fig. 1.5: Current conveyor

2. AIM OF DISSERTATION

This work is focused on the field of the active building blocks for the modern integrated circuits operated in current-mode or mixed-mode.

The main idea of the thesis consists in taking a commercially available modern integrated circuit-CFA and studying its application in various new electronic blocks even if some of them are already known in their voltage-mode versions. The thesis will be more oriented to the applied research than to the fundamental one and focused to the currently available current mode amplifiers.

Aims of the dissertation are in the following:

- 1) Investigations of the effects of the imperfections in current mode amplifiers.
- 2) Design and verification of the insensitive circuits with current mode amplifiers.
- 3) New designs of an integrator and a differentiator in both current- mode and voltage-mode forms.

3. STATE-OF-THE-ART

Analogue integrated circuit design is becoming increasingly important with growing opportunities. IC processing techniques have now evolved to the point where high-performance and novel “special” devices are being integrated. This in turn has led to a renewed interest in circuit design techniques, which were previously limited by the technology available – essentially we are now seeing technology-driven advances in circuit design. An example is the development of “current-mode” techniques (Toumazou 1990, Current mode approach [11]), many of which have only become practically feasible with the development of true complementary bipolar and MOS technology processes.

Voltage-mode analogue circuit design has called as a “traditional” nowadays. Current-mode signal processing circuits have recently demonstrated many advantages over their voltage-mode counterparts including increased bandwidth, higher dynamic range and better suitability for operational in reduced supply environments (e.g. supply voltage 3.3 V and lower). In addition, current-mode processing often lead to simpler circuitry (e.g. processing of current signals from measurements probes) and lower consumption.

There are some limitations in obtaining high current gain and wide bandwidth for low offset current and high-speed gain operation. Usually, higher gain can be achieved by using a closed-loop feedback gain configuration formed by a feedback resistor ratio. The signal processing speed is determined by the amount of voltage swing on each delay path. Ideally, a current-controlled current source (CCCS) has zero input impedance and infinite output impedance. The conceptual justification for high-speed operation in current-mode circuit results from the small voltage swing of each low-impedance node, operation near transition frequency f_T , and wide-band frequency response.

In CMOS technology developments have centred on a new generation of analogue sampled data processing that may refer to as switched or dynamic current circuits. These circuits include switched current filters, dynamic current mirrors and current copier and memory cells. At the other hand, there have been developed novel special analogue building blocks opposite to voltage-mode classical blocks. These blocks, including current amplifiers, current followers, current conveyors and others, can be called as “adjoint” refer to voltage amplifiers, voltage comparators, followers and so on. One of the primary motivations behind these developments has been the shrinking feature size of digital CMOS devices, which necessitates the reduction of supply voltages. This is the fact that 3.3 V is CMOS process standard nowadays (near future follows 1.5 V). Due this, process parameters such as threshold voltage will be chosen to optimise digital performance and so voltage domain behaviour will suffer as

a consequence. Such difficulties can be overcome by operating exclusively or selectively in the current domain. Current conveyor and current follower based filters replace traditional voltage-mode filters. Similarly current-mode implementations of VLSI CMOS A to D converters and neural computing processors represent exciting new developments and are clear examples of technology driven design. CMOS technology has become a dominant analogue technology because of good quality capacitors and switches. BiCMOS technology combines both the advantages of bipolar and CMOS providing a very attractive low power, high-speed technology for which current-mode techniques would be ideally suited.

Furthermore, with maturing CMOS VLSI, BiCMOS and true complementary bipolar technology, current-mode analogue design techniques play an important role in successfully exploiting these technologies in the analogue domain. As a consequence many of the early current-mode circuit techniques are enjoying a renaissance and a new generation of current-mode analogue building blocks and systems are being developed and described throughout this thesis.

The advancement of the semiconductor technology in the recent past had significant impact to the research and development (R&D) activities on electronic circuit and systems with vast coverage on Analog signal processing (ASP). The impact had renewed impetus with introduction of the versatile monolithic integrated circuit (IC) building block termed as Operational amplifier (OA) [21, 22].

The OA device is essentially a voltage controlled voltage source (VCVS) element. Since its inception, the OA element had been widely used for various voltage mode circuit design covering widespread areas of applicabilities in ASP [21, 22].

Among these, the design of passive inductorless active OA-RC function circuits, e.g., selective filters, phase equalizers, wave processors like integrators / differentiator, wave generator are quite popular, useful and IC- adaptable, since passive inductances are not compatible to IC technology . The approach subsequently gave way to synthesizing active immittance functions by OA-RC methods. During this course of research activity, Bruton suggested a new type of immittance function known as the Frequency Dependent Negative Resistance (FDNR) [24]. Popularized later either as Supercapacitor ($Y(p) = p^2$) or Superinductor ($Y(p) = p^{-2}$). In course of the progress on ASP circuit and system (CAS) design there emerged newer types of active building block viz., the Operational Transconductance Amplifier (OTA) and the current conveyor (CC) [12 - 20]. The OTA is essentially a Differential Voltage Controlled Current Source (DVCCS). Whereas the Current Conveyor is basically a Current Controlled Current Source (CCCS) element suitable for

current mode ASP [36-38]. Many workers had contributed elegant schemes on ASP function circuit design using the OTA and the current conveyor in its various forms in the recent past [11].

Most recently, another new device, known as the Current Feedback Amplifier (CFA) had been introduced which is a versatile building block compatible to both voltage mode and current mode functioning [11]. This is essentially a unity gain current transfer device wherein the voltage across its trans impedance can be copied at a voltage source output nodes.

The unique property of the device, now commercially available as an off the shelf items as AD-844 IC. The notable advantage of the device may be summarized as:

- accurate port transfer characteristics at extremely low tracking errors
- improved ac performance with better linearity.
- gain-independent constant bandwidth at moderate to high gains.
- high slew rate (SR) specification.
- both current and voltage signal cascadability
- low sensitivity design owing to accurate port tracking property.
- fast settling time.

Recently the CFA element is receiving considerable interest on the R&D activities in areas of ASP Circuits [25, 26]. In particular, the features of high SR and fast settling speed make the CFA readily adaptable to some special function circuits, video amplifiers, analog dividers, D/A current to voltage converters, high frequency current copiers, high speed data communication system etc.

Albeit many analog only domain CFA-based ASP designs had been presented in the literature, there is further possibility of R&D work in the domain of mixed analog-digital mode signal processing applications wherein the tuning component of an analog function circuit can be tuned through a digital word(code) [27,28].

We have chosen the CFA as the potential active element for our work on ASP circuit design and realization schemes through CFA-RC configurations in the thesis.

We like to study the design, synthesis and realization as aspects of deriving new immittance functions covering inductive and super capacitive admittances, high quality selective filters utilizing the CFA trans impedance integrators/ differentiators, non-minimum phase all pass(AP) equalizers, and Sine wave oscillators/Voltage Controlled Oscillator (VOC) [29].

4. CURRENT AND VOLTAGE CONVEYORS

Classical voltage operational amplifier (VOA) is a one of the most famous and common used blocks. VOA can be described as active building block that operates in voltage-mode. Another similar block is voltage follower (VF). A number of blocks with reciprocal behavior to previous voltage mode blocks have been proposed during last 15 years. Current operational amplifier (COA) and current follower (CF) can be mention as examples.

Moreover, some of basic building blocks can operate in both, voltage and current, modes. This type of bocks has been sorted as mixed-mode. Mixed-mode block usually has both, "voltage" and "current" terminals. The most famous mixed-mode active block is current conveyor [2, 3]. Nowadays becomes renaissance of these universal building blocks. Current conveyors appear in many modern constructions of wideband and high-speed operational amplifiers, etc.

4.1. CURRENT CONVEYORS - HISTORY AND PRESENCE [20]

One of the most basic building blocks in the area of current-mode analogue signal processing is the current conveyor (CC). It is a four (in basic form) terminal device which when arranged with other electronic elements in specific circuitry can perform many useful analogue signal processing functions. In many ways current conveyor simplifies circuit design in much the same manner as the conventional operational amplifier. The current conveyor offers an alternative way of abstracting complex circuit functions, thus aiding in the creation of new and useful implementations. Moreover, CC is a mixed-mode universal building block (in VLSI terms), which can substitute classical op-amps in voltage-mode applications or gives us chance to transform these applications to current-mode.

Many papers have demonstrated the universality, advantages and novel applications of the current conveyor since its first introduction in 1968 [2]. Concurrently with these papers, a number of authors have outlined improved implementations designed to enhance the performance and utility of this circuit building block. Unfortunately, there is still lack of available current conveyors in form of IC. Many designers cannot use this block in their developed applications and systems due this. If the situation will change, the designers will get the chance to be more familiar with the current conveyor and its usability. There is only one monolithic IC of "pure" current conveyor – CCII01. Paradoxically, many novel constructions of modern wideband and high-speed op-amps are based on current conveyor (OPA660, AD840).

In following chapters are reported existing types of current conveyor and will be discuss novel types and techniques that lead to improvement of their features.

4.2. CURRENT CONVEYOR OF THE 1ST. GENERATION – CCI

The *current conveyor* was originally introduced as 3-port device [2]. The operation of this device can be described by followings terms: if a voltage is applied to input terminal Y, an equal potential will appear on the input terminal X. In a similar fashion, an input current I being forced into terminal X will result in an equal amount of current flowing into terminal Y. Finally, the current I will be conveyed to output Z. Note, that Y output has characteristics of a current source of value I with high output impedance. Voltage at X terminal is independent on the current forced into this port. Similarly, the current flows through input Y is fixed by current through X terminal and is independent on Y potential. The CCI device exhibits a virtual short-circuit input characteristics at port X and dual virtual open-circuit input characteristic at port Y. This functionality can be described by following hybrid equation:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \quad (1)$$

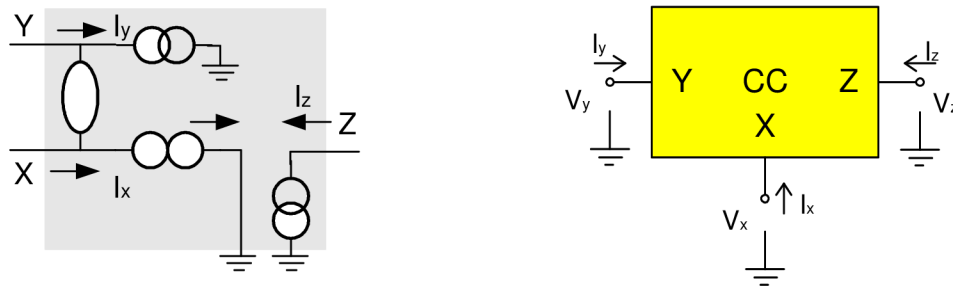
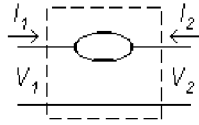
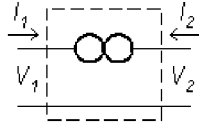
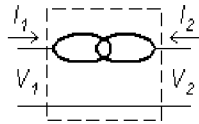
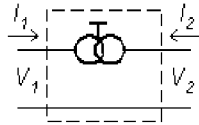


Fig. 4.1: CCI nullator-norator model and block diagram

Macromodels of conveyors types are used in this section. Macromodels consist from basic ideal elements – nullator, norator, ideal current- and voltage-sources, Tab. 4.1.

Basic elements		
Type	Symbol	Definition
nullator		$V_1 = V_2$ $I_1 = I_2 = 0$
norator		$I_1 = -I_2$ $V_1, V_2 \text{ are arbitrary}$
voltage mirror		$V_1 = -V_2$ $I_1 = I_2 = 0$
current mirror		$I_1 = I_2$ $V_1, V_2 \text{ are arbitrary}$

Tab. 4.1: Basic elements

4.3. CURRENT CONVEYOR OF THE 2ND GENERATION – CCII

To increase the versatility of the current conveyor, a second generation in which no current flows in terminal Y, was introduced [9]. This building block has since proven be more useful than CCI. CCI can be described by following matrix:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \quad (2)$$

From above equations is clear that terminal Y exhibits infinite input impedance. The voltage at X terminal follows the Y potential, X exhibits zero input impedance, and current flows through X port is again conveyed to the high impedance current output Z. Current flows

through Z terminal has same orientation as current through the terminal X (CCII+) or opposite polarity in case of CCII-.

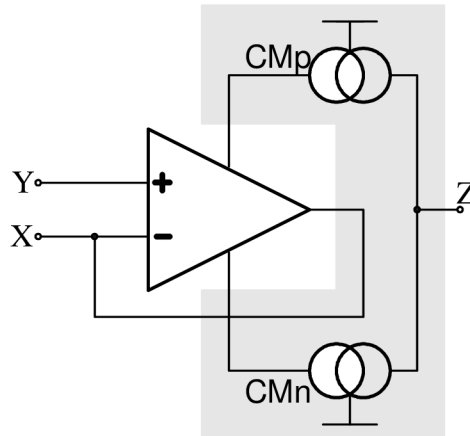


Fig. 4.2: CCII based on classical voltage opamp

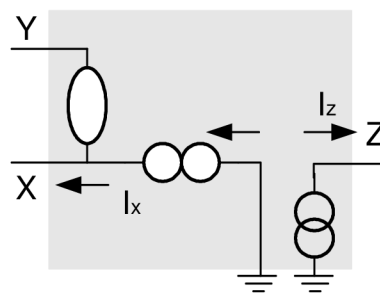


Fig. 4.3: CCI nullator-norator model and simple CMOS implementation

CCII has proven to be by far the more useful of the current conveyor family types. Wide range of applications was published. It's very suitable building block for design of the active-RC filters or number of special imittance (admittance) converters. In the last decade the number of high-speed and wide-range opamps are based on current conveyor structure. And also for low voltage applications CCII is starting to be very powerful building block.

5. CFA-BASED DESIGN OF ACTIVE IMMITTANCE

The CFA device we propose some new design schemes for low sensitivity immittance functions using CFA device. The proposed design is for deriving the driving point admittance for

- i. ideal inductance (L)
- ii. ideal supercapacitor type FDNR (D)

The topic of inductive (L) and FDNR type (D) immittance function simulation had been examined by various researchers using Operational amplifier (OA) current conveyor (CC) [49, 55-59] and the differential voltage controlled current source (DVCCS) devices [12 - 20].

We propose similar function realization schemes using the most recent device, the current feedback amplifier (CFA). The advantages of such CFA based realizations are derived mainly owing to the accurate port tracking characteristics of the CFA device which leads to practically insensitive design [29, 30].

The effects of the port tracking errors on the simulation element L and D were examined and subsequent compensation design equation have been derived. First we present the inductance simulation followed by the FDNR simulation scheme.

Measurement on the VI characteristics of the proposed inductor exhibited good quality response of the synthetic coil up to 330 kHz. Responses of frequency selective resonator circuit using the simulated element have been examined. The responses were verified both with hardware implementation and by PSPICE macro model simulation.

5.1. ANALYSIS FOR INDUCTANCE L

The CFA device we propose some new design schemes for low sensitivity imittance. The CFC is a 3- terminal current mode device with port relations

$$\begin{pmatrix} I_y \\ V_x \\ I_z \end{pmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta & 0 & 0 \\ 0 & \pm a & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \text{ and } V_0 = \delta V_z \quad (5.1)$$

Where the port transfer ratio may be expressed in terms of error coefficients (ϵ) as

$$\alpha = 1 - \epsilon_i \quad \beta = 1 - \epsilon_v \quad \delta = 1 - \epsilon_z \quad (5.2)$$

According to available literature report these tracking errors are extremely small

$$(0.01 \leq \epsilon_{i,v,z} \leq 0.004)$$

Analysis of the proposed circuit in Fig. 5.1 using the above expression, we get the driving point admittance.

$$Y_i = (\alpha_1 \alpha_2 \beta_1 \beta_2) (y_1 y_2 / y_0) \quad (5.3)$$

The derivation of this equation does not necessitate any reliability condition. For a lossless inductor assuming ideal ($\alpha = \beta = \delta = 1, \epsilon_{i,v,z} = 0$) CFAs, we may select

$$\begin{aligned} Y_0 &= pC; \quad Y_{1,2} = 1/R_{1,2} \\ L_{eq} &= CR_1 R_2 \end{aligned} \quad (5.4)$$

The inductance value slightly increases because of the increment in the resistor value given by

$$\left. \begin{aligned} \tilde{R}J &= RJ(1 + \epsilon_{0j}) \\ \text{Where } \epsilon_{0j} &= 1 - (\epsilon_{ij} + \epsilon_{vj}) \end{aligned} \right\} \quad (5.5)$$

Here products of error terms have been neglected since $\epsilon_{i,v,z} \ll 1$.

The inductance may be varied independently by any of the RC components. In the event of non ideal CFAs ($\epsilon_{i,v,z} \neq 0$), the modified impedance function is

$$Z'_i = pCR'_1 R'_2 = pL'_{eq} \quad (5.6)$$

$$\text{where } R'_j = R/\alpha_j\beta_j; \quad j=1,2 \quad (5.7)$$

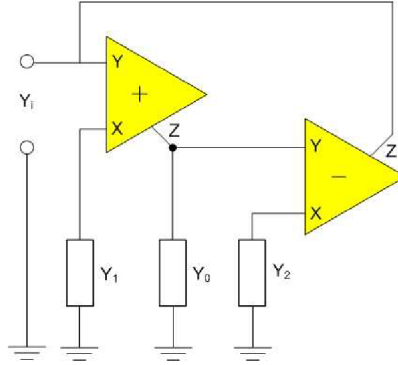


Fig. 5.1: Lossless grounded inductor

On the Fig. 5.1. is lossless grounded inductor ($L_{eq} = CR_1R_2$) with $y_{1,2} = 1/R_{1,2}$ and $y_0 = pC$.

5.2. COMPENSATION DESIGN

The compensation scheme calls the reduction of increments indicated in eq. (5.5) caused by the port errors of the non ideal CFAs. This may be done by shunting $R_{1,2}$ by suitable compensating resistors $r_{1,2}$ given

$$\tilde{R}_j^{-1} + r_j^{-1} = R_j^{-1} \quad j = 1,2 \quad (5.8)$$

Which yields the compensation design equation

$$r_j = R_j / \epsilon_{0j} \quad j = 1,2 \quad (5.9)$$

5.3. SENSITIVITY

The classical sensitivity figure may be defined $(S_a^b) = a(db)/b(da)$ the active sensitivity figures for the simulated inductance are given by

$$\left. \begin{aligned}
s_{\epsilon_{j,v_j}}^L &= \frac{\epsilon_{j,v_j}}{1 + \epsilon_{01} + \epsilon_{02}} \ll 1 \\
s_{\epsilon_j}^L &= 0
\end{aligned} \right\} \quad j = 1, 2 \quad (5.10)$$

The immittance function realization is therefore practically active insensitive. The passive sensitivity may be computed considering the fractional change expressed in terms of the sensitivity summation and incremental change in RC components (due to temperature variations , ageing .) given by

$$\Delta L / L = \sum_{j=1}^2 (S_{R_j}^L) (\Delta R_j / R_j) + S_C^L (\Delta C / C) \quad (5.11)$$

In monolithic or hybrid IC Technology , increments in one kind of component track quite closely, i.e., $\Delta R_j / R_j = \Delta R / R$. Calculation of the sensitivity and noting that average fractional change in resistors can be made equal to that of capacitors, we get $\Delta L / L = (\Delta R / R) + (\Delta C / C)$. It is possible to get RC components with equal opposite temperature coefficients in thin film technology i.e., $\Delta R = -\Delta C$; therefore

$$\Delta L / L = 0 \quad (5.12)$$

Hence the incremental passive sensitivities may be significantly reduced with appropriately matched RC components in microcircuit fabrication .It may be noted in eq.(5.3) that even with nonideal CFA devices, the proposed configuration is able to realize lossless inductance element, but with slightly altered magnitude an added advantage.

5.4. FLOATING IMMITTANCE

The circuit of Fig. 5.1 may be modified for the realization of floating lossless inductor, by insertion of another CFA as shown in FIG. 5.2 a unity gain buffer may be needed to isolate y_1 from the input port. Here the realizability condition is $y_2 = y_3$, and for a floating inductive immittance we make $y_0 = pC$, $y_1 = y_3 = 1/R$ then the driving point admittance matrix is

$$Y = \begin{bmatrix} 1 \\ pL_{eq} \end{bmatrix} \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \quad (5.13)$$

where $L_{eq} = CR^2$

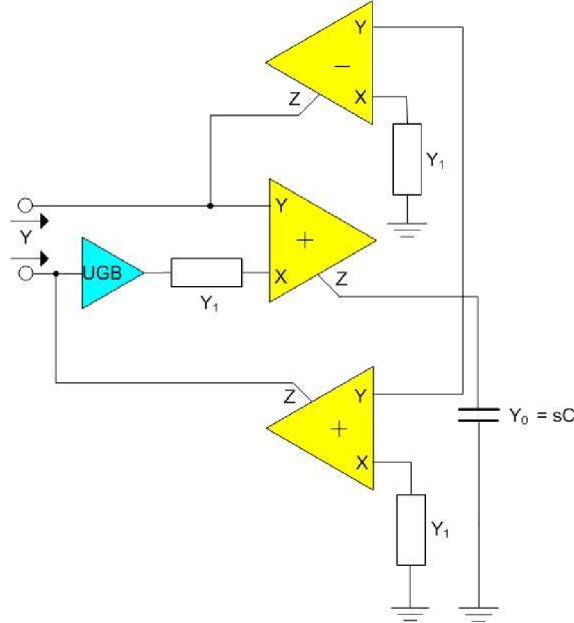


Fig. 5.2: Lossless grounded inductor ($L_{eq} = CR^2$) with $y_1 = y_2 = 1/R$ and $y_0 = pC$.

5.5. AN INSENSITIVE IDEAL SUPERCAPACITOR

A super capacitor type FDNR (D) element is a second order immittance function which is generally obtained by the frequency transformation of capacitive immittance (sc) multiplied by a Laplace operator $s\tau$, that yields $D = C\tau$. The driving point admittance (Y_i) has been synthesized as multiplicative form $Y_i = Y_a \cdot Y_b / K$ where K must be another admittance for dimensional equality. The CFA device with a high gain operational Amplifier (OA) in the feedback loop as in Fig 5.2(b) has been used to generate an immittance function of the form $Y_{in} = Y_a \cdot Y_b / Y_c$, The port errors introduce slight deviations in the element values (D' or L') and there appears some shunt lossy terms (r_x with L, C_x with D) whose effects are insignificant since $\epsilon \ll 1$. A simple design application of the FNDR- a third order low pass Butterworth filter realization had been proposed and maximally flat response had been verified.

5.6. ANALYSIS FOR SUPERCAPACITOR

Analysis of the circuit in Fig. 5.3 using the ideal CFA ($\epsilon = 0$), yields

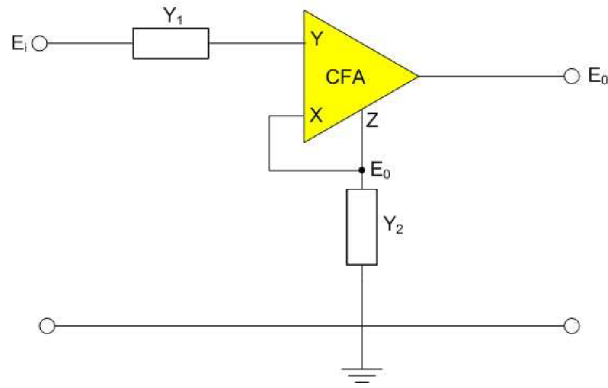


Fig. 5.3: Realization of $F(p)$

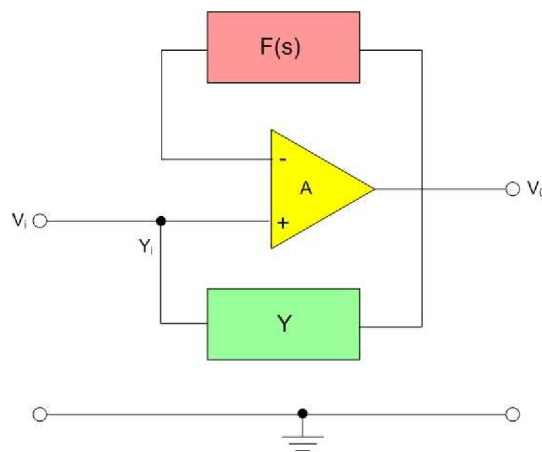


Fig. 5.4: Generation of Inverse of $F(p)$

$$E_o / E_i = Y_1 / (Y_1 - Y_2) \quad (5.14)$$

$$E_o / E_i = Y_1 / (Y_1 - Y_2) \quad (5.15)$$

$$\text{Denoting } E_o / E_i = F(p), \text{ we get } F(p) = \{1 - (Y_2 / Y_1)\}^{-1} \quad (5.16)$$

The CFA has been connected in feedback of a high gain operational amplifier of gain A ($A \rightarrow a$), Fig. 5.4. The gain of the circuit

$$\frac{V_0}{V_i} = \frac{A}{1 + F(p)A} \approx \frac{1}{F(p)} \quad (5.17)$$

Analyzing for Y_{in} in Fig. 5.4 we get

$$Y_{in} = \left(1 - \frac{1}{F(p)}\right) y_0 \quad (5.18)$$

$$Y_{in} = \frac{y_2 \cdot y_0}{y_1}$$

where Y_{in} = Driving point impedance of Fig. 5.4

For a supercapacitor simulation, $y_{0,2} = pC_{0,2}$ and $y_1 = 1/R_1$

Then $Y_{in} = p^2 \cdot C_0 C_2 \cdot R_1 = p^2 D$

where supercapacitor element or FDNR is

$$D = C_0 C_2 R_1 \quad (5.19)$$

The FDNR elements are tunable by one of the components is no matching constraint-an advantage for microcircuit fabrication.

The effects of the CFA port errors are estimated by assuming non ideal CFA and considering finite port errors ($\epsilon_{i,v,z} \neq 0$) we get the modified admittance function

$$Y_{in}(p) = pC_x + p^2 D' \quad (5.20)$$

$$\text{Where } D'/D = 1/1 - \epsilon_i \text{ and } C_x = \epsilon_v C_0 \quad (5.21)$$

6. INTEGRATOR/DIFFERENTIATOR AND FILTER DESIGN

In the communication system, wave processing/ conditioning, by active – RC integrator/differentiator find wide application. These Integrators and Differentiator are involving active devices like the voltage operational amplifier (OA) and current conveyer (CC). Several active Integrators/ Differentiators circuit using OA [21, 22], OTA [21] and CC [12 - 20] have been developed in the pas.

The design of analog signal processing circuits and system in current mode is receiving attention at present. The current mode circuit offer substantive improvements over the voltage mode ones relative to linearity and bandwidth.

Usually these designs were carried out in the recent past using the voltage controlled current source (VCCS) or current conveyer (CC) element. Here CFA has been for this purpose.

The literature presents a number of integrator schemes using two or three CFAs. Some of these realizations are based on selection of design parameters with external discrete RC-components, while recently some are proposed utilizing the CFA device transimpedance. It is seen that the usable frequency range of such circuits can be significantly enhanced by taking into consideration the transimpedance elements in the analysis. Previously some CFA based single and dual input circuits with passive tuning of the time constant for the realization of Integrator and Differentiators have been made.

In this chapter, first we propose new dual input integrator using CFA device .next we propose a simplified version of integrator and differentiator using a single CFA. The CFA provides both current source (z-port pin#5) and voltage source pin (#6) for easy cascability.

Analysis has been made using the practical CFA model (e.g. AD 844) with finite port errors ($\epsilon \neq 0$). The circuits use a single resistor or capacitor without the need of large spread of passive components to tune the time constant (τ). The value of τ changes slightly to τ' due to the device imperfection. Subsequently compensation design equations have been derived for correcting the imperfection. The sensitivity analysis also reveals a low value.

The single –CFA configuration had been designed for a range of signal processing/generation function on the same topology .the analysis has been carried out utilizing the y- port parasitic element s and the z-port transadmittance of the CFA. The design equations had been derived for extended- range frequency operation (1 MHz - 30 MHz) for realizing the functions of:

- Ideal inverting integrator/differentiator,

- Filters (BP, LP, HP) with high-selectivity ($Q \geq 20$),
- Sinusoid Oscillator circuit.

The tuning parameters, e.g., time-constant (τ), selectivity (Q) and resonant/oscillation frequency (ω_0) may be varied by single R or C components. The performance on time-domain and frequency-domain processing of appropriate input signals, square/triangular wave for integrator/differentiator and sine wave for the filters have been verified by PSPICE macro model simulation and hardware implementation. Some simulated are included.

6.1. NEW DUAL INPUT INTEGRATOR

Next we present the derivation of two current mode structures which are derivable conveniently from those in Fig. 6.1 and Fig. 6.2.

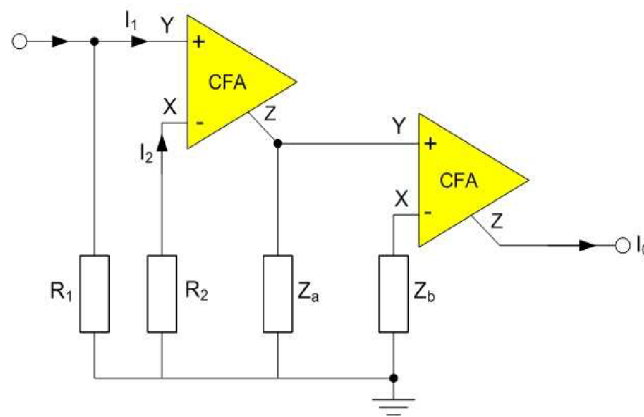


Fig. 6.1: Dual - input diferentiator ratio function (Z_b / Z_a)

$$H(P) = I_0 / I_d = Z_a / Z_b, \quad R_1 = R_2$$

Integrator, $Z_a = 1/pc, Z_b = Z$

Differentiator, $Z_a = R, Z_b = 1/pc$

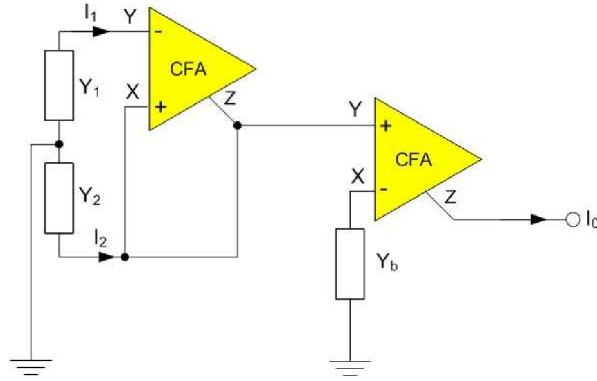


Fig. 6.2: Dual - input integrator ratio function (Z_b / Z_a)

$$H(P) = I_0 / I_d = Y_b / Y_a \quad Y_2 = Y_1 + Y_a$$

Integrator, $Y_a = pC, \quad Y_a = pC,$

Differentiator, $Y_a = 1/R, \quad Y_b = pC$

Analysis for Fig. 6.1 yields the output current (I_0)

$$I_0 = a_1 a_2 \beta_2 (k \beta_1 I_2 - I_1) \quad (Z_a / Z_b) \quad (6.1)$$

where $k = R_2/R_1$

With ideal CFAs where $\alpha = \beta = \delta = 1$ we get true differential input ($I_d = I_2 - I_1$) current transfer from eq. (6.1), with the realizability design of $k = 1$, Fig. 6.1 as

$$H = I_0 / I_d = Z_a / Z_b \quad (6.2)$$

Hence with $Z_a = 1/pC$ and $Z_b = R$, one gets an integrator function

$$H(p) = 1/pt, \quad t = RC \quad (6.3)$$

Interchanging the R and C components, a differentiator function is obtained

Similar analysis for fig 3.2 (b) yields

$$I_0 = \frac{\alpha_2 \beta_2 y_b}{y_2 - \alpha_1 \beta_1 y_b} (I_2 - \alpha_1 I_1) \quad (6.4)$$

With ideal CFAs, we get

$$H = I_0 / (I_2 - I_1) = \frac{y_b}{y_2 - y_1} \quad (6.5)$$

Selecting $y_2 = y_a + y_1$ as realizability design, we get a ratio function

$$H = y_b / y_a \quad (6.6)$$

Here taking $y_a = pC$ and $y_b = I/R$, we have an integrator, and interchanging R and C, we get a differentiator, both with $\tau = CR$. Here must be taken as $y_{1,2} = 1/r_{1,2}$

The effects of CFA port-errors in Fig. 6.1 have been examined and subsequently, the modified expressions are derived. It may be concluded that both configurations in Fig. 6.1 and Fig. 6.2 provide dual-input capability on differential current (I_d) signal. The circuit of fig. Fig. 6.2, this input signal is modified to $I_d = I_2 - I_1(1 - \epsilon_{i1})$, where I_1 signal is slightly reduced in magnitude. Both configurations realize ideal current mode integrator/differentiator function with signale-tunable time constant (1) by (R or C). The effects of the CFA port errors ($\epsilon_{i,v,z} \ll 1$) can be precisely compensated. The relevant compensation design equation is shown in Tab. 6.1.

Tab. 6.1: Modified design equations for new dual-input current-mode integrator/differentiator realization in Fig. 6.1 and Fig. 6.2

Fig 3.1.	Output current	Realizability
(a)	$I_0 = (1 - \epsilon_1)(Z_a/Z_b)\{(1 - \epsilon_{I_1})kI_2 - I_1\}$ $\epsilon_1 = \epsilon_{i1} + \epsilon_{I_1} + \epsilon_{v2}$	$k = r_2/r_1 = 1/(1 - \epsilon_{1_1})$
(b)	$I_0 = \frac{1 - \epsilon_{x2}y_b}{y_2 - (1 - \epsilon_{x1})y_1} \tilde{I}_d$ $\tilde{I}_d = I_2 - I_1(1 - \epsilon_{i1})$ $\epsilon_{x2} = \epsilon_{I2} + \epsilon_{v2}$ $\epsilon_{x1} = \epsilon_{I1} + \epsilon_{v2}$	$y_2 = y_a + y_1(1 - \epsilon_{x4})$

Fig 3.1.	Modified Expressions			Compensation Design	
	Current Transfer H	Integrator	Differentiator	Integrator	Diferentia tor
(a)	$I_0/I_d = (1 - \epsilon_1)Z_a/Z_b$ $I_d = I_2 - I_1$	$\tilde{H} = 1/s\tilde{\tau}$ $\tilde{\tau} = \tilde{R}C$ $\tilde{R} = R/(1 - \epsilon)$ $Z_a = 1/sC$ $Z_b = R$	$\tilde{H} = 1/s\tilde{\tau}$ $\tilde{\tau} = R\tilde{C}$ $\tilde{C} = C/(1 - \epsilon)$ $y_a = 1/R$ $y_b = sC$	$R_c = R/\epsilon$ <p>Parallel to R</p>	$C_c = \epsilon_i C$ <p>Parallel to C</p>
(b)	$I_0/\tilde{I}_d = (1 - \epsilon_{x2})(y_b/y_a)$ $\tilde{I}_d = I_2 - I_1(1 - \epsilon_{i1})$	$\tilde{H} = 1/s\tilde{\tau}$ $\tilde{\tau} = R\tilde{C}$ $\tilde{R} = R/(1 - \epsilon_{x2})$ $y_a = sC$ $y_b = 1/R$ $y_1 = g$ $y_2 = sC + g$ $\tilde{g} = g(1 - \epsilon_{x1})$	$\tilde{H} = 1/s\tilde{\tau}$ $\tilde{\tau} = R\tilde{C}$ $\tilde{C} = C(1 - \epsilon_{x2})$ $y_a = 1/R$ $y_b = sC$ $y_1 = 1/r$ $y_2 = R^{-1} + \epsilon_{x1} r^{-1}$	$R_c = R/\epsilon_{x2}$ <p>Parallel to R</p>	$C_c = \epsilon_{x2} C$ <p>Parallel to C</p>

6.2. SENSITIVITY FOR DUAL INPUT INTEGRATOR

The active sensitivities relative to the CFA imperfections of the time-constant may be calculated on the residues of the negative-real (1) pole/zero. It shows single resistor/capacitor tenability at low sensitivity and realization of the pole/zero at the origin [114].

The classical sensitivity figure is defined as $S_a^b = (db/b)/(da/a)$. The active τ -sensitivity figures are calculated after normalizing all passive components equal to unity; for all the circuits in Fig. 6.1 and Fig. 6.2, the sensitivity figures are

$$\left. \begin{array}{l} \left[\begin{array}{l} \tilde{\tau} \\ S_{\epsilon_{i,v}} \end{array} \right] = \frac{\epsilon_{i,v}}{\epsilon_i + \epsilon_v} \\ \left[\begin{array}{l} \tilde{\tau} \\ S_{\epsilon_0} \end{array} \right] = \frac{\epsilon_0}{1 + \epsilon_0} \end{array} \right\} \ll 1 \quad (6.7)$$

Hence the proposed networks exhibit extremely low active-sensitivity.

In the case of non ideal CFA, the circuit has been reanalyzed and we get,

$$I_0' = (K'I_2 - I_1) \left(n \cdot \frac{Z_2}{Z_1} \right) \quad (6.8)$$

where

$$\frac{K'}{K} \cong 1 + \epsilon_{i1} - \epsilon_{v2} \quad \text{and} \quad n \cong 1 - (\epsilon_{i1} + \epsilon_{iz} + \epsilon_{v2})$$

The design equation for differential reliability now becomes

$$K' = 1 \quad \text{i.e.} \quad r_1 = (1 + \epsilon_{i1} - \epsilon_{v1}) \quad r_2 \quad (6.9)$$

so, τ changes to $\tau' = \frac{RC}{n}$

7. CURRENT MODE NONMINIMUM-PHASE ALLPASS FILTERS

The non minimum-phase all pass filters are useful for various phase processing applications such as correcting signal phase aberrations, phase recondition at a constant magnitude transmission over arrange of frequencies of interest.

In this chapter, we present a new design of current mod non minimum phase all filter using a current feedback (CFA). The type of filters have been realized in the past using operational amplifier (OA) and current conveyer (CCII) [5-9] devices for both voltage mode and current mode applications. But now the design of current mode analog signal processing circuits is gaining importance owing to certain advantages.

The CFA, AD-488 provides an advantage over the basic current conveyer element because of the low output impedance buffer between the z-port and the V_0 terminals, that allows the voltage (V_z) at z node to be accessed without affecting output current (I_0), which helps cascadability [31].

The current output stages of such advice can be designed with high accuracy (low tracking error) and with extremely large output impedance [21].

The CFA had recently been for the realization of magnitude selective filters. In this chapter we have utilized CFA to design, cascade current mode first and second order phase-selective all-pass with a simple active circuit topology. The effects of the device imperfections in view of finite tracking errors ($\epsilon_{i,v} \neq 0$) have been examined which shows slight deviations in the network parameters from the nominal values. It has been shown that even with nonideal CFA, the circuit realizes the nominal function but at a slight altered center-frequency.

We present here four schemes for the first order and two schemes for second order functions that can be generated from the basic topology. The design equations for all these realizations have been derived under both ideal and nonideal conditions. The active sensitivities in all these cases are been to be extremely low.

7.1. REALIZATION

Analysis of the proposed circuit in **Fig. 7.1** using eq.(7.1) and assuming ideal CFA we get the current transfer function $I_0/I = F(p)$ as

$$F(p) = (y_1 y_4 - y_2 y_3) / (y_1 + y_2) y_4 \quad (7.1)$$

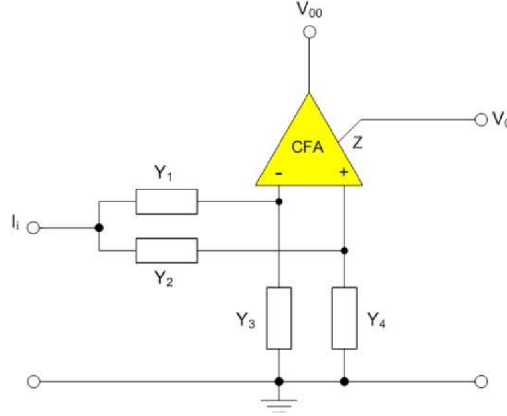


Fig. 7.1: Nonminimum phase network using a CFA.

Where $y_j (j = 1 \text{ to } 4)$ are positive immittances to be chosen appropriately for obtaining the first and second order functions.

It may be mentioned that similar realizations of first order functions had been reported earlier [8] with an inverting CCII conveyer element. Here the additional advantage by the use of the CFA device is that a voltage signal (V_o) output at the follower, proportional to current output (I_o), could be obtained by resistive termination of the z-port without affecting (I_o), as it is being drawn from the current source node.

7.2. FIRST-ORDER FUNCTIONS

We have the following four first order functions by selecting the component set as listed in Tab. 7.1.

$$\left. \begin{aligned} F1(p) &= (1 - pk\tau) / D(s) \\ F2(p) &= (p\tau - k) / D(s) \\ F3(p) &= 1/2(1 - p\tau(k-1)) / D(p) \\ F4(p) &= 1/2(p\tau - (k-1)) / D(p) \end{aligned} \right\} \quad (7.2)$$

where nominal time constant $\tau = RC$ and $D(p) = (1 + p\tau)$.

The realizability conditions and phase variation for these functions are shown in Tab. 7.1. The gain is constant at unity for F1 and F2 while it is 0.5 for F3 and F4. It may be mentioned that F3 and F4 need one more resistor but the capacitor is grounded. Note that the CFA has voltage source output at node V_0 which is to be obtained, if desired, by passing I_0 through a suitable resistive load. This would provide a transimpedance function corresponding to a constant resistance with phase shifting characteristics.

Tab. 7.1: Summary of first order function realizations

Function	Components						Relizability	Gain	Phase
	Z_1	Z_2	Z_3	Z_4	K	τ	k	F_0	φ
F1	R	$1/pC$	r_3	r_4	r_4/r_3	RC	1	1	0 to $-\pi$
F2	$1/pC$	R	r_3	r_4	r_4/r_3	RC	1	1	π to 0
F3	r_1	r_2	$\frac{(pR_3C+1)}{pC}$	R_4	R_4/R_3	RC $R_3 = R$	2	0.5 if $r_1 = r_2$	0 to $-\pi$
F4	r_1	r_2	r_3	$\frac{R_4}{(pR_4C+1)}$	R_4/R_3	RC $R_4 = R$	2	0.5 if $r_1 = r_2$	π to 0

7.3. SECOND ORDER FUNCTIONS

We derive to alternative second order functions F5 and F6 from Fig. 7.1 by taking the following two sets of passive immittances.

$$y_1 = (p\tau + 1)/R, \quad y_2 = pC/(p\tau + 1), \quad y_{3,4} = 1/r_{3,4} \quad \text{and} \quad k = r_4/r_3 \quad (7.3)$$

$$y_{1,2} = 1/r_{1,2}, \quad y_3 = pC/(p\tau + 1), \quad y_4 = (p\tau + 1)/R \quad \text{and} \quad \lambda = r_1/r_2 \quad (7.4)$$

Combining (1) and (2) we get the function in the form

$$F(p) = F_0 \frac{(p n_2)^2 - p n_1 + n_0}{(p d_2)^2 + p d_1 + d_0} \quad (7.5)$$

Where the coefficients of F5(p) and F6(p) corresponding to eq. (7.3) and eq. (7.4) respectively are given below by eq. (7.6) and eq. (7.7)

$$\left. \begin{aligned} n_1 &= k - 2, n_2 = 1 \\ d_0 &= 1, d_1 = 3, d_2 = 1, F_0 = 1 \end{aligned} \right\} \quad (7.6)$$

and

$$\left. \begin{aligned} n_0 &= 1, n_1 = \lambda - 2, n_2 = 1 \\ d_0 &= 1, d_1 = 2, d_2 = 1, F_0 = 1(1 + \lambda) \end{aligned} \right\} \quad (7.7)$$

Equation (7.5) yields an allpass (AP) function with $n_1 = d_1$ and additional band-reject functions (BR) with $n_1 = 0$. These realizability conditions for F5(p) and F6(p) are given by eq.(7.8) and eq. (7.9) respectively as

$$K(\text{AP})=5 \quad k(\text{BR})=2 \quad (7.8)$$

$$\lambda(\text{AP})=4 \quad \lambda(\text{BR})=2 \quad (7.9)$$

Note that F6(p) realized by component set of eq. (7.4) has equal-value grounded capacitor. The phase shift for both F5 and F6 are lagging. The phase responses may be expressed in terms of the normalized frequency parameter $u = (\omega / \omega_0)$ as

$$\begin{aligned} \phi_5(u) &= 2 \arctan \{3u / (1 - u)^2\} \\ \phi_6(u) &= 2 \arctan \{2u / (1 - u)^2\} \end{aligned} \quad (7.10)$$

Both these variation are in the range (lagging) of $0 \leq \phi_{5,6}(s) \leq 2\pi$.

7.4. EFFECTS OF CFA NON- IDEALITIES

Reanalysis of Fig. 7.1 assuming a non-ideal CFA ($\epsilon \neq 0$) modifies eq.(5.1) to

$$F = (1 - \epsilon_i) \frac{y_1 y_4 - b y_2 y_3 + \epsilon_v y_1 y_2}{y_4 (y_1 + y_2) + \epsilon_v y_1 y_2} \quad (7.11)$$

the nominal function F_j ($j = 1$ to 6) will be modified which we examine next

7.5. MODIFIED FUNCTION

Reanalysis with eq.(7.11) for the realization of F_1 yields

$$\tilde{F}_1(p) = (1 - \epsilon_i) \frac{1 - p \tau k (1 - \epsilon_v) - m \epsilon_v}{1 + p \tau (1 + m \epsilon_v)} \quad (7.12)$$

where $m = r_4 R$

The modified design equation is

$$k = \frac{1 + 2m \epsilon_v}{1 - \epsilon_v} \quad (7.13)$$

This may be simplified after writing $(1 - \epsilon_v)^{-1} \approx (1 + \epsilon_v)$, since $\epsilon_v \ll 1$, and then neglecting products of errors, given by

$$k \cong (1 + 2m \epsilon_v)(1 + \epsilon_v) \quad (7.14)$$

which yields

$$r_3 = \frac{r_4}{1 + \epsilon_v (1 + 2r_4 / R)} \quad (7.15)$$

In practice, if one selects $r_4 = R$, this further reduces to

$$r_3 = R / (1 + 3\epsilon_v) \quad (7.16)$$

which may be set precisely. We observe that with an ideal CFA ($\epsilon_v = 0$) this equation reduces to the nominal design of $k = 1$.

Substitution of eq.(7.13) in eq. (7.12) gives

$$\tilde{F}1(p) = (1 - \epsilon_i)(1 - p\tilde{\tau}) / (1 + p\tilde{\tau}) \quad (7.17)$$

$$\text{Where } \tilde{\tau} = C(R + \epsilon_v r_4) \quad (7.18)$$

Equation (7.17) indicates that even with a nonideal CFA the circuit is able to realize the allpass functions but at a slightly altered center-frequency. The voltage error (ϵ_v) alters only the time constant

Similarly we get F_2 changing to

$$\tilde{F}2(p) = (1 - \epsilon_i) \frac{p\tilde{\tau}(1 - \epsilon_v)}{1 + p\tilde{\tau}} \quad (7.19)$$

and

$$\tilde{k} \cong 1 / (1 - \epsilon_v) \cong (1 + \epsilon_v) \quad (7.20)$$

The effects of the CFA imperfections on the other two first order functions F3 and F4(p) and on the second order functions F5 and F6 have also been examined which are listed in Tab. 7.1. It may be mentioned here that for F6 one gets differing values of ω_p and ω_z since

$$\tilde{d}_0 = 1 - p\epsilon_v \text{ and } \tilde{n}_0 = 1 + (P\epsilon_v)/(1 + \lambda) \quad (7.21)$$

This difference may be insignificant if we note that $\epsilon_v \ll 1$ and may be further eliminated if r_2 is scaled to a relatively high value ($P = R/r_2 \ll 1$) such that the quantity $p\epsilon_v$ can be extremely small leading to $\tilde{d}_0 = 1 = \tilde{n}_0$. The design equations are then $\lambda(Ap) = 4/(1 - \epsilon_v) \cong 4(1 + \epsilon_v)$ and $\lambda(BR) = 2/(1 - \epsilon_v) \cong 2(1 + \epsilon_v)$.

8. MULTIFILTER FUNCTION DESIGN

Recently CFA based circuits find wide application on signal and wave processing. Here we present two new CFA based circuits to obtain good quality band pass (BP) band reject (BR) and all pass filters (AP). The BP filter has been used with subtract or to derive variable phase all pass (AP) functions

The simulation of lossless inductor and the Bruton's concept of supercapacitor developed earlier has been used in the RC resonator circuit to obtain the above mentioned filters. This idea can also be extended to design a high $Q(Q \rightarrow \alpha)$ oscillator function.

All the proposed functions have been verified with hardware implementation and by PSPICE macro model simulation in frequency range of $30 \text{ kHz} \leq f_0 \leq 300 \text{ kHz}$. This analysis has also been made taking the effect of finite port errors (ϵ) in case of nonideal CFAs.

8.1. ANALYSIS

The proposed circuit is shown in the Fig. 8.1. Here I_i = input current and V_i = input voltage. Applying the mesh equation, we find at Node B, [where voltage at node B is V].

$$V = I_z / Y_4$$

$$\text{or, } V.Y_4 = I_z$$

$$\text{or, } V.Y_4 = I_x \text{ [since } I_z = I_x \text{]} \quad (8.1)$$

At Node D, $(V - V_i)Y_2 = V_i Y_3$ (Since the voltage at node D is V_i)

$$\text{or, } V = \frac{V_i(Y_2 + Y_3)}{Y_2} \quad (8.2)$$

At Node A,

Putting the value of I_x from eq. (5.1)

$$\text{or, } I_i = V_i Y_i - \frac{V_i(Y_2 + Y_3)(Y_1 - Y_4)}{Y_2}$$

$$\text{or, } Y_i = (Y_3 Y_4 + Y_2 Y_4 - Y_1 Y_3) / Y_2 \quad (8.3)$$

Writing

$Y_1 = 1/R_1$, $Y_2 = 1/R_2$, $Y_3 = pC_2$, and $Y_4 = pC_1$ in Fig. 8.2 we get

$$Y_i = p^2 \cdot C_1 C_2 \cdot R_2 + pC_1 - pC_2 \cdot \frac{R_2}{R_1}$$

$$= p^2 \cdot C_1 C_2 R_2 + pC_2(n - K), \quad n = C_1 / C_2 \quad \text{and} \quad K = R_2 / R_1 \quad (8.4)$$

The realizability condition for an ideal supercapacitor is $n=K$, hence

$$Y_i = p^2 D; \quad D = C_1 C_2 R_2 \quad (8.5)$$

By similar analysis, we get from Fig. 8.3,

$$Y_i = p^2 \cdot C_1 C_2 \cdot R_2 + pC_2 \{(1+n) - K\} \quad (8.6)$$

Using the component ratios as above [$n = C_1 / C_2$ and $K = R_2 / R_1$]

Writing $K = 1 + n$ for the realizability, we get

$$Y_i = p^2 \cdot D \quad (8.7)$$

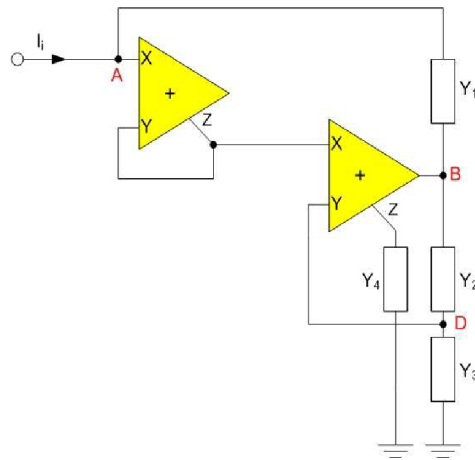


Fig. 8.1: Proposed CFA- based configuration

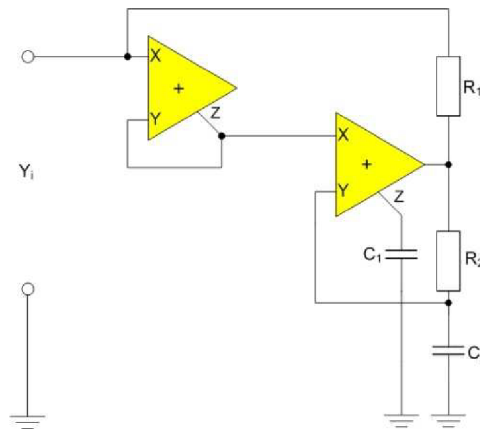


Fig. 8.2: Proposed CFA – based circuit of super capacitor

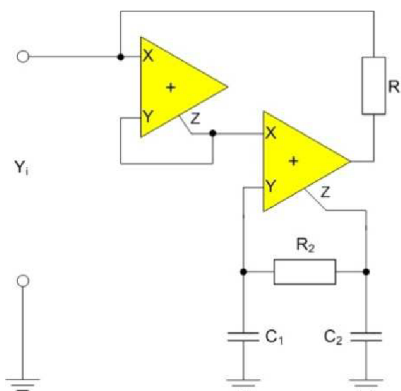


Fig. 8.3: Proposed CFA – based circuit of super capacitor

8.2. EFFECTS OF CFA ERRORS

Re-analysis of **Fig. 8.1** assuming non-ideal CFAs and considering finite port errors ($\epsilon_{i,v,z} \neq 0$), we get the modified admittance function

$$Y'_i(p) = p^2 D' + pC' + G \quad (8.8)$$

where

$$D' = D(1 + \epsilon_i) \quad (8.9)$$

$$C' = C_2[(n - K) + \{n\epsilon_i - K(\epsilon_{v1} + \epsilon_{v2})\}] \quad (8.10)$$

$$G = \frac{-(\epsilon_{v1} + \epsilon_{v2})}{R_1} \quad (8.11)$$

$$\epsilon_i = \epsilon_{i1} + \epsilon_{i2} + \epsilon_{v1} + \epsilon_{v2} + \epsilon_{v2} + \epsilon_{v2} \quad (8.12)$$

Thus the super capacitor becomes non-ideal, being shunted by a lossy capacitor (C') with a low value negative conductance (G). The notified realizability condition for an ideal-D element is

$$K = \frac{n(1 + \epsilon_i)}{1 + \epsilon_{v1} + \epsilon_{v2}} \quad (8.13)$$

The negative resistance may be cancelled by connecting a high-value shunt resistance (R_c) at the input port, given by $R_c = R_1 / (\epsilon_{v1} + \epsilon_{v2})$. Note that with ideal CFAs, eq.(8.13) reduces to the nominal condition $K=n$. similar analysis had been carried out for the circuit in Fig. 8.2 and the modified expressions are summarized in Tab. 8.1.

9. SINUSOID-OSCILLATOR REALIZATION: DOUBLE INTEGRATOR LOOP

In the area of analog signal processing the voltage controlled oscillator (VCO) is being used as building block for the design of phase locked loop (PLL). FM telemetry, swept super heterodyne spectrum analysis, frequency synthesis, and digital voltage measurement by the v-f conversion. In the recent past operational Amplifier (AO) based RC oscillator has been developed where the tuning resistor is being replaced by FET-VVR [3] to obtain a VCO.

Some CFA based RC- oscillator have been recently reported here we present sine wave oscillator design utilizing the Double integrator loop (DIL) based on the CFA active element.

In this chapter, we present some voltage tuned DIL- based sinusoid oscillators using the AD844 device. The time constant ($\tau_{0,1,2}$) of the two voltage controlled integrators of an oscillator is tuned by the d.c. control voltage (V_c) of the Multiplier (ICL-8013). The multiplier element with integrator has been used in the feed forward connection in the first DIL.

Here we have also examined CFA based linear voltage controlled sinusoidal oscillator (VCSO) wherein the multiplier element (ICL-8013) is connected with each CFA device in such a way that the d.c. control voltage (V_c) of the multiplier produces the f_0 -tuning linearly. The oscillation frequency (f_0) over specific band, set by the different RC components, can be varied by the control voltage (V_c) of the multiplier. The choice of the multiplier element is advantageous since (V_c) may be generated from a digital code through a D-A converter (DAC) [162].

9.1. VOLTAGE CONTROLLED OSCILLATOR (VCO)

We present some new voltage controlled sinusoid oscillators (VCO's) based on the implementation of double integrator loop (DIL) as shown in **Fig. 9.1**. Here an non inverting Voltage Controlled Integrator and inverting Voltage Controlled Integrator, developed using CFA device have been used along with the multiplier element in the loop to control the time constants of the DILs. The oscillation frequency ω_0 (or f_0) is tunable by V_c of the multiplier element. In Fig. 9.1, each integrator is a minimal realization using only one RC-section, one multiplier and a CFA device. In Fig. 9.2, however two resistors have been used for each

integrator. Here two CFA's of same polarity have been used which may be suitable for microminiaturization of the circuit.

Fig. 9.1 and **Fig. 9.2:** The proposed VCO configurations using DIL:

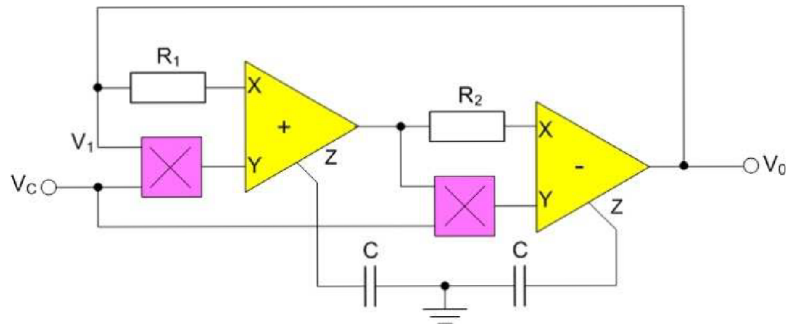


Fig. 9.1: Multiplier element in feed forward connection

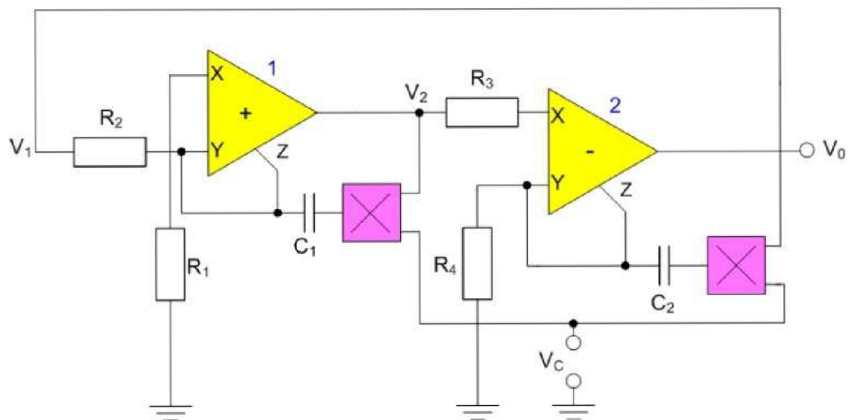


Fig. 9.2: Multiplier element in feedback connection

9.2. ANALYSIS

By analysis assuming ideal CFA, we get the voltage transfer function ($G_{1,2}$) respectively of the VCI#1 and VCI#2 in Fig. 9.1, assuming loop is cut at V_1 , as

$$V_2/V_1 = G_1(p) = 1/p\tau_{01} ; \tau_{01} = R_1C_1/(1-kV_c) \quad (9.1)$$

$$V_0/V_2 = G_2(p) = 1/p\tau_{02} ; \tau_{02} = R_2C_2/(1-kV_c) \quad (9.2)$$

Where $k = 0.1/\text{volt}$ is the multiplier constant.

Hence the loop- transfer is

$$G_0(p) = G_1G_2(p) = -1/p^2\tau_{o1}\tau_{o2} \quad (9.3)$$

The oscillation frequency (ω_0) obtained on closing the loop is

$$\omega_0 = 1/\sqrt{(\tau_{o1}\tau_{o2})} = (1 - kV_c)/\sqrt{(R_1C_1R_2C_2)} \quad (9.4)$$

Thus ω_0 is tunable by either the passive RC components or electronically by the dc control voltage in the range $1 \text{ V} \leq V_c \leq 10 \text{ V}$.

Similar analysis had been carried out for the circuit in Fig. 9.2; the pertinent design equations are listed in Tab. 9.1.

Tab. 9.1: Design Equations for the Proposed VCOs.

Fig.8.2	Transfer Equation	Loop Transfer
(a)	$\frac{V_2}{V_1} = G_1(s) = \frac{1}{s\tau_{o1}}$ $\frac{V_0}{V_2} = G_2(s) = -\frac{1}{s\tau_{o2}}$	$G(s) = -\frac{1}{s^2}\tau_{o1}\tau_{o2}$
(b)	$\frac{V_2}{V_1} = H_1(s) = \frac{a}{sC_1R_1(1 - kV_c) + a - 1}$ $a = \frac{R_1}{R_2}$ $\frac{V_0}{V_2} = H_2(s) = \frac{1}{sC_2R_3(1 - kV_c) + b - 1}$ $b = \frac{R_3}{R_4}$	$H(s) = \frac{a}{s^2\tau_{o1}\tau_{o2} + s\{(\tau_{o1}(a - 1) + \tau_{o2}(b - 1)) + (a - 1)(b - 1)\}}$ $\tau_{o1} = C_1R_1(1 - KV_c)$ $\tau_{o2} = C_2R_3(1 - KV_c)$

Fig.8.2	Realizability Design	ω_0	Modified ω_0
(a)	None	$\frac{1 - kV_c}{\sqrt{(R_1 C_1 R_2 C_2)}}$	$\left\{ \frac{\alpha_1 \alpha_2 \delta_1 \delta_2 (1 - \beta_1 kV_c)(1 - \beta_2 kV_c)}{R_1 R_2 C_1 C_2} \right\}^{\frac{1}{2}}$ $= \frac{\alpha \delta (1 - \beta kV_c)}{RC}$ <i>for matched components</i>
(b)	<p>Ideal CFA:</p> <p>$a = 1$</p> <p>$R_1 = R_2 = R_a$</p> <p>$b = 1$</p> <p>$R_3 = R_4 = R_b$</p> <p>Non ideal CFA:</p> <p>$\frac{R_1}{R_2} = 1 - \alpha_1 \delta_1$</p> <p>$\frac{R_3}{R_4} = 1 - \alpha_2 \delta_2$</p>	$\frac{1}{\{(1 - kV_c)\sqrt{(R_a C_1 R_b C_2)}\}}$	$\{(1 - \delta_1 kV_c)(1 - \delta_2 kV_c) R_a C_1 R_b C_2\}^{\frac{1}{2}}$ $= \frac{1}{(1 - \delta kV_c) RC}$ <i>for matched components</i>

9.3. EFFECTS OF CFA IMPERFECTIONS

Re-analysis of the circuit in Fig. 9.1 assuming nonideal CFA devices yields the modified expressions

$$\tilde{G}_1(p) = \alpha_1 \delta_1 (1 - kV_c \beta_1) / R_1 C_1 \quad (9.5)$$

$$\tilde{G}_2(p) = \alpha_2 \delta_2 (1 - kV_c \beta_2) / R_2 C_2 \quad (9.6)$$

$$\text{and } \tilde{G}_0(p) = -1 / p^2 \tilde{\tau}_{01}^2 \tilde{\tau}_{02}^2 \quad (9.7)$$

$$\text{where } \tilde{\tau}_{0j} = R_j C_j / \alpha_j \delta_j (1 - k V_c \beta_j) ; j=1,2 \quad (9.8)$$

The modified value of ω_0 is now

$$\tilde{\omega} = \{ \alpha_1 \alpha_2 \delta_1 \delta_2 (1 - k V_c \beta_1) (1 - k V_c \beta_2) / R_1 R_2 C_1 C_2 \}^{-1/2} \quad (9.9)$$

Assuming matched-pair of the device, we get

$$\tilde{\omega}_0 = \alpha \delta (1 - k V_c \beta) \sqrt{R_1 R_2 C_1 C_2} \quad (9.10)$$

By similar analysis, we get the modified value of ω_0 for Fig. 9.2 as

$$\tilde{\omega}_0 = 1 / RC (1 - \delta k V_c) \quad (9.11)$$

Assuming matched component, i.e.; $\delta_1 = \delta = \delta_2$ and $R_a C_1 = RC = R_b C_2$

Thus the CFA port errors alter slightly (since $\varepsilon \ll 1$) the value of ω_0 for both the circuits in Fig. 9.1 and Fig. 9.2 as listed in Tab. 9.1. However, their effects are quite insignificant as can be seen from the sensitivity computation.

9.4. SIMPLE LINEAR VOLTAGE CONTROLLED SINUSOID OSCILLATOR (VCSO)

In this section we present a simple linear Voltage Controlled sinusoid Oscillator (VCSO) using the CFA device. A multiplier ICL-8013 element is connect suitably with each CFA device such that electronic tuning of frequency (f_o) is varied linearly with the d.c. control voltage (V_c) of the multiplier. The structure is based essentially on double integrator loop where in each unit is voltage controlled integrator (VCI) consisting of a CFA multiplier composite block and only one grounded RC section. Two phase quadrate oscillations at the two integrator output would be available upon closing the loop.

10. CONCLUSIONS

The target of this thesis was to bring the contribution on the field of the active building blocks for the modern integrated circuits operated in current- or mixed- mode. The group of the blocks was made tighter – the works was focused on current feedback amplifiers. The aim was an exploration of the family of the CFA circuits focusing on novel blocks and especially their applications.

The theoretical and practical results of the work were presented in three main chapters, which showed the usability and universality of the novel introduced blocks and moreover proved the possibility of the implementation of these blocks.

With growing importance of designs in voltage-to-current and current-to-current mode domains, we subsequently obtained the OTA, current conveyor, and voltage conveyor building blocks. For easy cascadability and signal translation from voltage/current input to any one of these as output, the designer needed a more versatile building block. Such an element emerged in mid-80s and was termed as the current feedback operational amplifier (CFOA) or more precisely as the current feedback amplifier (CFA). Thanks to its good technical features and parameters, it is one of the few current mode circuits, which have been accepted even by the manufacturers and are already currently available in the market (e.g. AD-844).

The CFA device was being used by many designers for a variety of analog signal processing applications. Because of the timelines of CFA-based research and development activity and its functional superiority over the previous devices, the we had chosen this device as the building block for the work on ASP circuits and systems.

In this thesis I presented some new CFA-based design of active immittance function pertaining to ideal grounded and floating inductance simulation schemes with a further extension to the design of an active ideal FDNR type super capacitor. The theoretical analysis had been verified experimentally through a typical BP filter design. It had been shown that these designs have very low active sensitivity without requiring any passive component

Active integrators and differentiators find wide applications in various, the well-known OA-RC Miller integrator gives rise to some dc instability at high signal levels owing to the capacitive negative feedback; the problem had subsequently been avoided by the modified designs, but here OA compensation pole introduces additional phase shift at higher frequencies.

I have presented some new CFA-based design of an integrator and differentiator in

both current-mode and voltage-mode forms; dual input capability had been derived in some of the designs. It had been shown that these designs are well-suited for monolithic IC fabrication process in which event the sensibility of the time constant may be reduced to extremely low values. Some CFA-based AP phase equalizer circuits of first and second order realization is also described. The effects of the CFA device imperfections had been investigated.

Satisfactory immitance and transfer properties od the proposed functional blocks had been verified after circuit simulation through PSPICE.

I can select the following new and significant contributions ofthis thesis:

- Design and verification of the insensitive ideal FDNR-type supercapacitor.
- New CFA-based designs of integrator/differentiator in both current- mode and voltage-mode forms well suited for IC fabrication.
- Investigations of the effects of the CFA imperfections for some CFA- based AP phase equalizer circuits.
- New results from the investigation of multifiltering capability in an appropriate RCD resonator
- Novel VCO using a multiplier in the CFA-based double integrator loop

Both the current conveyor (CC) and the CFA devices are basically current-mode devices; the CFA (e.g. AD-844) however has an added capability of copying its transimpedance voltage available at the current source output mode, to wide band buffer's voltage source output mode. Hence most of the elegant CC-based function circuits may easily transform the equivalent CFA-based configuration with an added voltage signal output-hence extreme ease on design flexibility and smooth cascadability, recently the next version of the current conveyor of the third generation (CCIII) is receiving considerable attention for current mode ASP applications. It may be examined how a composite CFA structure can be modeled to yield the CCIII characteristics so that either polarity current signals may be handled by the same device. Another potential area of future R and D appears to be the design of digitally programmable current mode circuits.

The presented work represents the investigation on building blocks for modern current-mode and mixed mode based integrated circuits. A number of novel introduced building blocks together with their implementation are the results. The functionality of the proposed blocks was proved by simulations in the SPICE programme.

With respect to the above discussion it can be declared that aims of this thesis were fulfilled.

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