DEPARTMENT OF MICROELECTRONICS

TEST METHODS FOR THE EVALUATION OF RADIATION EFFECTS IN HIGH PRECISION ANALOGUE AND MIXED-SIGNAL DEVICES FOR SPACE APPLICATIONS

Doctoral thesis

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ABSTRACT

The traditional radiation testing of space electronics has been used for more than fifty years to support the radiation hardness assurance. Its typical goal is to ensure reliable operation of the spacecraft in the harsh environment of space. This PhD research looks into the radiation testing from a different perspective; the goal is to develop radiation testing methods that are focused not only on the reliability of the components but also on a continuous radiation-induced degradation of their performance. Such data are crucial for the understanding of the impact of radiation on the measurement uncertainty of data acquisition systems onboard research space missions.

The thesis is divided into three parts: the first theoretical part contains a discussion of the challenges with designing data acquisition systems for space missions and an overview of the process of estimating measurement uncertainty. It also summarises the theoretical background of the space radiation environment, effects of radiation and temperature on electronic components. The first part concludes with an overview of the traditional radiation hardness assurance and testing.

The second part gives an overview of the new era of a commercial approach to the space technology (NewSpace) and its impact on the radiation hardness assurance and testing processes. A set of advanced in-situ radiation test methods is proposed to address the requirements of the NewSpace and also to provide data with total dose resolution adequate for the development of the models that will be used for live estimation of the measurement uncertainties of data acquisition systems during their missions.

The development of the radiation testing methods and tools is described in the third part of the thesis together with results of various terrestrial total ionising dose tests. A range of commercial electronic components has been tested during the radiation experiments. The experimental campaign started with different types of PMOS devices and continued with precision voltage references and high-resolution A/D converters. The PMOS devices and voltage references were also tested for radiation-induced changes of their temperature coefficients using a novel in-situ measurement method. The third part of the thesis concludes with a description of an in-orbit experiment, which has been designed with a goal to become one of the world’s first attempts to measure the impact of the space radiation on a state-of-the-art data acquisition system during spaceflight. The in-orbit experiment has been successfully ground tested for its capability of monitoring total ionising dose, temperature and measuring degradation of various data acquisition components. The in-orbit experiments are expected to be launched on-board two CubeSat missions in the 2020’s.

The thesis ends in a conclusion chapter. This chapter summarises both the theoretical and experimental parts of the work. It also provides suggestions for future work and an overview of papers and other presentations published during this PhD programme.

KEYWORDS

Analogue to digital converter, automated test equipment, bias, calibration, CubeSat, data acquisition system, delta-sigma modulation, detector, dosimeter, dosimetry, in-orbit testing, in-situ testing, ionising chamber, measurement, measurement uncertainty, metrology, modelling, multimeter, nanosat, NewSpace, RADFET, radiation, sensor, single event effects, source-measurement unit, space environment, temperature, temperature coefficient, temperature drift, test instrumentation, test software, testing, thermometer, total ionising dose, vacuum, voltage reference.

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V Brně dne ....

(podpis autora)

When you can measure what you are speaking about, and express it in numbers, you know something about it.
Lord Kelvin, Electrical Units of Measurement, Vol 1, 1883

For a successful technology, reality must take precedence over public relations, for Nature cannot be fooled.
Richard P. Feynman, Rogers Commission Report of Space Shuttle Challenger accident, 1986

And now here is my secret, a very simple secret: It is only with the heart that one can see rightly; what is essential is invisible to the eye.
Antoine de Saint-Exupéry, The Little Prince, 1943

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1 INTRODUCTION

The year 2017 marked the sixty-year anniversary of the space age. It all started with the launch of the Soviet Sputnik in October 1957, which triggered the so-called space race. The following years brought a revolution into the field of space electronics. For example, the payload instrumentation of the first US satellite, Explorer-1 launched in 1958, was based on thirty transistors. Only seven years later the MIT developed the world's first embedded computer that allowed the Apollo spacecraft to land on the Moon. In those days, space and defence programs were the drivers and enablers of the rapid development of modern microelectronics. The following massive growth of consumable electronics in the 1970's was the next logical evolution of the industry and, was in fact a by-product of space and defence programs.

During the following decades, space and commercial electronic industries followed different developmental paths. The USA won the space race, and the development of the space-rated hardware slowed down to address reliability issues. Robust quality assurance processes, including the radiation hardness assurance/testing, were established. The industry became standardised and achieved high mission reliability. A typical example would be the commercial telecommunication satellites, routinely designed to work for at least fifteen years in the harsh environment of geosynchronous orbits. The downside of this successful approach was the technological obsolescence of the space-rated electronics, extremely high-budget requirements and long lead times.

As soon as commercial electronics achieved the reliability and quality levels suitable for industrial control systems, automotive and aerospace industries, engineers started to consider designing the space applications using commercial electronic components. This trend led to the proposal of the CubeSat standard, a low-cost platform for the simple development of affordable miniaturised satellites in 1999. Only a few years later the SpaceX Company was established with the goal of developing the first fully commercial low-cost space launch systems. The recent success of these so-called NewSpace projects demonstrated that the commercial electronic components and processes could be used for space engineering.

The traditional processes for radiation hardness assurance and testing are facing the challenges of the NewSpace approach. It is obvious that these, rather conservative, methods need to be dramatically changed to follow the aggressive development of the NewSpace technologies.

This presented PhD research was focused on the development of test methods enabling the radiation testing for NewSpace low-cost projects including advanced ground and in-orbit experiments. The goal was not only to perform affordable radiation testing but also to possibly change the approach of NewSpace radiation hardness assurance from the classical reliability analysis to continuous, real-time, mission degradation assessments. The proposed test methods were used for components of high-precision space data acquisition systems. The modern components allow the engineers to design commercial data acquisition systems with performance that was previously only achievable by high-tech scientific experiments. Therefore, the ambition of this PhD was to help to bring the powerful commercial data acquisition technologies into space.

1.1 Objectives and motivation

The PhD research, presented in this thesis, was focused on various goals requiring a combination of multiple engineering fields to be addressed. Therefore this chapter is divided into particular sections describing the individual research objectives and their connections.

1.1.1 The need for high-resolution COTS data acquisition in space

Space technology has been one of the key contributors to the rapid development of modern astronomy, especially in the fields of stellar astronomy, cosmology and planetary science [1]. Other typical space science is the search for extraterrestrial life. Although still not successful, this multidisciplinary field has achieved excellent progress, including applications of modern "on-chip" bio-sensing solutions [2].

Among these traditional astronomical research programs, there are other space science fields that might be crucial for the future of mankind. The intention of "asteroid mining" became an emerging objective of private industry with a vision of sourcing materials from space [3]. The asteroid collision avoidance research, also called the planetary defence, has gained a higher profile as well [4].

All the listed space research programs have one common attribute: a need for high resolution/precision data acquisition (DAQ) systems for the digitalisation of signals from a broad spectrum of sensors. There are at least two major reasons for using the COTS (commercial of the shelf) DAQ technologies for these space projects.

The first reason is financial. Despite the great achievements, space-based astronomy missions suffer both a financial and a schedule crisis [5]. The budgets of the large spacecraft seem to be getting out of control. An illustrative example would be the James Webb Space Telescope (JWST), which will cost at least ten times more than anticipated and when launched, possibly in 2020, various technologies on board will be obsolete due to the extreme duration of the development [6].

The solution to this problem seems to lie in the massive application of commercial technologies including the COTS parts and rapid design/manufacturing processes. The space industry is expected to change dramatically with the rise of the NewSpace industry; low-cost launch providers including SpaceX [7] and Rocket Lab [8] are expected to reduce the launch cost by at least an order of magnitude [9] or even more. Such a cost reduction could cause a paradigm shift in the philosophy of the design and operation of spacecraft; there will be no need to design a perfectly reliable spacecraft if their replacements are cheap to build and launch.

Another important trend of the NewSpace era is the miniaturisation of the spacecraft and potential mass production of nanosatellites using COTS technology. Variety of studies have been published to promote the idea of launching a constellation of low-cost scientific nanosatellites with capabilities of a conservative single large spacecraft [1], [10], [11]. This concept has been successfully demonstrated by the QB50 project, during which a constellation of fifty CubeSat class satellites is planned to be deployed to provide Earth observation of unprecedented detail, using distributed sensors [12]. There are also ambitious plans for exploration of deep space using COTS nanosatellites [13] and nanosatellite constellations [14], [15].

The second important argument for the COTS solutions is the remarkable technological level of the commercial components. Although there have been projects aiming to develop space qualified, radiation hardened parts with performance comparable to the COTS, the capabilities of COTS parts are more advanced the employment of rapid commercial development processes. An example of such a complex, high-budget effort was the NASA's project AAPS (Advanced Avionics and Processor Systems) aiming to develop radiation hardened processors [16] and avionics systems. In contrast to AAPS (which was cancelled), ESA (European Space Agency) has been running a similar program but based on COTS technologies [17].

In conclusion, there is a strong demand for COTS DAQ technologies to be used in the future NewSpace-style scientific missions. Hence, the primary vision of this work is to address the issues related to the applications of the DAQ COTS electronic components and their radiation hardening assurance.

1.1.2 Radiation testing in the era of NewSpace and COTS

The traditional radiation hardening assurance (RHA) is a complex process based on the expected space environment and results from various radiation tests [18]. These datasets are typically obtained from manual component-level testing [19]. Hence, the traditional RHA process is practically impossible to be applied to the NewSpace-style nanosatellites due to budget and time limits. The full radiation test campaign of a single complex integrated circuit can be as expensive as the whole COTS electronics of a CubeSat and the time taken to obtain the results could also cause a significant delay to the project [20].

Despite the above-listed constraints NewSpace/COTS based spacecraft need RHA - radiation effects are believed to be likely a cause of a failure of a significant amount of CubeSat missions [21]. Therefore, the first PhD objective is to design an advanced total ionising dose (TID) radiation testing methods affordable for NewSpace projects. The methods shall be demonstrated on COTS components for DAQ systems.

1.1.3 Real-time mission radiation-induced degradation

The primary goal of traditional RHA is to ensure the reliability of the spacecraft electronics during the planned lifetime of the mission. The RHA analysis is typically performed as a part of the spacecraft design phase [22], [23]. It only defines the expected lifetime of the mission regarding the total radiation dose. Though, there were projects demonstrating techniques for near real-time evaluation of the radiation-induced changes of the reliability during the mission. Those included the ESA's G4MRES (Geant4 for Mission Radiation Effects Simulation) [24] and Vanderbilt University's GSN (Goal Structuring Notations) Assurance Models, aimed to be demonstrated in a CubeSat [25]. A mission TID failure probability model was published by NASA [26].

However, reliability is only one of the attributes characterising the success of the mission. For scientific missions, the quality of the scientific data is equally important. Hence, there is also a need for modelling of the real-time mission degradation of the performance of space DAQ systems, based on measurements of the radiation environment. Proposal for such a model is the second objective of this PhD work, and the advanced TID test methods shall be designed to provide TID data for these models.

1.1.4 Research of synergy between radiation and temperature

Temperature effects have to be carefully considered for the successful design of high-precision DAQ systems [27], [28]. The common term, defining the temperature sensitivity in linear/mixed-signal electronics, is the temperature coefficient *TC* [29].

The traditional RHA literature only discusses the impact of temperature during the irradiation on the magnitude of the radiation-induced changes in the components [18], [30]. Hence, the third PhD objective is to develop and demonstrate a method allowing measurement of radiation-induced changes in *TC* parameters of COTS components for DAQ systems. The resulting data should also be applicable for real-time mission modelling.

1.1.5 In-orbit experiment

A long-term goal of this work is to obtain real in-orbit data to validate the proposed radiation testing methods and models. A broad spectrum of in-orbit experiments has been performed, including various CubeSat projects. A typical goal of these projects was to measure single event effects (SEEs) in various digital components [31]. So far there were missions, observing in-orbit TID effects, however not in DAQ technologies [32]. Therefore the final objective of this PhD work is the development of an in-orbit experiment that can be flown on a nanosatellite (CubeSat). It shall demonstrate:

- The design and calibration of a simplified radiation monitor
- An in-orbit performance test of a temperature monitoring system
- An in-orbit test of a dual, high resolution, DAQ system
- An in-orbit TID test of voltage references and comparison of the results with the data from ground TID tests
- A real-time “Live” model of TID-induced degradation of the measurement uncertainty of the DAQ system

The PhD phase of this project includes the following tasks:

- The hardware and software for t in-orbit and ground testing segment are to be developed. The design shall be compliant with the limits of CubeSat platforms (ultra-low power, minimum size and weight, EMC issues)
- The experiment shall be sensitive enough to be able to observe the TID effects within the limited lifetime of the CubeSat mission
- TID ground tests of the candidate devices for the in-orbit testing
- A TID experiment using a ground simulation of the whole CubeSat experiment, running under the conditions of a space flight
- Demonstration of this experiment to CubeSat teams and negotiation to obtain a flight opportunity
- Development of an integration package allowing a smooth integration of this experiment with typical CubeSat platforms
- Preliminary estimation/simulation of the mission TID levels based on the actual missions (negotiated flight opportunities)

The launch of the in-orbit experiment is expected after the submission of this PhD thesis. This project has the great potential to be a first (as far as published) experiment demonstrating in-orbit radiation testing of a state-of-the-art DAQ system.

1.2 Novelty

There are three areas of novelty in this work. Firstly, advanced TID tests methods were developed with the following unique features:

- Fully automated advanced in-situ measurements
- High-resolution test system allowing evaluation of high-precision DAQ components
- High-resolution dose data
- Combined TID and *TC* in-situ testing with unprecedented stability and dynamic response using thermoelectrical technology

Secondly, real-time "live" mission models were developed to estimate the measurement uncertainty of the space DAQ systems during a random moment of the mission.

Thirdly, an in-orbit CubeSat experiment was designed. This project has a potential of introducing a high-tech commercial DAQ technology into the NewSpace scientific missions.

Another important aspect of this work was the multidisciplinary nature of the presented research. Among the others, this work combined the following fields:

- Design of spacecraft and space instruments
- Space radiation environment
- Radiation effects in electronics and related testing
- High precision linear and mixed-signal designs
- Temperature effects in electronics and their testing
- Design of hardware and software for high precision temperature control
- Design of fully automated test systems
- Metrology for high accuracy measurements

1.3 Outline of the thesis

The first part of the thesis (chapters 2 to 4) outlines the current theory in the field and traditional approach of space electronics design and its RHA.

The challenges of the design of high-resolution space DAQ systems are discussed in chapter 2, including calibration techniques, measurement uncertainty modelling and selection of components for space DAQ systems.

Chapter 3 defines the space environment and discusses the various radiation effects with emphasis on TID effects in linear and mixed-signal devices that are used in DAQ designs. The temperature effects are discussed as well. The synergetic effects between radiation and temperature and other variables are the final topic of chapter 3.

The concept of traditional RHA and testing is discussed in chapter 4 together with both European and American test standards. The published test results for key DAQ components (voltage references and A/D converters) are also outlined in chapter 4 including an overview of the modern technologies of these devices and their parameters.

The second part of the thesis, chapter 5, provides an overview of the challenges and opportunities of the emerging NewSpace industry and the applications of the COTS technology in space. It also gives a discussion of the proposed advanced test methods for both ground and space radiation testing. The chapter concludes with an outline of the novel Life Mission Measurement Uncertainty model. This model is designed to be demonstrated in the in-orbit experiment.

The third part of the thesis (chapters 6 to 10) contains the practical results of the PhD projects and experiments.

The aim of chapter 6 is to give an outline of the tools and facilities that were used for the PhD experiments. Most of them were developed and manufactured from scratch to follow the special requirements of the ISTM experiments. The first part of the chapter describes the irradiation facility and dosimetry systems. The second part is dedicated to the development of the custom test hardware and software including the novel DUT temperature controller.

The first series of radiation experiments were performed on MOS devices, and the results are summarised in chapter 7. The MOS experiments were focused on TID effects on commercial PMOS transitions and RADFETs including TID-induced changes of their temperature sensitivity.

Chapter 8 summarises the results of two radiation experiments focused on the in-situ measurement of TID-induced degradation of COTS voltage references. The chapter concludes with an analysis of the impact of the measured TID-induced changes on a space DAQ system.

Final component-level TID experiment in this PhD work was designed to measure TID-induced degradation of two types of high-resolution A/D converters (ADCs). A custom-developed ISTM tester was used to perform all measurements. The results of the ADC experiment are outlined in chapter 9.

The experimental part of the thesis concludes with a description of an in-orbit experiment, which has been designed with a goal to become one of the world's first attempts to measure the impact of the space radiation on a state-of-the-art data acquisition system during spaceflight. The in-orbit experiment has been successfully ground tested for its capability of monitoring total ionising dose, temperature and measuring degradation of various data acquisition components.

The final part of the thesis is a chapter 11. This chapter summarises both the theoretical and experimental parts of the work. It also provides suggestions for future research and an overview of papers and other presentations published during this PhD programme.

2 SPACE DATA ACQUISITION SYSTEMS

This chapter summarises the specific requirements on the data acquisition systems designed for the high precision experiments to be performed in the space environment. Furthermore, the issues related to the modelling of measurement uncertainty are discussed. The chapter concludes with an overview of the key electronic components used in modern high precision DAQ systems.

The basic metrology-related terminology, used in this work, is based on the internationally recognised guidelines: the International Vocabulary of Metrology (VIM) [33] and the Guide to the Expression of Uncertainty in Measurement (GUM) [34].

2.1 DAQ systems in space

2.1.1 Influence of space environment on the DAQ system

A typical design of a modern high precision DAQ system is shown in Fig. 2.1. The input signal is firstly processed throughout an analogue signal conditioning stage that commonly consists of a filter, a PGA (Programmable Gain Amplifier) and a MUX (multiplexer). The second stage of the DAQ signal chain is a high-resolution ADC (A/D converter) that uses a reference circuit as a measurement standard. The resulting digital data is communicated to the CPU (Central Processing Unit) which also digitally controls all the programmable parts of the DAQ chain.

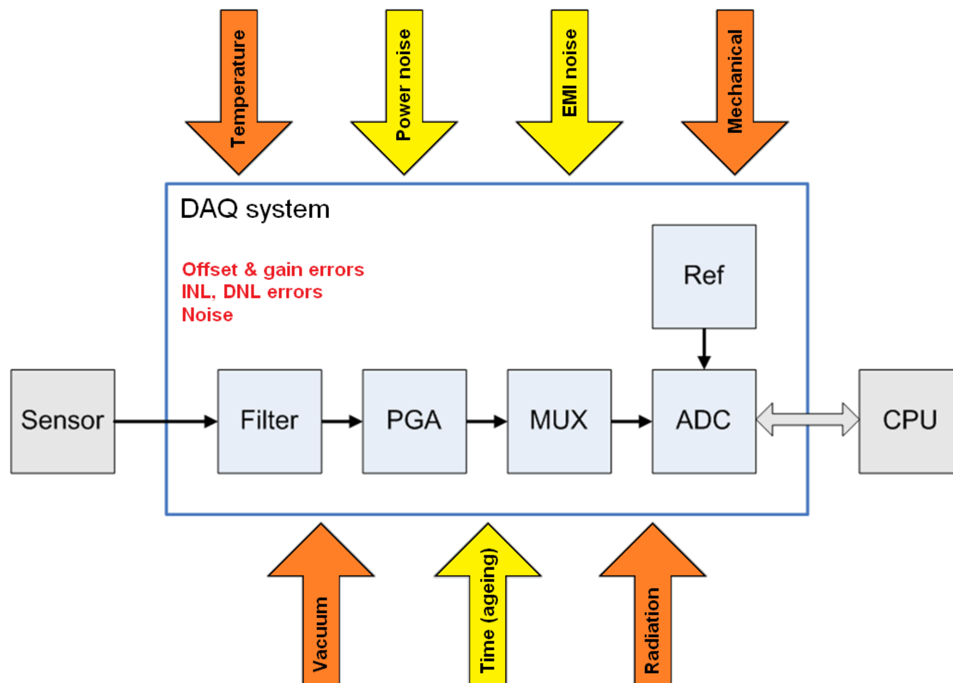

Fig. 2.1: Block diagram of a typical data acquisition system. The DAQ signal chain is shown with its inherent sources of measurement error. When in space, the DAQ system is exposed to harsh environmental conditions as illustrated by coloured arrows.

Every part of the DAQ signal chain is responsible for the overall measurement uncertainty of the entire DAQ system. Therefore, the parasitic properties of these parts are the sources of measurement errors that increase the measurement uncertainty. The typical errors for high precision DC measurements are:

1. offset and gain errors
2. integral (*INL*) and differential (*DNL*) non-linearity errors
3. noise error (measurement repeatability error)

These errors can be identified and ideally suppressed either by calibration or by data processing or by a combination of both. However, these errors are not constant; they drift with the time (ageing) and exhibit a complex dependency on environmental conditions [27]. Therefore there is a broad spectrum of the environmental conditions that may have a strong influence on the measurement uncertainty of a DAQ system as illustrated by the coloured arrows in Fig. 2.1.

The yellow arrows in Fig. 2.1 represent environmental conditions typical for terrestrial applications, and the orange arrows show the additional influence of the harsh space environment, which not only increases the magnitude of some conditions (temperature, mechanical stress) but also brings new conditions including vacuum and space radiation effects. For practical terrestrial DAQ instruments, the dependency of the measurement error sources on the environmental conditions is typically a key factor for the estimation of measurement uncertainty budgets [28], [35]. Hence, this problem is even more important for space DAQ system as the space environment is even harsher.

2.1.2 Calibration in space

Traditional calibration of terrestrial DAQ systems is a robust, standardised process consisting of two subsequent stages [36]:

1. initial calibration at the vendor
2. regular calibrations during the lifetime of the DAQ system

Typically, the DAQ system is adjusted during the vendor calibration stage, and the following regular calibrations only check that its measurement errors are within a specification. Should there be a need for an adjustment, it is commonly performed by a change of calibration data stored in the DAQ system. Such a standard calibration process, based on the usage of external traceable calibration instruments, is recognised as a system calibration. This term is often used in the ADC literature [37].

On top of these system calibration processes, a DAQ system can regularly perform a self-calibration (SCAL) routine, during which the input of the DAQ channel is connected to a known calibration signal, and the DAQ system executes a set of SCAL measurements. The firmware calculates new calibration data to compensate for the actual measurement errors using results from the SCAL measurements. This technique is frequently used to compensate for thermal drift of the input amplifier's offset error by measuring analogue inputs connected to the signal ground [38]. The gain error can be measured by connecting the input to a reference voltage, and a resistor ladder/network [39] can be used to calibrate the linearity error.

As far as the space DAQ systems on unmanned spacecraft are concerned, the traditional system calibration is limited only to the pre-launch phase of the mission.

During the post-launch period, the DAQ system would have to be equipped with additional space-environment-hardened calibration standard should the self-calibration be used to provide similar coverage as of the traditional pre-launch system calibration. In fact, this would make the DAQ hardware significantly more complex. Even the accuracy of the basic offset error self-calibration is not guaranteed in space as the analogue switches, used for shortening the inputs, can suffer radiation-induced enhancement of their parasitic properties including ON-resistance and the leakage currents [40]. The resistor-ladder linearity self-calibration can suffer a similar problem.

Another calibration method for space scientific instruments is a calibration of the whole experiment by exposing the sensors to a known physical value; there is a non-electrical calibration standard used instead of the electrical calibration standard. Such a process is commonly used for calibration of optical experiments during which a black-body system generates light of defined parameters [41]. It is obvious that such a solution is not simplifying the design of the instrument and does not solve the principal problem: the calibration system may suffer as significant damage due to space environment as the DAQ system itself. However, some experiments require post-launch calibration as their instruments are properly working only when exposed to real space conditions. An example would be the high-resolution electrostatic accelerometers that work only in zero gravity and space-grade vacuum [42].

2.2 Measurement uncertainty models

2.2.1 Measurement uncertainty versus measurement accuracy

Traditionally, the term "measurement accuracy" has been used in the industry to define the precision of the measuring instruments or processes. An illustrative example could be a specification of measurement accuracy of high-resolution digital multimeters (DMM). An application note [43] demonstrates the measurement accuracy of a Keysight 6.5-digit DMM as shown in Tab. 2.1.

Tab. 2.1: Accuracy specification of Keysight 34401A DMM, table adapted from [43].

Time from calibration [days]	**1 V DC voltage measurement accuracy [% of reading + % of range]**
1	0.0020 + 0.0006
90	0.0030 + 0.0007
365	0.0035 + 0.0007

Although such a definition seems to be appropriate, it is in conflict with the metrological definition of the term "measurement accuracy" as can be found in the VIM: *Measurement accuracy is the closeness of agreement between a measured quantity value and a true quantity value of a measurand.* The "true quantity value of a measurand" is unknown and unknowable. Hence, there is an additional note in the VIM: *The concept "measurement accuracy" is not a quantity and is not given a numerical quantity value*. To conclude, the usage of the term "measurement accuracy", despite its commonality in practical engineering, is in fact incorrect.

In contrast to the measurement accuracy, the VIM and GUM define a term "measurement uncertainty" as follows: *measurement uncertainty is a non-negative parameter characterising the dispersion of the quantity values being attributed to a measurand, based on the information used*. As illustrated in Fig. 2.2, the measurement uncertainty is typically expressed as a range of values in which the value of measurand is estimated to lie, within given statistical confidence, but it does not attempt to define or rely on a unique true value of a measurand [44], [45].

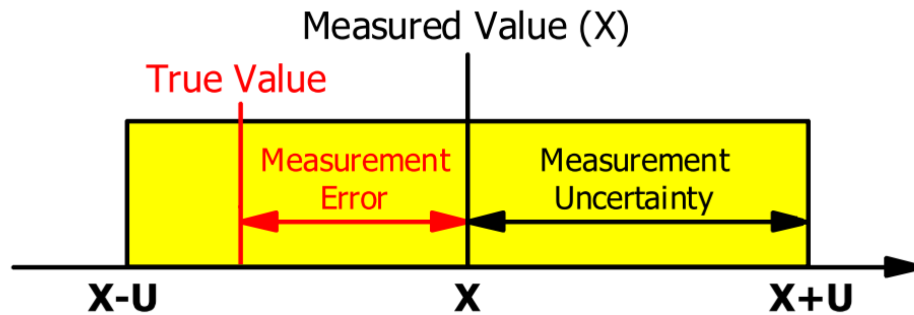

Fig. 2.2: Plot of the measurement uncertainty interval versus measurement error and the true value of the measurand (the quantity to be measured). Plot adapted from [45].

2.2.2 Standard estimation of measurement uncertainty

The process of estimating the measurement uncertainty (MU) is formally defined by the GUM. A variety of guidelines have been created to be used for practical applications. These include a NASA handbook [46] and a manual compiled by National Measurement Institute of Australia [47]. The MU analysis procedure is comprised of the following steps [46]:

1) Define the measurement process. Determination of the measurand, the type of measurement (direct or multivariate), parts of the measurement chain and environmental conditions to be used for the identification of the error sources.

2) Develop the error model. In the case of a multivariate measurement, an error model covers the contribution of measurement error of each measured quantity based on their sensitivity coefficients.

3) Identify the error sources and distributions. Measurement process errors are the key elements (contributors) of the MU analysis. For DAQ systems they include, but may not be limited to the following [46]:

- Reference and calibration error
- Repeatability and resolution error
- Environmental factors error (and possible correction errors)
- Computation error (data processing error)

The measurement errors can be characterised by probability distributions (mathematical descriptions that relate the frequency of occurrence of values to the values themselves). They include a normal, lognormal, uniform (rectangular), triangular, quadratic, cosine, exponential, U-shaped and trapezoidal. For the majority of measurements, the uniform and normal distributions are default choices; optionally the lognormal distribution is to be used for non-symmetric situations [46].

4) Estimate uncertainties. According to the GUM, the standard MU is determined from Type A uncertainty and Type B uncertainty estimates [47]. However, Type A and Type B are not types of errors; they are types of evaluation of error contributors [45].

Type A uncertainties are estimated by use of statistical methods. They represent a random error (noise) in the multiple measurements (samples) performed within a time short enough to eliminate variations due to systematic drifts and other long-term factors. The standard deviation s_x can be used to estimate Type A uncertainty u_{xA} in the mean value due to repeatability or random error [46], [48]:

$$u_{xA} \cong \frac{s_x}{\sqrt{n}}, \tag{2.1}$$

where n is the number of samples. The s_x is computed by taking the square root of the sum of the squares of sampled deviations from the mean [46], [48]:

$$u_{xA} = \sqrt{\frac{1}{n \cdot (n-1)} \sum_{i=1}^{n} (x_i - \bar{x})^2}, \tag{2.2}$$

where x_i are the samples, $\bar{x}$ is the mean value of the samples. Type A is suitable for evaluating variable measurement errors (random, deterministic and stochastic) and therefore it is not a method to be used for systematic (fixed) errors [45].

Type B uncertainty is defined by VIM as follows [33]: *Type B is an evaluation of a component of measurement uncertainty determined by means other than a Type A evaluation of measurement uncertainty*. For practical applications, Type B evaluation covers the systematic errors and errors induced by environmental conditions [45]. Each of the Type B uncertainty from a particular error source e_i can be expressed by the following formula [47]:

$$u_{eBi} = \frac{\Delta e_{i\max}}{\chi}, \tag{2.3}$$

where $\Delta e_{i\max}$ is the maximal contribution of the error source to measurement uncertainty, and χ is the coefficient converting the measurement error contributor to the standard uncertainty. Tab. 2.2 summarises the most common distributions used in MU evaluations; more functions can be found in GUM [48].

Tab. 2.2: Distribution functions used for MU evaluation [45].

Distribution	χ	Distribution	χ
Normal	2 (95 %), 3 (99 %)	Triangular	$\sqrt{6}$
Rectangular	$\sqrt{3}$	U-shaped	$\sqrt{2}$

5) Combine uncertainties. Firstly, the Type B contributors have to be combined. The following formula can be used for independent (uncorrelated) contributors [47]:

$$u_{xB} = \sqrt{\sum_{i=1}^{n} \left(A_i \cdot u_{eBi}\right)^2}, \tag{2.4}$$

where u_{xB} is the combined Type B uncertainty, and A_i are the conversion coefficients used to convert the Type B contributors to the same physical property as the measurand. The Type A and Type B uncertainties can be combined using the formula [46]:

$$u_x = \sqrt{u_{xA}^2 + u_{xB}^2}, \tag{2.5}$$

where u_x is the combined standard measurement uncertainty.

6) Set the confidence limits. Assuming the combined standard measurement uncertainty has a normal distribution, the confidence level is approximately 68 % [46]. Therefore the u_x needs to be extended by using a coverage factor [45]:

$$U_x = u_x \cdot \mathrm{k}, \tag{2.6}$$

where U_x is the extended measurement uncertainty and k is the coverage factor, which is k = 2 for the confidence level of 95 %, respectively k = 3 for the confidence level of 99 %.

2.3 Components selection for space DAQ systems

When designing a space qualified DAQ system, the engineers are often limited by the component selection. Once the standard space design processes are to be used (e.g. for ESA and NASA missions), the part selection options would be as follows [49]:

1. Space qualified components, ideally radiation hardened (rad-hard)
2. COTS components chips custom hardened and qualified for space
3. Standard COTS components

The A/D converter (ADC) is a key part of a high-precision DAQ system. Hence, the selection of the ADC component will be discussed in this section to illustrate the problems related to the space DAQ designs. Both space and COTS markets have been analysed for the availability of the high-resolution ADCs. There was a significant difference between the technological levels of these two industries as shown in Fig. 2.3.

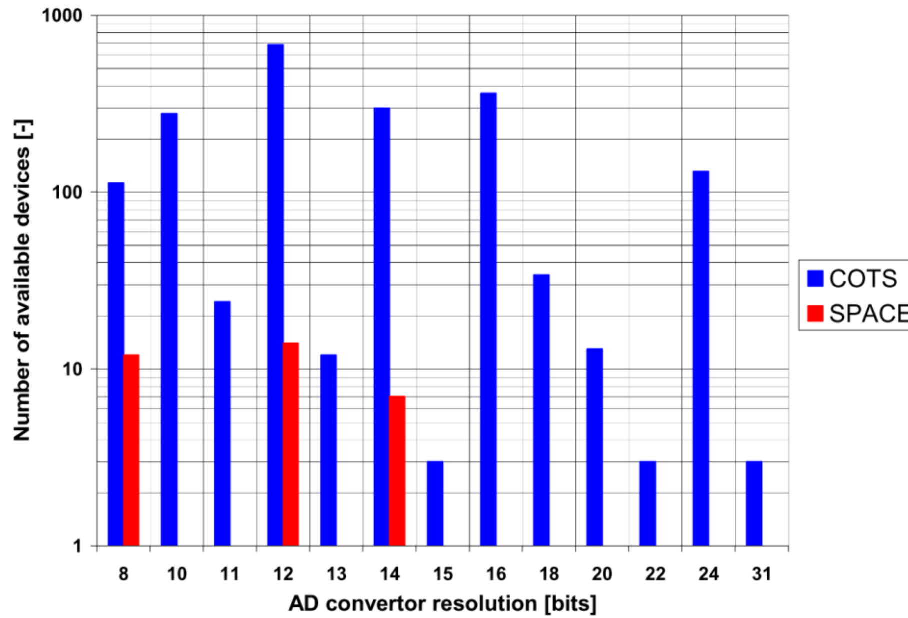

Fig. 2.3: A comparison of the number of COTS ADCs and space qualified ADCs available in 2014. Products of Texas Instruments, Analog Devices, Linear Technology, Maxim integrated and ST Microelectronics are included in this chart.

The absence of high-resolution ADCs in the space rad-hard component market is a clear indicator of the limited size and flexibility of the market. This situation seems to be caused by the fact that scientific missions of large space agencies have budgets high enough to cover the development of custom solutions, such as radiation-hardened versions of COTS ADCs components with the needs of their particular project in mind. A paper, published by Maxwell [50], demonstrates such an approach; three types of commercial ADC 16-bit parts were radiation hardened and tested to be qualified for NASA-JPL missions. Such an approach is affordable only for large space agencies and the lead times of such custom-made components could be in the order of years.

As demonstrated in the chart in Fig. 2.3, the COTS solutions seem to be the most practical option for low-cost missions due to the modern features, affordable price and short lead time. The benefits and challenges of the COTS components are discussed in detail in the chapter 5.2.1.

Among space-science projects, there are other civil applications, for which rad-hard and high-resolution ADC components are required: high-energy physics, nuclear power research, and medical applications.

The approach of the high-energy physics community has been demonstrated during the development of the electronics for the state-of-the-art LHC (Large Hadron Collider) in CERN [51]. The current version of the LHC experiment has a mixed radiation environment [52], which contains various types of radiation particles of the wide energy spectrum and various dose rates and will become even more challenging with the planned upgrades to the High-Luminosity system (HL-LHC) [53].

As far as the literature suggests, there were two principal methods used for the radiation hardening of the LHC electronics:

1. Custom developed rad-hard components for the most radiation exposed areas of the experiment. These included the electronics placed inside the detectors [54] and development of special Time-to-Digital Converters [55]. These were high-budget projects, and their use in space applications would be rather complicated due to the specific features of the developed devices and limited "off-the-shelf" availability of the parts.
2. COTS components were used in large quantities (tens of thousands), for instruments placed at lower-radiation positions of LHC. These included the LHC tunnel and its shielded areas. Various COTS ADCs were intensively tested by CERN engineers along with other components for collimators monitoring [56] and control systems of power converters for magnets [57]. The published results are very useful and can be used directly for low-cost space missions.

Radiation hardness assurance for medical applications is driven by slightly different requirements of the medical instrumentation and related quality/safety standards. These are commonly mass-produced commercial products. Therefore the development and qualification cost could be significantly higher, even comparable to the budgets of the large space missions. A typical solution is a development of radiation-hardened ASICs (Application Specific Integrated Circuit) and an extensive test campaign. An example of these designs could be the ASICs for medical imaging instruments. There were various research projects of medical imaging ASICs with the aim to be also used in space and nuclear applications [58], [59].

3 RADIATION AND TEMPERATURE EFFECTS IN SPACE ELECTRONICS

This chapter summarises the theoretical background of radiation and temperature effects in space electronics. It starts with a general definition of the radiation in space and continues with an overview of the radiation effects applicable to the space electronics. The radiation effects are discussed concerning the differences between the two key modern semiconductor technologies – MOS and bipolar. Another key topic is the temperature sensitivity of semiconductors due to its crucial role in the understanding of the performance of data acquisition systems. The chapter concludes with an overview of the synergy between the radiation effects and dependency on other physical quantities including the temperature.

3.1 Space radiation environment

The radiation in the space environment is composed of a variety of energetic particles with energies of a wide range from keV to hundreds of GeV and beyond [18]. These particles are either passing through the space environment or are trapped by the magnetic fields of planets. There are three main sources of the radiation in space [60]:

1. Galactic cosmic rays. These are high-energy charged particles including heavy ions extending to energies beyond TeV. Their fluxes are low, and all ions in the periodic table could be present.
2. Particles generated during solar events (solar flares). Solar eruptions produce a particle cocktail consisting mainly of energetic protons, but there are also alpha particles, heavy ions and electrons in it. The energies could reach hundreds of MeV.
3. Particles trapped inside planets' magnetospheres. These particles form radiation belts around the planets (e.g. Earth, Jupiter). This radiation typically consists of a broad spectrum of energetic particles.

3.1.1 Galactic cosmic rays

Galactic cosmic rays (GCRs) are charged particles that originate from outside the solar system. The GCRs are composed of 87 % protons, 12 % helium ions (alpha particles) and the remaining 1 % is heavy ions [61]. Highly energetic particles in the heavy ion component, or HZE (ions with high atomic number Z and energy E), play a particularly important role in space electronics. HZE particles, especially iron nuclei which are relatively major over the other high Z ions, possess high-LET and are highly penetrating, which make them virtually impossible to shield with a practically achievable thickness of the material. GCR HZEs dominate the GCR-induced single event upset (SEU) rate. GCR protons are mainly important to devices that respond to the very lightly ionising high-energy protons by direct ionisation (e.g., proton detectors) [62]. In contrast, the HZEs are a significant source of SEU. To summarise, the primary impact of GCR on spacecraft electronics are the heavy-ion-induced single event effects (SEEs).

The current models assume the distribution of GCR to be isotropic throughout the interstellar space. The flux of GCR becomes modulated in anti-correlation with solar activity due to the solar wind [63]: the GCR flux entering the solar system interacts with the solar wind and is partially attenuated. This attenuation is greatest during solar maximum when the solar wind is most intense. Contrarily, the GCR flux is greatest during solar minimum when the decreased solar wind produces less attenuation. This effect suppresses mainly the lower energy particles (below ~ 1 GeV), while the high energy particles are less attenuated [61]. The long-term observations of the sunspots and overall activity of the Sun suggest that the periodicity of the solar maximum and minimum take eleven years of which seven years are of the solar maximum followed by four years of solar minimum. The source and acceleration mechanisms of GCR are still not fully understood, and it is a topic of the high-energy astrophysics. The recent results from both the ground and in-orbit astronomical observations proved that the energy of cosmic rays could reach levels of tens of EeV (1 EeV ≡ 10^{18} eV) [64], but the fluxes of these ultra-high energy cosmic rays are very low.

3.1.2 Particles generated during solar events

The second source of the radiation in space are the stars; in the case of the solar system, it is the Sun. The solar energetic particles (SEPs) typically contain electrons, protons, alpha particles, neutrons, heavy ions, gamma rays, and X-rays. Energetic particles originate at some solar activity phenomena (e.g., by acceleration processes during solar flares, SFs, and coronal mass ejections, CMEs), because SEPs follow in time these solar eruptions [65]. SEP gamma-rays and X-rays travel at the speed of light. Therefore, they reach the Earth within approximately eight minutes. The SEP neutrons and charged particles can be observed within hours to days after the start of the solar event. Large solar events are related to the eleven-year solar cycle and are much more probable during solar maximum than during solar minimum. Only statistical predictions can be made for solar events. The time profiles of solar event articles show a rapid rise (a few hours or less), followed by a slow decay (several hours to several days) [62].

The SEPs can cause permanent damage, such as Total Ionizing Dose (TID) and Displacement Damage (DD) that is due mainly to protons and particularly due to the alpha particle components. The heavy ion content is small, but it cannot be ignored. Heavy ions, as well as protons and alpha particles, in solar particle events, can cause both transient and permanent SEE [66].

3.1.3 Trapped particles

The trapped particles around the planets are the third fundamental type of radiation source in space. In this thesis, only Earth's radiation environment will be discussed as it is in the interest of most of the in-orbit radiation test missions and in general, most spacecraft orbit Earth. The principal particles of the radiation environment of Earth are the protons and electrons trapped in Earth's magnetic field and thus creating Earth's radiation belts. These electrons and protons can penetrate the spacecraft shielding and are the main particles of interest for the TID part of radiation hardness assurance process (RHA). There are also some trapped heavy ions, but their energies are low enough to be stopped by a typical spacecraft shielding [62]. The Earth's radiation belts are often referred to as Van Allen belts after James Van Allen, who discovered them

using the results of the Explorer-1 mission [67]. The latest NASA mission focused on the detailed mapping of Earth's radiation belts was named Van Allen Probes in honour to this scientist [68]. Van Allen belts are most significant between 1000 to 60000 km, and they consist of the inner belt and outer belt. While the inner contains both electrons and protons, the major particles in the outer belts are electrons. The shape and energy spectrum of the belts strongly depends on solar activity [63]. As shown in Fig. 3.1, the spacecraft orbiting in the low Earth orbits (LEO) are under the massive shield of the radiation belts and therefore are well protected from the space radiation. This feature of the LEO orbit is a key benefit for the radiological protection of the crew of the international space station (ISS). In contrast, the satellites at higher orbits, including the geostationary orbits (GEO), are exposed to significantly higher radiation doses. Therefore, the orbit is a key factor for the planning of future space missions [69].

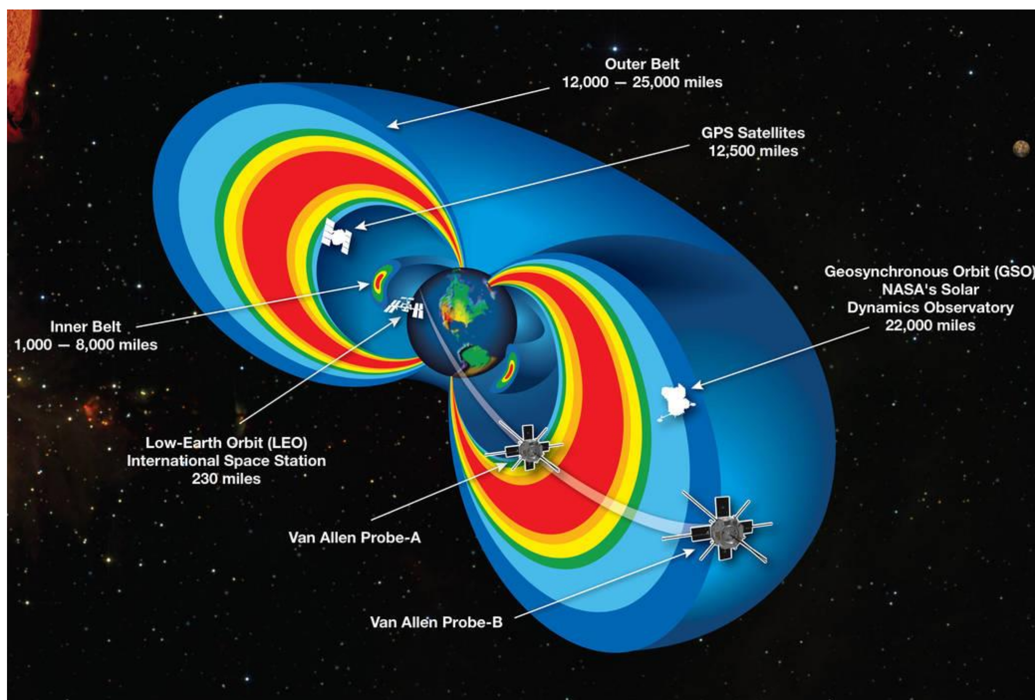

Fig. 3.1: A cutaway model of the radiation belts with the two Van Allen Probes satellites flying through them. The significant difference between the inner and outer belt can be seen. This graphic also shows other satellites flying in the typical orbits in the region of trapped radiation. Figure adapted from [68], credit: NASA

The energy of the trapped electrons in Van Allen belts differs between the belts; there are electrons with energies less than 5 MeV in the inner belt, and the outer belts contain electrons with energies up to 7 MeV. The flux of electrons in the outer belt is about an order of magnitude higher than in the inner belt [61]. The protons are located mainly in the inner belt, and their energy spectrum is more complex than for electrons. The energy of protons starts with a few MeV and can reach hundreds of MeV [62]. The Van Allen belts are very dynamic environments mainly relying on the dynamics of the Earth's magnetosphere driven by the activity of the Sun. There are solar events with a time constant from minutes (sub-storms) up to weeks (storms). While these are not significant for the understanding of the variations of the induced total dose, the eleven-year solar cycle is fundamental [66].

3.1.4 South Atlantic Anomaly

A particular feature of the Earth's radiation environment is the South Atlantic Anomaly (SAA). As the axis of the Earth's magnetic field is not entirely in parallel with the Earth's axis of rotation, there is a region off the coast of Brazil, where the geomagnetic field is significantly closer to the Earth's surface. SAA has great importance for the spaceflights as it allows the protons from the inner Van Allen belt to reach the Earth's atmosphere. Most of the total dose collected on low-altitude orbits is typically from the passes through the SAA [60]. The latest studies suggest that the SAA is not static: its position and shape significantly changes with the time. This important effect is caused by the long-term changes of the Earth's dipole moment [70].

3.1.5 Space environment models

There were many models of the space environment developed during the more than fifty years of the research. They are based on dosimetry data gathered during the space missions and on astrophysical models. One of the standard modelling tool used by the space industry is the SPENVIS system developed by ESA [71]. Using these models and in-orbit data from flown missions the typical TID doses can be estimated. Results from such an analysis, created recently by the French space agency, can be seen in Tab. 3.1.

Tab. 3.1: Typical mission doses (indicative) for encapsulated equipment inside a middle size spacecraft, table adapted from [72].

Mission	Duration	Typical TID	Note
LEO missions	5 to 10 years	Few krad(Si)	600 to 800 km altitudes
JASON	5 years	10 to 20 krad(Si)	LEO; Joint Altimetry Satellite Oceanography Network; research S/C
GLOBALSTAR	15 years	60 krad(Si)	LEO; constellation for satellite phone and low-speed data communications
GEO missions	15 years	10 to 50 krad(Si)	GEO; typically telecommunication missions
GNSS	15 years	30 to 80 krad(Si)	Global Navigation Satellite System (GPS, Galileo, GLONASS)
Mars mission	5 to 10 years	Few krad(Si)	Typical Mars exploration mission
JUICE	11 years	50 to 150+ krad(Si)	Jupiter Icy Moons Explorer; a planned ESA mission

3.1.6 Artificial radiation in space

Among the natural sources of radiation discussed above, the spacecraft could also be exposed to artificial (human-made) sources of radiation. One particular source of radiation is created by the onboard radioisotope thermoelectric generators (RTG), used for supplying electricity on the deep-space missions, where the solar panels would not be efficient enough to provide electrical power and heating for the payload [73]. The shielding of these radiation sources causes a significant increase in the weight of these spacecraft which is even more critical for the deep-space missions.

Another example of artificial enhancement of the natural radiation environment in space is represented by the high altitude nuclear explosions. Such a test would result in the injection of high energy electrons into the magnetosphere causing enhancement of the electron populations by many orders of magnitude. Experiments as STARFISH performed in the early 1970's caused failures on satellites [74].

3.1.7 Deep space environment

The current understanding of the space environment is limited to the data gained from the space missions; therefore the models for deep-space are limited as there were only a few missions to the edges of the solar system. As of 2019, the key deep-space data are still being obtained by the Voyagers spacecraft - the first human-made interstellar missions [75]. With forty years of operation in space(including the harsh Jovian environment) the Voyagers proved that ultra-long-life spacecraft can be designed [76].

3.2 Radiation effects in space electronics

In general, the space radiation causes two major types of radiation-induced effects in space electronics:

1. Cumulative effects: total ionising dose effects (TID) and displacement damage effects (DD)
2. A wide range of single events effects (SEE).

As can be seen in Fig. 3.2, these effects are partially linked as there have been synergistic effects observed during combined radiation experiments. The TID-induced enhancement of SEE sensitivity is an important synergistic effect for the space electronics industry [77].

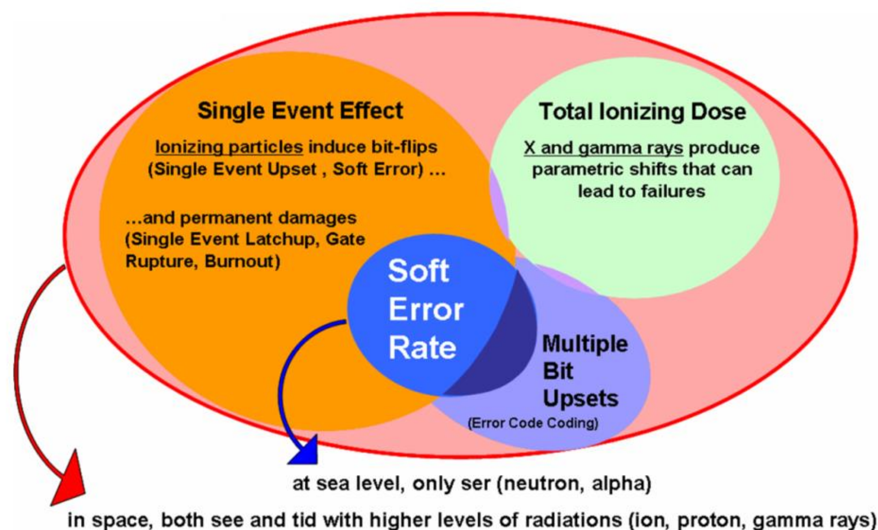

Fig. 3.2: An overview of the family of radiation effects on space electronics and the links between the effects. As the graphics suggest, there is a link between SEEs and TID effects. Figure adapted from [78].

3.2.1 Total ionising dose effects

The TID is cumulative damage induced to the device by exposure to ionising radiation. It typically leads to a degradation ("shift") of device parameters and may end up in its functional failure (in some literature defined as a "catastrophic" failure [79]). The device would typically fail to operate either when its internal compensating circuits are not capable of keeping the device bias points within the designed operational range, or when the increase of the supply current causes a thermal overload of the device. Total dose level is an essential parameter of space rated electronic devices and is defined as TID level, for which the device is still within the specified parameters. The TID physical unit, traditionally used in space electronics, is a rad (radiation absorbed dose) even though the SI derived unit of absorbed radiation is a gray (Gy) [80]. One rad is defined as 0.01 Gy, and that corresponds to deposition of the energy of 0.01 J per 1 kg of the target material. As absorption depends on the target material, the TID level is typically indicated with the target material. For silicon devices, the TID level is defined in rad(Si) [79]. In contrast to classical ageing effects, the TID effects are partially reversible due to the annealing process. The resulting TID degradation is a combination of the cumulative exposure to radiation and concurrent annealing [81].

3.2.2 Displacement damage

Second important cumulative type of radiation effect is the displacement damage (DD). It occurs in semiconductor materials due to scattering interactions of energetic particles with the atoms of the semiconductor lattice. DD could be caused by a variety of particles such as protons, neutrons, and even high-energy electrons [62]. The displacement damage produced by different particles and energies is determined by the Non-ionizing Energy Loss (NIEL) [82]. The devices most affected by DD are those that interact with or emit optical radiation. Those devices include optoelectronics such as LEDs, optocouplers, and laser diodes. Displacement damage causes an increase in the threshold current of LEDs and thus lowers the CTF (Current Transfer Ratio) of optocouplers. Similar degradation mechanisms are crucial for laser diodes used in fibre optics [83]. The space industry is also focused on the DD effects in solar cells and CCD devices [79].

3.2.3 Single event effects

A single event effect (SEE) can be caused by a single charged particle travelling through a sensitive part of the device, and creating ionising track behind it. Depending on the response of the device (and potentially of the whole system) the SEE may be categorised either as a soft event, during which the data could be corrupted, or a hard event, which can lead to a catastrophic (destructive) failure of the device [79]. In comparison to TID and DD, the SEE can occur stochastically. The duration of a SEE is of the order of nanoseconds. While the cumulative effects (TID, DD) are assumed to be uniform across the whole device, the SEE affects only a particular part of the device; the corrupted area is typically tens of square nanometres [84]. The SEE sensitivity of a device is a function of the linear energy transfer (LET), which is usually normalised by the density of the target material, and is measured in $MeV \cdot cm^2 \cdot mg^{-1}$.

A device could be corrupted by one of the following SEE mechanisms [85]:

- Single event upset (SEU): a soft effect causing corruption in a single bit of memory or register. Correction logic can restore the original value.
- Multiple-bit upset (MBU): a soft effect causing corruption of multiple adjacent bits of memory or register
- Single event transient (SET): a voltage/current transient in the digital or analogue part of the device. It may propagate through the IC and eventually be latched in a storage cell (memory, register). The analogue SETs are typically transient pulses in operational amplifiers, comparators, voltage references. Carefully designed analogue filters or signal processing can suppress analogue SET.
- Single event functional interrupt (SEFI): loss of functionality of digital devices due to perturbation of control registers, state machines, or clock circuits (PLLs). SEFIs are soft effects and can be recovered by resetting or power cycling the device.
- Single event gate rupture (SEGR): a hard/destructive effect causing a rupture of the gate oxide. Typically a problem of power MOSFETs.
- Single event burnout (SEB): a hard/destructive effect leading to burnout of a power device due to the activation of parasitic bipolar structures.
- Single event latch-up (SEL): a radiation-induced activation of parasitic bipolar structures inherently present in CMOS structures that lead to a rapid increase in the supply current. If the supply current is not limited, this may lead to a destructive event (thermal overload).

3.3 Total ionising dose effects in MOS devices

The metal oxide semiconductor (MOS) technology is the key process of manufacturing modern electronic devices [86], especially in the form of CMOS (Complementary MOS). The key TID-induced problems in a MOS include threshold voltage shift, increased leakage current, and degraded timing parameters [62].

3.3.1 Gate threshold voltage shift

The most crucial TID-induced degradation of MOS devices is the gate threshold voltage shift, as illustrated in Fig. 3.3. During the normal operation (A), the application of an appropriate gate voltage causes a conducting channel to form between the source and drain so that current flows when the device is turned on. The effect of TID is illustrated in figure (B): TID-induced trapped charge has built up in the gate oxide, causing a shift in the threshold voltage. If this shift is large enough, the device cannot be controlled. This extreme case leads to functional failure of the device [87]. Regarding the construction of commercial devices, the TID-induced charging of the oxide involves several different physical mechanisms, which take place on very different time scales, with different field dependences, and various temperature sensitivities. Therefore the overall radiation response of a device or circuit was found to be extremely complex, but the problem could be divided into its components, and those have been studied individually [18], [30].

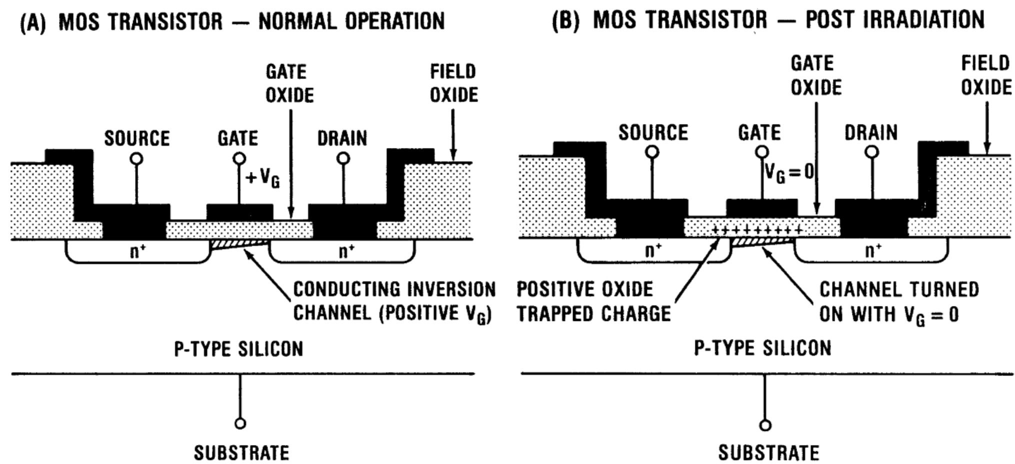

Fig. 3.3: Schematic of the structure of n-channel MOSFET showing the radiation-induced charging of the gate oxide in two modes: (A) normal operation and (B) post-irradiation. Figures adapted from [87].

In general, two dominant components are assumed to cause the gate threshold voltage shift [18]:

- oxide trapped charge (also known as charge trapping)
- interface trapped charge (or interface traps)

Typical I_D-V_{GS} curves of irradiated MOSFETs are plotted in Fig. 3.4 to demonstrate the contribution of these two components. While the oxide-trapped charge causes a simple translation of the I_D-V_{GS} characteristics, the interface trapped charge is responsible for both shift and distortion of the curve [18].

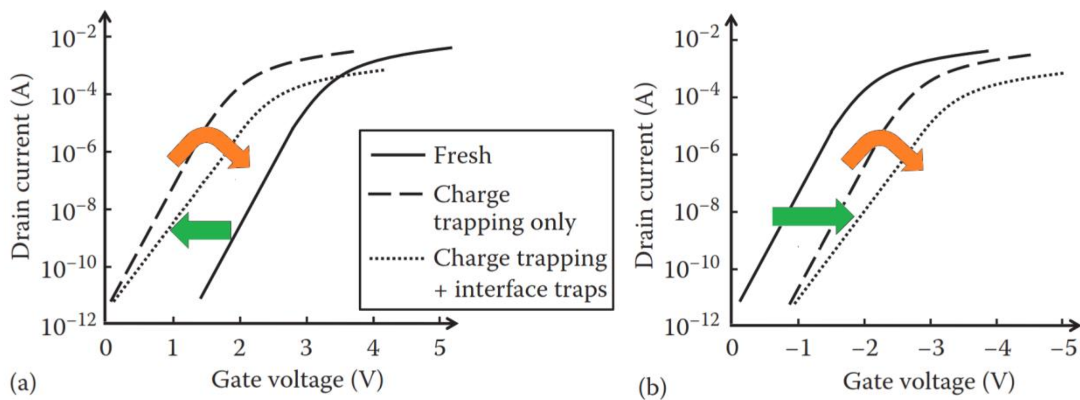

Fig. 3.4: Effect of oxide trapped charge and interface trapped charge on I_D-V_{GS} curves of MOSFETs. Chart (a) shows n-channel type and (b) displays a p-channel. Figures adapted from [79].

There is a notable difference in the TID response (green arrows in Fig. 3.4) of the n-channel and p-channel MOSFETs. Positive oxide trapping and interface traps cause additive effects in p-channel MOSFETs (orange arrows) because they both tend to shift the I_D-V_{GS} characteristic towards higher V_{GS}. In contrast, these effects tend to cancel

in n-channel MOSFET. In CMOS circuits, the different TID response of both the p-channel and n-channel types may cause a degradation of the complementarity of the CMOS.

The gate threshold voltage shift is a time-dependent variable, and therefore the actual gate threshold voltage V_T can be expressed as [87]:

$$V_T(t) = V_{T0} + \Delta V_T(t), \tag{3.1}$$

where V_{T0} is an initial threshold voltage before irradiation and $\Delta V_T(t)$ is the TID-induced threshold voltage shift. The $\Delta V_T(t)$ consists of three components:

$$\Delta V_T(t) = \Delta V_{st}(t) + \Delta V_{ot}(t) + \Delta V_{it}(t), \tag{3.2}$$

where $\Delta V_{st}(t)$ is a short-term contribution from the TID-generated mobile holes transporting in the oxide bulk, $\Delta V_{ot}(t)$ is caused by the deep trapped holes near the interface, and finally, $\Delta V_{it}(t)$ is the contribution from the charged interface traps. The equations for all three $\Delta V_T(t)$ components are based on the oxide capacitance per unit area C_{ox}, which is defined as:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \tag{3.3}$$

where ε_{ox} is the dielectric constant of the oxide and t_{ox} is the thickness of the oxide. The following formula defines the $\Delta V_{st}(t)$:

$$\Delta V_{st}(t) = \frac{-q}{C_{ox}} \int_0^{t_{ox}} \frac{dx}{t_{ox}} n_h(x,t), \tag{3.4}$$

where q is the electronic charge, $n_h(x, t)$ is the space and time-dependent density of free holes. Distance x is measured relative to the gate/oxide interface. The $\Delta V_{ot}(t)$ can be calculated as:

$$\Delta V_{ot}(t) = \frac{-q}{C_{ox}} \Delta N_{ot}(x,t), \tag{3.5}$$

where $\Delta N_{ot}(x, t)$ is the TID-induced areal density of deep trapped holes near the oxide/silicon interface. It is time-dependent for two reasons: firstly due to its time-dependent build-up as the transporting holes reach the interface, and secondly because of its long-term annealing (years).

This set of equations is concluded with the definition of the $\Delta V_{\mathrm{it}}(t)$ as follows:

$$\Delta V_{\mathrm{it}}(t) = \frac{-\Delta Q_{it}(t)}{C_{\mathrm{ox}}}, \tag{3.6}$$

where $\Delta Q_{\mathrm{it}}(t)$ is the TID-induced interface trapped charge. It can contribute either net-negative charge ($\Delta Q_{\mathrm{it}}(t)$ with a negative sign as in equation (3.6)) or with a net-positive charge. The polarity depends on the type of channel (negative for n-channel).

3.3.2 TID-induced degradation of CMOS devices

An example of a typical TID-induced degradation sequence of a CMOS device is shown in the Tab. 3.2. These effects are caused predominantly by the TID-induced changes of the threshold voltage. A system malfunction may occur already at level 2 when the threshold voltage V_{T} of the n-channel transistors crosses the zero voltage leading to a rapid increase of the supply current (typically in orders of magnitude) [18].

Tab. 3.2: Four types of failure modes in typical LSI CMOS circuit from successive irradiations, table sourced from [18].

Level	Typical TID [krad(Si)]	ΔV_{T} [V]	Main degradation effects
1	0.8	0.2	minor reduction in noise immunity minor loss in switching speed device out of datasheet specification
2	5	1	the rapid increase in supply current
3	10	2	significant switching speed reduction
4	30	4	Functional failure – impossible to change logic state

3.3.3 MOS leakage current

The radiation-induced leakage current (RILC) is a problem independent of the threshold voltage shift phenomenon and is related mainly to the implications of the application circuits and the risk of reduced reliability of the devices. RILC may cause a breakdown in the oxide, or a “wear out” of the gate oxide (reduced lifetime of the device) [88]. RILC was observed on ultra-thin gate oxide devices at high doses (Mrads) from Cobalt-60 gamma rays [89] and also from other radiation sources [90].

3.3.4 MOS gate oxide thickness

A key technological parameter controlling the radiation hardness of the MOS devices is the gate oxide thickness. As the thickness of the gate oxide decreases, radiation hardness improves [90]. Fig. 3.5 shows threshold-voltage shifts due to interface-trap and oxide-trapped charge for dry and steam grown (wet) oxides. Because of the improvement in hardness with decreasing thickness, gate oxides in advanced commercial technologies can be extremely radiation tolerant, but there is a potential problem with the RILC [91].

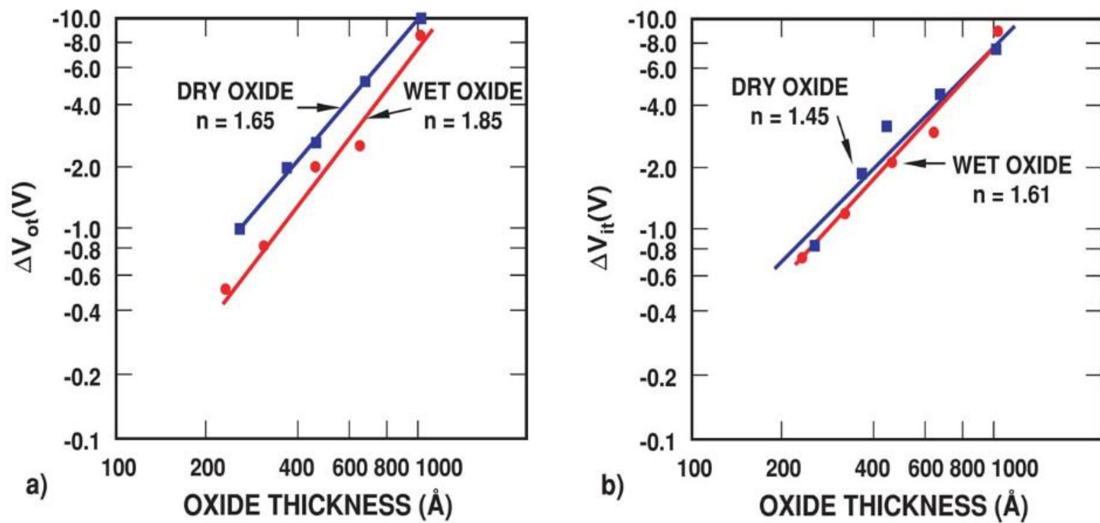

Fig. 3.5: The dependence of the threshold-voltage shift on the gate oxide thickness due to a) oxide trapped charge and b) interface trap charge. 1 Å = 0.1 nm. Charts adapted from [90].

To interpret the results of the TID experiments, the knowledge of the gate oxide thickness is essential. Unfortunately, for the majority of the tested COTS (Commercial-Off-The-Shelf component) the technological details are strictly confidential. Most of the vendors are not willing to provide these details, as a radiation testing of their COTS products conflicts with their space product business. Another motivation is the general protection of their IP. One way to work around this issue is to perform a complex "reverse engineering" of the die of the tested device, allowing a direct measurement of the particular technological parameters [92]. However, such an effort requires a high-tech semiconductor laboratory equipped with an electron microscope.

3.3.5 Future CMOS devices

The development of modern CMOS devices still follows Moore's Law [93]. To make such aggressive technological growth possible, the international technology roadmap for semiconductors (ITRS) has been constructed [94]. Its purpose is to identify the capabilities needed for the semiconductor industry to remain Moore's law valid for the technology development. The next-generation technologies, currently considered by ITRS, are as follows [94]:

- ultra-small bulk CMOS
- fully depleted silicon-on-insulator (SOI)
- ultra-thin gate oxides
- high-k gate dielectrics

These technologies bring new challenges not only to the semiconductor industry but also to the radiation effects research and test community [90].

3.4 Total ionising dose effects in bipolar devices

In space electronics, the bipolar junction transistor (BJT) technology is used in both discrete and integrated form. The main applications are analogue and mixed-signal ICs, especially when combined with MOS into the BiCMOS technology [95]. In comparison to the MOS devices, the BJT technology can provide higher speed, higher gain, and lower output resistance [96]. In general, the TID produces degradation of gain and an increase in the leakage currents in BJTs [18].

3.4.1 BJT device structures

The traditional vertical structure of an NPN transistor is shown in Fig. 3.6 a). The red dashed line in this figure defines the area where the transistor is the most sensitive to TID: the surface of the base region, where it intersects the overlying oxide [97]. Defects in the silicon/oxide interface over the base have the strongest influence on the sensitivity to the TID. Charge trapped in the base oxide partially inverts the base, which leads to increased collector current, even when the base is biased off [98]. When the base current is increased, the collector current increases less than in a non-exposed device. This effect reduces the current gain.

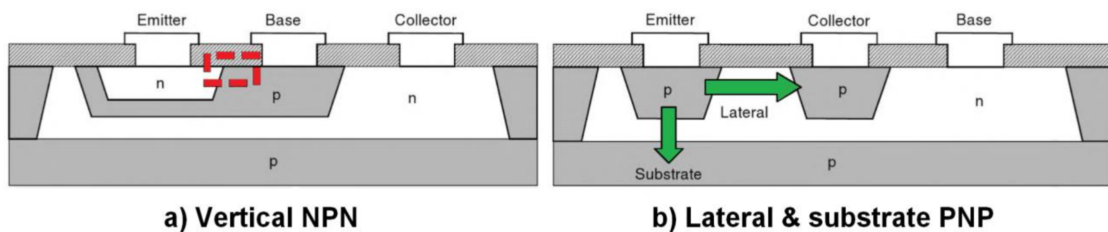

Fig. 3.6: Cross-sections of typical BJT structures: a) shows a conventional vertical NPN transistor; the dashed lines indicate its most radiation-sensitive section. Picture b) represents the lateral and substrate types of PNP. The green arrows indicate the current flow of each type of PNP devices. Illustrations adapted from [99].

Three basic types of PNP bipolar transistors are used in ICs [97]. The structure of vertical PNP transistors is similar to vertical NPN devices. Fig. 3.6 b) shows qualitative cross sections of lateral and substrate PNP transistors. The active region of the lateral PNP is at the silicon surface, and the current flows laterally between emitter and collector regions. These regions are both at the surface. Substrate PNP devices have a vertical current-flow pattern, and their substrate works as the collector. The lightly doped n-type base can be quite sensitive to radiation, particularly at the oxide interface [100].

The work published in [98] proved that lateral PNP devices were the most sensitive because the current flow was along the Si surface, right below the base oxide. Defects in the oxide have the greatest effect because the current is closer to the oxide for longer than in any other device type examined. The lateral PNP was 20-50x more sensitive than in any other device type tested.

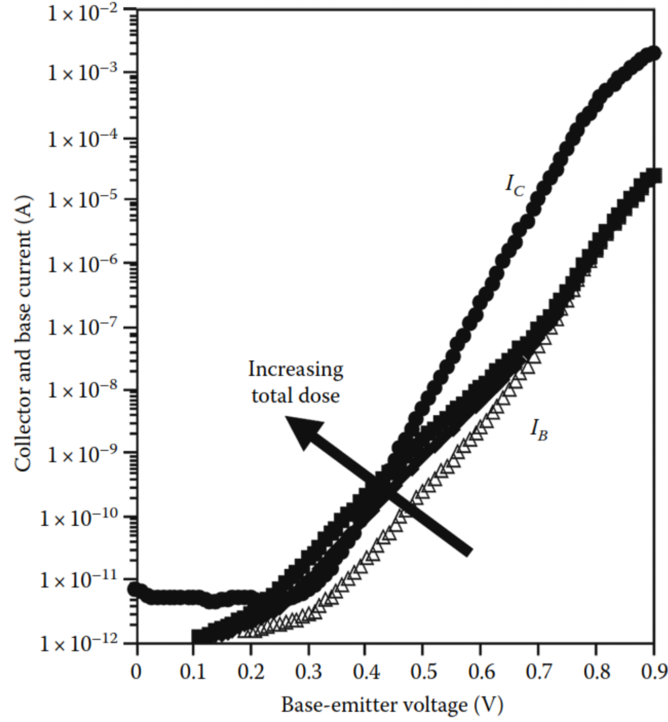

Fig. 3.7: Collector and base current versus base-emitter voltage (Gummel plot) for an irradiated NPN BJT. Chart adapted from [100].

3.4.2 Degradation of BJT gain

When a BJT is exposed to radiation, the base current increases, but the collector current typically remains relatively constant, causing the current gain to decrease [18]. An example Gummel plot is shown in Fig. 3.7. As can be seen in the plot, the collector current remains virtually unchanged except at very low bias levels, while the base current increases significantly and thus causes a large reduction in the current gain, especially at low bias levels where the base current increases most rapidly. The classical definition of the current gain of a BJT is based on the most used amplifier topology of the BJTs - the common-emitter as follows:

$$h_{FE} = \frac{I_C}{I_B}, \tag{3.7}$$

where h_{FE} (or β in some literature) is the common-emitter current gain, I_C is a collector current, and I_B is a base current. The TID-induced degradation of the h_{FE} gain is usually defined as a “gain damage figure” $\Delta(1/h_{FE})$ represented by formula [18]:

$$\Delta(1/h_{FE}) = (1/h_{FE}) - (1/h_{FE0}), \tag{3.8}$$

where h_{FE0} is the current gain before irradiation, and h_{FE} is the current gain after the irradiation.

The chart in Fig. 3.8 illustrates TID-induced degradation of current gain of various conventional BJT transistors and input transistors for two operational amplifiers measured by Johnston et al. [101]. The transistors were irradiated with 75 % of the rated V_{CE} from collector to emitter, and -2 V applied from base to emitter. The operational amplifiers were irradiated in a closed-loop condition with power supply voltages of 15 and -15 V. This experiment was performed at a dose rate of 180 krad(Si)/h.

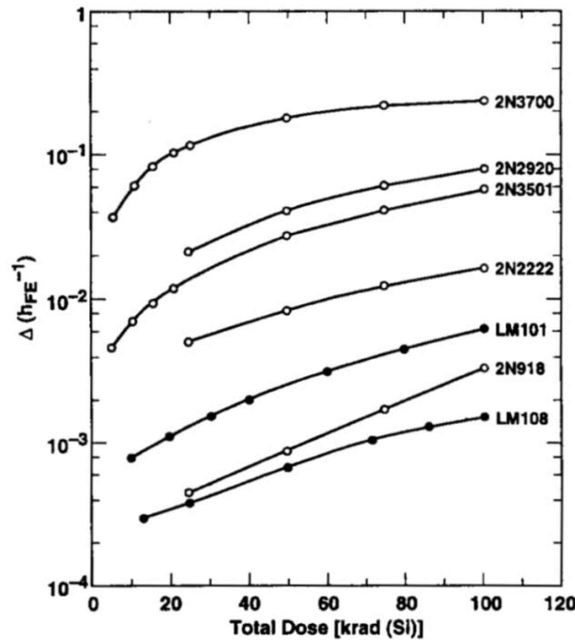

Fig. 3.8: TID-induced change in $\Delta(1/h_{FE})$ at low currents for the various device types. Chart sourced from [101].

3.4.3 BJT leakage current

In some bipolar ICs, the only requirement for the current gain is that it exceeds some minimum value and therefore the ICs are TID hard to a certain dose due to the gain margin. In these ICs, the TID-induced leakage current could be the dominant failure mechanism [97]. There are three types of leakage currents considered to be products of the response of the BJT technology to TID:

- leakage currents in discrete devices
- the increase of the input current of bipolar ICs
- device-to-device leakage current within bipolar ICs

Increase in collector-base reverse leakage currents I_{CBO} is typically caused by the formation of a surface channel [81]. This current is then amplified by h_{FE} to produce additional collector current. Data published by Holmes-Siedle [18] shows that the I_{CBO} may increase by order of magnitude when BJT exposed to 100 krad(Si), but the accuracy of the modelling of this phenomenon is limited due to the device-to-device difference (scattered results from the TID experiments).

The work [102] reported functional failures of glue logic ICs fabricated using the recessed field oxide process. These devices were failing at very low TID levels of 5 krad(Si). The failure was caused by the input leakage current high I_{IH}. This problem was originated by the inversion of the p buried layer channel stop (guard band) under the recessed field oxide isolation between n-type regions as illustrated in Fig. 3.9.

In addition to the input current problem, the collector-emitter leakage current in walled-emitter transistors can also cause the functional failure of a bipolar IC as shown in Fig. 3.9. The collector-emitter leakage is the result of inversion of the p-type base along the recessed field oxide sidewall [103].

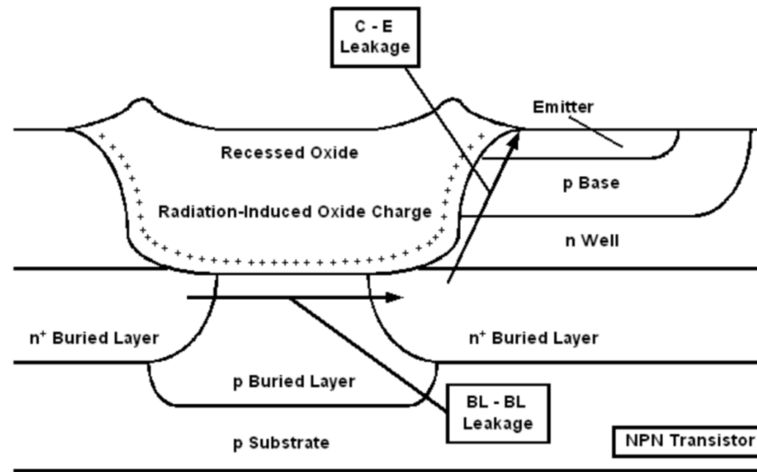

Fig. 3.9: Cross section of recessed field oxide bipolar NPN transistor showing buried-layer-to-buried-layer leakage path and collector-to-emitter leakage path [103].

3.5 Dose rate sensitivity

The majority of both commercial and experimental TID tests are performed under accelerated conditions. For example, as defined in Tab. 3.1, the maximal dose rate of an LEO mission is approximately 2 krad(Si)/year. Assuming an even distribution of the dose over the time, that would be equal to a dose rate of 0.23 rad(Si)/hr. The lowest dose rate the commercial TID tests are executed at is 36 rad(Si)/hr [18]. That is why even the TID tests, performed under the lowest dose rate test conditions, are approximately 100x accelerated concerning dose rates in LEO. Therefore the understanding of a potential dose rate sensitivity of the irradiated devices is crucial for the realistic interpretation of TID test results. As for the TID effects, there is a principal difference in the dose rate sensitivity of the bipolar and MOS devices.

3.5.1 Dose rate sensitivity of bipolar devices

A variety of TID experiments have proved the dose rate response of bipolar devices to be a complex problem [104], [105]. Fig. 3.10 illustrates results of a TID test of LM117 as reported in [106]. LM117 is a linear positive voltage regulator. In this test one set of LM117s was exposed at high dose rate (HDR) of 540 krad(Si)/hr, and another set was

irradiated at low dose rate (LDR) of 5.4 krad(Si)/hr. The measured, non-monotonic, response of the device suggested complex changes in the circuitry. The changes were related to the circuit-level compensation of effects of one part of the circuit by the effects in another part of the circuit (a current source). This experiment demonstrated that the dose rate might not only control the magnitude of the TID-induced degradation, but also the polarity of it (the LDR results were practically opposite to the HDR).

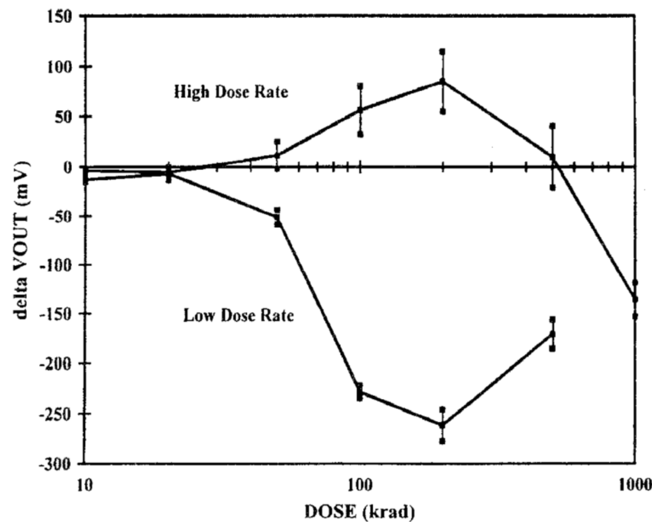

Fig. 3.10: TID-induced change of the output voltage for an LM117 irradiated at high and low dose rates. Figure sourced from [106].

3.5.2 Enhanced low dose rate sensitivity in bipolar devices

As demonstrated in the previous section, the BJT technology may suffer a strong negative dependence on dose rate (the lower dose rate, the higher sensitivity to TID). This phenomenon is in a potential conflict with the conventional accelerated TID test methods. Therefore a variety of experiments have been performed to investigate the impact of dose rate on the accuracy of TID data. The low and ultra-low dose rate TID tests proved this effect to be real, and it became to be recognised as an Enhanced Low Dose Rate Sensitivity (ELDRS) [18].

When the TID-induced degradation is plotted versus dose rate, it typically exhibits a non-linear response, as illustrated in Fig. 3.11. The chart shows a normalised current gain versus dose rate for a particular lateral PNP BJT, demonstrating that the device sensitivity changes significantly [97]. The TID level was constant at 20 krad(Si) for all measurements. The plotted scale covers the range of dose rates from the expected dose rates in the space environment (green area in the chart) up to typical dose rates used for ground TID tests (yellow interval). The most rapid variation was in range between 0.1 and 10 rad(Si)/s (0.36 to 3600 krad(Si)). In general, dose rate sensitivity is strongly dependent on technology; therefore if a device exhibits ELDRS, the particular range of dose rates over which it occurs is difficult to predict [100].

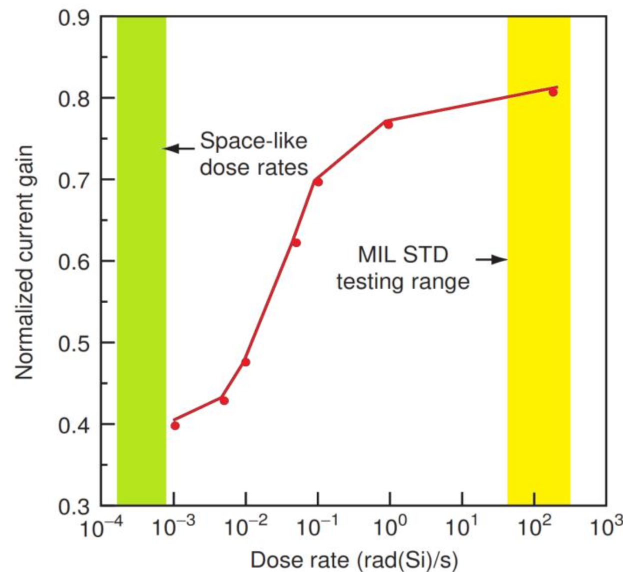

Fig. 3.11: Normalised current gain versus dose rate for a lateral PNP BJT irradiated to TID level of 20 krad(Si) as a function of dose rate. The degradation of gain increases at low dose rates expected in the space environment. Chart adapted from [97].

As discussed in [105], the original understanding of the ELDRS was that the BJT devices could be significantly more sensitive at low dose rates. Soon after the discovery and acceptation of the phenomenon, the first models were published [107], [108]. The models showed that the mechanism was in fact not an "enhanced" degradation at low dose rate but "reduced" total dose degradation at high dose rate. Therefore the authors suggested a more accurate acronym RHDRS (Reduced High Dose Rate Sensitivity). Holmes-Siedle refers to this effect as SHDRS (Suppressed High Dose Rate Sensitivity) [18]. Nevertheless, the original term ELDRS remains to be used by the industry.

The lack of the LDR data of the bipolar devices and the need to demonstrate if the ELDRS was a real effect in space triggered a project of an in-orbit ELDRS experiment. The experiment was part of the Microelectronics and Photonics Testbed (MPTB) mission launched in 1997 [109]. The DUTs (devices under test) were LM124 (quad operational amplifier) and LM139 (quad differential comparator). The parts accumulated TID level of 45 krad(Si) during the approximately seven years experiment. The orbit was highly elliptical geosynchronous transfer orbit (GTO), and therefore the payload received most of the TID in the one-hour flight through the Van Allen belts during each twelve-hour orbit.

The results for the LM139 are shown in Fig. 3.12 as a comparison of various ground tests at different dose rates to the in-orbit measurements [110]. The average data of two packages (eight DUTs) for the space experiment and three packages (twelve DUTs) for ground TID tests for each condition are plotted. Despite the fact, that the actual mission environment consisted of protons and electrons of various energies and widely changing dose rates [111], the in-orbit degradation was between the degradation at a constant dose rate of 1 mrad(Si)/s and 10 mrad(Si)/s using cobalt-60. Although the average mission dose rate was 0.2 mrad(Si)/s, the dose rate during the flights through the belts was approximately 2.4 mrad(Si)/s, which was in excellent agreement with the ground tests.

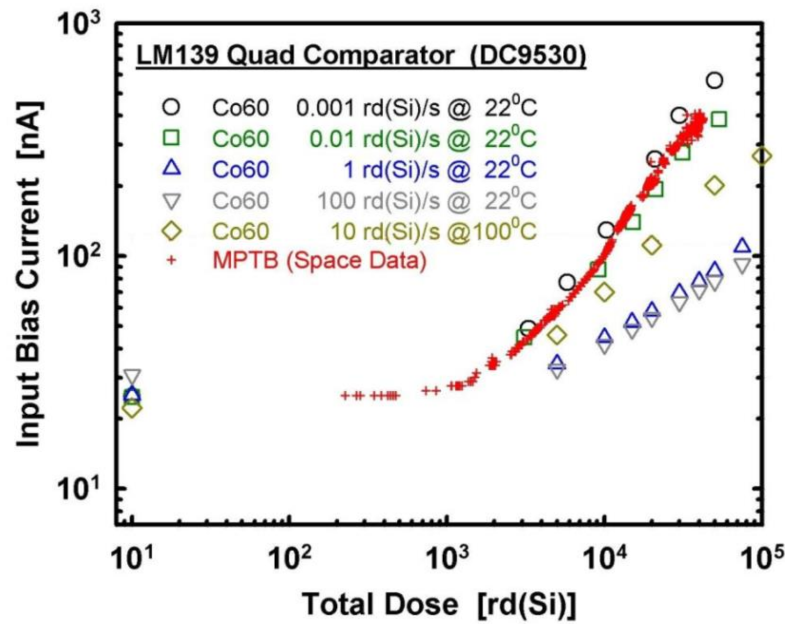

Fig. 3.12: Comparison of MPTB space data to ground cobalt-60 test data for input bias current (I_{IB}) of the LM139 comparator (rd is short for rad). Figure adapted from [110].

From the semiconductor physics point of view, the ELDRS could be explained by three general categories of effects [97]:

1. space charge effects due to slowly transporting holes
2. bimolecular explanations: hydrogen reactions or molecular hydrogen formation combined with electron-hole recombination
3. binary reaction rate processes

Various potential influences of the fabrication process were investigated. The thermal history of the devices [105] appeared to be a significant issue, and it is nowadays recognised as pre-irradiation elevated temperature stress (PETS). The presence (or absence) of the passivation layers on the die is also considered to be an ELDRS driver [18]. The influence of the hydrogen contamination on the ELDRS has been investigated as well [112].

3.5.3 Dose rate sensitivity of MOS devices

The early works from the 1980's suggested that there was no "true" dose rate effect (TDRE) in MOS technology as there is the ELDRS in bipolar devices [87], [113]. A TDRE is assumed when the degradation at the end of LDR irradiation is greater than the degradation measured after HDR irradiation to the same dose, followed by a room temperature anneal for a time at least as long as the LDR irradiation time. A time-dependent effect (TDE) means that the degradation at HDR and LDR is essentially the same when measured at the same time from the beginning of irradiation (including anneal time). The TDE effects were observed in the MOS technology [105].

A comprehensive set of experiments was performed by Sandia [114] to investigate a potential dose rate sensitivity of the CMOS technology. This work covered eleven orders of magnitude of dose rates from 0.05 to 6×10^9 rad(Si)/s. Such a wide range was

achieved by the use of a variety of radiation sources including LINAC, cobalt-60, caesium-137 and X-ray. The work reported within 10 % accuracy that there was no TDRE observed. The samples were CMOS transistors with 30 to 60 nm gate oxides. The accuracy was assumed to be limited by the accuracy of the dosimetry systems.

However, some later works suggested that there are potential TDRE effects in the modern MOS technology. A possible ELDRS effect was measured in the leakage current tests of n-channel MOSFETs [115]. National Semiconductor published a work reporting results of LDR/HDR TID testing of various mixed-signal product manufactured using CMOS technology [116]. CMOS processes have typically parasitic bipolar structures. These are unintentional bipolar “devices” formed in the CMOS structures that might be causing ELDRS effects. The work reported rather enhanced response from the HDR; therefore the ELDRS effects in CMOS were minimal.

Dose rate sensitivity was reported for the RADFETs (Radiation-sensitive Field Effect Transistors) in various papers, including [117]. Nonetheless, this is not in conflict with the previous conclusions, because the RADFETs are not standard MOS products; they are based on a thick gate oxide to be made sensitive to radiation [18]. RADFETs are designed to be used for TID dosimetry, and this technology is discussed in detail in section 5.4.3.

3.6 Annealing

As soon as the irradiation is completed, the exposed devices start to undergo a period during which the post-irradiation effects (PIE) occur. The PIE could range from normal recovery to catastrophic failure [118]. A common PIE is the annealing, which is typically represented by a recovery of the device. For some particular applications, e.g. RADFET dosimeters, the term fading is used instead of annealing [18]. While the annealing/recovery is a required feature of space electronics, the fading of dosimeters is usually seen as a negative effect to be suppressed by its design (an ideal dosimeter should store the dose information as long as requested by the application).

Annealing is a very slow process at room temperature (hours to years, depending on the bias and also on the actual progress of the annealing) because the charge exchange between the oxide and semiconductor is very slow after the initially liberated mobile electron-hole pairs are gone [62]. Annealing can be accelerated by exposing devices to elevated temperatures.

Some devices can exhibit a continuous degradation during annealing (there is no recovery; the trend of a parametric degradation is the same as during the irradiation). This effect is known as “reverse annealing” [81]. The recovery of a device parameter during the annealing may also cause an overshoot of the original (pre-irradiation) value. Such a phenomenon is called “rebound”. The annealing can be a very complex problem with the limited accuracy of simulations. As a result, a catastrophic failure is sometimes found to happen later after irradiation of large complex ICs [18].

3.6.1 Annealing of MOS devices

In MOS devices, annealing is (among the temperature and bias conditions) dependant on the gate oxide thickness and other technological parameters [87].

Fig. 3.13 shows results of a TID experiment published by Winokur et al. [119]. Five CMOS 4007 inverters were irradiated under HDR conditions (5 rad(Si)/s) up to TID level of 15 krad(Si) and then left to anneal for 11 days. The bias conditions were kept constant during both irradiation and annealing periods: $V_{DD} = V_{GS} = +10$ V, which corresponds to +10 V across the n-channel gate oxide and 0 V on the p-channel gate oxide. Following irradiation, all V_T curves were observed to be linear with ln(t) greater than 10^6 s. The results for the n-channel devices showed a clear difference for the Fairchild device, which even exhibited the rebound effect. This principal difference (the Fairchild device versus the other devices) could be explained by the construction of the gate (Si-gate of the Fairchild device versus Al-gate of the other samples). The response of the p-channel transistors for all the inverters was similar across the p-channel devices. However, the measured V_T shift during the exposure was significantly lower than for the n-channel devices due to the 0 V gate bias. The reverse annealing phenomenon could be seen on the p-channel transistors, especially for the Fairchild device.

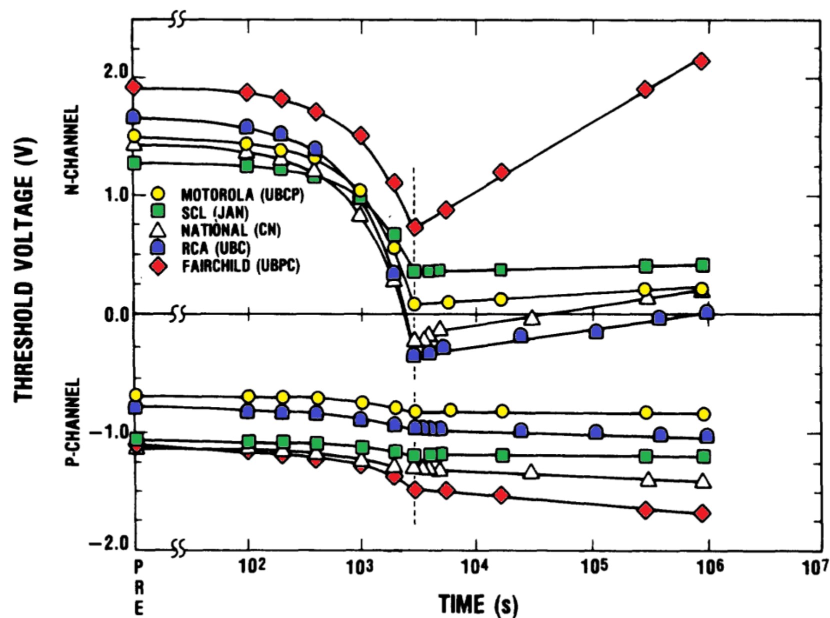

Fig. 3.13: Threshold voltage curves for n-channel and p-channel transistors of commercial 4007 inverters during 5 rad(Si)/s cobalt-60 irradiation as well as during the following isothermal annealing at room temperature. The dashed vertical line at 3000 s indicates the end of irradiation at TID level of 15 krad(Si). Chart adapted from [119].

The physical mechanisms that produce rebound effect were explained by research performed by Sandia National Laboratories [120]. The rebound effects can be observed only in the n-channel devices. As shown in Fig. 3.4, the effects of oxide trapped charge and interface trapped charge are counterparts for the n-channel devices. After exposure

of a positively biased device, electrons from the silicon tunnel into the oxide, and neutralise the oxide trapped charge producing an increase in the V_{T}, and thus they cause the rebound effect. The rebound effect was reported to be responsible for an unexpected failure of various NMOS based digital ICs including MCUs [121]. The payload for the NASA's Galileo mission had to be reworked due to this problem [18].

3.6.2 Annealing of bipolar devices

In general, the annealing of bipolar devices has a lower profile in literature than for the MOS devices [18]. For conventional BJT transistors and ICs, the TID-induced damage has been observed to recover gradually with time, although there were also cases where bipolar gain degraded further after irradiation – the devices exhibited reverse annealing [101]. In most cases, BJT gain anneals relatively slowly at room temperature, although leakage currents have been observed to recover rapidly after irradiation [103].

An illustrative example of annealing of an NPN transistor can be seen in Fig. 3.14. An experimental sample was irradiated up to 70 krad(Si) at various dose rates and later annealed at an elevated temperature of 100 °C for 168 hours (a week). The bias conditions were the same during both phases: all pins shorted to GND. As shown in the right picture in Fig. 3.14, the device did not fully recover.

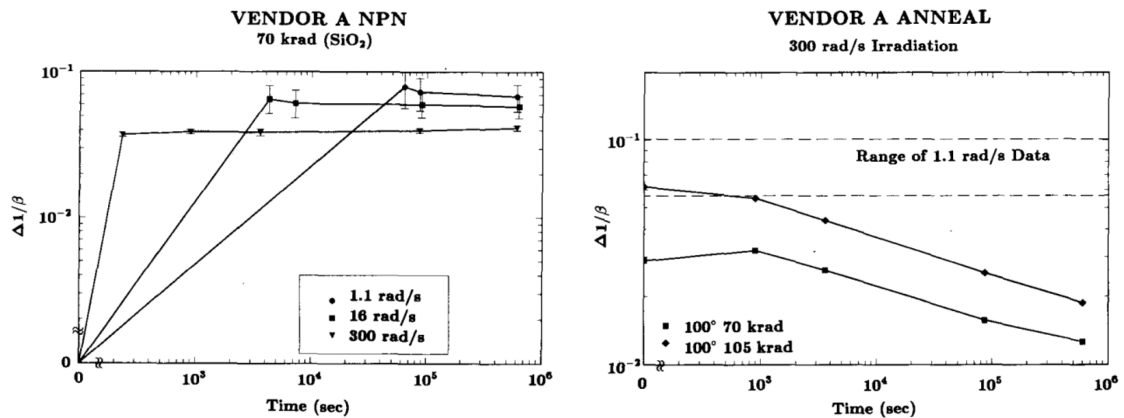

Fig. 3.14: Changes of $\Delta(1/h_{FE})$ during the irradiation (left chart) and the annealing (right picture) of an NPN transistor with the crystalline emitter. Charts adapted from [122].

Legacy data from the Mariner Jupiter/Saturn Program reported both the reverse annealing and rebound effects for an LM111 (bipolar voltage comparator) [123]. The LM111 input bias current, I_B, was measured to change from 20 nA to 400 nA with a TID level of 50 krad(Si) and to continue to degrade by another 400 nA during a 96 hour 150 °C elevated temperature annealing. This effect is believed to be caused by the time-dependent build-up of interface traps. This phenomenon occurs primarily in the substrate and lateral PNP transistors, such as those used for the input stage of the LM111. The input offset current, I_{OS}, shifted negatively during the irradiation phase. During the annealing period, the rebound effect was observed - the I_{OS} increased, overshooting its original value by 15 nA.

3.7 Bias sensitivity

The bias conditions during the TID test have an essential impact on the TID sensitivity of the devices [18]. There are two principal biased modes used in TID tests:

1. mission specific bias conditions
2. general bias conditions (part qualification tests)

For a TID test tailored to an individual space mission, the bias conditions are typically defined by the particular circuit (application) design. In the space industry, this approach is called "Test like You Fly" or TLYF and it provides the most objective results [124]. However, a typical spacecraft uses a power plan to save the battery power, and therefore many of the systems are regularly shut down. The timing of the particular power cycle can be planned before the mission, but it may change during the flight due to various reasons including the degradation/ageing of power sources (solar panels or RTGs) or failures of the systems (there would be more power for the functional systems). Thus the TLYF bias conditions should be dynamic during TID tests using cycling of the power to simulate the mission power plan.

To practically demonstrate the dynamic bias technique, a TID experiment was performed during which COTS digital thermometers (DS18B20) were irradiated using switched bias conditions with various duty cycles [125]. In total 25 devices (DUTs) were TID tested. The DUTs were biased with a voltage of 5 V and duty cycle from 1 % to 100 %. The duty cycle period was 5 min. The DUT temperature measurement error was obtained by comparing the DUT results with readings of a calibrated, radiation tolerant, temperature sensor. The results plotted in Fig. 3.15 show a clear dependence of the measurement error on the duty cycle.

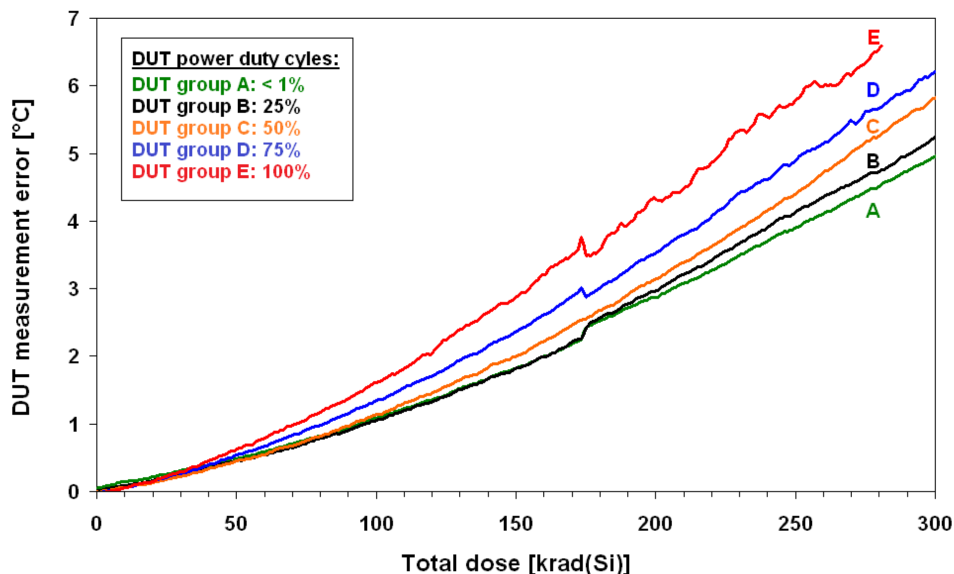

Fig. 3.15: TID-induced degradation of average measurement accuracy of DS18B20 digital thermometers. Each group of five DUTs was biased with a different duty cycle to demonstrate the bias sensitivity of TID-induced changes. Chart adapted from [125].

When a general (mission independent) TID test is required, the key challenge is to define the bias conditions that would cover a typical space mission. If it is not a research experiment, the goal of such a test is usually to qualify a part for space missions and add it to approved-parts databases. Among others, the following parameters need to be defined:

1. power supply voltage (bias voltage during TID)
2. decoupling
3. clock frequency (digital or mixed-signal devices)
4. feedback loops (amplifiers)
5. output loading
6. cooling (to avoid thermal annealing)

3.7.1 Bias sensitivity of MOS devices

The MOS technology exhibits a proportional bias dependence; the higher irradiation bias voltage V_I, the higher TID-induced degradation [18]. The applied electric field on the gate (and thus on the MOS oxide) strongly drives the charge transport and trapping in the irradiated MOS devices [30]. As defined in the equation (3.2), the ΔV_{ot} and ΔV_{it} are the key contributors to the gate threshold voltage shift ΔV_T. The chart in Fig. 3.16 shows the ΔV_T and the contributing ΔV_{ot} and ΔV_{it} for an irradiated n-channel MOS transistor as a function of electric field in oxide E_{OX}. The transistor had a hardened 45 nm SiO_2 gate oxide. The irradiation was performed with 10-keV X-ray source up 500 krad(SiO_2) [126].

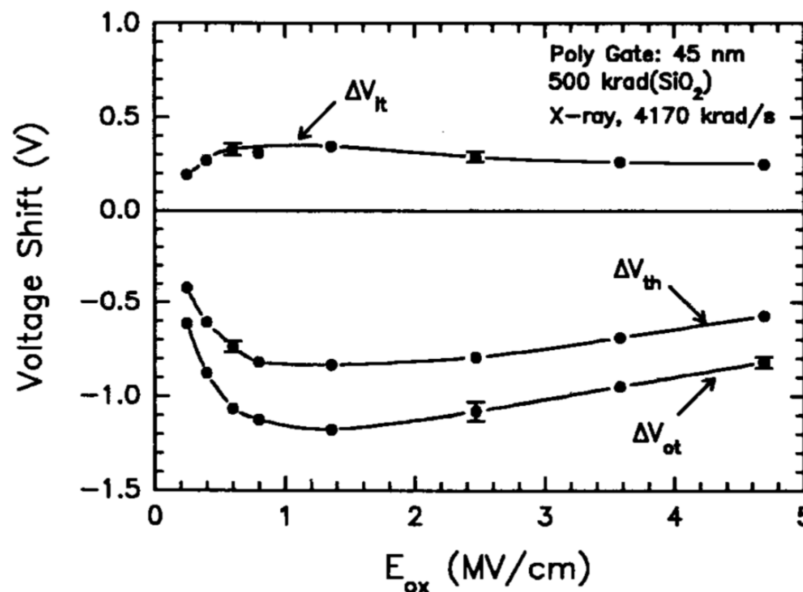

Fig. 3.16: Threshold voltage shifts ΔV_T due to oxide and interface-trap charge ΔV_{ot} and ΔV_{it} for an n-channel MOS transistor irradiated up to 500 krad(SiO2) with 10-keV X-rays at a dose rate of 4.2 krad(SiO2)/s at electric fields from 0.2 to 4.7 MV/cm. Chart adapted from [126].

Freeman and Holmes-Siedle developed a simplified linear model for predicting the radiation effects in MOS devices [127]. Using the model, the threshold voltage shift ΔV_T could be estimated using this formula:

$$\Delta V_{\mathrm{T}} = R \cdot A \cdot D, \tag{3.9}$$

where R contains the characteristic parameters for a given experiment (including the irradiation bias V_I), A is the probability that the hole will be trapped on passing through the passing sheet ("softness factor", determined by thermal processing of the oxide film [18]), and D is the dose. This model can be used, together with appropriate values R, to create idealised ΔV_T curves as a function of irradiation bias voltage V_I as shown in Fig. 3.17. These "growth" curves can be used by design engineers [127] for simple modelling of TID response of MOS devices including CMOS technology [18].

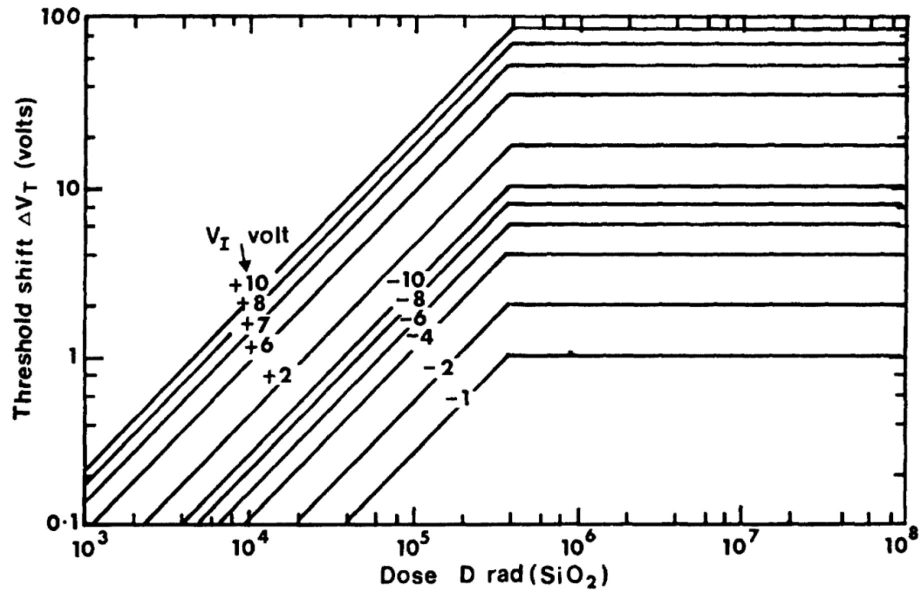

Fig. 3.17: Growth curves of gate threshold voltage shift ΔV_T as a function of irradiation voltage V_I. Both positive and negative values of V_I are plotted. Figure adapted from [127].

3.7.2 Bias sensitivity of bipolar devices

While the bias sensitivity of MOS transistors has been evaluated to be proportional to the biasing during the irradiation, the bias dependence of the BJTs is a rather more complicated problem not only due to the complexity of BJT geometries [101].

For the discrete BJTs, the following bias conditions are typically investigated:

1. collector-emitter bias dependence
2. emitter-base bias dependence
3. zero bias dependence

JPL has performed a set of TID tests of various transistor types, including the industry-standard type 2N2222A [101]. The HDR TID-induced degradation of the gain of 2N2222A plotted in Fig. 3.18 shows a strong collector-emitter bias dependence. Much greater degradation was observed at high irradiation bias voltage than for the low voltage. The h_{FE} was measured at constant $V_{CE} = 10$ V. At the low collector current (0.1 mA), the $\Delta(1/h_{FE})$ was approximately four times higher at $V_{CE} = 50$ V than at 10 V.

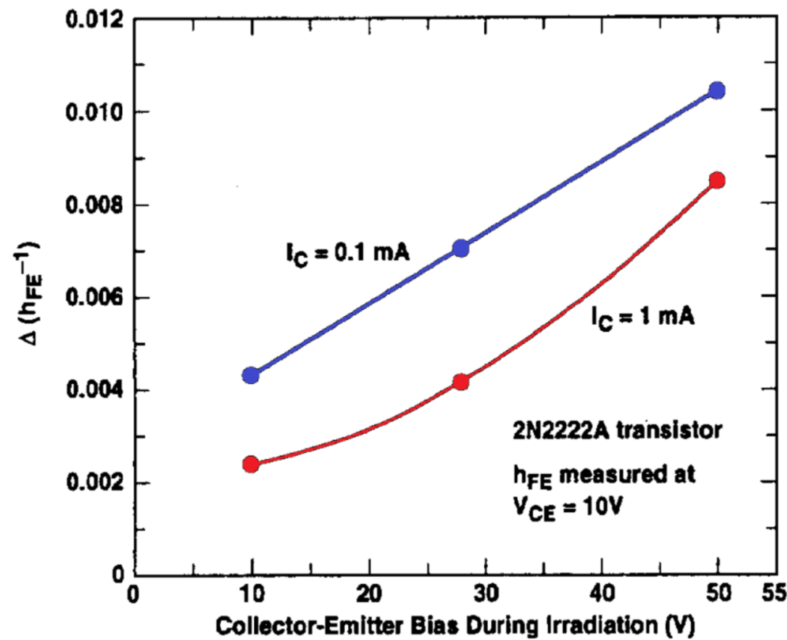

Fig. 3.18: Effect of collector-emitter irradiation bias on the TID-induced degradation of $\Delta(1/h_{FE})$ of a 2N2222A transistor. Plot adapted from [101].

For BJT integrated circuits, the bias dependence was investigated in combination with the dose rate sensitivity effects including the ELDRS [128]. Due to the complexity of this problem, these studies are typically attempting to identify only the worst case bias conditions. The worst case bias conditions are also one of the classical strategies for the bias conditions during the TID part acceptation tests. The test results in [128] suggest that for a single DUT, some parameters had worst case bias conditions with DUT unbiased, while some other parameters degraded the most at the highest supply voltage. This behaviour makes this problem even more complex and shows that the bias conditions during the TID testing should be as much tailored to the target application as possible.

One example is shown in Fig. 3.19 for the LT1185, a low dropout linear voltage regulator [129]. For high dose rate, there was only a little difference between biased and unbiased irradiation and biased irradiation was worst case. However, at low dose rate, the unbiased condition was significantly worse, even with a functional failure approximately at 30 krad(Si).

To conclude, for the bipolar integrated circuits, the testing at both biased and unbiased conditions is a key strategy for the best understanding of the TID-induced degradation of these devices.

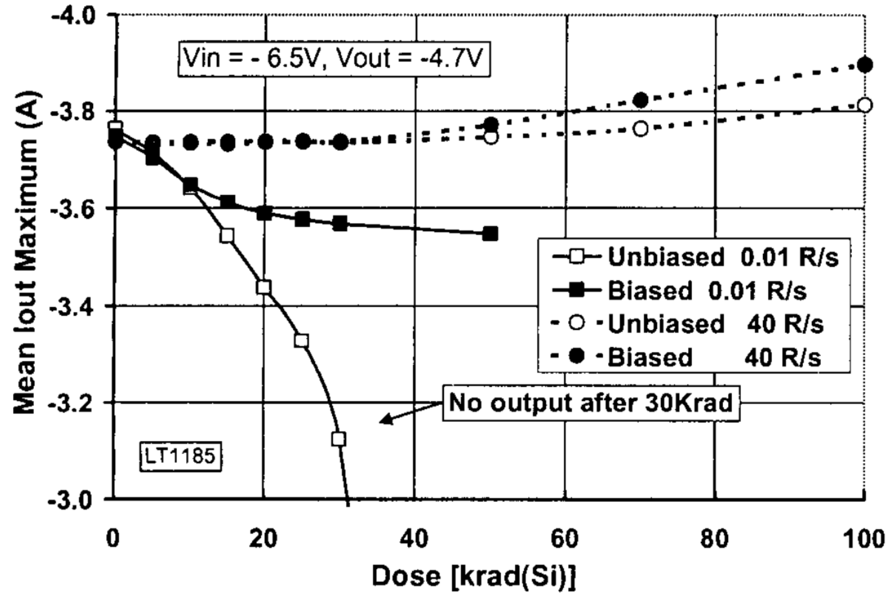

Fig. 3.19: The TID-induced degradation of the output current of an LT1185 linear low dropout voltage regulator measured at various bias and dose rate conditions. Chart adapted from [129].

3.8 Temperature effects in semiconductors

The first part of this section summarises the temperature dependence of the physical properties of the semiconductor materials [130]. The impact of temperature on the parameters of devices (MOS and bipolar transistors) is discussed in the second part.

3.8.1 Temperature dependence of the energy bandgap

The impact of temperature on the energy bandgap is a fundamental temperature-sensitive property of semiconductors. According to Varshni [131], the energy bandgap E_g could be expressed as a function of temperature T:

$$E_g(T) = E_{g0} - \frac{\alpha \cdot T^2}{T + \beta}, \tag{3.10}$$

where E_{g0} is the energy bandgap at absolute zero temperature ($T = 0$ K) for the given material and α, and β are material constants. A plot was created using this model and Varshni constants for the two major industry-used materials [132]. The resulting temperature curves are shown in Fig. 3.20 including the material constants used. At room temperature and under normal atmospheric pressure, the values of the band gap are $E_g = 1.12$ eV for Si and $E_g = 1.42$ eV for GaAs.

The Varshni model was published in 1967 and ever since then it has been extended by some other works, including O'Donnell et al. [133] and Cardona et al. [134].

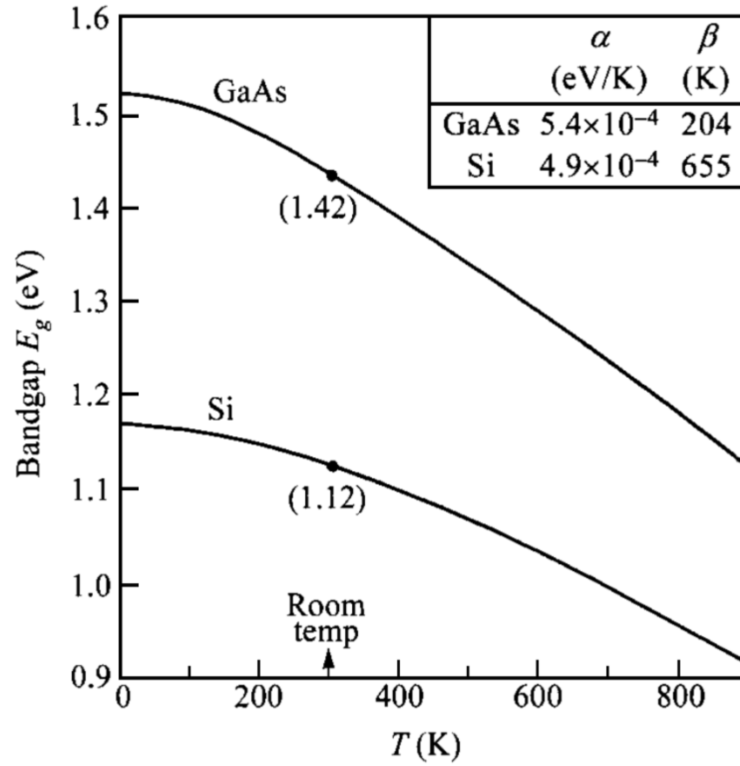

Fig. 3.20: The energy bandgap E_g as a function of temperature. The chart and table adapted from [132].

3.8.2 Temperature dependence of carrier density

The carrier densities have an impact on the electrical and thermal conductivity [135] and can be calculated using the following equations [132]:

$$n = N_C e^{\left(\frac{-E_C - E_F}{kT}\right)}, \quad (3.11)$$

$$p = N_V e^{\left(\frac{-E_F - E_V}{kT}\right)}, \quad (3.12)$$

where n is the electron density, p is the hole density, N_C is the density of states in the conduction band, N_V is the density of states in the valence band, E_C is the conduction band energy level, E_V is the valence band energy level, E_F is the Fermi energy level, k the Boltzmann constant and T is temperature.

3.8.3 Temperature dependence of carrier mobility

For non-polar semiconductors, such as Si and Ge, the presence of acoustic phonons (quasiparticles representing pressure (acoustic) waves in the lattice) and ionised impurities results in carrier scattering that significantly affects the mobility [132].

The temperature dependence of the mobility from interaction with acoustic phonon of the lattice, μ_l, can be approximately estimated by the following formula [132]:

$$\mu_l \propto \frac{1}{m_c^{*\frac{5}{2}} T^{\frac{3}{2}}}, \tag{3.13}$$

where m_c^* is the conductivity effective mass and T is the temperature. The mobility from ionised impurities μ_i can be expressed as a function of temperature [132]:

$$\mu_i \propto \frac{T^{\frac{3}{2}}}{N_I m^{*\frac{1}{2}}}, \tag{3.14}$$

where N_I is the ionised impurity density and m^* is the effective mass. The combined mobility, which includes these two components, can be calculated by the Matthiessen rule [132]:

$$\mu = \sqrt{\left(\frac{1}{\mu_l} + \frac{1}{\mu_i}\right)}, \tag{3.15}$$

Fig. 3.21 shows the temperature effect on mobility for n-type and p-type silicon samples [136]. For lower impurity concentrations, the mobility is limited by phonon scattering, and it decreases with temperature as predicted by (3.13).

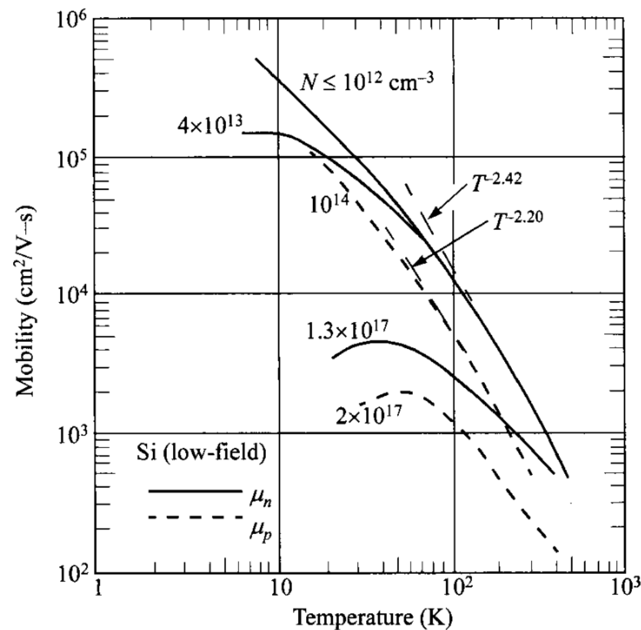

Fig. 3.21: Mobility of electrons and holes in Si as a function of temperature (after [136]).

3.8.4 Temperature dependence of MOS threshold voltage

The temperature dependence of the threshold voltage TC_{VT} is a complex effect and can be estimated using the following equation [137]:

$$TC_{\mathrm{VT}} = \frac{\delta V_{\mathrm{T}}}{\delta T} = \frac{\delta \Phi_{\mathrm{GS}}}{\delta T} + 2\frac{\delta \Phi_{\mathrm{F}}}{\delta T} + \frac{\gamma}{\sqrt{2\Phi_{\mathrm{F}}}}\frac{\delta \Phi_{\mathrm{F}}}{\delta T}, \tag{3.16}$$

where ϕ_{GS} is the gate-substrate contact potential, ϕ_{F} is the Fermi energy and γ is a body effect parameter. Filanovski at al. [137] suggested a TC_{VT} of -0.83 mV/K.

3.8.5 Temperature dependence of MOS transistors

The temperature dependence of carrier mobility and threshold voltage are the key contributors to the overall temperature sensitivity of MOS transistors [132], [137]. Their impact on a drain current I_{D} of an n-channel MOS transistor can be obtained from the following formula [138]:

$$I_{\mathrm{D}} = \frac{\mu_{\mathrm{n}} C_{\mathrm{ox}}}{2}\left(\frac{\mathrm{W}}{\mathrm{L}}\right)\left(V_{\mathrm{GS}} - V_{\mathrm{T}}\right)^2, \tag{3.17}$$

where μ_{n} is the electron mobility, C_{ox} is the oxide capacitance per area, W is channel width, L is channel length, and V_{GS} is gate voltage. An example of a simulated transconductance of an n-channel 0.35 μm CMOS device is plotted in Fig. 3.22 as a function of temperature [137]. The curves are plotted for temperature steps of 50 °C and are crossing in a point of zero *TC* (*ZTC*), sometimes called *MTC* (minimum *TC*).

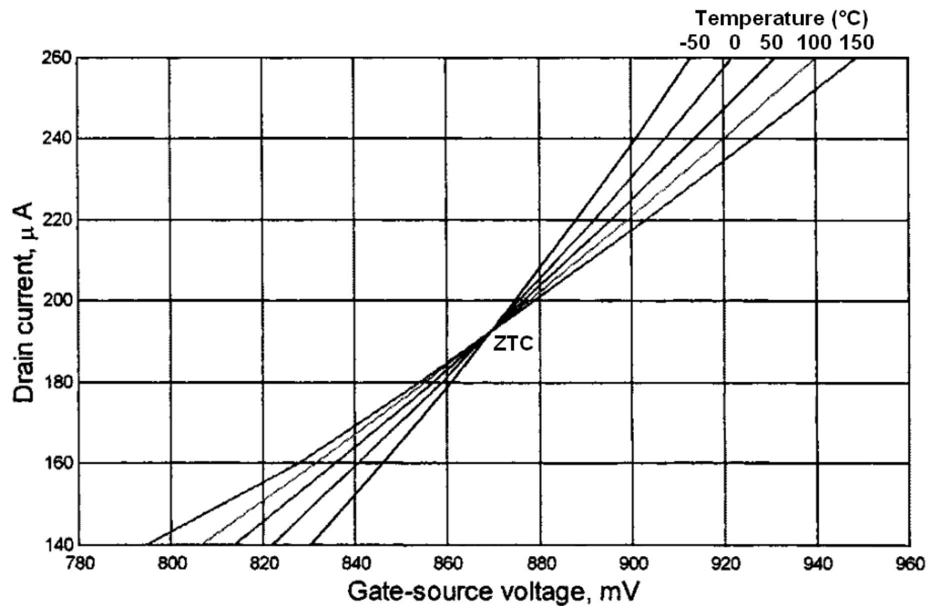

Fig. 3.22: Transconductance characteristics and *ZTC* point of a simulated CMOS n-channel device at various temperatures. The W/L = 50/2.5. Chart adapted from [137].

3.8.6 Temperature dependence of MOS leakage current

The subthreshold leakage current is exponentially dependent on temperature; it approximately doubles with every increase of temperature by 10 °C [139]. For low voltage MOS devices, the Shockley diode model can be used to calculate the subthreshold leakage current I_{sub} as follows [139]:

$$I_{\text{sub}} = I_0 \left[\mathrm{e}^{\left(\frac{\mathrm{q}V_{\text{DS}}}{\mathrm{k}T}\right)} - 1 \right], \tag{3.18}$$

where I_0 is the reverse saturation current, T is temperature, V_{DS} is the drain-source voltage, q is an electronic charge and k is Boltzmann's constant. The I_0 is also a function of temperature:

$$I_0 = \mathrm{A}T\mathrm{e}^{\left(\frac{-1.12\mathrm{q}}{2\mathrm{k}T}\right)}, \tag{3.19}$$

where A is a material constant. In comparison to I_{sub}, the temperature dependence of the gate leakage current was reported to be negligible [130].

3.8.7 Temperature dependence of base-emitter voltage of BJT

The collector current of a bipolar transistor is a function of base-emitter voltage as follows [140], [141]:

$$I_{\text{C}}(T) = I_{\text{s}}(T)\mathrm{e}^{\frac{\mathrm{q}V_{\text{BE}}}{\mathrm{k}T}}, \tag{3.20}$$

where I_C is the collector current, I_s is the saturation current in the forward-active region, T is temperature, V_{BE} is the base-emitter voltage, q is an electronic charge and k is Boltzmann's constant.

The derivation of the V_{BE} as a function of temperature is a rather complex process, and it has been modelled for the use in bandgap voltage references [141]. Although the V_{BE} temperature dependence is a parasitic effect, it has a variety of applications. Those include temperature sensors, for which a simplified equation can be used to determine the $V_{BE}(T)$ using the diode voltage model [132]:

$$V_{\text{BE}}(T) = \frac{E_{\text{g}}(0)}{\mathrm{q}} + \frac{\mathrm{k}T}{\mathrm{q}} \ln\left(\frac{I_C}{C_2 T^{C_3}}\right), \tag{3.21}$$

where $E_g(0)$ is the extrapolated energy bandgap for absolute zero temperature, I_C is the collector current, T is temperature, q is an electronic charge, k is Boltzmann's constant and C_2, C_3 are constants. Typical sensitivity of Si BJTs is 1 to 3 mV/°C [132].

3.8.8 Temperature dependence of gain of BJT

The current gain of bipolar transistors exhibits strong temperature dependence as demonstrated in Fig. 3.23, in which common-emitter current gain is plotted as a function of absolute temperature [142]. This parasitic effect can be explained by the lower effective intrinsic carrier concentration in the base than in the emitter [143]. This imbalance is caused by the high impurity concentration in the emitter, leading to a decrease of the bandgap E_g, as well as a change in the density of states [142].

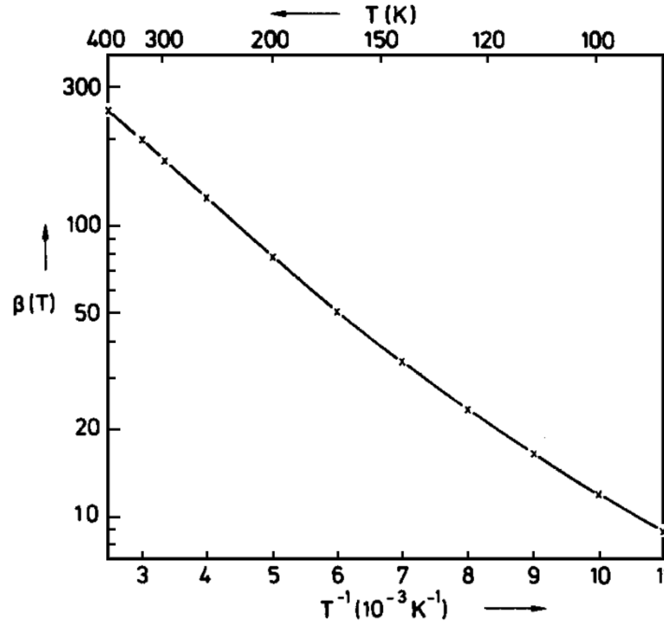

Fig. 3.23: Current gain as a function of the reciprocal temperature of an NPN bipolar transistor BC237A at I_C = 2 mA and V_{CE} = 2 V. Plot adapted from [142].

The current gain h_{FE} temperature dependence can be approximately calculated by the use of the following simplified equation [142]:

$$h_{FE}(T) = e^{\left(-\frac{\Delta E_g}{kT}\right)}, \tag{3.22}$$

where E_g the energy bandgap, T is temperature and k is Boltzmann's constant. The equation (3.22) can lead to poor calculations because this model ignores the contribution of minority carrier motilities in base and emitter, and assumes intrinsic carrier concentration at low impurity concentration in base [142].

3.9 The synergy between TID and temperature

The ambient temperature has a key impact on the TID-induced changes in electronic components [18]. Furthermore, the temperature of the payload aboard a spacecraft can vary significantly [144]. Therefore the synergy between TID and temperature could have a significant impact on the performance of space electronics.

There is a strong connection (synergy) between radiation effects and temperature, including the following effects:

1. irradiation temperature controls the TID-induced changes
2. temperature dependence of the post-irradiation annealing
3. TID-induced change of temperature effects in semiconductors and devices

These effects can be in fact combined; therefore the TID-induced change of temperature effects in semiconductors is also a function of the irradiation temperature. A similar situation is assumed for the annealing of this phenomenon.

3.9.1 Temperature dependence of TID-induced degradation of MOS

For the discrete MOS semiconductors, the influence of the irradiation temperature on the magnitude of the TID-induced changes can be explained on the silicon oxide level [18], [30], [145]. The hole trapping in the oxide is non-proportional to the temperature. The TID-induced electron transport still occurs efficiently at low temperatures, but the holes transport significantly slows down. The ΔV_{OT} contribution of the ΔV_T is also non-proportional to the temperature [145].

The dependence on time and irradiation temperature of hole transport in an irradiated SiO_2 is shown in Fig. 3.25 [146]. The test sample was an Al-gate MOS capacitor with 85 nm SiO_2 gate oxides irradiated to 60 krad(SiO_2) with 12 MeV electrons pulse at a dose rate of 1.5×10^{10} rad(SiO_2)/s. The shift in the flatband voltage ΔV_{FT} was plotted at irradiation temperatures ranged from 80 to 293 K.

The hole transport is very low at low temperatures, and therefore the space electronics working at cryogenic temperatures could be significantly more sensitive to radiation than if it operates at or near room temperature. An example of such conditions would be the astrophysical missions, during which the camera ICs (CCD, CMOS) are typically cooled down to cryogenic temperatures to suppress the dark currents.

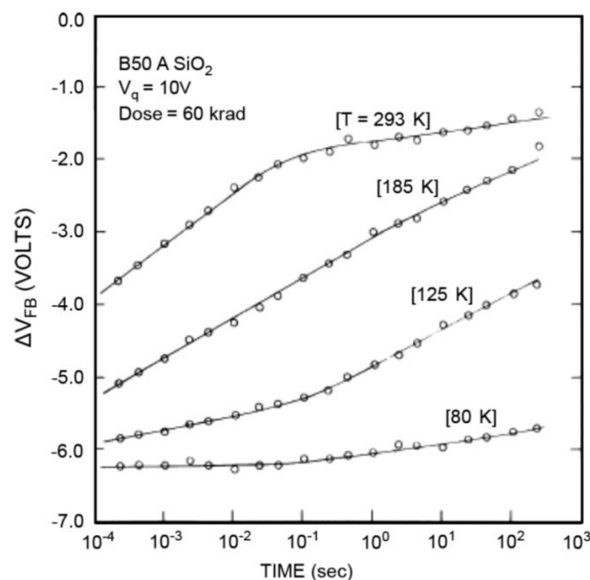

Fig. 3.24: The TID-induced shift in the flatband voltage ΔV_{FT} as a function of irradiation temperature and time after the pulse. Plot adapted from [146].

3.9.2 Temperature dependence of TID-induced degradation of BJT

For bipolar devices, the influence of the irradiation temperature has been investigated as a part of the dose rate sensitivity research, focused on accelerated testing of potential ELDRS [97], [100]. There was a hypothesis that an equivalent magnitude of enhanced degradation could be created by HDR irradiation at elevated temperature [147]. As discussed in section 3.5.2, it was suggested that if ELDRS is related to the space charge produced by slowly transporting holes, a higher degradation could also be induced if the hole transport is accelerated by an elevated temperature.

This effect was proved by experiments as shown in Fig. 3.25, which demonstrated that the temperature could have a significant impact on the TID-induced change of an NPN BJT [147]. However, the thermal enhancement had a limit; at higher temperatures, accelerated annealing overtook the enhancement produced by the reduced space charge [107]. The temperature dependence was a function of TID; as the TID level increased, the peak moved to lower irradiation temperatures.

The other physical explanations of ELDRS listed in the section 3.5.2 are also consistent with the proportional dependence of the TID-induced degradation on the irradiation temperature [97].

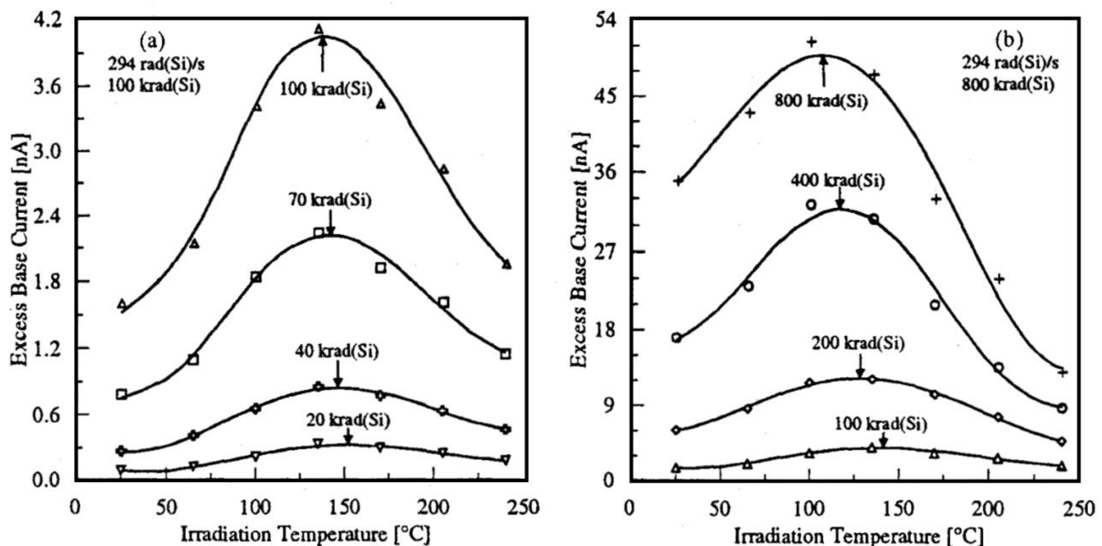

Fig. 3.25: Dependence of excess base current on irradiation temperature in an NPN test structure for (a) low and (b) high TID. Peak enhanced degradation was achieved at a temperature that was non-proportional to TID. Charts adapted from [147].

3.9.3 Thermal enhancement of annealing of MOS

The temperature dependence of the annealing of MOS devices was measured by a series of annealing experiments [148]. Fig. 3.26 shows an illustrative example of isochronal annealing curve of NXP 4069 CMOS inverter. The device was irradiated to TID level of 24 krad(Si) using cobalt-60 with a dose rate of 0.18 rad(Si)/s. The device was biased with $V_{GS} = 9$ V, and the irradiation was performed at room temperature. The majority of the TID-induced threshold voltage shift was considered to be contributed to the positive bulk oxide trapped charge.

The isochronal annealing was performed in a tunnel furnace with all pins of the device shorted together. The dwell time was 360 s, and the temperature steps were 20 K each. That corresponds to a heating rate of 5.5×10^{-2} K·s^{-1}. After every step, the device was quickly cooled down, and the measurements of ΔV_T were performed at room temperature. The plot in Fig. 3.26 shows a strong temperature dependence of the annealing of the normalised ΔV_T. The dwell time of six minutes was relatively short, which, in combination with the unbiased condition, explains the low annealing at the beginning of the staircase sweep of the temperature.

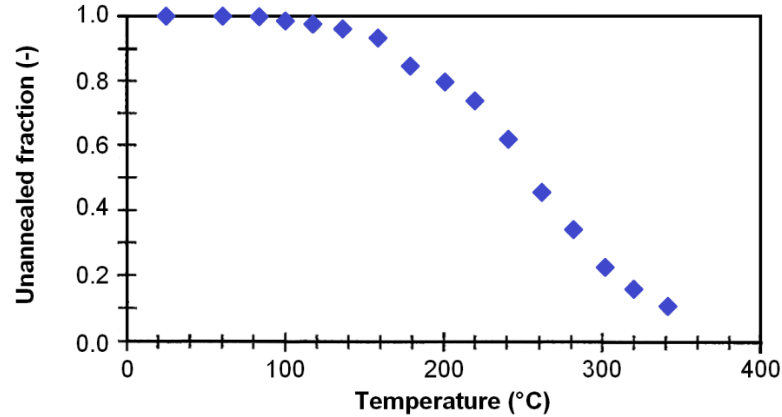

Fig. 3.26: Isochronal annealing curve of the NXP 4069 CMOS inverter. The TID level was 24 krad(Si), and the heating rate was 5.5×10^{-2} K·s^{-1}. Plot adapted from [148].

According to Holmes-Siedle [18], the exact mechanism of the thermal annealing has not been established yet, but there was a suggestion that the effect was potentially caused by injections of electrons into the silicon-oxide interface from the silicon.

3.9.4 TID-induced changes in carrier mobility

As discussed in section 3.8.5, the carrier mobility has a strong impact on the temperature dependence of MOS devices as well as of the bipolar components as demonstrated in section 3.8.8. Therefore the TID-induce change of carrier mobility could play a vital role in the TID-induced changes of temperature sensitivity of space electronics.

Work by Stojadinovič et al. [149] summarised the results of various experiments and modelling efforts. Stojadinovič's team proposed an empirical model for the degradation of mobility μ due to the effects of the interfacial charges employing a linear combination of interface trapped charge and oxide trapped charge [149], [150]:

$$\frac{\mu}{\mu_0} = \frac{1}{1 + \alpha_{it}\Delta N_{it} + \alpha_{ot}\Delta N_{ot}}, \tag{3.23}$$

where μ_0 is the pre-irradiation mobility, ΔN_{it} and ΔN_{ot} are the TID-induced changes in densities of interface trapped charge and oxide trapped charge, respectively. The constants were proposed to be $\alpha_{it} = 1.135 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 0.0645 \times 10^{-12}$ cm^2.

To validate this model, a TID experiment was performed [149]. N-channel power VDMOSFETs (gate oxide thickness 100 nm) were exposed to TID-level up to 100 krad(Si) using a cobalt-60 source and dose rate of 4 rad(Si)/hr. Gate bias voltage was 9 V. TID-induced densities of both oxide and interface trapped charge is plotted in the left chart in Fig. 3.27. Using the ΔN_{it} and ΔN_{ot} and formula (3.23) the TID-induced change of carrier mobility was calculated. Using the α_{it} and α_{ot} suggested by [149], a very good fitting of experimental data could be achieved (curve m2 shown in the right plot of Fig. 3.27). The model m1 was based on older α_{it} and α_{ot} constants after [151].

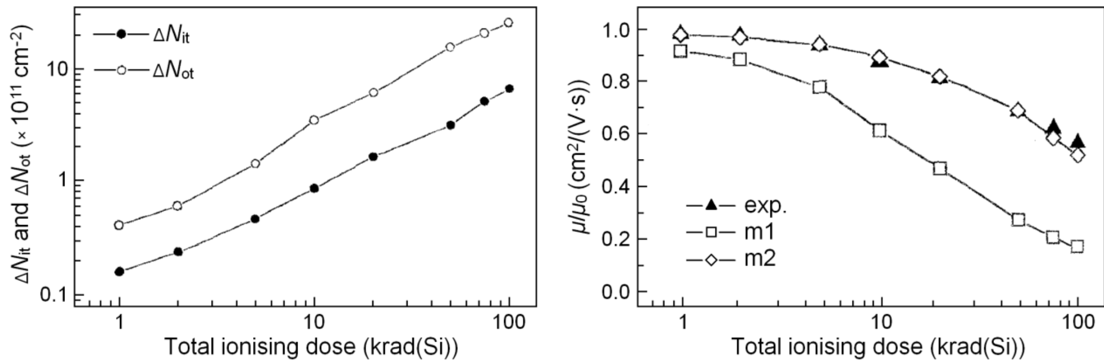

Fig. 3.27: TID-induced changes in the densities of interface and oxide trapped charges (left) and carrier mobility (right) in VDMOSFET device. Charts adapted from [149].

This experiment proved that TID could cause significant degradation of the carrier mobility, leading to a non-trivial change of temperature sensitivity of electronics.

3.9.5 TID-induced changes in temperature dependence of devices

The TID-induced changes of the temperature sensitivity of space components have not been evaluated extensively. Therefore the amount of available literature was limited to a few publications.

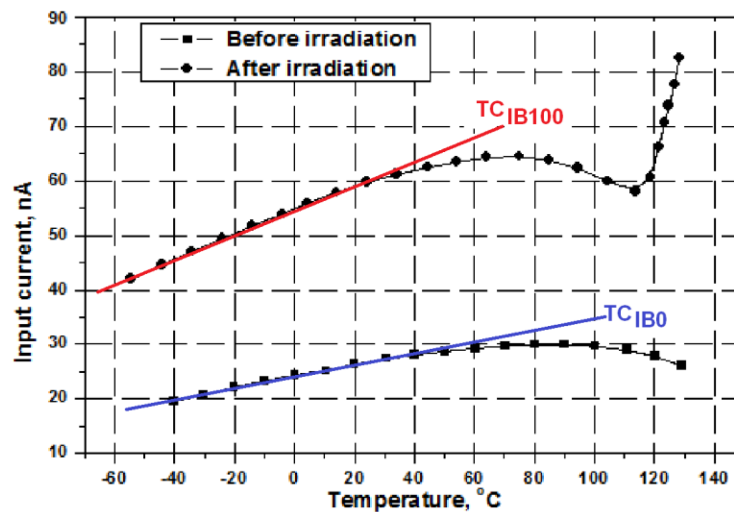

Fig. 3.28: Temperature dependence of input bias current of LM124 before and after 100 krad(Si) irradiation. Plot adapted from [152].

The influence of TID irradiation on the temperature dependence of an operational amplifier (OPA) was measured [152]. A bipolar LM124 OPA was irradiated to TID of 100 krad(Si) using X-ray with a dose rate of 60 rad(Si)/s. The temperature dependency of the input bias current I_B was measured before and after the irradiation as shown in Fig. 3.28. The published curves were analysed to obtain the temperature coefficient of the input bias current using the following formula:

$$TC_{IB} = \frac{\Delta I_B}{\Delta T}, \quad (3.24)$$

where TC_{IB} is the temperature coefficient of the input bias current and T is the temperature of the sample. The values of ΔI_B and ΔT were obtained by linear fitting of the measured curves in Fig. 3.28. From those lines, the values of pre-irradiation TC_{IB0} and post-irradiation TC_{IB100} were calculated. Finally, the radiation-induced change in the TC_{IB} can be expressed as:

$$\Delta TC_{IB} = \frac{TC_{IB100}}{TC_{IB0}} \cdot 100, \quad (3.25)$$

where ΔTC_{IB} represents the TID-induced change of the TC_{IB}. Using the formula (3.25), the resulting ΔTC_{IB} was 230 %, demonstrating that the TID level of 100 krad(Si) caused the TC_{IB} to increase by more than a factor of two. Noticeable is also the change in the shape of the curve of the irradiated sample possibly caused by the instantaneous annealing during the *TC* measurements.

3.10 Other synergistic effects

The conventional TID testing of space electronics is focused on the radiation-induced effects on the electrical parameters on electronic components and systems. However, the radiation can also have an impact on some the other (usually parasitic) properties of electronics and vice versa. The following effects are discussed in this section as they are relevant to this work:

1. mechanical stress – the influence of mechanical stress on TID effects
2. EMC/EMI – the impact of TID on the electromagnetic compatibility

Among these synergistic effects, there is also a synergy between the TID and SEE effects as discussed in section 3.2. The impact of TID on SEE (TID enhanced SEE) has been reported in various works as summarised in [153]. However, the SEE has no impact on the TID (in the real space environment the TID is, in fact, a product of the accumulation of particle strikes, which may lead to SEE).

3.10.1 Mechanical stress versus total ionising dose

The sensitivity to mechanical stress is a typical problem for high accuracy analogue/mixed-signal electronics, including voltage references. Therefore this effect

must be taken into account especially during the mechanical design of the instruments and the related PCB design phase (component placement) [140]. The space instrumentation can be mechanically stressed during most of the space mission phases, especially during the launch and the active part of the mission (e.g. due to thermal expansion during the crossing of the planet's terminator) [154].

The influence of the TID on the sensitivity of electronics to mechanical stress has not been published. However, a series of experiments have been performed to measure the influence of mechanical stress on the TID-induced degradation of both bipolar and MOS devices.

A correlation between mechanical stress and hydrogen-related effects on TID-induced damage in MOS capacitor was reported in [155]. The work demonstrated that a compressive stress effect could reduce the TID-induced degradation of a MOS structure.

The LM111 and LM139 analogue comparators produced by National Semiconductor were irradiated to measure the effects of mechanical stress on bipolar ICs [156]. The DUTs were irradiated at HDR and LDR conditions with mechanical stress applied. The paper reports a strong enhancement of the LM111 intrinsic ELDRS effect possibly caused by the device passivation (as discussed in section 3.5.2). Nonetheless, the second device, the LM139, was reported to be both ELDRS-free and immune to the mechanical stress. The LM139 is a device with no passivation layer.

3.10.2 The influence of total ionising dose on EMC

The impact of the electromagnetic compatibility (EMC) on the performance of a high-resolution data acquisition could be essential [28]. There is a variety of sources of electromagnetic noise onboard a spacecraft, including telemetry transmitters, switched power converters and possibly also electrical propulsion systems [157]. The potential dependence of the electromagnetic susceptibility (or EMI) on the TID has been found as an emerging problem, and a small number of research papers have been published lately.

Significant TID-induced enhancement on the electromagnetic susceptibility of a discrete bipolar transistor has been measured; a COTS bipolar transistor was exposed to a TID level of 150 krad(Si), and a significant change in susceptibility to RF band from 100 MHz to 1.5 GHz was observed [158].

Another team focused on the potential influence of TID on EMI of field-programmable gate arrays (FPGAs) and published a series of papers. They demonstrated a noticeable degradation of electromagnetic susceptibility as well an increased SEU rate in a COTS FPGA and a synergy between these phenomena [159].

4 TRADITIONAL RADIATION HARDNESS ASSURANCE AND TESTING

The concept of traditional RHA and testing is discussed in this chapter together with both European and American test standards. The published test results for key DAQ components (voltage references and ADCs) are also summarised in this chapter.

4.1 Industry-standard radiation hardness assurance

The RHA covers a broad spectrum of activities undertaken to ensure that the performance of space electronics is within the design specifications after exposure to the space radiation environment [160]. ESA defined the RHA in the ECSS-Q-ST-60-15C standard [161] in order to standardise the RHA process among all agency's projects. The American RHA standard MIL-HDBK-814 was created by the US Department of Defence [162].

According to ESA, the RHA shall deal with environment definition, part selection, part testing, spacecraft layout, radiation tolerant design, mission/system/subsystems requirements and mitigation techniques [160]. The RHA typically requires multiple iterations to achieve an optimal, radiation hardened design as shown in Fig. 4.1.

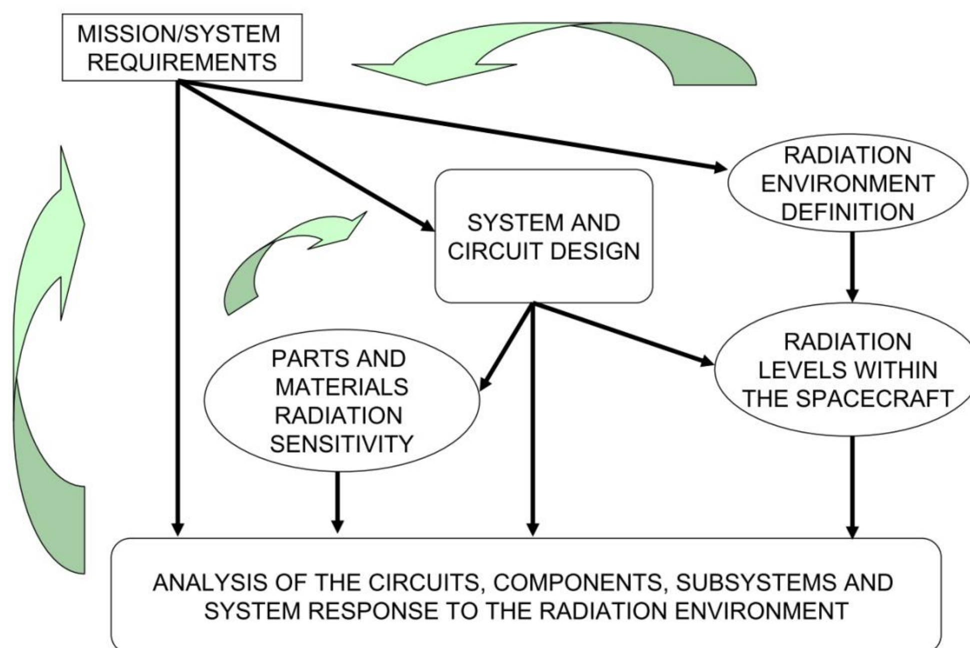

Fig. 4.1: Overview of RHA process as defined by ESA. Figure adapted from [160].

The flowchart of the TID analysis is shown in Fig. 4.2. The inputs to the analysis are the mission requirements from which two key data flows are derived:

1. The functional and parametric requirements on the analysed component
2. The mission TID level and component sensitivity to TID

The next step is the circuit-level worst-case analysis investigating the impact of the TID-induced change on the required performance of the circuit. The TID analysis continues in a loop until the design requirements are satisfied. The TID test results (represented by the PART TID SENSITIVITY block in the flowchart) are commonly processed by one of the following ways [161], [162]:

1. Worst-case value of the parameter
2. A statistical approach using one side tolerance limits

In both cases, the test data are used for worst-case design analysis, and therefore the standard RHA coverage is limited to the maximum possible impact of the radiation on the design, not on the real impact of the radiation on the performance of the design during the mission.

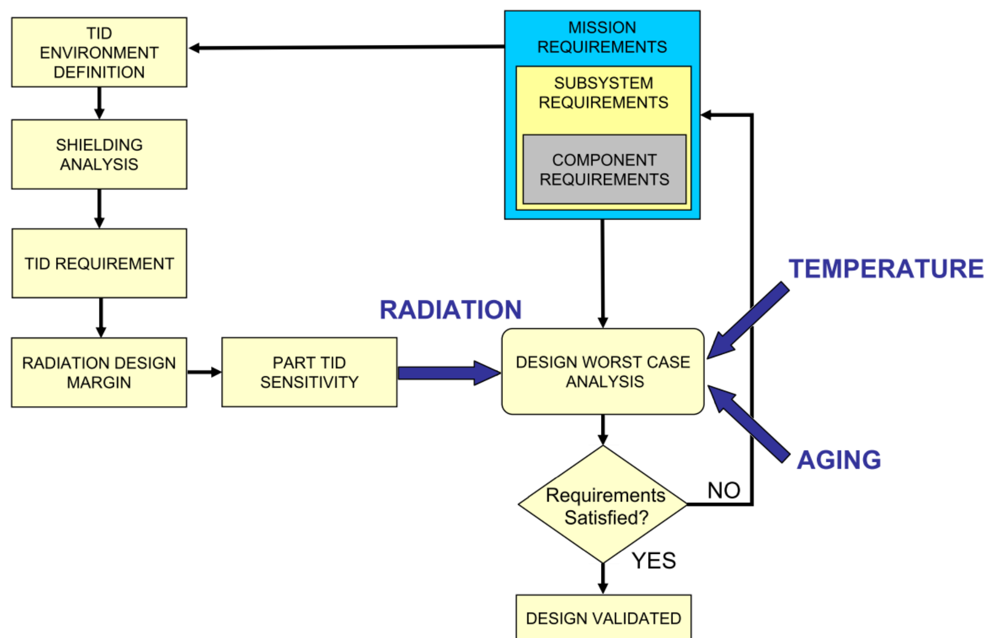

Fig. 4.2: TID analysis flow as defined by ESA. Chart adapted from [160].

4.2 Industry-standard total ionising dose test

During a traditional TID test, the device under test (DUT) is irradiated, and changes in its parameters are measured. The TID tests for space applications are performed by standardised test methods, as defined in European 22900 [163] and American MIL-STD 883 [164] standards. There are two main methods by which DUT parameters are measured:

1. Standard bench test (SBT) – the device is exposed for a period of time and, once a certain total dose is reached, a post-irradiation measurement is performed in an electronics lab. Once the measurement is done, the irradiation continues until the next total dose step.
2. In-situ test method (ISTM) – measurements are performed continuously during irradiation, i.e. it does not have to be interrupted.

4.2.1 Standard bench TID test

The main advantage of this approach is that the test system (either manual or automated) is located in a non-radiation area and there are no limits to the use of classical laboratory bench instruments. The labour demand is relatively low at the test system design phase, but an operator is required to perform the test exactly at the time when a particular total dose step is reached. This is sometimes a challenge, especially if the facility is shared with other jobs and there are random downtime periods caused by interruptions for these. It is also important to mention that the operators are typically trained only to execute the tests; hence the risk of a human error is present [165].

The number of dose steps is typically limited to around ten, so the number of measurements during the whole test campaign is also limited to this number. The annealing of parameter values is usually measured only before and after the DUT being placed in a temperature chamber (in the case of accelerated annealing). The resulting set of data allows the radiation engineer to perform only a limited analysis. It could be extremely complicated to perform any advanced statistical analysis using such a small amount of data.

The following chart (Fig. 4.3) shows results from TID test of a COTS 12-bit AD converter AD574AJN [166], which was performed during the early (training) phase of the PhD research using SBT. In total six irradiation steps were applied. It can be seen that a significant increase in ADC measurement error can be expected due to the TID-induced degradation of the voltage reference. The result after the first irradiation step is already more than 1 LSB, which is a considerable value compared to the other converter errors as defined in [166]. Thus, it would have been beneficial to have more measurements taken, especially at low total doses.

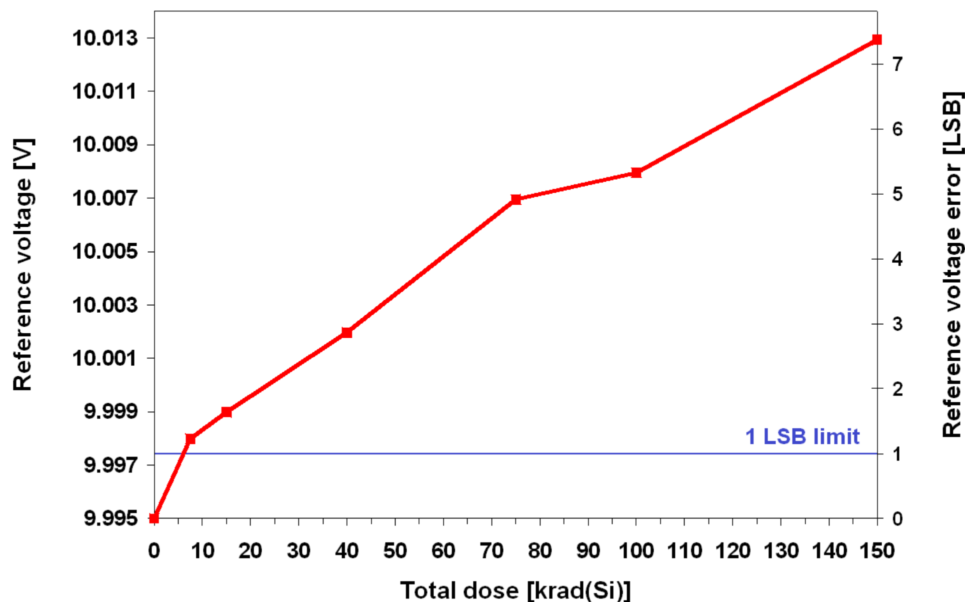

Fig. 4.3: AD574 voltage reference output versus total dose. The calculated equivalent ADC error induced by the reference voltage is shown on the secondary Y axis. The dose rate was 36 rad(Si)/hr up to 15 krad(Si) and 180 rad(Si)/hr for the rest of the test. The DUT was irradiated unbiased, and all power lines were grounded.

Another significant problem is the interruption of irradiation which needs to be controlled to a minimum ([163] and [164] specify a maximum of two hours). The immediate or short-term annealing during these interruptions can significantly influence the accuracy of test results, and the number of parameters measured must be limited so that the tests can be performed within the available time. This can be stressful for the operator, especially when a typical manual test on multiple DUTs is performed, potentially leading to a significant risk of measurement error and/or DUT damage.

The problem of immediate annealing can be demonstrated when an ISTM experiment is performed, and the irradiation is interrupted. During long-term irradiation, a set of a precision voltage references LT1021DCS8-10 [167] was exposed, and ISTM was used to measure a TID-induced degradation of the output voltage of these devices using a high-precision digital multimeter (type DMM 4050 [168]). The experiment was designed to prove that the ISTM concept is suitable for a TID test on such precision analogue devices. The duration of the experiment was more than six months, and there were multiple short interrupts during the test as the radiation source was shared with other jobs. Fig. 4.4 shows a detailed record of such a gap in irradiation, during which the immediate annealing appeared (the original negative trend immediately changed to a positive trend caused by the annealing). It is clear that such behaviour could be expected during the SBT and therefore the immediate annealing may cause significant measurement errors. The standards [163] and [164] also do not specify the sequencing of the testing of DUTs, hence should the bench test of each DUT take significant time (minutes), the annealing will obviously cause a significant device-to-device difference.

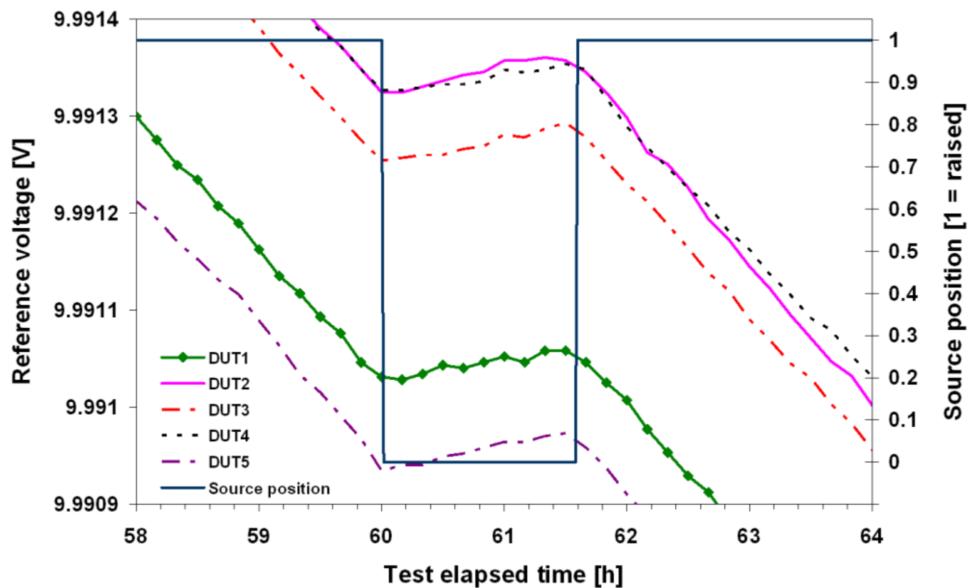

Fig. 4.4: A detailed record of irradiation interrupt showing that the DUT output voltage reacted immediately. The time resolution of the source position was one second. The DUT voltage sampling period was ten minutes. Raising the source took approximately fifteen seconds.

4.2.2 Radiation sources for the TID testing

The cobalt-60 isotope is used as a standard source for space TID tests due to its good repeatability, relatively low cost and easy handling. The decay of the source can be precisely calculated and so test results can be compensated for this type of systematic error. Although a majority of the industry-standard tests have been performed using the cobalt-60 sources, some experimental works were also based on x-ray and caesium-137 irradiations [114], [165]. While the MIL-883 standard assumes only use of cobalt-60 source [164], the European standard 22900 also allows an electron accelerator beam irradiation to be applied [163].

The use of cobalt-60 is justified more by the practicality and economics of the testing than on the technical grounds [165]. As discussed in chapter 3.1, the TID-induced degradation of space electronics is primarily caused by the high-energy protons and electrons. Hoverer, the cobalt-60 sources are producing gamma photons with an average energy of 1.25 MeV [169]. Various analyses were published to discuss the limits of the cobalt-60 testing [165]. The data from irradiations using proton and electron accelerators were compared with the results of experiments using cobalt-60 and X-ray irradiation facilities [170], [171], [172]. According to these papers, cobalt-60 radiation sources may overestimate the total dose degradation for proton-rich environments, but the irradiation more closely matches the stopping power and charge yield of 1-MeV electrons than X-ray irradiation. Thus, to simulate TID degradation in electron-rich environments, Co-60 gamma sources will still be the optimum radiation source for device qualification. Hoverer, these conclusions are based on a relatively small amount of data using a limited amount of MOS samples. Therefore this problem shall be addressed by future works [165].

4.2.3 Dosimetry and sample placement during the TID test

The final result of any hardness assurance test is no more accurate than the accuracy of the dosimetry used for the radiation source analysis [173]. The European standard 22900 specifies that the cobalt-60 source shall be calibrated to 5 % or better [163] in accordance with the ESCC Basic Specification No. 21500 [174], which defines calibration and traceability requirements. The MIL-883 standard does not directly define the accuracy requirements of the dosimetry system. However, it links various related ASTM standards, including ASTM E 1249 [175] and ASTM E 1250 [176].

The placement of the samples is another important factor; the influence of dose enhancement effects caused by low-energy and scattered radiation must be minimised. Therefore, both the 22900 and MIL-883 standards require the samples to be placed in a lead/aluminium (Pb/Al) container. A minimum of 1.5 mm Pb, surrounding an inner shield of at least 0.7 mm Al, is required. The dosimeter shall be placed in the irradiation container in the position of the samples [164].

4.3 TID tests of voltage references

This chapter outlines the most common types of voltage references, discusses the test methods used for the measuring of their parameters and summarises the published results of TID testing of voltage references for various applications.

4.3.1 Voltage references types and topologies

The designs of modern voltage references (VREF) range from relatively simple diode-based circuits up to sophisticated bandgap systems [140]. The following VREF circuit topologies are commonly used for practical applications [177]:

- Shunt voltage references (SHVRs) are two-terminal devices with similar functionality to Zener diodes (Fig. 4.5). The SHVRs are typically used in low precision applications such as voltage regulators and limiters. They offer a wide range of input voltage and can be used as negative reference voltage sources.
- Series voltage references (SEVRs) are typically much higher accuracy and lower noise than shunt mode references. However, the supply voltage is limited to the absolute maximum rating of the device. The majority of them have three terminals (Fig. 4.5), although the most precise types use independent sense lines to suppress voltage drops on the output voltage PCB trace.

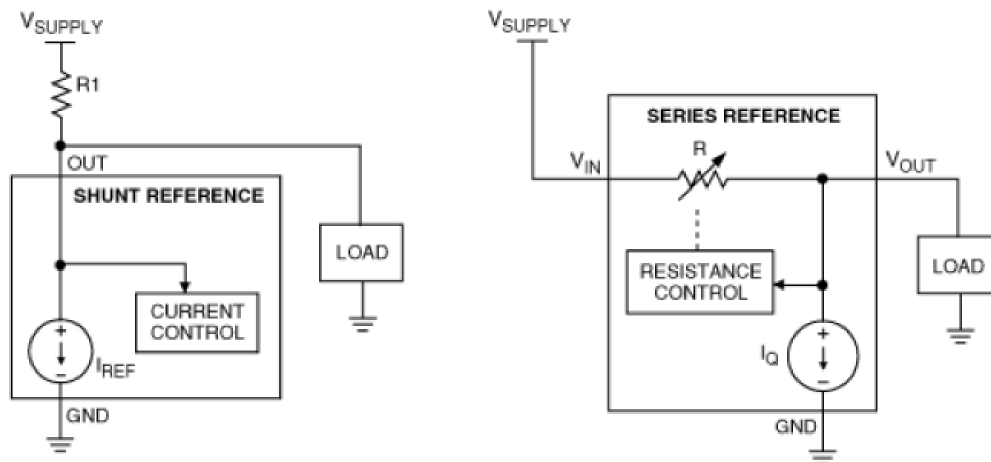

Fig. 4.5: Block diagrams of the two traditional VREF topologies. The shunt reference is shown on the left picture and the right picture represents the three-terminal series voltage reference. Pictures adapted from [177].

A variety of design techniques have been developed to suppress the key VREF challenges: the impact of changes in ambient temperature and input voltage on the reference voltage. The design techniques include [178], [179]:

- Buried Zener diode voltage references
- Bandgap voltage references
- XFET voltage references

The temperature-compensated Zener diode circuit has been the industry-standard technology used in high-precision calibration systems, as well as secondary voltage standards for national metrological institutes [180]. The Zener diode based reference standards have excellent temperature stability, and therefore they are used in new designs despite the existence of more modern technologies [181]. The buried Zener diode voltage reference (BZRs) technology was developed to address the noise and stability issues of the surface junctions of VREF integrated circuits. These problems were caused by surface contamination and crystal imperfections [182]. Despite its potentially out-of-date technology, BZRs are still in the product portfolio of the manufacturers of precision devices. However, the output voltage range starts at 5 V; hence the BZRs are typically used for higher reference voltage designs. The most stable voltage reference device on the COTS market, the LTZ1000 [183], illustrates the legacy of this technology - the LTZ1000 was introduced in 1987, and it still does not seem to have a direct competitor [179].

Nowadays, the bandgap voltage references (BGRs) are the most common voltage references used in various IC designs. Originally, the BGR was developed to provide a reference voltage for monolithic voltage regulators, in which the power transistor is placed on the same chip [179]. With further technological development, they became more stable and accurate, and thus appropriate as reference sources for ADCs. The key enabler of this development was the application of high-order curvature-correction techniques allowing excellent temperature independence [184]. The BGRs are practically the only technology used for internal VREF in high-resolution ADCs. The most important disadvantage of the voltage-mode BGRs is that the minimal reference voltage is about 1.2 V (the silicon bandgap energy), so these VREFs are not suitable for ultra-low voltage applications. However, this issue has been a research topic for a variety of teams [185].

A third and relatively new category of IC voltage reference technology is based on the properties of junction field effect (JFET) transistors. It was developed by Analog Devices to circumvent the limitations of the other VREF types [179]. Analogous to the bandgap reference for bipolar transistors, the reference operates a pair of JFETs with different pinch-off voltages, and amplifies the differential output to produce a stable reference voltage [186]. One of the two JFETs uses extra ion implantation. Therefore the XFET acronym has been used (eXtra implantation junction Field Effect Transistor). Nowadays, Analog Devices offers a variety of monolithic VREF devices using the XFET technology, but it has not been integrated as an internal reference of ADCs yet. The comparison of the performance of the XFET versus the other types is in Tab. 4.1.

Tab. 4.1: Characteristics of VREF architectures, table adapted from [186].

VREF type	**Supply volt/curr.**	**Noise**	***TC* drift and Long-Term Stability**	**Hysteresis**
Buried Zener	> 5 V, high	Low	Good	Fair
Bandgap	< 5 V, high	High	Fair	Fair
XFET	< 5 V, low	Low	Excellent	Low

4.3.2 Voltage reference parameters

The voltage references are tested for various parameters as can be seen in the datasheets. However, these tests are not standardised. Therefore the values of some parameters may not be directly comparable due to the limited compatibility of test methods used by various manufacturers. This chapter lists the key parameters related to the measurement uncertainty of the DAQ systems [140], [179].

The initial accuracy (V_{OERR}) defines the deviation of the output voltage from the nominal value at powering up of the VREF. This systematic error can be compensated by the system calibration procedure before the launch. Typically, it is measured at ambient temperature T_A = 25 °C with no load applied and expressed in mV or %.

The temperature drift (tempco, TC_{Vo}), specified in ppm/°C, is the dominant error source from a VREF in the DAQ systems. For a linear temperature dependence, the TC_{Vo} can be obtained from the following formula [179]:

$$TC_{Vo} = \left(\frac{V_{max} - V_{min}}{V_{nom} \cdot (T_{max} - T_{min})} \right) \cdot 10^6 , \quad (4.1)$$

where V_{max} is an output voltage measured at temperature T_{max} and V_{min} is an output voltage measured at temperature T_{min}. The V_{nom} is the nominal output voltage. The two most commonly used methods for definition of the TC_{Vo} by the manufactures are shown in Fig. 4.6. The Box method simply uses the minimum and maximum limits of the output voltage and temperature range of the device to determine the TC_{Vo}. In contrast, the more precise Butterfly method is defining the TC_{Vo} for the whole temperature range of the device. This method is also called a Bow-tie in some literature, and it is frequently used with very-high-precision voltage references.

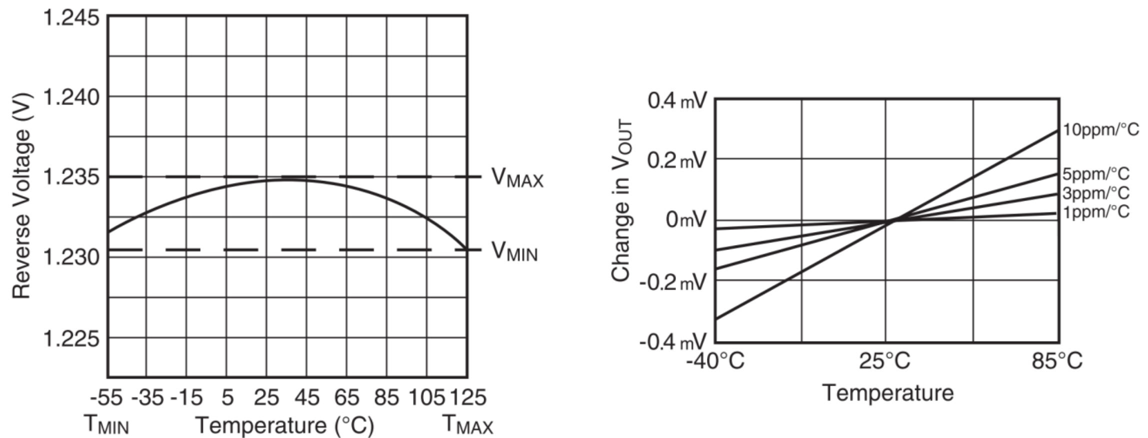

Fig. 4.6: Traditional methods for defining the temperature drift of VREFs. The Box method is shown in the left chart, and the right chart displays a TC_{Vo} of a precision device using the Butterfly method. Pictures adapted from [182].

An analysis was made to demonstrate the impact of the ambient temperature span on the DAQ system measurement accuracy, due to the VREF temperature drift. The chart in Fig. 4.7 shows the maximum allowed temperature span to maintain 0.5 LSB (Least Significant Bit) measurement errors in a DAQ system using VREF of three different temperature drifts. It is clear from the chart that accuracy better than 16 bits is achievable only by limiting the temperature span and using a VREF with TC_{V_o} lower than 1 ppm/°C.

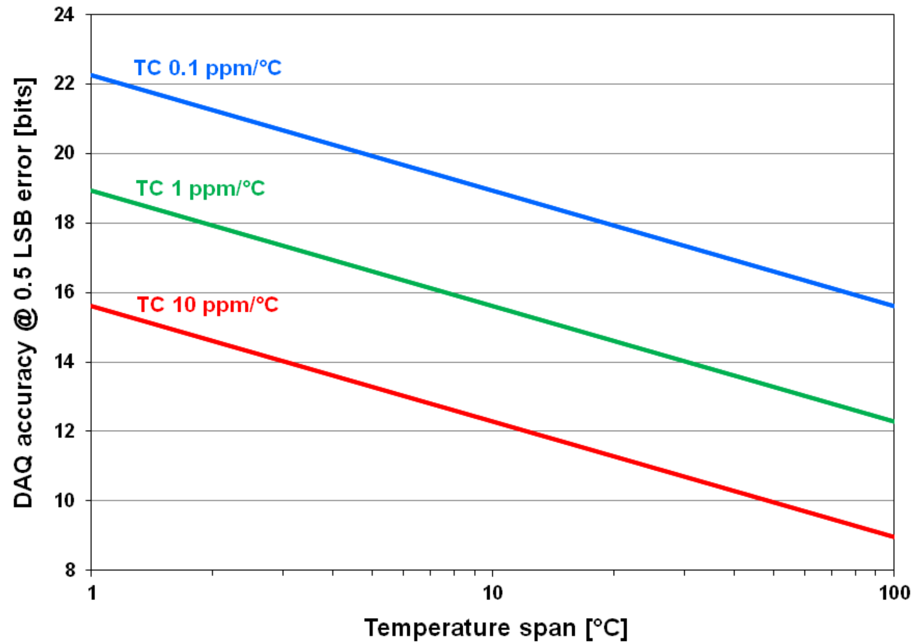

Fig. 4.7: The impact of the temperature span on the full-scale accuracy of a DAQ system caused by the TC_{V_o} of the voltage reference. The curves are plotted for three values of VREF TC_{V_o} to maintain measurement error of 0.5 LSB.

According to Intersil, the thermal hysteresis specifies the maximum change in output voltage at T_A after the voltage reference is cycled between two extreme temperatures [182]. Analog Devices also provides full temperature range value [186]. The other manufacturers test at a lower temperature window; Linear Technology provides data for $T_A \pm 25$ °C [167], and Texas Instruments only provides data for a $T_A + 25$ °C test [187]. Hence it is complicated to cross-compare these values. The thermal hysteresis is specified in ppm. It is believed to be caused by mechanical stresses in the die of the VREF IC, and therefore it is a function of the package design and the speed of the temperature sweep during the thermal testing [140], [179].

Another important parameter is the long-term drift. It represents the stability of the reference voltage over a long period. It is specified in ppm/1000 hours, and it is measured under the same conditions as the initial accuracy. It was demonstrated that this error decreases over a long period [188] and therefore various burn-in processes were used to accelerate this process [179]. In principle, the long-term drift is indistinguishable from the TID-induced shift of the VREF during the TID test.

Line regulation is the ability of the VREF to suppress the impact of variation of the input voltage (it is also called power supply rejection). It is typically specified in ppm/V or µV/V, and it is measured in a pulsed mode [179]. The line regulation degrades with increasing frequency. Therefore the decoupling has a crucial impact on the line regulation [186].

Load regulation is the ability of the VREF circuit to provide a stable output voltage within a range of output (load) currents. It is specified in ppm/mA or µV/mA. In some literature, it is also specified as output impedance [179]. Load regulation is linked to the layout of the PCB, and for high precision systems, the Kelvin connection (four-wires) shall be used to suppress the voltage drops across the PCB traces [186].

4.3.3 Voltage references TID test results

This section discusses the available data from published TID tests of various voltage references. The focus was on the highest-precision devices and advanced test TID methods. The most relevant results are listed in Tab. 4.2.

The test data suggested that there were no true rad-hard VREF devices; in fact, the rad-hard parts suffered a similar level of TID-induced shift of the output voltage (ΔV_O) as the COTS devices. However, comparing of these results could be misleading, as they were not obtained under the identical irradiation conditions. The literature also showed that the VREF devices could degrade from the start of the irradiation.

The total dose resolution is a significant limitation of the published results. The majority of the reports contained SBT data. Hence there were typically only up to ten total dose steps published. The ISTM data were found in two papers. There was only one work containing annealing data within the discussed papers [189].

The lowest observed degradation was published in 1997 for the LTZ1000, the industry-best VREF device [190]. The unprecedented radiation hardness of this device was based on two factors: the simplicity of the device, and the integrated heater. Therefore it is possible that the ultra-low TID-induced change was caused by the irradiation at elevated temperature (however the paper does not specify the die temperature used during the irradiation).

The literature was also intensively searched for data of TID-induced changes of the temperature drift TC_{Vo}. The only related information was found in the datasheet of the LM4050QML [191], which extends the paper [192] by specifying a strong TID sensitivity of the TC_{Vo}. It changes from 10 ppm/°C to 387 ppm/°C (at TID level of 100 krad(Si)).

Another limitation of the existing TID data can be illustrated on the results for the LM185 devices. There was an order of magnitude difference between TID-induced degradation reported by Abare et al. [189] and Hatch [193]. This phenomenon clearly shows the limitations of the testing of COTS devices and the influence of the radiation test conditions (such as the type of source, bias conditions).

The listed papers were not the only source of TID data for high precision voltage references. TID data could also be found in various radiation test compendia papers, although these results are typically limited to a single plot [128] or even pass/fail statements as could be found in NASA's papers [194] and CERN's [195].

Tab. 4.2: Summary of results and key parameters of selected TID tests of voltage references.

Year	**Source**	**Part numbers**	**VREF type**	**Technology**	**Test method & purpose**	**Target dose [krad(Si)] & source**	**Dose rate [krad(Si)/hr]**	**Dose steps**	**Test results: TID-induced trends, or at a target dose**	**Notes**
1997	[190]	LTZ1000 and 6 more	Various	Si COTS Si rad-hard	SBT research	100 Co-60, protons	0.018, 180	10 - 20	LTZ1000 ΔV_O ~ 0.01 % others ΔV_O ~ 1 %	The only data for LTZ1000
2000	[196]	HS-584RH	BGR	Poly–DI rad-hard	SBT research	1000 Co-60	0.29 - 180	10	ΔV_O ~ 1 % Δ Line/load reg < 0.1 %	Bonded wafer harder
2001	[197]	RH1009 HS1009	SHVR	Si rad-hard	SBT qualification	1000 Co-60	1.5, 180	5	ΔV_O ~ 0.5 % (unbiased)	Strong bias sensitivity
2002	[189]	LM185	BGR SHVR	Si COTS	SBT research	50 Co-60	0.03, 497	6	ΔV_O ~ 10 % (25 krad) ΔV_O ~ 35 % (50 krad)	High dose rate sensitivity
2005	[198]	ADR291, 420, 430	XFET	Si COTS	ISTM research	45 neutrons	~4.5	-	ADR291 failed 420, 430 ΔV_O ~ 2.5 %	The only data for XFET
2007	[199]	IS1009RH	SHVR	Si rad-hard	SBT qualification	100 Co-60	0.036	4	ΔV_O ~ 0.2 %	No bias data
2009	[200]	LM4132, 28, 20	BGR (EEPROM)	Si COTS	SBT research	18, 32, 55 Co-60	0.36	5 - 10	ΔV_O ~ 0.2 %	No bias data
2010	[192]	LM4050QML	SHVR	Si rad-hard	SBT qualification	150 Co-60	0.036, 547	4	ΔV_O ~ 1.2 % (biased)	Minor bias sensitivity
2011	[193]	LM185	BGR SHVR	Si COTS	ISTM research	25 Cs-137	0.04 - 1.5	-	ΔV_O ~ 0.4 % (unbiased) ΔV_O ~ 1 % (biased)	Elevated temp. data
2013	[201]	-	BGR	DTMOS SOI rad-hard	SBT research	300 Co-60	209	5	ΔV_O ~ 0.5 % (best IC) ΔV_O ~ 13 % (worst IC)	No bias data
2014	[202]	-	BGR	SiGe HBT rad-hard	SBT research	100 Co-60	0.036, 180	10	ΔV_O ~ 2.6 % (LDR) ΔV_O ~ 2.8 % (HDR)	Low dose rate sensitivity

4.4 TID tests of A/D converters

4.4.1 High-resolution A/D converters

Over the decades, a number of various ADC architectures were developed. However, the majority of modern high-resolution (better than 16 bits) ADCs are based on two architectures: the SAR (Successive Approximation Register) and the ΔΣ (delta-sigma) converters [203]. The ADC families, based on these architectures, in fact, have partially overlapping performance as shown in Fig. 4.8.

The SAR is a Nyquist-rate ADC; it operates at the minimum sampling frequency necessary to acquire all the information about the full input bandwidth. Therefore the sampling rate could be high [204]. The SAR converter performs a search on the input signal using a comparator and DAC. The search routine uses an interval-halving (binary) technique and continues in a loop until the LSB is determined [205]. The SAR converters can reach 20 bits resolution and sampling rates of MSPS [206].

The ΔΣ ADC is a key technology for the modern high-resolution converters. The ADC consists of ΔΣ modulator and a digital filter [205]. The role of the modulator is to suppress the quantisation noise at low frequencies, where the input signal is expected, and leave it at higher frequencies (noise shaping). The digital filter at the output of the modulator acts as a low pass filter and will cut off all high-frequency signals including the quantisation noise [203]. The digital filters in ΔΣ ADCs typically offer various frequency responses, including the sinc^n characteristics, which has a notch response. Such a filter can effectively reject the line frequency when adjusted at it [207]. By employing high-order ΔΣ modulators and advanced programmable digital filters, these ADCs can reach a resolution of 32 bits [206]. Although the effective resolution of such ultra-high resolution converters is lower than 32 bits, they allow designing of DAQ systems with an unprecedented resolution reaching the of a few ppb (parts per billion).

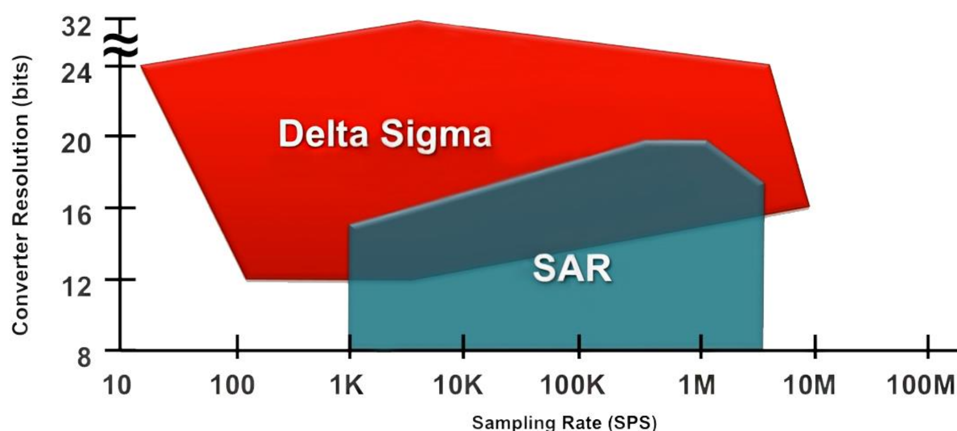

Fig. 4.8: Performance of the high-resolution ADCs (Texas Instruments data from 2015). Picture adapted from [206].

4.4.2 A/D converters test parameters

In contrast to the voltage references, the testing of the ADCs is partially standardised. The methods of ADC testing are defined by standard IEEE 1241 [208]. The IEEE 1057 specifies the testing of Digitizing Waveform Recorders [209]. Typically, ADC tests cover two principal groups of parameters and test methods [37]:

- Static parameters include various attributes of the ADC transfer characteristics and are crucial for the evaluation of the ADC accuracy (DC errors) and the resulting MU of the DAQ system.
- Dynamic parameters, or AC characteristics, are defining the noise and resolution performance of the ADC. The dynamic testing is a complex process which requires sophisticated RF equipment [210]. In comparison to the static parameters, its influence on the MU of the DAQ system is minor.

A response of an ideal ADC to the input voltage can be represented by a staircase function, which is commonly called transfer function (characteristics) [37]. Fig. 4.9 a) illustrates the transfer function of an ideal N-bit ADC, where N is the resolution of the ADC (number of digitised bits). For linear converters, the full-scale (*FS*) input range is segmented into 2^{N} equally sized bins (code bins) of nominal width Q [211]:

$$Q = \frac{FS}{2^{\mathrm{N}}} = \frac{V_{\max} - V_{\min}}{2^{\mathrm{N}}}, \tag{4.2}$$

where $V_{\max}$ is a maximum input voltage and $V_{\min}$ is a minimum input voltage respectively. Q is also frequently referred to as 1 LSB (a least-significant bit). The LSB size is typically expressed in volts.

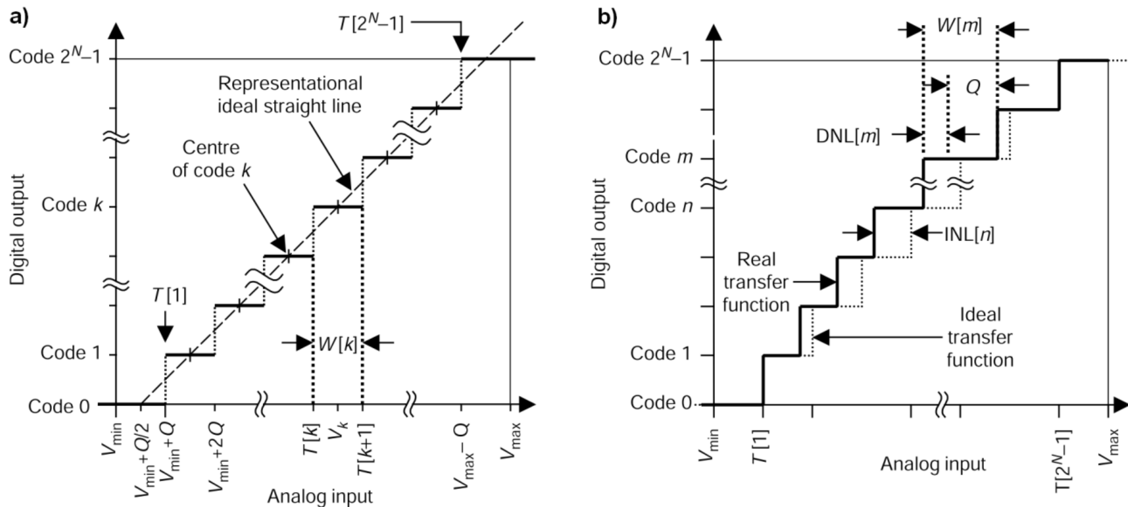

Fig. 4.9: Transfer functions of an ADC. The chart a) represents the transfer function of an ideal N-bit ADC and chart b) shows terminal-based DNL and INL in ADC transfer function. Charts adapted from [211].

The staircase transfer function can be approximated by a straight line using linear regression. As can be seen in Fig. 4.9 a), the ideal straight line starts (ADC output code = 0) at $V_{in} = V_{min} + Q/2$ and ends (ADC reports *FS*) at $V_{in} = V_{max} - Q/2$. However, the transfer function of real ADC deviates from this definition as a result of the offset error ε_{os} and gain error ε_G. The effect of the offset error in ADCs is defined as a uniform lateral displacement of the transfer function and is expressed in volts:

$$\varepsilon_{os} = T_m[1] - (V_{min} + Q), \tag{4.3}$$

where $T_m[1]$ is the measured ADC input voltage at which the output code transits from 0 to 1. The deviation from ideal gain is defined as a difference in the transfer function's slope after offset compensation and is typically expressed in ppm:

$$\varepsilon_G = \left(\frac{G_m - G_{id}}{G_{id}}\right) \cdot 10^6 = \left(\frac{T_m[1] - T_m[2^N - 1]}{V_{max} - V_{min} - 2Q} - 1\right) \cdot 10^6, \tag{4.4}$$

where G_{id} is the ideal gain, G_m is the measured gain, and $T_m[2^N-1]$ is the measured ADC input voltage at which the output code transits from (2^N-2) to (2^N-1).

In real ADCs, the transfer function is not perfectly linear. Therefore the term non-linearity was introduced [37]. The impacts of the non-linear behaviour of a real ADC on its transfer function are illustrated in Fig. 4.9 b). The *DNL* (Differential Non-Linearity) is defined as a difference of the gain and offset corrected real code widths from the ideal value. The *DNL* values are expressed in ppm for the codes 1 to (2^N-2) [211]:

$$DNL[\mathrm{k}] = \frac{(W_m[k] - Q)}{Q} \cdot 10^6, \tag{4.5}$$

where k is the code, and $W_m[k]$ is the measured width of code bin k corrected for the gain and offset. The *DNL* value of -10^6 indicates a missing quantisation step. The term "missing code" is typically used for this type of error. Modern ADCs are frequently specified as "no missing code" devices [37].

Another non-linearity error is termed as integral non-linearity (*INL*). It is defined as the distance of the code centres in the transfer function from the ideal line (Fig. 4.9 b)). The *INL* is typically given in ppm and can be calculated using the formula:

$$INL[\mathrm{k}] = \frac{(T_m[k] - T_{id}[k])}{Q} \cdot 10^6, \tag{4.6}$$

where $T_m[k]$ is the measured ADC input voltage at which the output code transits from (k - 1) to k and $T_{id}[k]$ is the ideal value of the same measure. Both *DNL* and *INL* are typically fully characterised by the ADC manufactures (*DNL* and *INL* plots can be found in datasheets), or their maximum values are defined [210].

4.4.3 A/D converters TID test results

This section discusses the published results of TID testing of high-resolution ADCs. The most relevant data are summarised in Tab. 4.3.

Hirex performed TID tests of three COTS types of 16-bit ADCs for ESA in 2004. These tests covered most of the ADC attributes, including static parameters (measured using a histogram analysis) and dynamic parameters (using FFT analysis of the signal from 18-bit AWG). The results showed that the AD7677 was strongly sensitive to the bias conditions (presence of an AC signal at the analogue and clock inputs) [212]. The AD9260 was practically immune to TID [213]. Finally, the ADS8402 had a strong TID-induced degradation of most of its parameters (it is unclear if the internal VREF had any impact on these results). This work demonstrated the broad spectrum of possible responses of ADCs to TID as all the parts were tested under identical conditions.

Only a few published ADC tests were performed in-situ (ISTM). A Russian paper [214] demonstrated a successful ISTM test of a rather obsolete dual-slope integrating (DSI) ADC. Austrian Academy of Science reported an ISTM test of a ΔΣ ADC for the ROSETTA mission [215], during which the dynamic test method was used. The results were inconclusive, possibly due to radiation effects on the secondary hardware on the irradiation PCB and cabling. However, the same team published later results of successful tests of lower resolution SAR ADCs using identical test system [216]. An ISTM test of 24-bit ΔΣ ADC was reported by Mikkola et al. [217]. Unfortunately, there were no detailed ADC data published in his work. Finally, a research team from CERN mentioned a limited ISTM TID test of a SAR ADC in their paper [56].

Among the ISTM papers discussed ([215], [217]), only one additional work related to high-resolution ADCs was found [218]. This Indian paper reported TID results of various types of ADCs including a 24-bit ΔΣ ADC. The authors claimed problems with their test system (poor resolution). A detailed review of the published data showed that the reported effects could be artefacts of the failures of the test system. A very high dose rate was used since the target application of this research was the nuclear power industry. Therefore some of the TID-induced degradations could be a product of dose rate effects.

Two TID reports of rad-hard ADCs were also studied. Maxwell reported results of qualification tests of three types of hardened ADCs [50]. These devices were based on COTS chips. Most of the tested parameters drifted linearly with the TID, and strong bias sensitivity was observed. This report also discussed the importance of the extreme quality of the test system and the influence of the reference voltage on the results, especially the linearity. An ultra-high dose rate test of a pipeline 16-bit ADC was published by Aeroflex [219]. This advanced space product showed a low response to TID, although the ADC part of the device was not entirely immune. The internal VREF source suffered a strong TID-induced degradation.

This literature review demonstrated a lack of high-precision TID data for ADCs with a resolution above 16 bits. Most of the published ISTM tests had a variety of limits due to the poor quality and reliability of the measurements. It is also important to mention that the rad-hard parts could still suffer a non-trivial TID-induced degradation despite their excellent immunity to SEEs and latch-ups.

Tab. 4.3: Summary of results and key parameters of selected TID tests of A/D converters.

Year	**Source**	**Part numbers**	**ADC type resolution [bits]**	**Technology**	**Test method & purpose**	**Target dose [krad(Si)] & source**	**Dose rate [krad(Si)/hr]**	**Dose steps**	**Test results: TID-induced trends, or at a target dose**	**Notes**
1998	[214]	ICL7107 PV2	DSI 12	COTS Si	ISTM research	100 Co-60, X-ray	Not published	-	All param. out of spec, *G* was the most sensitive	No bias data
1999	[215]	CS5508	ΔΣ 20	COTS Si	ISTM qualification	20 - 30 Co-60	0.73 - 4.6	~100	ADCs failed at target dose ΔI_{CC} ~ 200 %	STD, S/N inconclusive
2003	[50]	5016RP 7805ALPRP 7809LPRP	SAR 16	rad-hard Si (from COTS)	SBT qualification	20 - 30 Co-60	0.036, 0.36	6 - 8	~Linear shift with TID, strong bias sensitivity dose rate sensitivity	OPA causing INL/DNL? ATE issues?
2004	[212]	AD7677AST	SAR 16	COTS Si	SBT qualification	51 Co-60	0.36	5	Static biased out of spec Dynamic biased OK	external VREF
2004	[213]	AD9260AS	Pipelined ΔΣ, 16	COTS Si	SBT qualification	51 Co-60	0.36	5	All param. within spec No trends with TID	external VREF
2004	[220]	ADS8402	SAR 16	COTS Si	SBT qualification	51 Co-60	0.36	5	Out of spec at 19 krad (both bias conditions)	internal VREF
2005	[218]	AD7705 ADS1210	ΔΣ 16, 20	COTS Si	SBT research	16, 300 Co-60	64.8	3 - 5	out of spec at ~6 krad, failure at 16 krad (7705) and ~40 krad for 1210	Poor measurements of INL/DNL
2007	[217]	MSC1211	ΔΣ 24	COTS Si	ISTM research	20 - 30 Co-60	9.24	-	Failures at 20 to 30 krad I_{DD} steady up to 10 krad	Only I_{DD} reported
2012	[219]	UT16AD40P	Pipeline 16	rad-hard Si	SBT qualification	2000 Co-60	626.4 (Very high!)	12	ADC minor shifts VREF strong shift	Triple-Well CMOS process
2013	[56]	Not published	SAR 16	COTS Si	ISTM research	28 protons	Not published	-	VREF shift of ~7 mV	Dynamic test

5 RADIATION TESTING FOR THE NEWSPACE ERA

This chapter provides an overview of the challenges and opportunities of the emerging NewSpace industry and the applications of the COTS technology in space. It also gives a discussion of the proposed advanced test methods for both ground and space radiation testing. The chapter concludes with an outline of the novel Life Mission Measurement Uncertainty model. This model was designed to be demonstrated in the in-orbit experiment.

Fig. 5.1: The launch of the SpaceX Falcon Heavy rocket opens up deep space to the NewSpace industry. Picture after [221].

5.1 NewSpace technology

Alongside with the promising rise of the private space-launch industry (Fig. 5.1), the key element of the NewSpace revolution was the rapid development and manufacturing of affordable satellites. Although the motivation for this effort was purely economic, the low-cost spacecraft were not originally developed by private companies, but by the universities.

One of the teams, pioneering the NewSpace technology, was at the University of Surrey, UK. The UoSAT-l was a first Surrey's experimental microsatellite, which was successfully launched in 1981 [222]. The success of the UoSAT missions led to the establishment of a spin-out company SSTL (Surrey Satellite Technology Ltd) in 1985.

5.1.1 Features of the NewSpace industry

The commercial success of the SSTL can be used as an illustrative example of the revolutionary nature of the NewSpace industry. The traditional electronics and test industries have to adapt to these emerging trends. The associated challenges and opportunities were identified by Keysight [223] as:

- Rapid growth in the number of relatively low-cost satellites
- Numerous deployments of satellite constellations
- Satellites with short orbital life expectancies
- Prolific use of COTS components
- Lower launch costs - more frequent launches, increasing global competition
- Joint developments - hosted payloads

5.1.2 The CubeSat standard

The key cost factor for spacecraft is their mass. Hence, the classification of satellites is based on their mass. Typically, the small satellites are defined to have a mass ranging 500 to 1000 kg. The NewSpace satellites are significantly smaller. For these mass categories, the SI-style prefixes are used [222]. These include the nanosatellite class with the mass 1 to 10 kg. CubeSat is the industry standard for the nanosatellites.

Standard CubeSats are made up of 10×10×11.35 cm units ("Us") designed to provide 10×10×10 cm or 1 dm^3 of useful volume. The mass limit is 1.33 kg per unit. The units can be combined to create larger spacecraft such as 3U, 6U [224], [225]. Fig. 5.2 shows an example of a 3U CubeSat used for the O/OREOS biological mission.

The standardisation of the CubeSats brings a variety of benefits. Firstly, the satellites can be launched and deployed from unified deployers which could be provided by the launch provider, or a third-party [225], [226]. Secondly, the standardisation allows for commercialisation of the CubeSat development process. The complete, fully tested, systems can be purchased. Even the whole satellites can be procured as COTS kits to be integrated with the custom-developed payloads [227].

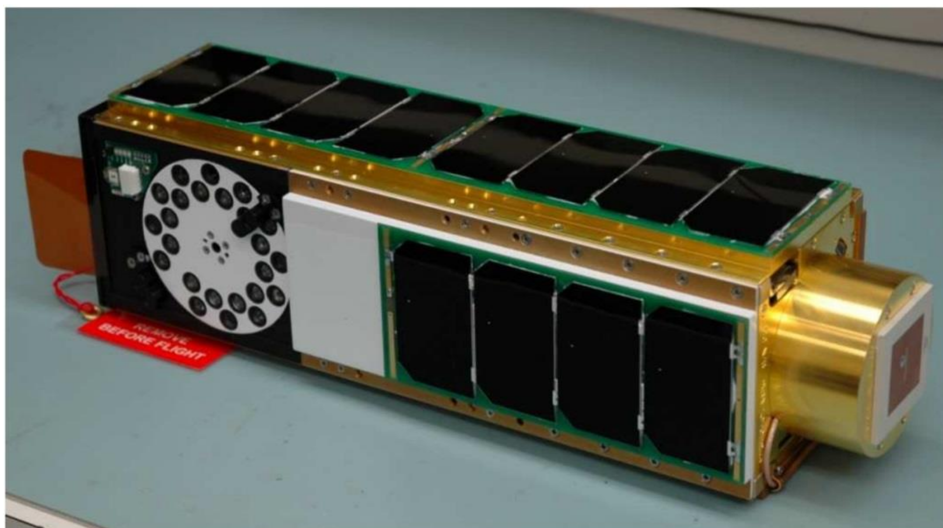

Fig. 5.2: The O/OREOS 3U CubeSat developed by NASA Ames. Picture credit [228].

5.2 Commercial components for NewSpace

This section aims to discuss the applications of the COTS parts in space designs and the related challenges including testing and qualification of these parts.

5.2.1 Space applications of commercial components

The key motivation for the usage of COTS components is the cost; according to SSTL, the savings are not only on the hardware for the FMs (flight models), but there could also be significant savings of the cost related to the development/debugging phases [229]. The purchase cost of the COTS parts could be reduced down to 1 % of the price of the space-qualified parts, and the delivery could be ten times faster [230].

Among the budgetary and programmatic factors, the COTS components also excel in various engineering factors [231], including:

- State-of-the-art functionality/performance (see chapters 1.1.1 and 2.3)
- Low size and weight
- Low power (important both for power and cooling designs)

However, when placed in the space environment, the COTS devices could suffer a variety of serious issues that require additional testing [231]. These include:

- Radiation tolerance
- Limited temperature range
- Vacuum performance
- Shock and vibration
- Limited lifetime

Another set of important drawbacks is related to the component engineering attributes such as [160]:

- Poor traceability
- Rapid and un-announced design and process changes
- Rapid obsolescence
- Packaging issues (plastic packages)

The poor traceability and rapid changes are the most important factors limiting the practicality of COTS parts testing. This problem can be reduced by procuring whole lots of devices and use the parts from the same lots for both parts testing and building the FMs [232]. The risk of applying the COTS components can also be reduced by using COTS components with a known flight heritage [229].

Both NASA and ESA are working on research programs focused on using automotive parts in space [233]. The automotive parts are designed and manufactured to meet higher quality and reliability standards, but they are of a similar price compared to classical COTS components. They also offer higher traceability and more information on changes (potential problems are more likely to be published). However, automotive parts are of limited types (i.e. there are no automotive grade high-resolution ADCs) and large minimum order quantities can be required. According to NESC [234], automotive certified or compliant parts are a type of COTS+ parts. The COTS+ part represents the level of commercial parts for which the customers are provided with test data [235].

5.2.2 Radiation testing of commercial components for NewSpace

The traditional RHA requires radiation testing of COTS components [236]. According to NASA's analysis [237], a typical cost of radiation testing (both TID and SEE) of a microcircuit was $50000 to $100000. Such a cost could be easily 50 % of a budget for a CubeSat project [227]. Hence, the radiation testing for low-cost missions has to be reduced to a practical (affordable) minimum. This section summarises published results of these low-cost radiation tests.

The team from Stellenbosch University published results of low-cost TID testing of various COTS components [238]. This work demonstrated that a significant cost-reduction could be achieved by testing in-situ and by reducing the number of parameters to only those which are crucial for the particular application. The reported test data included a plot of TID-induced degradation of an OPA as shown in Fig. 5.3. Such a smooth and monotonic degradation curve is ideal for the development of MU models. Notable are also annealing periods (marked with orange dashed vertical lines). These were caused by the interruptions of the irradiations during the nights.

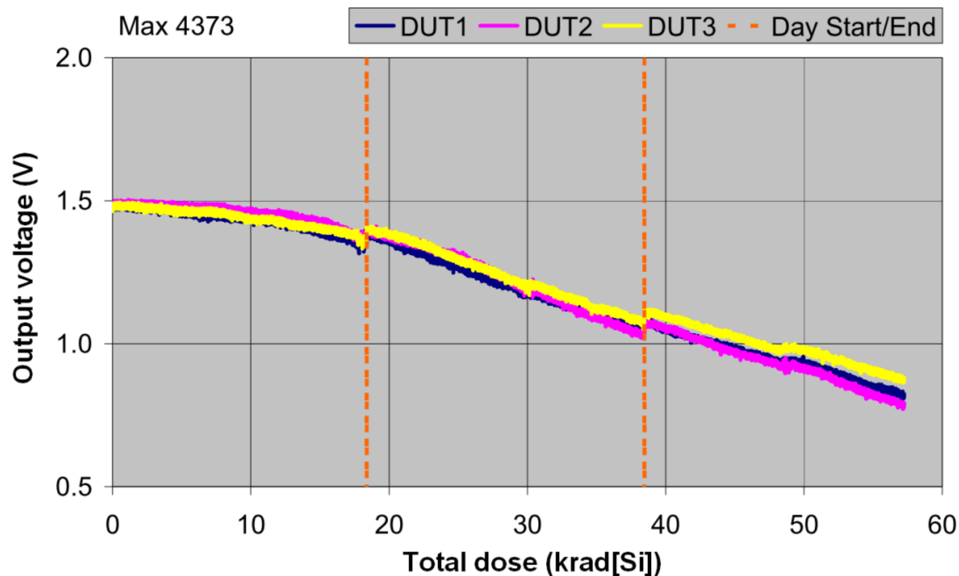

Fig. 5.3: TID response of MAX4373 OPA, showing that the output voltage started to degrade as soon as irradiation begins. Chart adapted from [238].

An alternative method of the cost reduction could be the reduction of the dose steps of a TID test using SBT. This approach was used by MIT students to test a set of digital COTS parts including MCUs and SD cards [239]. Only two dose steps were used which simulated an expected mission dose of 8 krad(Si), and 24 krad(Si) representing a safety factor of three. The results showed the drawback of the method; this test approach was only capable of showing that some parts could pass the test. For those parts, which failed, the test results were not detailed enough to understand the failure mechanism.

The tests discussed above were examples of TID testing of individual parts. Another emerging test method is testing at board level. Some recent works are reporting board-level tests of MCU boards. A good indication of the overall degradation and identification of the most sensitive components could be achieved [240].

5.3 Advanced in-situ TID test methods

As discussed in the previous paragraphs, the standard bench test is a rather obsolete method for the TID testing. The goal of this section is to give an overview of the in-situ test methods (ISTMs) and discuss the proposed advanced ISTMs that were demonstrated during this PhD research. The early results of the ISTM analysis were presented at the NSREC 2012 conference [241].

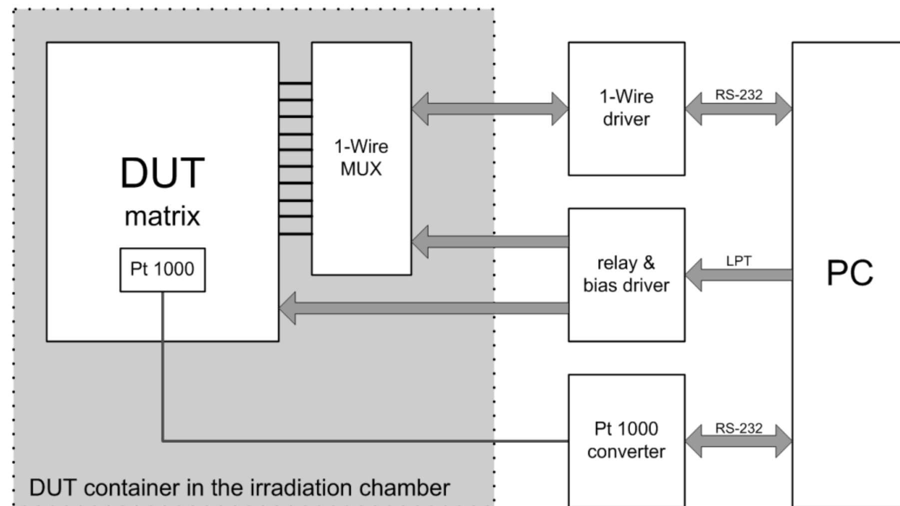

Fig. 5.4: Block diagram of an ISTM ATE. The equipment is divided between the DUT container located in the irradiation chamber and the set of test instruments placed in the laboratory.

5.3.1 In-situ TID test methodology

The ISTM is frequently based on fully automated test equipment (ATE). This typically consists of a DUT container which is irradiated and a set of test instruments located in a non-radiation area nearby. The two are connected via cables (see Fig. 5.4 for an example of an ISTM ATE). Such a test method brings numerous advantages, including:

- Fully automated testing, i.e. no manual operations are required ("run and forget")
- No limit of measurements duration
- No annealing occurs during measurements
- A higher limit on the number of parameters measured
- A significantly higher amount of data, allowing a detailed data analysis to be made
- The investigation of unknown effects/phenomena
- Temperature monitoring and control
- Precision DUT bias control using switched bias

The major technical challenge of the ISTM ATE is the design of the radiation tolerant electronics which have to be located in the DUT container, due to a limited connectivity between the container and the external set of test instruments. The limiting factor is the cables. A typical TID irradiation facility requires 15 m length of cables to

be placed in the labyrinth inside the concrete shielding. The cables could be a limiting factor for both high speed digital and precision analogue testing. Given these constraints, the typical purposes of the electronics in the DUT container are:

- To drive digital signals
- Signal conditioning of analogue signals
- To provide the multiplexing of both digital and analogue test channels

While the multiplexing can be easily realised using mechanical relays (inherently radiation tolerant at space-related doses), the design of radiation tolerant drivers and conditioners could be a serious problem. Nevertheless, there are a few options which can deal with such a hardware design challenge:

1. Using radiation hardened and proven components. This solution is limited by the high price of such components and their limited availability. A self-test circuit should be added to make sure that the test electronics are working properly during the test.
2. Using low-cost, COTS components in easily replaceable packages, replacing them as indicated by the results of the self-test routine. The ATE software can make a failure prediction and warn the test engineer in advance (before the actual failure of the hardware).
3. Adding an auxiliary shielded container, located in a lower dose rate area of the irradiation cell. This container would contain the electronics and would be connected to the DUT container via a short cable so that the signal integrity remains intact.

In nearly all cases, the best strategy is to combine options 2 and 3, i.e. to build a shielded container with low cost, commercial electronics incorporating a self-test using a mechanical relay loop-back. The ATE software would analyse the results and warn the test engineer about potential failure or significant parameter degradation. This strategy may be complicated for precision analogue systems, where the calibration of test electronics is needed. However, it can be used for digital components which have margins in the acceptable logic levels.

The benefits of the ISTM were demonstrated in a pilot experiment during which COTS digital thermometers (DS18B20) were TID tested in-situ (Fig. 3.15). The results of this successful experiment were presented at the RADECS 2011 conference [125].

To conclude, the ISTM ATE system is a rather more complicated concept than the standard test method. However, it is believed that the effort invested in designing and building the ATE is worth it, as the results of such a test are much more objective, and many advanced analyses can be carried out using the resulting data. It is also possible to combine the ISTM method with a standard bench test. Such a hybrid solution can be quite effective, especially for high-speed DUTs for which a pure ISTM test would be either impossible to design or too expensive to build.

5.3.2 In-situ TID-TC testing

The key technical challenge of the ISTM of the temperature coefficients is to perform the temperature sweep of the DUTs during the irradiation. The standard bench TID tests are typically performed to simulate the full temperature range of the devices using

temperature chambers such as Weiss [242]. This method is relatively simple, but has a lot of serious constraints:

- The irradiated devices can be thermally annealed during the *TC* measurement so the radiation-induced changes may be lost due to the long-duration exposure to elevated temperature
- The temperature profile of large chambers might be too slow. Therefore the two hours test window might not be followed [164].
- The repeatability of the *TC* measurements is limited by the accuracy of placing the samples in the chamber and the timing accuracy of the temperature profile.
- Temperature chambers are typically large and expensive (not affordable for low-cost COTS testing)

Modern localised temperature test systems (LTTS) were designed to address the constraints of the traditional testing in temperature chambers. These advanced instruments typically consist of a thermal head, which controls the temperature of the DUTs, and a base unit, that generates the air of stable temperature [243]. During the temperature test the head is attached to the PCB, and the forced air stream provides the heating or cooling of a single DUT. The LTTS is ideal for bench testing as it allows for fast temperatures changes and good test accuracy/repeatability.

As far as the ISTM testing is concerned, none of the methods described above is suitable. The temperature chambers are too spacious to be placed in the irradiation chamber, and the LTTS contains electronics that would have to be radiation hardened. In both cases, the prices of these instruments are not affordable by low-cost projects.

To address these issues, a novel method for fine DUT temperature control was designed to be used for ISTM testing during this PhD. As can be seen in Fig. 5.5 the method was based on a thermoelectric cooler technology (TEC).

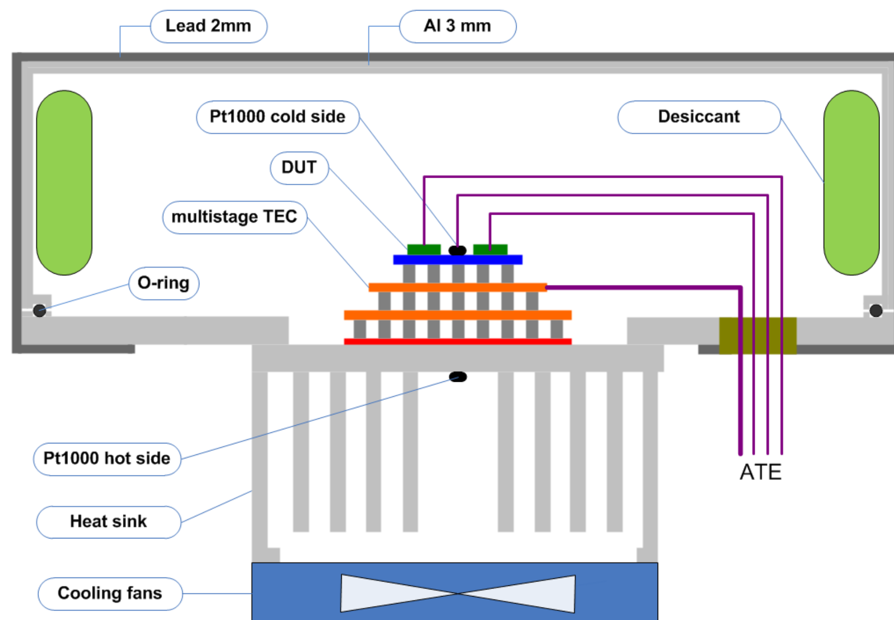

Fig. 5.5: Mechanical structure of the TEC assembly for the ISTM TID-TC testing.

In this concept, the DUTs are attached to a cold side of a multistage TEC using thermally conductive compounds or glues. The cooling of the TEC hot side is provided by a powerful heat sink with attached fans. The temperatures of the DUTs, as well as the TEC hot side, are monitored using radiation tolerant Pt1000 sensors. The TEC can be operated both in cooling and heating mode by changing the polarity of the DC current [244]. The TEC assembly must be placed in a hermetic container to minimise the humidity of the air around the TEC cold side, and thus suppress frost build-up.

5.3.3 In-situ dynamic dose rate TID testing

Detailed understanding of the dose rate sensitivity is a key challenge for the TID testing due to the need for accelerated testing (see chapter 3.5). Traditional dose rate testing consists of multiple TID tests performed at various dose rates [114]. This method requires parallel irradiation of multiple devices, and thus its accuracy could be limited by unknown part-to-part and lot-to-lot variabilities [245], [246]. Another issue is the long duration of the exposures, especially when ELDRS dose rate is required. This could lead to high budgets for the irradiation time. Hence, there is a need for advanced accelerated ELDRS test methods that could predict the device degradation induced by low dose rate.

Various accelerated methods can be found in literature, as summarised in a paper published by AIT (Austrian Institute of Technology) [247]. These include irradiation at elevated temperature, application of an external source of hydrogen (ELDRS testing only), and finally switching of the dose rate during the exposure from a high to a low dose rate (SDRT). AIT reported results of the SDRT method for LM158 operational amplifiers and LM339 comparators. The reliability of the low dose rate prediction curves generated by the accelerated switching test method was validated by comparison with the LDR reference measurements.

An alternative test method can be proposed. The method is based on dynamic dose rate ISTM test approach. The DUTs are placed in an irradiation container, whose distance from the radiation source is controlled by the ATE using a linear actuator. Therefore this test system allows for dynamic change of the dose rate during the irradiation. The dose rate is changed in a continuous loop such as HDR-MDR-LDR. The cumulated dose at each irradiation position (or dose rate step) is kept constant by adjusting the duration of each step. The TID-induced degradation is measured at the end of each irradiation step. This fully automated solution can bring various advantages including:

1. Only one set of DUTs is used, no part-to-part and lot-to-lot variability
2. High dose and dose rate resolution can be achieved – a detailed analysis of the dose rate sensitivity versus dose can be performed. The importance of this analysis was reported by Chen at al. [104].
3. Significantly shorter irradiation time – affordable test for NewSpace

It should also be noted that the proposed test system can be used to simulate the in-orbit variations of the dose rate. Such a dynamic in-orbit simulation was demonstrated by ESA's ESTEC team [248].

5.4 In-orbit TID testing

Traditionally, the in-orbit testing (IOT) has been used for validation and demonstration of the performance of payloads of communication and Earth-observation satellites [249]. A broad spectrum of technology-demonstration missions has also been flown using both traditional-space and NewSpace technologies. The purpose of this chapter is to discuss published tests/experiments, requirements for NewSpace compliant experiments, and possible methods for monitoring the actual TID levels in-orbit. Flight opportunities for the in-orbit experiments are also outlined.

5.4.1 In-orbit TID test results

Over the decades, some technology-demonstration missions have been launched including missions that were measuring TID effects under real space conditions. This section gives an overview of the missions which were most relevant to this PhD.

The Japanese space agency NASDA published results obtained from the ETS-V, VI, MDS-1 and ADEOS-II missions [250]. The experiments on these satellites consisted of various logic circuits (CMOS, TTL) and sets of RADFETs (dosimeter DOS on board MDS-1 and ADEOS-II). Various shielding covers were used to study the effectiveness of the shielding thickness. The TID results from 10 months of the ADEOS-II DOS experiment are shown in Fig. 5.6. A TID level of 416 rad(Si) was measured by a RADFET under 0.7 mm shield. The ADEOS-II was launched on 14 December 2002 into Sun-synchronous sub-recurrent orbit at an altitude of about 800km. The inclination was 98°.

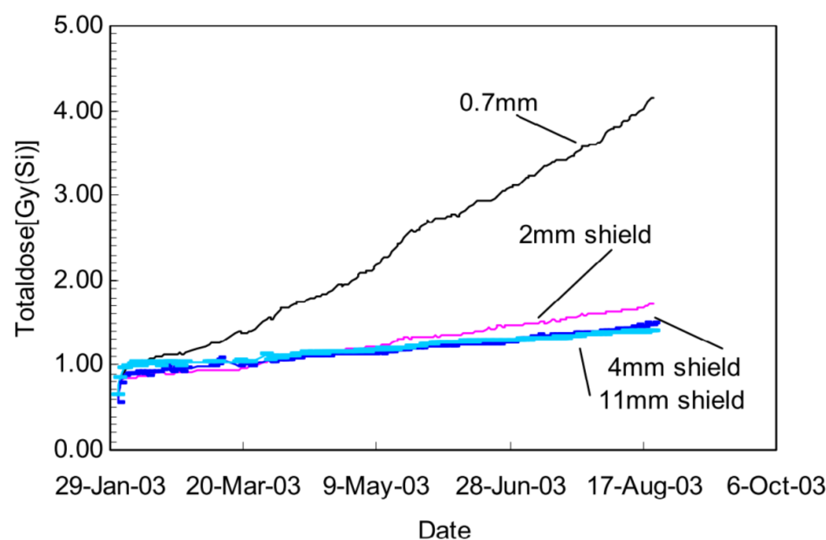

Fig. 5.6: Total dose profile for different thickness of Al shield from ADEOS-II DOS experiment. Chart adapted from [250].

The European PROBA-II mission carried a Technology Demonstration Module (TDM) to monitor radiation effects in semiconductor devices. The primary goal of this experiment was to observe SEEs in modern memory devices, but the experiment also measured TID for 18 months. The RADFETs were used to the measure mission TID,

and the paper reported problems with representing the TID measurements due to significant instabilities in the temperature of the RADFETs [251].

KITSAT-1 was a South Korean technological satellite launched in 1992. Among the other experiments, it also carried a total dose experiment (TDE). TDE was based on a set of RADFETs. The acquired data from 1992 to 1994 were analysed for a better understanding of the influence of the temperature on the RADFET readings. Furthermore, the data were compared with the AP8MAX/AE8MAX models with a good agreement [32].

RADFETs were also placed on board the Spanish NANOSAT-1B mission. Results of six years of TID measurements were published by INTA including a comprehensive analysis of the mission TID based on the SPENVIS simulations [252]. As can be seen in the charts in Fig. 5.7, there was an excellent match between the simulated and measured doses for solar protons.

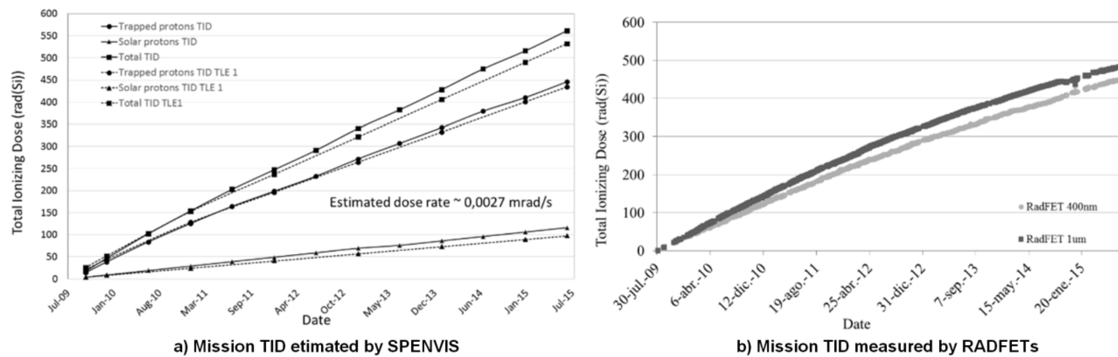

Fig. 5.7: Mission TID for the NANOSAT-1B as a function of date. Left chart a) represents results of the SPENVIS simulation and right chart b) shows the real TID mission data measured by a pair of RADFETs. Charts adapted from [252].

The final mission to be mentioned in this overview is the Van Allen Probes [253]. Built and launched by NASA, these twin probes were collecting data about the Earth's Van Allen radiation belts, and the response of these belts to solar activity. Each spacecraft carried a Relativistic Proton Spectrometer (RPS) [254], whose purpose was to measure the upper energy range of proton flux in the radiation belt environment to improve radiation models, and an Engineering Radiation Monitor (ERM) to provide telemetry data on the environment. Data published from the two-year primary mission showed mission TID levels of hundreds of krad(Si) and rather complex response of ERM's RADFETs to this harsh environment [68], [255].

In conclusion, the published in-orbit data demonstrated a good agreement of the TID measurements with the models and also showed a lack of data related to the TID-induced degradation of components for space DAQ systems.

However, there was a mission designed for such an in-orbit experiment. The University of Montpellier and Alcatel developed an in-orbit experiment to fly three electronic devices and monitor their degradation in flight, as well as the dose received and the temperature [256]. The tested devices included the AD670, an 8-bit ADC. Unfortunately, the mission failed to reach the orbit due to a malfunction of the Dnepr launch vehicle.

5.4.2 Requirements for the in-orbit experiment

The NewSpace style in-orbit radiation experiment shall be designed to follow the extreme constraints of the nanosat/picosat missions such as:

- Extremely low supply current in active mode, most of the mission time to be in a passive mode (unpowered mode), but still to be sensitive to radiation
- Very small PCB area
- Ideally no coils, solid capacitors only
- Easy integration with arbitrary satellite buses
- A software package to be provided for the satellite and ground controls

5.4.3 Measurement of total ionising dose in space

The accuracy and reproducibility of any radiation experiment strongly depend on the accuracy of the dosimetry system (see chapter 4.2.3). In principle, every dosimeter consists of a detector sensitive to radiation, and data acquisition electronics that is either radiation hardened, or placed outside the radiation. In the case of in-orbit experiments, the shielding of the electronics is limited due to its mass and volume, and in the case of NewSpace nanosat/picosat missions, it is usually avoided. Therefore the challenge is to design a compact dosimeter in which both the detector and DAQ electronics are exposed to the same environment. The following paragraphs discuss the detection techniques for in space dosimeters (radiation monitors) [257], [258]:

Ionisation chambers are very precise detectors and the industry-standard for terrestrial TID testing (see chapter 6.2.1). However, their use for in-orbit dosimetry is limited by their volume requirements, need for high voltage biasing (hundreds of volts), complicated signal conditioning for DAQ (conversion of pA currents). Ionisation chambers work only in an active mode; they measure dose rate. Nevertheless, the Geiger-Mueller tubes were used in the early missions, including the Explorer-1 [67].

After exposure to radiation, some materials retain part of the absorbed energy in metastable states. This energy is released in the form of light of various types, depending on the material (so-called luminescence). The luminescence can be accelerated (stimulated) by light, and this is the principle of the Optically Stimulated Luminescence (OSL) detectors. The University of Montpellier developed an OSL detector that was able to measure both TID and DDD effects. This OSL experiment flew on various missions including CARMEN-2 [259]. The OSL technology is a promising alternative to the other solid state detectors, but it is very complex (both the electronics and the optical part), and thus it is not ideal for the nanosats/picosat experiments as defined in chapter 5.4.2.

The Floating Gate Dosimeter (FGDOS) is a TID detector based on a floating gate metal-oxide-semiconductor FET transistor structure (FG-MOSFET). These devices were originally conceived for the implementation of cells in non-volatile memories, but they appeared to be also suitable for TID dosimetry due to their monotonous response to the TID exposure. This concept was successfully proved for the first-time on-board the MPTB experiment [109], during which AMD27C64 UVPROMs were in-orbit tested [260]. The FGDOS technology was also tested on the 4M Lunar Flyby Mission in 2014, during which a dual FGDOS measured TID level up to 23 rads(Si) in good agreement with TID simulated by OMERE 4.0 [261].

As demonstrated in section 5.4.1, the majority of in-orbit TID measurements were based on the RADFET technology. RADFETs were invented by Andrew Holmes-Siedle and W. Poch [262]. RADFETs are p-channel MOSFET transistors with specially fabricated, thick gate oxides. Radiation-induced holes are trapped in the transistor gate oxide, causing a shift in the gate threshold voltage, ΔV_T (see chapter 3.3.1). The magnitude of this shift is proportional to the TID received by the transistor [18], [263]. Typical radiation response of an unbiased Tyndall RADFET is shown in Fig. 5.8 b). The manufacturers provide calibration curves for every production batch [264]. Hoverer these typically show only HDR results at a single bias condition. Hence a custom calibration should be performed.

RADFET readout is performed either by measuring the I_D-V_{GS} curve of the RADFET and extracting V_T or, directly, by inducing a constant DC current, I_D, through the device and measuring the source-drain voltage, $V_{DS}\equiv V_{GS,}$ which is a suitable definition of V_T for practical use. In any case, radiation-induced shifts in V_T are not dependent on the definition of V_T. The constant current method has become a standard technique for most practical applications and typically works in combination with a bias voltage applied to the gate to control the TID sensitivity of the RADFET [265]. Such a dosimetry system periodically switches between the "exposure" mode, with gate bias voltage V_I applied, and the "reader" mode, during which the drain is driven with a constant current I_D (Fig. 5.8 a)).

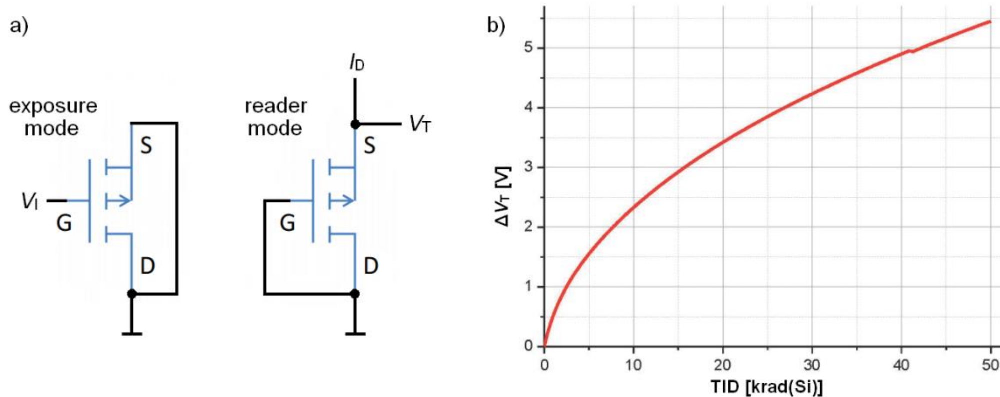

Fig. 5.8: Schematic diagrams of the RADFET in both exposure and reader mode (left-hand side). Typical radiation response of an unbiased Tyndall TY1002 RADFET is shown on the right-hand side. Chart adapted from [264].

One of the key sources of measurement error for a RADFET based dosimeter is the variation in the ambient temperature, as the main dosimetric parameter, V_T, is temperature dependent, i.e. has a temperature coefficient TC_{VT}. Over the decades of the use of RADFETs, some compensation methods for temperature effects have been developed. The most common method uses an *MTC* point of the I_D-V_{GS} characteristic (see chapter 3.8.5). The *MTC* point corresponds to the drain current at which the temperature sensitivity is minimum (virtually zero). If this current is used in the reader mode, the TC_{VT} becomes negligible. The disadvantage of this method is that the device-to-device variation in *MTC* current can be significant. Ideally, each RADFET should be *MTC* calibrated and an appropriate value of the *MTC* current used by the reader [266]. Another method uses a known value of the RADFET TC_{VT} and the actual temperature

of the RADFET during the readout; compensation is then done mathematically, during the processing of the data [32]. The third method is based on a dual measurement of two identical RADFETs integrated into a single package. Each of the RADFETs is biased using a different voltage, and thus they have a different shift in V_T. The difference between the shifts in V_T is proportional to the TID and, if the RADFETS are identical, the TC_{VT} should be minimised [267].

The major drawback of the methods listed above is their dependence on the stability of the TC_{VT} and *MTC* during the irradiation. It has been shown that the *MTC* point and TC_{VT} values change with TID [268], [269], [270]. These results were based mainly on a comparison of pre- and post-irradiation measurements only, and were not comprehensive in terms of bias conditions. As discussed in chapter 5.3.2, the post-irradiation bench measurement of TC_{VT} can often be affected by concurrent thermal annealing, reducing accuracy.

To conclude, the RADFETs seem to be an ideal solution for the in-orbit dosimetry due to their simple application, passive mode of operation (RADFETs can measure TID while unbiased) and very small footprint (SMD versions are available). However, there was a lack of detailed TID calibration and *MTC*/*TC* data. Therefore a set of RADFET TID experiments was performed as part of the presented PhD work.

5.4.4 Flight opportunities for in-orbit experiments

The NewSpace offers various options to fly a scientific payload on board small satellites. This section outlines flight opportunities that are most relevant for the presented PhD in-orbit experiment.

The CubeSats have become the most frequent type of small satellites. The rapid growth in the number of launched CubeSats can be seen in Fig. 5.9. This trend is believed to be driven by the standardisation of the CubeSat platform and affordable launch opportunities (both by ride-shares and dedicated low-cost missions).

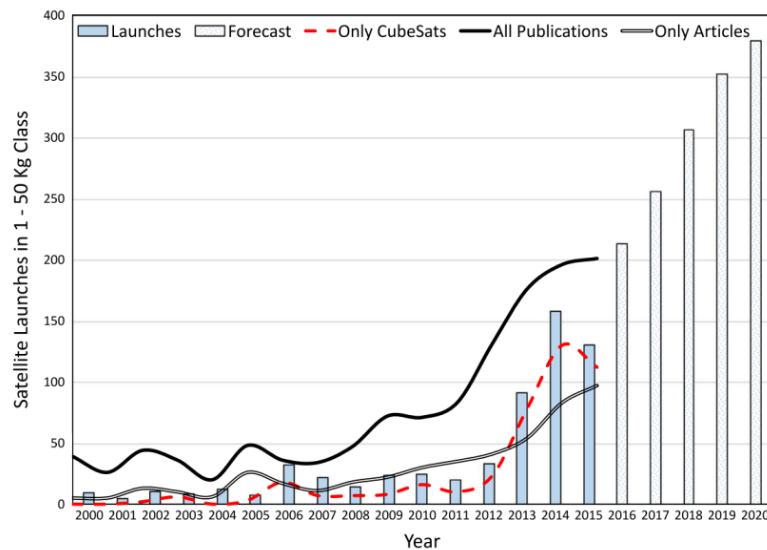

Fig. 5.9: Historical and predicted launches of small satellites. The red-dashed line shows a total number of launches confined to the CubeSat platform. Chart sourced from [10].

A significant proportion of these missions are the academic/research CubeSats [10]. Hence, flying an in-orbit experiment on an academic/research CubeSat mission is the first flight opportunity to consider, due to a potential non-commercial nature of these missions (free of charge payload access). The in-orbit experiment could be accepted as a useful payload for the primary mission as it provides mission TID and temperature measurements.

Another opportunity for payload access could be the so-called hosted payloads. This concept is based on the idea that even highly integrated small satellites may still have some limited, but a meaningful fraction of mass/volume, power and telemetry capability that could be used by a hosted payload. This payload access could be especially valuable when offered by satellite constellation programs such as Iridium NEXT, which provided up to 50 kg of custom-designed hosted payload [271]. A part of this offer was also standardised payload access named SensorPOD that allowed 5 kg of scientific payload to be integrated into a format similar to a 3U CubeSat and with an extended lifetime of ten years.

The final payload access opportunity, to be discussed in this section, is the revolutionary technology of payload "Plug&launch" developed by Open Cosmos [272]. This NewSpace-style commercial concept offers the customers to be focused only on their payloads and all the other attributes of the missions to be entirely covered by Open Cosmos [273]. As illustrated in Fig. 5.10, the mission development process is based on three overlapping "qb" tools. The payload design/development and integration are supported by the qbkit, which provides an identical interface as would be on-board the qbee satellite (Open Cosmos' CubeSat platform). The qbapp is a software package supporting all mission activities including simulations and ground control.

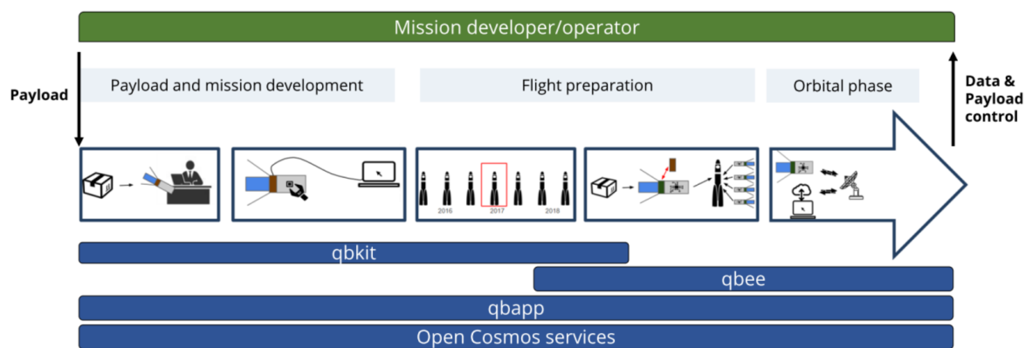

Fig. 5.10: The workflow of the Open Cosmos' mission development process. The customer's involvement can be reduced to providing payload and receiving in-orbit data. Diagram adapted from [273].

5.5 Life Mission Measurement Uncertainty model

The purpose of the proposed Life Mission Measurement Uncertainty model (LMMU) is to provide a near real-time value of the DAQ system MU during the space missions. Based on the actual environmental conditions, measured by the Space Environmental Monitor (SEM) subsystem of the space experiment, the LMMU can calculate the actual MU for the moment of the execution of the DAQ job of the experiment.

The LMMU model is based on three principal MU evaluations:

1. Type A uncertainty calculated from the repeated measurements of each DAQ channel
2. Initial values of the Type B uncertainties of each part of the DAQ signal chain u_{eBi} estimated before the launch
3. Extension of Type B uncertainties u_{eBi} for error contributors related to the following conditions:
   a) Mission duration (ageing)
   b) Actual temperature and temperature history
   c) Total Ionising Dose radiation (TID)

The Type A uncertainty will be calculated for the whole DAQ signal chain as described in section 2.2.2. The resulting value of u_{xA} can be processed using Student's distribution. Such a model is used in the software of high-tech calibration instruments for primary labs including the MI's resistance bridge 6020Q [274].

The Type B uncertainties will be processed using a two-stage model as shown in Fig. 5.11. The data from the SEM (temperature and dose rate) are processed using integrators to provide temperature history (average temperature AVT, current temperature CTE) and current Total Ionising Dose (TID). The data from a clock source will be used to compute the mission elapsed time MET.

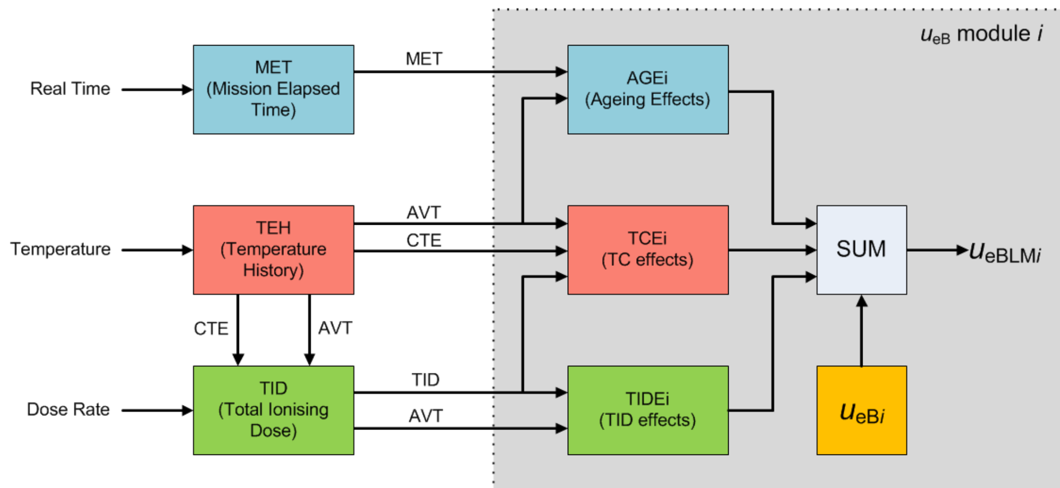

Fig. 5.11: Block diagram of the Type B part of the LMMU model. The inputs from the onboard clock and SEM are processed by the integrating blocks MET, TEH and TID so they can be used by multiple u_{eB} environmental modules. Each module processes environmental sensitivity of one particular measurement error source and combines it with the initial value u_{eBi}.

The second stage of the LMMU model consists of the individual modules calculating the influence of the environmental variables on each Type B measurement error contributors. Therefore every parasitic parameter of each part (each HW component) of the DAQ signal chain will have a dedicated u_{eB} environmental module. Each u_{eB} environmental module consists of a sum block combining the initial value of u_{eBi} with the results from the three blocks: AGEi, TCEi and TIDEi.

AGEi block calculates the ageing of the part of the signal chain using the MET value and ageing parameters provided by the part manufacturer; for example, there is a Long-Term Stability parameter defined for voltage references [188]. The ageing is also a function of temperature; therefore the AGEi block is also fed with the AVT value.

TCEi is responsible for calculating the temperature-induced effects on the parasitic parameter of the HW component. It uses a value of *TC* (Temperature Coefficient) provided by the manufacturer and the difference of the CTE from the nominal temperature at which the DAQ system was calibrated before the launch. The value of the *TC* is not static during the space mission; it is sensitive to radiation. Therefore the TCEi block uses a TC-TID model to calculate the true value of the *TC* based on the TID value. The TC-TID model can be obtained from terrestrial radiation experiments as shown in this work. The TC-TID model can also use the AVT value to take into account the influence of irradiation temperature on the TC-TID model.

TIDEi is a block computing a particular TID model providing a value of a TID-induced shift of the parasitic parameter of the HW component. It is based on results of terrestrial TID experiments performed ideally at various dose rates and temperatures. The dose rate and temperature sensitivities of the TID-induced effects are discussed in the in chapter 2. The TIDEi block may also compute a response of the HW component to a change of some electrical conditions, for example, the Line Regulation parameter of a voltage reference circuit could be sensitive to TID [178].

The LMMU model was designed to minimise the complexity of evaluation of the Type B MU. Therefore it is assumed that the structure of the computing blocks allows for the suppression of the correlation between them. Hence, it is believed that the results of the LMMU modules u_{eBLMi} can be combined using the equation (2.4).

6 EXPERIMENTAL TOOLS AND FACILITIES

This chapter aims to provide with an overview of the tools and facilities that were used for the PhD radiation experiments. The majority of them were developed and manufactured from scratch to follow the special requirements of the ISTM experiments, including the novel DUT temperature controllers.

6.1 Irradiation facility

The majority of the presented TID experiments were conducted in the MRC (Medical Research Council) cobalt-60 facility operated by Cobham RAD Solutions in Harwell, UK. The MRC irradiation facility (MIF) was originally built in the 1950's for medical research purposes. It consists of a concrete-shielded cell, in which two panoramic cobalt-60 sources are placed. The sources are operated remotely from the adjacent laboratory via electrically-driven Teleflex cables as shown in Fig. 6.1. MIF allows for non-stop irradiations in the order of weeks in duration. The layout of the MIF cell is shown in Appendix A.1. The irradiation area provides space for placing containers within 3 m distance from the source. Hence, the dose rate range could be as low as 10 rad(Si)/hr.

Fig. 6.1: A view of the irradiation area of the MIF during a PhD experiment. Two irradiation containers (2), (3) were placed in front of the sources (1). The source shielding block (4) allows for short irradiations (it reduces the travel time during which the sources are exposed).

To support the accommodation for the ISTM experiments, the MIF laboratory was equipped with instrumentation racks as illustrated in appendix A.2. This area was outside the irradiation cell; therefore the equipment was not exposed to radiation. The irradiation containers could be connected to the test equipment via 15 m long cables. An Internet-based remote control system was deployed in the MIF. It provided remote monitoring of the experiments including changing their settings and downloading actual test results. Test equipment was also remotely monitored by a set of cameras.

6.2 Dosimetry system

A calibration of the irradiation facility was performed during the preparation of each TID experiment as required by the test standards (see chapter 4.2.3). The calibration/dosimetry procedure was performed in multiple steps. The coarse position of the irradiation container in the MIF was firstly calculated based on the data from the dosimetry map of the MIF cell. Secondly, a set of new dose rate measurements was made, followed by another calculation of the target position and measurement of dose rate in it. This procedure continued until the measured dose was within ±0.1 % of the target dose rate.

6.2.1 Ionising chamber dosimetry equipment

The dosimetry system was based on an ionising chamber detector placed directly in the irradiation container instead of the DUT board as shown in Fig. 6.2. The detector was therefore exposed to the same dose rate as the DUTs. For larger DUT boards, the detector was placed in multiple positions within the irradiation container to ensure good uniformity across the whole DUT board.

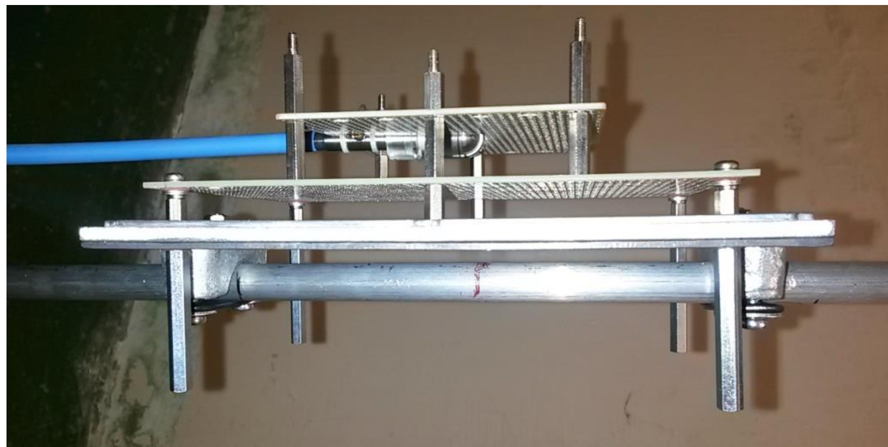

Fig. 6.2: A side-view picture of the open irradiation container during the dosimetry procedure prior to the TID experiment. The ionising chamber detector is attached to the top “dosimetry PCB”, which is in the identical distance from the radiation source as the DUTs would be during the experiment.

The selection of the commercially available ionising chambers was limited to a few manufacturers of medical instruments for radiation therapy. The key factor for the selection process was the dimensions and the sensing volume of the ionising chambers.

Ultra-small ion chambers offer better placement accuracy as the geometry of their sensing volume is similar to the geometry of the samples. The smallest ion chambers on the market were offered by PTW-Freiburg, Germany. Hence, the selected dosimetry equipment consisted of the following PTW equipment [275], [276]:

1. TN31010, 0.125 cm^3 semiflex ionising chamber detector
2. T26005.1.001-20, 20m detector to dosemeter extension cable.
3. UNIDOS-E, universal dosemeter.

The dosimetry system also contained an OPUS20 barometer and thermometer, manufactured by Lufft, Germany [277]. OPUS20 was used for the measurements of the air in the MIF cell before the dosimetry took place. These measurements were used for the air-density corrections [275]. All equipment was subjected to regular calibrations.

6.2.2 Measurement uncertainty of the dosimetry system

The MU of the dosimetry system was evaluated using a combination of error sources specified by the manufacturers and data from the testing of the actual dosimetry system at MIF. Standard MU estimation procedure was used as defined in chapter 2.2.2. It should be noted that the estimated MU is valid only for a dosimetry system in which the ionising chamber detector and dosemeter are within one year after calibration. All definitions of error sources are expressed in % of the measured dose rate (% of reading). The resulting measurement uncertainty budget is summarised in Appendix E.1.

The Type A uncertainty was estimated as a standard deviation of 130 dose rate measurements of 360 rad(Si)/hr. The integration time of 30 s was used. A histogram analysis of these readings showed very small scatter of the data (Fig. 6.3). The Type A uncertainty was calculated using the formula (2.2) as $u_{xA} = 0.01$ %.

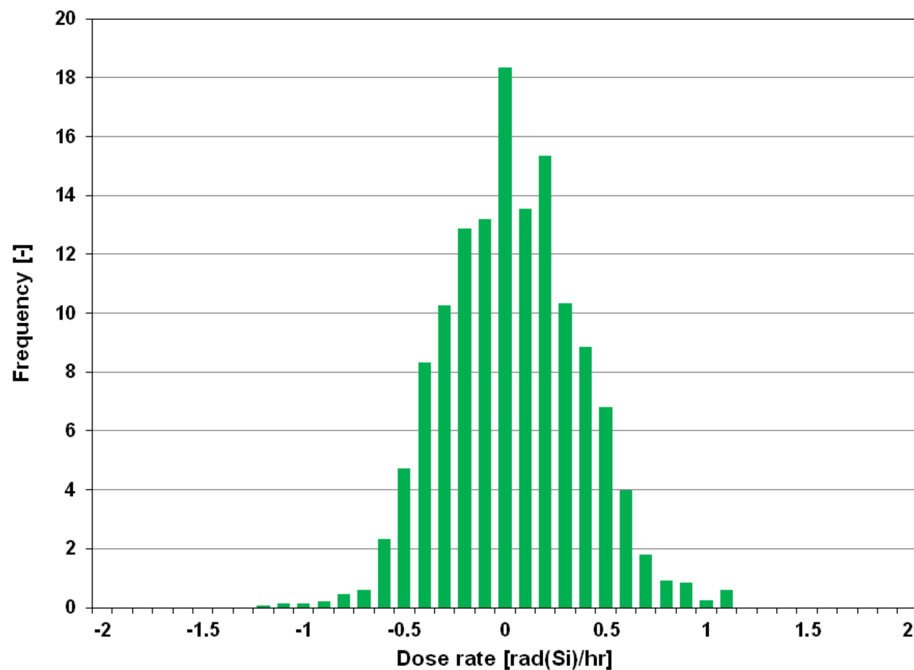

Fig. 6.3: A histogram of dose rate measurements. Most of the readings were within ±0.25 %.

The values of the Type B error sources obtained from the literature (operational manuals, calibration certificates and datasheets) are summarised in the Tab. 2.1. Normal and rectangular distributions were assumed to be appropriate for these error sources. Formula (2.3) and constants from Tab. 2.2 were used for calculating the u_{eBi} values.

Tab. 6.1: Type B error sources of the dosimetry system as specified in the literature.

Instrument	Literature	Error source	u_{eBi} [%]
Detector TN31010	[278]	Calibration uncertainty	$u_{eB1} = 0.55$
		Polarity effect	$u_{eB2} = 0.17$
	[279]	Long-term stability (per year)	$u_{eB3} = 0.58$
Dosemeter Unidos E	[280]	The accuracy of current/charge measurement	$u_{eB4} = 0.29$
		Reproducibility	$u_{eB5} = 0.29$
		Long-term stability (per year)	$u_{eB6} = 0.06$
		Non-linearity	$u_{eB7} = 0.29$

The imperfections of the extension cable from the detector to dosemeter introduced two types of error sources:

- Electrical current leakage, specified as 1 fA per the entire cable [276]. This systematic error was suppressed by the zeroing phase of dosimetry [280].
- Radiation-induced leakage current was specified as 1 pC(Gy.cm) [276], which was equivalent to 1 %/m when the cable was exposed to the same doserate as the detector [280]. Radiation-induced leakage current appeared to be a significant error source, and it needed to be further investigated.

For the case of the irradiations in MIF cell, the active (exposed) length of the cable consisted of two components:

1. The cable placed in the dosimetry position. It was assumed to be exposed to the same doserate as the detector. The maximum length of this cable section was $cl_1 = 0.25$ m.
2. The cable from the dosimetry position to the wall port from the irradiation cell (cl_2). The doserate drops across the cable, and it should be approximately proportional to the inverse square law as the cable goes straight from the dosimetry position to the wall port.

The doserate distribution across the length of the cable was measured in MIF cell. The worst-case dosimetry configuration was simulated; it was the measurement of the highest dose rate. The detector would be placed in the closest position to the source, and the exposed length of the cable would be the highest.

The results of the measurement of the dose rate distribution across the cable (placed on the floor in the MIF cell) are shown in Fig. 6.4. After normalisation, this dose rate profile was a relative measure and could also be expressed as an equivalent cable length ratio. The equivalent cable length was obtained by integration of the equivalent cable length ratio profile, and it resulted in $cl_2 \approx 0.5$ m. The total equivalent cable length was $cl = cl_1 + cl_2$, and therefore the radiation-induced leakage current introduced measurement error of 0.75 %. This error was assumed to have a rectangular distribution; hence the resulting error source was estimated to be $u_{eB8} = 0.43$ %.

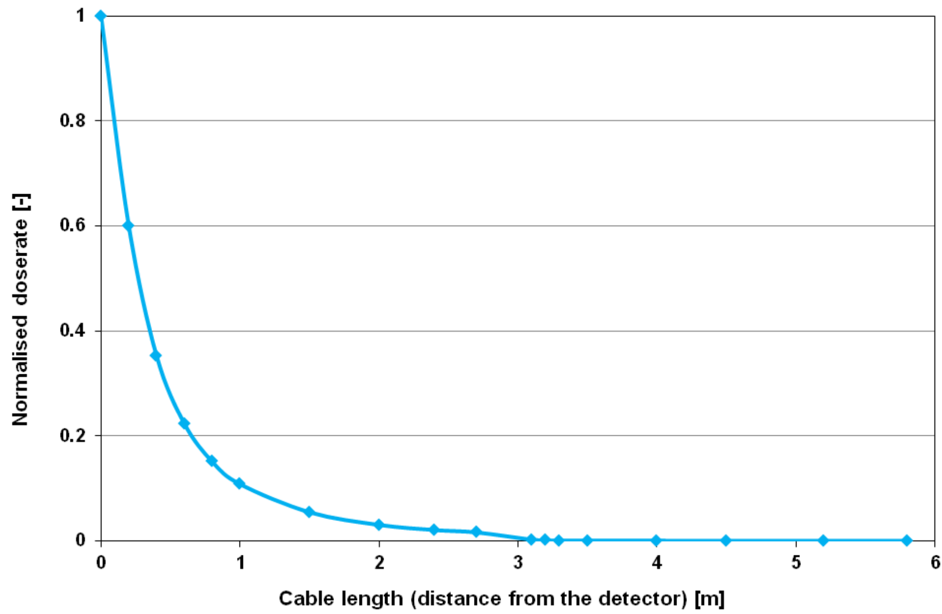

Fig. 6.4: Normalised doserate profile across a length of the dosimetry cable placed in the MIF cell. The layout of the cable represented a simulated high dose rate dosimetry job.

The calculation of the air-density correction factor k_{TP} of the ionisation chamber was automatically performed by the Unidos E using the formula [275]:

$$k_{TP} = \frac{P_0}{P} \cdot \frac{273.2 + T}{273.2 + T_0}, \tag{6.1}$$

where T and P are the temperature and pressure in the measuring environment, and the reference values are T_0 = 20 °C and P_0 = 101.3 kPa.

The actual values of T and P were obtained from the measurements in the MIF cell using the OPUS20 barometer. According to the manufacturer [277], the OPUS20 temperature measurement error was 0.3 °C and the air pressure measurement error was 0.5 hPa. OPUS20 did not measure the true temperature of the detector; the difference was estimated to be below 1 °C. Using the formula (6.1) and rectangular distribution, the random combination of these air measurement errors induced an air-density correction error sources u_{eB9} to u_{eB11}as summarised in Appendix E.1.

All of the identified Type B measurement error sources (u_{eB1} to u_{eB9}) were combined using the formula (2.4) resulting in a combined Type B uncertainty of u_{xB} = 1.07 %.

Using the formula (2.5), the combined standard measurement uncertainty u_x = 1.07 % was obtained by from the Type A and Type B uncertainties. Finally, the extended measurement uncertainty was calculated as per equation (2.6) and coverage factor k = 2:

$\underline{U_x = 2.2\ \%}$

6.2.3 Inverse square law test of the MIF cell

There were no means available to make an independent test of the irradiation facility as only a single dosimetry system was available. However, there was a possibility to perform a set of dose rate measurements at various linear distances from the source and analyse their agreement with the inverse square law [281]:

$$dr(d) = \frac{dr_0}{d^2}, \quad (6.2)$$

where dr_0 is the dose rate at the radiation source and d is the distance from the source. This law is valid only for point sources; therefore the impact of the real geometry of the radiation sources must be investigated.

The chart in Fig. 6.5 shows the results of the dose rate measurements performed in 0.2 m distance steps at the height of the sources. The dose rate covers the majority of the PhD experiments (36 to 360 rad(Si)/hr). The data were fitted with the inverse square function, and the fitting error was plotted.

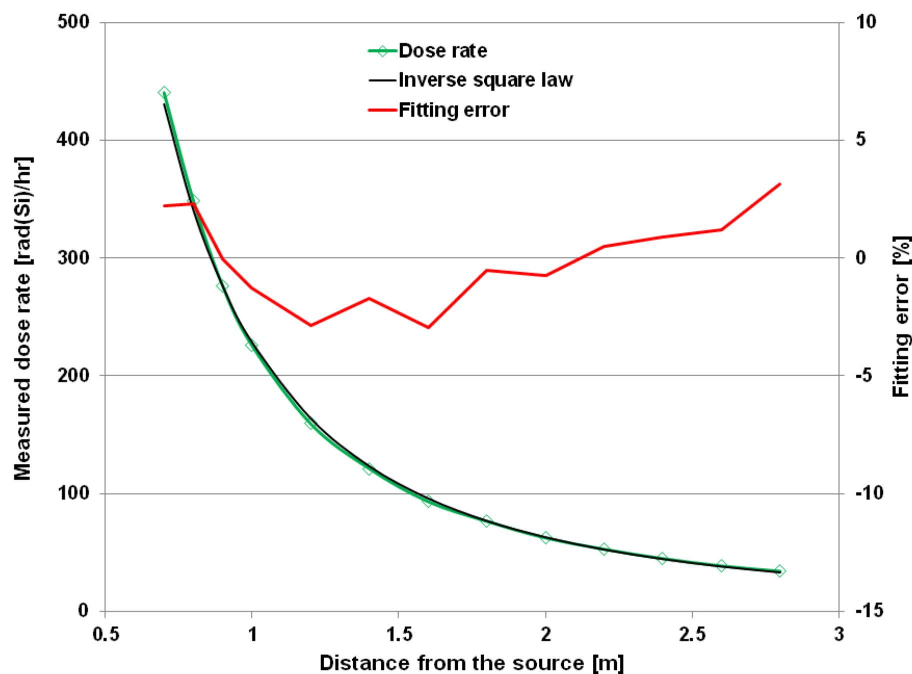

Fig. 6.5: Inverse square law test of the MIF cell and dosimetry system. The dose rate measurements were made with a 0.2 m resolution.

The analysis showed that measurements fitted the inverse square law within a ±3 % window, which seemed to be a very good result, taking into account the broad spectrum of error sources in this experiment. They included the real geometry of the source (approximately 30 x 5 mm pencil), MU of the dosimetry system, MU of the distance measurements (tape measure was used, alignment issues), scattered radiation in the cell, directional response of the detector and other error sources.

6.3 Test software

The PhD experiments required the development of complex software for various platforms, including software for the Windows-based PCs, proprietary embedded test controllers, COTS test instruments and Linux-based mini-computers. The test software had to be designed for high reliability – the TID radiation testing cannot be interrupted, and the experiments were often running non-stop for weeks and in some cases for months. Some of the advanced experiments required parallel testing, which was supported by multi-threaded PC software.

6.3.1 PC test software

The PC software was developed as a modular software package called STS (Systematic Test Software). STS was developed as a universal tool covering all the software needs related to fully automated radiation experiments, including:

- Dosimetry activities (dosimetry system DAQ and control)
- Irradiation scheduling and real-time monitoring (Cassandra tool)
- ISTM testing (control of instruments, DAQ, communication with DUTs)
- Remote monitoring of experiments
- Data analysis (both real-time and post-experiment)

The STS package was developed using ANSI C and C++ languages [282]. The use of the ANSI C allowed sharing of the STS code between various test platforms. All scientific data were processed using high-resolution 64-bit floating-point data [283].

STS consisted of five software layers/modules:

- Test instrument drivers (using VISA or custom APIs)
- DUT communication drivers (proprietary drivers or DLLs)
- Test scripts (individually developed/modified for a particular experiment)
- Data analysis and a chart plotting module
- User interfaces (customised for each experiment)

An example of the STS user interface is shown in Appendix B.1.

The majority of the instrument drivers were custom developed to ensure appropriate timing and error handling in case of unexpected failures during the ISTM experiments. SPCI command language was used to command the COTS test and measurement instruments, that were connected via RS-232, USB, GPIB and LXI using various VISA and IVA drivers [284].

6.3.2 TSP software

The advanced ISTM PhD experiments also used Keithley instruments that allowed for executing embedded test scripts loaded to the instrument from a PC. This modern test technology is called TSP (Test Script Processor), and it significantly increases the test speed by running the test scripts internally in the instrument, and thus reducing the communication with the test PC [285]. The STS was extended by a TSP driver module, which allowed running the scripts and transferring test data via USB and LXI. The TSP scripts were coded using the Lua language [286].

6.3.3 Software for the in-situ test controllers

The in-situ TID experiments required the development of a variety of in-situ test controllers (ISTCs). The software for the ISTCs was coded entirely in ANSI C, and it was standardised, so all the test controllers were running practically identical core software, although there were three different MCU platforms used within the range of developed ISTCs as discussed in section 6.4.3. The ISTC code was partially shared with the STS; for example, the command processing routines were identical including the communication error-checking/handling functions.

The core of the ISTC software consisted of multiple state machines that were running in a continuous loop and thus operating all regular tasks of the ISTC hardware. When a command was received from the test master computer (typically from the STS), it was decoded and executed without stopping the regular tasks.

The ISTC software also provided status information to the test master PC, containing various error counter data and status bytes, including possible restarts due to watchdog events. The ISTC software proved to be a reliable design; over the five years of cumulated run, it never caused a test failure (all the detected errors were handled).

6.3.4 Raspberry Pi software

The Raspberry Pi (RPI) single-board computers [287] were used in DTC modules (DUT Temperature Controller) to perform the algorithms for the fine temperature control of the DUTs (see chapter 6.5.6).

The RPI software package consisted of the Raspbian operational system and REX control system developed by REX Controls [288]. REX is PLC-style software that allows for the design of advanced automation algorithms. The REX system could be extended by custom code blocks, which accepted the C-style code; therefore the STS code was also used on the RPI/REX software.

6.4 Test equipment

The test equipment comprised of COTS instruments and custom designed hardware including the test controllers (ISTCs). All the custom hardware was manufactured in-house. The equipment was fully automated, except for some fixed-voltage DC power supplies that were monitored by digital cameras.

6.4.1 Irradiation containers

The mechanical structures of the irradiation containers were built considering the recommendations given by the test standards as summarised in chapter 4.2.3. The inner aluminium walls were 2 to 3 mm, and the outer lead layers were 1.8 mm.

The test electronics placed in the irradiation containers was chosen to be inherently radiation tolerant; there were only passive components such as relays, resistors, and capacitors used in signal paths of the DUT interfaces. All the capacitors for the DUT decoupling were ceramics and tantalum. Both these technologies were assumed to be radiation-tolerant to TID levels used in the PhD experiments [289], [290].

6.4.2 Commercial test instruments

There were tens of pieces of various laboratory test equipment used during the development phase of the PhD research. Out of those, there were five key instruments employed by the ISTM experiments:

- DMM4050, 6.5-digit precision digital multimeter, [168]
- DMM7510, 7.5-digit ultra-precision sampling DMM with TSP, [291]
- 2611B, 200 V Source Measure Unit (SMU) with TSP, [292]
- 2420, 60 V single-channel SMU, [293]
- U2722A, 30 V USB Modular triple-channel SMU, [294]

It should also be mentioned that there was another instrument used for performing precise measurements, especially of the MOS devices *I-V* characteristics. It was the B1500A, a multichannel semiconductor analyser [295]. It was used largely for validating the test results from the ISTM test setups.

6.4.3 In-situ test controllers

The family of in-situ test controllers was developed to serve various test functionality that was not available from the COTS instrumentation including:

- Driving relays located in the irradiation containers
- Generating programmable voltages for DUT biasing
- Communicating with DUTs via SPI and UART
- Monitoring of the MIF sources
- Driving stepper motors
- Communicating with the test master via RS-232 and Ethernet
- Monitoring temperature of test equipment

There were five ISTCs built with various sets of these functionalities as per demands of the particular experiments. The ISTC hardware design was modular; hence some of the modules could be swapped between the ISTCs as illustrated in Fig. 6.6.

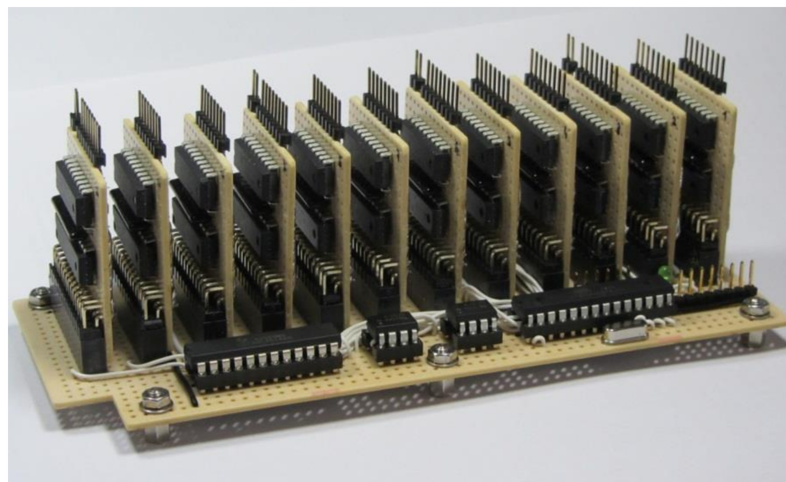

Fig. 6.6: The ISTC relay driver module with 96 channels. This module could be installed in any test controller and could also be extended as per the need of the experiment.

The MCU core modules of the ISTCs were unified for all the built controllers and were based on the STM32F407VG IC from STMicroelectronics [296]. This IC is a high-performance microcontroller with ARM Cortex-M4 32-bit core running at 160 MHz. The other modules of the ISTC were controlled directly from the core MCU, or they had their dedicated 8-bit AVR MCU by Atmel [297].

Three of the ISTC modules were built following identical mechanical design. A picture of the ISTC3 controller can be seen in Appendix C.1, which was used for the testing of the in-orbit experiment. The open/modular design philosophy was applied for the mechanical structure as well; the interior of the ISTC chassis was divided into two sections. One section was dedicated to the permanent hardware and the second (on the picture in C.1 it is shown as the upper part) could be used for special test hardware tailored to the particular experiment. The top panel (cover) could be occupied by the DTC system, which will be described in the following sections.

6.5 DUT Temperature Controller

This section outlines the development and testing of the novel DUT Temperature Controller (DTC) that was required for the in-situ TID-TC experiments as defined in chapter 5.3.2. The design of the DTC system was focused on meeting the following requirements:

- DUT temperature range: -40 to 100 °C (industrial range of COTS ICs), optionally -55 to 125 °C (military range)
- Stability of temperature control: 0.05 °C (to suppress TC-induced noise of DUTs to 1 ppm for TC = 20 ppm/°C. 1 ppm is a resolution of DMMs)
- Temperature measurement MU < 0.5 °C (for the whole range)
- Fast temperature setting/settling: < 100 s (to speed up the TID testing)
- Arbitrary temperature profiles to be generated by STS
- Ambient temperature: 15 to 35 °C (both the DTC system and irradiation container)
- Ambient relative humidity: up to 90 % RH (to be operated in the UK)
- EMC/EMI: minimum noise induced to the DUTs from the TEC
- Parts in the irradiation container to be TID-tolerant up to 150 krad(Si)
- 15 m cable length between DTC system and irradiation container

Commercial laser temperature controllers were analysed for their applicability to the DTC project as they are designed to control thermoelectric cooler modules (TECs). This solution was rejected due to various reasons. The primary problem was a high risk of EMC issues caused by the PWM (Pulse Width Modulation) technique used in the TEC power drivers. As shown in Fig. 5.5, the DUTs are attached directly to the TEC. Hence, the TEC must be driven by DC signals. Another principal risk was the length of the power cables that could be causing instabilities, as the laser controllers are designed only for local operations. Laser systems are also operated within a limited temperature range. Therefore the commercial system would have to be modified, which could be a challenge due to the limited documentation available.

Based on this analysis (and also on budget restrictions) a decision was made to develop a specialised control system.

6.5.1 DTC top-level design

The DTC system consisted of three principal parts as can be seen in Fig. 6.7. The TEC assembly was an integrated part of the mechanical structure of the irradiation container. The DTC control module contained all electronics for the measurements and control features. The TEC was powered by the TEC power drive module (TDM). The DTC was communicating with the TDM via the RS-232. The commands and data from/to the master PC were transferred via RS-232 and Ethernet buses.

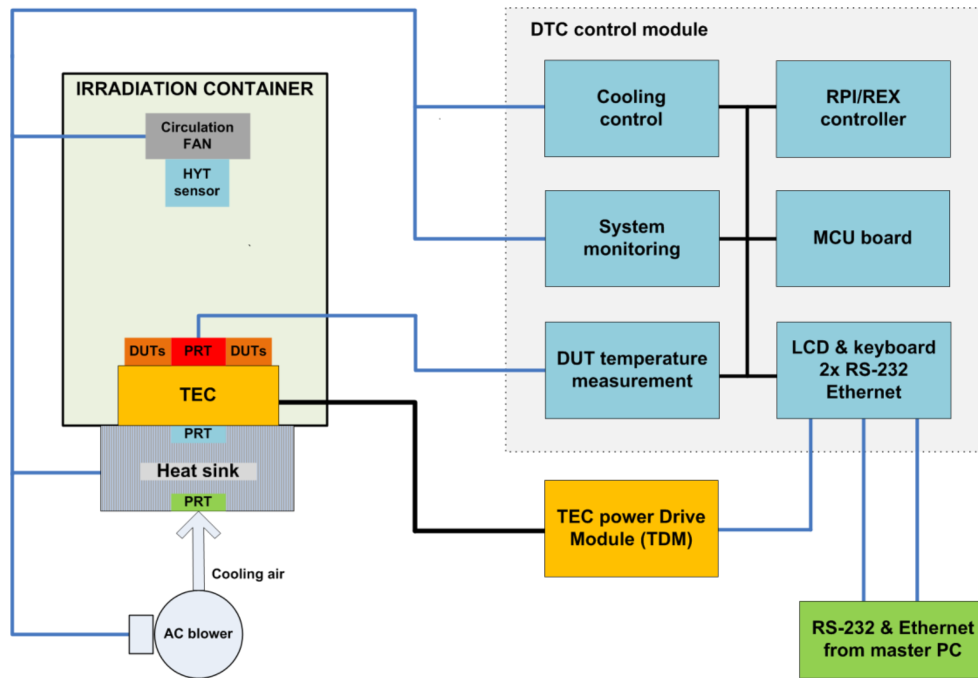

Fig. 6.7: Block diagram of the DUT temperature control system. It consisted of the TEC assembly installed in the irradiation container, DTC and TDM modules placed in the test equipment area (outside the irradiation facility).

6.5.2 DUT temperature measurement

A precise, low noise measurement of the DUT temperature was an essential capability of the DTC system. The platinum resistance thermometer (PRT) sensing technology was chosen concerning its excellent accuracy, long-term stability, and standardised temperature response [298]. Moreover, the ceramics-based PRTs were found to be inherently radiation tolerant [18], [299]. The Pt1000 sensor P1K0.232.6W.Y.010 was selected as it was the most accurate and smallest PRT available on the market [300].

The resistance of the PRT was measured by a ΔΣ ADC ADS1248, developed by Texas Instruments [301]. ADS1248 provided not only a high-performance ADC but also programmable excitation current sources for driving PRTs. Therefore the PRT could be directly connected to the ADS1248 using a four-wire connection to compensate for the resistance of the cable. The key sources of the measurement error were identified to be the drift of both the ADS1248 internal VREF and of its current source. This problem could be suppressed by application of a ratiometric circuit,

in which the excitation current flowed through the PRT, and the return current flowed through a reference resistor R_{REF}. The voltage across the R_{REF} was used as a reference voltage for the ADC [302]. This bias configuration allowed for full compensation of the excitation current drifts. It also completely removed the internal VREF from the MU budget as the R_{REF} became a primary reference device of this system. Vishay VPG supplied a custom-made R_{REF} type VHP101. This ultra-stable resistor provided absolute resistance change of lower than 10 ppm within temperature range 15 to 45 °C and long-term drift better than 2 ppm per 6 years [303].

To reduce the noise induced to both the ADC and PRT, the whole temperature measurement PCB board was physically separated from the digital part of the DTC module, optocouplers were used for galvanic isolation and separated linear DC power supplies provided noise-free supply voltages.

The calibration of the DUT measurement system was limited to an electrical calibration of the DTC module due to a limited budget. However, such a limited approach still allowed for precision temperature measurements. The electrical calibration was performed on a fully assembled DTC system, including the cables and the irradiation container. A set of precision resistors was connected instead of the PRT sensor in the irradiation container and also to the DMM4050, which acted as a calibration standard. Using ten resistors, the calibration simulated the PRT resistance for a full temperature range. This procedure allowed the DTC system to be calibrated for precision resistance measurements.

The DTC software performed high-accuracy calculations of the DUT temperature using the measured resistance of the PRT and a mathematical model of the PRT. The model was based on a high-degree polynomial interpolation of the tabulated Pt100 characteristic as defined by the standard IEC60751 [304] and the international temperature scale ITS-90 [305]. The IEC60751 also defines the tolerance windows in which the PRT was manufactured. The used PRT was of the tolerance class Y. Therefore the PRT shall not cause measurement error higher than 0.27 °C within the maximum temperature range of 100 °C [306].

The measurement uncertainty was estimated using the procedure described in chapter 2.2.2. The MU budget covered all parts of the signal chain, measured noise and temperature homogeneity across the TEC module as can be seen in the summary table in Appendix E.2.

The MU was estimated for two DUT temperatures using coverage factor k = 2:

$U_x = 0.24$ °C for $T_{DUT} = 20$ °C, respectively $U_x = 0.36$ °C for $T_{DUT} = 100$ °C

6.5.3 Selection and characterisation of the TEC modules

The selection process of the TEC module was a complex challenge. The main problem was to optimise the design of the TEC in the cooling mode. The design of the DTC required the TEC to operate in a nearly zero-power mode, in which the cold side of the TEC was only cooling negligible amount of the heat generated by the attached DUTs. The zero-power mode is not a typical application of the TECs [244]. Therefore the manufacturers provided a limited amount of data for this operational mode. It was also complicated to compare the datasheet specifications as the manufacturers did not characterise their products under unified conditions, especially at the identical TEC hot

side temperature. The cooling capability of the TEC is specified as the temperature difference dT between the TEC sides [307]:

$$dT = T_{H} - T_{C} , \tag{6.3}$$

where T_H is a temperature of the hot side of the TEC, which is attached a cooler (heat sink or a water block) and T_C is the cold side temperature. The dT is not constant; it is strongly temperature dependent [244].

Assuming the T_H could be as high as 40 °C (maximal ambient temperature plus limits of the TEC cooling system), the resulting minimal would be dT = 80 °C to achieve required T_C = -40 °C. The analysis of datasheets from various manufactures suggested that such a dT is achievable only by multistage (cascaded) TECs. The selection process was focussed on the following goals:

- Highest dT, at least 80 °C
- Lowest electrical power (to lower the power requirements for both the TEC cooling system and the TDM module)
- TEC cold side area must be large enough to accommodate the DUTs; the minimum requirement was 30 x 30 mm. This requirement limited the range of TECs to 2-stage models, as only those had cold side large enough.
- The operational temperature at least 150 °C to support the heating mode requirements with a safety/derating factor of 1.5.
- Affordable price. Each TEC was expected to be used only for a single experiment as the DUTs were glued to them. Limitation of cumulated TID levels was another attribute.

The selection criteria were met by the following 2-stage commercial TECs:

1. 19012-5L31-06CQQ, manufactured by Custom Thermoelectric [308], (USA), with dT_{MAX} = 83 °C, P_{MAX} = 93 W and T_{MAX} = 125 °C
2. MCPK2-19808AC-S, manufactured by Multicomp [309], (Russia), with dT_{MAX} = 85 °C, P_{MAX} = 137 W and T_{MAX} = 235 °C

The datasheets of these devices contained minimum data about the temperature dependency of the claimed dT_{MAX} [308], [309]. Therefore a decision was made to perform full characterisations of sample TEC devices under various cooling conditions.

During the characterisation, the TEC sample was attached to a powerful water block [310], which was supplied with a water chiller [311]. This system could maintain the T_H within ±1 °C of the programmed value. The T_H and T_C values were measured by PRT sensors, and a prototype of the TDM module controlled the TEC current. TEC current and voltage were measured to obtain a true value of TEC electrical power. This fully automated test setup allowed a precise comparison of the candidate devices as they were characterised under identical conditions.

The results from the characterisations showed the practically identical behaviour of the two candidates. Therefore the MCPK2-19808AC-S was selected due to its high value of T_{MAX}, more suitable mechanical construction (this TEC was sealed and more robust) and significantly lower price.

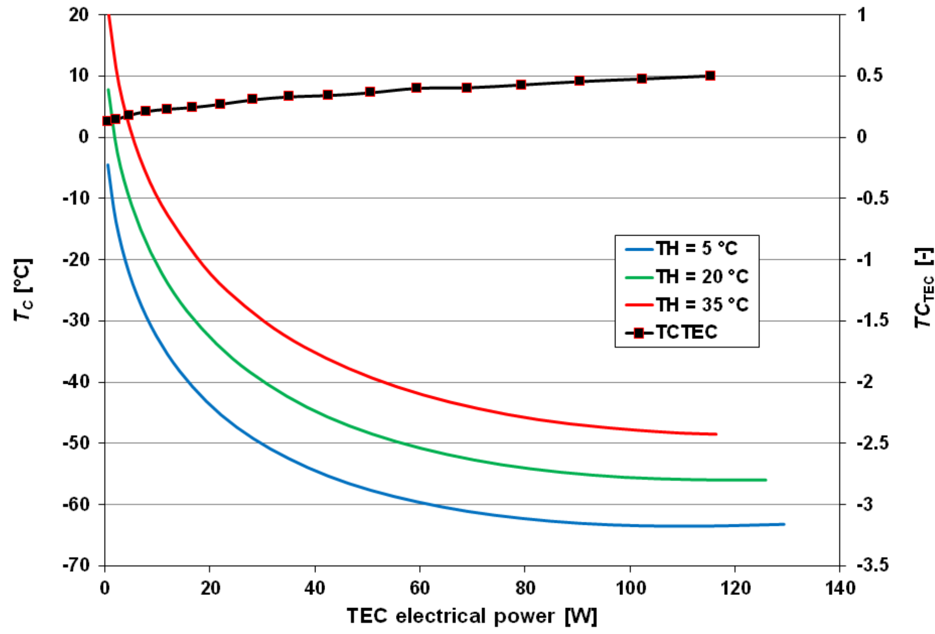

Fig. 6.8: Characterisation of the cooling capability of the MCPK2-19808AC-S TEC.

The measured characteristics of the selected TEC are shown in Fig. 6.8. The cooling characteristics were measured in three steps, with the $T_{\mathrm{H}} = 5$, 20 and 35 °C. The results showed that the TEC could reach the ideal $dT_{\mathrm{MAX}} = 85$ °C only at higher T_{H} than achieved during this experiment. The data were also analysed for the temperature dependency TC_{TEC} defined as:

$$TC_{\mathrm{TEC}} = \frac{d^2 T}{dT_{\mathrm{H}}}, \tag{6.4}$$

The TC_{TEC} is a function of the TEC power; it increased approximately by a factor of five at the maximum power. This experiment proved that with an excellent cooling system the tested TEC could provide cooling of the DUTs up to -65 °C (in this case the water cooling system was loaded only at approximately 10 % of its 1.2 kW range). It should also be noted that the characterisations were performed in open air. Therefore the performance should be even better if measured in dried air, or a vacuum.

Unfortunately, the water cooling system became unavailable during the later stages of the DTC development. It was also impractical to deploy a water system in the MIF cell. Therefore the final DTC system was based on a heat sink actively cooled with fans. This solution significantly lowered the performance of the TEC module, but the required range of -40 °C was still achievable, although only for $T_{\mathrm{A}} < 25$ °C.

The first use of the DTC during a pilot TID-TC experiment showed that the DC brushless fans were not tolerant of gamma radiation, possibly due to their Hall sensors or switching transistors. Therefore the fans were replaced with an external blower, which had to be placed outside the MIF irradiation area due to safety reasons (mains power). The pictures of the DTC system placed in MIF are in Appendices C.2 and C.3.

6.5.4 TID test of the TEC module

Another aspect of the DTC design was the radiation hardness of all critical DTC components. The TEC appeared to be the only semiconductor-based part of the hardware exposed to the radiation. The literature was searched for possible data on TID-induced changes to TEC devices, and only one paper was found [312], but no details of the TEC performance are mentioned in this work, except the fact that some degradation was observed.

The lack of TID data led to the design of a TID experiment targeted to test the cooling performance of a TEC. However, the TID test infrastructure was not capable of testing the selected TEC module at full power. Therefore a smaller TEC module (from the same manufacturer was tested [313], assuming the semiconductor technology used on the selected module was identical. The TEC was tested under constant DC current bias, attached to a heat sink, not thermally loaded (only by attached PRT sensor). The irradiation was performed at a dose rate of 36 rad(Si)/hr and the TEC was operated in a switched mode, with a period of 3 hrs. The results showed that no measurable TID-induced degradation was observed up to TID of 75 krad(Si). The later data from the real use of the DTC system during the PhD experiments also showed no degradation of the TEC modules. The results of the TEC TID experiment were presented at the RADECS 2013 conference [314].

6.5.5 TEC power driver module

The selected TEC module required a power supply voltage of 16.1 V at a current of 8.5 A. The requirement of an ultra-low EMI in combination with limited budget led to the development of a custom-built instrument, the TDM. The constant current mode design was selected to supply constant power to TEC and suppress the losses in the cables between TDM and TEC (15 m long).

The requirement of temperature stability of better than 0.05 °C within the 125 °C range was converted to a requirement of the resolution of the TDM current control. It was to be at least 0.004 %, which was achievable with a 16-bit DAC driven system. However, the initial bench experiments with TEC module assembly showed that the TEC current should be controlled with even a finer resolution; better than 0.1 mA, ideally 50 μA. Such a resolution could be provided only by 18-bit DACs.

Various concepts of linear TEC drivers were studied, including [315] and [316], and the ideal solution seemed to the “bridge-tied” driver, based on a couple of high-power OPAs. However, the development of such a power driver was expected to be a complicated effort, and a decision was made to reuse an existing MPPL design from the previous research program [317].

The MPPL (Maximum Power Point Load) was originally developed for *I-V* characterisation of photovoltaic panels. It was a programmable DC load with a current range of 10 A and 0.001 % resolution. The MPPL design was based on a single high-power MOS transistor driven by an analogue PI controller. The setpoint voltage for the PI controller was generated by 20-bit DAC controlled by an MCU.

The conversion of the MPPL to the TDM consisted of adding a DC power supply, extending the hardware by a relay-based TEC polarity control board and development of new MCU software based on the STS/ISTC software library.

6.5.6 DTC control module

Apart from the TDM module, all the DTC electronics was concentrated in the DTC control module, which was accommodating the DUT temperature measurement board, two computer board and additional systems for ensuring reliable operation of the DTC system (Fig. 6.7).

The main controller was based on the unified MCU design for the ISTCs (see chapter 6.4.3). This MCU controlled all the DTC hardware and was also responsible for all the communications with the external systems. The RPI/REX module was responsible for the execution of advanced temperature control algorithms.

The core of the RPI/REX software was a PID controller block PIDMA [288]. This advanced PID controller had two degrees of freedom. The PIDMA also provided a moment autotuning function, which was used for tuning the PID parameters. The key algorithms of the REX system have been developed by professor Schlegel, from the University of West Bohemia (Czech Republic) [318]. The RPI/REX software was created under collaboration with prof. Schlegel and his team.

The DTC control module also contained hardware for control and monitoring of the cooling system and other parts of the DTC system. The DTC software was designed to protect the TEC and DUTs. The protection system was based on continuous monitoring of various temperatures, TEC power, trends in TEC power and others, including the data integrity on crucial communication lines. The DTC system would switch to a safe mode in case of the activation of the protection system.

The mechanical part of the DCT control module was designed to be compatible with the ISTC chassis; hence it could be attached to any of the three ISTCs. A picture of the final version of the DTC control module hardware is shown in Appendix C.4.

6.5.7 DTC operation in the irradiation container

The irradiation container had to contain a dry-air atmosphere to prevent the build-up of the frost, which would have lowered the cooling performance of the TEC module and possibly degrade the DUT measurements. Therefore the irradiation container was hermetic, and silica gel bags were used to keep the humidity on negligible levels. This process also contained thermal desiccation of the silica gel bags in a thermal chamber before the installation into the container.

The humidity and temperature of the ambient air in the irradiation container were measured by the HYT sensor [319] to validate the container was hermetic, and the inner atmosphere was within limits. There was also a circulation fan inside the container to accelerate the initial drying of the inner atmosphere. Both the HYT sensor and the fan contained semiconductors; therefore they were monitored by the DTC control module to ensure they would be safely isolated in a case of TID-induced failure. This protection feature was found practical as both devices typically failed at TID levels between 20 and 30 krad(Si). This controlled failure of the HYT and fan did not compromise the performance of the DTC system; these devices were required to be functional only during the final assembly of the irradiation container and pre-irradiation phase of TID experiments.

6.5.8 Testing of the DTC system

The testing of the DTC system was performed at all stages of the development process and typically on the subsystem level. There was a series of tests performed to measure the performance of the system and also to validate its functionality, including:

- Tuning the PID controller for optimum static and dynamic performance
- Testing the protection system for various failure modes and their combinations, including communication errors
- Static test (temperature control stability)
- Dynamic test (response to a change of temperature setpoint)
- Test of the accuracy of the DUT temperature measurement
- Test of cooling capability (the impact of the temperature of the ambient air)
- Measurement of the inner atmosphere

The static test was performed at multiple stages of the development, but the most crucial was the final test, during which the STS recorded the DUT temperatures in a fully assembled experiment. The setup included all the cables, and it was placed in the MIF facility under the same condition as during the irradiation. The result of the static test during the pre-irradiation phase of the pilot PMOS experiment is shown in Fig. 6.9. The histogram was constructed from 34000 random samples taken from the STS records of two days. The DTC was commanded to maintain the DUT temperature at 20 °C. While 94 % of measurements lied within ±0.01 °C window, 99.8 % of measurements were within ±0.02 °C. This test demonstrated the excellent stability of the DTC system. It should be noted that this precise statistical analysis showed a slight offset in the DUT temperature (approximately 0.002 °C), which could be caused by imperfections in the settings of the PID controller.

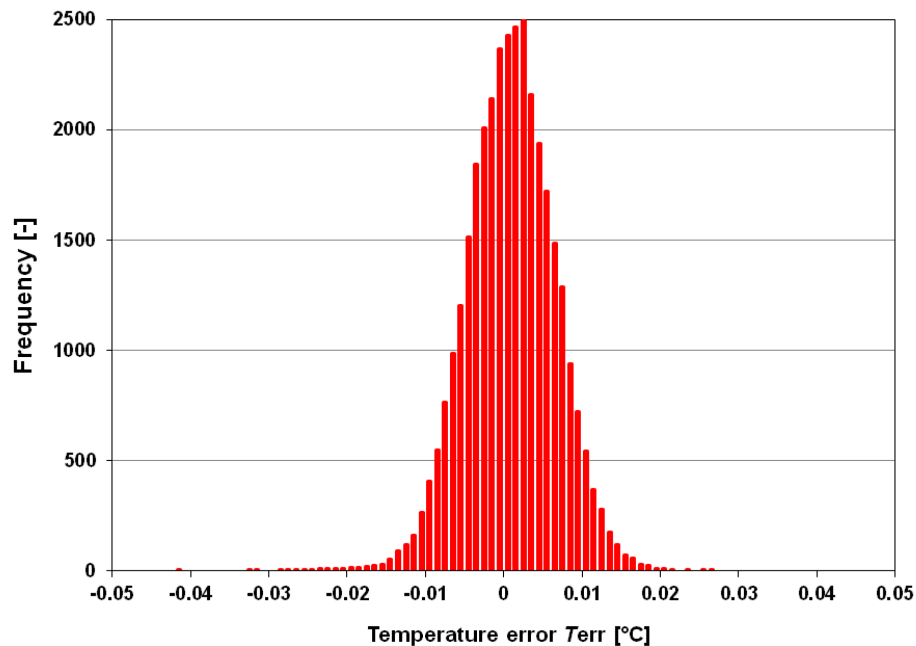

Fig. 6.9: A histogram of DUT temperature error constructed from 34,000 DTC temperature measurements.

The estimated measurement uncertainty of the DUT temperature measurements could not be verified by a proper test in calibrated temperature oven due to budget limits. However, the electrical calibration procedure (as defined in chapter 6.5.2) was performed before each experiment. After two years of the practical usage of the DTC system, the original calibration was verified with a higher class multimeter, the DMM7510. This independent test showed that after two years the DUT measurement system drifted less than 0.1 °C. This observation was in a good agreement with the MU estimation for the electronics of the DUT temperature measurements.

The dynamic testing was performed by acquiring DTC data of DUT temperature and by measuring the temperature of a DUT (8-lead SOIC package attached to the TEC) with a high-resolution thermal camera FLIR [320]. The measurements of a step change of the DUT temperature from 20 to 40 °C are shown in Fig. 6.10. At the time t = 0 s the DTC was commanded to set the temperature to 40 °C, and it took 30 s for the temperature measured by DTC to stabilise. However, the FLIR measurements of the DUT package showed that DUT's surface temperature stabilised at t = 50 s. This experiment proved (by use of a different sensing technology) that the dynamic parameters of the DTC systems are better than required by the planned experiments.

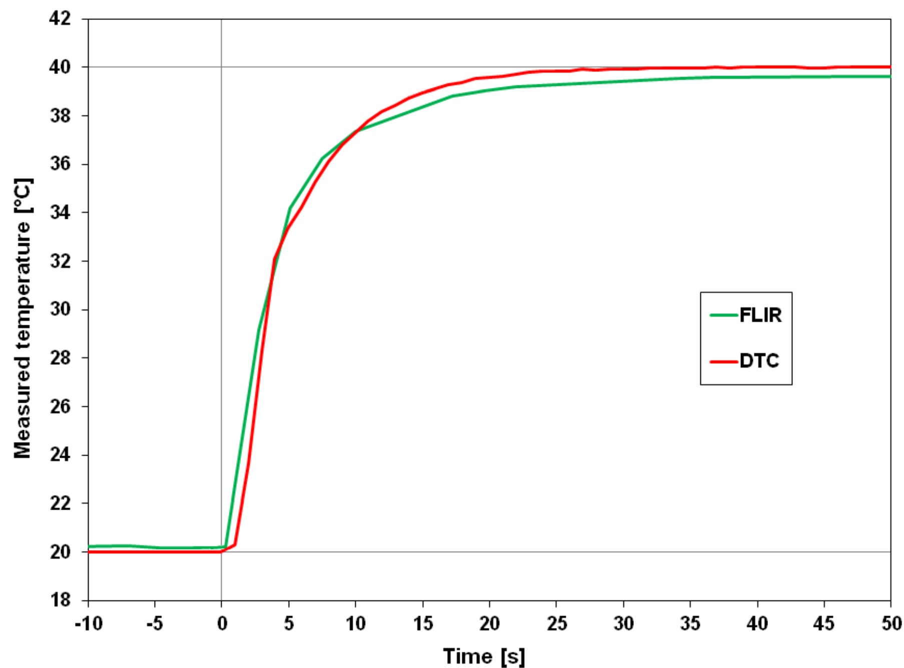

Fig. 6.10: A dynamic test of the DTC system. Data from DTC and FLIR camera were plotted.

6.5.9 ISTC mini-oven

The development of the DTC system was a complex effort, which resulted in a fully functional set of equipment and software that was proven to work as required by the research plans. The success of this project led to a decision to further explore the potential of the DTC technology by building an experimental mini-oven, which could be used for operating ultra-high precision electronics at a constant temperature.

The oven would be operated at a constant elevated temperature, for example at 40 °C. Such a temperature level can be kept by a heating-only system. This principle of temperature stabilisation is an industry-standard technique for stabilising crystal oscillators. This technology is called OCXO, or oven-controlled crystal oscillator [321]. However, the oven-controlled stabilisation was not found to be used in precision DC electronics for DAQ systems, except for the LTZ1000 ultra precision VREF [183].

The experimental mini-oven was designed to be compatible with the ISTC design; it could be placed in the ISTC in the section dedicated to the test-specific hardware. A prototype of the oven is shown in Fig. 6.11 (the oven was installed in the ITSC, but the insulation blankets were not installed yet). The heating and circulation of the air were provided by a miniature fan-heater module whose power was controlled by an OPA. The OPA was attached to the body of the heater. Therefore the heat produced by the OPA was also used for heating the oven. The DTC control module was extended to support the oven in parallel with the control of the DUT temperature.

The initial tests, during which an ADC module was placed in the oven as an example “payload”, showed that the temperature was kept within ±0.2 °C. It should be noted, that the mini-oven was still not perfectly thermally insulated during this test, so even better results can be expected.

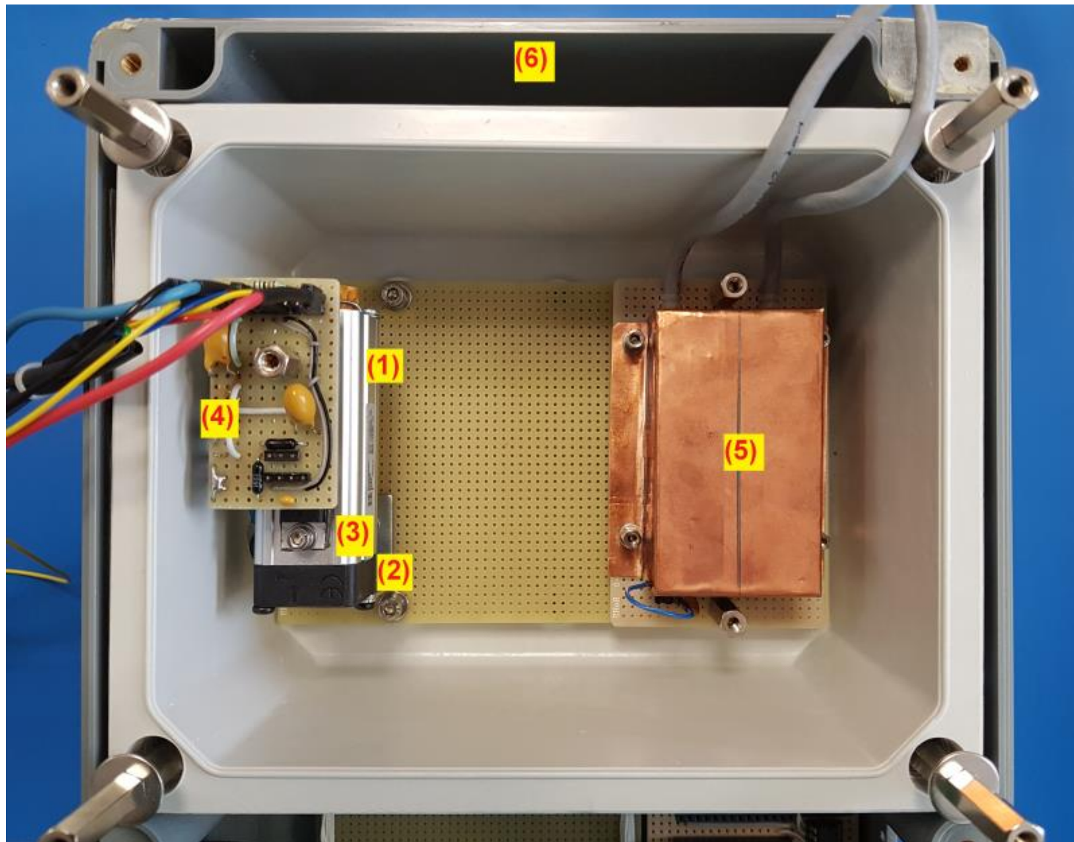

Fig. 6.11: Interior of the mini-oven prototype. The heater (1) was ventilated by the fan (2). The heater power driver OPA (3) was attached to the body of the heater and hardwired to the control board (4). An ADC module (5) simulated the hardware to be oven-controlled. The mini-oven was installed in the ISTC controller (6).

7 MOS TID EXPERIMENTS

The first series of radiation experiments were performed on MOS devices, and the results are summarised in this chapter. The MOS experiments were focused on TID effects on commercial PMOS transitions and RADFETs including TID-induced changes of their temperature dependence.

7.1 Objectives of MOS TID experiments

The complex theory of TID-induced changes in MOS technology has been published as discussed in chapter 3.3. However, the reported TID data were not comprehensive enough. Therefore a series of experiments was performed to meet the following objectives:

1. Measurement of TID-induced threshold voltage shift (responsivity) of commercial PMOS transistors to be used as DUTs and backup TID detectors in the in-orbit experiments
2. Measurement of TID-induced changes of *TC* of PMOS transistors to both demonstrate the ISTM test system (including the DTC system) and obtain TID-TC data for the in-orbit experiments
3. Measurement of RADFET TID responsivities and their TID-TC response
4. Investigation of various bias conditions and their impact on TID responsivity of MOS devices

7.2 COTS PMOS TID-TC experiments

There were two TID experiments performed during which COTS PMOS transistors were irradiated:

- PMOS1: this was a pilot TID-TC experiment focused on validation of the whole ISTM test system and acquisition of initial PMOS TID-TC data. The PMOS1 experiment was prematurely interrupted due to problems with the test system.
- PMOS2: a full TID-TC experiment using an upgraded test system and an alternative DUT characterisation method.

Tab. 7.1: Specification of PMOS DUT ZVP1320FPA, data from [322].

Parameter	Value
Manufacturer	Diodes Incorporated
Package	SOT23
Maximum continuous drain current	-35 mA
Maximum gate-source voltage	±20 V
Maximum drain-source voltage	-200 V
Operating/storage temperature	-55 to 150 °C

7.2.1 The PMOS devices under test

For both PMOS experiments, sets of twenty commercial PMOS transistors of type ZVP1320FPA were used. The key transistor parameters are summarised in Tab. 7.1. This type was chosen due to its very low drain current, which made it the lowest power discrete PMOS transistor available on the market. Therefore it was the most similar commercial PMOS transistor to the RADFETS used in previous works [263], [268], [269]. No further DUT production details were available apart from the specification in the datasheet [322]. The DUTs were delivered in the original reel. Therefore it was assumed that the parts were from the same lot. To measure the bias sensitivity of the threshold voltage shift and the *TCs*, the DUTs were divided into five bias groups as defined in Tab. 7.2.

Tab. 7.2: Definition of the bias conditions of the PMOS experiments.

Bias group	DUT numbers	Bias voltage [V]
1	DUT01 to DUT04	0 (GND)
2	DUT05 to DUT08	3
3	DUT09 to DUT12	5
4	DUT13 to DUT16	12
5	DUT17 to DUT20	18

7.2.2 The test system for the PMOS experiments

The ISTM test system was based on the 2611B SMU (see section 6.4.2), which performed all measurements. The SMU was combined with a custom-made test controller ISTC1 (chapter 6.4.3). The ISTC1 provided relay drivers, programmable DUT bias voltage sources and monitoring of the MIF sources. Both the SMU and the ISTC1 were commanded by the test PC. The DUT temperature controller DTC ran independently but was synchronised with the PC every second.

For most of the irradiation time, the DUTs were in the "exposure" mode, i.e. drain (D) and source (S) were grounded, and gate (G) was connected to the relevant bias voltage source via a 100 kΩ resistor (see Fig. 5.8 a) for details). Each bias voltage was generated by an independent circuit consisting of a 16-bit D/A converter followed by an amplifier with low offset voltage and capability of driving high-capacitance loads (cables to the MIF cell). The bias voltages were measured by the SMU and were kept within ±1 mV by programming the D/A converters. These measurements were performed at the beginning of each DUT measurement cycle. The STS software was able to correct bias voltage if it was outside the ±1 mV window. However, this situation was not recorded.

Regular *I-V* curve measurements were made either at the idle temperature of 20 °C or during the temperature sweep, as defined in Fig. 7.1. The DUTs were subsequently switched from "exposure" mode to "reader" mode, during which G and D were grounded, S was driven with a constant current from the SMU, and the S-D voltage (equivalent to DUT V_{GS} voltage) was measured (see chapter 5.4.3 for details). Sixty current steps were measured from 10 µA to 35 mA. The DUT multiplexing was done via mechanical relays placed in the DUT container near the DUTs. A measurement of

one *I-V* curve took 7.5 seconds and, in contrast to [268] and [269], there were no additional delays between setting the drain current and measuring V_{GS}. The main reason for such a fast measurement was to reduce the time during which the DUTs were exposed to elevated temperatures.

The main sources of measurement error were related to the SMU accuracy. The vendor specified the SMU current source accuracy as 0.03 % of reading + 30 µA and the voltage measurement accuracy as 0.02 % of reading + 5 mV [292]. The SMU was connected using a four-wire circuit, and thus the influence of the cables was minimised.

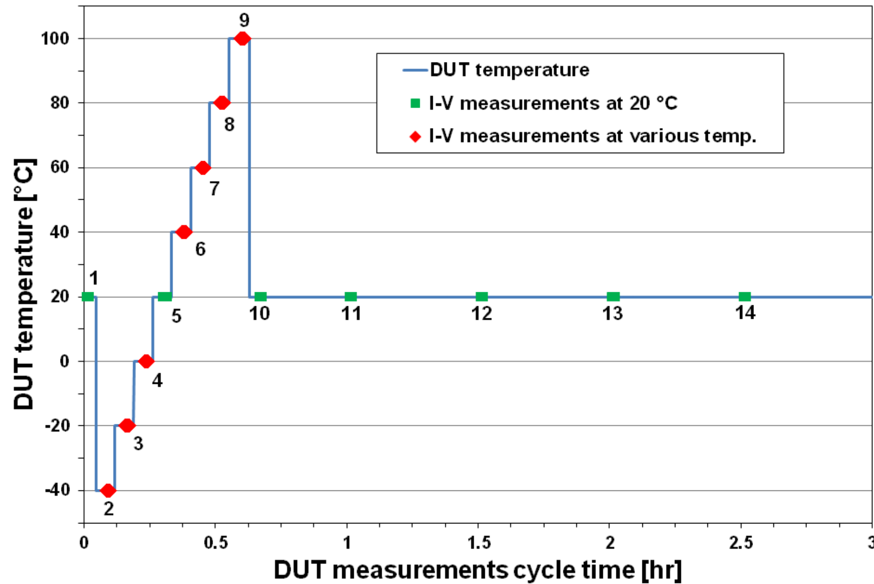

Fig. 7.1: The timing of the DUT measurement cycle, including the temperature profile. DUT *I-V* curves were measured at 20 °C every 30 minutes during the idle time (green squares) and at various temperatures during the temperature sweep (red dots). The temperature sweep started with DUT cooling down mode and continued with the DUT warming up mode. Notable is an *I-V* measurement at the idle temperature between these two modes (no. 5).

The DUTs were attached to the TEC using thermally conductive glue (silver-epoxy compound). To minimise thermal bridges, the DUTs were connected to the multiplexing boards via 100 µm wires. Pictures of the PMOS experimental hardware can be seen in the Appendices D.1and D.2.

7.2.3 The irradiation plan of the PMOS experiments

The MIF cell was used for the irradiation phase of the PMOS experiments. A dose rate of 360 rad(Si)/hr was used. The dosimetry was performed only prior to the irradiation. There was no dosimetry during the experiment as the mechanical structure of the DUT container did not allow the ion chamber to be placed permanently in the container. See sections 6.1 and 6.2 for details.

7.2.4 PMOS1 experiment idle temperature results

As expected, a TID-induced threshold voltage shift ΔVT was observed for all DUTs. Results for the most sensitive DUTs, using only those data points taken at the idle temperature of 20 °C, are shown in Fig. 7.2.

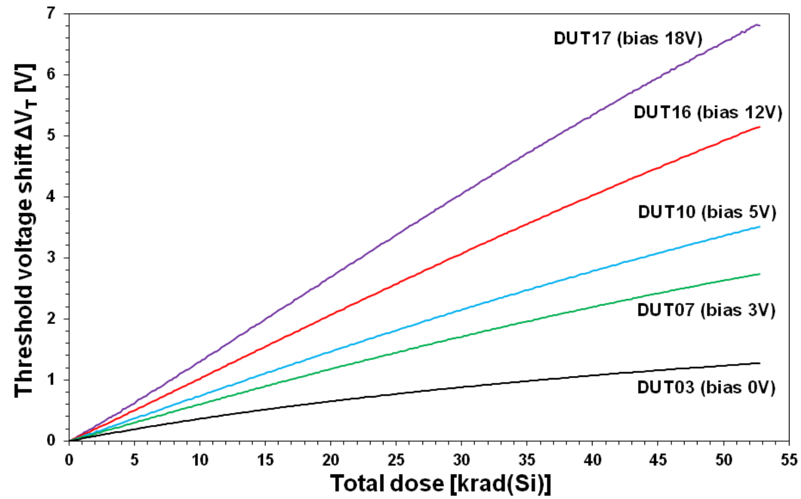

Fig. 7.2: Experiment PMOS1 threshold voltage shift ΔV_T at a drain current of 1 mA plotted as a function of the total dose for selected DUTs at the idle temperature of 20 °C.

The plotted ΔV_T curves were not smooth - a small but consistent ripple can be observed on all DUTs. This effect was one of the problems expected as the DUT temperature was cycled regularly during the irradiation.

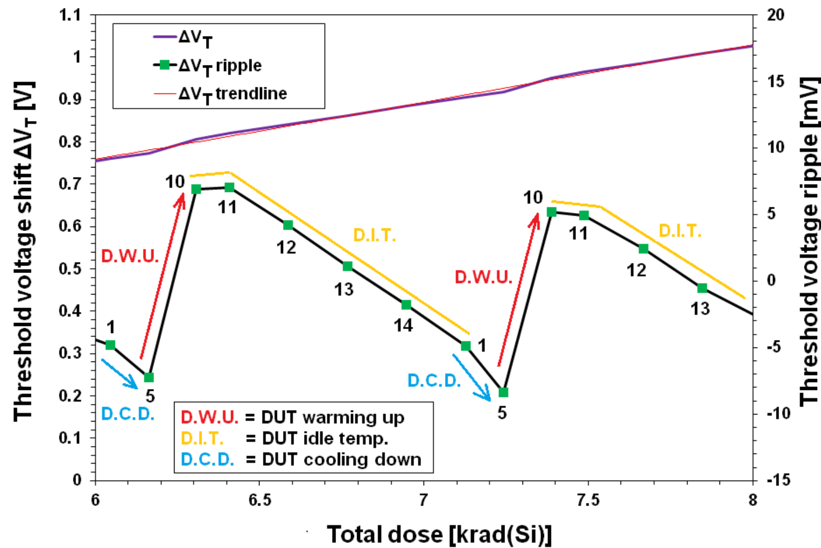

Fig. 7.3: Detail for PMOS1 DUT17 recorded over two DUT measurement cycles, showing that the temperature sweeps significantly alter the ΔV_T values. The ΔV_T curve was fitted with a polynomial function, which was subtracted from the ΔV_T curve to obtain the ripple on it. DUT measurement numbers were added to show the timing.

To analyse this problem, the ripple was "demodulated" from the ΔV_T curves and analysed concerning the timing and DUT temperature profile of the measurement cycle (Fig. 7.3 versus Fig. 7.1). The resulting plot shows that the ripple has an obvious positive temperature dependency. The ripple was not caused by the test method as it was not observed during the pre-irradiation measurements.

The chart in Fig. 7.4 shows the bias voltage dependency of the TID responsivity of the DUTs. A linear regression algorithm was used to calculate the responsivity of each DUT and a coefficient of determination (R^2) was used to compare the linearity of DUT responsivities. A significant difference in R^2 between unbiased and biased devices can be seen.

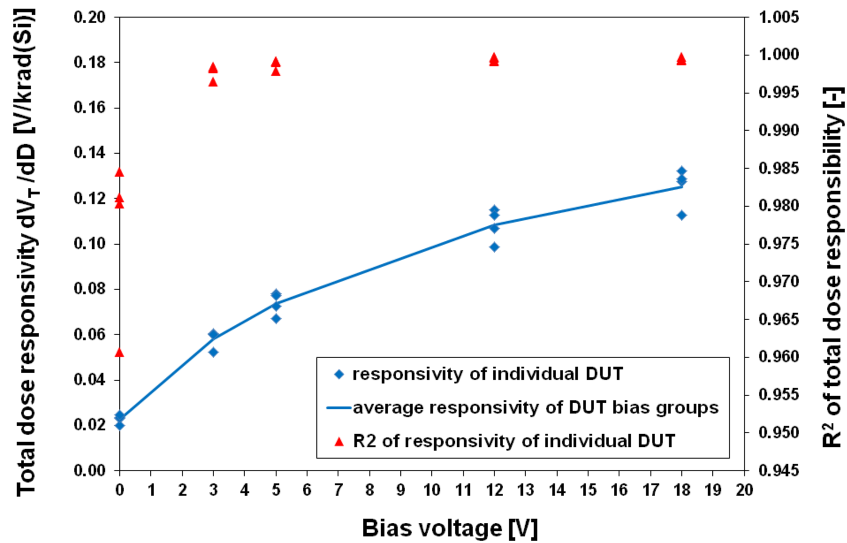

Fig. 7.4: Gate bias voltage dependency of the DUT total dose responsivity as measured during the experiment PMOS1. The individual responsivity of each DUT is plotted as a blue square marker; the blue line represents the average sensitivity of each DUT bias group. The red triangles show the R^2 value for individual DUT responsivities.

7.2.5 PMOS1 experiment temperature sweep results

As shown in Fig. 7.1, temperature sweep *I-V* curves were measured every three hours (*I-V* 2 to 9), which represents an accumulated dose of 1.08 krad(Si) per measurement cycle. In total, seven temperature steps were used to measure:

- The temperature coefficient of the DUT threshold voltage TC_{VT} [mV/°C]
- The *MTC* point, which represents the value of the drain current at which the magnitude of the TC_{VT} is minimised [mA].

The histogram in Fig. 6.9 shows that excellent stability of the DUT temperature control was achieved during the steady moments of the measurements. The accuracy of the *TC* measurements was also improved by the fast response of the DUT temperature controller, allowing compensation of the DUT self-heating. During the *I-V* curve measurements, the stability of the TEC temperature was measured to be within a window of ±0.05 °C. Fig. 7.5 shows a typical record of a DUT temperature sweep measurement.

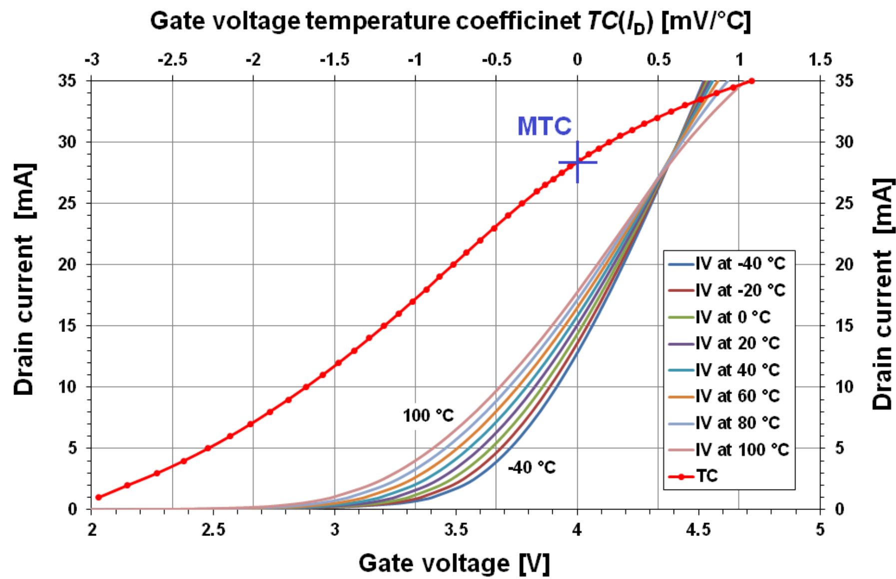

Fig. 7.5: Temperature sweep *I-V* measurements for DUT01 prior to the irradiation of experiment PMOS1. The gate voltage *TC* is plotted as a function of I_D (red line); the red markers show the size of I_D steps. The *MTC* point was at the zero value of the *TC* curve, which was equivalent to I_D at which the *I-V* curves were crossing other.

TID-induced changes in the TC_{VT} were determined at a drain current of 1 mA using 53 measured *I-V* curve data sets. The resulting traces of selected (most sensitive) DUTs shown in Fig. 7.6 exhibit a significant gate bias voltage dependency as well as an initially reversed polarity of the TC_{VT}. The TID-induced changes of the *MTC* points were obtained from the same data using interpolation of two lowest points of the $TC(I_D)$ curves. *MTC* measurements exhibited similar effects to TC_{VT} (Fig. 7.7).

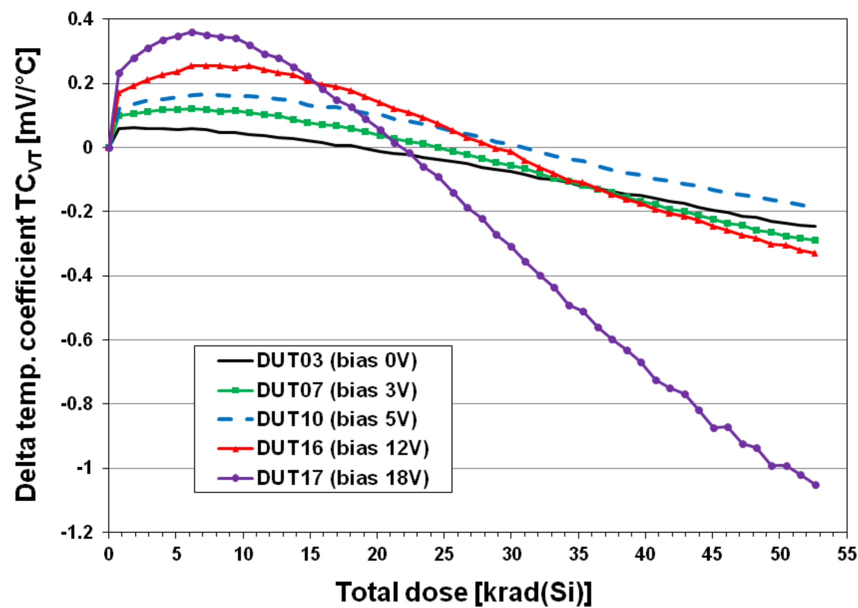

Fig. 7.6: TID-induced changes of TC_{VT} at 1 mA drain current during experiment PMOS1. The markers on the DUT17 curve show the TID resolution of the measurements.

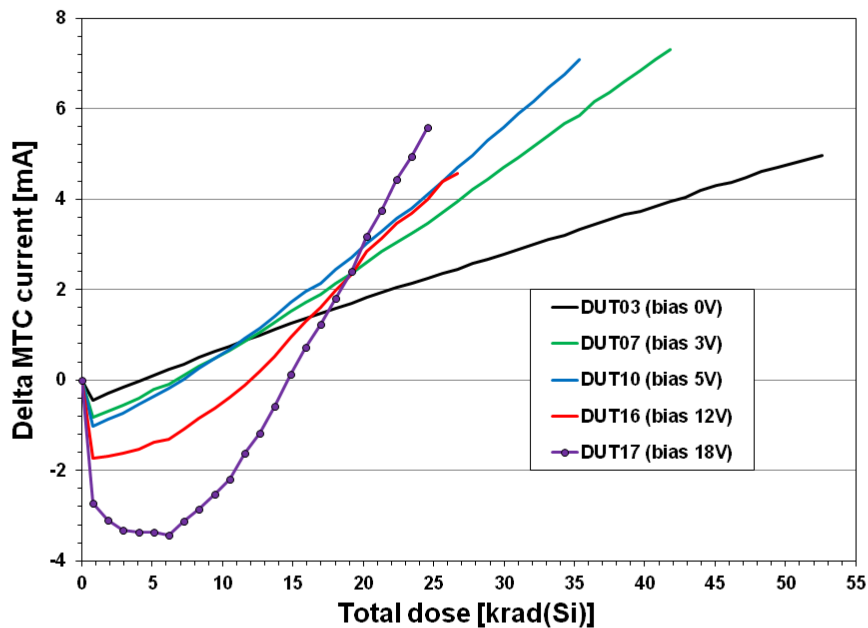

Fig. 7.7: Experiment PMOS1 TID-induced changes of selected DUTs *MTC* points. The markers on the DUT17 curve show the total dose resolution of the measurements. The results were limited by the DUT drain current range of 35 mA. The pre-irradiation *MTC* points ranged from 28 to 32 mA (initial DUT to DUT variation).

7.2.6 Upgrades to the tests system for the PMOS2 experiment

During experiment PMOS1, a fault developed after a total dose of 53 krad(Si) rendering the *I-V* data at higher doses invalid (the voltage readings at $I_D > \sim 10$ mA were unstable). To investigate this problem, the DUT container was taken out of the irradiation facility, and the DUTs were bench characterised using the Agilent B1500A semiconductor analyser working in the gate-voltage sweep mode. *I-V* curves measured by the B1500A were normal. The B1500A was later connected instead of the SMU and programmed to mimic the *I-V* curve measurement used in the PMOS1 experiment, and the results were also faulty. It is believed that the cause of this problem was the limited ability of the SMU to drive high capacitive loads (the 15 m cables and the hardware in the irradiation container). A decision was made to upgrade the measurement system for a classical, gate voltage sweep *I-V* curve measurement system and repeat the experiment using a second set of new DUTs that were delivered on the same reel as those used for the PMOS1.

The original test system was extended by adding another SMU (Keithley 2420) to provide a programmable gate voltage source. The SMUs were linked together using synchronisation signals, and a sophisticated embedded test script was developed to allow fast, high resolution, *I-V* curve measurements. Due to this fast embedded control method (see chapter 6.3.2), the duration of a single *I-V* curve measurement remained the same at 7.5 s. The step size of the gate voltage sweep was 50 mV, and the drain voltage was 15 V during the *I-V* curve measurements. The second measurement method was validated using the irradiated DUTs from PMOS1 and the *I-V* curve data obtained using the B1500A.

The constant drain current method used in experiment PMOS1 allowed the exact programming of the *I-V* curve drain current range. The second method, using the gate voltage sweep, had to be programmed to follow the TID-induced changes in the *I-V* curves continuously. A tracking algorithm was developed to cover this issue: the gate voltage sweep range was calculated prior each *I-V* curve measurement using a trend of a fixed *I-V* curve current point of 30 mA obtained during three previous measurements. The resulting gate voltage sweep range was then extended by 10 % to include a safety margin. This margin helped the algorithm to start smoothly and also compensated for the moderate flattening of the *I-V* curve caused by the TID-induced lowering of the *I-V* curve slope (see Fig. 3.4). This feature was implemented to the STS; the embedded *I-V* curve test script was updated, prior to each *I-V* curve measurement, individually for each DUT. In the case of any problem, a manual adjustment of the algorithm was possible during the experiment. The STS continuously checked the measured *I-V* curves to warn in case of any failure of the algorithm. The timing of the measurements, as well as the temperature profile, remained the same, so the results from experiment PMOS2 could be directly compared to those from experiment PMOS1. The main sources of measurement error were related to the SMU accuracy as for during the experiment PMOS1. The vendor specifies the SMU 2611B current measurement accuracy as 0.02 % of reading + 20 μA and the SMU 2420 voltage source accuracy as 0.03 % of reading + 3.2 mV.

7.2.7 PMOS2 experiment idle temperature results

Data for total dose up to 150 krad(Si) were analysed from experiment PMOS2. The data were analysed the same way as the results from experiment PMOS1. The data analysis software had to be updated; it employed a high-degree polynomial curve fitting algorithm to obtain the gate voltage values equivalent to the same drain current steps as during experiment PMOS1.

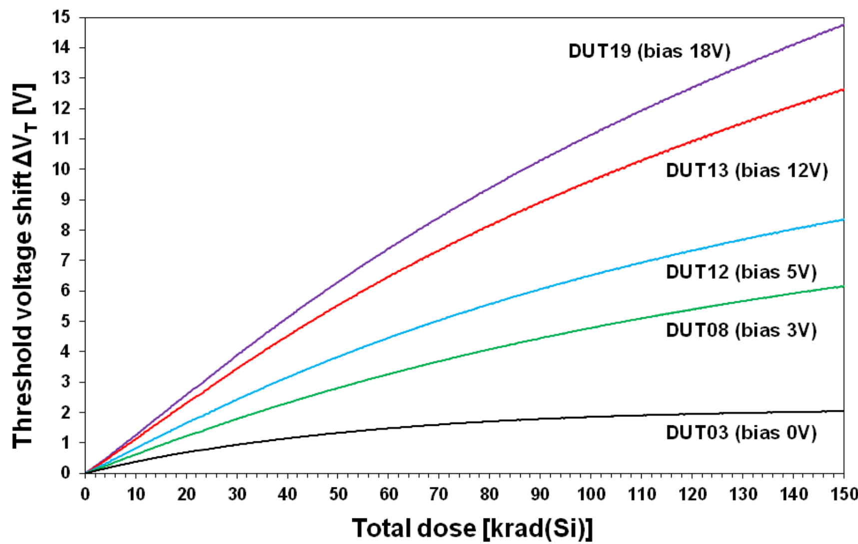

Fig. 7.8: Experiment PMOS2 threshold voltage shift ΔV_T at a drain current 1 mA plotted as a function of the total dose for selected DUTs. All measurements plotted here were taken at the idle temperature of 20 °C.

The TID-induced threshold voltage shift ΔV_T was again observed for all DUTs. A record of the most sensitive DUTs in experiment PMOS2, taken at the idle temperature, can be seen in Fig. 7.8. The initial shifts (up to approximately 50 krad (Si)) in the plotted ΔV_T curves were linear; for doses above this the sensitivity was reduced, and the unbiased DUTs were already saturated at 150 krad(Si). The initial DUT response was nearly identical to the response measured during the experiment PMOS1. The observed ripple was very similar to the ripple measured during the experiment PMOS1 (Fig. 7.3).

7.2.8 PMOS2 experiment temperature sweep results

The temperature coefficient results from experiment PMOS2 were analysed to obtain plots comparable to those from experiment PMOS1. The TID-induced changes of TC_{VT} were very similar for DUTs within each DUT bias group; therefore average values for each bias group were plotted (Fig. 7.9).

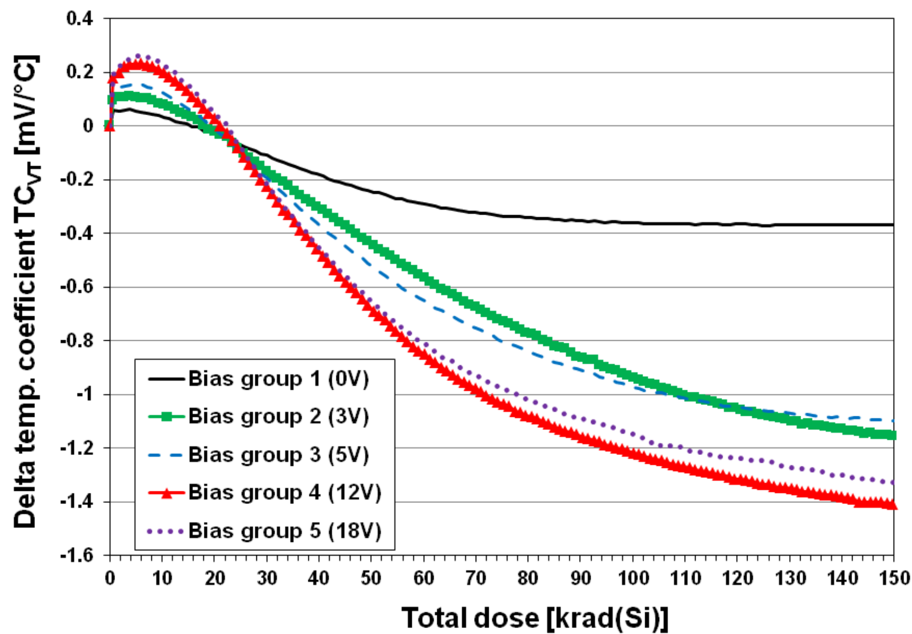

Fig. 7.9: Experiment PMOS2 TID-induced changes of TC_{VT} at 1 mA drain current plotted as an average value for each DUT bias group (four DUTs per group).

The resulting chart shows again that the initial TC_{VT} values were positive and, at a total dose of approximately 23 krad(Si), changed to a negative trend. While the initial positive response had a consistent positive bias dependency, the bias dependency of the negative trend was a more complex function. The initial peak positive TC_{VT} was measured at a total dose of 5 krad(Si), and a bias dependency function was plotted for this particular total dose (Fig. 7.10). The resulting quasi-linear curve was very similar to the bias voltage dependency of the DUT total dose responsivity as measured during the experiment PMOS1 (Fig. 7.4).

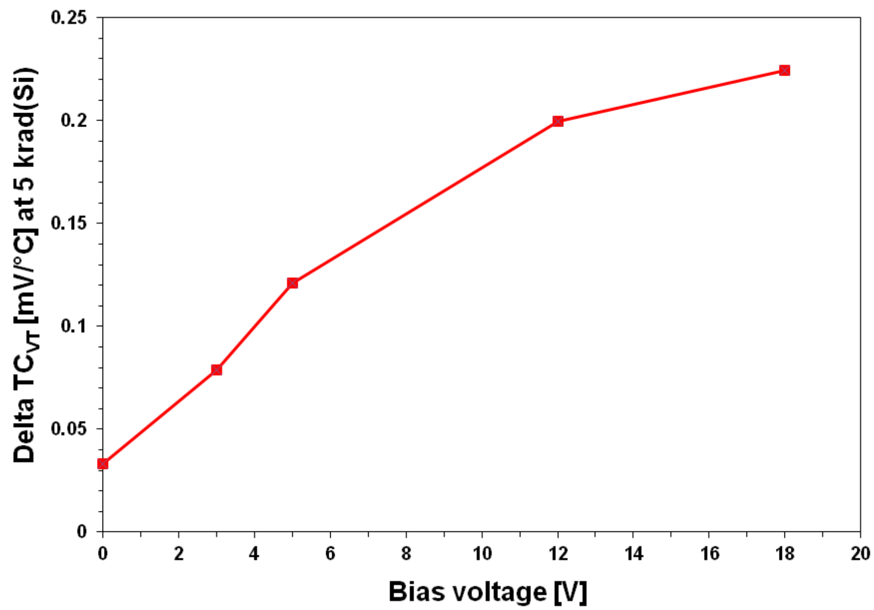

Fig. 7.10: Experiment PMOS2 TID-induced changes of TC_{VT} at 1 mA drain current as a function of bias voltage at the total dose of 5 krad(Si). This chart shows a strong bias sensitivity of the initial (positive) change of the TC_{VT}.

The chart in Fig. 7.11 shows the TID-induced shift in the results of the *MTC* point during experiment PMOS2. The initial negative region was strongly bias dependent, and the peak values were measured at a lower dose of 3 krad(Si).

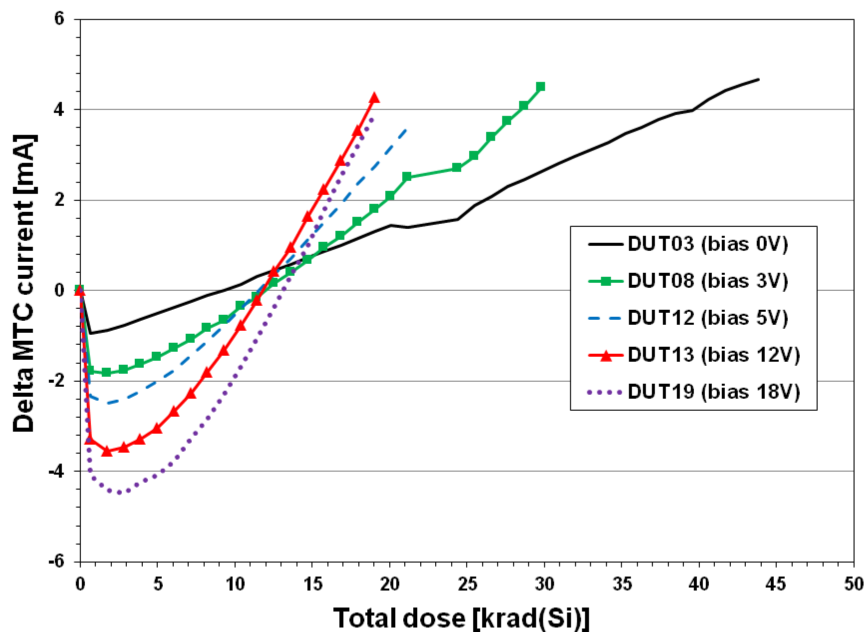

Fig. 7.11: Experiment PMOS2 TID-induced changes of selected DUTs *MTC* points. The results are limited by the drain current range of the DUTs of 35 mA. The pre-irradiation *MTC* points ranged from 29 to 32 mA (initial DUT-to-DUT variation).

7.2.9 Discussion of PMOS experiments results

The PMOS experiments demonstrated an in-situ test method developed to perform TID experiments and to observe TID-induced changes in temperature effects on a sufficient number of samples. Since there were no radiation test data published for the ZVP transistor series, it was not possible to validate the obtained results. However, the results of this experiment were comparable to data obtained from RADFETs as published in previous papers, including [265]. *I-V* data, collected during the two experiments, showed very good repeatability of this ISTM test system, even if two different *I-V* curve measurement methods were used.

As expected, a strong dependence of all measured parameters on the gate-bias conditions was observed. There was a good agreement of the observed threshold voltage shift bias dependence with irradiation curves published in Fig. 2 of [269]. A significant difference in responsivity was observed between the DUTs (scatter of the blue markers in Fig. 7.4). It is believed that it was not caused by the test method; the variation of the dose-rate across the miniature area of each bias group was negligible, as well as the bias conditions were uniform within each bias group. The DUT-to-DUT variability was probably caused by the limited reproducibility of the manufacturing process [246].

The initially reversed polarity of both the TC_{VT} and MTC curves was not in agreement with the published data for RADFETs (Fig. 20 in [263]). However, the RADFETs are special MOS devices as discussed in chapters 3.5.3 and 5.4.3. This effect was nearly invisible in the unbiased DUTs. Another interesting result was the positive temperature dependency of the ΔV_T ripple observed on all DUTs. It cannot be explained as concurrent thermal annealing, which was expected to have a negative temperature dependency. Hence the presented data showed temperature accelerated ΔV_T (as outlined in chapter 3.9.1). Moreover, the results of the ESAPMOS4 RADFETs testing, also suggested that the influence of temperature strongly depends on the dose rate (Fig. 2 versus Fig. 3 in [323]).

The *I-V* curves measured during the temperature sweeps were not symmetrical around the *MTC* point; while the V_{GS} temperature dependency was linear for drain current below *MTC*, it became non-linear above it (Fig. 7.5). This observation was not in agreement with the RADFET result published in [268], Fig. 1. Also, the simulated n-channel MOS device shown in Fig. 3.22 exhibited symmetrical behaviour around *MTC* point. A possible explanation was a self-heating of the DUT during the *I-V* curve measurement. The RADFETs tested in [268] had a drain current two orders of magnitude lower than the COTS transistors used in this work. This problem was investigated during the B1500A bench tests of the irradiated DUTs from experiment PMOS1. The DUT was still attached to the thermoelectric cooler, and the DUT temperature controller was set for 20 °C. A reversed gate voltage sweep measurement was made, and the resulting *I-V* curve was practically identical to the *I-V* curve from a normal gate voltage sweep. It is believed that this bench test proved that the temperature control is very effective in compensating for the self-heating of the DUT during the *I-V* curve measurement. Therefore, the observed non-linear behaviour above the *MTC* point was most likely a true behaviour of the tested transistor and not an artefact of the measurement method.

The early results of the PMOS experiments were presented at the NSREC 2015 conference, and an extended paper was published in the IEEE-TNS journal [324].

7.3 RADFET TID-TC experiment

RADFET research started after the completion of the PMOS experiments, which successfully validated the performance and reliability of the novel TID-TC test system.

7.3.1 The RADFET devices under test

For the experiment, a set of fifteen Tyndall RADFETs (DUT01 to DUT15) of type TY1003 was used [325]. TY1003 is a Tyndall RADFET chip denoted "COMRAD", packaged in a plastic six lead package SOT23-6. The part consists of two identical p-channel RADFETs (R1 and R2) and a temperature sensing diode. The RADFET gate oxide thickness is 400 nm, and W/L is 300/50 µm. The two RADFETs have individual gate and drain terminals, while the source and bulk are common and connected together; this is also the diode bulk contact. Only the RADFET R1 of each chip was tested; the other pins were left unconnected. The RADFETs were irradiated under five bias conditions as defined in Tab. 7.3.

Tab. 7.3: Definition of the bias conditions of the RADFET experiment.

Bias group	DUT numbers	Bias voltage [V]
1	DUT01 to DUT03	0 (GND)
2	DUT04 to DUT06	2.5
3	DUT07 to DUT09	5
4	DUT10 to DUT12	7.5
5	DUT13 to DUT15	10

7.3.2 The setup of the RADFET experiment

The test system was practically identical to the system used in the PMOS2 experiment. However, the *I-V* curves were measured using a single SMU 2611B operating in the current mode as described in section 7.2.2. The motivation for the employment of this method was the simplification of the data analysis (no need to perform complex *I-V* curve fitting as during PMOS2 experiment). To avoid the potential problems with voltage measurements at higher voltages, the following upgrades were made:

1. The test cables were replaced with a lower capacitance type
2. The 2611B was programmed to operate in high-capacitance drive mode
3. The length of the thin wires from DUTs to MUX board was minimised
4. The grounding of the DUTs was redesign to ensure low ground impedance

The upgraded test setup was validated by a test with an irradiated RADFET device. Sixty current steps were measured from 1 to 100 µA. The SMU was connected using a four-wire circuit to minimise the effect of the cables; thus the main source of measurement error was related to the accuracy of the SMU (current sourcing accuracy was 0.03 % of reading + 60 nA, and voltage measurement accuracy was 0.02 % of reading + 5 mV) [292].

The irradiation conditions were identical to those used during the PMOS experiments as defined in section 7.2.3.

7.3.3 RADFET threshold voltage shift results

A TID of 60 krad(Si) was reached during the irradiation stage of the experiment. The chart in Fig. 7.12 shows mean ΔV_T data during irradiation for each DUT bias group, using only data points taken at the idle temperature of 20°C. The V_T was measured at 10 µA, the pre-irradiation *MTC* current. The ΔV_T standard deviation was < 0.25 % for the 0V bias group and < 1 % for positive bias groups. The plotted ΔV_T curves were not smooth; a small but consistent ripple can be observed on all curves due to concurrent annealing during the temperature sweep cycle (see temperature profile in Fig. 7.1).

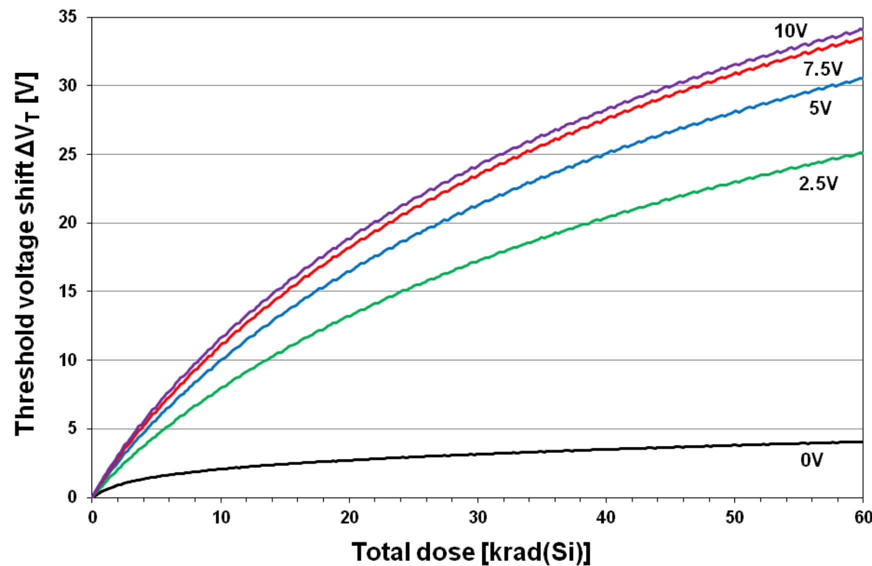

Fig. 7.12: Average threshold voltage shift, ΔV_T, plotted as a function of the total dose for each DUT bias group. A strong bias voltage dependence can be seen for lower voltages.

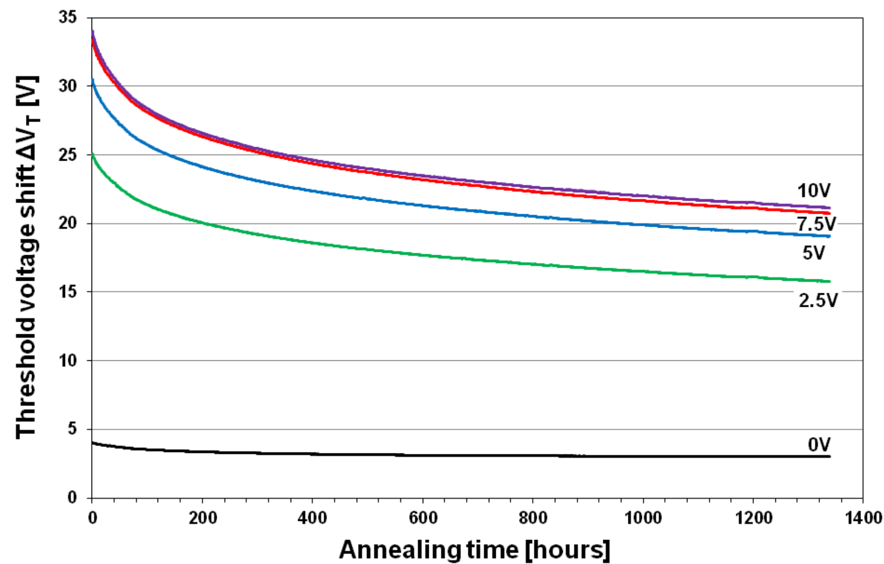

Fig. 7.13: Average threshold voltage shift, ΔV_T, plotted as a function of annealing time for each DUT bias group.

A week of irradiation was followed by 55 days of annealing, during which the experiment ran the same test sequence as during irradiation. Fig. 7.13 shows the ΔV_T during annealing for all bias groups. The ΔV_T recovery stopped after ~500 h for 0 V but was still present after 1,300 h in other samples. The annealing (fading) results are summarised in Tab. 7.4 in relative terms, as a percentage of ΔV_T recovery at selected annealing times. The fading was small for all bias groups within an hour after irradiation; this is important for applications using a single read-out shortly after exposure. However, the fading was large for all bias groups at longer times, being the least pronounced for the 0 V group and similar for all the other groups. Such behaviour can complicate RADFET calibration for systems with continuous, long-term read-out.

Tab. 7.4: Recovery in ΔV_T during the annealing of each RADFET bias group.

Elapsed time	**0 V**	**2.5 V**	**5 V**	**7.5 V**	**10 V**
30 min.	-0.2 %	-0.2 %	-0.2 %	-0.3 %	-0.3 %
1 hour	-0.3 %	-0.4 %	-0.5 %	-0.5 %	-0.5 %
1 day	-5.7 %	-6.2 %	-6.7 %	-6.9 %	-7.3 %
7 days	-16.1 %	-18.8 %	-19.5 %	-19.9 %	-20.6 %
55 days	-25.4 %	-37.0 %	-37.3 %	-37.8 %	-37.7 %

7.3.4 RADFET temperature coefficient results

The DUTs were exposed to a regular temperature sweep test; the temperature profile was identical to the profile used during the PMOS experiments (Fig. 7.1). The temperature sweep test was performed during both the irradiation and annealing. This method allowed the *I-V* characteristics at various temperatures to be measured and the TID-induced changes in the *MTC* point and TC_{VT} to be calculated. First, the data were adjusted by removing the concurrent shift in V_T caused by the continuing irradiation during the temperature sweep. The compensation was based on the idle temperature *I-V* measurements made before, during and after the temperature sweep (*I-V* curve measurements 1, 5, and 10 in Fig. 7.1).

The TID compensated data were processed to obtain the *MTC* values measured during each temperature sweep. A value of TC_{VT} was calculated for each current step of the *I-V* curves (measurements 2 to 9 in Fig. 7.1) using linear regression. The following step was a search for the point at which the TC_{VT} changes from negative to positive value and calculation of the drain current at which the TC_{VT} is equal to zero. This was done using linear interpolation.

The average initial (pre-irradiation) *MTC* current value was 10.13 µA, with a standard deviation of 0.2 µA, and range from 9.8 to 10.4 µA within the whole DUT sample. The radiation-induced change in the *MTC* current, as shown in Fig. 7.14, exhibits a significant gate bias dependence, qualitatively largely similar to that of the V_T shift in Fig. 7.12. Generally, a significant shift in *MTC* current was observed, enhanced by positive bias. The error bars in Fig. 7.14 show one standard deviation and the range of data (the difference between maximum and minimum of measured values) was 4.1 % (0 V), 4.0 % (2.5 V), 17.1 % (5 V), 14.7 % (7.5 V), and 9.5 % (10 V).

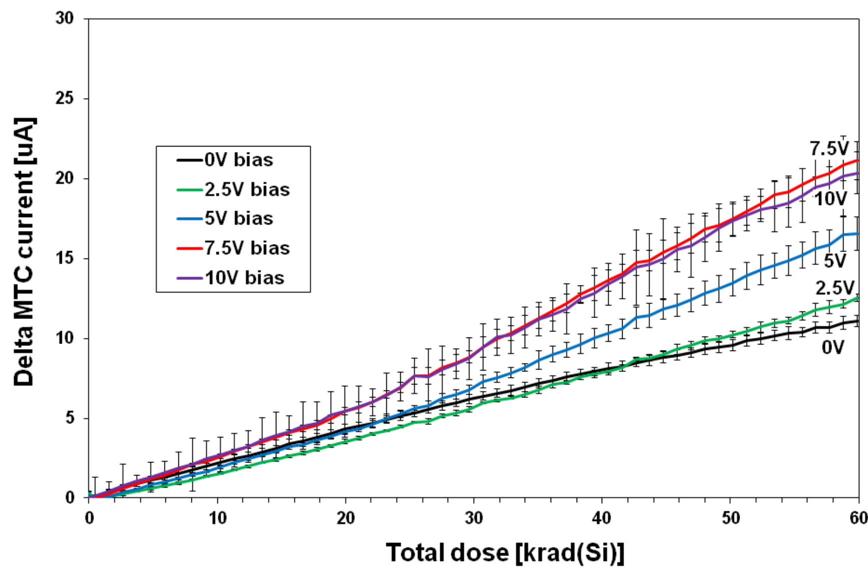

Fig. 7.14: Average *MTC* current shift plotted as a function of the total dose for each DUT bias group. The error bars show one standard deviation within each group of DUTs at a given bias voltage.

Fig. 7.15 shows the *MTC* current results for all bias groups during the 55 days of annealing. *I-V* curve data were processed in the same manner as the irradiation data in Fig. 7.14. Somewhat counter-intuitively, no decrease in *MTC* current was observed during annealing (i.e. *MTC* current data do not follow the ΔV_T post-irradiation recovery), but the *MTC* current continued to increase. The rate of the recovery was accelerated by a positive gate bias.

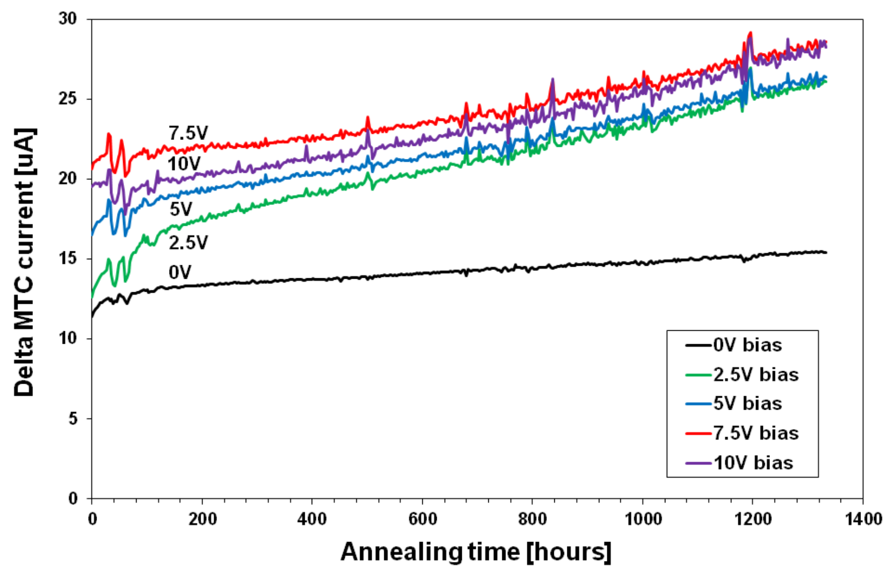

Fig. 7.15: Average *MTC* current shift plotted as a function of the annealing time for each DUT bias group.

The *MTC* current shift was a consequence of the opposite temperature dependence trends of two parameters: threshold voltage, V_T, and channel carrier mobility, μ, [266], [326]. In Fig. 7.16, the evolution of mobility during irradiation and annealing is plotted. The carrier mobility was calculated from the slope of the square root of I_D vs V_{GS} curve in the saturation region. From this figure, it can be seen that the *MTC* current trend qualitatively mirrored that of mobility during both the irradiation and annealing.

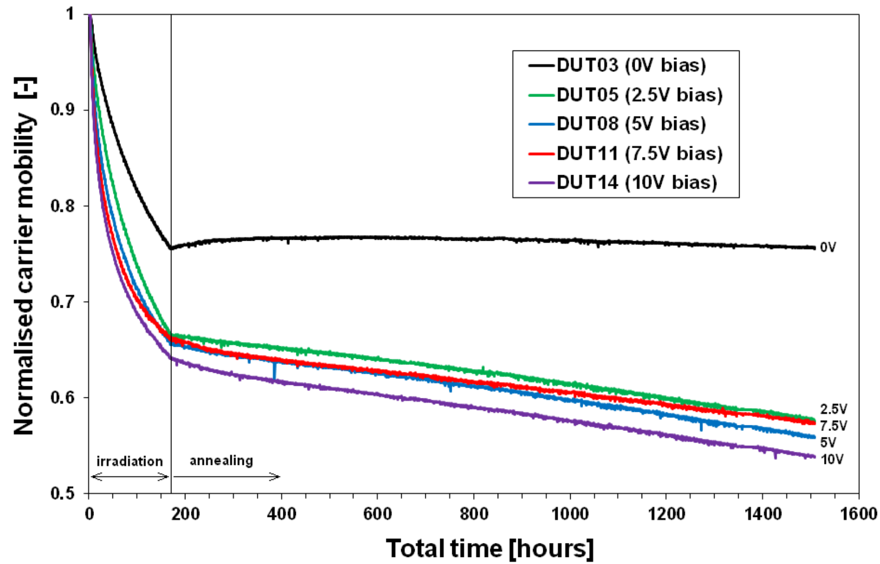

Fig. 7.16: Normalised carrier mobility (μ/pre-irradiation μ) of selected DUTs during irradiation and annealing. The irradiation phase took 167 hours.

7.3.5 Discussion of RADFET experiment results

The measured TID responsivity for the zero biased devices was in very good agreement with the Tyndall calibration data [325] and other work [323]. For positive bias groups, there was also a good agreement with Tyndall data (not published yet). It is obvious from Fig. 7.12 that increasing the bias voltage above 5 V is not advantageous for these samples, as it does not bring significant benefits regarding TID responsivity. The annealing results from Fig. 7.13 and Tab. 7.4 indicate low initial fading, followed by rather pronounced fading at longer annealing times. It should be noted that the magnitude of the annealing process could have been enhanced by the regular temperature cycling described in Fig. 7.1.

The main focus of this experiment was, however, characterisation of temperature effects in the RADFETs. Temperature dependence of V_T, reflected in TC_{VT} and *MTC* values, is of critical importance in RADFET applications. Fig. 2 in [251], showing ΔV_T and temperature measurements during 18 months of the Proba-II space mission involving Tyndall RADFETs similar to these in the current study, was an excellent example of how temperature effects can obscure the data trends and complicate data analysis. Namely, the temperature drop from 54 to 42 °C halfway through the mission results in significant (in relative terms) shifts of V_T and, particularly, ΔV_T, which needed to be compensated in order to obtain accurate mission dose information.

Temperature effects are particularly important in low-dose applications. Detailed on-wafer tests before packaging the samples used in this study showed the following average TC_{VT} values: -0.2 mV/°C at 9 μA read-out current (I_D), 0.05 mV/°C at 10 μA (closest to the actual *MTC*), and 0.30 mV/°C at 11 μA. The sensitivity of tested samples at low doses was approximately 0.60 mV/rad. Thus, the increase of temperature by just 1 °C would result in a dose error of 0.33 rad at 9 μA read-out current, 0.08 rad at 10 μA, and 0.5 rad at 11 μA. The relative importance of these errors increases with a decrease in the measured dose.

Among the space environment monitoring, there are other applications with high accuracy requirements, such as highly regulated medical applications, that also require careful temperature compensation. For example, a single-use OneDose dosimeter for quality assurance in radiotherapy, based on Tyndall RADFETs [327], measures doses from 0.2 to 0.5 krad($H_2 0$). However, to achieve the required overall accuracy of better than 5 %, all error budgets needed to be carefully managed. Therefore, temperature stabilisation in OneDose was achieved by the individual *MTC* calibration of each sample.

Furthermore, the results showed a pronounced change in the *MTC* current point during both irradiation and annealing. The monotonic increase in the *MTC* current suggested that the standard temperature compensated readout methods (using a constant current or data correction based solely on pre-irradiation *MTC* current/*TC* data) need to be applied with caution, particularly in high dose applications. A good practical example is DVS, an implantable dosimeter for the quality assurance of radiotherapy [328], also based on Tyndall RADFETs. The DVS needs to measure dose with 5 % accuracy in the range from 0.2 to 8 krad($H_2 0$). Temperature errors here have been minimised by operating the device at close to the initial (pre-irradiation) *MTC* and carefully monitoring the temperature. The accuracy was helped by the fact that the dosimeter remains in the human's body, thus at a fairly constant temperature throughout use. However, particular attention had to be given to the relationship between the calibration data at room temperature and 37 °C [328].

The results for the annealing of the *MTC* current in Fig. 7.15 were surprising, as the *MTC* data did not follow the threshold voltage recovery trends in Fig. 7.13. However, Fig. 7.16 shows that the *MTC* current indeed increased in line with the carrier mobility in the channel during both irradiation and annealing, i.e. the continuous decrease in mobility was mirrored by an equivalent increase in the *MTC* current. This indicates that mobility changes had the predominant effect on *MTC* evolution during irradiation and, particularly, during annealing. It was probably the build-up of the interface traps (which resulted in a decrease in the mobility) that governed the *MTC* current behaviour. This coincided with conclusions based on irradiation data reported in [326]. The impact of carrier mobility on the temperature dependence of the MOS transistors is discussed in sections 3.8.3 and 3.8.4, respectively.

Finally, the acquired data showed that the *MTC* point shift is significantly bias sensitive and thus the readout method [267] using the two RADFETs (one biased and one unbiased) is limited in its ability to suppress the temperature sensitivity.

The RADFET TID-TC experiment was presented at the NSREC 2016 conference, and an extended paper was published in the IEEE-TNS journal [329].

7.4 PMOS-RADFET combined experiment

The final MOS TID experiment was performed in order to extend the understanding of the TID effects on MOS devices for dosimetry applications. The MOS devices were irradiated at room temperature under various bias conditions. The research goals were:

1. To investigate the impact on the initial value of the threshold voltage V_{T0} on the TID responsivity of Tyndall RADFETs
2. To compare the linearity of the tested devices and its bias sensitivity
3. To extend the bias conditions by a permanent drain current mode, or “reader” mode. This bias condition was identified as one of the options for the TID dosimetry part of the SEM subsystem of the in-orbit experiment
4. To measure long-term annealing and its bias sensitivity
5. To irradiate identical devices as during the previous TID-TC experiments and compare the responsivity to understand the impact of TID-TC ISTM method on the TID responsivity
6. To attempt to acquire TID-TC data using the precise measurement of the variation of the ambient temperature during the experiment

7.4.1 The MOS devices under the test

Thirty MOS devices of three types were used in the experiment as summarised in the Tab. 7.5. The Tyndall and ZVP devices were of the same types used in the previous experiments. Moreover, a set of REM RADFETs was obtained for this experiment. The REM devices were developed by Holmes-Siedle, who invented the RADFETs [330].

Tab. 7.5: List of MOS devices tested during the PMOS-RADFET combined experiment.

DUT number	Type	V_{T0} [V]	Bias conditions
TYN01 to TYN03	TY1003	0.9	0 V (all leads shorted)
TYN04 to TYN06	TY1003	1.8	0 V (all leads shorted)
TYN07 to TYN09	TY1003	0.9	5 V gate voltage
TYN10 to TYN12	TY1003	1.8	5 V gate voltage
TYN13	TY1003	0.9	10 μA read mode
TYN14	TY1003	1.5	10 μA read mode
TYN15	TY1003	1.8	10 μA read mode
REM01 to REM03	RFT-300CC10G1	5.3	0 V (all leads shorted)
REM04 to REM06	RFT-300CC10G1	5.3	3 V gate voltage
REM07 to REM09	RFT-300CC10G1	5.3	5 V gate voltage
REM10	RFT-300CC10G1	5.3	12 V gate voltage
REM11	RFT-300CC10G1	5.3	18 V gate voltage
REM12	RFT-300CC10G1	5.3	10 μA read mode
ZVP1	ZVP1320FPA	3.2	0 V (all leads shorted)
ZVP2	ZVP1320FPA	3.2	5 V gate voltage
ZVP3	ZVP1320FPA	3.2	10 μA read mode

7.4.2 The setup of the combined experiment

The DUT *I*-*V* curve measurement system was practically identical to the system used in the RADFET TID-TC experiment as described in section 7.3.2. The principal instrument was the SMU 2611B. The I_D current sweep steps were identical to those used in the PMOS1 experiment for ZVP devices, and the Tyndall RADFETS were measured the same way as during the RADFET TID-TC experiment (the measurement errors were the same as well). Only the Q1 RADFETs of the REM devices were measured using sixty current steps ranging from 1 µA to 1 mA. The measurement errors of the REM RADFETs were identical to the ZVP devices (section 7.2.2).

The ambient temperature was measured using the same PRT as used in the DTC system (see section 6.5.2). The SMU 2611B was used to measure the resistance of the PRT. The bias voltage generators were identical to those used in the previous experiments. Each type of MOS devices had its own 10 µA constant current source provided by the triple SMU U2722A (see section 6.4.2). The irradiation conditions were identical to those used during the previous experiments as defined in section 7.2.3. The measurements were executed every 15 minutes giving a TID resolution of 90 rad(Si).

7.4.3 Threshold voltage shift results of the combined experiment

The threshold voltage shifts were analysed from the obtained *I*-*V* curves as during the previous experiments. The uninterrupted irradiation took 140.5 hours exposing the devices to TID level of 50.6 krad(Si). The following annealing phase lasted 1108 hours. It was interrupted twice; the first interruption was at the end of the irradiation (5 hours) and the second break was at the elapsed time of 619 hours (4 hours). The devices were not biased during the breaks. The ΔV_T results are shown in Fig. 7.17 to Fig. 7.19.

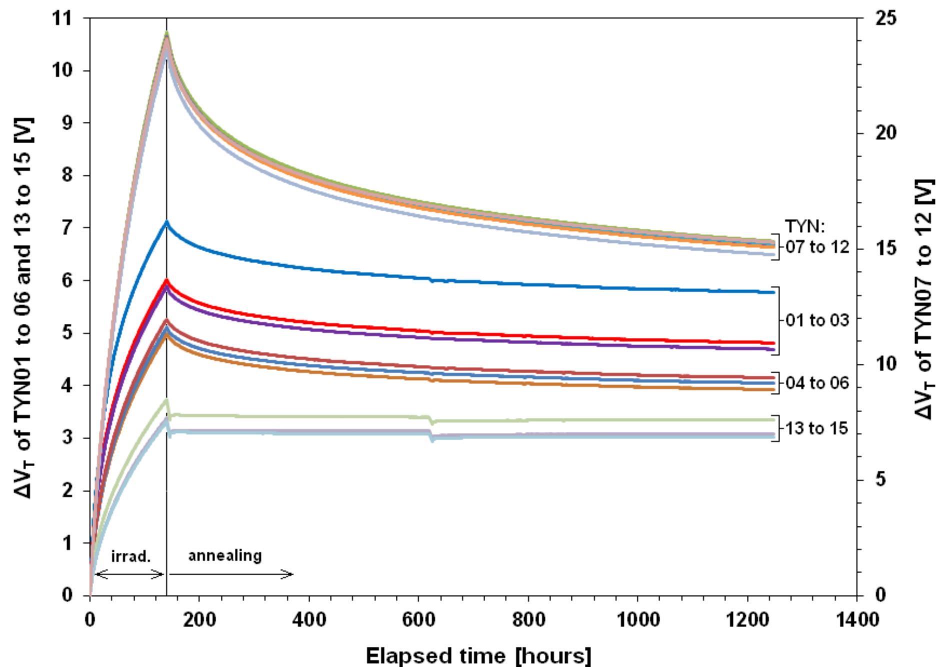

Fig. 7.17: Threshold voltage shift of the Tyndall devices at 10 µA during both irradiation and annealing. Dual Y axes chart was used to improve readability of the curves.

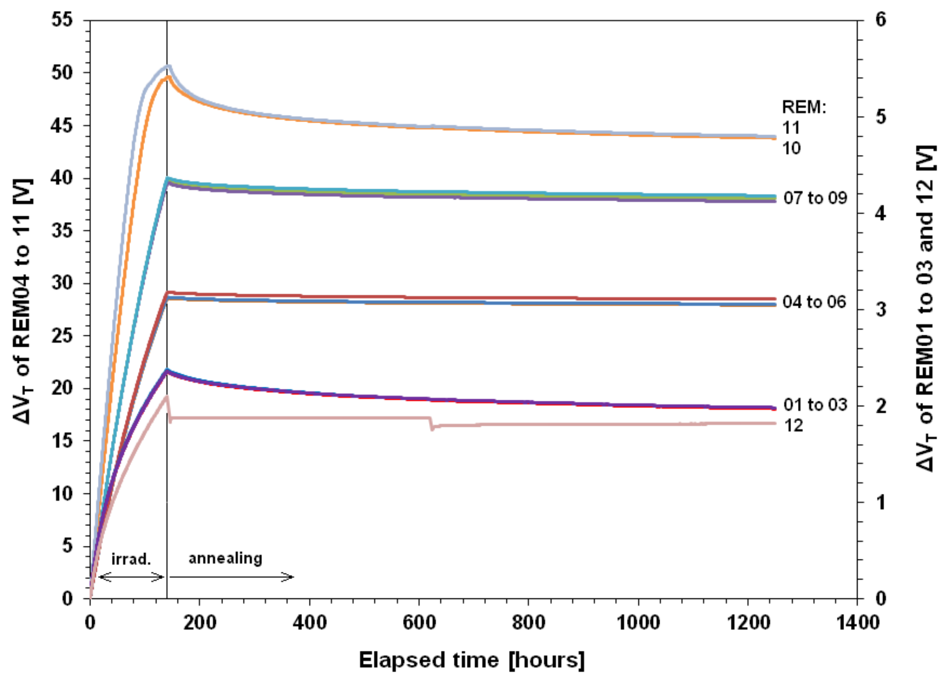

Fig. 7.18: Threshold voltage shift of the REM devices at 490 μA during both irradiation and annealing. Dual Y axes chart was used to improve readability of the curves.

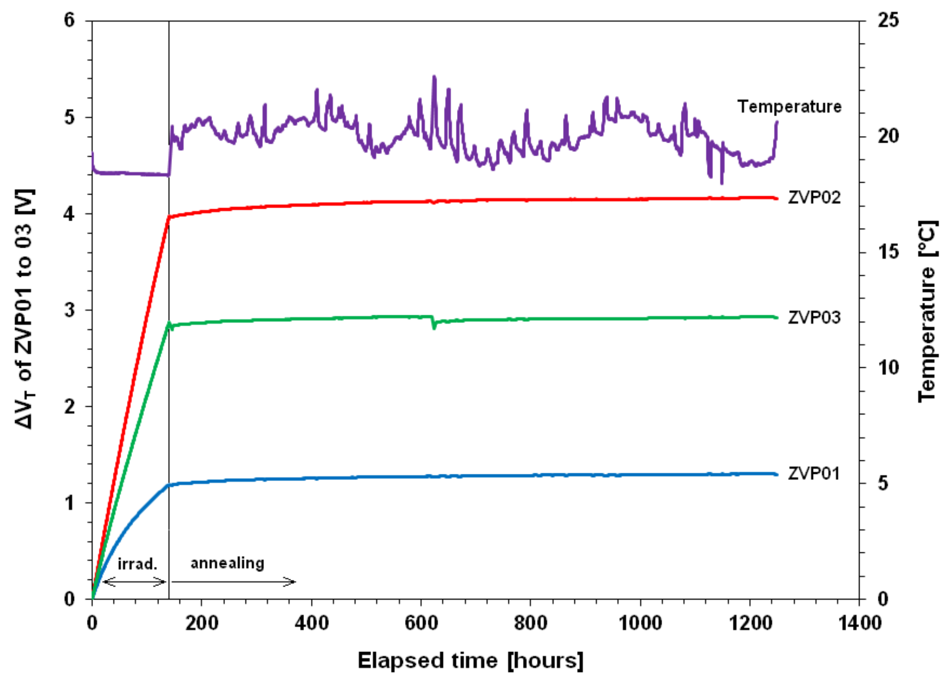

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Fig. 7.19: Threshold voltage shift of the ZVP devices at 1 mA during both irradiation and annealing. The temperature of the devices was plotted as well.

7.4.4 Analysis of the TID responsivity

The data of the gate threshold voltage shifts were processed to evaluate the linearity of the TID responsivity of each device group and the impact of both bias conditions and initial threshold voltage on it. The TID responsivity r is defined as [265]:

$$r = \frac{\Delta V_{\mathrm{T}}}{\Delta D}, \tag{7.1}$$

where D is the TID level (dose). The responsivity is typically given in mV/rad(Si). The average responsivity was calculated for each group of devices at various TID levels as outlined in the Tab. 7.6. It should be noted that the TYN01 data was not used as this device appeared to be anomalous (detail analysis of the responsivity showed a principal deviation of the responsivity curve from the other devices).

Tab. 7.6: TID responsivity measured during the PMOS-RADFET combined experiment.

DUT number	V_{T0} **[V]**	**Bias**	r_0 **[mV/rad(Si)]**	Δr **at 1 krad [%]**	Δr **at 5 krad [%]**	Δr **at 10 krad [%]**	Δr **at 20 krad [%]**	Δr **at 50 krad [%]**
TYN02 to 03	0.9	0 V	0.64	-15.5	-64.8	-76.8	-85.6	-92.4
TYN04 to 06	1.8	0 V	0.52	-26.9	-64.3	-75.9	-84.9	-91.1
TYN07 to 09	0.9	5 V	1.32	-13.2	-38.3	-51.1	-64.2	-82.4
TYN10 to 12	1.8	5 V	1.31	-13.9	-38.9	-51.6	-64.3	-82.0
TYN13	0.9	10 μA	0.37	-28.8	-65.9	-76.4	-83.6	-89.7
TYN14	1.5	10 μA	0.27	-24.6	-58.1	-69.8	-76.4	-85.4
TYN15	1.8	10 μA	0.26	-22.4	-57.4	-69.3	-77.0	-84.9
REM01 to 03	5.3	0 V	0.16	-16.6	-44.9	-60.2	-73.4	-84.3
REM04 to 06	5.3	3 V	0.85	-1.2	-9.8	-17.5	-29.6	-55.8
REM07 to 09	5.3	5 V	1.07	0.2	-6.5	-12.3	-21.3	-52.4
REM10	5.3	12 V	1.53	-0.4	-5.6	-10.3	-18.3	-88.9
REM11	5.3	18 V	1.80	-1.1	-5.4	-11.9	-19.4	-91.8
REM12	5.3	10 μA	0.12	-10.9	-33.7	-54.8	-68.3	-76.6
ZVP1	3.2	0 V	0.05	-5.6	-24.6	-33.2	-54.8	-74.9
ZVP2	3.2	5 V	0.09	-2.2	-2.6	-3.4	-8.5	-25.5
ZVP3	3.2	10 μA	0.07	-4.5	-9.8	-15.5	-22.4	-29.3

The analysis of the TID responsivity data suggested that:

1. The Tyndall devices provided higher initial responsivity than the other devices. However, they suffered significant degradation of responsivity already at a relatively low dose of 5 krad(Si).
2. The saturation-like behaviour caused the non-linear shape of both the $\Delta V_{\mathrm{T}}(D)$ and $r(D)$ functions. This phenomenon could be seen on all devices. The most linear were the REM devices operated in positive bias mode, especially at higher bias voltage up to the saturation dose of ~40 krad(Si).

3. The COTS ZVP devices were also very linear, especially in 5 V and "reader" bias modes. They were not saturated even at maximum dose.
4. For both REM and ZVP devices, the voltage bias improved the linearity of the responsivity.
5. Irradiating the devices at permanent "reader" conditions showed that the devices are less responsive in this mode. However, the ZVP device was more linear in reader mode than in 0 V mode, and the responsivity was practically the same.
6. For the REM devices the bias voltage dependency of the responsivity was linear, and thus it was in very good agreement with the formula (3.9).
7. The impact of the initial value of the V_{T0} appeared to be significant for the Tyndall 0 V bias group where the device with 50 % lower V_{T0} offered approximately 20 % higher responsivity. However, both groups suffered similar linearity issues at higher TID levels. Similar behaviour was observed for the devices biased in the "reader" mode.

Another analysis was performed to compare the previous TID-TC experiments of ZVP and Tyndall devices and to investigate if the temperature sweep had any impact on the final ΔV_T at 50 krad(Si). As can be seen in Tab. 7.7, the difference between the results of the ZVP experiments were within the repeatability of the experiments (dosimetry errors, test system errors).

The result of the comparison of the unbiased Tyndall devices was as expected; the TID-TC data suggested that the heating phase of the temperature sweep was causing temperature-enhanced concurrent annealing. However, the 5 V biased Tyndall devices showed opposite behaviour. This conflict could be possibly explained by the impact of the bias conditions on the temperature enhanced effects and limited comparability of the devices used in the experiments (the RADFETs in the TID-TC experiment were from an older batch with V_{T0} = 1.5 V).

Tab. 7.7: Comparison of the ΔV_T all MOS experiments.

Devices	**ΔV_T TID-TC experiments [V]**			**ΔV_T PMOS-RADFET combined experiment [V]**			**Delta [%]**
	Min	**Max**	**Aver**	**Min**	**Max**	**Aver**	
ZVP 0 V	1.22	1.29	1.25	-	-	1.18	-5.6
ZVP 5 V	3.63	3.90	3.80	-	-	3.94	3.7
TYN 0 V	3.81	3.83	3.82	4.96	5.24	5.10	33.5
TYN 5 V	27.88	28.33	28.17	23.50	23.99	23.81	-15.5

7.4.5 Analysis of the long-term annealing

Similarly to the RADFET TID-TC experiment, the exposed devices were annealed for 46 days. The results from the annealing measurements are summarised in Tab. 7.8. The following observations were made:

1. The recovery of Tyndall devices was strongly dependent on the bias conditions; the 5 V biased devices were annealing twice as much as the nonbiased devices. No difference was observed between the two V_{T0} groups.

2. The annealing of the REM RADFETs was the lowest at a bias voltage of 3 V and this biased group performed as specified by the REM datasheet [330]. However, the higher bias voltage was counterproductive; the devices were probably already saturated at 50 krad(Si), and therefore the annealing started to be significantly stronger from the 5 V bias voltage up.
3. The 0 and 5V biased ZVP devices exhibited reverse annealing; after the initial drop, the V_T continued to grow. The bias voltage seemed to have positive impact on this effect; the V_T of the 5 V biased device shifted almost 50 % more than the unbiased device. This effect is discussed in section 3.6.1 as well as in [330]. The observation of the reverse annealing also explained the reverse trend of the ΔV_T temperature sweep-induced ripple discussed in section 7.2.9.
4. Rather surprising was also the results for the "reader" mode biased devices; after the initial drop (caused by the interrupt of the bias supplies at the end of the irradiation) the devices were practically stable; especially the recovery of the ZVP device was within ±2 % of ΔV_T at the end of the exposure.
5. The annealing after 168 hours of Tyndall devices was compared to the results of the TID-TC experiment. As expected, the recovery of 0 V biased devices was approximately 25 % higher during the TID-TC experiment due to the thermal annealing (see section 3.9.3). However, annealing of the 5 V biased group was lower during the TID-TC experiment by 12 %. This conflict was consistent with the discrepancy discussed at the end of section 7.4.4 and was probably caused by the same effects.

Tab. 7.8: Recovery of the V_T measured during the PMOS-RADFET combined experiment.

DUT number	V_{T0} [V]	Bias	ΔV_T at 5 hrs [%]	ΔV_T at 24 hrs [%]	ΔV_T at 168 hrs [%]	ΔV_T at 484 hrs [%]	ΔV_T at 1100 hrs [%]
TYN02 to 03	0.9	0 V	-2.2	-4.8	-11.8	-17.0	-20.2
TYN04 to 06	1.8	0 V	-2.1	-5.0	-12.4	-17.8	-21.2
TYN07 to 09	0.9	5 V	-2.8	-8.2	-21.6	-30.5	-37.0
TYN10 to 12	1.8	5 V	-2.8	-8.3	-21.7	-30.6	-37.1
TYN13	0.9	10 μA	-9.4	-8.0	-8.7	-12.2	-10.6
TYN14	1.5	10 μA	-8.6	-6.5	-6.5	-10.9	-8.3
TYN15	1.8	10 μA	-7.8	-5.9	-6.5	-10.7	-8.9
REM01 to 03	5.3	0 V	-0.9	-2.6	-8.1	-12.9	-16.5
REM04 to 06	5.3	3 V	-0.1	-0.3	-1.1	-1.7	-2.3
REM07 to 09	5.3	5 V	-0.1	-0.8	-2.3	-3.3	-4.3
REM10	5.3	12 V	-0.1	-2.8	-7.4	-9.7	-11.7
REM11	5.3	18 V	-0.1	-3.6	-9.0	-11.3	-13.2
REM12	5.3	10 μA	-12.1	-10.7	-10.7	-16.2	-13.6
ZVP1	3.2	0 V	-0.4	0.9	4.5	6.3	9.1
ZVP2	3.2	5 V	-0.3	0.4	2.4	3.6	4.8
ZVP3	3.2	10 μA	-2.0	-0.7	0.8	-1.4	1.9

7.4.6 Analysis of the temperature effects

An attempt was made to obtain TC_{VT} data from the results of the PMOS-RADFET combined experiment. The temperature of the devices was precisely measured as shown in Fig. 7.19. The data were analysed only from the annealing phase as the temperature during the irradiation was practically stable. For the annealing, the experiment was placed in an electronics lab, and as can be seen in the plot, the variation of the ambient temperature was slow. The noticeable periodical variations were caused by the daily temperature trends in the environment.

However, no obvious trends in the TC_{VT} were observed. It is believed that it was caused by the low speed and small amplitude of the temperature changes, which were slower than the annealing trends and thus the changes in the TC_{VT} became indistinguishable from the “carrier” trend driven by the annealing.

7.5 Conclusions of MOS TID experiments

The MOS experiments were the first opportunity for the practical use of the proposed method for ISTM measurements of *TC* using the DTC system. After the upgrade of the faulty cooling system, the DTC system became a precise and reliable tool for controlling the DUT temperature. During the experiments, the STS was not only recording all experimental data, but it was also collecting and analysing various engineering data from the DTC system. No anomaly in the performance of the DTC was identified during more than 100 days of operation (nearly 44 million DUT temperature control tasks were performed). There was no TID-induced degradation observed in any primary part of the DTC system placed in the irradiation container. This excellent performance record validated the design of the DTC system and its readiness for more advanced experiments.

Three types of MOS devices were tested during the MOS experiments. These included two types of European RADFETs and one type of a COTS low-power transistor.

The primary goal of the MOS experiments was to perform novel ISTM measurement of the TID-induced changes of the TC_{VT}. Two successful TID-TC experiments were performed (on the COTS transistors and the Tyndall RADFETs), and the results showed a significantly different behaviour of these two devices. While the RADFETs exhibited a monotonous shift of the *MTC* point with the TID, the COTS transistor showed a more complex response to TID. As soon as the exposure started, the value of *MTC* dropped and then started to rise. This problem might be a subject of future studies, including TID-TC test of some other types of MOS devices.

The experiments proved that the TC_{VT} and *MTC* are strongly dependent on the TID. Therefore, the published methods of the RADFET temperature compensation (as discussed in section 5.4.3) have limited accuracy. A possible solution might be to measure the *I-V* curve of the RADFET. The current sweep range would be extended to cover the potential shift of the MTC point. Using the history of these *I-V* curves and the history of the ambient temperature, the actual shift of the *MTC* could be potentially reconstructed.

The mathematical method for RADFET temperature compensation (using precise temperature measurements) can be improved by using a model based on the TID-TC data. Such an advanced model would use the measured $TC_{VT}(D)$ function to compensate for the TID-induced change of the TC_{VT}.

Both of the proposed methods will be demonstrated during the data analysis of the in-orbit experiment. However, it is obvious that each of these compensation methods is, in fact, self-referring; the temperature-compensated TID level is calculated from the TID level. This problem can be eliminated by combining readings from multiple TID detectors with different (known from TID-TC experiments) $TC_{VT}(D)$ functions.

The detailed data of the MOS experiments provided excellent support for the secondary goal of these experiments, the selection of the detectors for the dosimetry part of the in-orbit experiment. A decision was made to employ the Tyndall RADFETs with V_{T0} of 0.9 V as primary TID detectors and the ZVP commercial PMOS transistors as secondary detectors. The reasons for this selection were as follows:

1. The REM RADFETs appeared to have the best performance in most of the investigated parameters. However, they achieved this excellent performance (especially linearity) only in a biased mode, which is not allowed for the CubeSat class missions, where the power is not available permanently. Another challenge of the application of REM devices is the need for high voltage DC-DC converter to allow the expected V_T span. Similarly, there would be a need for a high-voltage input range of the DAQ system.
2. In contrast to the REM RADFETs, both the Tyndall and ZVP devices can be measured within the 5 V voltage ranges, which is easily achievable by most of the ADC circuits.
3. The size limits: both of selected devices are available in ultra-miniature SOT23 packages.
4. The TID-TC data were measured for both of these devices. They have significantly different $TC_{VT}(D)$ functions, which makes them an ideal couple as discussed above.
5. Both of these devices offered good sensitivity both in 0 V and “reader” bias modes. Therefore both of these biasing methods can be tested during the in-orbit experiment if the power budget allows for it.
6. The ZVP devices showed reverse annealing, which seemed to be an excellent match with the normal annealing of the Tyndall devices. Having annealing data with opposite trends from both of these devices will help to identify the “quiet” mission stages, during which the devices are not exposed to TID.

To conclude, the MOS experiments proved the excellent performance of the DTC system, generated valuable high-resolution TID-TC data (which were published in IEEE journals) and helped to make an objective selection of the TID detectors for the in-orbit experiment.

8 VOLTAGE REFERENCES TID EXPERIMENTS

This chapter summarises the results of two radiation experiments focused on in-situ measurement of TID-induced degradation of COTS voltage references. As discussed and demonstrated in chapter 4.3.3, the published works did not provide such data.

8.1 Objectives of voltage reference TID experiments

There were multiple objectives to be addressed by the voltage reference experiments:

- To design an ISTM test system allowing high-precision measurement of the most important parameters related to the metrological performance of the VREF devices with respect to their application in an example space DAQ system and the planned in-orbit experiment. The DUTs shall be biased with respect of the planned in-orbit experiment
- To measure TID-induced changes of temperature drift of the VREF devices using a modified version of the DTC system
- To select an appropriate set of COTS voltage reference devices by applying requirements tailored to the TID experiments and the in-orbit experiment
- To demonstrate the metrological capabilities of practical implementation of the ISTM test system by observing the repeatability of the measurements made under constant conditions prior to the irradiation phase of the experiments

8.2 COTS voltage references TID experiment

8.2.1 Selection of the COTS voltage reference devices

Similarly to the COTS ADCs discussed in chapter 2.3, there were tens of various types of COTS VREF devices available for the TID experiment. To narrow down the selection, the following criteria were applied (see section 4.3.1 for definitions):

- Only series VREF topology (SEVRs) were to be used
- All VREF technologies were to be tested, including bandgap, buried Zener diode and XFET
- Unified packages were to be used with respect to the planned TID-TC test and its need for identical thermal properties of DUTs
- Only industrial-grade VREF devices with an extended temperature range of -40 to 85 °C could be used (as required by the planned in-orbit experiment)
- The in-orbit experiment requires low-power devices to be used
- Identical pinouts were to be used in order to simplify the hardware design of the test system
- Commercially available devices supplied from identical batches (identical lot codes)

For the experiment, a set of twenty-four voltage references (DUT01 to DUT24) was used. The DUT set was organised as a matrix of six by four. There were four different types of voltage reference and six identical devices of each type. Tab. 8.1 summarises the key parameters of the selected VREF devices.

Tab. 8.1: Parameters of the VREF devices used in the TID experiment.

Part number/ Device marking	**Data-sheet**	**VREF technology**	V_{nom} **[V]**	**Bias voltage [V]**	**Unbiased DUTs**	**Biased DUTs**
LT1236BIS8-5 443-e3/N74-928	[331]	buried Zener diode	5.000	12	01 to 03	04 to 06
ADR440ARZ #006-0328 1800328	[332]	XFET	2.048	5	07 to 09	10 to 12
LT1460EIS8-2.5 434-e3/N74-928	[333]	bandgap	2.500	5	13 to 15	16 to 18
ADR03ARZ #420-2685 2882685	[334]	bandgap	2.500	5	19 to 21	22 to 24

The six DUTs of each type were from the same production lot (they had identical package marking). The first three DUTs of each type were not biased during irradiation (the V_{IN} pin was grounded), and the bias voltage was applied only during the electrical measurement. The second three DUTs were permanently biased. Neither pre-conditioning nor burn-in of the DUTs was performed before the experiment.

All the DUTs were packaged in a SOIC-8 plastic package with an identical pinout. Each DUT was installed on a SOIC-8 to DIL8 adaptor PCB, creating an individual DUT module as shown in Fig. 8.1. As well as simplifying assembly, this solution also allowed the DUTs to be separated mechanically and, therefore, the mechanical stress on the individual DUTs was reduced. Mechanical stress has a strong influence on the stability of the DUT output voltage as discussed in chapter 3.10.1.

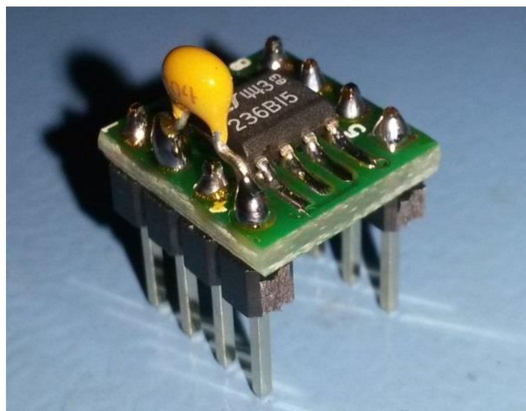

Fig. 8.1: A picture of the assembled DUT module. It consisted of the DUT, SOIC to DIL adaptor board and a decoupling capacitor.

8.2.2 Test system for the COTS voltage references experiment

The test system used in this work was designed to perform periodic measurements of the key parameters of the voltage references as defined in chapter 4.3.2. These included:

- The output voltage (or reference voltage)
- Temperature sensor voltage (DUT19 to 24 only)
- Line regulation
- Load regulation
- Supply current

The ISTM test system was fully automated and comprised a DUT container placed in the irradiation chamber, test instrumentation and a PC. The DUT container consisted of a filter box and a DUT board (see Appendix D.3). A lead-aluminium filter box was built as defined in section 4.2.3. The DUT modules were inserted into the DUT board, which provided the bias voltage and connection between the DUTs and the test instruments via multiplexing relays. A custom-made test controller ISTC2 provided relay drivers and monitoring of the MIF sources.

In order to measure the output voltage of the DUTs, a high resolution, 6.5 digit digital multimeter (Tektronix DMM4050) was used [168]. It was configured to the highest possible resolution using 100 NPLC (number of power line cycles) to suppress the power line noise. The DMM4050 offered 7.5 digits resolution using this setting and being operated in remote mode. The DMM4050 was also used to measure the temperature sensor voltage output of DUT19 to 24.

A Keysight E3631A programmable power supply was used to control the DUT supply voltage and thus allow measurement of the line regulation of the DUT output voltage. The line regulation was measured in five steps from 12 to 22 V for DUT01 to DUT06. DUT07 to 24 were measured from 5 to 15 V.

The load regulation was measured using an SMU Keithley 2420 [293]. The SMU acted as a programmable DC load and loaded the DUT from 0 to 10 mA in five steps. The SMU was connected to the DUTs as close as possible to them, so the voltage drop on the cables was negligible.

To simplify the cabling (and thus reduce any measurement error caused by the voltage drop), another digital multimeter (Fluke 8808A) was used to measure the DUT supply current. This multimeter was inserted to the DUT voltage input only during the measurement of supply current and, thus, its shunt impedance had no impact on the accuracy of the load regulation measurements.

The measurements were made every 30 minutes, and the measurement of each DUT took 40 seconds. Therefore, the unbiased DUTs were effectively biased for only 2% of the duration of the experiment. The temperature of the DUTs was monitored using a radiation tolerant Pt1000 sensor [300] (details in section 6.5.2).

8.2.3 The schedule of the VREF experiment

The experiment was performed in three successive phases. It started with installing the test system in the irradiation facility and running pre-test measurements, during which the entire system became thermally stabilised. The second phase was irradiation up to a TID of 100 krad(Si), followed by 40 hours of annealing. The third phase was long-term, room temperature, annealing. While the first two phases were performed in the irradiation facility at 20 °C ±0.5 °C, the third phase (annealing) was executed in an electronics laboratory, where the temperature was maintained between 19 and 24 °C.

8.2.4 The irradiation details of the VREF experiment

The MIF cell was used for the irradiation phase of the voltage reference experiment. The dosimetry was performed prior to the irradiation in order to place the DUT container in a position achieving dose rate of 360 rad(Si)/hr (see sections 6.1 and 6.2).

8.2.5 Results of the reference voltage measurements

The results of the 24-hour pre-test of selected DUTs are shown in Fig. 8.2. The settling of the temperature of the DUTs took approximately 10 hours, during which the DUT output voltages also settled. Once they had stabilised, the output voltages fluctuated within a window of only ±10 µV.

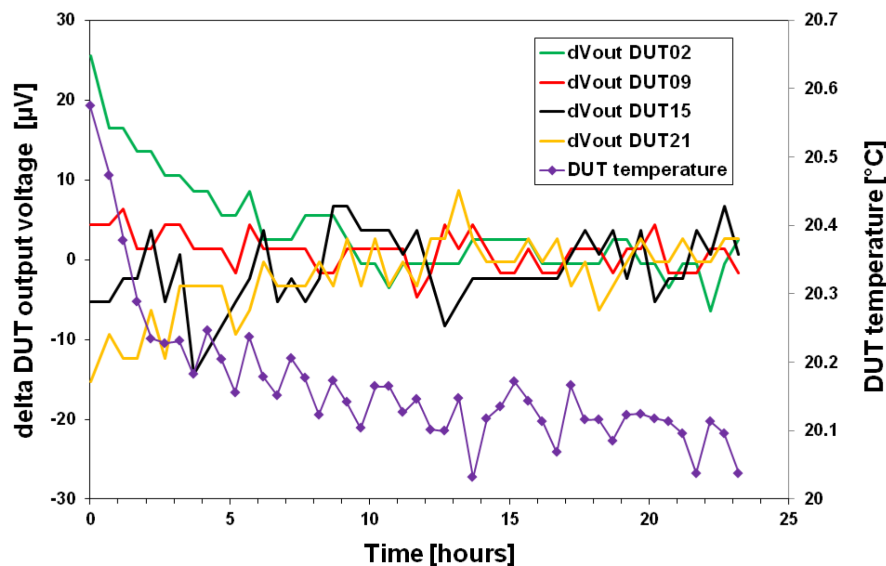

Fig. 8.2: A record of the initial, pre-test, phase of the experiment. Settling of the DUTs output voltage is linked to the temperature of the DUTs.

As soon as the DUTs had settled, the irradiation started with a target dose of 100 krad(Si). The uninterrupted irradiation took 278 hours. There were minor changes in the DUT supply currents, except for DUT07-13, whose supply current doubled.

The radiation-induced changes in the output voltage of the most sensitive unbiased DUTs are plotted in Fig. 8.3. Fig. 8.4 shows the same record for biased devices.

A strong difference in sensitivity can be seen. The glitches on the DUT10 and DUT16 curves were probably caused by the step change in the ambient temperature and absence of the bias during the transport of the system to the electronics laboratory for annealing.

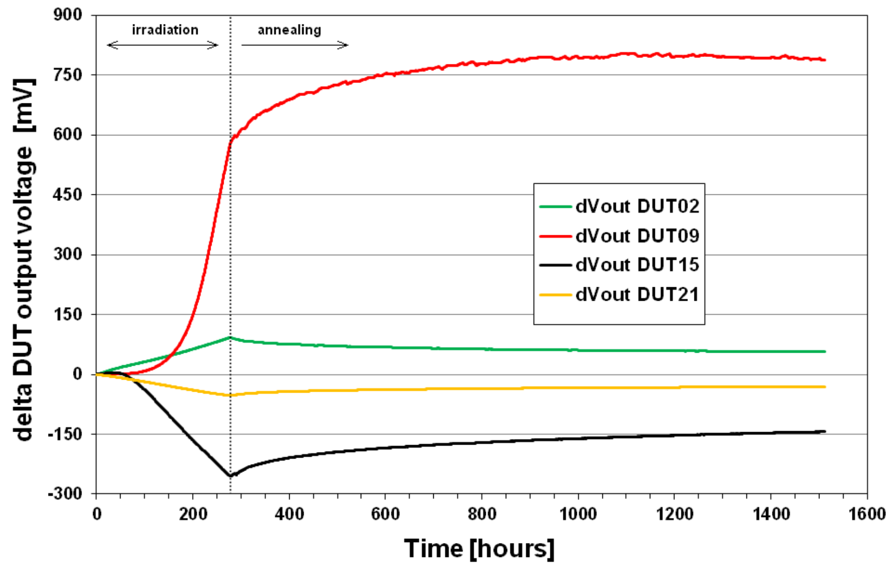

Fig. 8.3: Degradation and recovery of the output voltage of the unbiased DUTs during irradiation and annealing. The most sensitive DUTs from each type are plotted.

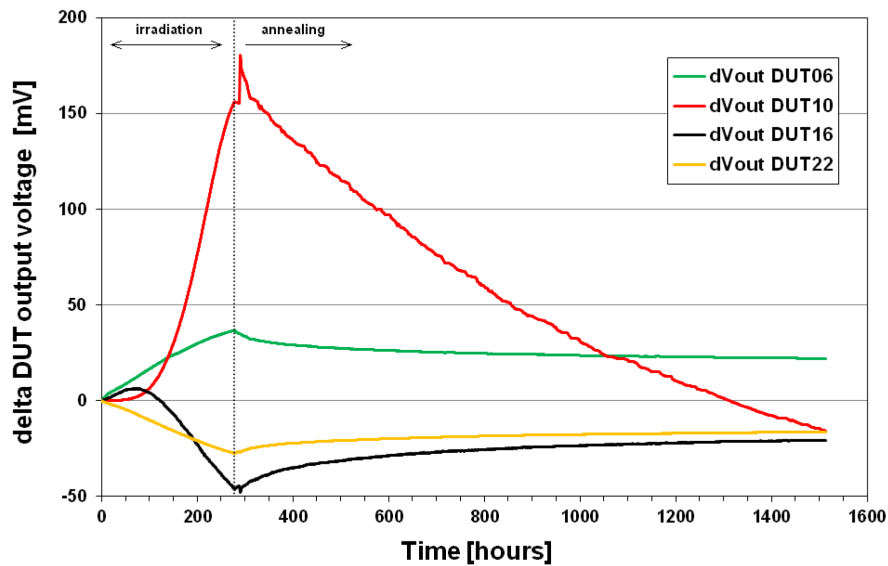

Fig. 8.4: Degradation and recovery of the output voltage of the biased DUTs during irradiation and annealing. The most sensitive DUTs from each type were plotted.

To demonstrate the influence of the radiation-induced degradation on a real application of the voltage reference (a DAQ system); the output voltage degradation was plotted again in Fig. 8.5. This format allowed the absolute magnitude of the output voltage error versus the TID to be seen.

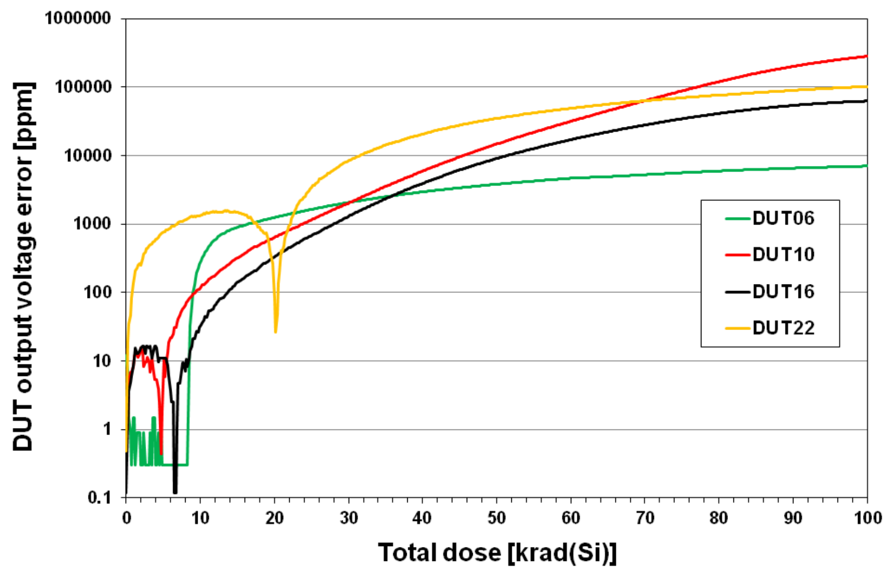

Fig. 8.5: The TID-induced degradation of the output voltage of the biased DUTs as a function of the total dose. These curves represent the absolute magnitude of the output voltage error relative to the initial values obtained during the pre-test.

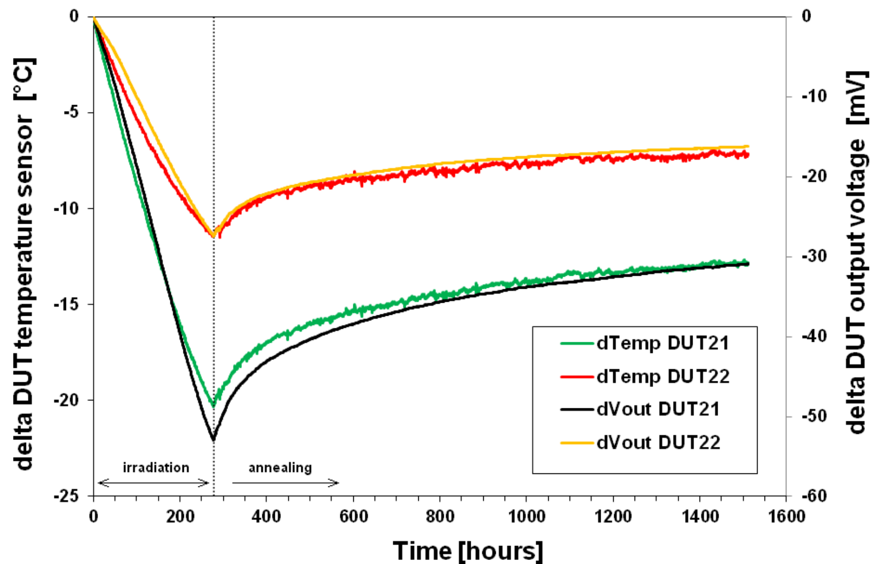

Fig. 8.6: Degradation and recovery of the ADR03 DUTs during irradiation and annealing. DUT output voltage and temperature sensor output are plotted. DUT21 was unbiased, and DUT22 was biased.

The final chart, in Fig. 8.6, shows the TID-induced changes exhibited by the ADR03 DUT21 and DUT22 temperature sensing outputs. The pre-test temperature measurements were used to calibrate the DUT temperature sensor. The degradation record was obtained by comparing the DUT outputs with the DUT temperature measurements provided by a radiation tolerant Pt1000 sensor. The DUT output voltage degradation curves were added to this chart to allow direct comparison of these two effects for an identical DUT.

8.2.6 Results of the measurements of line and load regulations

In addition to the regular measurements of the reference voltage, the test system also measured the load regulation and line regulation as they are essential for an understanding of the compatibility of the VREF device with the application (see section 4.3.2). The results of the measurement of the line regulation of the biased devices are shown in Fig. 8.7. Linear regression function was used to construct these plots.

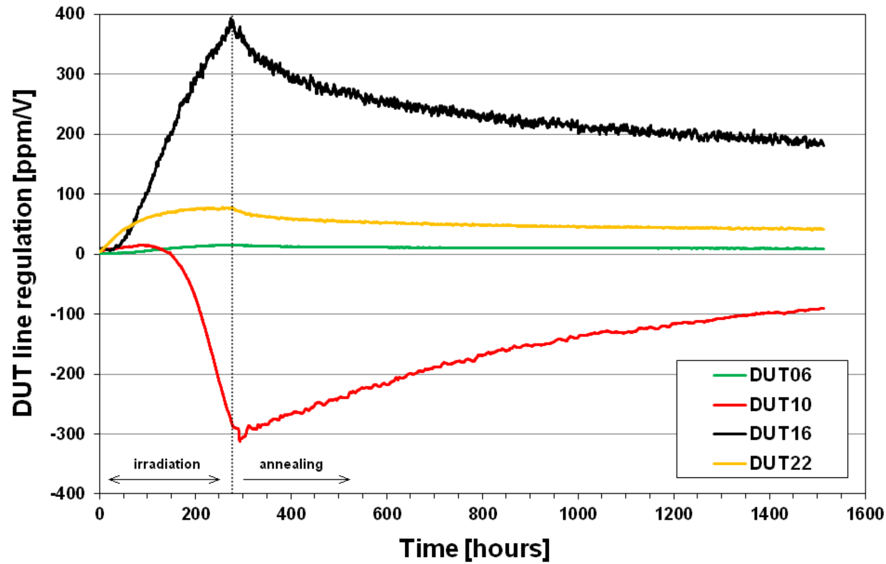

Fig. 8.7: TID-induced change and recovery of the line regulation of the biased DUTs.

Linear regression was also used for analysing the load regulation of the biased DUTs as shown in Fig. 8.8. The DUT06 failed to provide the output voltage at higher load currents; the output voltage measured at 5 mA dropped to zero at 59.1 krad(Si). Therefore only measurements made at lower load currents were used.

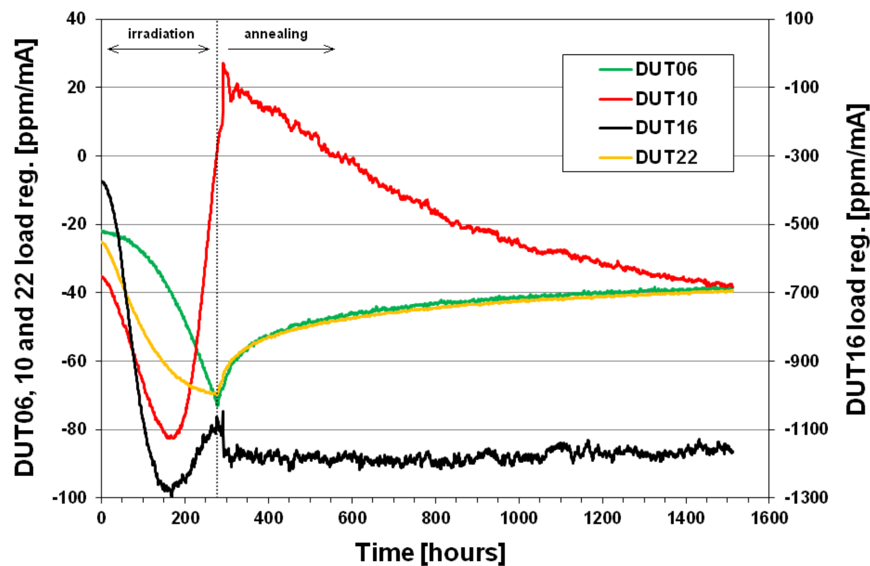

Fig. 8.8: TID-induced change and recovery of the load regulation of the biased DUTs.

8.2.7 Discussion of the results of the COTS VREF experiment

The recorded data suggests excellent functionality of the test system designed for this experiment. The results of the initial pre-test phase show superb stability and high signal/noise ratio of the voltage reference output measurements. The data suggest that a measurement resolution of better than 10 μV can be achieved, even though the measurement system was placed outside the irradiation facility and complex cabling of 15 m length was used. This was a promising result as more sophisticated, in-situ, TID experiments on A/D converters were planned in this PhD research program.

The TID-induced degradation of the output voltage of the DUTs is a crucial measurement from the application point of view. The data have been analysed to improve the understanding of the influence of this effect on a typical data acquisition application, where changes in reference voltage would cause a degradation of measurement accuracy. The resulting curves in Fig. 8.5 show that the measurement accuracy could be kept within 1000 ppm until a TID of 6 krad(Si) for all the biased DUTs. Above this dose, the degradation in accuracy would be more significant, and there was a strong difference between the types of voltage references tested. The unbiased devices suffered significantly stronger degradation (3 to 5 times).

The annealing was extended up to a period of 50 days to allow observation of long-term changes in the DUTs. This resulted in the substantial recovery of the DUTs, during which the readings approached their initial values. The annealing of DUT9 and DUT10 (ADR440, XFET) was more complex. The unbiased DUT9 continued to shift following the trend visible during irradiation (reverse annealing was observed). On the other hand, DUT10 showed a rebound effect – there was a rapid return to the initial value and even undershooting of it. These complex annealing phenomena are typical for MOS devices (as discussed in chapter 3.6) and could be a product of the XFET reference technology.

The ADR03 provides not only the reference voltage but also a temperature sensing output. These devices are standard bandgap references. The band gap cell contains two NPN transistors that differ in emitter area by a factor of two. The difference in their VBE produces a proportional-to-absolute temperature current (PTAT) which is available on a TEMP pin and allows external temperature sensing [334]. Therefore, this signal enables the monitoring of the internal conditions of the DUT circuit during the TID test. The results in Fig. 8.6 show that the degradation in output voltage is proportional to the degradation of the temperature sensing output. This effect may suggest that the primary source of the ADR03 TID sensitivity lies within the bandgap circuit. This conclusion might be useful for a radiation hardening process of these devices. The accuracy of this analysis is limited by the fact that the Pt1000 temperature sensor was not placed directly on the DUT, so the fitting of the curves might be influenced slightly by the thermal conductivity of the DUT board. The difference in the dynamic response of the miniature Pt1000 sensor and the DUT module also played a role (the Pt1000 has significantly lower mass).

The results of the COTS voltage reference experiment were presented at the RADECS 2016 conference [335].

8.3 COTS voltage references TID-TC experiment

8.3.1 COTS voltage reference under the test

For the experiment, a set of eight commercial voltage references (DUT1 to DUT8) was used. There were four different types of voltage reference and two identical devices of each type. Tab. 8.2 summarises the key parameters of the DUTs. The two DUTs of each type were from the same production lot (they had identical package marking) as during the previous experiment (as defined chapter 8.2.1). The first DUT of each type was not biased during irradiation (the VIN pin was grounded), and the bias voltage was applied only during the electrical measurements. The second DUT was permanently biased.

Tab. 8.2: Parameters of the VREF devices used in the TID-TC experiment.

Part number/ Device marking	Data-sheet	VREF technology	V_{nom} [V]	Typical/max TC [ppm/°C]	Unbiased DUTs	Biased DUTs
LT1236BIS8-5 443-e3/N74-928	[331]	buried Zener diode	5.000	5/10	DUT1	DUT2
ADR440ARZ #006-0328 1800328	[332]	XFET	2.048	2/10	DUT3	DUT4
LT1460EIS8-2.5 434-e3/N74-928	[333]	bandgap	2.500	10/20	DUT5	DUT6
ADR03ARZ #420-2685 2882685	[334]	bandgap	2.500	3/10	DUT7	DUT8

8.3.2 Test system for the voltage references TID-TC experiment

The test system used in TID-TC experiment was an upgraded version of the test solutions used in the previous voltage reference and MOS experiments.

An essential difference between the MOS TID-TC experiments and the voltage reference TID-TC experiment was the timing. The temperature sweep phase of MOS experiments could have been performed statically (e.g. by changing DUT temperature in discrete "staircase" steps and measuring the DUT parameters at a static temperature as shown in chart Fig. 7.1). In contrast, the temperature sweeping of the voltage reference devices had to be performed dynamically (e.g. by a continuous ramping of the DUT temperature and synchronous measurements of the voltage outputs of the DUTs). This challenging requirement was driven by the thermal hysteresis of the voltage references which would invalidate the static measurements of TC_{Vo}. It is believed that the manufacturers use the dynamic testing method for the same reasons [182].

A series of bench experiments showed that the temperature sweep should not be slower than 0.1 °C/s. Such a fast trend required a redesign of the test system. The DMM4050 used in the previous TID experiment needed more than 2 s to perform a single voltage measurement. Another factor was the limited speed of the mechanical

multiplexing of the DUTs (based on relays). The resulting duration of a single DUT output voltage measurement would be 2.5 s. Such a duration was not acceptable for the TID-TC experiment.

In order to accelerate the measurement of the DUT output voltages, a high-speed, 7.5 digit digital multimeter (Keithley DMM7510 [291]) was used. It was configured to the highest possible resolution using 10 NPLC (number of power line cycles) to suppress the noise from the power line and other sources.

To further speed-up the measurement process, the DMM7510 differential input multiplexing was provided by CMOS analogue multiplexer devices [336]. Although this solution significantly increased the switching speed, it also brought another challenge to the design; the CMOS multiplexer devices could not be placed in the DUT container due to a high risk of radiation-induced damage [337]. Hence, the multiplexers were placed close to the multimeter and connected via 15 m long shielded twisted cables directly to the DUTs. The number of connectors was limited to suppress the thermoelectric errors and noise. The multiplexors were supplied by a low noise power supply and controlled directly by the multimeter’s digital outputs via optocouplers. This hardware solution allowed the multimeter to control the whole measurement process via an internal TSP test script (see chapter 6.3.2).

The DUTs were biased using Keysight E3631A DC power supply. The E3631A was controlled by the PC which also allowed DUT supply current to be monitored. DUT1 and DUT2 were biased by 12 V, and the other DUTs were biased by 5 V. The measurement cycled was timed, so the unbiased DUTs were biased only in 7 % of the duration of the experiment. Both the input and output of each DUT was decoupled using X7R ceramic capacitors of 100 nF capacitance.

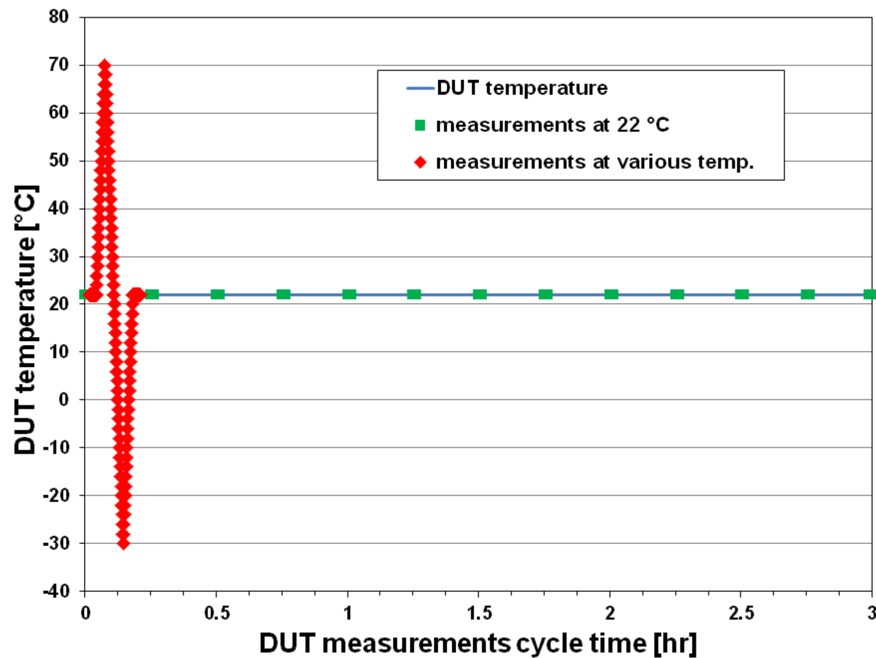

Fig. 8.9: The timing of the DUT measurement cycle, including the temperature profile. DUT output voltage was measured (22 °C) every 15 minutes during the idle time (green squares) and at various temperatures during the temperature sweep (red dots).

8.3.3 The timing of the TID-TC measurements

Regular measurements of DUT output voltage were made, either at the idle temperature of 22 °C or during the temperature sweep, as defined in Fig. 8.9. During the idle temperature measurements, the DMM7510 was configured to provide the highest resolution and accuracy by enabling auto-zeroing, line synchronisation and averaging. The idle temperature measurements were made every 15 minutes. The temperature sweep was a ramp profile using a trend of 0.4 °C/s to achieve fast measurement and shorten the sweep to less than 12 minutes. The temperature sweep was performed every 3 hours, which corresponds to a cumulated dose of 1.08 krad(Si) per sweep.

8.3.4 The irradiation setup of the VREF TID-TC experiment

The irradiation details of the TID-TC experiment were identical to the irradiation performed during the VREF TID experiment (see section 8.2.4). As shown in Appendix D.4, the DUTs were placed in a modified version of the hermetic container originally built for the MOS experiments. All the active parts in the container (the TEC, fan, sensors and silica gel bags) were replaced with fresh devices.

8.3.5 Results of the VREF TID-TC experiment

The experiment started with installing the test system in the irradiation facility and running pre-irradiation measurements, during which the entire system stabilised. The second phase was the irradiation up to a TID of 100 krad(Si), followed by 70 hours of annealing. The third phase was extended annealing, during which the entire experiment was placed in an electronics laboratory.

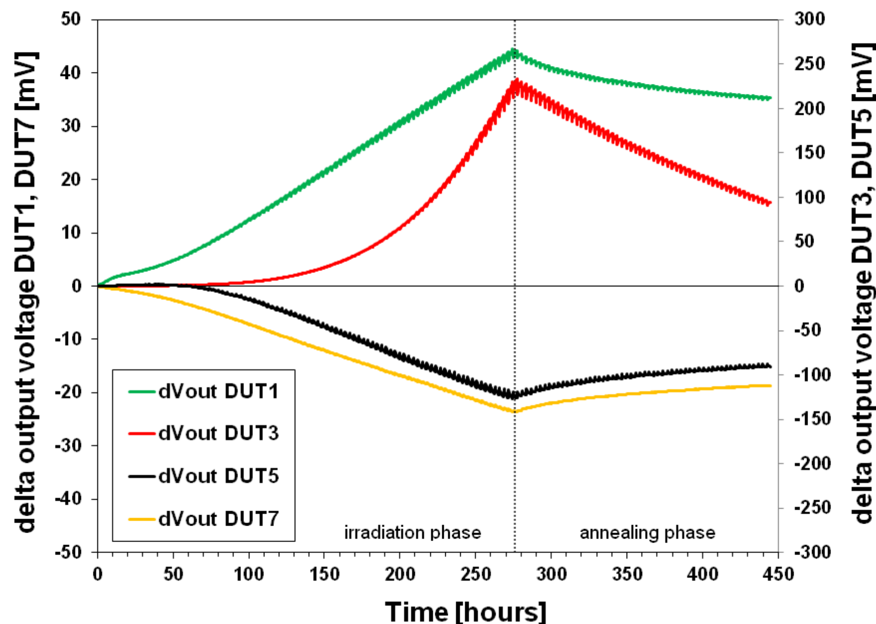

Fig. 8.10: Degradation and recovery of the output voltage of the unbiased DUTs during the irradiation and annealing phases.

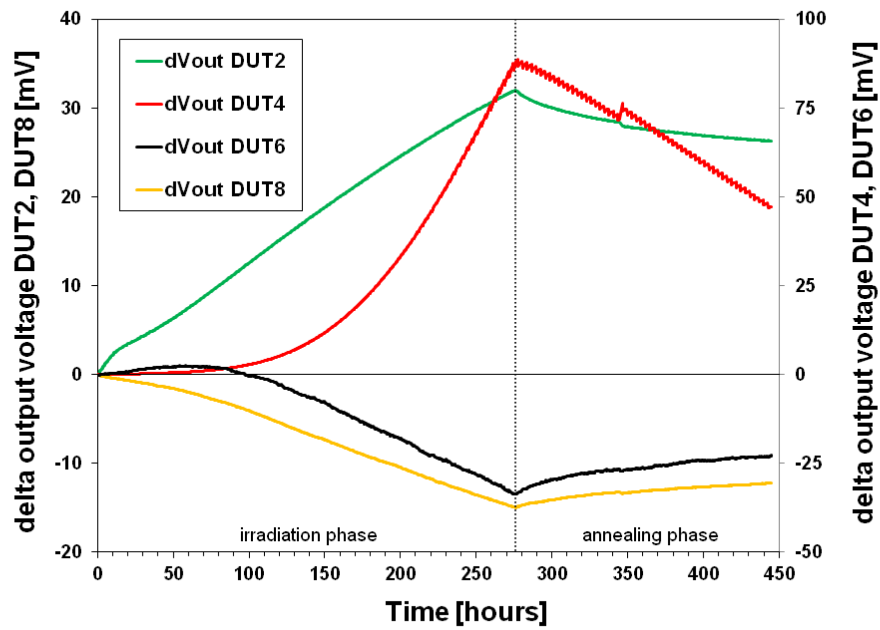

Fig. 8.11: Degradation and recovery of the output voltage of the biased DUTs during the irradiation and annealing phases.

The radiation-induced changes in the output voltage of the unbiased DUTs are plotted in Fig. 8.10. The same record for biased devices is shown in Fig. 8.11. A significant bias sensitivity can be seen when the scales of the charts are compared. The glitches on the DUT2 and DUT4 annealing curves were caused by the absence of the biasing during the transport of the test system to the electronics laboratory.

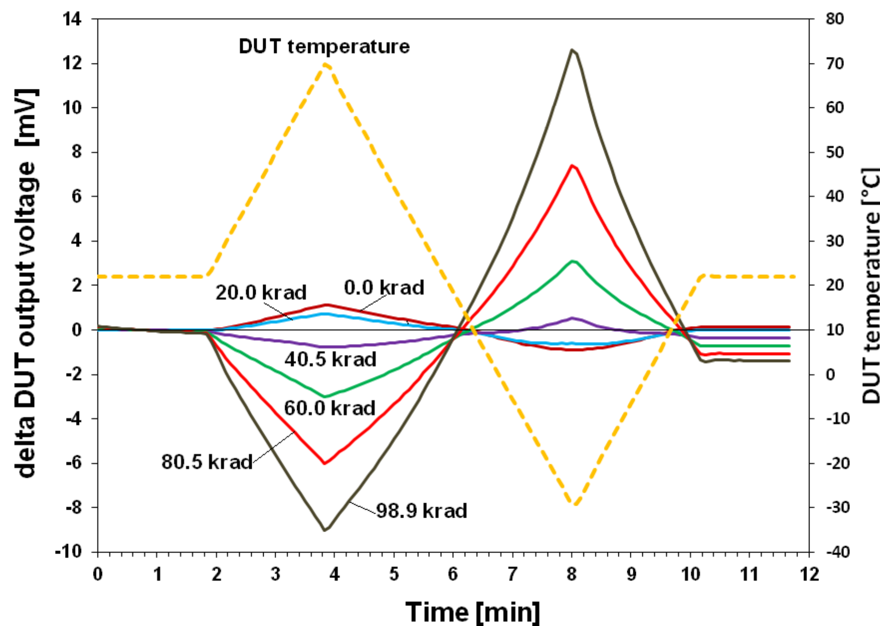

Fig. 8.12: TID-induced change of the DUT1 response to the temperature sweep. Only selected temperature sweeps at TID steps of 20 krad are displayed.

The chart in Fig. 8.12 shows how the TID gradually changed the response of the DUT1 to the temperature sweeps. The temperature sweep data have been processed to obtain the temperature coefficients (temperature drift TC_{Vo} as defined in chapter 4.3.2). The TC_{Vo} of each DUT was calculated using linear regression during the cooling part of the TC_{Vo} sweep from +70 to -30 °C. The resulting changes in TC_{Vo} of unbiased DUTs can be seen in Fig. 8.13 and biased devices are shown in Fig. 8.14 respectively.

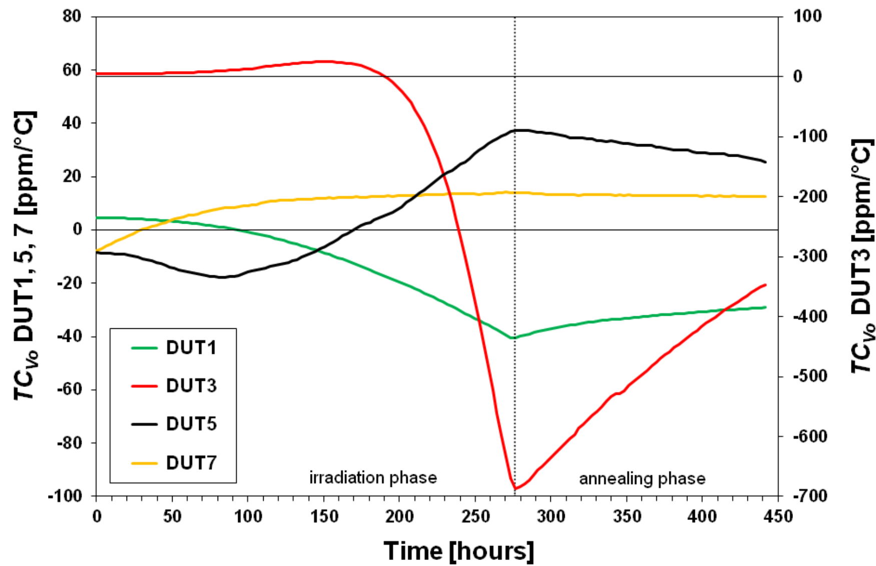

Fig. 8.13: The change and recovery of the temperature coefficients of the unbiased DUTs during the irradiation and annealing phases.

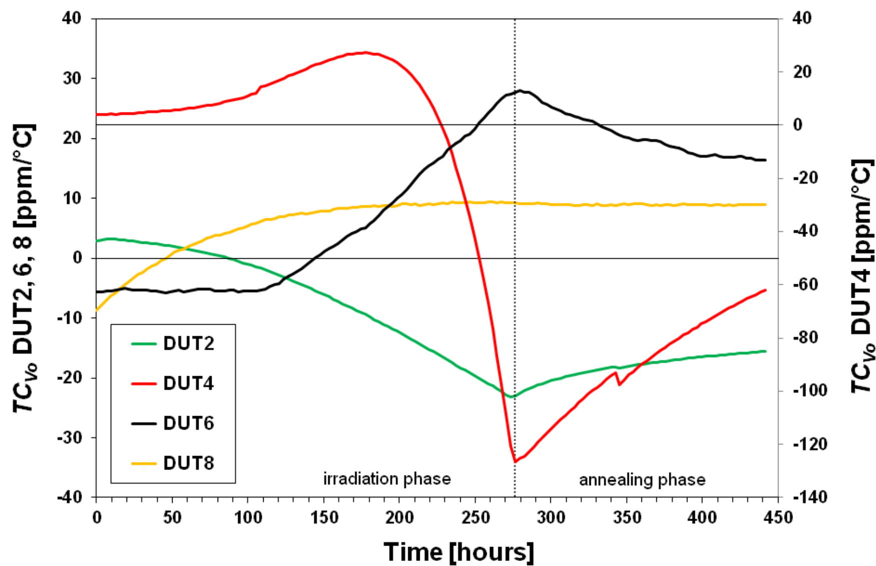

Fig. 8.14: The change and recovery of the temperature coefficients of the biased DUTs during the irradiation and annealing phases.

8.3.6 Discussion of the results of the VREF TID-TC experiment

The recorded data suggest excellent functionality of the test system designed for this experiment. The data show that a measurement resolution of better than 10 µV can be achieved by the ISTM test system, despite the fact that the measurement system was placed outside the irradiation facility and complex cabling of 15 m length was used.

The observed TID-induced degradation of the output voltage of the DUTs was compared with the results from the previous VREF TID experiment as the DUTs were from the same lots, and the measurements were under the same conditions. The shape of the resulting curves (Fig. 8.10 and Fig. 8.11) was the same, but the magnitude of the degradation was significantly lower during this experiment (this time the maximum degradation was about 70 % lower than during the previous experiment on unbiased DUTs and 50 % on the biased DUTs). This could be explained by thermal annealing during the temperature sweeps, which lowered the overall degradation. The DUT output voltage, in general, does not fully return to the initial value at the end of the temperature sweep (Fig. 8.12). This is caused by the thermal hysteresis, and it gets stronger with the dose and can also be observed as a ripple on the plots in Fig. 8.10 and Fig. 8.11.

The initial pre-irradiation readings of the temperature coefficients were in close agreement with the datasheet specifications. Depending on the type of DUT, the TC_{Vo} readings were varying from ±0.05 to ±0.2 ppm/°C showing excellent stability and repeatability of the developed ISTM measurement method. The TID-induced changes of the temperature coefficients were rather complex, as can be seen in Fig. 8.13 and Fig. 8.14, but they had one feature in common: the initial polarity of the TC_{Vo} changed with the TID. That means there was an initial TID window during which the TC_{Vo} was getting lower, and at some certain TID the TC_{Vo} was practically zero. A similar phenomenon was observed on TC_{VT} of PMOS transistors as shown in sections 7.2.5 and 7.2.8. TC_{Vo} of DUT7 and DUT8 showed saturation at 50 krad at a TC_{Vo} of opposite polarity, but the similar value to the starting TC_{Vo}. All the other DUTs continued to change the TC_{Vo} significantly. The worst case was the TC_{Vo} of DUT3, which increased by more than two orders of magnitude. A similar result, from DUT1, is in agreement with a TID report published by Texas Instrument [191], where comparable results were reported. Such a high value of TC_{Vo} would be unacceptable for a practical precision DAQ application; as demonstrated in Fig. 4.7 a TC_{Vo} of an order of 100s ppm/°C would degrade the measurement accuracy to 10-bit or worse.

The results of the COTS voltage reference TID-TC experiment were presented at the RADECS 2017 conference [338].

8.4 Conclusions of voltage references experiments

The TID experiments with voltage references were successful in obtaining detailed data on the radiation-induced degradation of the selected voltage reference devices and validating the performance of the proposed ISTM test method.

The results of the TID tests were interpreted in two ways: firstly, the performance of VREF devices was evaluated as if the devices were used as reference voltage sources in a space DAQ system; secondly, the compliance with the planned in-orbit experiment was analysed.

To enable analysis of the TID-induced degradation of each type of voltage reference device, the test results were summarised in the Tab. 8.3 to Tab. 8.11. Each reported parameter was calculated from the average readings within every DUT group, and has been expressed in ppm to represent a measurement error it would induce to a space DAQ system. Results at particular radiation dose steps and after seven days of annealing are shown for the following sources of measurement error:

- ΔV_{OERR} represents the measurement error induced by the TID-induced shift in VREF output voltage (assuming the system was calibrated prior to the launch as discussed in section 2.1.2).
- V_{LNRERR} refers to the measurement error caused by VREF line regulation changes and is expressed by the V_{LNRERR} factor for a 5 % change in supply (bias) voltage to the VREF device.
- V_{LDRERR} refers to the load regulation error caused by a change of the loading of the VREF output by 0.1 mA.
- TC_{VOERR} is a measurement error induced by the temperature drift; it was calculated for change in the ambient temperature by 20 °C.

The listed error sources were combined into the total measurement error using the formula (2.4). An equivalent ADC resolution was calculated assuming a requirement of having the VREF-induced measurement error at 1 LSB using the equation (4.2).

There were in total eight DUT groups (four VREF types, each type biased and unbiased as defined in Tab. 8.1 and Tab. 8.2). Hence, the results of the VREF TID experiments are summarised in eight tables labelled Tab. 8.3 to Tab. 8.10.

Tab. 8.3: Summary of TID-induced degradation of LT1236 unbiased devices.

TID level / Meas. error	**0 krad(Si)**	**5 krad(Si)**	**10 krad(Si)**	**20 krad(Si)**	**50 krad(Si)**	**100 krad(Si)**	**7 days anneal**
ΔV_{OERR} [ppm]	0	977	2087	3902	8709	18495	14742
V_{LNRERR} [ppm]	1	0	-3	-6	-13	-35	-21
V_{LDRERR} [ppm]	-2	-2	-2	-3	-8	N/A	N/A
TC_{VOERR} [ppm]	88	91	82	60	-129	-812	-582
Total error [ppm]	88	982	2089	3903	8710	18513	14754
ADC res. [bits]	13.5	10.0	8.9	8.0	6.8	5.8	6.1

Tab. 8.4: Summary of TID-induced degradation of LT1236 biased devices.

TID level / Meas. error	**0 krad(Si)**	**5 krad(Si)**	**10 krad(Si)**	**20 krad(Si)**	**50 krad(Si)**	**100 krad(Si)**	**7 days anneal**
ΔV_{OERR} [ppm]	0	810	1216	2019	4604	7316	5653
V_{LNRERR} [ppm]	0	1	1	2	6	10	8
V_{LDRERR} [ppm]	-2	-2	-2	-2	-3	-7	-5
TC_{VOERR} [ppm]	56	64	55	36	-94	-462	-311
Total error [ppm]	56	813	1217	2019	4605	7331	5662
ADC res. [bits]	14.1	10.3	9.7	9.0	7.8	7.1	7.5

Tab. 8.5: Summary of TID-induced degradation of ADR440 unbiased devices.

TID level / Meas. error	**0 krad(Si)**	**5 krad(Si)**	**10 krad(Si)**	**20 krad(Si)**	**50 krad(Si)**	**100 krad(Si)**	**7 days anneal**
ΔV_{OERR} [ppm]	0	34	165	734	15412	284712	344882
V_{LNRERR} [ppm]	4	5	5	8	5	-1140	-1108
V_{LDRERR} [ppm]	-3	-3	-4	-5	-14	6	19
TC_{VOERR} [ppm]	83	89	97	123	470	-13723	-6940
Total error [ppm]	83	95	191	745	15419	285045	344954
ADC res. [bits]	13.6	13.4	12.4	10.4	6.0	1.8	1.5

Tab. 8.6: Summary of TID-induced degradation of ADR440 biased devices.

TID level / Meas. error	**0 krad(Si)**	**5 krad(Si)**	**10 krad(Si)**	**20 krad(Si)**	**50 krad(Si)**	**100 krad(Si)**	**7 days anneal**
ΔV_{OERR} [ppm]	0	-9	54	424	11491	77417	62542
V_{LNRERR} [ppm]	5	5	6	8	3	-164	-147
V_{LDRERR} [ppm]	-4	-4	-4	-5	-8	9	9
TC_{VOERR} [ppm]	78	81	92	115	424	-2529	-1243
Total error [ppm]	78	82	107	439	11499	77459	62554
ADC res. [bits]	13.6	13.6	13.2	11.2	6.4	3.7	4.0

Tab. 8.7: Summary of TID-induced degradation of LT1460 unbiased devices.

TID level / Meas. error	**0 krad(Si)**	**5 krad(Si)**	**10 krad(Si)**	**20 krad(Si)**	**50 krad(Si)**	**100 krad(Si)**	**7 days anneal**
ΔV_{OERR} [ppm]	0	601	1076	-126	-32632	-99869	-80650
V_{LNRERR} [ppm]	6	4	4	51	471	1004	763
V_{LDRERR} [ppm]	-36	-39	-50	-96	-118	-16	-89
TC_{VOERR} [ppm]	-177	-202	-250	-330	-143	731	460
Total error [ppm]	181	635	1106	369	32636	99877	80655
ADC res. [bits]	12.4	10.6	9.8	11.4	4.9	3.3	3.6

Tab. 8.8: Summary of TID-induced degradation of LT1460 biased devices.

TID level / Meas. error	**0 krad(Si)**	**5 krad(Si)**	**10 krad(Si)**	**20 krad(Si)**	**50 krad(Si)**	**100 krad(Si)**	**7 days anneal**
ΔV_{OERR} [ppm]	0	524	1123	2098	-2843	-18464	-12260
V_{LNRERR} [ppm]	6	9	8	17	111	244	171
V_{LDRERR} [ppm]	-38	-41	-47	-70	-125	-119	-125
TC_{VOERR} [ppm]	-100	-81	-92	-119	35	513	329
Total error [ppm]	107	532	1128	2103	2848	18473	12267
ADC res. [bits]	13.2	10.9	9.8	8.9	8.5	5.8	6.3

Tab. 8.9: Summary of TID-induced degradation of ADR03 unbiased devices.

TID level / Meas. error	**0 krad(Si)**	**5 krad(Si)**	**10 krad(Si)**	**20 krad(Si)**	**50 krad(Si)**	**100 krad(Si)**	**7 days anneal**
ΔV_{OERR} [ppm]	0	-968	-1832	-3761	-10524	-20740	-16439
V_{LNRERR} [ppm]	3	12	22	40	76	94	76
V_{LDRERR} [ppm]	-2	-2	-3	-4	-9	-14	-10
TC_{VOERR} [ppm]	-163	-86	-9	90	232	277	250
Total error [ppm]	163	972	1832	3762	10527	20743	16441
ADC res. [bits]	12.6	10.0	9.1	8.1	6.6	5.6	5.9

Tab. 8.10: Summary of TID-induced degradation of ADR03 biased devices.

TID level / Meas. error	**0 krad(Si)**	**5 krad(Si)**	**10 krad(Si)**	**20 krad(Si)**	**50 krad(Si)**	**100 krad(Si)**	**7 days anneal**
ΔV_{OERR} [ppm]	0	-596	-1047	-2088	-5873	-10996	-8611
V_{LNRERR} [ppm]	2	10	16	29	47	49	36
V_{LDRERR} [ppm]	-2	-3	-3	-4	-6	-7	-5
TC_{VOERR} [ppm]	-182	-116	-54	27	148	184	178
Total error [ppm]	182	607	1049	2088	5875	10997	8612
ADC res. [bits]	12.4	10.7	9.9	8.9	7.4	6.5	6.9

For all the tested devices it was clear that the main source of the initial (0 krad(Si)) measurement error was the temperature drift TC_{VOERR}. This result was expected as discussed in chapter 2.1.1. For thermally stabilised terrestrial DAQ systems, the overall measurement error could be maintained in order of a few ppm.

As soon as the irradiation started, the TID-induced shift in VREF output voltage ΔV_{OERR} became a significant and dominant error source. The ΔV_{OERR} was orders of magnitude stronger than the other error sources.

The line and load regulation errors were low for doses below 50 krad(Si), and in most cases, they were typically lower than temperature drift errors by an order of magnitude. For the higher TID levels, the line and load regulation errors became stronger but still less significant than the ΔV_{OERR} and TC_{VOERR}, respectively. The results for the load regulation error V_{LDRERR} were not available for the unbiased LT1236 devices as these devices failed to deliver output voltage under loaded output. As shown in Tab. 8.3, this problem started with TID levels above 50 krad(Si). Such a behaviour can be interpreted as a functional failure of the output stage of the devices. The biased devices were free of this effect.

The TID-induced changes of the temperature drift were also changing significantly with the higher TID levels, above 50 krad(Si). The typical phenomenon was a change of the polarity of the TC_{Vo}. This result is very important for potential temperature drift compensation techniques using measured ambient temperature. An interesting product of this behaviour is a virtually zero value of the TC_{Vo} at particular TID level. For example, the unbiased ADR03 devices would have negligible TC_{Vo} at ~12 krad(Si).

Finally, the TID-induced total measurement errors were compared between the VREF types and their bias conditions. The summary of the total measurement errors is shown in Tab. 8.11. The values are expressed in percentage rather than ppm to allow easier comparison of the errors.

The best performance was measured for ADR440 and LT1460 devices for TID levels up to 20 krad(Si). However, the unbiased ADR440 become the worst candidates for higher doses applications, as the total measurement error reached nearly 30 % at doses of 100 krad(Si) and there was even a reverse annealing phenomenon observed. In contrast, the LT1236 and ADR03 devices had a poorer performance at lower TID levels but suffered lower degradation at higher doses.

Tab. 8.11: Summary of TID-induced total measurement errors of all VREF devices.

TID level / Total meas. error	**0 krad(Si)**	**5 krad(Si)**	**10 krad(Si)**	**20 krad(Si)**	**50 krad(Si)**	**100 krad(Si)**	**7 days anneal**
LT1236 unbiased [%]	0.009	0.098	0.21	0.39	0.87	1.85	1.48
LT1236 biased [%]	0.006	0.081	0.12	0.20	0.46	0.73	0.57
ADR440 unbiased [%]	0.008	0.010	0.019	0.07	1.54	28.5	34.5
ADR440 biased [%]	0.008	0.008	0.011	0.04	1.15	7.75	6.26
LT1460 unbiased [%]	0.018	0.063	0.11	0.04	3.26	9.99	8.07
LT1460 biased [%]	0.011	0.053	0.11	0.21	0.28	1.85	1.23
ADR03 unbiased [%]	0.016	0.097	0.18	0.38	1.05	2.07	1.64
ADR03 biased [%]	0.018	0.061	0.10	0.21	0.59	1.10	0.86

The compatibility of the tested devices with the in-orbit experiment will be also discussed in detail in the particular section of chapter 10. However, at this stage, it could be concluded that the tested parts were satisfactory as they can deliver acceptable measurement error up to TID levels expected for the experiment (10 to 20 krad(Si)). An exception would be the LT1236 device, which is not suitable for the in-orbit experiment due to the 12 V supply voltage requirement. Unfortunately, the buried Zener VREF devices are available only for the reference voltages of at minimum 5 V (as discussed in section 4.3.1).

The validation of the performance of the specially constructed in-situ test systems could be performed only using their own results; there was no means of comparing the results with measurements performed by other independent (ideally more accurate) systems. For this reason, the validation could be performed only by observing the noise and repeatability of the readings under stable conditions and by comparing the test results with the typical values specified by the manufacturers in the datasheets.

The detailed analysis of the initial (pre-irradiation) measurement showed that the noise levels could be maintained below ±10 μV (Fig. 8.2), which was only an order of magnitude higher than the LSB size of the multimeters used. This excellent result was a product of complex shielding and high-performance test instrumentation combined with low noise power supplies and decoupling. The typical variation in the measurements of the TC_{Vo} showed that the developed test system could reliably measure with repeatability of ±50 ppb/°C. This excellent result was achieved by using the precision test system together with the custom DTC temperature controller and STS software.

9 A/D CONVERTERS TID EXPERIMENT

The final component-level TID experiment in this PhD work was designed to measure TID-induced degradation of two types of high-resolution A/D converters (ADCs). A custom-developed ISTM tester was used to perform all measurements. This solution was also chosen to allow practical demonstration of the NewSpace style low-cost testing as discussed in chapter 5.

9.1 Goals of the ADC TID experiment

The key goal of the ADC experiment was to obtain test data with fine dose resolution. As demonstrated in section 4.4.3, there was a lack of such test results. The particular goals/tasks of the ADC experiment were as follows:

- To identify appropriate test samples (DUTs)
- To design and manufacture an in-situ test system capable of measuring static parameters (DC errors), DUT supply current and temperature
- To perform a TID experiment and analyse the TID-induced changes
- To evaluate the suitability of the low-cost ISTM method for ADC testing

9.2 The ADC devices under test

The COTS devices used in the ADC experiment were chosen using the following selection criteria (see section 4.4 for definitions):

1. Delta-sigma modulation, 24 bits resolution
2. External reference and clock source (to avoid TID degradation of the internal sources to influence the test results)
3. SPI bus (I2C is not reliable when long cables are to be driven)
4. SOIC-8 package to keep the thermal compatibility with the DUTs used previously (for potential future TID-TC experiments)

Based on these requirements, two candidate devices were identified [339], [340]. Their key parameters are summarised in Tab. 9.1.

Tab. 9.1: Key parameters of the selected ADC devices as specified in [339] and [340].

ADC part number/ parameter	LTC2400IS8	ADS1251U
Manufacturer, package	Linear Technology, SOIC-8	Texas Instruments, SOIC-8
VREF source	external	external
Clock source	internal/external	external
Nominal resolution [bits]	24	24
INL [ppm of V_{REF}]	2 typical, 10 max	2 typical, 10 max
Offset Error [ppm of V_{REF}]	0.5 typical, 2 max	30 typical, 100 max
Gain Error [ppm of V_{REF}]	4 typical, 10 max	1000 typical, 10000 max
ADC noise [ppm of V_{REF}]	0.6 typical (RMS)	1.5 typical, 2.5 max (RMS)

When introduced in 1999, the LTC2400 was the industry's first No Latency delta-sigma ADC [341]. As shown in the block diagram in Fig. 9.1 it is equipped with an automatic offset and full-scale calibration, an internal oscillator, a sinc^4 digital filter and flexible 3-wire digital interface which is compatible with SPI and MICROWIRE protocols. The delta-sigma technology provides single cycle settling time which is suitable for multiplexed applications [339]. LTC2400 was constructed to serve as an ADC for temperature measurement and high-resolution instrumentation applications, such as digital multimeters [342].

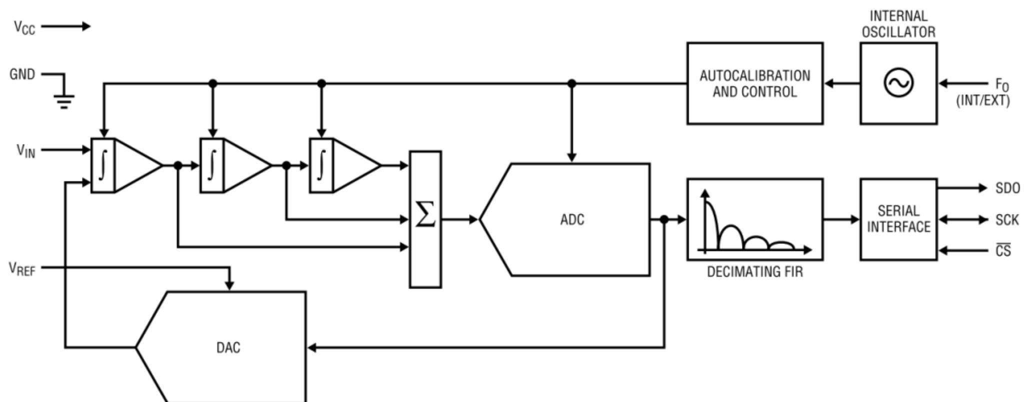

Fig. 9.1: Functional block diagram of the LTC2400. Picture adapted from [339].

The second selected ADC device was the ADS1251 [340]. As can be seen in the block diagram in Fig. 9.2, the design of the ADS1251 is similar to LTC2400. However, there is a variety of differences between these ADCs. ADS1251 contains a fully differential analogue input, the modulator is of the fourth order, and the digital filter is of sinc^5 response. The auto-calibration circuit is not implemented in the ADS1251. The digital interface is based only on two signals (clock pin SCLK and combined pin DOUT/DRDY). ADS1251 has no internal oscillator circuit; the clock for the modulator must be provided externally. Although this simplifies the hardware design of the interface to the MCU; it makes the communication software more complicated.

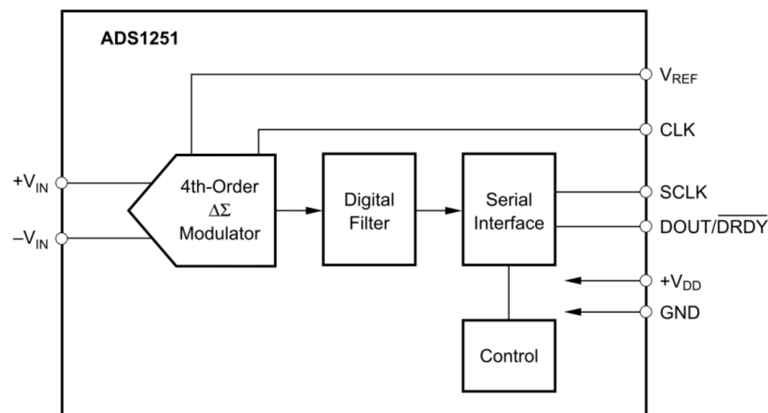

Fig. 9.2: Block diagram of the ADS1251. Picture sources from [340].

9.3 ADC in-situ TID test system

As can be seen in Fig. 9.3, the top-level design of the ADC test system followed the ISTM philosophy defined in section 5.3.1. The automated test equipment, or ADC tester, consisted of: a set of custom-developed hardware; Tektronix TDS2012B digital storage oscilloscope (DSO); and a test PC, which ran the test software STS.

The custom test hardware was responsible for generating the analogue test signals for the DUTs and communicating with them to control and read the results of their A/D conversions. The TDAC (test D/A converter) circuit was based on precision, 16-bits DAC manufactured by Texas Instruments under part number DAC8564D [343]. There was a common VREF source used by both the TDAC and the DUTs. The VREF source consisted of ADR443B XFET voltage reference [344] and an ultra-low noise operational amplifier OPA2350PA, which acted as a double unity-gain buffer assuring isolation of the DUTs from the TDAC reference input.

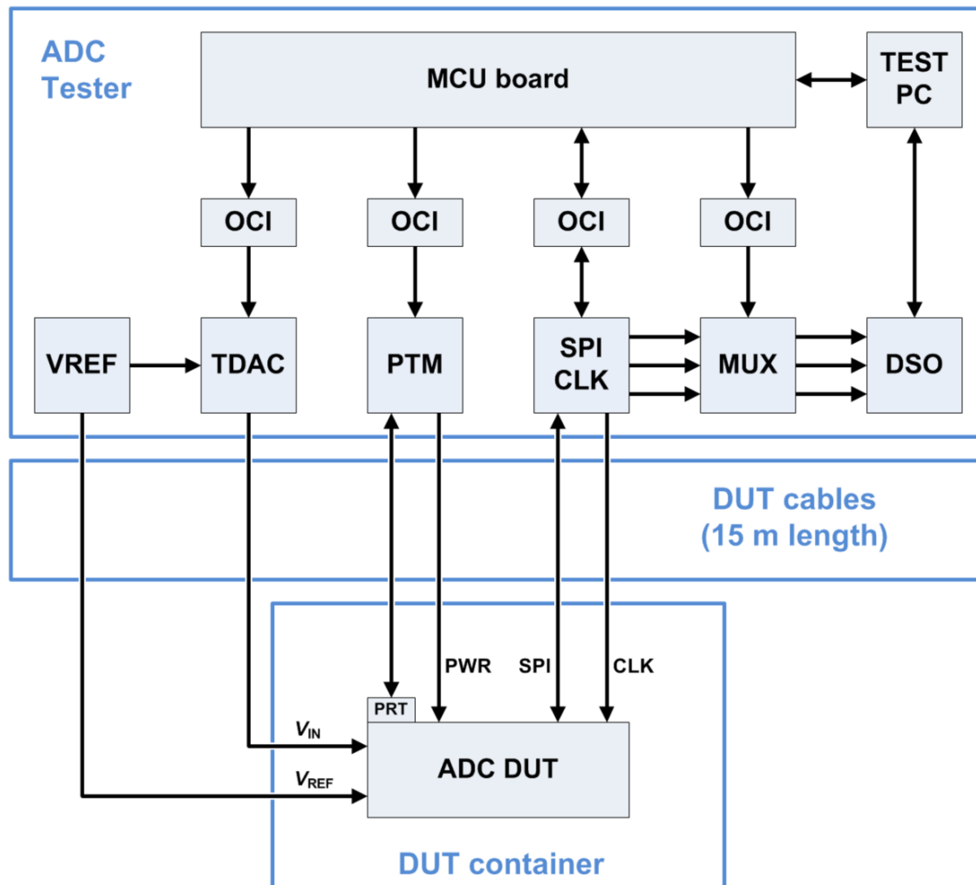

Fig. 9.3: Block diagram of one channel of the ADC test system. It consisted of the test hardware (placed outside the irradiation cell), a set of cables and DUT container placed in the irradiation cell.

The power supply currents and the temperature of the DUTs were monitored by the PTM (power and temperature monitor). The PTM consisted of the ADS1248 ADC module developed for the DTC system (see section 6.5.2). This ADC module was used

to measure the DUT temperature using PRT sensor identical to the one used in the DTC system. The DUT supply current was sensed by ultra-low *TC* shunt 0.1 Ω resistors, whose differential voltages were amplified by instrumentation amplifiers AD8237 and digitalised by the ADS1248. PTM also allowed cycling of the DUT power supply in case the DUT needed a hard-restart. All PTM channels were calibrated using the DMM4050 multimeter. The decoupling of the DUTs consisted of 10 µF tantalum and SMD 100 nF X7R ceramic capacitors soldered directly to the DUT pins.

The digital interfaces for the DUT (including clock signals) were generated by the MCU and buffered by 74HC7541N Octal Schmitt trigger buffers/line drivers. The termination of the digital lines was provided by serial termination resistors. The waveforms of the DUT digital communication were captured by the DSO, which was connected to the particular digital lines via multiplexors.

The whole ADC tester was controlled by the common MCU module, which was defined in section 6.4.3. All MCU signals were galvanically isolated via four optocoupler isolator (OCI) modules. This solution (in combination with six, independent, linear DC power supply units) not only allowed suppression of digital signal induced noise but also isolation of the ground lines. This rather complex design allowed full separation of the ground lines up to a single point on the DUT board in which all the ground lines were connected. Therefore both the DC and AC ground loop errors could be practically avoided.

9.4 ADC test conditions during the experiment

This section summarises the key hardware and software conditions of the test procedure used during the ADC experiment.

The voltage reference source was providing a 2.5 V reference voltage that was shared between the TDAC and the DUTs. The reference voltage for DUTs was buffered by the operational amplifiers to avoid potential interference between these circuits. Therefore the TDAC and the VREF inputs of the DUTs were practically on the same potential, and the only voltage difference was caused by the imperfections (errors) of the operational amplifiers. The most important errors included noise, temperature drift of the input offset voltage and the PSRR (power-supply rejection ratio). According to the datasheet, these errors were in the order of microvolts [345]. Therefore the voltage reference error (or full-scale error) was estimated to be a few ppm.

The DUTs were supplied by an external clock from the ADC tester. The clock signals were generated by the counter/timer units in the MCU and were selected to suppress the mains frequency (50 Hz). The clock sources were calibrated within the listed tolerance using laboratory counter 53220A, as specified in Tab. 9.2.

Tab. 9.2: Clock settings for the ADCs as specified in [339] and [340].

ADC type / clock parameter	LTC2400IS8	ADS1251U
Clock frequency	128.0 kHz ±0.01 %	3.84 kHz ±0.01 %
Conversion time	160	100
50 Hz rejection	>110 dB	>200 dB

Only one piece of each ADC type was tested. The DUTs were tested once per hour. The DUTs were in sleep mode during the idle time between the tests. During the sleep mode, the DUTs were biased. However, the clock sources were disabled. This mode allowed the supply current of the devices to drop to levels of microamperes. During the testing, only the DUT under test was woken-up, and the clock was provided. This solution suppressed a potential interference between the DUTs. When woken up, the DUTs were reset using a power-up reset sequence. After the reset sequence, a continuous conversion mode was used.

The key challenge was to minimise the test time. To suppress the noise, every measurement was performed multiple times, and an average value was used. Assuming the conversion times shown in Tab. 9.2, the full transfer characteristics (65536 points) would take approximately 29 hours to measure (averaging of ten samples). This is a common issue of ADC/DAC testing which may take days to perform. This is a problem even for ordinary functional testing because it is complicated to keep the electrical and environmental conditions stable for such a long time [346]. To minimise the duration of the ADC transfer characteristic measurements, only a limited set of steps was measured. As defined in Tab. 9.3, there were in total 46 steps distributed among the whole range of TDAC. The transfer characteristic was divided into nine sectors, during which five adjacent TDAC steps were used. This way the *DNL* could also be measured. However, it was limited to 16-bit resolution. The start and stop steps were selected with 4 mV margin allowing for initial offset and gain errors of both TDAC and DUTs. It should be noted there was an additional step number 46 during which the start voltage was measured again - the additional step allowed for the evaluation of the repeatability of the measurements during the pre-irradiation phase and measurement of the TID-induced shift during the measurements of the transfer characteristics during the irradiation.

Tab. 9.3: Definition of ADC transfer characteristic measurement steps.

Transfer char. section	Test step number	TDAC input code [-]		Ideal DUT V_{IN} [mV]	
		start	stop	start	stop
1	1 to 5	100	104	3.81	3.97
2	6 to 10	8190	8194	312.42	312.58
3	11 to 15	16382	16386	624.92	625.08
4	16 to 20	24574	24578	937.42	937.58
5	21 to 25	32765	32769	1249.89	1250.04
6	26 to 30	40958	40962	1562.42	1562.58
7	31 to 35	49149	49153	1874.89	1875.04
8	36 to 40	57341	57345	2187.39	2187.54
9	41 to 45	65400	65404	2494.81	2494.96
-	46	100	-	3.81	-

Similarly to previous experiments, the MIF cell was used for the irradiation phase of the ADC experiment. A dose rate of 360 rad(Si)/hr was used. The dosimetry was performed only prior to the setup of the experiment in the cell. There was no dosimetry during the experiment as the mechanical structure of the DUT container did not allow the ion chamber to be placed permanently in the container.

9.5 Initial testing of the ADC test system at MIF facility

As soon as the experiment was ready for the irradiation phase, it was placed in the MIF facility. After 20 hours of thermal settling, a set of measurements was performed in order to evaluate the noise of the whole system. The plot in Fig. 9.4 shows measured noise of the ADCs at the mid-scale point of $V_{IN} = 1.25$ V. There were 14000 samples acquired during the LTC2400 test and 54000 for ADS1251. The ADCs were uncalibrated and a difference between their outputs of 0.4 mV, was seen.

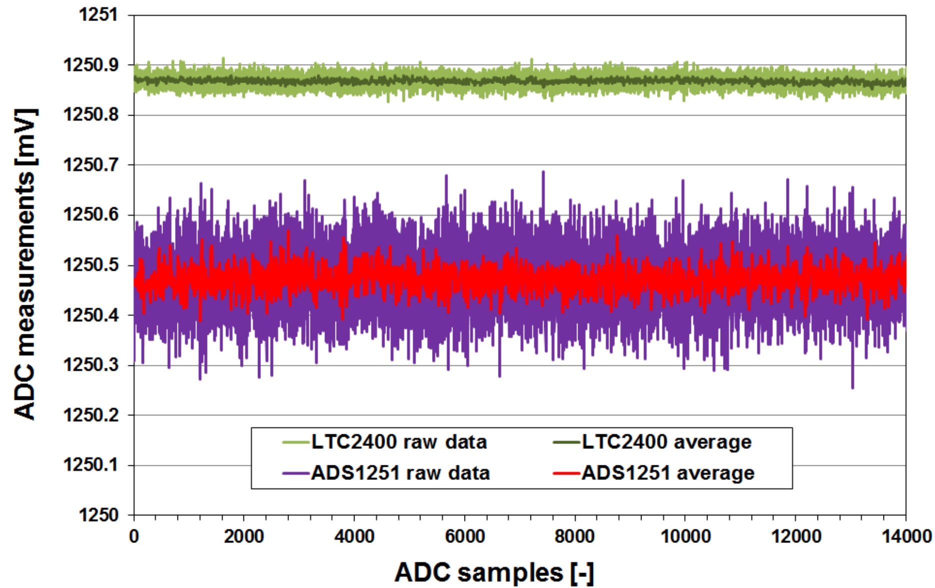

Fig. 9.4: Plot of the mid-scale noise measured during testing in the MIF facility prior to the TID experiment. Averaging of ten ADC samples was used for the average lines.

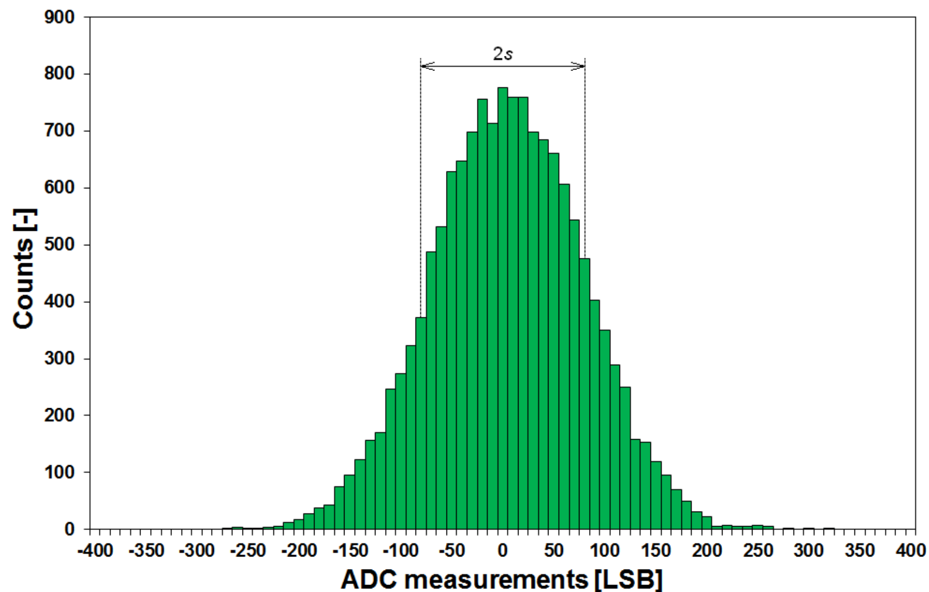

Fig. 9.5: Histogram of the mid-scale noise of the LTC2400 including its standard deviation.

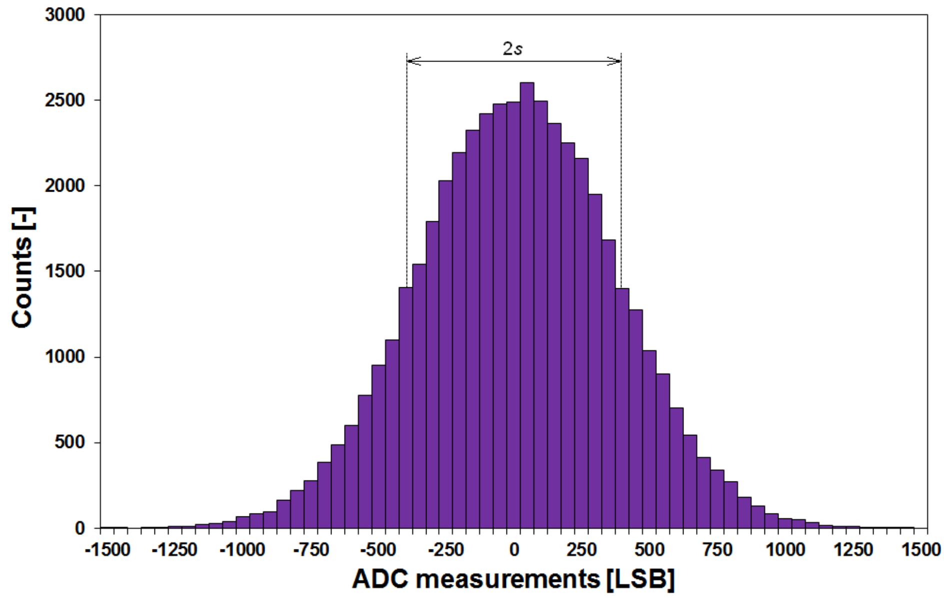

Fig. 9.6: Histogram of the mid-scale noise of the ADS1251 including its standard deviation.

Additionally, the raw ADC data from noise measurements were processed statistically. In order to evaluate the nature of the noise, histograms were plotted. Both the resulting charts (Fig. 9.5 and Fig. 9.6) showed that the noise could be approximated as Gaussian. Such noise data could be used to calculate the RMS value of the noise s_{RMS} using standard deviation s defined as follows [347]:

$$s_{\mathrm{RMS}} = s = \sqrt{\frac{\sum_{i=1}^{n}(x_i - \bar{x})^2}{n-1}}, \tag{9.1}$$

where n is the number of samples, x_{i} are the measured samples, $\bar{x}$ is the mean value of the samples. The effective resolution N_{ef} of the ADC could be then calculated using the following formula [348]:

$$N_{\mathrm{ef}} = \log_2\left(\frac{2^{\mathrm{N}}}{s_{\mathrm{RMS}}}\right), \tag{9.2}$$

where N is the nominal resolution of the ADC (N = 24 for both tested ADCs), s_{RMS} is the RMS value of the ADC noise expressed in LSBs.

Firstly, the effective resolution of the bare ADCs was calculated for both devices using the formulas (9.1) and (9.2) and the datasheet values of the RMS noise as shown in Tab. 9.1. Secondly, the measured noise data sets were processed to calculate the effective resolution of the whole ADC test system using raw noise data and average values obtained from 10, 20, 30 and 40 samples. The results of the calculations of the effective resolutions are summarised in Tab. 9.4.

Tab. 9.4: Effective resolution of the tested ADCs and the whole test system.

Data source	N_{ef} of LTC2400	N_{ef} of ADS1251U
ADC noise from the datasheet	20.67	19.35
Raw noise samples	17.78	15.45
Averaging of 10 noise samples	19.25	16.53
Averaging of 20 noise samples	19.60	17.04
Averaging of 30 noise samples	19.77	17.40
Averaging of 40 noise samples	19.88	17.65

The analysis of the effective resolution showed that the LTC2400 had significantly lower noise and thus higher effective resolution than the ADS1251. The results from the evaluation of the impact of the averaging on the effective resolution led to a decision to use 40 samples per step during the transfer characteristic test. This approach not only allowed for nearly 20 bits effective resolution for LTC2400 but the test system also generated enough data for rough statistical analysis of the transfer characteristic. Hence, the test system collected 1800 raw AD samples during every test. A data analysis script was used to obtain the value of the effective resolution during the entire experiment. It also allowed analysis of a potential dependence of the effective resolution on the input voltage of the ADCs. The chart in Fig. 9.7 shows the effective resolution of the LTC2400 plotted for every section of transfer characteristic. Average values of ten measurements were used. A minor dependence can be seen. However, as the error bars suggest, it was rather a product of the limited number of samples used for the calculation of each section (200 samples were used to calculate effective resolution of each section) than a real effect. There was no dependency of the effective resolution observed on the ADS1251 either.

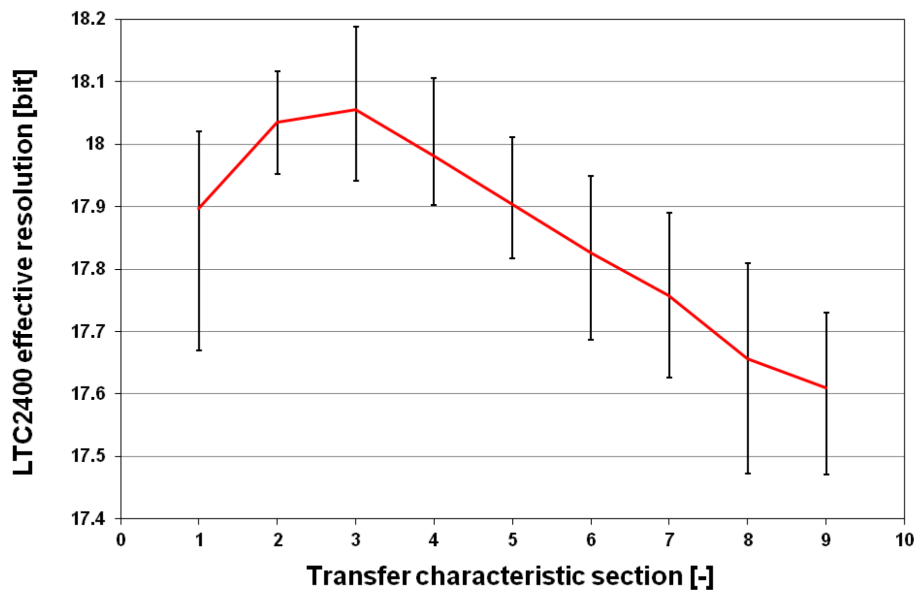

Fig. 9.7: Effective resolution of LTC2400 plotted for each section of the transfer characteristic. The error bars show scatter of the ten measurements used to calculate average values.

9.6 Results of the irradiation of the ADCs

After the completion of the initial testing of the whole ADC test system (section 9.5), there was a two-day period of pre-irradiation measurements followed by the irradiation phase of the experiment. The following sections summarise the results of each measurement.

9.6.1 TID-induced changes of the transfer characteristic of LTC2400

The key set of ADC measurements was performed to obtain the ADC transfer characteristic, as defined in section 9.4 and Tab. 9.3. The charts in Fig. 9.8 to Fig. 9.10 show the results of the selected sections of the transfer characteristic test of the LTC2400. The pre-irradiation readings were fluctuating within ±10 μV. As soon as the irradiation started, the LTC2400 started to degrade, and it failed to communicate with the test system at TID level of approximately 26 krad(Si).

While the zero-scale test (section 1 of transfer characteristic, Fig. 9.8) showed a smooth, linear, shift with the TID, the other sections (Fig. 9.9 and Fig. 9.10) exhibited a linear response to a dose of 20 krad(Si) and then followed even more rapid trend.

An additional zero-scale test step (TS) was used to evaluate the repeatability of the measurements and a potential TID-induced shift of the ADC during the transfer characteristic test. Such an "inherent" shift would cause false linearity and gain errors. As can be seen in Fig. 9.8 the TS1 and TS46 (both performed at TDAC input binary code of 100) measurements were practically identical. Therefore there were no repeatability issues, and the measured transfer characteristics were free of TID-induced "inherent" errors.

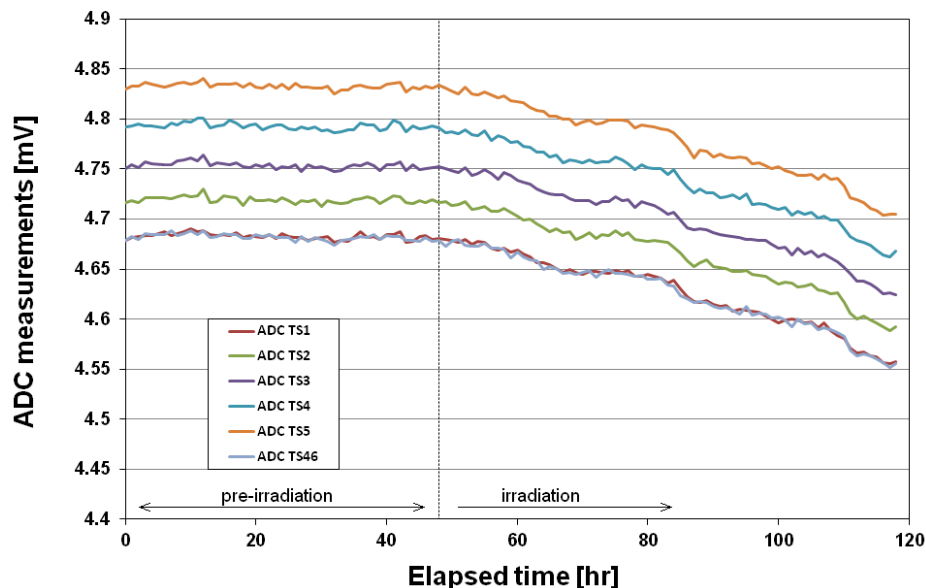

Fig. 9.8: TID-induced changes of the zero-scale part of the ADC transfer characteristics (test steps 1 to 5) of LTC2400. The test step 46 is displayed to demonstrate the repeatability of the test.

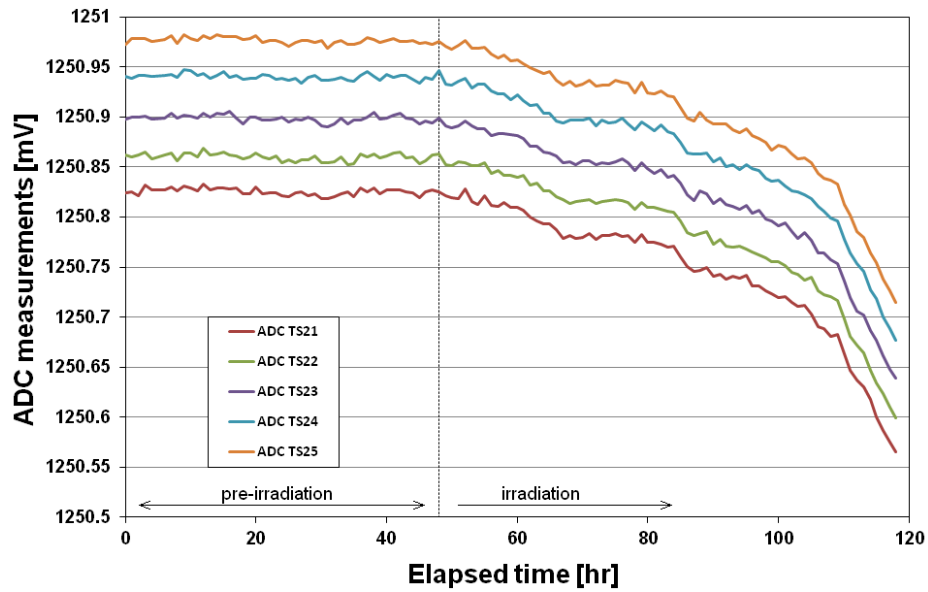

Fig. 9.9: TID-induced changes of the mid-scale part of the ADC transfer characteristics (test steps 21 to 25) of LTC2400.

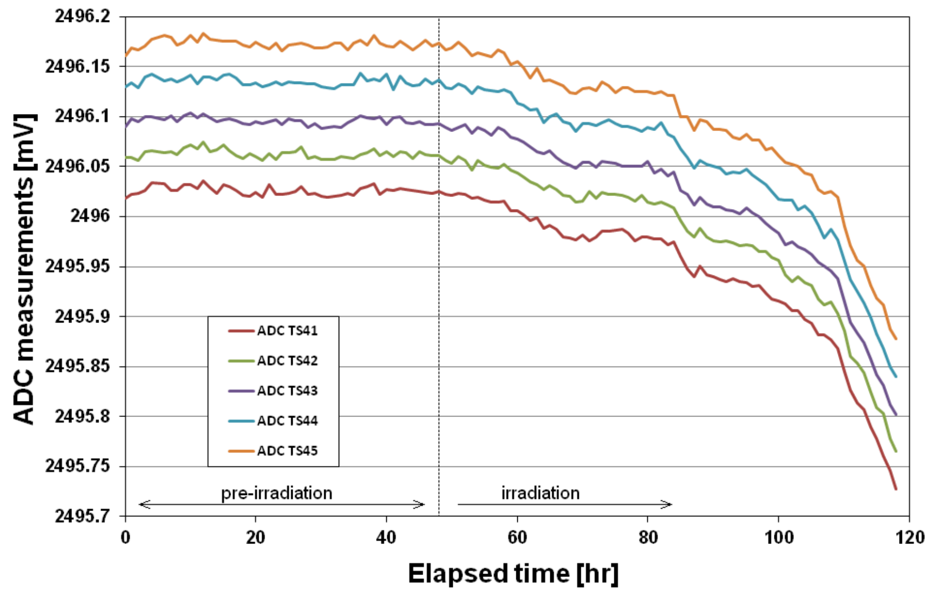

Fig. 9.10: TID-induced changes of the full-scale part of the ADC transfer characteristics (test steps 41 to 45) of LTC2400.

9.6.2 TID-induced changes of the DC errors of LTC2400

The DC errors of the ADCs could be calculated from the transfer characteristic data using the equations defined in section 4.4.2. The DC offset error ε_{os} and gain error ε_G were expressed in the ppm of the full-scale range (reference voltage) and plotted as a function of TID in Fig. 9.11.

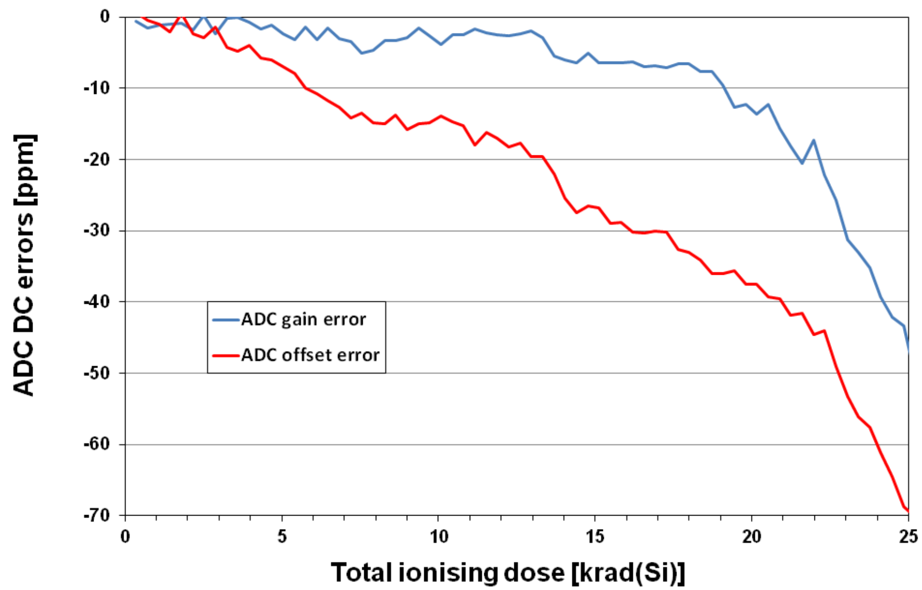

Fig. 9.11: TID-induced change of the DC offset and gain errors of LTC2400.

Another evaluated parameter was the integrated non-linearity (*INL*). Equation (4.6) was used to calculate the *INL* for every section of the transfer characteristic and a maximal value was plotted as a function of TID in Fig. 9.12.

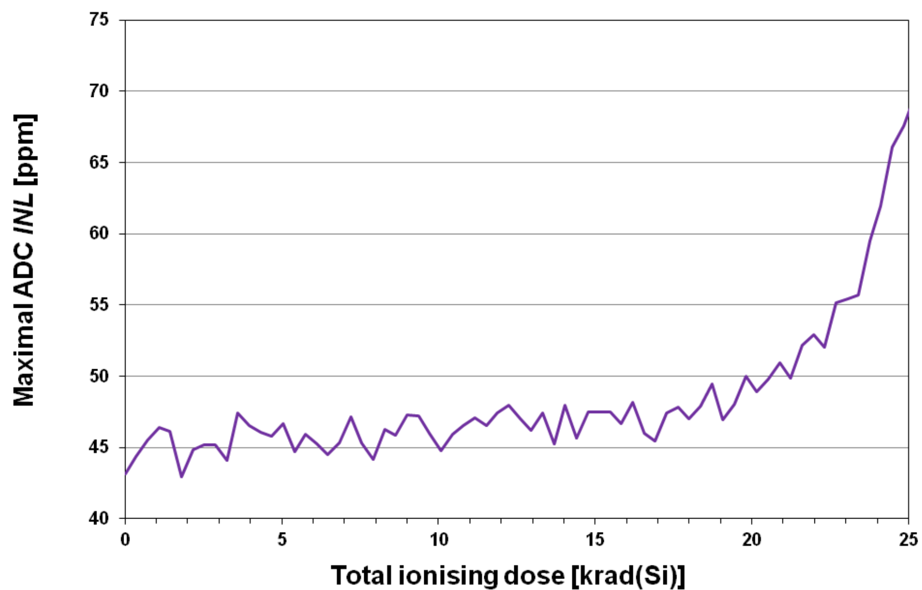

Fig. 9.12: TID-induced change of the integrated non-linearity of LTC2400.

9.6.3 Effective resolution of the LTC2400 during the irradiation

As discussed in section 9.5, the raw ADC data from transfer characteristic test could also be used for a calculation of the effective resolution of the tested ADCs. Fig. 9.13 shows the effective resolution of the LTC2400 during the TID experiment.

No significant TID-induced change was observed, and the results were in a good agreement with the initial noise measurements (see raw data results in Tab. 9.4).

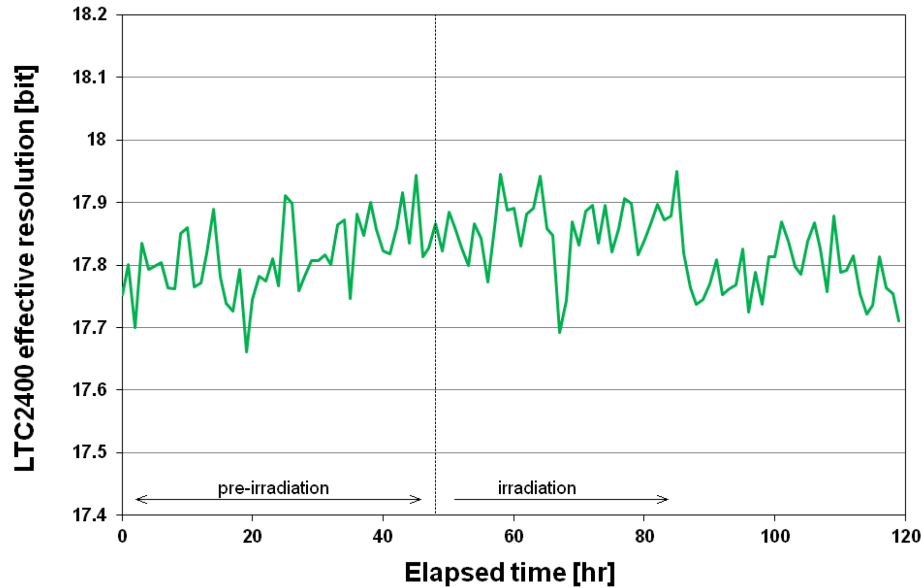

Fig. 9.13: Effective resolution of LTC2400 measured during the TID experiment.

9.6.4 TID-induced changes of the measurement error of LTC2400

To summarise the TID-induced degradation of the LTC2400, the value of the mid-scale measurement error was evaluated. The ADC readings were initially calibrated using the pre-irradiation measurements, and a deviation of the mid-scale measurement error was calculated. The chart in Fig. 9.14 shows the ADC measurement error as a function of TID and a comparison to 1 LSB error of ADCs of typical resolutions.

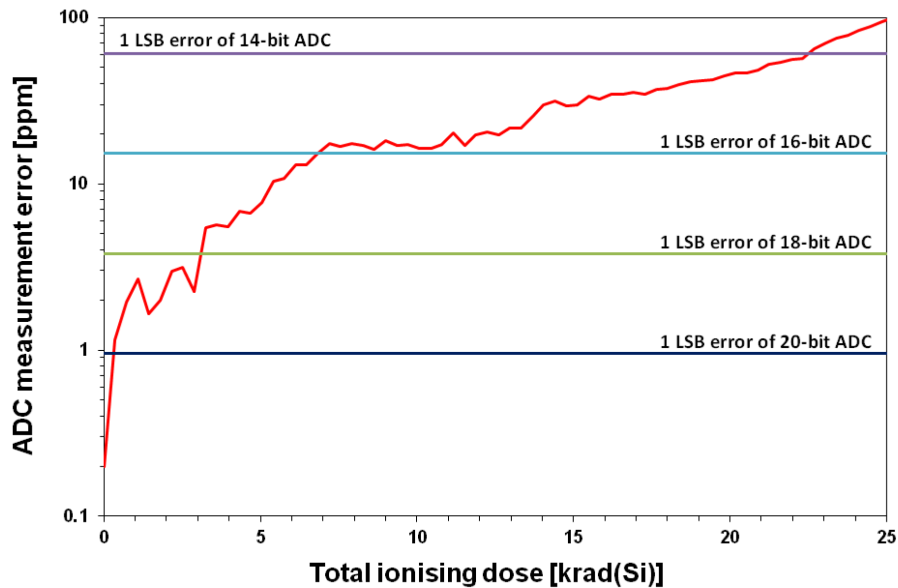

Fig. 9.14: Mid-scale measurement error of the LTC2400 recorded during the TID experiment.

9.6.5 Supply currents of the LTC2400 during the irradiation

The PTM module measured the supply currents both during the sleep and conversion modes of the ADC. The recorded values of the supply currents are plotted in Fig. 9.15.

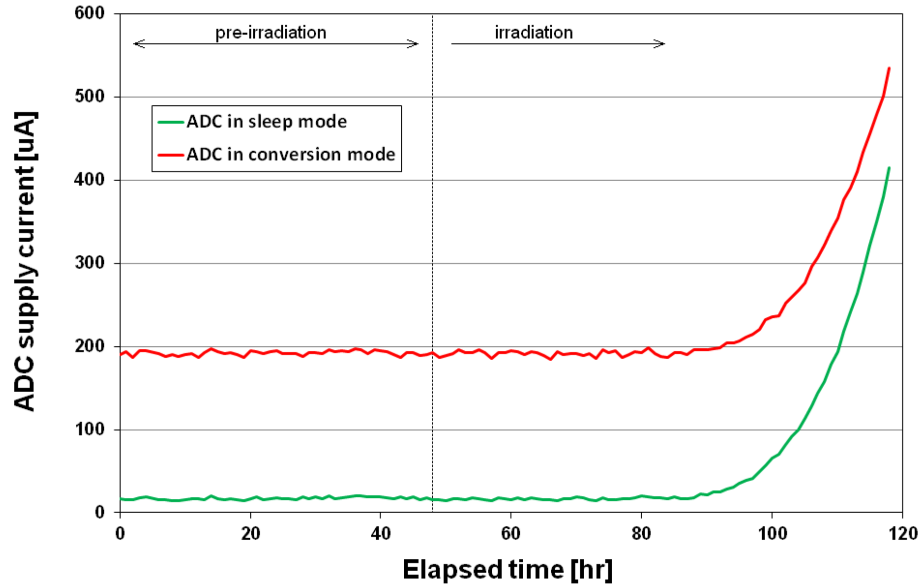

Fig. 9.15: Supply currents of the LTC2400 measured during the TID experiment.

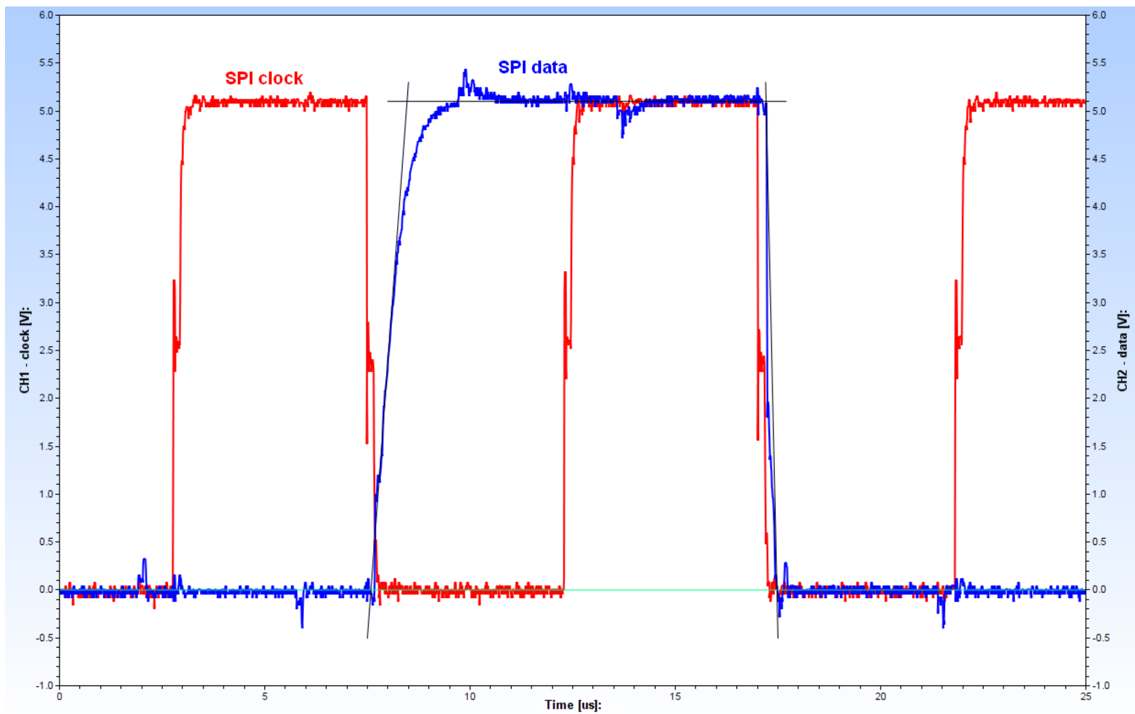

Fig. 9.16: A waveform of SPI bus of the LTC2400 captured during the TID experiment and processed/displayed by the STS software. The horizontal scale was 25 µs, and the vertical scale was 6 V.

9.6.6 Performance of the LTC2400 SPI bus during the irradiation

The test system stored and analysed the SPI waveforms to detect potential TID-induced degradation of the digital outputs of the ADC. An example of SPI waveform processed and displayed by STS software is shown in Fig. 9.16. The glitches on the edges of the clock signal were products of the imperfect termination of the signals to the DSO, the signals at the ADC had no anomalies (moreover, the DSO was only connected to ADC, via the MUX, when its measurements were being taken and not at any other time). No significant change of the LTC2400 SPI data output was observed, even during the final measurements prior to the functional failure at 26 krad(Si).

The functional failure of the device was detected when the SPI data started to be erroneous (there were false high levels on the SPI bus). However, the SPI data output was still nominal regarding logic levels and rising/falling times. Only a few hours later (at a dose of 27.3 krad(Si)) the logic level started to drop, and the SPI data were invalid at the rising edge of the clock signal as shown in Fig. 9.17. The DUT stopped generating any SPI signal at a dose of approximately 28 krad(Si).

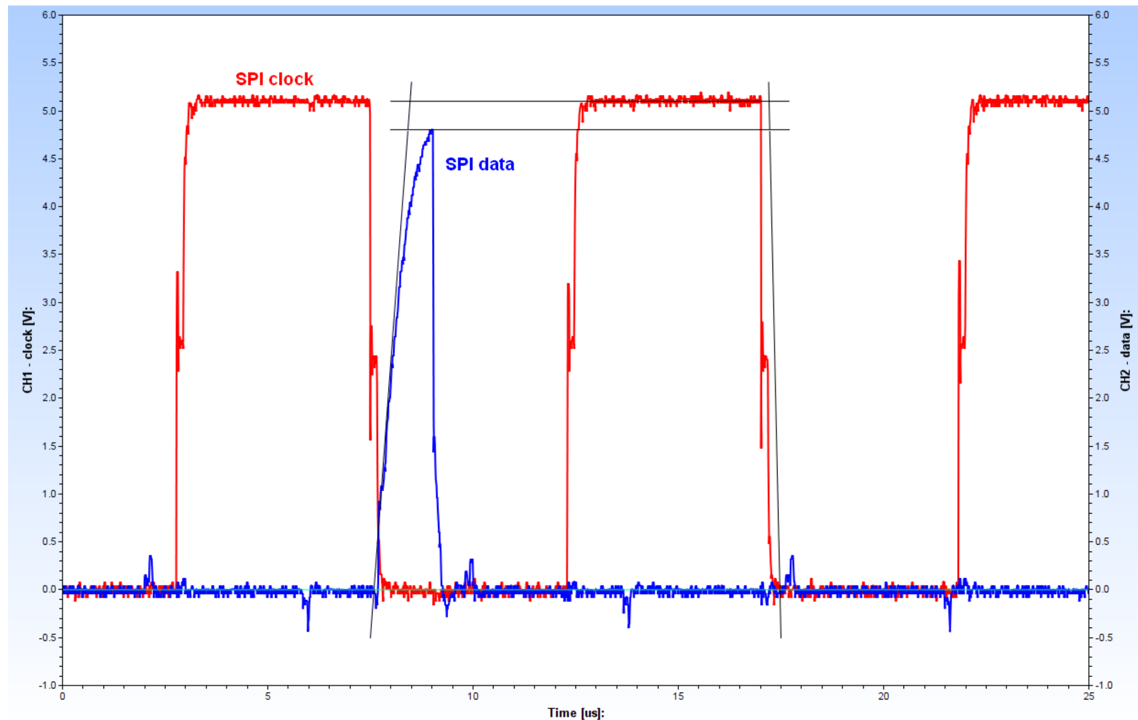

Fig. 9.17: A waveform of a functional failure of the SPI bus of the LTC2400 captured during the TID experiment at the dose of 27.3 krad(Si). The horizontal scale was 25 μs, and the vertical scale was 6 V.

9.6.7 Results of the irradiation for the ADS1251

The noise of the ADS1251 was significantly noisier than the LTC2400, and the results of the ADS1251 experiment were not as precise (see Tab. 9.4). Therefore the presented results for the ADS1251 are less detailed. The ADS1251 was immune to radiation up to the TID level of approximately 13 krad(Si), at which it started to degrade rapidly and

monotonously with the dose (Fig. 9.18). The supply current of the ADS1251 followed practically the same trend as the ADC measurements (Fig. 9.19 versus Fig. 9.18). Noticeable is the trend in the sleep mode current, which grew more rapidly than the conversion mode current. The part failed to operate at the dose of 56 krad(Si). The failure started with faulty SPI data and with the supply current going over 100 mA, which led to the interruption of the experiment. The SPI rising/falling times and voltage levels remained intact even at the failure dose.

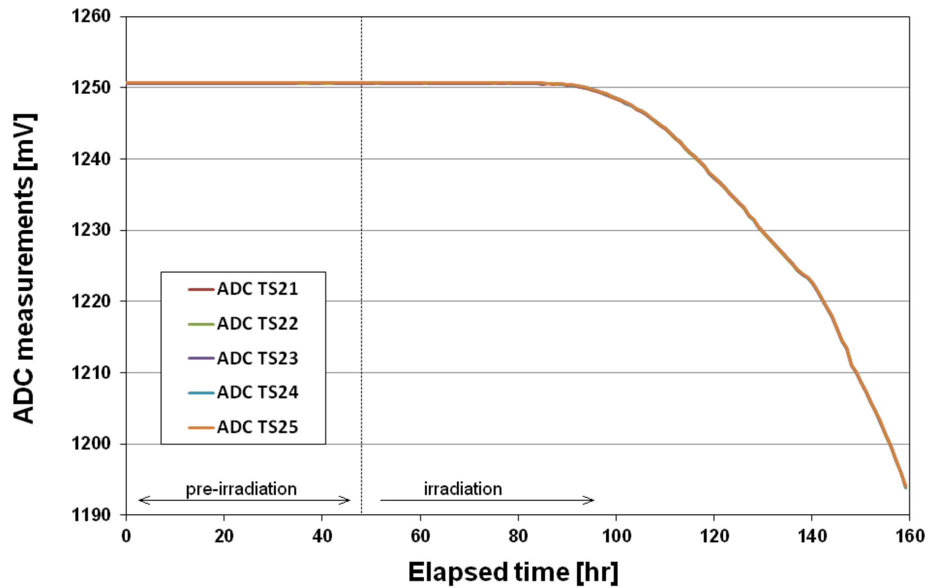

Fig. 9.18: TID-induced changes of the mid-scale part of the ADC transfer characteristics (test steps 21 to 25) of ADS1251.

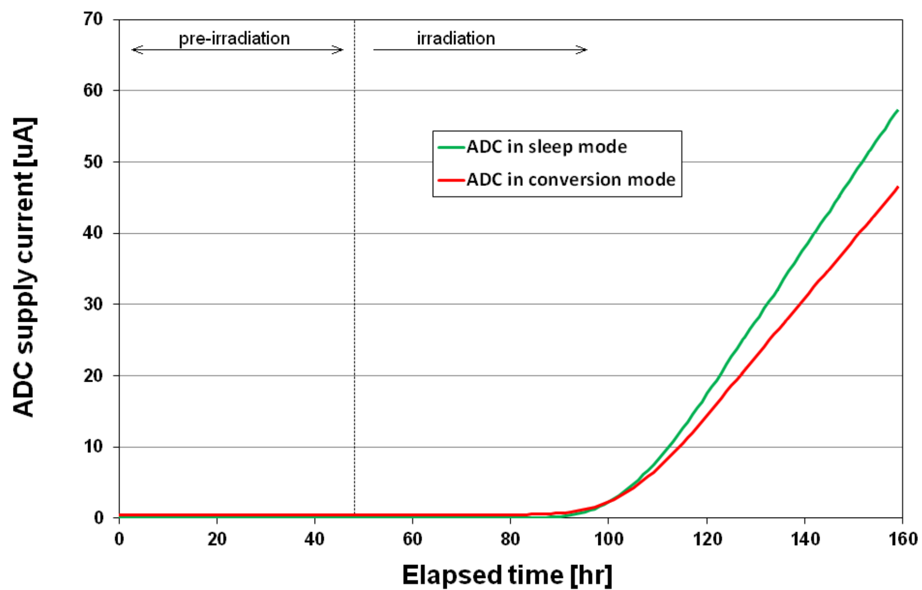

Fig. 9.19: Supply currents of the ADS1251 measured during the TID experiment.

The analysis of the noise in the transfer characteristic data sets showed that the effective resolution had stable values during the whole experiment with fluctuations within the ±0.5 bit. The mean value of the effective resolution was in agreement with the initial noise test as defined in Tab. 9.4.

The final chart of this section, Fig. 9.20, shows the mid-scale measurement error of the ADS1251 versus the 1 LSB error margins calculated for each typical ADC resolution.

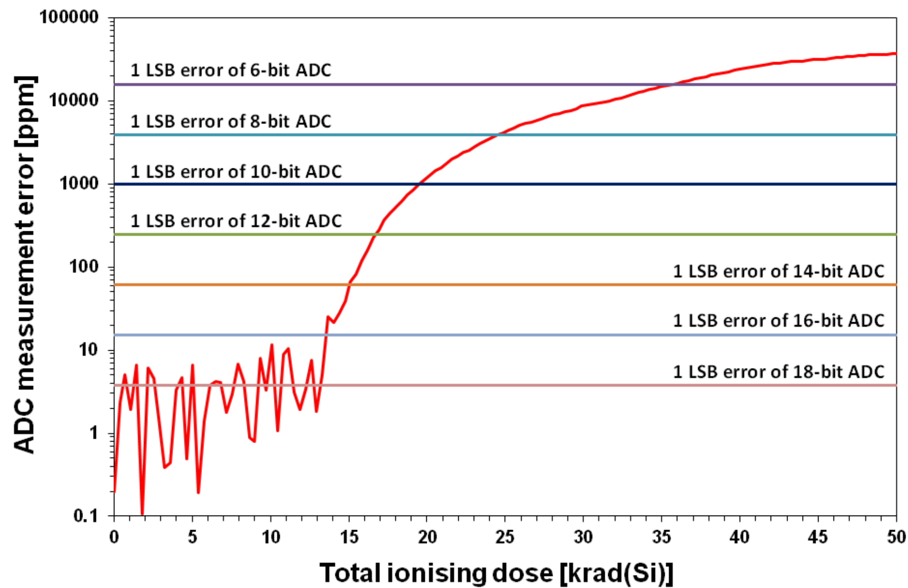

Fig. 9.20: Mid-scale measurement error of the ADS1251 recorded during the TID experiment.

9.7 Discussion of the results of the ADC TID experiment

The results of the ADC TID experiment are discussed in this section in two ways. The first view is an analysis of the test performance/capabilities of the ISTM test system, which was developed for high-resolution testing of precise A/D converters and was demonstrated in this experiment. The second perspective was an evaluation of TID-induced degradation of two interesting candidates for high-precision COTS space DAQ systems.

The test system performed reliably during the whole experiment; no functional failure was detected during its operations (the STS software could detect various problems both internal within the ADC tester and external related to the communication with the ADCs under test). The STS was thus validated for the future in-orbit testing.

Noise is the key limiting factor for high-resolution measurements/testing. Therefore the noise performance of the whole signal chain of the ADC tester and the ADCs under the test was measured in-situ in the MIF facility at two stages. The first test was a continuous data acquisition at a constant input voltage of thermally stabilised hardware. The second opportunity for noise analysis came during the TID experiment itself, as the test system allowed measurement of data that could also be used for

simplified noise evaluation (at least with precision good enough to observe if there was TID-induced change of the effective resolution of the ADCs). These tests concluded that the effective resolution of the designed test system could reach 20 bits if the raw ADC data is processed using oversampling and averaging. As can be seen in the Tab. 9.4 the achieved effective resolution of 19.8 bits was very close to the typical effective resolution of the LTC2400 itself as defined in the datasheet. More proof of this optimistic result can be seen in the pre-irradiation reading shown in Fig. 9.8. It is clear that there was a "plenty of space" between the 16-bit voltage steps generated by the TDAC. This combined with the excellent matching of the TS1 and TS46 measurements also showed that the effective resolution of more than 18-bit could be achieved with ISTM testing.

The initial noise performance of the ADS1251 was expected to be poorer than of the LTC2400. However, the measured results were even worse than expected. As the noise of the inputs of the ADCs could be assumed to be identical, the problem could have been caused by imperfections of the VREF source of the ADS1251. The manufacturer recommends buffering of the VREF, and the reference voltage was buffered independently for each ADC. However, the buffers (operational amplifiers) were placed outside the irradiation facility due to a potential TID-induced shift of their voltage outputs. Therefore there could have been an additional noise created across the analogue lines in the cable from the ADC tester to the DUT container. Moreover, the V_{REF} signal could have been interfering with the V_{IN} of the ADS1251 as they were present in the same cable and the shielding was common to them. This problem can be easily avoided in future experiments by using separated cables.

The stability of the effective resolution of both tested devices during the irradiation suggested that the modulator part of the devices did not cause the observed degradation in the measurement error. It could be assumed that the degradation in the modulator part would be seen as a change in the noise performance of the devices. Furthermore, the test system also measured the duration of each conversion step, and no changes were observed during the irradiation phase. There were no other errors detected in the digital parts of the devices (until the communication problems started near the dose level of a functional failure of the device). Hence, it could be assumed that digital parts of the devices were not responsible for the observed degradation in the precision of the A/D conversions.

There was no observation of a dependence of the effective resolution on the ADC input voltage. Therefore the future test systems could be measuring the effective resolution only at one point of the transfer characteristics, for example at the mid-scale level. That would allow for more precise measurements of the effective resolution as there could be more ADC samples acquired (ideally at least ten thousand samples).

The TID-induced degradation of the measurement errors of the ADCs were significantly different between the devices; while the LTC2400 started to degrade immediately after the start of the irradiation, the ADS1251 appeared to be immune to the radiation up to a dose of 13 krad(Si) after which it started to degrade practically constantly with the dose.

The degradation of the transfer characteristics of the LTC2400 was not consistent across the input voltage range; while the degradation at the zero-scale level was practically linear with the dose, the response to the radiation was rather more complex

at higher input voltage steps (Fig. 9.8 versus Fig. 9.9 and Fig. 9.10). In contrast, the TID-induced changes of the ADS1251 were homogenous across the whole range of the input voltage of the device.

The results of the initial measurement errors of the tested ADCs were in a good agreement with the typical values defined by the manufacturers. An exception was the significantly higher values of the integral non-linearity of the LTC2400 acquired during the pre-irradiation phase. As shown in Fig. 9.12, the *INL* was approximately 45 ppm at the start of the irradiation. That was more than four times higher than the maximal datasheet value. This could be explained by a combination of the *INL* of the tested ADC with the *INL* of the TDAC. According to its datasheet, the linearity error of the DAC could reach 4 LSB (16-bit). Such a linearity error would be equal to 61 ppm *INL*. This error was inherent to the test system and was stable during the TID experiment. Therefore the initial value of the *INL* could be subtracted, and it has minimal impact on the observed TID-induced change of the *INL*.

Another interesting result was the measurements of the devices' supply currents. A decision was made to develop the PTM module (see section 9.3) as there was a need to measure ultra-low currents in the order of μA during the sleep mode of the ADCs, but also to perform precisely synchronised measurements of the supply current during the A/D conversions. The performance of the PTM measurements was very good; the noise was lower than 1 μA within a range of 200 mA, and the accuracy was better than 1 %, which was validated by repeated measurements with DMM4050.

The measured values of the supply currents of the LTC2400 were stable until the TID-level reached approximately 16 krad(Si) and started to rise with increased speed. While the conversion mode supply current doubled, the sleep mode current increased by two orders of magnitude. There was a clear correlation between the final rise of the supply currents and the trends in the LTC2400 ADC measurement errors (Fig. 9.15 versus Fig. 9.11 and Fig. 9.12).

As for all other measurements, the supply currents of the ADS1251 were stable until the TID level of 13 krad(Si) and then started to grow rapidly (Fig. 9.19). The increase of the current was significant: the conversion mode current rose from 0.4 mA to 45 mA. Such a major change in supply current had a significant impact on dissipated heat by the device (the power dissipation changed from 2 to 250 mW). Therefore the observed measurement errors could have also been a product of the temperature dependency of the ADC. The ground lines of the test system were terminated close to the ADCs, but there could have been a voltage drop in power supply cabling to the ADS1251, and thus another potential source of the measurement errors was the drop in power supply line poorly compensated by the ADC. This would suggest a TID-induced degradation of the *PSRR* of the ADC.

To conclude, the ADC TID experiment successfully demonstrated promising capabilities of the designed ISTM ADC test system and reliably measured TID-induced degradation of two COTS 24-bit A/D converters. However, there was not enough data to make final conclusions about the performance of the tested devices as there was only one piece of each type of ADC tested. Despite this limitation, the LTC2400 could be an interesting candidate device for in-orbit testing.

The results of the ADC TID experiment were presented in March 2017 at the RADFAC conference in Sevilla, Spain.

10 IN-ORBIT EXPERIMENTS

The final chapter of this thesis is focused on the in-orbit experiments developed during the PhD program. These experiments were called RadEx (short for Radiation Experiments). Two generations of the in-orbit experiments have been developed: RadEx1 and RadEx2. While the first experiment RadEx1 is described only briefly (due to its cancellation), the second experiment RadEx2 is discussed in detail as it fulfilled objectives of that phase of the PhD work.

10.1 Overview of the RadEx1 experiment

RadEx1 was one of the first attempts to design a miniature-scale, in-orbit TID experiment following the limitations of a CubeSat platform (half of a standard CubeSat PC104 board was the maximum expected area of the RadEx1 electronics). The experiment was designed to be integrated as an auxiliary payload within the PilsenCUBE satellite [349], but it could be used in any future CubeSat mission due to its practically autonomous hardware solution (Fig. 10.1). The main objectives were as follows [350]:

1) to measure the total dose the satellite electronics receives during the mission
2) to perform continuous monitoring of the performance of devices under test (DUTs) in order to evaluate their TID-induced degradation
3) to provide functional and parametric self-test of the data acquisition block to ensure objective test results and observe potential TID degradation of its performance

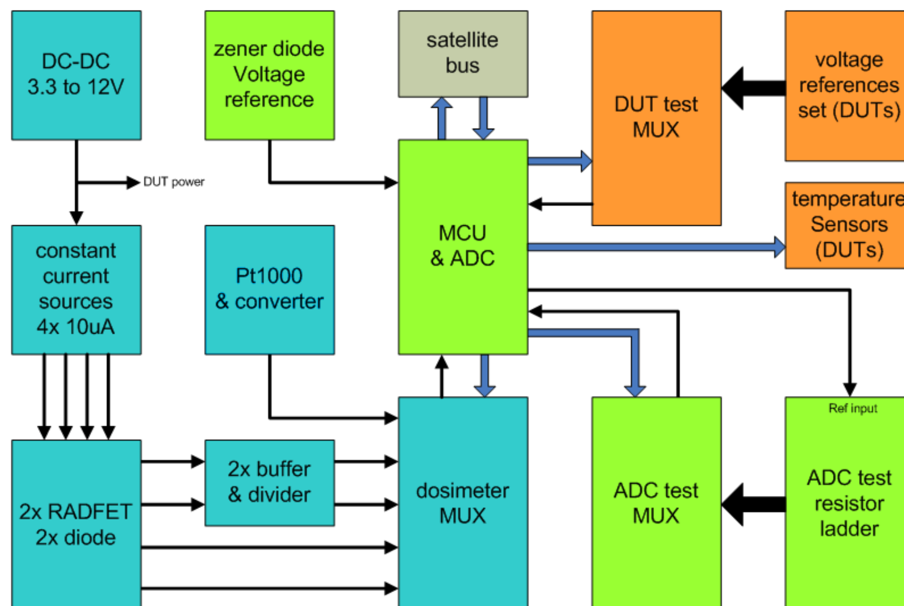

Fig. 10.1: Block diagram of the RadEx1 experiment. It consisted of the following subsystems: the dosimetry subsystem (blue), the DUTs (orange) and the DAQ block (green) comprising of MCU with an integrated ADC plus an external high-resolution ADC.

In early 2013, the hardware design of the RadEx1 experiment was completed (a fully functional prototype was built and tested) and the flight software was about 80 % integrated with the CubeSat software package. The TID testing of various components was also in progress, for example, the results of the power supply block (DC-DC converters and current sources for the dosimetry system) was successfully finished, and a paper was presented at the NSREC 2013 conference in San Francisco, USA [351].

The plan was to fly the experiment aboard the PilsenCUBE satellite during the period 2014/2015. However, the project was cancelled in the autumn of 2013 due to a budget cut at the University of West Bohemia (Czech Republic), which was responsible for the development and operation of the PilsenCUBE mission. Negotiations with other CubeSat/nanosat teams give only a small chance of launching the RadEx1 experiment within a reasonable period of time and with an acceptable risk of the success of the CubeSat project itself. Therefore the further development of the RadEx1 experiment was put on hold until a realistic launch opportunity arose.

10.2 Background and objectives of the RadEx2 experiment

The development of the in-orbit experiment was restarted in late 2016 when two new launch opportunities appeared. A decision was made to completely redesign the experiment because of the following factors:

1) The primary launch opportunity (CubeSat FEES) had even more challenging requirements/constraints for PCB area and power budget than the original experiment.
2) In the meantime, a series of advanced TID-experiments was performed (chapters 7 to 9) and the results and lessons-learned could be implemented in the new design.
3) New ultra-high precision DAQ devices appeared on the marked together with low voltage RADFETs. This allowed simplifying the hardware design of the experiment and lowering its power budget.

As the final hardware design was practically brand new, the design was recognised as a next-generation experiment named RadEx2. Despite the new design, the research goals were the same with some extensions:

1) The design and calibration of a simplified radiation monitor
2) An in-orbit performance test of a multi-channel temperature monitor
3) An in-orbit test of a dual, ultra-high resolution, DAQ system
4) An in-orbit TID test of voltage references and comparison of the results with the data from ground TID tests
5) A real-time “Live” model of TID-induced degradation of the measurement uncertainty of selected channels of the DAQ system (the LMMU model described in section 5.5)
6) A completely autonomous design that could be used in various CubeSat and nanosat platforms
7) An integration package allowing a smooth integration of this experiment with typical CubeSat platforms
8) Preliminary estimation of the mission TID levels for the RadEx2 mission
9) Ground segment support (software)

10.3 Flight opportunities for the RadEx2

10.3.1 FEES – the 1/3U CubeSat mission

The primary launch opportunity for the RadEx2 experiment is the project FEES (Flexible Experimental Embedded Satellite) developed and operated by a private enterprise GP Advanced Projects Srl, Italy.

The key mission objectives of FEES are [352]: in-orbit qualification of an attitude determination and control subsystem (ADCS), together with the relative GNC architecture; in-orbit qualification of commercial GPS receivers; exploitation of IRIDIUM signal to receive data and support onboard traditional radio transmission architectures. Moreover, FEES aims to test transmission protocols by using software defined radio (SDR) digital technology and perform Earth imaging with a multispectral camera. The FEES is expected to be launched on a Soyuz rocket in Q4 2019 to Q1 2020 as a secondary payload.

The RadEx2 experiment will be placed on the bottom side of the PCB (the satellite is designed as "single-board" hardware as shown in Fig. 10.2). The satellite bus will provide DC power together with a digital data/control bus; therefore there is no need for the RadEx2 to have its own dedicated MCU. The hardware design of the RadEx2 and the integration with FEES hardware design package was completed in 2017, the final hardware/software integration effort (using an EM of the FEES PCB) is planned for late Q3 2019.

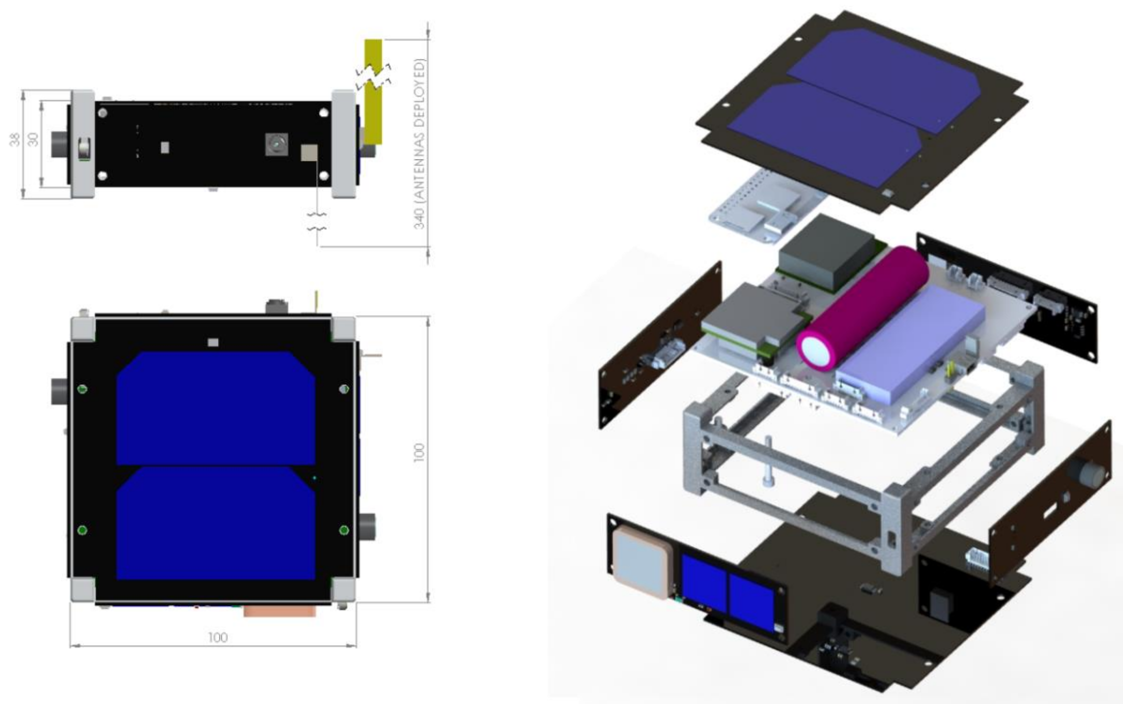

Fig. 10.2: Dimensional drawings (left) and an exploded view drawing (right) of the FEES satellite. The RadEx2 experiment is located on the bottom side of the central PCB. Pictures credit: GP Advanced Projects, Italy.

10.3.2 Mission dose estimate for the FEES satellite

A preliminary mission dose estimate was performed using both SPENVIS [71] and OMERE tools [353]. This analysis was based on the definition of the planned orbit for the FEES mission as summarised in Tab. 10.1.

Tab. 10.1: Estimated parameters of the FEES mission used for simulations.

Parameter	Value
Type of orbit	Sun-synchronous (SSO)
Apogee [km]	653
Perigee [km]	539
Semimajor axis [km]	6974
Inclination [°]	97.62
Eccentricity [-]	0.008
Local Time of Descending Node (estimated)	10.30
Launch site	Russia, Kazakhstan
Solar activity	Low, end of cycle 24

The results of the simulations are shown in Fig. 10.3. The simulation was based on a simplified mechanical model of the satellite. The shielding material was assumed to be aluminium (AL6061-T6 Structural parts 2715) of thickness ranging between 0.75 and 1.5 mm (vertical bars in the chart). The resulting TID level for one year mission was estimated to be 5 to 10 krad(Si), which was in a good agreement with estimates calculated by CNES as shown in Tab. 3.1.

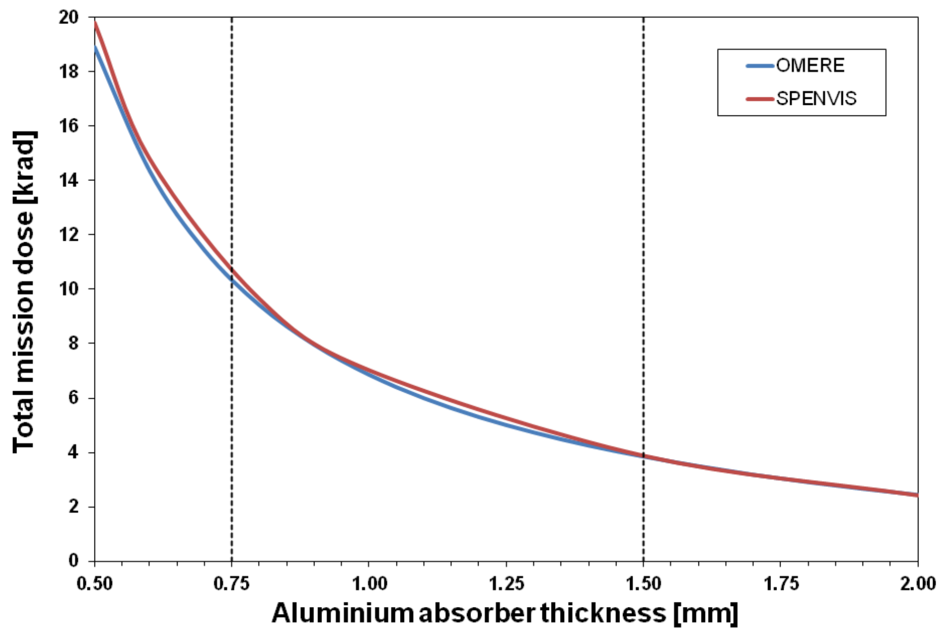

Fig. 10.3: Results of the FEES mission dose estimation from OMERE and SPENVIS tools. The vertical bars define the range of expected thickness of aluminium shielding.

10.3.3 Project PilsenCUBE-II

PilsenCUBE-II is a second generation of the PilsenCUBE picosatellite platform developed by the Department of Applied Electronics and Telecommunications (part of the University of West Bohemia, Czech Republic). The 1U standard CubeSat frame will be used to host various student research payloads [349]. The satellite will also perform numerous technological experiments including deployable solar panels (Fig. 10.4), advanced power system using super-capacitors, a redundant on-board computer based on automotive solutions and an experimental high-speed telemetry system using SDR at 2.4 GHz. The primary experiment will be a new version of the Medipix sensor [354].

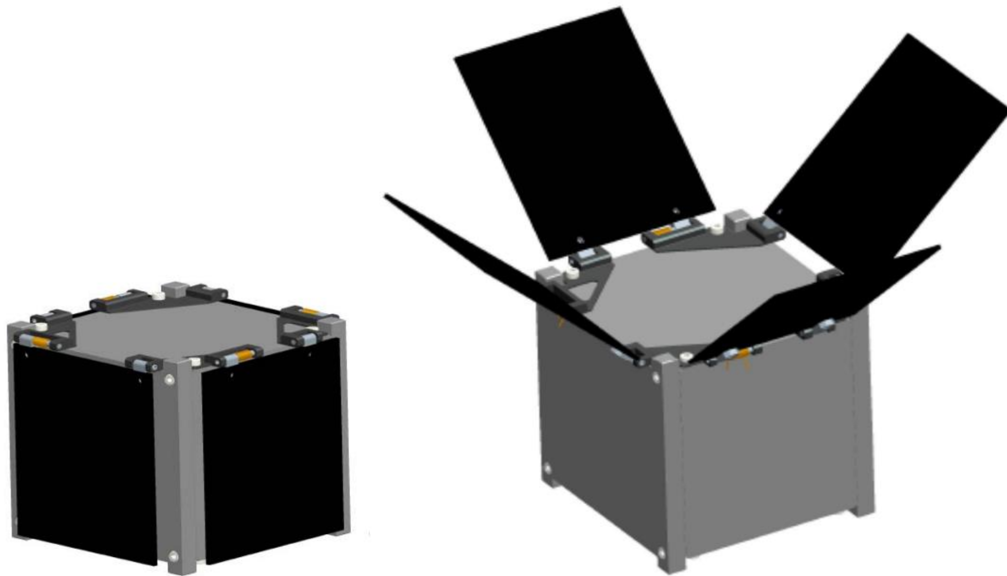

Fig. 10.4: PilsenCUBE-II will be a 1U sized CubeSat (left) with deployable solar cells (right). Drawings adapted from [349].

The integration of the RadEx2 hardware design with the design of the PilsenCUBE-II hardware was completed in 2017 (on the schematic level). The RadEx2 experiment will be part of a measurement board MES responsible for monitoring various properties of the spacecraft “house-keeping” systems such as power system (batteries, capacitors, solar cells), temperature monitoring, Sun sensors and others. The MES board also acts as an interface for the student projects [354].

The budget for the launch of the PilsenCUBE II satellite was secured in collaboration with the Information Technologies Management of the Pilsen City (SITMP). However, a detailed schedule and launch provider has not been selected (at the time of submitting this thesis). Therefore the mission orbit has not been defined, and the mission dose simulation could not be performed at this stage. The launch is not expected before the year 2020.

In the meantime, the University of West Bohemia designed and deployed a ground station [355] that was successfully used to send commands to and receive telemetry from various satellites. This including the first Czech CubeSat, VZLUSAT-1, that was launched in 2017 in order to perform various technological experiments [356].

10.4 Design of the RadEx2 experiment

10.4.1 RadEx2 hardware design

The second generation of the RadEx experiment is based on two principal changes to the original design:

1) The new design is based on a "single-chip" architecture, in which most the testing functionality is provided by the ADC integrated circuit
2) The dosimetry system no longer requires DC-DC conversion as it requires only 5 V supply voltage

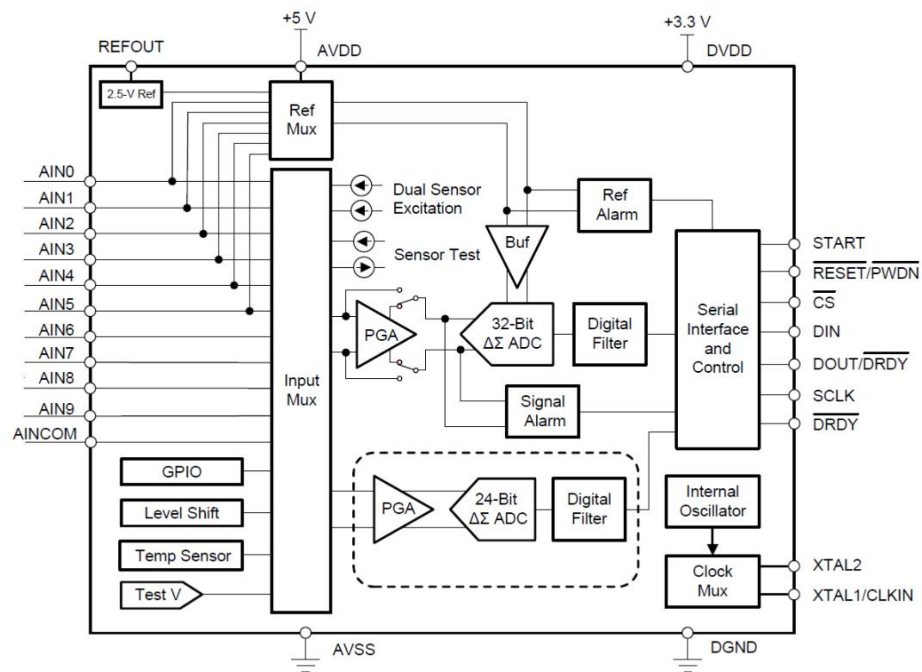

Fig. 10.5: Block diagram of the ADS1263 showing its advanced architecture. Picture adapted from [357].

The block diagram of the core chip of the RadEx2 is shown in Fig. 10.5. The ADS1263 was an excellent solution as it is a state-of-the-art ultra-high resolution ADC with advanced features including [357]:

- 32-bit ADC1 with an auxiliary 24-bit ADC2 (both ΔΣ modulation)
- Programmable current sources for sensor excitation
- Precision internal VREF circuit (VREFI)
- Integrated test D/A converter (TDAC)
- Internal Fault Monitors

With all this functionality in a single IC, the whole experiment could be designed as a core IC surrounded by directly connected sensors, reference sources and devices under the test. Therefore the RadEx2 block diagram in Fig. 10.6, in fact, shows particular devices, not subsystems - each functional bock consisted of a single device (passive or active sensor, a reference resistor, or VREF integrated circuit).

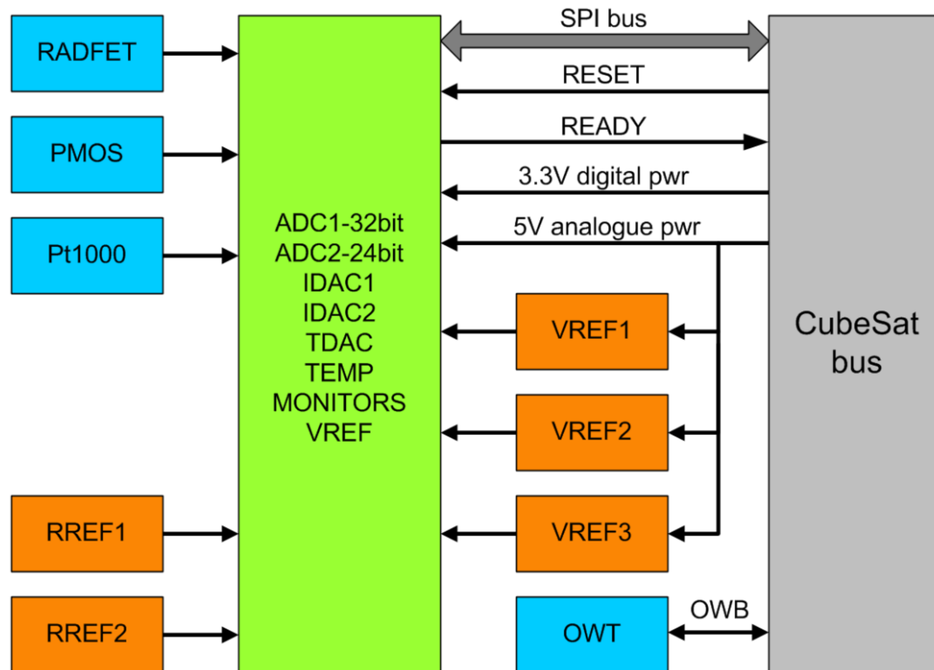

Fig. 10.6: Block diagram of the RadEx2 experiment. It consists of the core ADC (green), set of sensors (blue blocks) and set of reference devices and DUTs (orange blocks). The interface to the satellite bus is shown as a grey block.

10.4.2 RadEx2 integration package

The RadEx2 experiment can be easily integrated with practically any spacecraft design due to its simple electrical interface. RadEx2 integration package (R2IP) was created to simplify the integration process and provide the satellite designers with all necessary details. The R2IP for the space segment (satellite) consists of:

- Hardware package:
    - Hardware interface control document (ICD) defining all interfaces to and from RadEx2 hardware including power lines
    - Schematic diagrams
    - Recommendations for the PCB layout
    - Bill of material (BOM)
    - Set of active components (with predictable response to TID)
    - Set of special components (reference resistors and others)
    - Power budget spreadsheet
- Software package:
    - Software ICD (telemetry commands, scientific data package, configuration data)
    - Software code package (ANSI C) to be used in the satellite MCU (or FPGA) that can be compiled with various IDEs

The design of the ground segment (ground stations) will be entirely a responsibility of the teams operating the satellites. The team at the Brno University of Technology (BUT) will be provided with the raw scientific data packages. BUT will process the data and publish the results. The data processing will be performed using STS scripts.

10.4.3 RadEx2 data acquisition channels

The RadEx2 ADC allows connection of up to ten analogue inputs (Fig. 10.5). They are all used for connection of the sensors and VREF (DUT) devices as defined in Tab. 10.2. In addition to that, there is a digital one-wire thermometer DS18B20 (OWT) connected directly to the satellite MCU/FPGA via a one-wire bus (OWB).

Tab. 10.2: Allocation of the RadEx2 ADC inputs.

ADC input	Device PN	Function
AIN0 (REFP1)	ADR444	VREF1 (4.096 V)
AIN1	Y4027100K000B9W	RREF1 (100 kΩ)
AIN2 (REFP2)	LT1460	VREF2 (2.500 V)
AIN3	Y40231K00000B9W	RREF2 (1k kΩ)
AIN4 (REFP3)	ADR03	VREF3 (2.500 V)
AIN5	00647795	PRT (Pt1000)
AIN6	ADR440	VREF4 (2.048 V)
AIN7	ADR03	VREF3 temp. sensor
AIN8	ZVP1320	COTS PMOS
AIN9	TY1003	RADFET

Each ADC input can be measured under various conditions. Every combination of ADC input and measurement condition is recognised as a RadEx2 DAQ channel (RDCH) as defined in the following tables. The architecture of the design of the RDCHs was designed in order to provide multiple resources for each measured property. Therefore there is a redundancy in most of the measurements. The redundancy improves the reliability of the design. Further, more importantly, it allows for cross-comparison of the results, which can identify the TID-induced changes in any part of the experiment. The design was based on the results from the previous TID experiments and assumptions that some devices are inherently radiation tolerant.

Tab. 10.3: RadEx2 DAQ channels for the RADFET part of the SEM subsystem.

RDCHs	Device	ADC VREF source	Measurement Conditions
4	RADFET	AVDD	Sensor excited by SBIAS at 0.5, 2, 10, 50 μA
2	RADFET	AVDD	Sensor excited by IDAC1 at 50, 100 μA
2	RADFET	AVDD	Sensor excited by IDAC2 at 50, 100 μA
2	RADFET	VREFI	Sensor excited by SBIAS at 0.5, 2, 10 μA

Tab. 10.4: RadEx2 DAQ channels for the PMOS part of the SEM subsystem.

RDCHs	Device	ADC VREF source	Measurement Conditions
4	PMOS	AVDD	Sensor excited by SBIAS at 0.5, 2, 10, 50 μA
10	PMOS	AVDD	Sensor excited by IDAC1 at 50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000 μA
10	PMOS	AVDD	Sensor excited by IDAC2 at 50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000 μA
4	PMOS	VREFI	Sensor excited by SBIAS at 0.5, 2, 10, 50 μA
1	PMOS	VREFI	Sensor excited by IDAC1 at 50 μA
1	PMOS	VREFI	Sensor excited by IDAC2 at 50 μA

Tab. 10.5: RadEx2 DAQ channels for the PRT and reference resistors of the SEM subsystem.

RDCHs	Device	ADC VREF source	Measurement Conditions
1	PRT	AVDD	Sensor excited by SBIAS at 50 μA
1	PRT	AVDD	Sensor excited by IDAC1 at 50 μA
1	PRT	AVDD	Sensor excited by IDAC2 at 50 μA
1	PRT	VREFI	Sensor excited by SBIAS at 50 μA
1	PRT	VREFI	Sensor excited by IDAC1 at 50 μA
1	PRT	VREFI	Sensor excited by IDAC2 at 50 μA
4	RREF1	AVDD	Sensor excited by SBIAS at 0.0, 0.5, 2, 10 μA
4	RREF1	VREFI	Sensor excited by SBIAS at 0.0, 0.5, 2, 10 μA
5	RREF2	AVDD	Sensor excited by SBIAS at 0.0, 0.5, 2, 10, 50 μA
10	RREF2	AVDD	Sensor excited by IDAC1 at 50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000 μA
10	RREF2	AVDD	Sensor excited by IDAC2 at 50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000 μA
5	RREF2	VREFI	Sensor excited by SBIAS at 0.0, 0.5, 2, 10, 50 μA
8	RREF2	VREFI	Sensor excited by IDAC1 at 50, 100, 250, 500, 750, 1000, 1500, 2000 μA
8	RREF2	VREFI	Sensor excited by IDAC2 at 50, 100, 250, 500, 750, 1000, 1500, 2000 μA

Tab. 10.6: RadEx2 DAQ channels for the temperature sensors of the SEM subsystem.

RDCHs	Device	ADC VREF source	Measurement Conditions
1	ADC	VREFI	Internal temperature sensor
1	VREF3 sensor	AVDD	Temperature sensor of VREF3
1	VREF3 sensor	VREFI	Temperature sensor of VREF3
1	VREF3 sensor	VREF2	Temperature sensor of VREF3
1	OWT	N/A	One-wire thermometer

Tab. 10.3 to Tab. 10.6 define RadEx2 DAQ channels for the particular devices of the Space Environment Monitor (SEM) subsystem, which is responsible for the measurement of mission TID level and ambient temperature (as discussed in section 5.5). The dose measurements are based on a combination of RADFET and PMOS device (demonstrated in chapter 7). The temperature is measured using four independent sensing methods:

1. Radiation tolerant PRT sensor measured by ADC (see section 6.5.2)
2. ADC internal temperature sensor (two diodes design [357])
3. DS18B20 sensor connected directly to the satellite bus
4. Temperature sensor output from the ADR03 (see section 8.2.5)

The temperature sensors are placed as close to each other as possible. Therefore their measurement results can be cross-compared. The temperature measurements will be calibrated prior to the launch, by placing the FM in a calibrated temperature chamber (see section 10.5 for the definition of the RadEx2 test plan).

As can be seen in the tables, the SEM sensors are mainly current biased (current excitation). The constant current can be generated by three blocks of the ADC: SBIAS (sensor bias), and two IDAC blocks. These programmable current sources allow measurement of simplified *I-V* characteristics of the RADFET and PMOS devices.

A self-calibration feature of the current sources was added to the design; there are two extremely precise resistors used as resistor reference devices (RREF1 and RREF2). These advanced thin-film resistors were provided by Vishay VPG, and they are based on the Z1 foil technology. Z1 seemed to be the best choice as it provides TC_R of ±0.2 ppm/°C typical (–55 °C to +125 °C), which was found to be the lowest value of TC_R available for SMD devices [358]. The measurements of RREF resistors are expected to be the most stable readings within the whole RadEx2 data package.

Tab. 10.7: RadEx2 DAQ channels for the TDAC testing of the ADC.

RDCHs	Device	ADC VREF source	Measurement Conditions
9	ADC	AVDD	TDAC test with PGA on at 0.5, 1.5, 2.0, 2.25, 2.5, 2.75, 3.0, 3.5, 4.5 V
9	ADC	AVDD	TDAC test with PGA off at 0.5, 1.5, 2.0, 2.25, 2.5, 2.75, 3.0, 3.5, 4.5 V

The ADC chip has an integrated test D/A converter (TDAC). This circuit allows for a simplified transfer characteristic test of both of the internal ADCs (block “TEST V” in Fig. 10.5). As defined in Tab. 10.7, the TDAC test is performed twice to provide measurements with and without the internal PGA circuit (PGA can be bypassed only for the 32-bit ADC).

Tab. 10.8: RadEx2 DAQ channels for the VREF DUTs.

RDCHs	Device	ADC VREF source	Measurement Conditions
1	VREF1	AVDD	VREF1 measurement PGA on
1	VREF2	AVDD	VREF2 measurement PGA on
1	VREF3	AVDD	VREF3 measurement PGA on
1	VREF4	AVDD	VREF4 measurement PGA on
1	VREF2	VREF1	VREF2 measurement PGA on
1	VREF3	VREF1	VREF3 measurement PGA on
1	VREF4	VREF1	VREF4 measurement PGA on
1	VREF2	VREF1	VREF2 measurement PGA off
1	VREF3	VREF1	VREF3 measurement PGA off
1	VREF4	VREF1	VREF4 measurement PGA off
1	VREF4	VREFI	VREF4 measurement PGA on
1	VREF4	VREF2	VREF4 measurement PGA on
1	VREF4	VREF3	VREF4 measurement PGA on
1	VREF4	VREFI	VREF4 measurement PGA off
1	VREF4	VREF2	VREF4 measurement PGA off
1	VREF4	VREF3	VREF4 measurement PGA off

The final set of RDCHs is dedicated to the measurements of the voltage reference devices (Tab. 10.8). The results from these channels can be used both to create a virtual “group VREF source” and to evaluate the TID-induced changes to VREF devices such as outlined in chapter 8.2.5. The design of the input stage of the ADC allows the input pins to be used as V_{REF} inputs of the ADC. Hence, the VREF sources of higher voltage (VREF1, 2, 3) could be used as a V_{REF} voltage for the measurements of the VREF4.

As can be seen in the tables Tab. 10.3 to Tab. 10.8, there are 138 DAQ channels identified for the RadEx2 experiment. However, there are two A/D converters present in the ADC chip, so all the readings are also performed by the ADC2 (24-bit A/D converter) to obtain a second set of data that can be compared with the first. Thus, any TID-induced difference in the performance of the A/D converters can be identified.

10.4.4 RadEx2 thermal-vacuum experiment

In addition to the RadEx2 DAQ channels, there is a possibility to perform an auxiliary experiment that can use the RadEx2 hardware for experimental measurement of the space vacuum. One of the methods for vacuum gauges (sensors) is based on a pressure-dependent thermal loss of a heated element through the gas [359].

One of the sources of measurement error of resistance thermometers (including the platinum type PRT) is self-heating (see Appendix E.2). This (normally parasitic) effect

can be used to measure thermal loss and thus vacuum-level on-board the satellite. The IDAC sources in the ADC chip allow the excitation current to be changed in steps (as shown in Tab. 10.5). The IDAC current range is from 50 to 3000 µA, which is equivalent to dissipated power from 2.5 µW to 9 mW. Therefore the PRT can be operated in two modes:

1. Low power mode, during which is the self-heating negligible
2. High power mode, during which the electric power in the order of milliwatts can create self-heating in order of a few °C [306]

To demonstrate this measurement method, a similar Pt1000 sensor was placed in a vacuum chamber, and the resistance was measured by the DMM Fluke 8808A using a four-wire measurement method. The STS measured the resistance using the first 20 kΩ range, during which the measurement current was 80 µA, and the PRT was dissipating 7 µW. These measurements were performed every second until T = 500 s. Then the range of the multimeter was switched to 2 kΩ for another 500 s and then (at T = 1000 s) back to 20 kΩ range. In the 2 kΩ range the multimeter provided 0.8 mA, and the PRT had to dissipate 0.7 mW. This step change in excitation current caused a warm-up of the PRT by 0.4 °C (Fig. 10.7) at the atmospheric pressure (green line in the chart). The chamber was then pumped out, and the pulsed self-heating measurement was repeated. The pressure dropped by more than five orders of magnitude, and the self-heating doubled.

The measurement resolution using the RadEx2 ADC will be significantly better than of the Fluke 8808A. Therefore this auxiliary experiment has an excellent potential to measure the vacuum when in orbit successfully. The EM/FM are planned to be tested in a calibrated vacuum chamber to obtain reference self-heating data (see section 10.5).

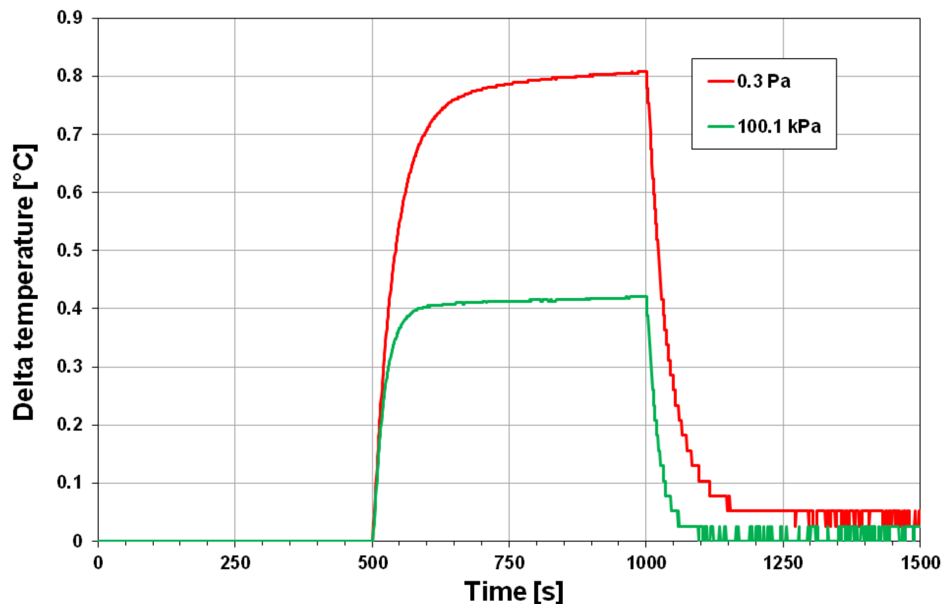

Fig. 10.7: Results of experimental measurement of vacuum level using self-heated PRT. The green line represents measurements made at ambient (atmospheric pressure), and the red line is a record obtained in a vacuum. The low resolution of the multimeter at 20 kΩ range caused the “step pattern” at the PRT cooled.

10.5 Development and testing plan for the RadEx2

The development, debugging and testing of the RadEx2 experiment was planned to be performed in the following phases:

1. Prototyping/demonstration phase (part of the PhD):
   a. A prototype of the RadEx2 hardware with a simulated satellite bus using standardised MCU core module and the STS software package
   b. In-situ DEMO TID test to validate the performance of the design
2. Engineering model phase (after the PhD, using at least five EM level PCBs of the final satellite hardware):
   a. Repeated thermal test to demonstrate the MU of the thermometers
   b. Vacuum testing to obtain reference data for the thermal-vacuum experiment (optional)
   c. Final In-situ TID-test using methodology of the DEMO TID test. The goal is to obtain TID data from the final hardware design to develop the LMMU models. Final sets of active components (from the same production lots as the FMs) are to be used.
3. Flight model(s) testing (after the PhD, in the months prior to the final assembly of the satellite):
   a. Final temperature calibration in the calibrated thermal chamber
   b. TID test - expose the FMs to low dose (TID level of 100 rad (Si) to obtain initial calibration data for the dosimetry sensors)
   c. Optional vacuum test/calibration
   d. Long-term (weeks, ideally months) of DAQ run to perform room-temperature burn-in and annealing from the low-dose TID exposure

The prototype of the RadEx2 (Fig. 10.8) was used as a demonstrator of the experiment and for the software development of the C library (see section 10.4.2).

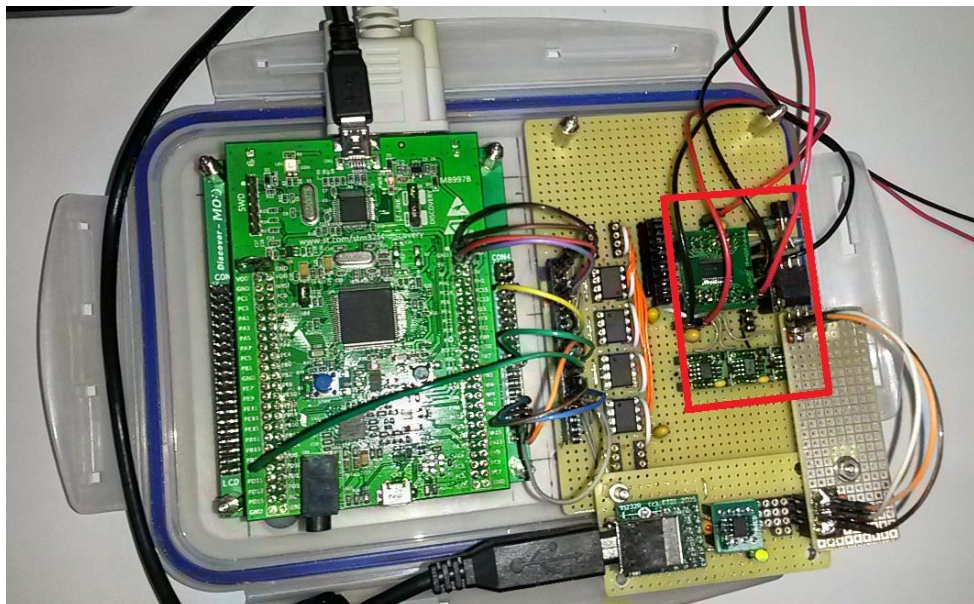

Fig. 10.8: Prototype of the RadEx2 experiment. It consisted of an MCU board (left-hand side) and the RadEx2 hardware (red-marked PCB area on the right-hand side).

10.6 RadEx2 DEMO TID test

The final TID test presented in this thesis was the RadEx2 DEMO TID test. The goals of this project were as follows:

- To practically demonstrate the designed capabilities of RadEx2 including:
    - Measurement of TID level (TID dosimetry)
    - Measurement of temperature
    - Testing of DUTs (combined measurement of VREF devices)
    - Self-testing of the ADC chip (A/D converters, current sources, system monitors)
- To obtain identical measurements using an external high-resolution multimeter so that the RadEx2 readings could be compared with "true" data in order to evaluate:
    - The in-orbit testing capability of the experiment
    - The accuracy of the ADC measurements
- To perform a TID test of the ADC chip (there were no TID data available for the ADS1263 when this chip was chosen)
- Measurement of TID-induced changes of the supply currents (to evaluate the impact of the TID on the power budget of the experiment).

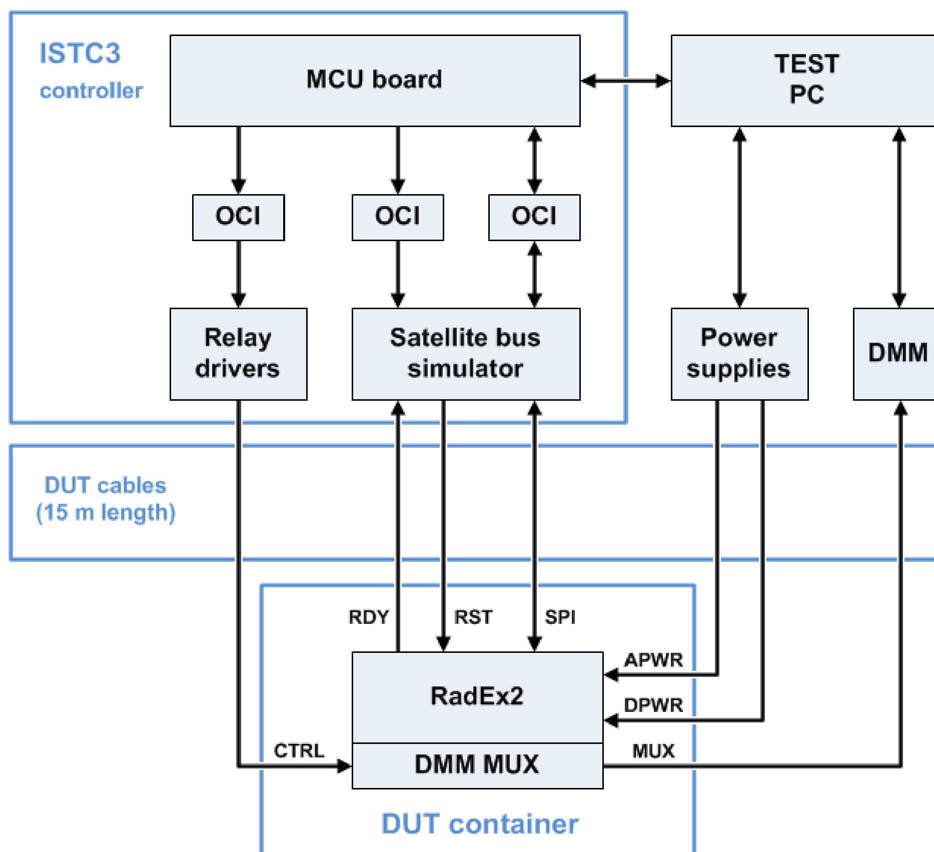

Fig. 10.9: Block diagram of the RadEx2 DEMO TID test. It consisted of the test hardware (placed outside the irradiation cell), a set of cables and DUT container placed in the irradiation cell.

10.6.1 RadEx2 TID DEMO test system

Fig. 10.9 shows a block diagram of the ISTM test system for the RadEx2 TID DEMO test, which was designed to simulate the conditions of anticipated spaceflights. The core of the test system was the ISTC3 controller that provided a digital satellite bus (SPI bus and control/status signals). ISTC3 also controlled the multiplexing relays for the multimeter (DMM MUX). The external multimeter was used to perform identical measurements as the ADC chip. Ultra-high precision digital multimeter DMM7510 was used. Moreover, the DMM measured temperature using its independent PRT; it also monitored power supply voltage lines (analogue power 5 V APWR and digital power 3.3 V DPWR), and both analogue and digital supply currents via low TC_R 10 Ω shunt resistors. The shunt resistors were normally bypassed. A photograph of the RadEx2 DEMO hardware can be found in Appendix D.5.

10.6.2 RadEx2 TID DEMO test conditions

The hardware for the RadEx2 TID DEMO test was practically identical to the planned design; however, there were some differences as can be seen in Tab. 10.9. The reference resistors were with higher TC_R because the anticipated SMD resistors were not available for the DEMO test due to a limited budget. The DEMO RREFs were also products of VISHAY with TC_R of ±2 ppm/°C typical (–55 °C to +125 °C), which was the lowest value of TC_R affordable for the DEMO test. Another difference was the PTR sensors. The standard PTRs were used such as in the DTC system (see section 6.5.2). Finally, the VREF DUTs were limited to three pieces as there was a need to release the AIN6 pin for the DMM MUX (the output from the TDAC could be connected to this pin for precise measurements by the external DMM).

Tab. 10.9: Allocation of the ADC inputs for the RadEx2 DEMO.

ADC input	Device PN	Function
AIN0 (REFP1)	ADR440	VREF1 (2.048 V)
AIN1	Y0785100K000T9L	RREF1 (100 kΩ)
AIN2 (REFP2)	LT1460	VREF2 (2.500 V)
AIN3	Y07851K00000T9L	RREF2 (1k kΩ)
AIN4 (REFP3)	ADR03	VREF3 (2.500 V)
AIN5	P1K0.232.6W.Y.010	PRT (Pt1000)
AIN6	-	TDAC to DMM
AIN7	ADR03	VREF3 temp. sensor
AIN8	ZVP1320	COTS PMOS
AIN9	TY1003	RADFET

The measurements were performed every 30 minutes during the TID test. The RadEx2 hardware was powered down during the idle times between the measurements.

The MIF cell was used for the irradiation phase of the test. In contrast to the previous TID experiments, the dose rate of 36 rad(Si)/hr was used to create conditions closer to those of the real radiation environment in space (as discussed in section 3.5).

The RadEx2 system was placed in the MIF facility for the entire duration of the DEMO test. The test consisted of three successive phases:

1. The pre-irradiation phase of 36 hours
2. Irradiation phase of 278 hours, the target TID level was 10 krad(Si)
3. 110 days (2640 hours) of annealing

10.6.3 RadEx2 TID DEMO test results for SEM current sources

The first analysis was focused on the performance of the ADC chip current sources, which are used for excitation of the dosimeters and temperature sensors of the RadEx2 SEM subsystem. The chart in Fig. 10.10 shows the measurements of the 10 µA current generated by the SBIAS block of the ADC chip. The deviation from the initial value is shown as recorded by the external DMM and the ADC1 converter (using VREFI). The match between these readings was better than 0.05 %. This current is used for excitation of the RADFET sensor. It should be noted that the time axis of the charts in this section is logarithmic in order to display all the test phases with appropriate time resolution.

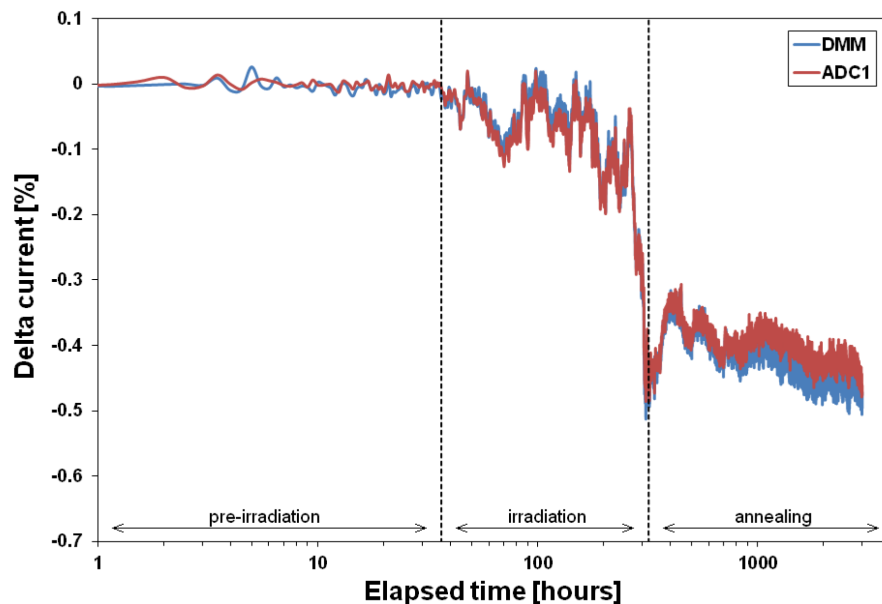

Fig. 10.10: Results of the test of the SBIAS 10 µA current source of the ADS1263. The blue line shows the measurements performed by an external DMM. The red dataset was obtained by the ADC1.

The excitation current for the PRT sensor was 100 µA, and it was generated by both IDAC1 and IDAC2 sources of the ADC chip (for both redundancy and comparable measurements). The results of the test of the IDAC1 are shown in Fig. 10.11. The TID-induced degradation is again a complex, non-monotonic, function. However, the degradation is significantly lower. Excellent match between the DMM and ADC1 readings could be seen too. The results for the TIDC2 test were practically identical.

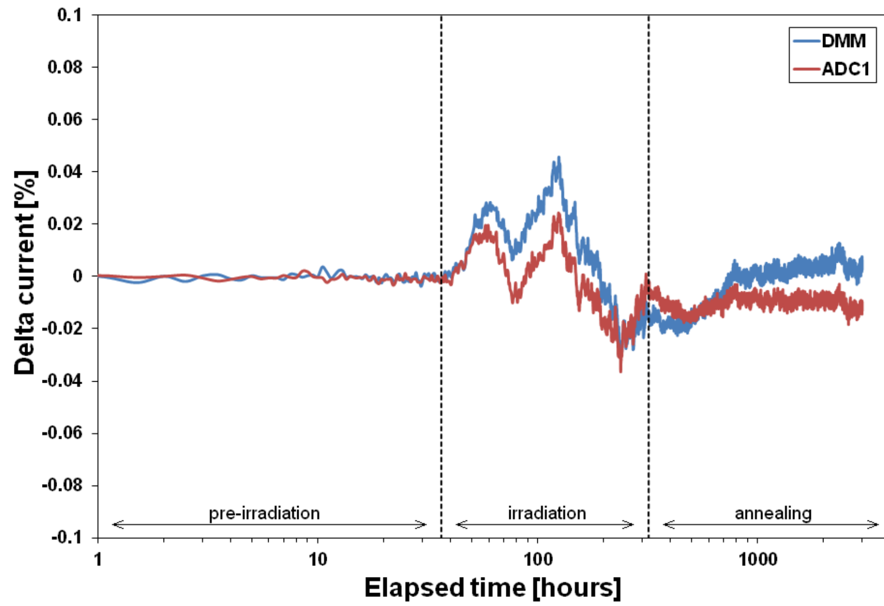

Fig. 10.11: Results of the test of the 100 µA generated by the IDAC1 current source of the ADS1263. The blue line shows the measurements performed by an external DMM. The red dataset was obtained by the ADC1.

The final current source tests to be shown in this section were for sourcing of 1000 µA. This current (again from each source) is used to measure the V_T of the PMOS sensor and DUT. The chart in Fig. 10.12 shows that the TID caused only minor degradation of this functionality of the ADC chip. TIDC2 exhibited similar changes.

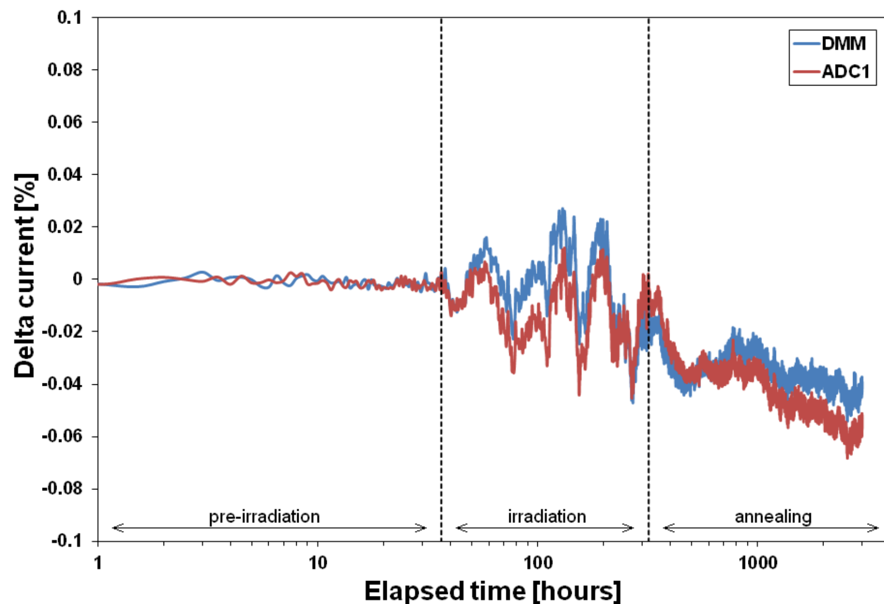

Fig. 10.12: Results of the test of the 1000 µA generated by the IDAC1 current source of the ADS1263. The blue line shows the measurements performed by an external DMM. The red dataset was obtained by the ADC1.

10.6.4 RadEx2 TID DEMO test results for SEM thermometers

The analysis of the current sources showed that there was only a minor impact of the irradiation on the excitation currents and that the ADC chip can accurately measure these changes. Next step was an analysis of the performance of the various temperature sensors to be used in the RadEx2 experiment (see Tab. 10.5 and Tab. 10.6 for the definition of these DAQ channels).

The first evaluation was focused on the behaviour of the PRT (Pt1000) sensor. There were two identical sensors; one was connected to the ADC chip, and the other was attached to the DMM. As discussed in section 6.5.2, these sensors can be assumed to be radiation resistant. Therefore, the DMM measurements of the PRT sensor, as shown in Fig. 10.13, could be used as the true value of the temperature and all other readings were compared with it. The temperature was controlled by the ambient air in the MIF facility; no active temperature control was used.

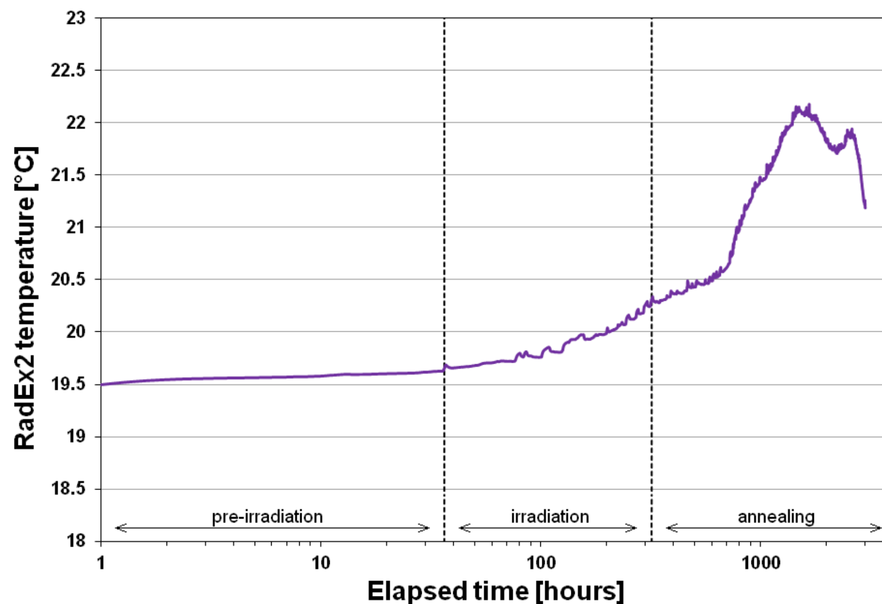

Fig. 10.13: Measurement of the temperature of the RadEx2 module during the TID DEMO test.

Prior to the experiment, the PRT measurements performed by the ADC1 were calibrated (matched) with the true temperature readings made by the DMM. The results of the calibrated ADC1 readings during the DEMO test are plotted as a green line in Fig. 10.14. The measurement error was within ±0.1 °C. One of the sources of such an error was the TID-induced degradation of the current source IDAC1, which was used for excitation of the PRT sensor. As demonstrated in Fig. 10.11, the RadEx2 has the capability to precisely measure the true value of the IDAC1 current source. Hence, the IDAC1-induced error could be compensated. The resulting measurement error for the compensated readings was significantly lower than the calibrated readings (red line in Fig. 10.14). This plot was not perfectly flat. There is a “U-shaped” trend in it, which could be caused by the calibration and PRT model used. The resistance-temperature model of Pt1000 is non-linear, but the resistance channels were calibrated using linear functions. Hence, the non-linear differences between the sensors could be seen.

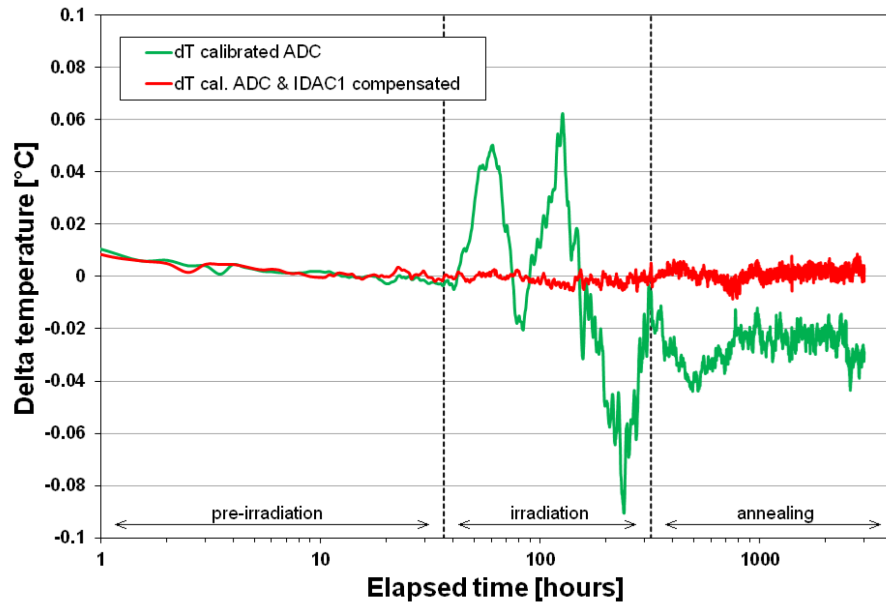

Fig. 10.14: Measurement errors of the RadEx2 PRT temperature acquired by the ADC1 during the TID DEMO test. The green line represents the calibrated ADC1 readings, and the red dataset displays calibrated ADC1 data compensated for the IDAC1 errors.

The ADC chip has a temperature sensor, which is based on two internal diodes with one diode having 16 times the current density of the other. The difference in the current density of the diodes generates a voltage that is a function of temperature [357]. The resulting measurement error plot in Fig. 10.15 showed a response to TID similar to the current sources. Hence the errors were likely caused by the sources. However, the design of the chip does not allow monitoring of the current sources. Therefore there was no means for compensating for the TID-induced changes of the current sources.

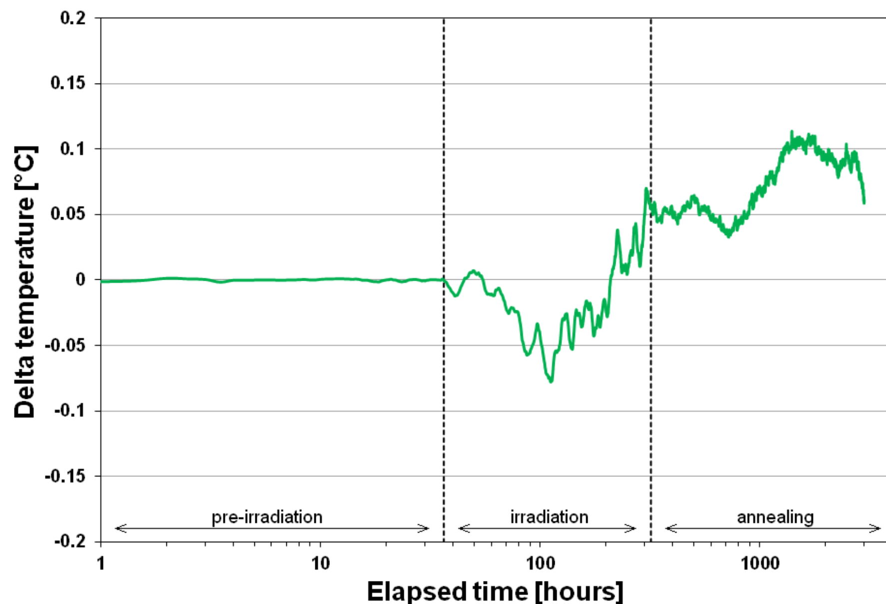

Fig. 10.15: Measurement errors of the RadEx2 ADC chip temperature sensor read by ADC1.

The ADC chip also measured the temperature sensor output of the ADR03 (VREF3). This channel was expected to be sensitive to TID as it was measured during the VREF experiments (see section 8.2.5). Therefore this measurement was not intended to be a primary source of temperature data for the SEM, but rather a DUT channel. The results confirmed the expected behaviour (Fig. 10.16 versus Fig. 8.6). The expected TID-induced change at 10 krad(Si) was approximately 2 °C; the measured value was 2.9 °C. The difference could be explained by a DUT-DUT difference (the devices were from the same lot) and also by the different input impedance of the DAQ systems used (ADR03 temperature output is not buffered). The difference in the input impedance of the DMM and ADC1 could also be partially responsible for the minor difference between the DMM and ADC1 readings in Fig. 10.16.

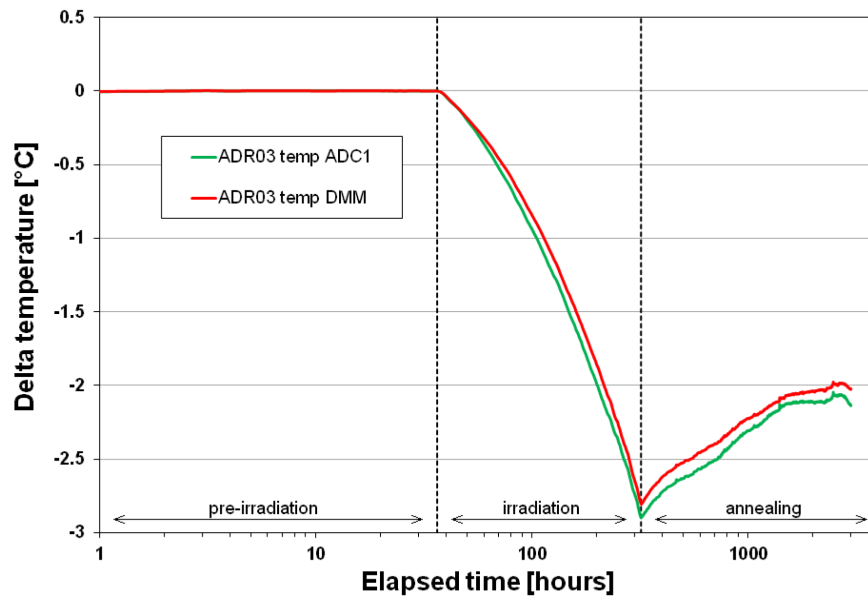

Fig. 10.16: Measurement errors of the RadEx2 VREF3 temperature sensor acquired by ADC1 using VREFI (green line) and the DMM (red line).

The final evaluated temperature channel will be independent on the ADC chip; there will be digital thermometers DS18B20 in the RadEx2 experiment. The TID-induced changes of these 1-Wire thermometers (OWTs) were measured during the early phases of the PhD, and these sensors were found to be sensitive to TID [125]. Another set of similar measurements was performed as an auxiliary experiment to the PMOS-RADFET combined experiment (section 7.4). A set of three DS18B20U+ devices in the USOP-8 package was tested [360]. No TID-induced changes were observed. This conflicted with the results of the early experiment and could be a product of the COTS nature of these devices (there was a six-year gap between purchasing the device sets).

In conclusion, the DEMO TID test showed that the SEM part of the RadEx2 experiment could measure the temperature using four methods. Two of them can be used as TID-resistant (compensated PRT readings, DS18B20U+ sensors) and one had acceptable measurement error (internal temperature sensor of the ADC chip). The fourth one (ADR03) is TID sensitive and thus can be used as a DUT for demonstrating the in-orbit test capability of the RadEx2 experiment.

10.6.5 RadEx2 TID DEMO test results for SEM dosimeters

The dosimetry part of the SEM subsystem is based on two PMOS devices. The TY1003 RADFET is intended to be a primary dosimeter, and the ZVP1320 is planned to act as a secondary dosimeter and a DUT. These devices were extensively tested during a series of TID experiments as summarised in chapter 7.

The results from dosimetry channels of the RadEx2 TID DEMO test were analysed with the following objectives:

1. To evaluate the ability of the ADC chip to measure the V_T of the sensors
2. To analyse a method of calibrating the TID responsivity of sensors proposed for the RadEx2 mission
3. To investigate the annealing effects of the dosimeters

During the irradiation, both devices responded to the increased TID levels by shifting their threshold voltage V_T as shown in Fig. 10.17. The V_T was measured at the same currents as during the previous PMOS experiments: TY1003 was measured at 10 µA, and the ZVP1320 was driven by 1 mA.

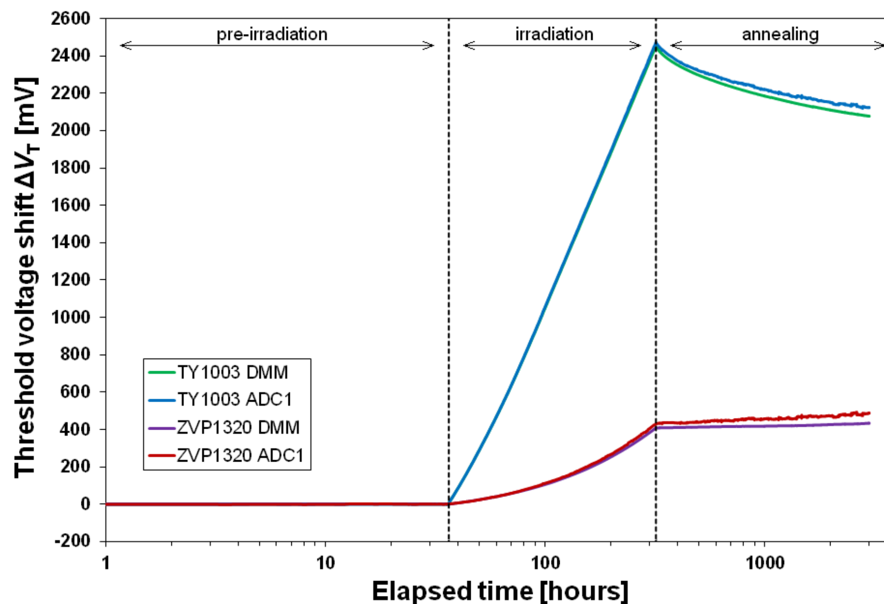

Fig. 10.17: Threshold voltage shift of the dosimetry devices measured by the DMM and ADC1 during the TID DEMO test of the RadEx2.

The initial threshold voltage V_{T0} of the TY1003 was 0.9 V, and it was equal to 3.2 V for the ZVP1320. Therefore the voltage span of the dosimetry readings exceeded the voltage range of the VREF sources in the RadEx2 DEMO. Hence, the ADCs had to use AVDD (5 V) as a reference voltage. Therefore the raw ADC1 readings in Fig. 10.17 had higher values than the DMM readings and were noisier (due to the ripple of the power supply and 15 m cabling). These errors were plotted in a relative scale (percentage of the reading) in Fig. 10.18 and could reach up to 1.5 % of reading. This problem was only a limitation of the design of the hardware for the TID DEMO. The final RadEx2 experiment will be equipped with a COTS 4.096 V VREF device.

However, the TID DEMO experiment could compensate for this issue by using the measurements of the AVDD (ADC chip can monitor both analogue and digital supply voltages). The resulting errors were lower by more than an order of magnitude (red and blue datasets in Fig. 10.18.).

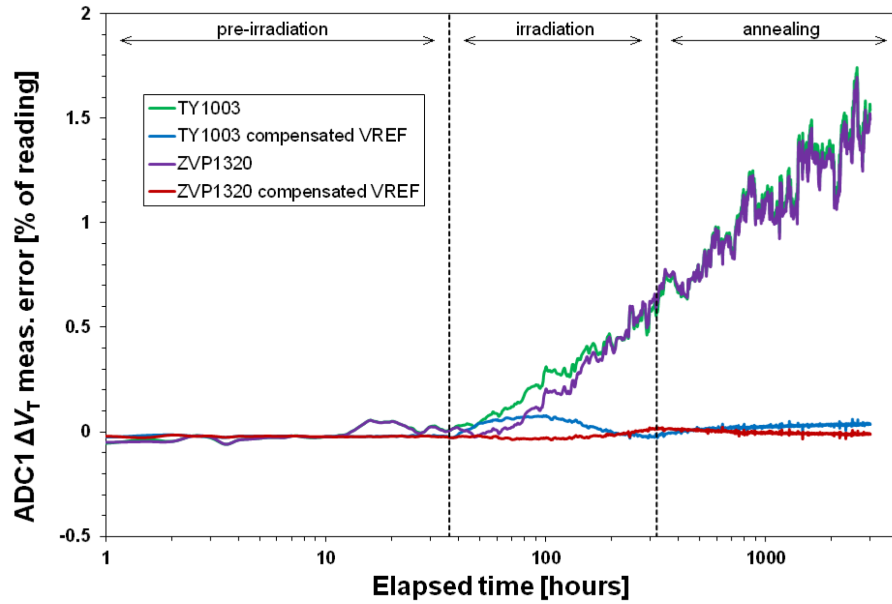

Fig. 10.18: Measurement errors of the threshold voltage shift of the dosimetry devices measured by the ADC1 during the TID DEMO test of the RadEx2.

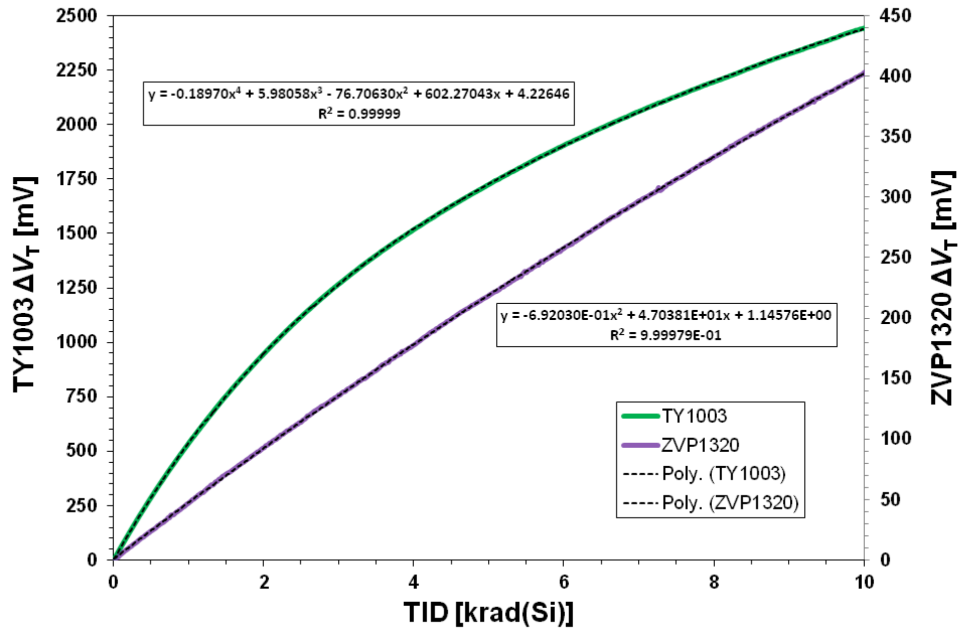

Fig. 10.19: Results ΔV_T of the dosimetry devices measured by the ADC1 and compensated for the AVDD and current sources.

Furthermore, the threshold voltage shifts ΔV_T of the dosimetry devices measured by the ADC1 were corrected for the TID-induced shift of the SBIAS and IDAC1 current sources (see section 10.6.3). The resulting "true" ΔV_T data were plotted as a function of TID, and polynomial functions were used to fit the plots (Fig. 10.19). The R^2 coefficients were nearly 1.0 which suggested an excellent fitting of the polynomial functions.

The threshold voltage shift ΔV_T plots need to be calibrated in order to obtain the measured TID levels. The calculated polynomial functions were valid only for the irradiated dosimeters. Despite the annealing effect, the irradiation is a one-way process (it cannot be repeated). Therefore only an indirect calibration can be used. The key issue is the device-to-device variation even for RADFETs from the same lot [250]. To address this issue, the RadEx2 PCB engineering models (at least five pieces) will be irradiated at the lowest dose rate practically achievable to obtain calibration curves. The flight models will also be irradiated to a small dose of 100 rad(Si) in order to obtain initial responsivity of the dosimetry devices to be flown. Both the engineering and flight models will be constructed from the devices delivered in the same lots. It is believed that this process can produce calibration data with acceptable quality.

To illustrate the proposed calibration process, the data from the PMOS-RADFET combined experiment were used (see section 7.4.3). There were three TY1003 devices irradiated under the non-biased regime. Hence the results were similar to those of the RadEx2 experiment. There was a significant difference in the response of the devices to irradiation (Fig. 7.17). The data were calibrated using a common polynomial function and individually adjusted using the initial response to TID. The resulting measurement error plots are shown in Fig. 10.20. The testing of the RadEx2 engineering models is expected to produce more precise calibration data due to a higher number of samples and up to two orders of magnitude lower dose rate. The TID measurements will also be combined with the results of the ZVP1320s that provide a nearly linear response to TID.

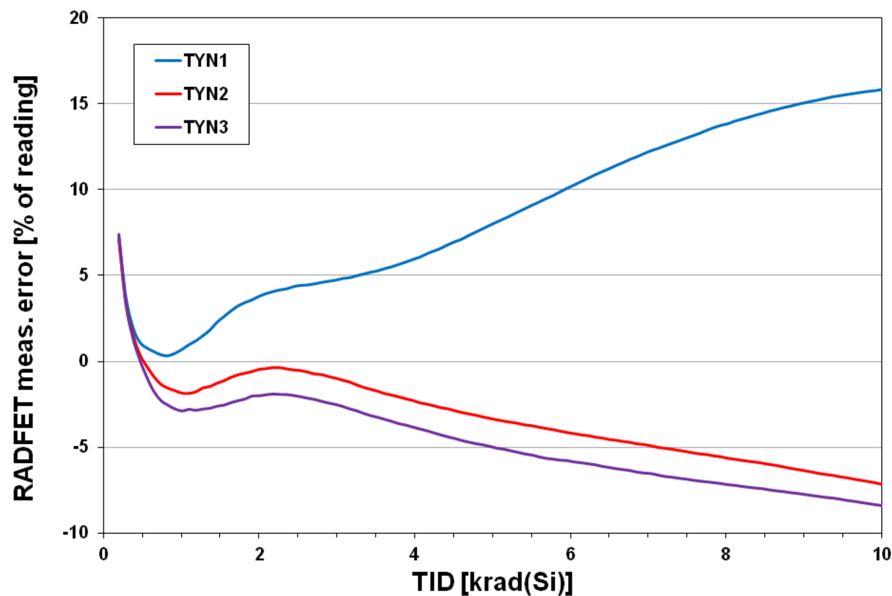

Fig. 10.20: Measurement errors of the TY1003 RADFETS. The data from the PMOS-RADFET combined experiment were used.

The long-term data acquisition of the RadEx2 TID DEMO allowed a detailed measurement of the annealing (fading) of the dosimeters. As displayed in Fig. 10.21, the RADFET device started to anneal immediately with a similar trend as during the PMOS-RADFET combined experiment (Fig. 7.17). The annealing trend was similar, but the magnitude was smaller (8 % versus 20 % at 1000 hours). Such a difference could be explained by a five-time higher end dose of the PMOS-RADFET combined experiment. The initial annealing of the ZVP1320 was negligible (it was lower than 0.1 % first 100 hours). The annealing of these two dosimeters offers an interesting ability to observe the zero radiation moments of the mission (the V_T of the RADFET would start dropping while the ZVP1320 remains stable).

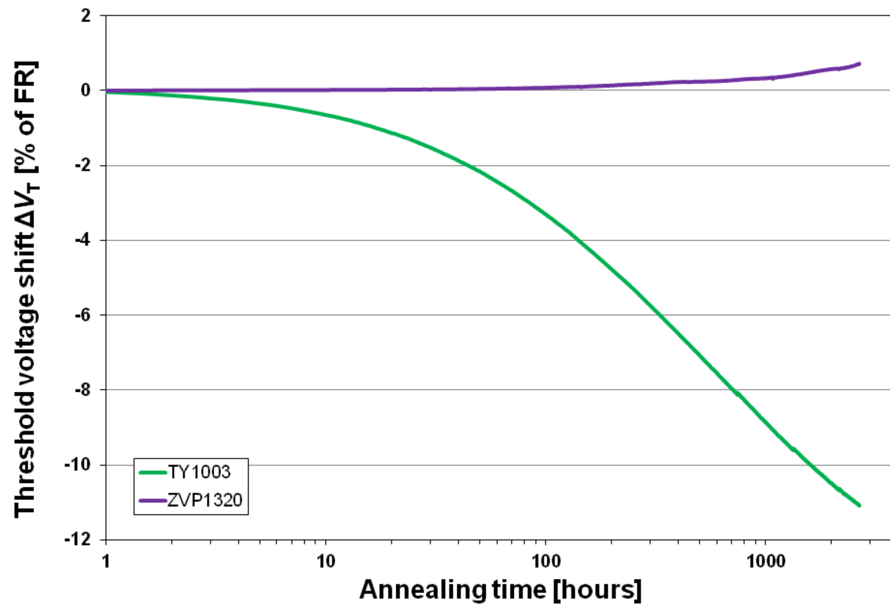

Fig. 10.21: Measurements of the annealing of the dosimetry part during the RadEx2 TID DEMO test.

10.6.6 RadEx2 TID DEMO test results for ADC

The ADC is equipped with an internal test D/A converter (TDAC). This DAC is designed as a programmable voltage divider, used for self-testing and verification of both ADCs. It has an output range of 0.5 to 4.5 V, and the accuracy is specified as 0.1 % typical and 1.5 % maximal [357]. The AVDD voltage is the only option for the reference voltage source of the TDAC and the ADC under the self-test.

The TID DEMO data were firstly analysed for a potential degradation of the performance of the TDAC. Both the TDAC output voltage and its reference voltage (AVDD) were measured by the DMM. Nine voltage steps were measured as defined in the Tab. 10.7. The initial mid-scale DC error was 315 ppm. The TDAC data did not show any TID-induced degradation of the nine test voltage steps. Furthermore, the *INL* was calculated for three moments of the TID DEMO test using the formula (4.6). As shown in Fig. 2.1, there was also no observable TID-induced change of the *INL* of the TDAC. The *INL* repeatability (the difference between the three *INL* plots) was limited by the compensation for the AVDD and its noise.

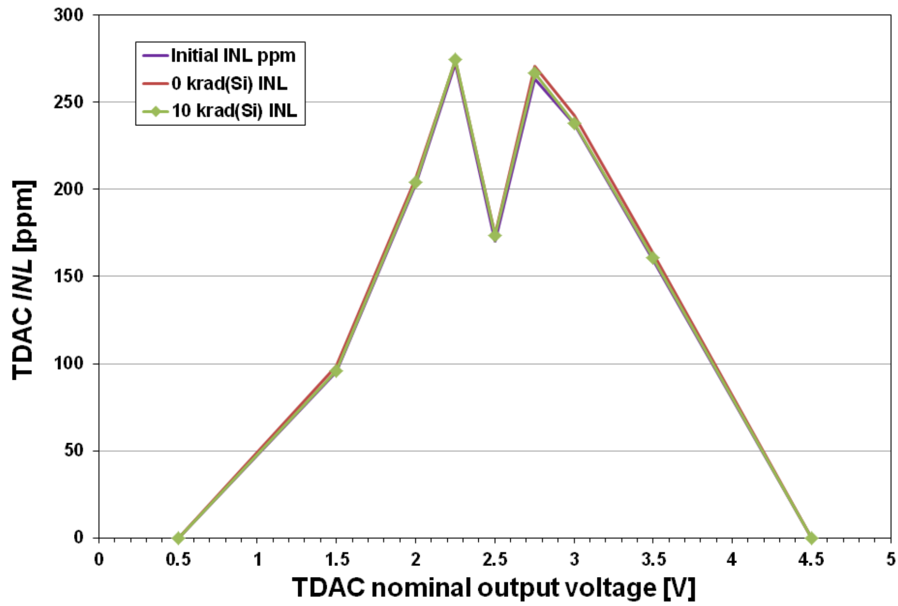

Fig. 10.22: Integral non-linearity of the TDAC part of the ADC chip measured by the DMM during the RadEx2 TID DEMO test.

Identical *INL* analysis was performed for the TDAC voltage steps measured by the ADC1. The obtained values of *INL* were identical to those from the DMM. Therefore the *INL* of ADC1 was negligible and has not changed during the irradiation (Fig. 10.23). Furthermore, the repeatability of the *INL* measurements was significantly better due to the direct measurements by the ADC1 (AVDD was V_{REF} for the ADC1, so the noise had lower impact, and the measurements were performed within the ADC chip).

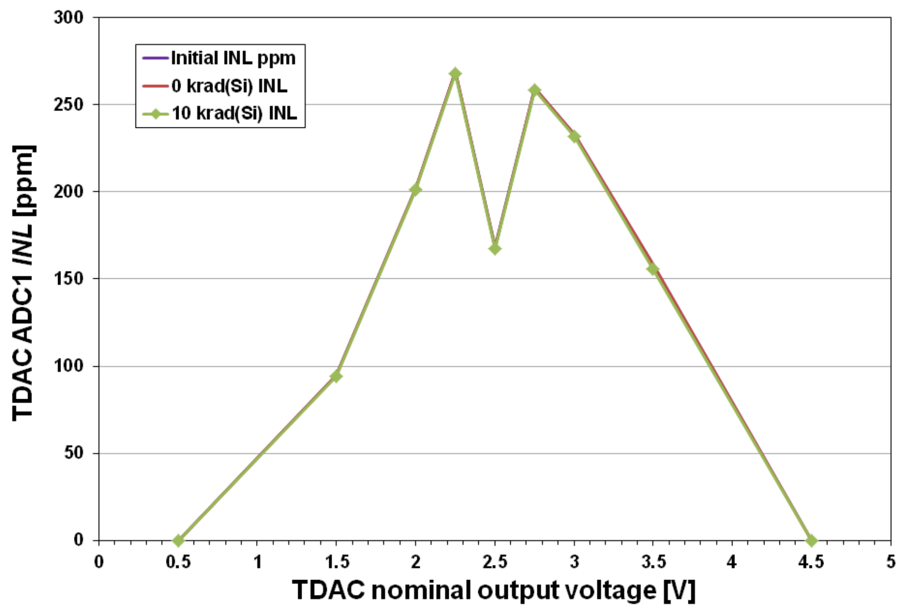

Fig. 10.23: Integral non-linearity of the TDAC part of the ADC chip measured by the ADC1 during the RadEx2 TID DEMO test.

The analysis of the *INL* could only identify ADC errors “modulated” on the base non-linearity of the TDAC. However, the TDAC was measured to be stable (within the resolution of the measurement method used). Hence, the measurements (conversions) of ADC1 taken at each TDAC voltage step were analysed to obtain finer details. The chart in Fig. 10.24 shows the results of ADC1 measurements of three TDAC voltage steps.

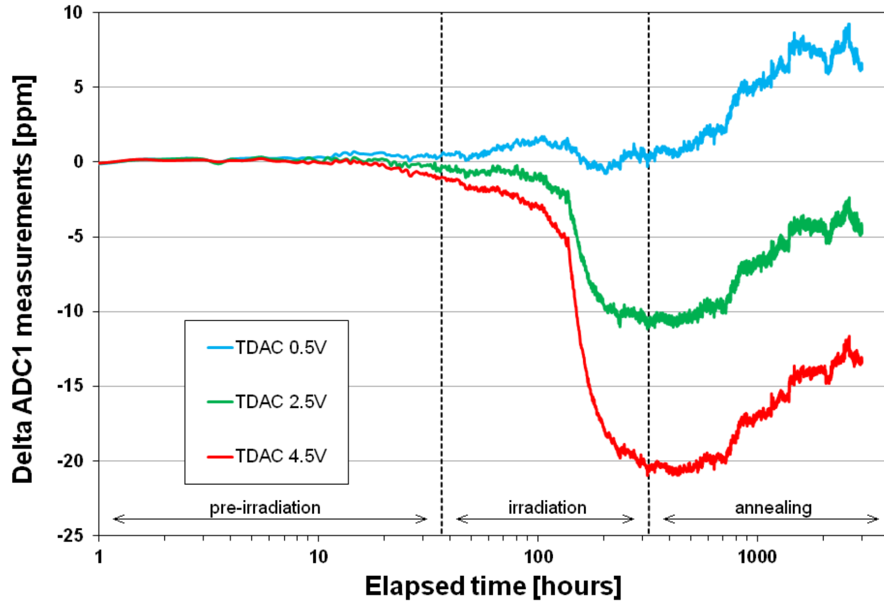

Fig. 10.24: Plots of three test voltages generated by the TDAC of the ADC chip and measured by the ADC1 during the RadEx2 TID DEMO test.

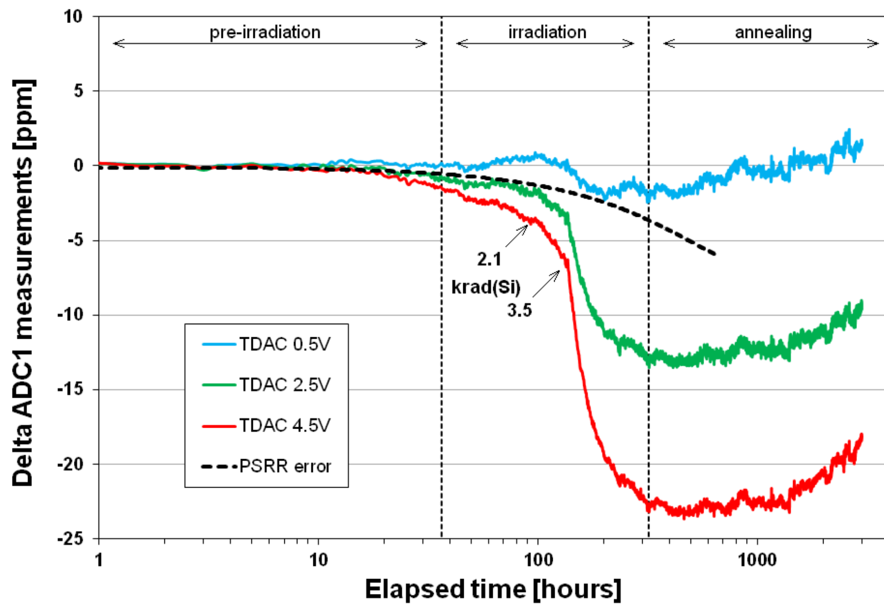

Fig. 10.25: Plots of three test voltages generated by the TDAC, measured by the ADC1 and compensated for the ADC1 offset drift due to variations in ambient temperature.

Strong temperature drift of the measured TDAC voltage steps could be seen (see plots in Fig. 10.24 versus temperature record in Fig. 10.13). The offset drift was, in fact, a product of the TDAC test; the offset self-calibration ("chop mode") had to be disabled to allow for the TDAC measurements [357]. The data were processed to compensate for the offset drift by subtracting this component from the ADC data using the actual value of the RadEx2 temperature and calibration data obtained from the pre-irradiation phase. The resulting chart in Fig. 10.25 is practically free of the influence of the temperature.

While the zero-scale reading (0.5 V, the TDAC could not generate a lower voltage) remained within ±1.5 ppm window, the other two measurements exhibited a TID-induced degradation. The degradation started at TID-level of 2.1 krad(Si) and accelerated more at a dose of 3.5 krad(Si). However, there was an obvious trend in the 2.5 and 4.5 V readings even during the pre-irradiation phase of the test, which must have been a product of some other error source. The offset calibration suppressed the impact of the temperature. The other source of instability was the AVDD, which was supplied by a classical bench-top power supply TTi EL302RD. This instrument was not able to keep stable voltage long-term. The actual value of the AVDD was measured by the DMM (for the testing of the TDAC), and this data was used to simulate a potential ADC error due to the PSRR (Power Supply Rejection Ratio). The datasheet value of the ADS1263 PSRR was -80 dB, or 0.1 mV/V [357]. The calculated error caused by the PSRR was plotted as a black dashed line in Fig. 10.25 and its trend was similar to the initial trends in the ADC1 readings. Therefore it is believed that the initial trends in the plots were caused by the long-term decrease of the AVDD unrelated to the irradiation.

The readings of the ADC1 offset error could also be obtained from the measurements of the RREF2, which was measured in an unbiased mode providing zero-scale (input shorted) readings. The data showed excellent stability of the self-calibration and that TID had only a small impact on this ultra-low error (Fig. 10.26).

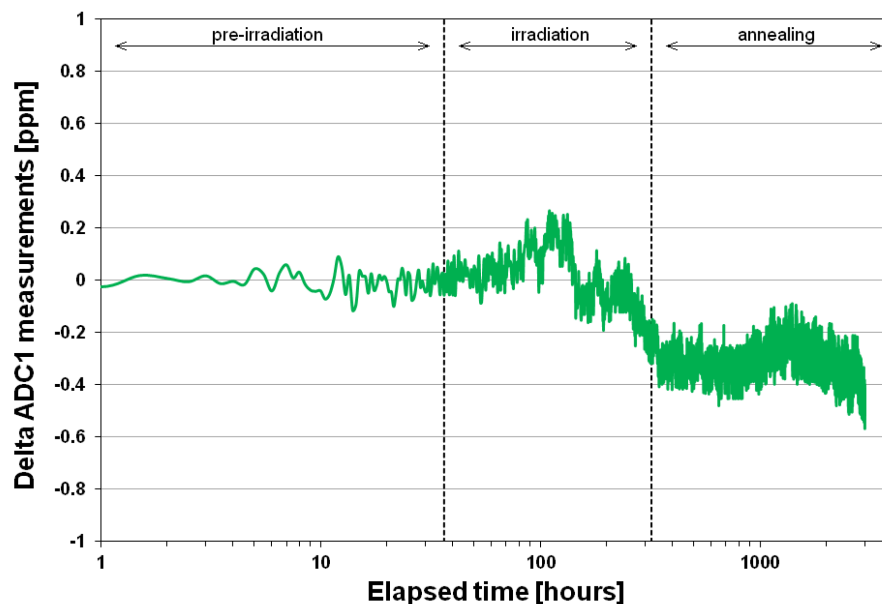

Fig. 10.26: Zero-scale measured by the ADC1 connected to an unbiased RREF2 resistor and compensated for the ADC1 offset drift by self-calibration.

The ADC chip has an auxiliary A/D converter (ADC2). This converter was also tested as the ADC1, and it performed regular measurement of identical channels as ADC1 including measurements of the TDAC test voltages. The first result for ADC2 was the zero-scale RREF2 test (Fig. 10.27). Although the ADC samples were significantly noisier than for the ADC1, the averaged reading showed that there was no observable impact of the TID on the offset of the ADC2.

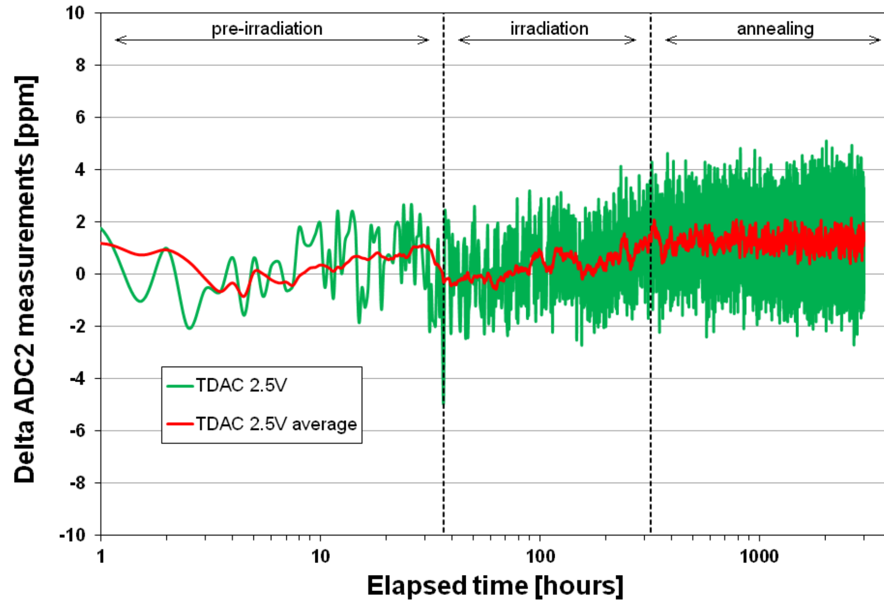

Fig. 10.27: Zero-scale measured by ADC2 connected to an unbiased RREF2 resistor (green line). The red line represents averaging of 20 ADC samples.

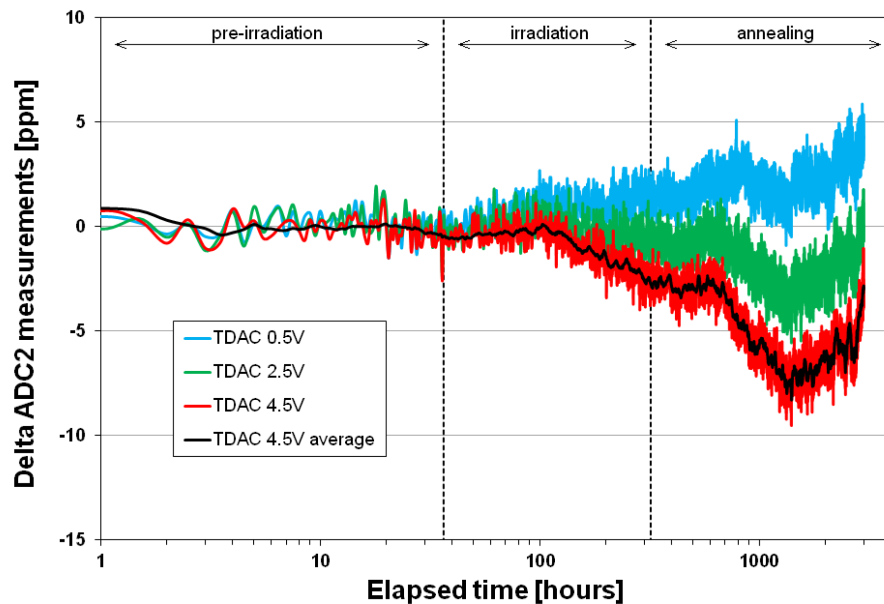

Fig. 10.28: Plots of three test voltages generated by the TDAC, measured by ADC2 and compensated for the ADC2 offset drift due to variations in ambient temperature.

The TDAC data for ADC2 were also processed using the identical method as for the ADC1. Therefore the results could be directly compared. The chart in Fig. 10.28 shows TDAC test results for the ADC2 which were corrected for the ADC2 offset voltage temperature drift. In contrast to ADC1 (Fig. 10.25), there was no initial trend in data, which would suggest that the ADC2 was immune to the non-TID influence causing the initial trend in ADC1 data (probably ADC2 had higher PSRR). The average values of the ADC2 samples (black line in Fig. 10.28) showed that the TID-induced degradation also started at TID-level of approximately 2 krad(Si) and was weaker than for the ADC1 (5 ppm at 4.5 V versus 23 ppm for the ADC1 at the same voltage).

The results of the testing of the TDAC and ADCs of the RadEx2 core ADC chip can be summarised as follows:

1. The TDAC (despite its limited voltage resolution) appeared to be suitable for the in-orbit self-testing of the on-chip ADCs
2. The common VREF source for both TDAC and ADC under test makes the TDAC testing immune to VREF noise and drifts. However, the ADCs could be sensitive to PSRR. Therefore the AVDD needs to be as stable as possible during the in-orbit operations. The data from the testing of the engineering models also need to be analysed for this problem (the results from the VREF testing suggested that the PSRR might also be changed by TID (see results for line regulation in section 8.2.6).
3. The TID-induced changes could be measured with a resolution better than 0.1 ppm for the ADC1. The observed degradation of ADC2 was lower than for the ADC1, and this phenomenon (if confirmed by testing more EM samples) could be used as a base-line for cross-comparison analysis of the ADCs.
4. The ADC2 had had significantly higher noise than ADC1. This was expected as the ADS1263 datasheet defines the RMS noise levels as 0.121 μV for ADC1 and 7.34 μV for ADC2 [357].

10.6.7 RadEx2 TID DEMO test results for VREF devices

There were four voltage references measured during the TID DEMO test (Tab. 10.9). Three of them were COTS VREF devices of the same types and from the same lots as those tested in the series of VREF experiment (see chapter 8). The fourth device was the internal VREF source in the ADC chip (VREFI).

The VREF1 to VREF3 were external to the ADC chip, and their output voltage was measured by both the ADCs and the DMM. However, the VREFI was available only as a reference source for ADCs. Hence the VREFI could be measured only indirectly by the AD sampling of an external reference voltage VREF1, which had a nominal output voltage of 2.048 V and thus was within the 2.5 V range of the VREFI. The indirect measurement method could also be used for the other two reference devices VREF2 and VREF3.

The first analysis was performed using the DMM measurements of the output voltage of the external VREF devices (Fig. 10.29). The TID-induced changes were comparable to those measured previously (data from the nearly identical test are shown in Fig. 8.3. using the same colour-coding of the plots). Rather unexpected was the noisy response of the VREF2, which could be a product of the TID-induced degradation of

the line regulation of VREF2 (Fig. 8.7) and also an effect of the changes of the ambient temperature as measured during the TID-TC experiment (see section 8.3.5).

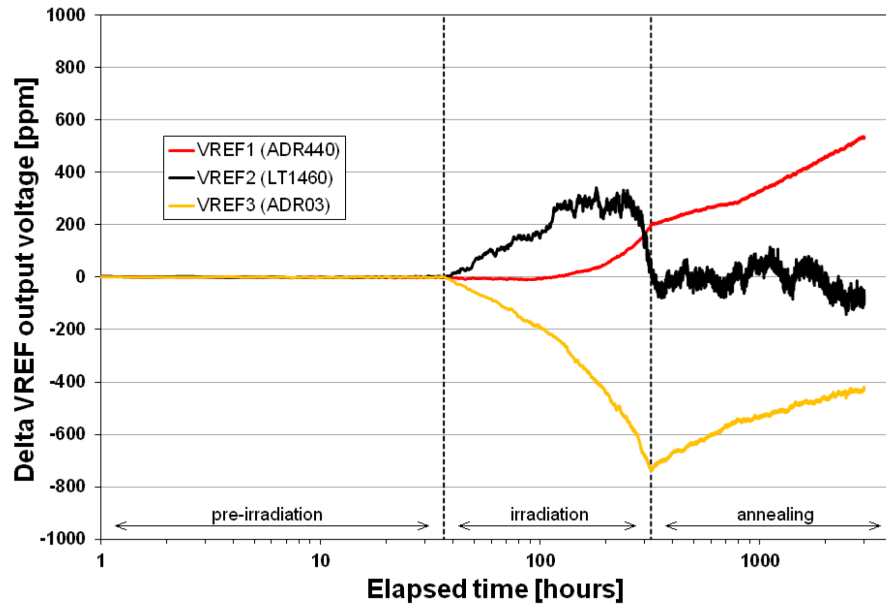

Fig. 10.29: DMM measurements of the TID-induced changes and annealing of the VREF devices during the RadEx2 TID DEMO test.

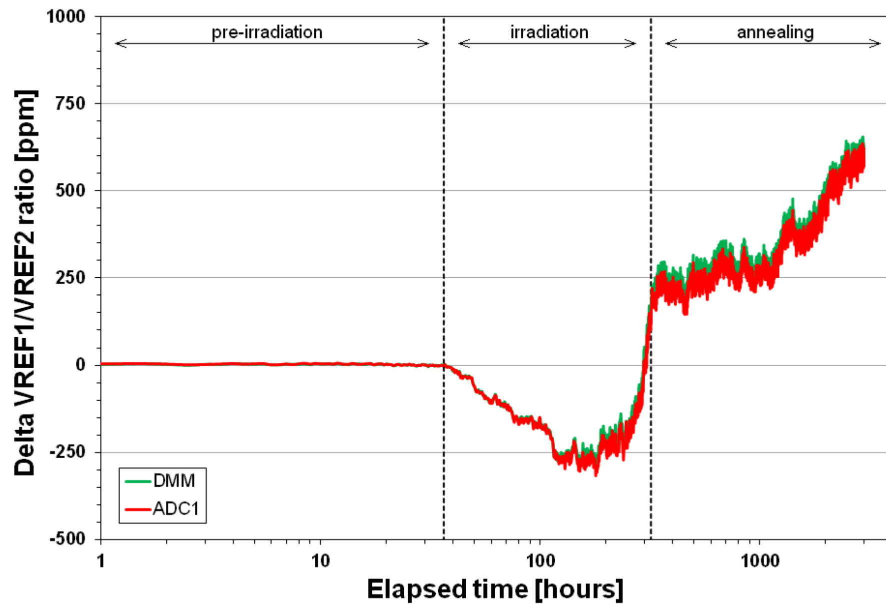

Fig. 10.30: ADC1 and DMM measurements of the TID-induced changes and annealing of the VREF1/VREF2 ratio during the RadEx2 TID DEMO test.

Next step was an analysis of the measurements of the VREF devices performed by the ADC1. The results of the ADC1 measurements were compared with the DMM readings, which were processed to provide comparable proportional AIN/VREF data as

the ADC1 (ratio between the VREF1 and VREF2 were calculated). The resulting VREF1/VREF2 plots showed a slight difference between ADC1 and DMM readings (Fig. 10.30). Similarly, the results for the VREF1/VREF3 in Fig. 10.31 showed that there was a small error in the ADC1 readings.

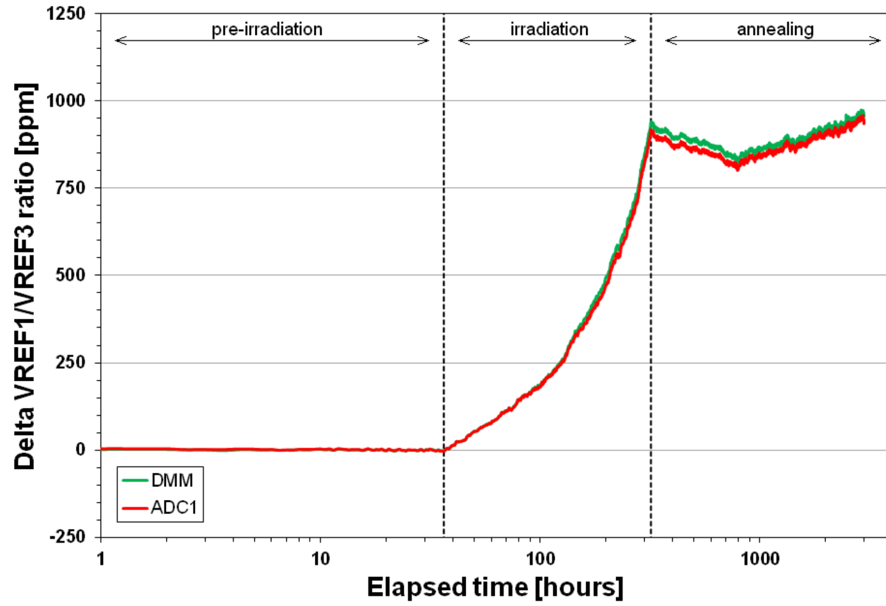

Fig. 10.31: ADC1 and DMM measurements of the TID-induced changes and annealing of the VREF1/VREF3 ratio during the RadEx2 TID DEMO test.

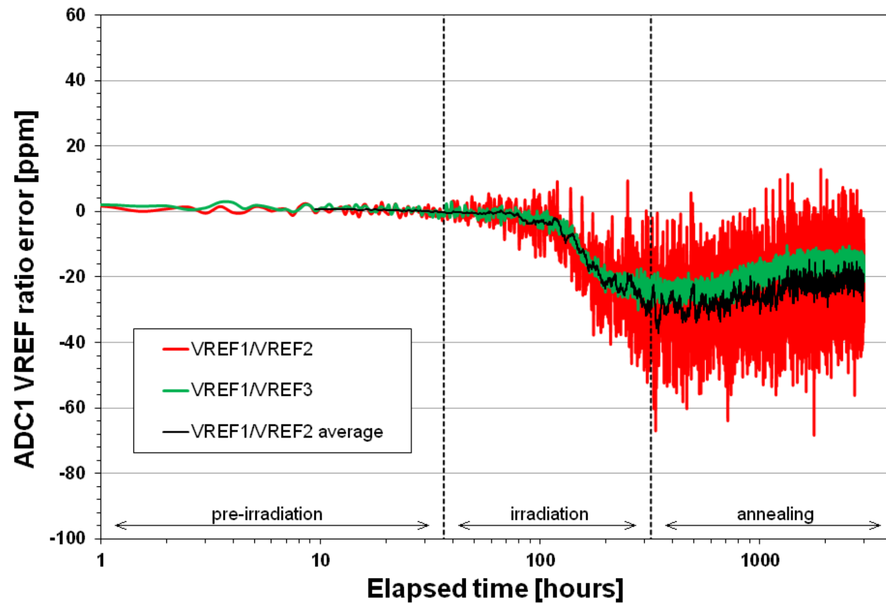

Fig. 10.32: Measurement error of the proportional measurements of the VREF1/VREF2 and VREF1/VREF3 ratio performed by the ADC1 during the RadEx2 TID DEMO test.

The measurement error of the ADC1 VREF measurements was plotted for the whole duration of the TID DEMO test (Fig. 10.32). This was another method to test the performance of the ADC1 during the test as it did not use the TDAC and the AVDD as a reference voltage. The resulting plot was in a good agreement with the outputs from the TDAC test (Fig. 10.32 versus Fig. 10.25).

The final VREF analysis was focused on the performance of the internal voltage reference VREFI. Two methods were used to investigate the TID-induced degradation of the VREFI, as follows:

1. The Results of the ADC1 measurements of the VREF1 (using VREFI as a reference source) were compared with the results of the VREF1 measurements performed by DMM
2. The ADC1 regularly measured DVDD voltage using the DVDD monitor feature referred to the VREFI. The DVDD voltage was also regularly measured by the DMM.

The results of these two methods were practically identical (Fig. 10.33), and thus could be used as a record of the TID-induced degradation of the VREFI source and the ADC1. This error was present also during the measurements of the SEM sensors, but its impact is minor in comparisons with measurement errors inherent to the SEM sensors.

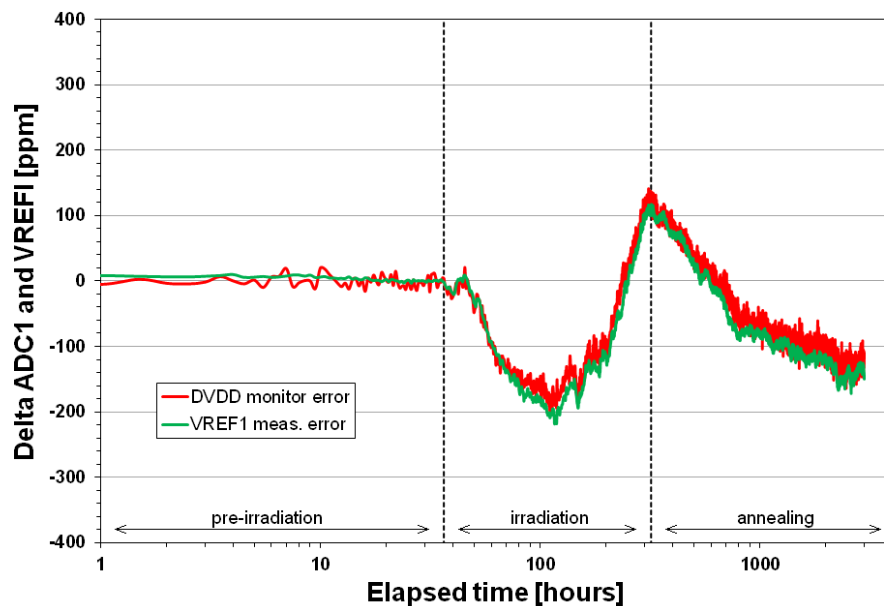

Fig. 10.33: TID-induced degradation and annealing of the VREFI and ADC1 measured during the RadEx2 TID DEMO test.

10.6.8 RadEx2 TID DEMO test results for supply currents

The final RadEx2 TID DEMO data analysis was dedicated to the TID-induced changes of the supply currents. The digital supply current was only supplied to the ADC chip, and it stayed stable at a value of 1 mA ±5 % during the entire RadEx2 TID DEMO test.

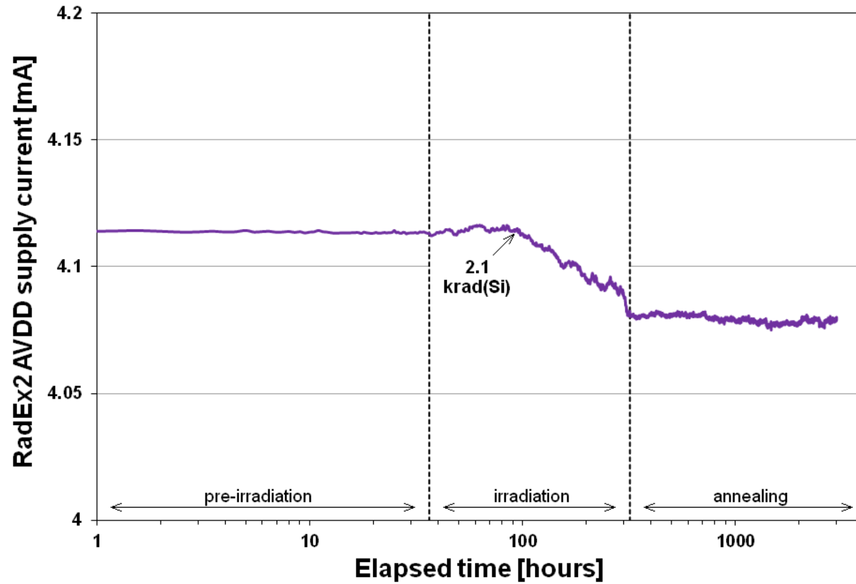

Fig. 10.34: TID-induced changes and annealing of the analogue supply current measured by the DMM during the RadEx2 TID DEMO test.

The readings of the analogue supply current were reflecting the TID-induced changes of the ADC chip. As can be seen in Fig. 10.34, the analogue current started to decrease at the dose identical to the dose at which the degradation of ADCs started.

10.7 Conclusions of the in-orbit experiments

The final experimental chapter of this thesis was focused on development and testing of an experiment RadEx, which was intended to be one of the first attempts to observe TID-induced degradation of high-precision DAQ electronics during a space flight. Two generations of RadEx experiments were developed following the constraints of the CubeSats, which were the primary platforms for these experiments. However, the RadEx2 can be flown on almost any spacecraft.

The work on the RadEx1 experiment had to be stopped due to the cancellation of the CubeSat mission the experiment was designed for. However, the RadEx project was later restarted as RadEx2, which became more advanced as it was designed to achieve significantly higher resolution/accuracy, and as well as lower power and PCB area.

Two flight opportunities for the RadEx2 were successfully negotiated on-board CubeSat missions. The schematic of the RadEx2 was integrated with the hardware design of both satellites. An integration package was also created to ease implementation of the RadEx2 with potential future missions.

A test plan for the RadEx2 was defined, and it has three stages. The first stage was completed as a part of the presented PhD research; it was focused on a validation of the design of the experiment and demonstration of its functionality (both regarding the performance of the DAQ hardware and its response to radiation). Prototype hardware of the RadEx2 was built and used as a demonstrator and as a platform for the development of the software library, which was used for ground testing as well as for the satellites.

The second principal part of the RadEx2 design validation process was an in-situ radiation test, called the RadEx2 TID DEMO test. It was performed using hardware and software as similar as possible to the final RadEx2 design and a test controller simulating the satellite bus. The results of the RadEx2 TID DEMO test can be summarised as follows:

1. The ISTM test system for the RadEx2 TID DEMO test worked reliably for 3000 hours of non-stop testing.
2. As far as public data suggested, this was a first TID test of the core ADC chip ADS1263. Only minor TID-induced degradation of the ADS1263 was observed. The engineering and flight models will use the ADC chips from the same lot.
3. The current sources of the ADC chip exhibited minor TID-induced degradation. However, the RadEx2 design allows for compensation of the variation of current sources. This capability was validated during this test.
4. The RadEx2 employs four thermometers. Two of them were found practically immune to TID. The internal sensor of the ADC chip was slightly sensitive to radiation. The fourth sensor was validated to be highly sensitive and thus ideal as a test device (DUT) for the in-orbit TID testing.
5. The capability to precisely measure the dosimetry sensors (two PMOS devices) was also validated. A calibration method for the RADFET sensor was proposed and demonstrated.
6. The self-test capability of the A/D converters in the ADC chip was evaluated. The test DAC (TDAC) was found immune to radiation. Both the ADC1 and ADC2 converters were found slightly sensitive to TID. Excellent sensitivity of the ADC self-test was demonstrated.
7. Four voltage references were tested (three external and one internal to the ADC chip). An indirect “proportional” method of their measurement was demonstrated. The TID-induced degradation of the VREF devices was as expected. The analysis of the measurement of the internal VREF devices also validated the results of the ADC self-tests.
8. RadEx2 TID DEMO test also showed that supply currents of the experiment would be only slightly changed by TID. Hence the power budget of the experiment was confirmed.
9. The results of the RadEx2 TID DEMO test could also be used as a demonstration of the capability of the RadEx2 experiment to produce DAQ data that can be used for the in-orbit validation of the proposed LMMU models (see section 5.5). However, the development of the models will require statistical data from the testing of the final PCBs, which is not a part of the presented PhD (it will be performed once the engineering models of the satellites are provided by the CubeSat teams).

To conclude, RadEx2, a second generation of the in-orbit experiment has been developed, and its performance was successfully validated during the TID test. The results proved that the RadEx2 experiment could perform precise in-orbit TID testing of advanced DAQ components. The RadEx2 was presented at the iCubeSat 2017 workshop [361].

11 CONCLUSIONS

This work was focused on the development of advanced testing methods for evaluation of the impact of the total ionising dose radiation on space data acquisition systems. The long-term goal of this research is to develop ground and in-orbit radiation testing methods that would generate accurate data for various purposes. Firstly, the data can be used for modelling the impact of the TID radiation on the measurement uncertainty of space data acquisition systems. Secondly, the data from combined in-orbit and ground tests can help to improve the understanding of the validity of traditional terrestrial total ionising dose testing. Thirdly, the advanced test methods can make radiation testing affordable to the low-cost NewSpace projects by allowing greater automation of the test process.

11.1 Theoretical background of the work

This thesis contains four chapters dedicated to the theory. Three of them (chapter 2 to 4) were focused on the current theory in the field, and the fourth (chapter 5) summarised the modern trends in space technology and proposals for advanced test methods.

Chapter 2 contains a discussion of the challenges encountered while designing data acquisition systems for space missions and an overview of the process of estimating its measurement uncertainty. A summary of the theoretical background of the space radiation environment, the effects of radiation and temperature on electronic components can be found in chapter 3. The theoretical overview concluded with an outline of traditional radiation hardness assurance and testing (chapter 4).

The final theoretical section (chapter 5) gave an overview of the new era of a commercial approach to space technology (NewSpace) and its impact on the radiation hardness assurance and testing processes. A set of advanced in-situ radiation test methods was proposed to address the requirements of NewSpace and also to provide data with total dose resolution adequate for the development of models that will be used for live estimation of the measurement uncertainties of data acquisition systems during their missions. A concept of such a novel “life mission measurement uncertainty” model concluded the theoretical part of this thesis.

11.2 Development of in-situ test methods and tools

One of the key goals of the presented PhD work was to demonstrate the in-situ radiation testing and evaluate its practical limitations. The in-situ experiments required the development of a variety of special test/measurement methods and tools.

The test systems for experiments were typically based on a combination of high-precision commercial measurement instruments with custom-developed test hardware and software. The aim was to achieve high resolution and accuracy together with reliability. The requirement for the accuracy was driven by the precision of the devices under test and the research of the practical limits of the in-situ test method. Reliability was necessary in order to reduce the risk of an unscheduled interruption of testing,

which would lead to a repetition of the experiment and thus to a loss of valuable radiation testing time and samples.

A series of in-situ test controllers (ISTCs) have been developed to provide a test functionality that was not available within the affordable commercial test solutions. The ISTCs were responsible for: driving the multiplexors; digital communication with the DUTs; monitoring the radiation sources and DUT temperature; generating programmable bias voltages and simulating satellite buses. Five of the ISTC modules have been built, and their robust design led to excellent reliability (no errors were detected during more than three years of operation).

A novel method has been developed for in-situ measurement of radiation-induced changes in temperature coefficients of semiconductors (TID-TC). The need for precise and fast control of the temperature of tested devices led to the development of a DUT temperature controller (DTC). The active part of the DTC (heating/cooling module with the attached samples and temperature sensors) had to be exposed to the radiation during the experiment. To address the special requirements a completely custom solution has been developed and validated during a comprehensive test campaign. The resulting DTC system had excellent parameters (temperature range -40 to 100 °C, with stability of 0.02 °C, settling time lower than 100 s and measurement uncertainty of 0.4 °C).

The complexity of the PhD experiments led to the development of software for various platforms, including software for the Windows-based PCs, proprietary embedded test controllers (ISTCs, DTCs); COTS test instruments and Linux-based mini-computers. A modular software package called STS (Systematic Test Software) was developed using ANSI C and C++ languages. This meant that the code could be shared between various test platforms.

The developed test system (including the multipurpose STS software package) has also been used for various commercial applications. The majority of them were confidential. However, two of these commercial projects were published. The ISTC and STS technologies were successfully used for heavy ion single event effects testing of RF attenuators [362]. The STS software was also used for characterisation of REM RADFETs for a commercial research program focused on the development of alpha radiation dosimetry [363]. The intended application for this research was monitoring of process stability in the ion implantation process.

11.3 Results of PhD experiments

In general, the TID experiments were performed with the following goals:

- To demonstrate advanced in-situ test methods and evaluate their limits
- To perform novel radiation-temperature testing (TID-TC)
- To improve knowledge of response to TID of various PMOS devices that could be used for in-orbit TID measurements (dosimetry)
- To obtain high-resolution TID-induced degradation data for high-precision commercial data acquisition system components. The TID data would also be used to identify candidate DUTs for in-orbit experiments
- To design and demonstrate an advanced experiment for both terrestrial and in-orbit TID testing of components for precision data acquisition systems.

The very first TID experiment was an in-situ pilot test of digital thermometers DS18B20. It was intended to demonstrate the in-situ technology on relatively simple devices (regarding test instrumentation). The experiment proved that the STS test software and in-situ method could be used for long-term testing, and precision temperature measurements can be performed during irradiation. The experiment also showed the possibility of precise evaluation of the bias sensitivity of the TID-induced degradation (see section 3.7).

11.3.1 PMOS devices

In total three various types of PMOS devices were tested during the PMOS experiments (chapter 7): a commercial transistor ZVP1320 was tested together with two types of RADFET sensors (developed by REM and Tyndall). These experiments were designed to improve understanding of the bias dependency of the devices (especially under rather special conditions like a constant current bias), to allow comparison of the responsivity of the devices under identical conditions (both radiation and bias).

The final goal was to measure the TID-induced change of their temperature coefficients using the novel TID-TC method. The obtained TID-TC data showed a significant impact of the radiation on the temperature dependency of the TID readings of the PMOS sensors. The TID-TC results were discussed concerning the current methods of compensation of the temperature sensitivity of the RADFETs – it was demonstrated that the traditional compensation methods should be modified in order to implement the TID-induced change in the temperature coefficients (the current methods assume it is constant).

The PMOS experiments helped to identify the most suitable dosimetry sensors for the planned in-orbit experiment. The best candidates (in terms of the device-to-device variation in responsivity and linearity) were the REM and ZVP1320 devices. However, the Tyndall RADFETs offer significantly lower starting value of threshold voltage and are provided in an SMD package suitable for the limited size of the in-orbit experiment. Therefore the final candidates were the Tyndall RADFETs and ZVP1230s.

11.3.2 Voltage references

A compressive set of experiments has been performed to measure TID-induced changes of various parameters of precision voltage references. Four types of commercial VREF device were chosen to test all modern VREF technologies including bandgap, buried Zener diode and XFET. Low power and small components were used to fit the requirements of the planned in-orbit experiment.

The experiments proved that the TID could significantly change all measured parameters of the VREF devices. These included output voltage (reference voltage) and its temperature coefficient, line regulation, load regulation and supply current. The biased devices appeared to be significantly more immune to TID than the unbiased devices. This was a very important finding for the in-orbit experiment, during which the hardware will be most of the time unbiased. The majority of the devices started to suffer radiation-induced changes from the beginning of the exposure. However, the LT1236 VREF devices (buried Zener diode technology) remained practically unchanged until 10 krad(Si). Such radiation hardness makes these devices interesting candidates

for low-dose missions, such as LEO orbiting satellites. Unfortunately, the LT1236s were not suitable for the planned in-orbit experiment as their supply voltage was too high.

The TID-TC experiment was also performed with the VREF devices. An upgraded test system was developed to address the thermal hysteresis issue with static temperature sweeps - the new test system allowed for the dynamic measurement of the temperature coefficients. The upgrade included a use of an advanced 7.5 digit multimeter, fast multiplexing of the DUTs and dynamic profile of the temperature sweep provided by the DTC controller. The TID-TC results showed that all devices exhibited an initial TID-induced change of the polarity of the TC_{Vo}. In absolute figures, the low doses of radiation were, in fact, lowering the TC_{Vo}, and there was a dose at which the TC_{Vo} was practically zero. A strong bias sensitivity of the VREF devices was confirmed during the TID-TC experiment.

11.3.3 Analogue to digital converters

The final component-level TID experiment in this PhD work was designed to measure TID-induced degradation of two types of high-resolution A/D converters (ADCs). A custom-developed in-situ test system was used to perform all measurements. This solution was also chosen to allow practical demonstration of NewSpace style low-cost testing. The in-situ test system was capable of measuring static parameters (DC errors), DUT supply current and temperature. It could also record waveforms of the digital SPI bus with the DUTs in order to observe potential TID-induced degradation of both static and dynamic parameters of the bus.

Two 24-bit single-channel A/D converters were tested: LTC2400 and AD1251. The noise was the key limiting factor for high-resolution measurements/testing. Therefore the noise performance of the whole signal chain of the ADC tester and the ADCs under the test was measured in-situ in the MIF facility at two stages. These tests concluded that the effective resolution of the designed test system could reach 20 bits, if the raw ADC data is processed using oversampling and averaging, which was very close to the typical effective resolution of the LTC2400 itself.

The TID-induced degradation of the measurement errors of the ADCs were significantly different between the devices; while the LTC2400 started to degrade immediately after the start of the irradiation, the ADS1251 appeared to be immune to the radiation up to a dose of 13 krad(Si) after which it started to degrade practically constantly with the dose.

The ADC TID experiment successfully demonstrated promising capabilities of the designed in-situ test system and reliably measured TID-induced degradation of two COTS 24-bit A/D converters. However, there was not enough data to make final conclusions about the performance of the tested devices as there was only one piece of each type of ADC tested. Despite this limitation, the LTC2400 could be an interesting candidate device for in-orbit testing.

11.3.4 In-orbit experiment

The final chapter in this thesis was focused on the results of the in-orbit experiments developed for in-orbit use during the PhD program. These experiments were called RadEx (short for Radiation Experiments). Two generations of the in-orbit experiments have been developed: the RadEx1 and RadEx2. While the first experiment RadEx1 is described only briefly (due to its cancellation), the second experiment RadEx2 was discussed in detail as it fulfilled objectives of the work planned for the PhD.

The goal of the RadEx2 project was to create a miniature radiation experiment that could be launched on-board an arbitrary satellite including the modern CubeSats. The experiment was designed to perform monitoring of the mission TID level, temperature and precise measurements of degradation of a set of voltage references and the DAQ/test system itself.

Two CubeSat flight opportunities for the RadEx2 have been successfully negotiated, and the schematic of the RadEx2 was integrated with the hardware design of both satellites. An integration package was also created to ease implementation of the RadEx2 with potential future missions.

A comprehensive test plan for the RadEx2 was defined, and it had three stages. The first stage was completed as a part of the presented PhD research, and it was focused on a validation of the design of the experiment and demonstration of its functionality (both regarding the performance of the DAQ hardware and its response to radiation). Prototype hardware of the RadEx2 was built and used as a demonstrator and as a platform for the development of the software library. This software package will be used for ground testing of the experiment and for integration with the satellites.

The second part of the RadEx2 design validation process was an in-situ radiation test, called RadEx2 TID DEMO test. It was performed using hardware and software as similar as possible to the final RadEx2 design and a test controller simulating the satellite bus. The results of the RadEx2 TID DEMO test were discussed in detail in section 10.6 and proved that the RadEx2 experiment could fulfil all planned in-orbit test and measurement tasks. The space segments of the experiments are expected to be launched on-board two CubeSat missions in the 2020's.

11.3.5 Performance of the in-site test method

The results of the various PhD experiments demonstrated that the in-situ test technique can be used even for high-precision measurements of components for advanced high-resolution data acquisition systems.

The reported TID experiments were executed in the MIF facility, which required fifteen-meter cables to interconnect the test instrumentation with the hardware placed inside the irradiation cell. Despite this constraint and a limited budget for the hardware of the test systems, very low noise measurements could be realised.

The initial measurements of the VREF devices showed noise/repeatability better than ±10 µV (±1 ppm at the 10 V measurement range). Also, the data from the ADC tests showed similar results that could be interpreted as 20-bit effective resolution, and RadEx2 had even better results. The repeatability of the measurements of the temperature coefficient was also excellent: it was within ±50 ppb/°C.

11.4 Publications

The presented results of the PhD research were published in various papers and orally presented at workshops and conferences. These results were primarily reported regarding space applications. However, they are also applicable to other fields dealing with the challenges of the radiation effect in electronics. These included high-energy physics, nuclear power research, and medical applications.

The in-situ pilot test of the digital thermometers was presented at the RADECS 2011 conference [125]. The in-situ test method was discussed in a paper which was published at the NSREC 2012 conference [241]. The testing strategy of the early version of the in-orbit experiment (RadEx1) was accepted for a poster presentation at RADECS 2012 [350]. TID testing of the power system for the RadEx1 experiment was presented in an NSREC 2013 paper [351]. The second paper of the 2013 season was dedicated to radiation test of the TEC module for the DUT temperature controller [314]. The TID-TC method was demonstrated on the PMOS transistors. The early results of this experiment were presented at the NSREC 2015 conference, and an extended paper was published in the IEEE-TNS journal [324]. The experimental work continued with testing of the COTS voltage reference devices, which was published at RADECS 2016 conference [335]. A second IEEE-TNS journal paper was published in 2017, and it summarised the results of the TID-TC testing of RADFETs [329]. The final paper, dedicated to the TID-TC experiment with the COTS voltage references, was presented at RADECS 2017 [338]. The early results of the ADC experiment were orally presented at the RADFAC 2017 conference. The 6th Interplanetary CubeSat Workshop (iCubeSat 2017) accepted a talk given on the in-orbit testing experiments [361].

11.5 Future work

The presented PhD research program accomplished its goals. It has been demonstrated, that the TID-induced degradation of commercial DAQ components is a serious problem and that it can be tested with excellent accuracy of measurement and dose resolution by the use of the in-situ technology.

The research program is expected to continue with further development of the test methods and tools, as well as design and execution of advanced experiments. The most important event will be the final ground radiation testing and launch of the RadEx2 experiment. The long-term goal is to obtain two sets of test data: the results of the ground tests and the data from the in-orbit testing. The comparison analysis will show the limitations of the ground TID testing and the true impact of space radiation on the performance of advanced DAQ electronics based on commercial (COTS) components. The data will also be used for the development of the live mission measurement uncertainty (LMMU) models.

The results of this research programme will support the development of future scientific spacecraft. It is also believed, that NewSpace technology has the potential to perform research missions with scientific capabilities comparable to large missions such as the SORCE [364]. The developed of fully-automated test methods can help to provide affordable radiation hardness assurance for these low-cost missions.

11.5.1 Advanced test methods

The development of automated TID testing methods is planned to continue following these principal topics:

1. More automated and standardised development to shorten the development time and make the testing more affordable. The automation would be also beneficial to the data analysis stages of the experiments.
2. Further improvement (lowering) of the measurement uncertainty on the hardware level by applying better instrumentation, increasing the signal-noise ratio (better shielding, cables, filtering).
3. Use of advanced data processing methods in the STS software such as digital filter algorithms
4. Development of the dynamic dose rate testing as proposed in this work
5. Further development of the TID-TC test method:
    a. testing at different idle temperatures to evaluate the impact of the irradiation temperature on the results of the TID-TC test
    b. analysis of the impact of the TID-TC testing on the overall TID-induced changes to the devices (by speeding up the temperature profile, changing the shape of it)
    c. TID-TC testing at ultra-low temperatures to suppress concurrent thermal annealing effect
6. Research of advanced combined (synergetic) effects, such as:
    a. impact of the mechanical stress on the accuracy of DAQ devices
    b. the synergy of the mechanical stress with TID effects
    c. mechanical stress of the devices during the TID-TC testing (this could be tested by comparing results of temperature cycling performed using devices glued to the TEC (standard DTC system) and standalone devices exposed to temperature cycling in a thermal chamber)
    d. long-term stability (ageing) versus the burn-in process (DTC system can be used for various burn-in experiments)
    e. burn-in versus TID-induced changes (impact of the burn-in process on the response to TID)
    f. temperature dependence of ageing

11.5.2 Next generation test tools

The modular design of the STS software package appeared to be a very effective concept allowing rapid development of the test scripts and other tools for development of the experiments. The STS code could be implemented on various platforms due to the strict usage of ANSI C code (C++ was used only for user interfaces). However, the future experiments will require more advanced programming languages such as Python and also the integration of the STS with advanced mathematical tools such as Matlab/Simulink and Octave. Therefore next generation of the STS package will use multi-language codes and platforms. This approach will allow the development of advanced data analysis tools and more effective test scripts.

The long-term execution of the ISTC test controllers proved them to be a reliable platform for operating several custom-built test modules. The future ISTC family could

be developed to be compatible with the modern test script processor (TSP) technology, which allows the instruments to run their own embedded test scripts and thus dramatically increase the speed of testing. Thus the next generation ISTCs could be communicating via Keithley TSP bus and be controlled directly by the test instruments.

The DTC temperature controller demonstrated its capabilities during a series of successful novel TID-TC experiments. However, the current DTC can be significantly improved by applying more advanced technologies as follows:

1. The stability of the DUT temperature can be improved by using a new generation of ADCs, such as ADS1263 (core ADC chip in the RadEx2), and finer control of the TEC power. The TEC power is currently controlled by the TDM module, which can be extended by a secondary fine-resolution bipolar current source that would improve the control of the TEC and suppress the latency of the polarity switching relays.
2. The MU of the DTC system can be dramatically lowered by a direct calibration of the temperature measurement. The DTC cabling would have to be modified so it could be removed from the hermetic DUT container and placed in the thermal chamber in the calibration facility.
3. The reference resistor in the DUT temperature measurement block can be upgraded using the resistors from the RadEx2 design.
4. The temperature sensor (PRT) in the current DTC design can also be replaced by a more precise type; it would have to be a custom-designed type
5. The statistical analysis of the DTC data showed a minor offset in the data that indicated that the PID controller could also be optimised.
6. The current version of the TDM module uses linear control of the TEC power. A future research project can identify potential switched solutions with acceptable EMI.
7. Future DTC systems can use TECs with more than two stages to achieve lower DUT temperatures. The market research showed that the three stages TECs were available only for the very small surface of the cold side. Hence, these TECs would only accommodate a few DUTs (only one IC). A multichannel DTC would have to be used to control these individual TEC assemblies. The advantage of this concept would be the individual control of the temperature of each DUT.
8. The cooling of the hot side of the TEC could also be significantly optimised by employing a water cooling system. The early DTC tests demonstrated that the DUTs could be cooled down to -60 °C with the current type of TEC and powerful water cooling of the hot side.
9. The TEC assembly can be redesigned to employ a DUT mounting method that would allow easy removal of devices (DUTs are glued to the TEC in the current concept of the TEC assembly).

11.5.3 PMOS devices

One of the very interesting results of the PMOS experiments was the finding that the commercial PMOS transistors could be used as a low-cost alternative to the RADFET sensors. The future experiments can provide more data of the responsivity of these

cheap devices. It is important to obtain data from a large number of devices, ideally a few tens of samples from various production lots. That would dramatically improve the understanding of the accuracy of a dosimetry system based on these devices. Another important aspect is the dose rate sensitivity of these devices. It would be ideal to employ the dynamic dose rate test method to measure the dose rate sensitivity free of potential errors due to device-to-device variations.

The future research can also use the DTC system to perform a TID experiment that would measure the effectiveness of temperature compensation techniques in-situ during irradiation of the PMOS dosimeters. This system-level TID experiment would perform temperature sweeps of the entire hardware of the dosimeter circuit, during the irradiation.

11.5.4 Voltage references

The measurements of the four types of COTS voltage references showed a very high sensitivity to the TID. The aim of future VREF experiments could be to measure the broader spectrum of available COTS voltage references to identify other TID-immune types (so far only the LTZ1000 was identified as a radiation-hardened commercial voltage reference). The future TID experiments could also measure TID-induced changes in the noise of various types of VREF devices.

The TID-TC experiments of the VREF devices can be extended by various advanced features including:

1. Testing and comparison of various grades of devices. The presented TID-TC experiment was performed using low-grade devices. The high-grade devices will have significantly lower initial TC_{Vo}. The research goal is to find out if the high-grade devices also suffer lower TID-induced change of the TC_{Vo}, or if the only difference is in the initial value of the TC_{Vo}.
2. Testing of a larger number of DUTs. The presented TID-TC experiment could test only one piece of each type of DUT.
3. Investigation of the impact of the temperature profile of the measured TC_{Vo} and thermal hysteresis of the output voltage.
4. TID-TC measurement of other parameters (line and load regulation, noise, supply current)
5. Dose rate sensitivity of the TID-induced changes of the TC_{Vo}.

11.5.5 A/D converters

The interpretation of the results of the reported ADC experiment was limited due to the number of tested samples (there was only one piece of each type of ADC tested). Hence, a future ADC experiment should be designed in order to test multiple DUTs. The obvious challenge of such a multichannel test setup is the multiplexing of the DUT stimuli.

The noise analysis performed during the processing of the results of the ADC experiment was found to be very useful and will be extended in future experiments. The next generation of the STS package can be upgraded by advanced data analysis tools to support the noise analyses.

The ADC tester used in the PhD experiment was based on DC testing techniques and employed 16-bit test DAC converter (TADC). The future experiments can be significantly improved by the following options:

1. The TDAC can be upgraded to a higher-resolution type. One candidate could be a 20-bit DAC device AD5791 developed by Analog Devices [365]. This DAC offers outstanding *INL* of 1 ppm.
2. The voltage reference source and buffers can also be significantly improved. The LTZ1000 VREF devices could be used.
3. Furthermore, the sensitive parts of the ADC tester circuitry can be placed in a thermally stabilised environment. The ISCT mini-oven was designed and validated to provide a stable ambient temperature within a window of ±0.2 °C and therefore would be an ideal platform (see section 6.5.9).
4. The next generation of ADC experiment could also perform the TID-TC testing of the ADCs.
5. The ADC testing could also be performed using a dynamic method, which would require an ultra-low noise AC generator. Development of such advanced instrumentation could be a subject of future research.

11.5.6 RadEx experiments

The future work on the family of RadEx in-orbit experiments will include the following activities:

1. The testing and validation RadEx2 will continue as defined in the plan in section 10.5. The key events will be the TID testing of multiple pieces of the engineering models of the satellite's PCB with the RadEx2 hardware and the final testing of the flight models prior to launch.
2. The in-orbit operation of the RadEx2 experiments
3. Detailed SPENVIS/OMERE simulations of the mission dose will be performed using final orbit data and 3-D models of the satellites' mechanical structure. The goal is to obtain precise data that could be used to validate the calibration of the RadEx2 dosimetry system.
4. The dosimetry data will be processed to compensate for the TID-induced changes of the TC_{VT}.
5. The data analysis will be performed to include comparisons of terrestrial and in-orbit results.
6. The development of the LMMU models based on the terrestrial testing as well as in-orbit testing.

While these activities are in progress, other CubeSat/nanosat teams will be contacted, with the goal of arranging more RadEx2 flights. The RadEx2 integration package should make collaboration with any new team(s) an uncomplicated process.

The development of the next generation of RadEx experiments will also be a continuous process. The next generation experiment could, for example, be an extended version of the RadEx2 with the following added functionality:

- The dosimetry system extended by adding more PMOS sensors and by adding another (ideally independent) dosimetry method. The OSL sensor might be one of the candidates.

- The set of DUTs extended to contain more devices, including ADCs (LTC2400 seems to be a preliminary candidate)
- There could also be more types of digital thermometers
- The RadEx could also be used to monitor TID-induced changes of electronics of the other payloads by its measuring the signals from sensors and comparing them with the results with the DAQ systems of the payload.
- The monitoring of individual DUT supply currents (this is very interesting because the PhD experiments showed that the TID-induced changes of the DUTs often had trends similar to their supply currents).

11.5.7 Development of the LMMU models

The concept of the LMMU model, introduced in this thesis, was a first attempt to create a model that could provide a continuous “live” estimation of the impact of the environment on the measurement uncertainty of a precision data acquisition system in space. It was based on the following assumptions (simplifications):

- The TID-induced changes of the DAQ devices is a monotonic process (there is no significant annealing during the mission)
- There is no correction for the dose rate effects
- There are no other impacts on the DAQ system such as power supply rejection ratio, mechanical stress
- The SEM data are assumed to be perfect (there is no calculation of the measurement uncertainty of the SEM readings)
- The LMMU blocks use cumulated values of temperature/radiation data instead of true life data. Therefore, the dynamic effects are ignored (such as solar flares).
- The internal blocks of the LMMU model are assumed to be independent (there is no correlation between them)

Future versions of the LMMU could attempt to address the problems listed above. However, the first versions will be developed using the data from the TID tests of the engineering models of the RadEx2 and the satellite hardware. It is expected that the development of the LMMU models will be a continuous research programme that will continue even after the end of the space missions (the results of the models will be calculated only during the ground processing of the in-orbit data. Therefore the LMMU models can be modified as many times as necessary).

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LIST OF ACRONYMS

AAPS	Advanced Avionics and Processor Systems
AC	Alternating Current
ADC	Analogue to Digital Converter
ADCS	Attitude Determination and Control Subsystem
AGE	Ageing effects block of LMMU model
AIT	Austrian Institute of Technology
ANSI	American National Standards Institute
API	Application Programming Interface
APWR	Analogue power line (RadEx2 experiment)
ASIC	Application Specific Integrated Circuit
ASTM	American Society for Testing and Materials
ATE	Automated Test Equipment
AVT	Average Temperature (LMMU model)
AWG	Arbitrary Waveform Generator
BGR	Bandgap Voltage Reference
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistors
BOM	Bill Of Material
BZR	Buried-Zener diode Voltage Reference
CCD	Charge-Coupled Device
CERN	European Organization for Nuclear Research
CLK	Clock
CME	Coronal Mass Ejection
CMOS	Complementary Metal Oxide Semiconductor
CNES	National Centre for Space Studies (French space agency)
Co-60	Cobalt-60 source
COTS	Commercial-Off-The-Shelf component
CPU	Central Processing Unit
Cs-137	Caesium-137 source
CTE	Current Temperature (LMMU model)
CTF	Current Transfer Ratio (optocouplers)
DAC	Digital to Analog Converter
DAQ	Data Acquisition
DC	Direct Current
DD	Displacement Damage
DDD	Displacement Damage Defect
DMM	Digital Multimeter
DNL	Differential nonlinearity
DOS	Dosimeter experiment (NASDA missions)
DPWR	Digital power line (RadEx2 experiment)
DSI	Dual-Slope Integrating analogue to digital converter
DSO	Digital Storage Oscilloscope

DTC	DUT Temperature Controller
DUT	Device Under Test
DVS	Dose Verification System (an implantable dosimeter for radiation therapy)
ELDRS	Enhanced Low Dose Rate Sensitivity
EM	Engineering Model (spacecraft)
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ERM	Engineering Radiation Monitor (Van Allen Probes mission)
ESA	European Space Agency
ESD	Electro-Static Discharge
ESTEC	European Space Research and Technology Centre (ESA facility)
FEES	Flexible Experimental Embedded Satellite
FET	Field-Effect Transistor
FFT	Fast Fourier Transform
FGDOS	Floating Gate Dosimeter
FG-MOSFET	Floating Gate Metal Oxide Semiconductor Field-Effect Transistor
FM	Flight Model (spacecraft)
FPGA	Field Programmable Gate Array
G4MRES	Geant4 for Mission Radiation Effects Simulation
G4MRES	Geant4 for Mission Radiation Effects Simulation
GCR	Galactic Cosmic Rays
GEO	Geostationary Earth Orbit
GND	Ground potential
GNSS	Global Navigation Satellite System
GPIB	General Purpose Interface Bus
GRC	Glenn Research Centre
GSN	Goal Structuring Notations
GSN	Goal Structuring Notations
GUM	Guide to the Expression of Uncertainty in Measurement
HDR	High Dose Rate
HL-LHC	High-Luminosity Large Hadron Collider
HZE	High atomic number, high energy (ions)
IC	Integrated Circuit
ICD	Interface Control Document
IDAC	Current D/A converter (RadEx2 experiment)
IDE	Integrated Development Environment (software development package)
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral nonlinearity
IOT	In-orbit Testing
IP	Intellectual Property
ISS	International Space Station
ISTC	In-situ Test Controller
ISTM	In-situ Test Method

ISTS	In-situ Test System
ITRS	International Technology Roadmap for Semiconductors
JFET	Junction Field Effect Transistor
JPL	Jet Propulsion Laboratory
JUICE	Jupiter Icy Moons Explorer
JWST	James Webb Space Telescope
LDR	Low Dose Rate
LED	Light Emitting Diode
LEO	Low Earth Orbit
LET	Linear Energy Transfer
LHC	Large Hadron Collider
LINAC	Linear Accelerator
LMMU	Life Mission Measurement Uncertainty model
LSB	Least Significant Bit
LSI	Large-Scale Integration
Lua	Lightweight, multi-paradigm programming language
LXI	LAN eXtensions for Instrumentation
MBU	Multiple-Bit Upset
MCU	Microcontroller Unit
MDR	Medium Dose Rate
MET	Mission Elapsed Time (LMMU model)
MI	Measurement International Limited
MICROWIRE	Serial 3-wire interface standard
MIF	MRC Irradiation Facility
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MPE	Maximum Permissible Error
MPPL	Maximum Power Point Load
MPTB	Microelectronics and Photonics Testbed
MRC	Medical Research Council
MTC	Minimum Temperature Coefficient
MU	Measurement Uncertainty
MUX	Multiplexer
N/A	Not available or applicable
NASA	National Aeronautics and Space Administration
NASDA	National Space Development Agency of Japan
NIEL	Nonionizing Energy Loss
NMOS	N-type Metal Oxide Semiconductor logic
NPLC	Number of Power Line Cycles
NPN	Bipolar transistor with P-doped base
NSREC	Nuclear and Space Radiation Effects Conference
NXP	Next eXPerience, a new brand of Philips Semiconductors
OCI	Optocoupler Isolator
OCXO	Oven-Controlled Crystal Oscillator

OPA	Operational Amplifier
OSL	Optically Stimulated Luminescence
OWB	One-Wire Bus (digital bus for sensors)
OWT	One-Wire Thermometer
PCB	Printed Circuit Board
PETS	Pre-irradiation Elevated Temperature Stress
PGA	Programmable Gain Amplifier
PI	Proportional-Integral (type of controller)
PID	Proportional-Integral-Derivative (type of controller)
PIE	Post-Irradiation Effect
PLL	Phase-Locked Loop
PMOS	P-channel Metal Oxide Semiconductor transistor
PNP	Bipolar transistor with N-type base
POR	Power On Reset
PRT	Platinum Resistance Thermometer
PSRR	Power-Supply Rejection Ratio
PTM	Power and Temperature Monitor (ADC tester)
PWM	Pulse Width Modulator
PWR	Power
QM	Qualification Model (spacecraft)
R2IP	RadEx2 integration package
RADECS	Conference on Radiation Effects on Components and Systems
RadEx	Radiation Experiment (in-orbit)
RADFAC	RADECS thematic conference
RADFET	Radiation-sensitive Field Effect Transistor
RDCH	RadEx2 DAQ channel
RHA	Radiation Hardness Assurance
RHDRS	Reduced High Dose Rate Sensitivity
RILC	Radiation-Induced Leakage Current
RMS	Root Mean Square
RPI	Raspberry Pi
RPS	Relativistic Proton Spectrometer (Van Allen Probes mission)
RS-232	Standard for serial communication/transmission of data
RT	Room Temperature
RTG	Radioisotope Thermoelectric Generator
S/C	Spacecraft
SAA	South Atlantic Anomaly
SAR	Successive Approximation Register analogue to digital converter
SBIAS	Sensor bias generator (RadEx2 experiment)
SBT	Standard Bench Test (TID test)
SCADA	Supervisory Control And Data Acquisition
SCAL	Self-Calibration
SDR	Software Defined Radio
SDRT	Switching Dose Rate Test

SEB	Single Event Burnout
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-Up
SEM	Space Environmental Monitor
SEP	Solar Energetic Particle
SET	Single Event Transient
SEU	Single Event Upset
SEVR	Series Voltage Reference
SF	Solar Flare
SHDRS	Suppressed High Dose Rate Sensitivity
SHVR	Shunt Voltage Reference
SITMP	Information Technologies Management of the Pilsen City
SMU	Source Measure Unit
SOC	System On Chip
SpaceX	Space Exploration Technologies Corporation
SPENVIS	SPace ENVironment Information System (ESA)
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSO	Sun-synchronous Orbit
SSTL	Surrey Satellite Technology Ltd
STS	Systematic Test Software
TC	Temperature Coefficient
TCE	Temperature sensitivity (dependence) block od LMMU model
TDAC	Test Digital to Analogue Converter
TDE	Time-Dependent Effect
TDE	Total Dose Experiment (KITSAT-1 payload)
TDM	Technology Demonstration Module (PROBA-II payload)
TDM	TEC power Drive Module
TDRE	True Dose Rate Effect
TEC	Thermoelectric Cooler
TEH	Temperature History (LMMU model)
TID	Total Ionising Dose
TIDE	TID radiation effects block of LMMU model
TLA	Three-Letter Acronym
TLYF	Test like You Fly
TNS	Transactions on Nuclear Science (IEEE journal)
TS	Test step
TSP	Test Script Processor
USB	Universal Serial Bus
UUT	Unit Under Test
VDMOSFET	Vertical Double Diffused Metal Oxide Semiconductor Field-Effect Transistor

VIM	International Vocabulary of Metrology
VISA	Virtual Instrument Software Architecture
VREF	Voltage Reference
VREFI	Internal VREF source of the ADC chip (RadEx2 experiment)
XFET	eXtra implantation junction Field Effect Transistor (voltage reference)
ZTC	Zero Temperature Coefficient
ΔΣ	Delta-Sigma analogue to digital converter

LIST OF SYMBOLS

μ	Carrier mobility
μ_i	Mobility from ionised impurities
μ_l	Temperature dependence of the mobility from interaction with acoustic phonon
μ_n	Electron mobility
A	Softness factor of the R·A·D model
A	Material constant
A_i	Conversion coefficients used to convert the Type B contributor to the physical property
C_2	Diode voltage model constant
C_3	Diode voltage model constant
cl	Cable length (dosimetry system)
C_{ox}	Oxide capacitance per unit area
D	Dose in the R·A·D model
d	Distance
DNL	Differential Non-Linearity (ADC testing)
dr	Dose rate
dr_0	Dose rate at the radiation source
dT	Temperature difference - cooling capability of TEC module
E	Energy
E_C	Conduction band energy level
E_F	Fermi energy level
E_g	Energy bandgap
E_{g0}	Energy bandgap at absolute zero temperature
e_i	Error source
E_{OX}	Electric field in oxide
E_V	Valence band energy level
FS	Full-scale voltage (ADC testing)
G_{id}	Ideal gain (ADC testing)
G_m	Measured gain (ADC testing)
h_{FE}	Common-emitter current gain of bipolar transistors
h_{FE0}	Current gain before irradiation
I_0	Reverse saturation current
I_B	Base current
I_B	Input bias current
I_C	Collector current
I_D	Drain current
I_{IH}	Input leakage current high
INL	Integral non-linearity (ADC testing)
I_{OS}	Input offset current
I_s	Saturation current in the forward-active region

I_{sub}	Subthreshold leakage current
k	Boltzmann constant
k	Coverage factor (measurement uncertainty)
k_{TP}	Air-density correction factor (dosimetry system)
L	Channel length
m^*	Effective mass
m_c	Conductivity effective mass
n	Electron density
n	Number of samples
N	Resolution of the ADC
N_C	Density of states in the conduction band
N_{ef}	Effective resolution of the ADC
n_h	Density of free holes
N_I	Ionised impurity density
N_V	Density of states in the valence band
p	Hole density
P	Air pressure (dosimetry system)
P_0	Reference air pressure (dosimetry system)
q	Electronic charge
Q	Nominal width of code bins (ADC testing)
R	Characteristic parameters of the R·A·D model
r	Responsivity of TID detectors
R^2	Coefficient of determination of linear regression
s	Standard deviation
s_{RMS}	RMS value of the noise of the ADC
T	Temperature
T_0	Reference air temperature (dosimetry system)
T_A	Ambient Temperature
T_C	Temperature of the cold side of the TEC
TC_{IB}	Temperature coefficient of the input bias current
TC_{TEC}	Temperature dependence of the thermoelectric cooler
TC_{Vo}	Temperature drift of voltage references
TC_{VOERR}	Measurement error induced by the temperature drift of the VREF device
TC_{VT}	Temperature coefficient of threshold voltage
T_H	Temperature of the hot side of the TEC
T_{id}	Ideal input transit voltage (ADC testing)
T_m	Measured input transit voltage (ADC testing)
T_{max}	Maximum temperature (voltage reference temperature drift)
T_{min}	Minimum temperature (voltage reference temperature drift)
t_{ox}	Thickness of the oxide
u_B	Type B measurement uncertainty

u_{eB}	Type B measurement uncertainty contributor
u_{eBLM}	Life Mission Type B measurement uncertainty contributor (output of the LMMU model)
u_x	Combined standard measurement uncertainty
U_x	Extended measurement uncertainty
u_{xA}	Type A measurement uncertainty
V_{BE}	Base-emitter voltage
V_{CE}	Collector-emitter voltage
V_{DD}	Drain supply voltage
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
V_I	Irradiation voltage
V_{LDRERR}	Measurement error induced by the load regulation of the VREF device
V_{LNRERR}	Measurement error induced by the line regulation of the VREF device
V_{max}	Output voltage measured at maximum temperature (voltage reference temperature drift)
V_{max}	Maximum input voltage (ADC testing)
V_{min}	Output voltage measured at minimum temperature (voltage reference temperature drift)
V_{min}	Minimum input voltage (ADC testing)
V_{nom}	Nominal output voltage (voltage reference temperature drift)
V_{OERR}	Initial accuracy of voltage references
V_T	Threshold voltage
V_{T0}	Pre-irradiation threshold voltage
W	Channel width
W_m	Measured width of code bin (ADC testing)
x_i	Measured samples
Z	Atomic number
α_{it}	Interface trapped charge constant for Stojadinovič model
α_{ot}	Oxide trapped charge constant for Stojadinovič model
β	Common-emitter current gain of bipolar transistors
γ	Body effect parameter
$\Delta(1/h_{FE})$	Gain damage figure
ΔN_{it}	TID-induced change in density of interface trapped charge
ΔN_{ot}	TID-induced areal density of deep trapped holes near the oxide/silicon interface
ΔN_{ot}	TID-induced change in density of oxide trapped charge
ΔQ_{it}	TID-induced interface trapped charge
ΔTC_{IB}	TID-induced change of the temperature coefficient of the input bias current
ΔV_{FT}	TID-induced shift in the flatband voltage
ΔV_{it}	Contribution from the charged interface traps
ΔV_O	TID-induced shift of the output voltage (voltage reference)
ΔV_{OERR}	Measurement error induced by the TID-induced shift in VREF output voltage

ΔV_{ot}	Contribution of deep trapped holes near the interface
ΔV_{st}	Short-term contribution from the TID-generated mobile holes transporting in the oxide bulk
ΔV_T	TID-induced threshold voltage shift
ε_G	ADC gain error
ε_{os}	ADC offset error
ε_{ox}	Dielectric constant
ϕ_F	Fermi energy
ϕ_{GS}	Gate-substrate contact potential
χ	Converting coefficient of a distribution function

LIST OF UNITS

°C	Degree Celsius, unit of temperature
A	Ampere, unit of electric current
Å	Ångström, unit of length equal to 1E−10 m
C	Coulomb, unit of electrical charge
eV	Electronvolt, unit of energy
F	Farad, unit of capacitance
g	Gram, unit of mass
Gy	gray, SI derived unit of absorbed radiation
hr	Hour, unit of time
Hz	Hertz, unit of frequency
J	joule, unit of energy
K	Kelvin, unit of thermodynamic temperature
LSB	Least-significant bit, used for ADC testing
m	Meter, unit of length
Pa	Pascal, unit of pressure
ppb	Part Per Billion, notation of ratio
ppm	Part Per Million, notation of ratio
rad	radiation absorbed dose
s	Seconds, unit of time
SPS	Sample per second, unit of sampling rate
V	Volt, unit of electric voltage
VAC	Volt, Alternating Current, unit of voltage
VDC	Volt, Direct Current, unit of voltage

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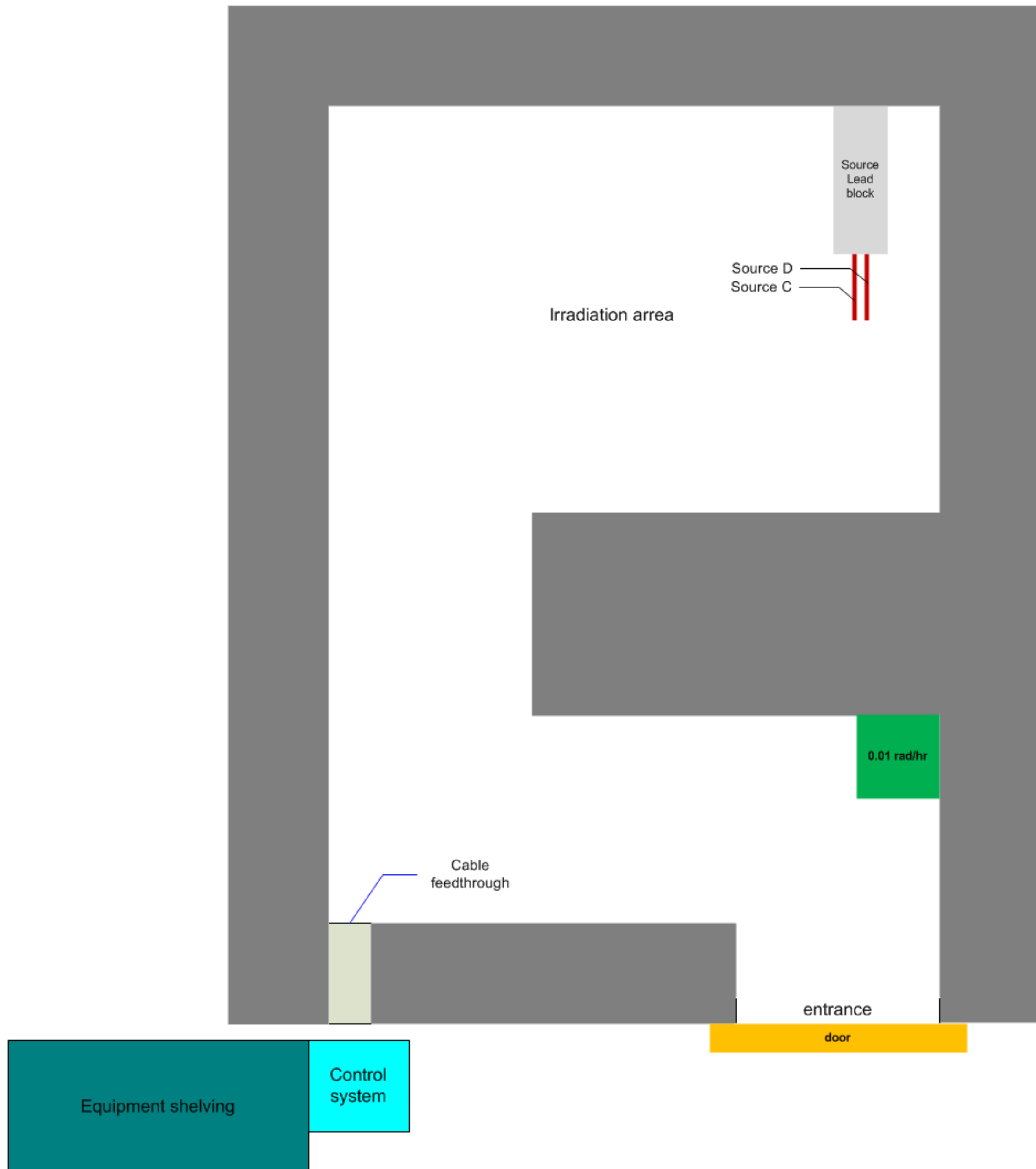
A MRC IRRADIATION FACILITY

A.1 The layout of MRC irradiation facility

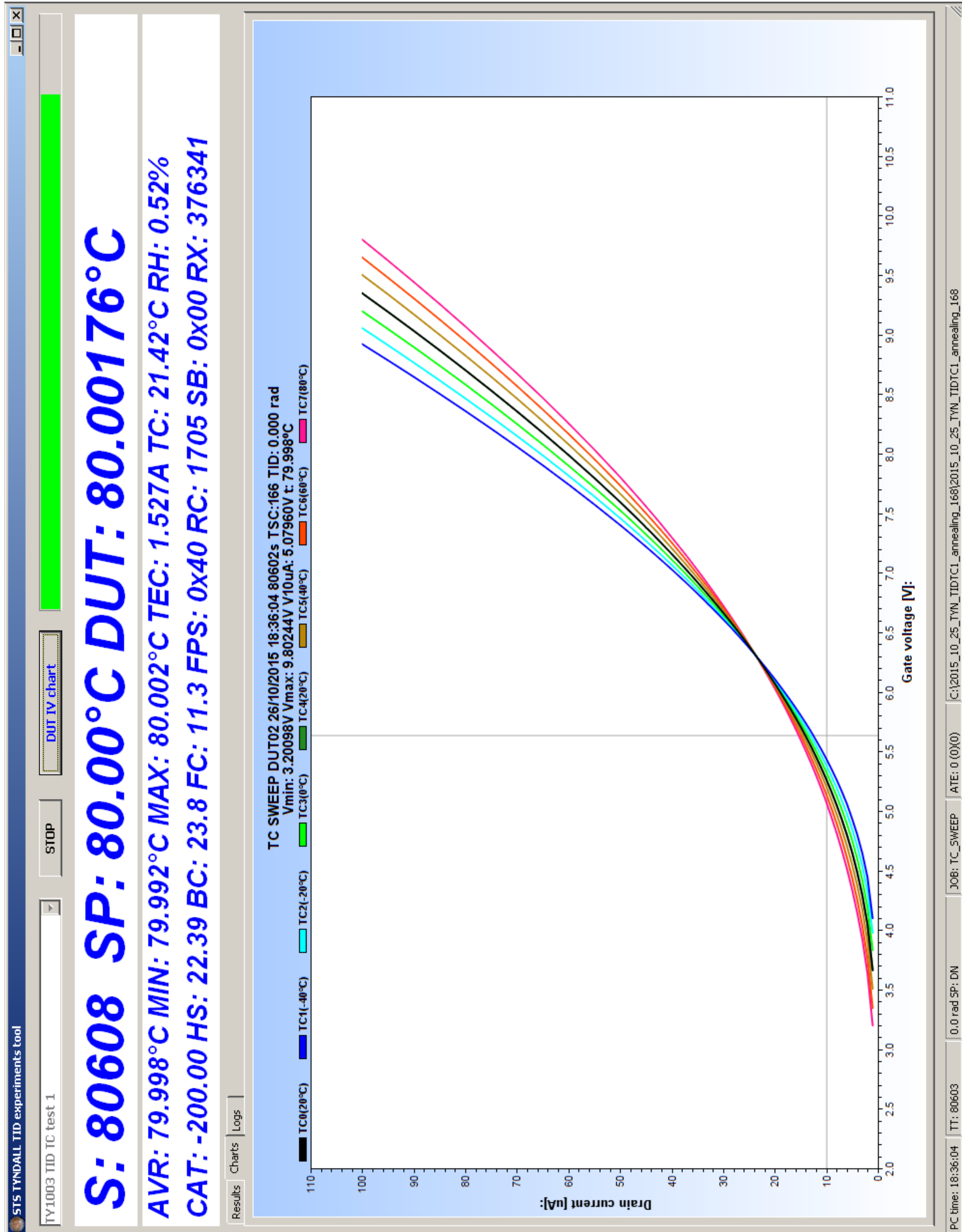


A.2 MIF test equipment racks during experiments

Legend: (1) ISTC1/DTC controllers, (2) ISTC2 controller, (3) Test master PCs, (4) Programmable power supplies, (5) Fixed voltage power supplies, (6) Digital multimeters, (7) DMM7510 MUX unit, (8) TDM module, (9) SMU 2420 and (10) UPS.

B STS SOFTWARE

B.1 STS user interface during a TID-TC experiment

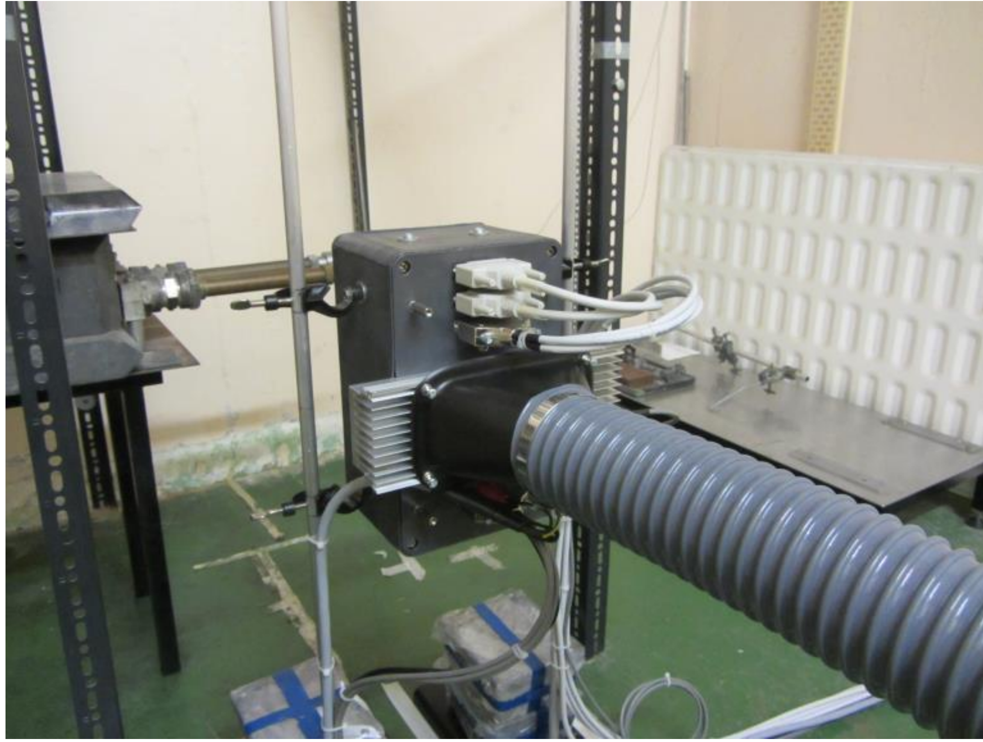


C TEST EQUIPMENT

C.1 Interior of the ISTC3 controller

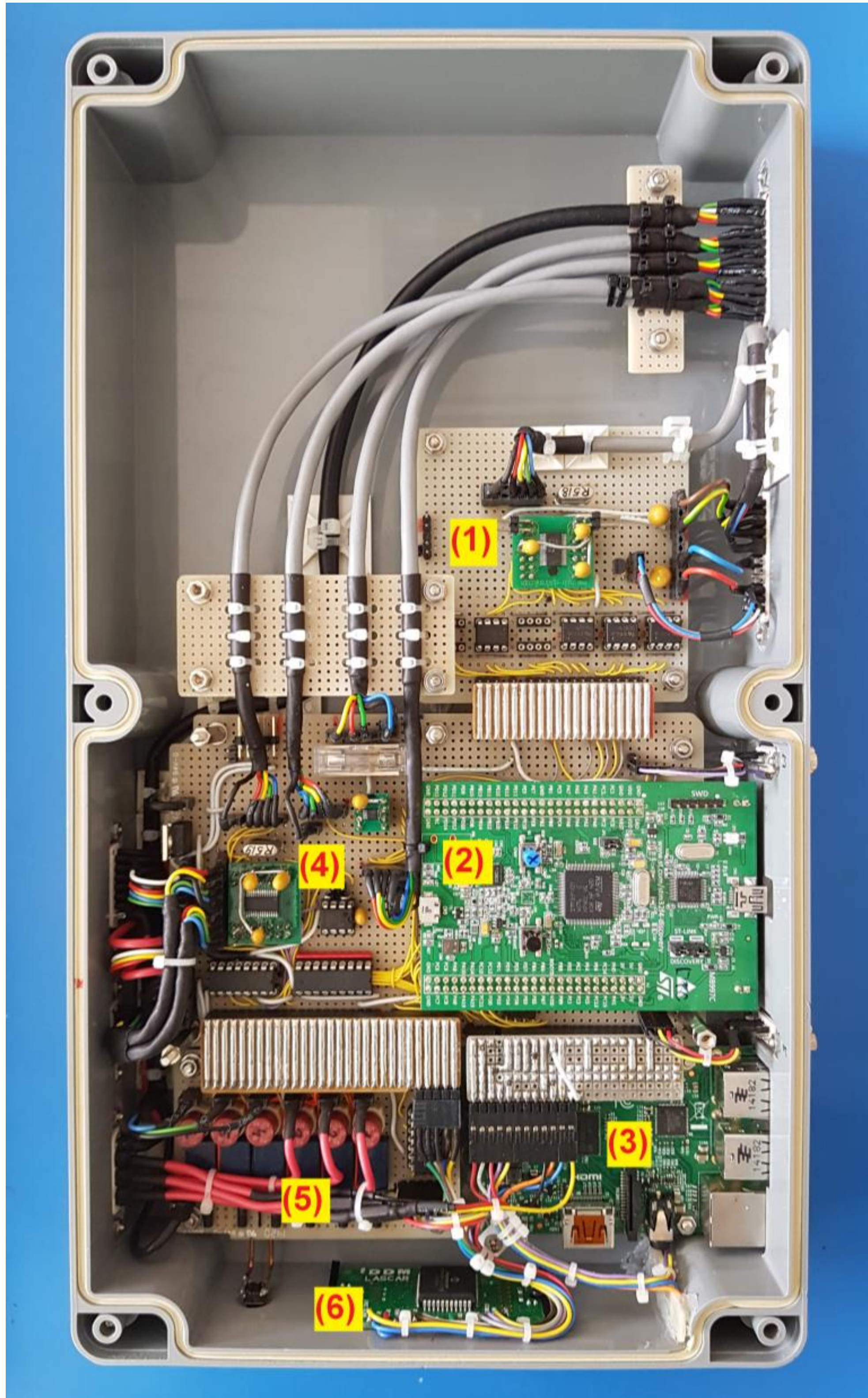
Legend: (1) the MCU board stack, (2) relay driver module, (3) touchscreen display for debugging, (4) USB memory stick interface, (5) DUT interface board (custom hardware for a particular experiment).

C.2 Irradiation container with DTC in the MIF cell



C.3 DTC blower in the MIF ultra-low radiation area

C.4 DTC control module hardware

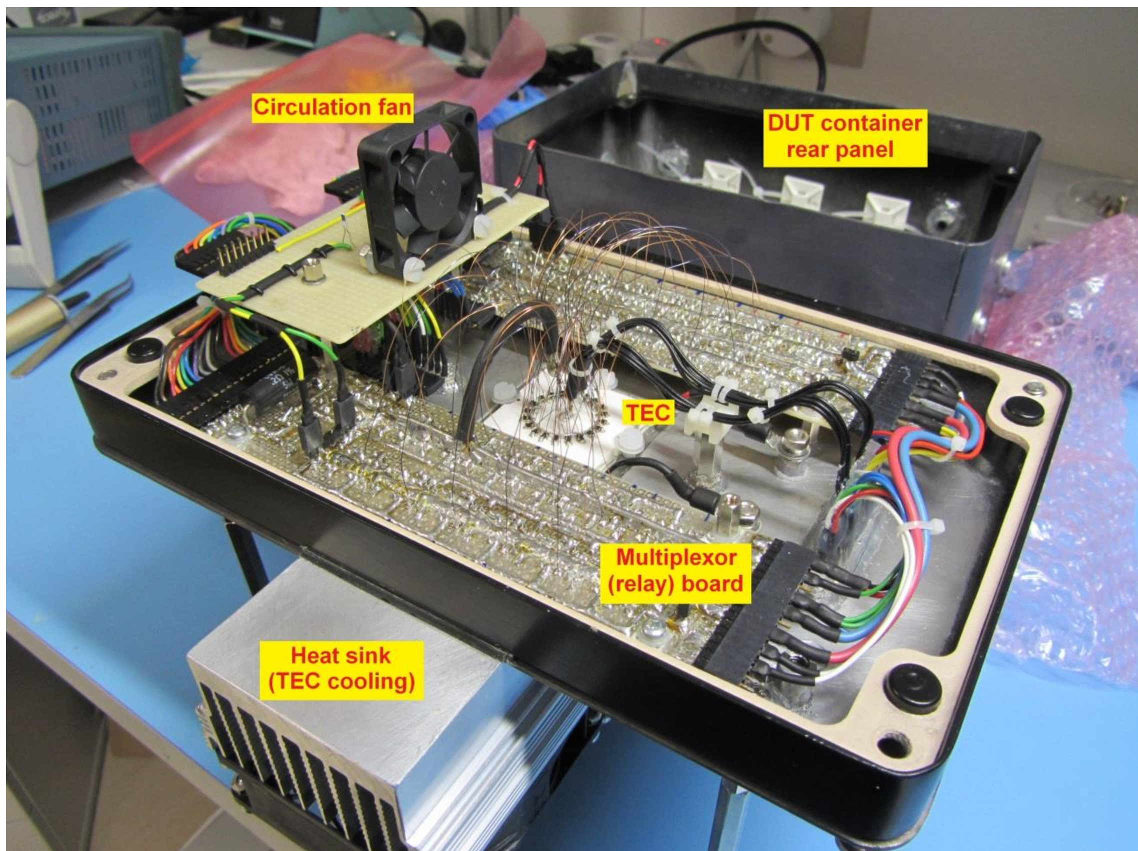


Legend: (1) DUT temperature measurement, (2) MCU board, (3) RPI/REX module, (4) monitoring/protection board, (5) fans/blower protection, (6) LCD and buttons

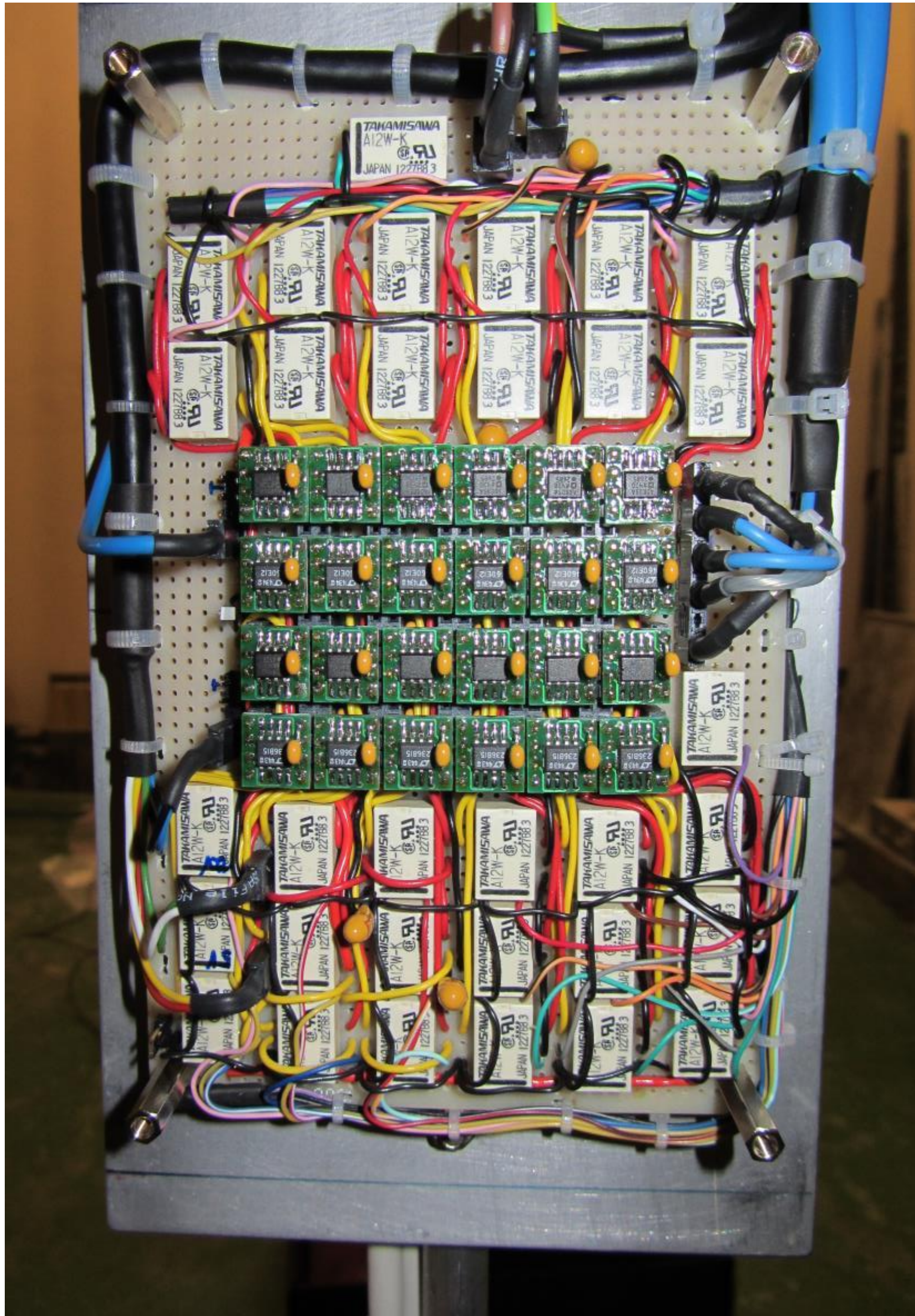
D EXPERIMENTAL HARDWARE

D.1 PMOS DUTs attached to the TEC during the assembly

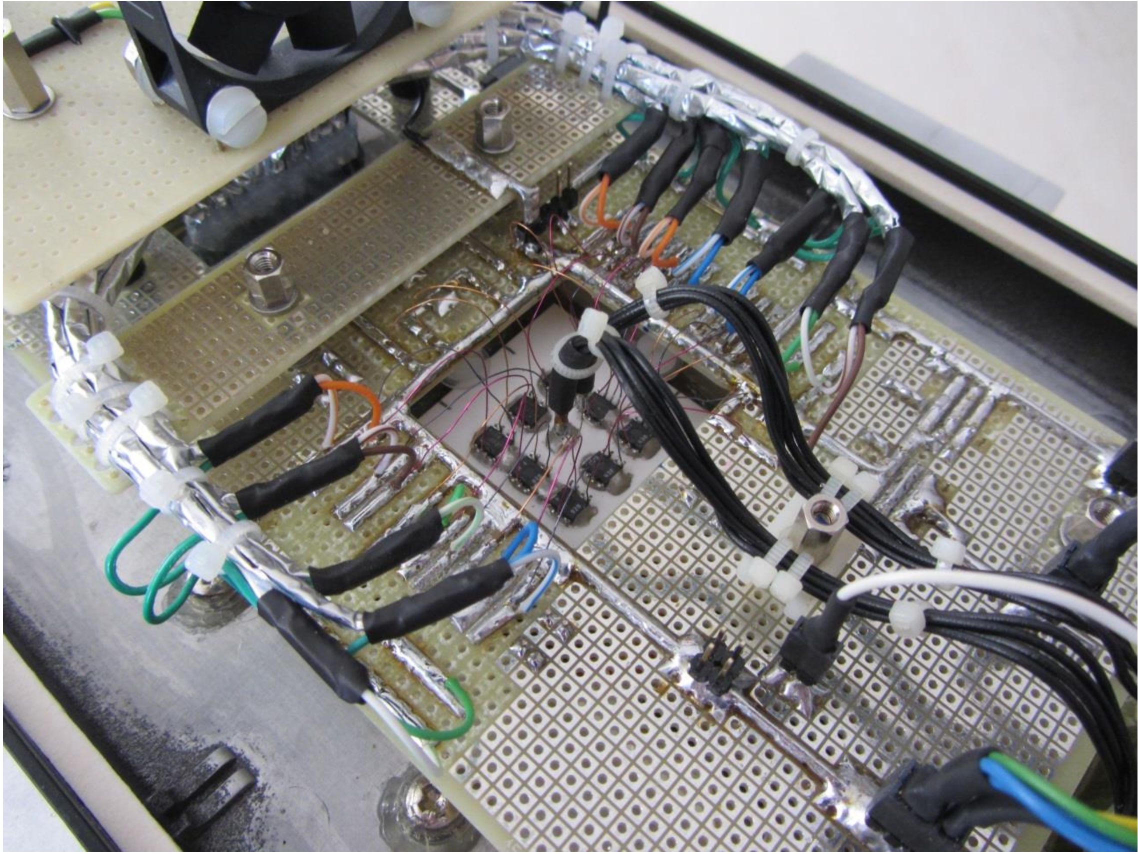
D.2 PMOS DUT container prior to the irradiation



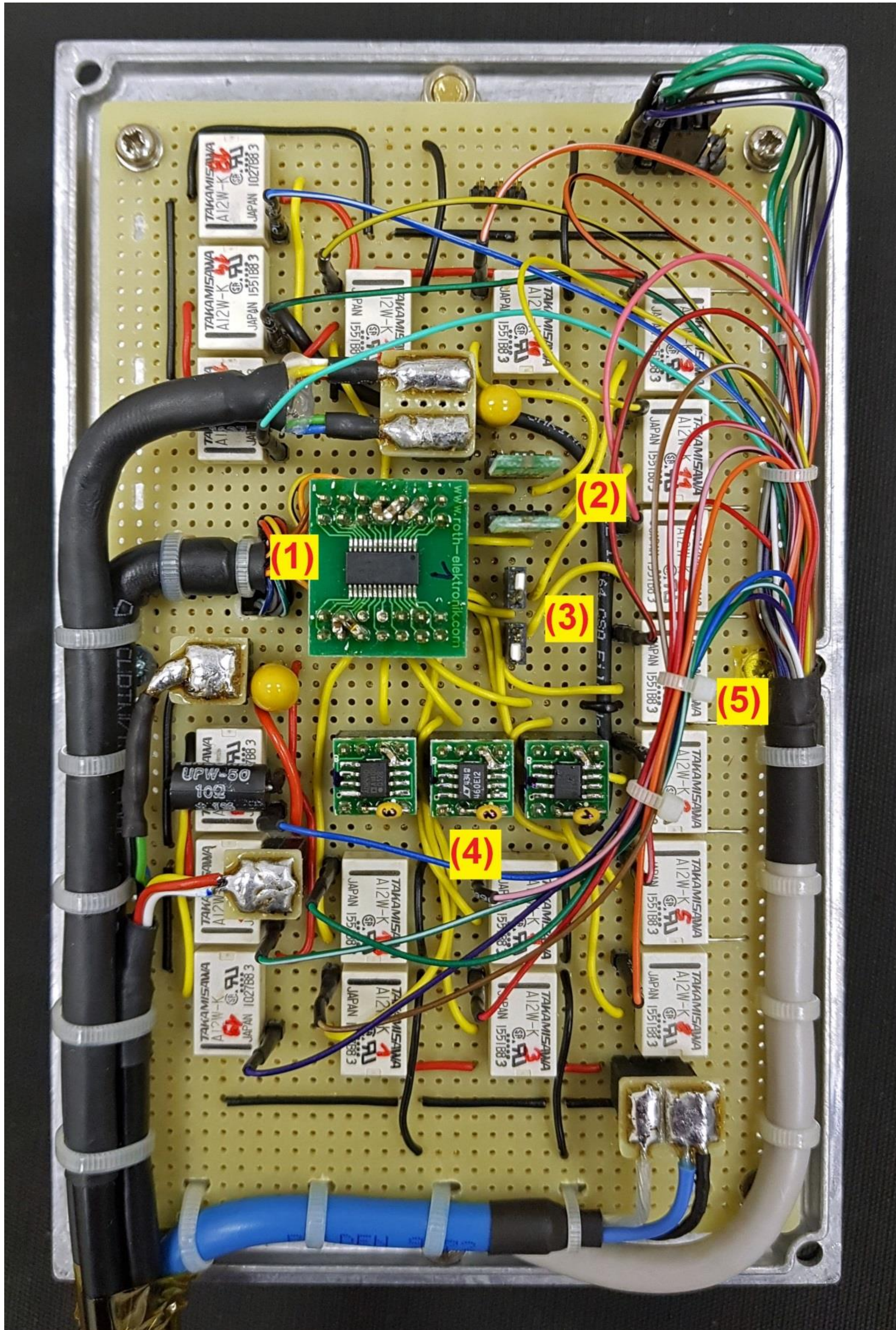
D.3 Voltage reference DUT board prior to the irradiation



D.4 Interior of the voltage reference TID-TC container



D.5 RadEx2 DEMO hardware in the TID container



Legend: (1) core ADC, (2) MOS detectors, (3) Temperature sensors (PRTs), (4) VREF devices, (5) multiplexing relays for external DMM

E MEASUREMENT UNCERTAINTIES

E.1 MU budget of the dosimetry system

Type A sources		**Notes**				
Experimental STD of the mean (u_{xA}) [%]	0.00675	Obtained from 130 dose rate measurements				
Type B sources						
Item	**Index**	$\Delta e_{i\,\max}$ **[%]**	χ	u_{eBi} **[%]**	u_{eBi} **^2[%]**	**Notes**
Detector Calibration uncertainty	1	1.1	2.000	0.550	0.303	Obtained from PTW literature
Detector Polarity effect	2	0.3	1.732	0.173	0.030	Obtained from PTW literature
Detector Long-term stability (per year)	3	1	1.732	0.577	0.333	Obtained from PTW literature
Dosemeter Accuracy of current/charge measurement	4	0.5	1.732	0.289	0.083	Obtained from PTW literature
Dosemeter Reproducibility	5	0.5	1.732	0.289	0.083	Obtained from PTW literature
Dosemeter Long-term stability (per year)	6	0.1	1.732	0.058	0.003	Obtained from PTW literature
Dosemeter Non-linearity	7	0.5	1.732	0.289	0.083	Obtained from PTW literature
Cable radiation induced leakage	8	0.75	1.732	0.433	0.188	Real value from measurement in the cell
Air density correction error (Opus20) temperature	9	0.101	1.732	0.058	0.003	Obtained from OPUS literature
Air density correction error (Opus20) pressure	10	0.050	1.732	0.029	0.001	Obtained from OPUS literature
Air density correction error (Opus20) temperature diff.	11	0.338	2.000	0.169	0.029	Estimated difference
Combined type B sources (u_{xB}) [%]	1.07					
Combined standard MU (u_x) [%]	1.07					
Extended MU (U_x for k = 2) [%]	2.2					

E.2 MU budget of the DTC temperature measurement

Type A sources		Notes				
Experimental STD of the mean (u_{xA}) [°C]	0.001	Estimated - the typical noise was below 0.005 °C				
Type B sources						
Item	**Device**	$\Delta e_{i\,max}$ [°C]	χ	u_{eBi} [°C]	u_{eBi} ^2[°C]	**Notes**
Tolerance @ 20 °C	PRT	0.134	1.732	7.736E-02	5.985E-03	Class Y at 20 °C
Selfheating	PRT	0.0005	1.732	2.887E-04	8.333E-08	I = 100uA, Pt1000, E = 20
Long-Term Stability	PRT	0.081	2.000	4.050E-02	1.640E-03	less than 0.04 % of R at max temp. of 150 °C
Tolerance 15 to 35 °C	RREF	0.0026	1.732	1.501E-03	2.253E-06	10 ppm within 15 to 35°C
Long-Term Stability	RREF	0.0005	1.732	2.887E-04	8.333E-08	2 ppm per 6 years
INL	ADC	0.0015	1.732	8.660E-04	7.500E-07	15 ppm max value
Offset error	ADC	0.0386	1.732	2.229E-02	4.967E-04	15 uV out of 0.109V @ 23°C
Offset error TC	ADC	0.0257	1.732	1.484E-02	2.202E-04	1 uV out of 0.109V @ 23°C
Gain error	ADC	0.02	1.732	1.155E-02	1.333E-04	0.02 % at 100 °C span
Gain error TC	ADC	0.01	1.732	5.774E-03	3.333E-05	0.01 % at 100 °C span as ADC warmed up by 20 °C
TEC homogenity	TEC	0.1	1.732	5.774E-02	3.333E-03	measured
Calibration using the DMM	ADC+RREF	0.1	2.000	5.000E-02	2.500E-03	estimated as worst-case
Combined type B sources (u_{xB}) [°C]	0.11977					
Combined standard MU (u_x) [°C]	0.11978					
Extended MU (U_x for k = 2) [°C]	**0.24**					