BRNO UNIVERSITY OF TECHNOLOGY
VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION
FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF MICROELECTRONICS
ÚSTAV MIKROELEKTRONIKY

ACCCELEROMETER SIGNAL PROCESSING FOR VIBRATION MEASUREMENT
ZPRACOVÁNÍ SIGNÁLU Z AKCELEROMETRU NA MĚŘENÍ VIBRACÍ

MASTER'S THESIS
DIPLOMOVÁ PRÁCE

AUTHOR — **Bc. Peter Marčišovský**
AUTOR PRÁCE

SUPERVISOR — **prof. Ing. Vladislav Musil, CSc.**
VEDOUCÍ PRÁCE

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Diplomová práce

magisterský navazující studijní obor **Mikroelektronika**

Ústav mikroelektroniky

Student: Bc. Peter Marčišovský ***ID:*** 173696
Ročník: 2 ***Akademický rok:*** 2019/20

NÁZEV TÉMATU:

Zpracování signálu z akcelerometru na měření vibrací

POKYNY PRO VYPRACOVÁNÍ:

Seznamte se s metodami monitorování stavu mechanického zařízení pomocí měření vibraci a používanými senzory. Navrhněte a realizujte precizní modul (DPS) na zpracování signálu z piezoelektrického akcelerometru, použitého na měření vibrací pro monitorování rotačního mechanického zařízení (elektromotor, turbína). Ze snímaného signálu chceme získat informaci o diagnostickém stavu stroje, např. opotřebení ložisek a vyvážení rotoru. Použijte rychlou Fourierovu transformaci (FFT) pro získání spektra signálu ze senzoru, posunutí stejnosměrné úrovně signálu (voltage level shifting) a následnou digitalizaci převodníkem ADC. Zhodnoťte dosažené výsledky.

DOPORUČENÁ LITERATURA:

According to recommendations of supervisor

Termín zadání: 3.2.2020 ***Termín odevzdání:*** 1.6.2020

Vedoucí práce: prof. Ing. Vladislav Musil, CSc.

doc. Ing. Lukáš Fujcik, Ph.D.
předseda oborové rady

BRNO UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

Master's Thesis

Master's study field **Microelectronics**

Department of Microelectronics

Student: Bc. Peter Marčišovský ***ID:*** 173696

Year of study: 2 ***Academic year:*** 2019/20

TITLE OF THESIS:

Acccelerometer signal processing for vibration measurement

INSTRUCTION:

Study methods for monitoring the mechanical system performance by vibration measurement and used sensors. Design and realise the precise module (PCB) for signal processing from a piezoelectric accelerometer used for vibration measurement aimed for monitoring of a spinning machine (like electromotor, turbine). From the signal obtained we want get the diagnostic information, e.g. bearing health, or balancing of rotor. Use a so-called voltage level shifting technique to process the input signal from the sensor and prepare it for the ADC conversion and then use the Fast Fourier Transform (FFT) to calculate the signal spectrum. Evaluate obtained results.

RECOMMENDED LITERATURE:

According to recommendations of supervisor

Date of project specification: 3.2.2020 ***Deadline for submission:*** 1.6.2020

Supervisor: prof. Ing. Vladislav Musil, CSc.

doc. Ing. Lukáš Fujcik, Ph.D.
Subject Council chairman

ABSTRACT

This master thesis deals with a design of a system capable of a high precision vibration measurement using a piezoelectric accelerometer. The system is meant to be used as a machine health conditioning for investigating a health conditions mainly, of electrical machines like an electro motor or a turbine. In order to achieve a high precision and a high linearity measurement in extreme low frequency spectrum ranging even from DC levels, trough sub-hertz spectrum to tens of hertz, as well as in a higher frequency spectrum, a possibility of using a DC-coupled approach called a "voltage level shifting" technique has been required to investigate and consequently to evaluate the difference between the DC-coupled and a generally used AC-coupled approach for interfacing with piezoelectric accelerometers.

KEYWORDS

vibrations, FFT, machine health monitoring, piezoelectric accelerometer, precision ADC, sigma-delta, signal processing, voltage level shifting

ABSTRAKT

Táto diplomová práca sa zaoberá návrhom zariadenia schopného vysoko presného merania vibrácií za použitia piezoelektrického akcelerometra. Zariadenie je určené na vyhodnocovanie zdravotného stavu strojov, najmä elektrických strojov ako elektromotor, veterná turbína a iné. Za účelom dosiahnutia vysoko presného a vysoko lineárneho merania v spektre extrémne nízkych frekvencií siahajúcich až ku jednosmerným napätím, cez sub-hertzové pásma po desiatky hertzov, ale aj vo vyšších frekvenciách, bola vyžadovaná možnosť použitia prístupu s jednosmernou väzbou zvaného "posúvanie napäťovej úrovne" a následné vyhodnotenie a porovnanie prístupu so striedavou väzbou, ktorý sa bežne používa pre pripojenie piezoelektrického akcelerometra.

KLÍČOVÁ SLOVA

vibrácie, FFT, pozorovanie zdravotného stavu stroja, piezoelektrický akcelerometer, precízny ADC, sigma-delta, spracovanie signálov, posúvanie napäťovej úrovne

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ROZŠÍŘENÝ ABSTRAKT

Na trhu sa vyskytuje značný počet návrhových riešení, ktoré sa zaoberajú touto problematikou, avšak drvivá väčšina riešení používa vstupný člen so striedavou väzbou pre pripojenie piezoelektrického akcelerometra k meraciemu systému. Tento prístup je jednoduchý a lacný, avšak má za následok rapídne zhoršenie vlastností vo veľmi nízkom spektre frekvencií, ako aj v ostatných frekvenčných pásmach, ak sa nepoužije dostatočne kvalitný kondenzátor vo väzbe.

Spoločnosť Analog Devices, v ktorej tento projekt vznikol sa rozhodla preskúmať práve prístup s jednosmernou väzbou, pri ktorom je očakávané rapídne zlepšenie presnosti a linearity. Tento prístup využíva techniku takzvaného posúvania napäťovej úrovne, keďže všetky piezoelektrické akcelerometre majú značne vysoké predpätie, s ktorým musí byť správne naložené. Práve dokonalé zvládnutie tejto techniky je jedna z hlavných výziev pre riešenia s týmto typom väzby. Návrh hardvéru bol vedený tak, aby sa s jednoduchosťou mohlo prechádzať medzi obidvomi väzbami, za účelom porovnania ich vlastností.

Ako aktívny vstupný člen - posúvač napäťovej úrovne, bolo zvolené invertujúce zapojenie operačného zosilňovača, ktorý sa v tomto prípade chová ako sumačný zosilňovač. Na neinvertujúci vstup sa privedie pohyblivé napätie z DAC prevodníka. Na invertujúci vstup je privedené napätie zo sensora, ktoré sa ďalej spracúva. Toto napätie pozostáva z jednosmerného predpätia a striedavého napätia ktoré je už priamo úmerné vibráciám.

Pre posúvanie napäťovej úrovne bol zvolený DAC prevodník, ktorý umožňuje automatizáciu celého procesu. DAC prevodník vyvažuje vstupnú napäťovú asymetriu pomocou aktívnej kontrolnej slučky pozostávajúcej z ADC a DAC prevodníkov. Proces je podobný fungovaniu SAR ADC. Kdežto v tomto prípade sa nehľadá konečná hodnota neznámeho napätia ale minimalizuje sa stredné napätie pri vstupoch ADC prevodníka za účelom minimalizácie ofsetu.

Signál je navzorkovaný 24-bitovým sigma-delta ADC prevodníkom AD7768-1 s digitálnym postprocesingom. AD7768-1 bol zvolený hlavne kvôli linearite, nízkemu harmonickému skresleniu, nízkemu šumu a vhodnému frekvenčnému pásmu.

Frekvenčné pásmo, pomocou ktorého sa skúmajú defekty prístrojov, sa získa za použitia rýchlej Furiérovej transformácie FFT. Transformácia, ako aj všetky potrebné kalkulácie prebiehajú bez použitia osobného počítača, čo dodáva zariadeniu vyššiu flexibilitu. Celý dizajn ovláda mikrokontrolér s DSP modulom, na ktorom prebieha transformácia.

Aby sa potvrdilo, že Furiérova transformácia spolu so všetkými potrebnými kalkuláciami je správna, sada dát zachytených AD prevodníkom sa spracovala dvomi spôsobmi. Pomocou tohoto firmvéru, ktorý pracoval výhradne na mikrokontroléri

a pomocou firemného FFT jadra založeného na softvéri LabView, ponúkaného ako evaluačný softvér zákazníkom spoločnosti. Zhoda týchto dvoch spôsobov je zhrnutá v tabuľke 3.2 a dosahuje mimoriadnej presnosti ako to napríklad: rozdiel kalkulácie dynamického rozsahu je iba $1\,mdB$.

Vyhodnocovacie merania celého dizajnu naznačujú, tak ak sa očakávalo, že celkový integrovaný šum varianty s jednosmernou väzbou je vyšší. Nejde však o nejaký závratný nárast, keďže rozdiel v dynamickom rozsahu je iba $1{,}7\,dB$ pre šírku pásma $16\,kHz$ a teda celkový dynamický rozsah je lepší ako $105{,}7\,dB$ pre obidve varianty na danej šírke pásma, čo je veľmi dobrý výsledok na tento pomerne zložitý analógový frontend, pričom dynamický rozsah samotného ADC so skratovanými vstupmi je podľa katalógového listu $108{,}45\,dB$ pri zhodnej konfigurácii registrov. Jedná sa taktiež o meranie so skratovanými vstupmi celého riešenia.

Pri meraní harmonického skreslenia sa prejavil efekt nesprávne zvoleného kondenzátora vo vstupnej striedavej väzbe, kde pri použití klasického keramického kondenzátora umiestneného v rozmerovo malom puzdre sa harmonické skreslenie zhoršilo o viac ako $60\,dB$ oproti variante s jednosmernou väzbou, pričom frekvencia vstupného signálu bola ešte stále ďaleko v priepustnom pásme vstupného filtra.

Po výbere správneho typu kondenzátora sa úroveň harmonického skreslenia obidvoch variánt takmer vyrovnala s tým, že varianta s jednosmernou väzbou dosahovala lepšie výsledky. Spodná frekvenčná hranica použitého vstupného signálu bola limitovaná laboratórnou technikou na $10\,Hz$ a medzná frekvencia vstupného filtru typu hornej priepuste bola experimentálne zvolená na hodnotu okolo $1\,Hz$. Táto konfigurácia umožňovala porovnávať rozdiely spôsobené rôznymi typmi väzieb a nie nastavením polohy medznej frekvencie. Fakt, že linearita, meraná amplitúda a šum sa znížia keď signál nebude v priepustnom pásme filtra je jasný a teda nebol ani overovaný meraním, keďže sa jedná o záležitosť nastavenia medznej frekvencie, čo nie je náplňou tejto práce.

Merania znázorňujúce detekciu defektov na zariadení boli vykonané len pre demonštráciu na malom ventilátore. Merania ukazujú dva typy defektov, a to nevyváženosť a nerovnováhu. Nerovnováha bola docielená pripevnením malého závažia na lopatku ventilátora.

DECLARATION

I declare that I have written the Master's Thesis titled "Accelerometer signal processing for vibration measurement" independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the thesis and listed in the comprehensive bibliography at the end of the thesis.

As the author I furthermore declare that, with respect to the creation of this Master's Thesis, I have not infringed any copyright or violated anyone's personal and/or ownership rights. In this context, I am fully aware of the consequences of breaking Regulation § 11 of the Copyright Act No. 121/2000 Coll. of the Czech Republic, as amended, and of any breach of rights related to intellectual property or introduced within amendments to relevant Acts such as the Intellectual Property Act or the Criminal Code, Act No. 40/2009 Coll., Section 2, Head VI, Part 4.

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author's signature

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Thank you!

Brno ....

author's signature

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Introduction

There are many designs dealing with the machine health conditioning on the market. While a vast majority of the available commercial solutions use an AC-coupled approach to interface the piezoelectric accelerometer, which is very cheap and easy to design, those solutions lack precision in a low frequency spectrum due to the cutoff frequency of the input high-pass filter and a coupling capacitor parasitic distortion effects. A frequency range of some solutions starts as high as $10\,Hz$ which might be insufficient for slowly spinning machines like wind turbines.

A company Analog Devices, where this thesis was created, has allocated its resources for a project based on a completely different approach based on a DC-coupled interface called a "voltage level shifting". While there is no high-pass filter at the very input of the signal chain, the frequency response can be pushed down to mHz spectrum, even to investigate DC voltage levels. Due to lack of the coupling capacitor, the harmonic distortion and linearity is expected to be improved significantly. But on the other hand, the DC-coupled approach comes with more expensive and complicated design.

The thesis begins with a hardware design, which accentuate a very low noise and high linearity design. A vibration dependent voltage signal passes through a first stage of the analog signal chain where the signal is attenuated and shifted to a desired voltage level, afterwards an FDA converts it from single-ended to differential voltage and limits it's bandwidth, preparing it to be sampled by an ADC.

Following firmware design chapter interprets how the sampled signal is being transformed from a time domain to a frequency domain and how all the necessary calculation of THD, DR, SNR etc. are carried out, in order to deliver a reliable and a precise signal processing. Those calculations are further used to evaluate the input signal. All the processing is taking place on a microcontroller featuring a DSP module. The microcontroller also interfaces with the ADC, DAC, and other circuitry present on the PCB.

The thesis ends with evaluation measurements, showing the achieved results of various types of measurements and testing. Results of demonstration vibration spectrum analysis are shown, detecting faults on a real testing device.

Since the topic of the thesis was granted by the company Analog Devices, there might be a potential risk of claiming the company's contribution as my own contribution. I was the only person actively working, from a design point of view, on this project with an intensive help from my ex colleagues whom I am enormously grateful for their support. But a piece of the project I am sharing in this thesis is solely my contribution, except the PCB design which was carried out by an ex colleague of mine.

1 Theoretical background

The following chapter provides a theoretical introduction about most common types of defects, detectable by vibration spectrum analysis.

1.1 Types of defects

Various types of mechanical defect could be observed on any piece of machinery in order to determine a health status of a machine. Some of them, the more obvious, can be easily recognized just by looking at, or by listening to the machine. In other, most of the cases, machines must be investigated by set of sensors. There are various ways of determining the health status of a machine, using various types of sensors. When an accelerometer attached directly to the machine is used for investigating, an user can very easily and quickly find out if the machine is running correctly or if there is a hidden slowly developing threat which might be mortal for the machine. [1, 2]

A frequency spectrum of the vibrations produced by the machine is very convenient and straightforward method for the machine health evaluating. The scientific discipline of evaluating a machine health status based on a frequency spectrum of vibrations has been explored in detail by various institutions around the world. It has been found, that each already known defect has a typical frequency spectrum pattern, sometimes based on a construction of a machine like a diameter of balls in a bearing, number of blades on a fan etc. The typical frequency spectrums were defined in [1, 2]. Only the most common types will be covered in following subsections:

- Imbalance
- Misalignment
  - Angular misalignment
  - Parallel misalignment
- Mechanical looseness

1.1.1 Imbalance

The most usual and the easiest defect to detect is imbalance. The imbalance could be defined as: *The imbalance occurs when the shaft's mass centerline does not coincide with its geometric centerline* [2]. It can be understood as a fan with one blade slightly heavier than the other blades, which creates the uneven distribution of the mass. There are several types of imbalances described in [1], but the important

thing is, that all of them have the same typical frequency response depicted in a figure 1.1 below, where only the $1 \times RPM$ is visible and very dominant.

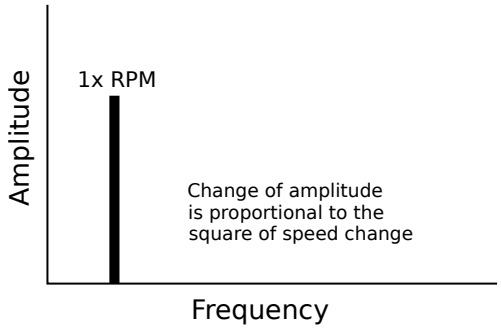


Fig. 1.1: Typical frequency spectrum of an imbalance [3]

The easy-to-detect ability of this defect is a fact, that the imbalance amplitude changes with the square of the rotor's speed.

1.1.2 Misalignment

The next, most common type of faulty state along with the imbalance is a misalignment. This type of defect originates in couplings, bearings and shafts not being correctly aligned. There are two types of the misalignment depicted on a figure 1.2 below: angular and parallel or a combination of the two. [1, 3]

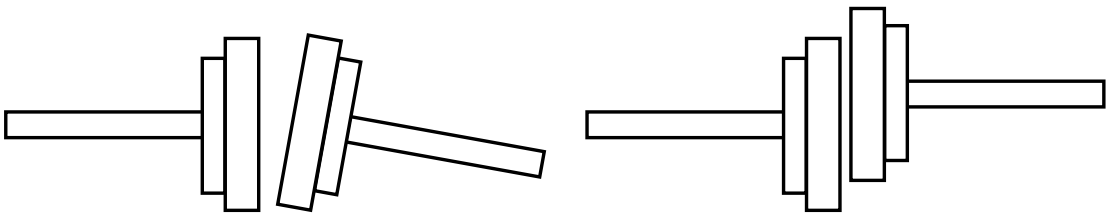


Fig. 1.2: Angular and parallel misalignment [2]

- Angluar misalignment affects the 1xRPM amplitude in the frequency spectrum of axial vibration and usually goes along with non-dominating 2^{nd} and 3^{rd} harmonics. The pure angular misalignment is exceptional.
- Parallel misalignment's envelope is similar to the angular misalignment, since usually both occur together. It can be recognized as a 2^{nd} harmonics domination in the radial direction. [3]

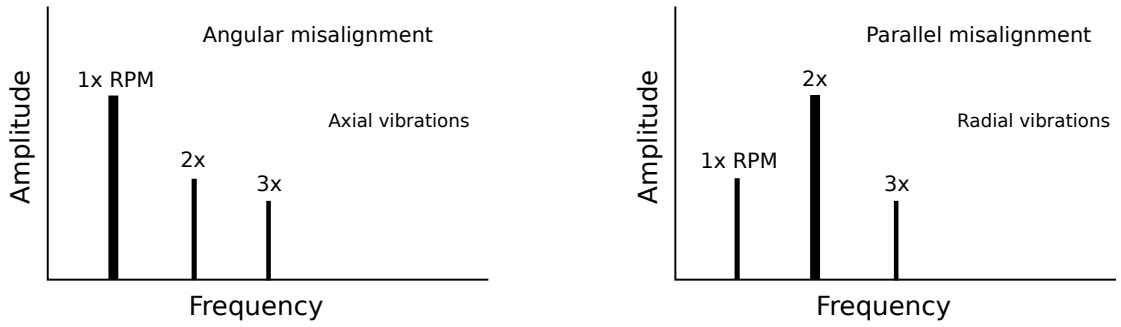


Fig. 1.3: Typical frequency spectrum of both types of misalignment [3]

The figure 1.3 above depicts typical frequency response of both, the angular and the parallel misalignment. Keep in mind the different direction of vibrations - axial and radial directions in which the certain type of misalignment dominates, which is caused by a $\pi/2$ phase shift across the mechanical coupling. [3]

1.1.3 Looseness

There are several types of looseness that may occur: looseness in the machine's structure or base plate, but the most common is an internal assembly looseness. It could be caused by a sleeve or a ball in a bearing, by a shaft, by incorrect alignment between machine's parts etc. [3]

It is very directional and time unstable. The same set of measurement might vary with time from each other even though, if the same condition measurement is assured. This looseness can be measured from different angles. Sub-harmonic multiplies are strong cognitional signs, as a figure 1.4 below depicts. There might appear multiplies at ½ or ⅓ of the RPM, even further multiplies like 2 ½ or 5 ½ are common. [3]

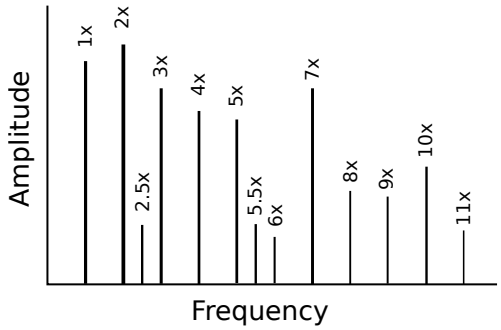


Fig. 1.4: Typical frequency spectrum of a looseness [3]

1.2 Frequency spectrum of interest

To picture out where a typical bandwidth of interest lays, let us consider a common 4-pole electric generator used in a power plant providing an alternating current of $50\,Hz$. To get the RPM of the generator a following equation is used:

$$RPM = f_c \times 60 \times (\frac{2}{n}) \tag{1.1}$$

where the f_g is the mechanical frequency of the generator, f_c is the frequency of the generated alternating current and n is number of poles. The generator rotating speed results in $1500\,rpm$, which is only $25\,Hz$. For comparison, a typical rotating speed of a $5\,V$ powered PC fan is $7000\,rmp$, which is $177\,Hz$. While more than $250\,Hz$ of any turning machine is very rare. For a very slow turning machines like a win-turbine, having only a few RPMs, even lower, a sub-hertz and DC spectrum is very interesting to look at.

As the section 1.1 above shows, only few harmonics of a very-low frequency carrier are required to identify vast majority of defect types, when not considering bearing problems which are visible at very high frequencies - at tens of kHz.

2 Hardware design

The following chapter deals with a hardware design, explaining basic blocks of the circuitry, selection and values of all the used parts.

2.1 High level design

A picture 2.1 below shows a simplified block diagram of the hardware solution.

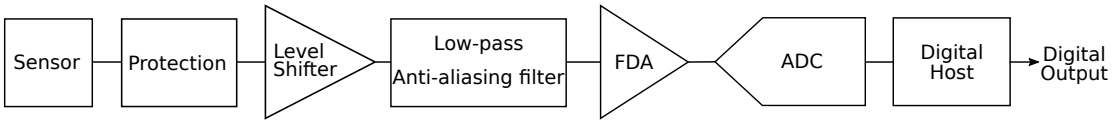


Fig. 2.1: Basic block diagram

The main signal path goes from the piezoelectric sensor, through an input protection, to a voltage level-shifter, an anti-aliasing filter, a driving amplifier stage and finally to an ADC. A microcontroller or an FPGA is used to communicate with the ADC, mostly for the data reception, but also for setting various registers in the ADC.

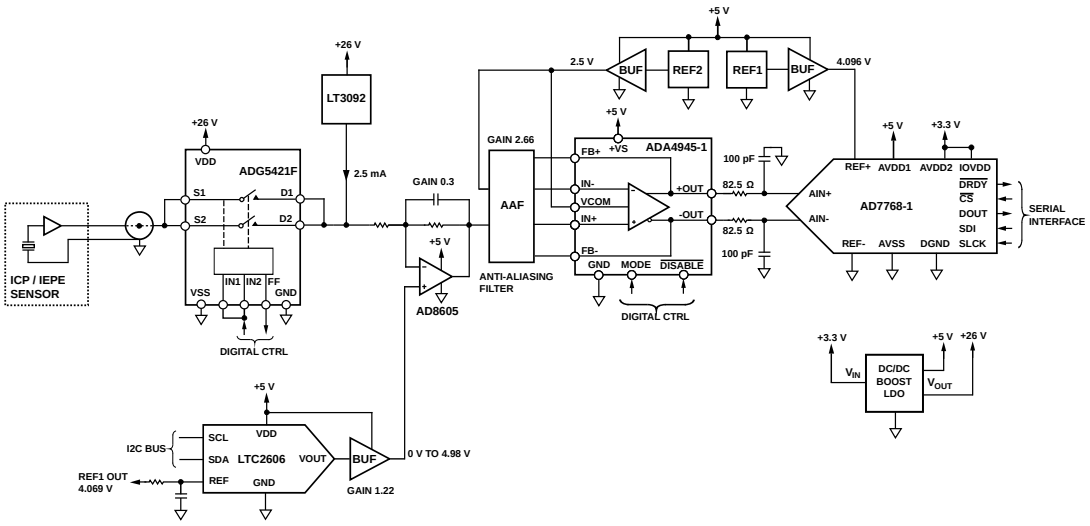


Fig. 2.2: Detailed block diagram without the digital host

More detailed block diagram from the picture 2.2 above is showing not only the main signal path, but also auxiliary ones with specified part numbers and, important voltage levels and gains. Majority of the blocks from the detailed block diagram will be discussed.

2.2 The sensor

There are two types of piezoelectric accelerometers distinguishable by an output impedance are either low or high output impedance accelerometers. The high output impedance ones provide a user with a charge output which must be converted into a voltage using an external circuitry. The low output impedance ones have the charge to voltage converter built in, thus use the same sensing element. For most of applications it is more convenient to use the low output impedance one. [4]

The low output impedance accelerometers are manufactured by various companies, but usually are compatible with IEPE or its equivalent ICP standards. Thus, the working principle of the IEPE/ICP compatible accelerometers is the same. The design is not targeting any specific piezoelectric accelerometer, but is carried out in more general way, in which the design will be compatible with various piezoelectric IEPE/ICP compatible accelerometers.

The sensor selection providing the best parameters for the specific application is not necessary. The ICP piezo sensor PCB 333B53 has been chosen as a reference which will be worked with, due to its sufficient frequency response of up to $3\,kHz$, the measurement range of $\pm\,5\,g$ and a fairly low wide band noise density of $0.4\,\mu g\sqrt{Hz}$. [5]

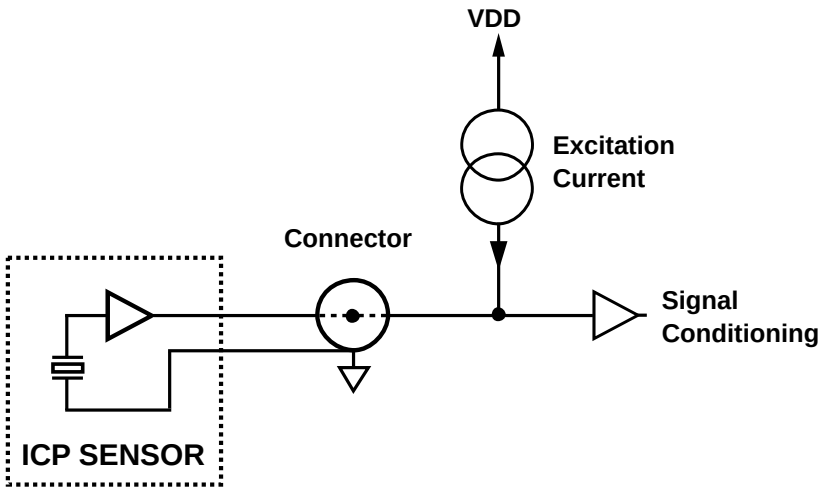


Fig. 2.3: Driving an ICP/IEPE piezoelectric accelerometer

The figure 2.3 depicts an ICP/IEPE accelerometer being driven by an external circuitry. The charge of the piezoelectric sensing element is amplified and transformed from the charge to the voltage internally by a charge amplifier which is driven by the excitation current. The output value is a voltage. The level of the excitation current could according to the data sheet lays anywhere between $2\,mA$

and $20\,mA$ [5]. The excitation current depends solely on a type of cable being used, according to a following equation 2.1: [4]

$$f_{max}\,[Hz] = \frac{10^9 \times (I_{exc}\,[mA] - 1)}{2\pi \times C_{cable}\,[pF] \times V} \tag{2.1}$$

where:

- f_{max} is the maximum output frequency of the sensor - cable setup,
- C is a cable capacitance,
- V is the maximum peak to peak output voltage of the sensor,
- I_{exc} is the excitation current.

Note that in the equation 2.1, $1\,mA$ is subtracted from the total current supplied to the sensor I_{exc}, where approximately $1\,mA$ is used for powering the sensor itself and the rest of the current is used for driving the cable.

For example, in our case when the sensor PCB 333B53 having the maximum output peak to peak voltage of $10\,V$ was used together with a $10 - ft$ long cable with a capacitance of $29\,pF/ft$ and the excitation current was experimentally chosen to be $2.5\,mA$. Applying the equation 2.1, the maximum theoretical bandwidth of the sensor is $82.3\,kHz$. Both, the used cable, and the chosen current level do not limit the performance of the sensor, having actual bandwidth of $3\,kHz$.

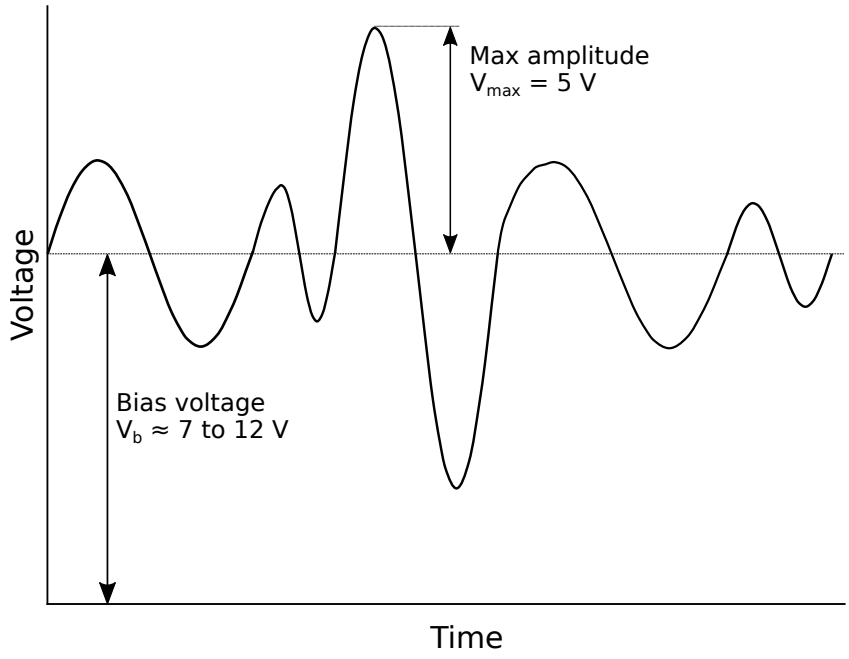


Fig. 2.4: Typical voltage output of the piezoelectric accelerometer PCB 333B52 [4]

The figure 2.4 depicts a typical voltage output of the used piezoelectric accelerometer. The bias voltage differs from sensor to sensor and typically lays between a

voltage range from $7\,V$ to $12\,V$ for this specific sensor. The bias is steady and do not carry any information, thus is normally high passed or level shifted in a signal conditioning. The AC part of the voltage output directly depends on vibrations. [4]

2.3 Input protection

The solution is intended to be used in a harsh industrial environment, thus relying on an embedded input, mostly only the ESD protection every integrated circuit features with is not enough. A more robust protection is commonly required, even advised, to meet the industrial standards.

In this application, mainly the input of the circuitry is considered as an issue. In case of a long cable used to connect the sensor mounted directly on the machine and the PCB itself, there is a potential risk of inducted voltage. There also might happen to be a cable connection mismatch when a high voltage output cable is accidentally connected to the connector on the PCB. To prevent the PCB from destroying by presence of the high voltage at the input of the PCB, it is advised to use a high voltage protection switch. It would be comfortable to use the over-voltage protection in combination with the ESD protection in one package.

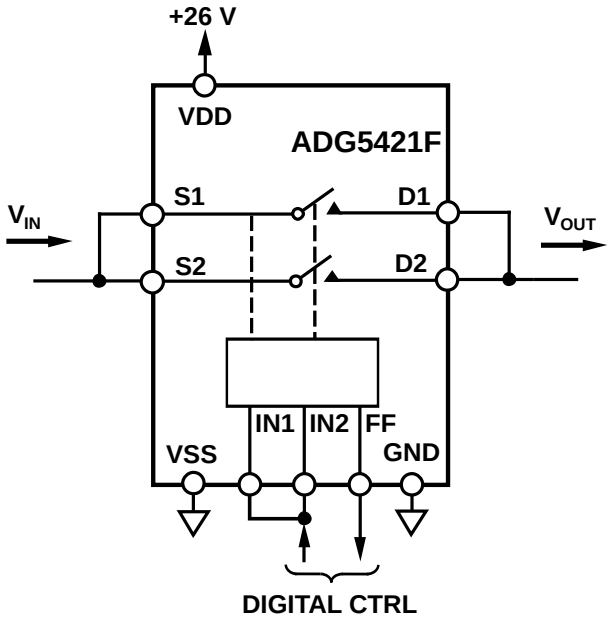


Fig. 2.5: Internal structure of the input protection switch ADG5421F

The Analog Devices has a wide portfolio of over-voltage protection products. In order to promote new products, the ADG5421F [1] , displayed on the figure 2.5

[1]The ADG5421F has not been released yet

above, suits to this project very well. The fault flag output FF, gives a user a binary information whether a fault state has occurred or not. An unprotected input signal goes to the $S1$ and $S2$ inputs and a protected signal appears at the $D1$ and $D2$ outputs. The switches can be operated either manually by changing the voltage levels at the $IN1$ and $IN2$ inputs or automatically by the part itself. In case of the fault state has occurred, the ADG5421F protects the following circuitry by disconnecting the Sx from the Dx. The fault state can be understood as any voltage level higher than $VDD + 0.7\,V$ applied to the Sx, which includes the ESD case as well. In this case the switch is powered by the highest voltage level available on the PCB, which is $26\,V$.

2.4 Constant current source

A constant current source (CCS) is required, when interfacing any ICP/IEPE piezoelectric accelerometer. Some competitive designs might feature with a CCS controlled by an MCU/FPGA over a data bus, or feature with a current output DAC. But an accurate current value provided by the CCS is not important for the sensor performance as already explained above in the subsection 2.2. Also changing the current value does not make any sense during the operation. The most important attribute of the CCS is a current noise produced by the CCS block, which will be explained in a subsection below.

Taking in account the above-mentioned demands, a fully integrated on-chip solutions with an LT3092 yields a discrete current source solution for its compactness and small dimensions, up-to $40\,V$ of tie input voltage, up to $200\,mA$ of regulated current and a fully-floating structure. The Analog Devices offers various current sources capable of delivering much higher currents, but taking in account the maximum driving current of tens of mA required by an ICP/IEPE piezoelectric accelerometer the LT3092 has been chosen mainly for its maximum output current which is the lowest among the other on-chip current sources and is more than enough for powering the sensor. [6]

As a figure 2.6 below depicts, the CCS requires only 2 resistor R_{SET} and R_{OUT} to set the output current value. The C_{SET} capacitor reduces a bandwidth of the current noise produced by the whole block and the C_{COMP} is placed, when there are stability issues. The noise parameters will be described in the subsection below.

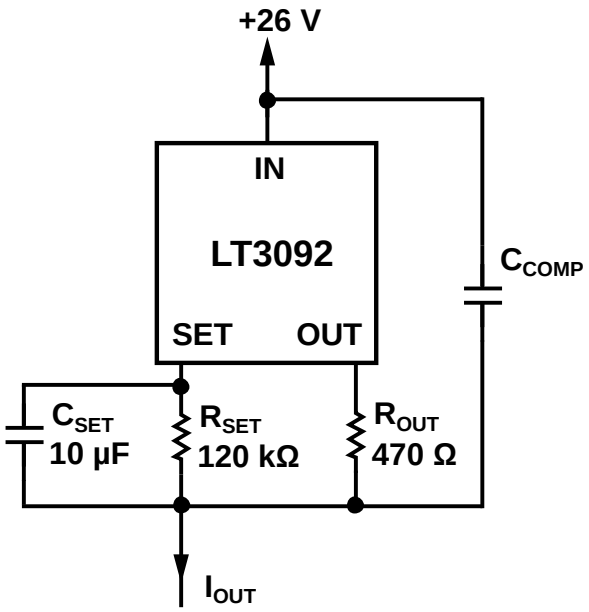


Fig. 2.6: Constant current source LT3092 providing a 2.5 mA output current [6]

An LT3092's internal $10\,\mu A$ reference current source holds a stable voltage across the R_{SET}. The voltage across the R_{SET} mirrors to the R_{OUT} which sets the output current according to a following equation 2.2:

$$I_{OUT} = \frac{V_{SET}}{R_{OUT}} = \frac{10\,\mu A \times R_{SET}}{R_{OUT}} \tag{2.2}$$

note that the actual I_{OUT} current is $10\,\mu A$ larger than the output current given by the equation 2.2 because of the internal reference current flowing out of the SET terminal. After substituting into the equation 2.2, the output current value was was set to $2.5\,mA$. [6]

2.4.1 Constant current source noise

As already mentioned above, a special care must be taken when designing the CCS from a perspective of the output current noise. The CCS block is at the very beginning of the signal chain and any current noise flowing through the input impedance having a resistive character, will be transformed to the voltage noise and multiplied by the actual value of the resistive element.

The LT3092's data sheet recommends the R_{SET} equals to $20\,k\Omega$ to minimize the offset voltage of the IC itself and to set the voltage drop across the R_{SET} to low (even to minimal), $200\,mV$, value. [6]

$$i_{noise} = \sqrt{\frac{4 \times k \times T}{R}} \tag{2.3}$$

An equation 2.3 above, is the equation of white current noise produced by a resistor, where T is an absolute temperature in $Kelvins$, k is the Boltzmann's constant in and R is the resistance of a resistor. Since a resistor value is indirect proportional to the current noise of the resistor, increasing a value of the R_{SET} from recommended $20\,k\Omega$ to $120\,k\Omega$ will increase R_{OUT} as well (keeping the output current at the same level according to the equation 2.2), but most importantly will rapidly decrease the white noise current produced by the resistors. A capacitor C_{SET} across the R_{SET} is recommended to lower the current noise of the R_{SET} and of the LT3092's internal current reference. The C_{SET} capacitor bypasses the current noise coming from the LT3092. [6]

An LTspice simulation of the constant current source from the Figure 2.6 was performed in order to explain component values and placement dependency. A non-ideal voltage source was modeled, providing $0.7\,mV\,RSM$ of the voltage noise and $224\,nA\,RMS$ of the current noise at very wide bandwidth up to $20\,MHz$ simulating a bench power supply Keysight E3631 with two outputs connected into series, set to $26\,V$.

Tab. 2.1: Quieting the current noise of the constant current source

Noise [nA RMS]	**R_{SET} [kΩ]**	**R_{OUT} [Ω]**	**C_{SET} [F]**	**C_{COMP} [F]**
158.8	20	80.6	-	-
1273.5	20	80.6	-	100 n
202.7	20	80.6	-	10 n
15.5	20	80.6	100 n	-
14.5	20	80.6	10 μ	-
3.1	120	470	10 μ	-

The table 2.1 above shows a part and a value dependency on the current noise coming out of the constant current source block. The RMS noise current of the CCS block was simulated for a bandwidth from $1\,mHz$ to $100\,kHz$. Please note, that the table 2.1 above shows only a made-up scenario to show an impact of the real (non-noiseless) voltage source connected to the CCS block. The LTSpice simulator does not allow to simulate a noise of an DC-DC converter, which is in our case connected to the CCS block, thus the real scenario is not possible to simulate.

The C_{COMP} acts like a high-pass filter, passing the noise from the voltage source to the output. Further increasing of the R_{SET} and the R_{OUT} would help in the

current noise reduction, but it would also cause higher voltage drop over the resistors. When a long cable with a high level of capacitance is used, a user might face a stability issue. In this case the C_{COMP} is recommended to consider.

As mentioned above, a downside of increasing the resistor values is increasing the dropout voltage over the CCS block, thus a wider voltage room is required when designing the voltage source for the CCS block. In our case, the voltage dropout over the CCS block is calculated as:

$$V_{DROP} = R_{SET} \times I_{INT\,REF} + 1.2 \tag{2.4}$$

where, the $I_{INT\,REF}$ is the internal, $10\,\mu A$ current reference of the LT3092, and $1.2\,V$ is a voltage dropout over the LT3092 itself at the temperature of $25\,°C$ and the output current of approx. $10\,mA$. Applying the equation 2.4 to our case: before the current noise improvement, the dropout is $1.4\,V$ and after the improvement $2.4\,V$. The toll we paid only one volt of additional dropout, but the noise improvement is tremendous, where more than 50-times better noise parameters have been achieved in the simulation, looking at the table 2.1.

2.5 Input signal conditioning

The chosen piezoelectric accelerometer has a typical output bias voltage of $10\,V$ and an output voltage swing of $\pm 5\,V$. This output signal is too high and has too wide voltage swing to be connected directly to a standard ADC input. There are two possible ways, of transforming the sensor's output voltage to a desirable voltage level. One can choose either a DC or an AC coupling. Even though, this project deals with the DC coupled design, the AC will be discussed anyway to compare the two solutions.

2.5.1 Coupling capacitor - AC coupling

The easiest way how to extract the AC part and remove the DC bias voltage is to put a decoupling capacitor to the signal path. Employing a capacitor to the signal path would have been a vital option, if we did not care about very low frequency band. Vibrations produced for example by wind turbines which are rotating quite slowly, tend to have very very low frequency spectrum, sometimes less than $1\,Hz$!

Each real capacitor has an internal serial impedance, which depends on its capacitance and on a frequency of a signal passing through the capacitor. This phenomenon can be expressed by a following formula:

$$X_C = \frac{1}{2\pi C f} \tag{2.5}$$

where C stands for the capacitance in Farads and f stands for the frequency in Hertz. So for example: if a capacitor with the capacitance of $10\,\mu F$ is put to the signal path and the formula 2.5 is applied, the capacitor's impedance at the frequency of $10\,mHz$ is $1.6\,M\Omega$ and at frequency of $100\,Hz$ is only $160\,\Omega$. This frequency dependency causes too big non-linearity to be accepted. By increasing the value of the capacitor, we also increase price and dimensions of the solution, while big-valued capacitors tent to be bulky, expensive and have other non-vital abilities. The coupling capacitors in general cause variety of distortion effects, which will be explained in a section 4.9.

2.5.2 Voltage level shifter - DC coupling

While the usage of the coupling capacitor is not sufficient solution for this application, an active voltage level shifting technique will be used. This approach is based on an op amp with a negative feedback, where the common mode voltage at the output of the op amp is actively controlled by a control feedback loop. This op amp structure is basically a well-known summation op amp topology with one voltage level being constant (the shifting one) an the other being used as a signal path, which subsequently works as a voltage level shifter.

2.5.3 Level shifter requirements

It is very vital to set the requirements at the very beginning of the design. Once the expected voltage levels on the input of the signal chain are known, a proper level shifter which fits into the application can be designed. The V_{out} voltage produced by the voltage shifter is desired to be as close to the $VCOM(2.5\,V)$ as possible to balance the input of the following stage with an FDA. The gain of the op amp must be set with respect to a following aspects:

- supply voltage of the shifting op amp: $(0\,V - 5\,V)$,
- range of the shifting voltage: $(0\,V - 5\,V)$,
- stability of the shifting op amp,
- full-scale range of the ADC: $\pm 4.096\,V$,
- maximum input signal amplitude: $10\,V_{Pk-Pk}$,
- maximum input signal offset: up to $13\,V$,
- maximum input voltage capable of being handled: $18\,V$,
- sufficient input impedance: $\sim 100\,k\Omega$,
- low noise design.

The above-mentioned requirements must be carefully considered for efficient design of the signal chain's first stage.

2.5.4 Topology of the voltage level shifter

There are three main level-shifting op amp topologies for driving an ADC input in DC-coupled applications depicted in a figure below. [7]

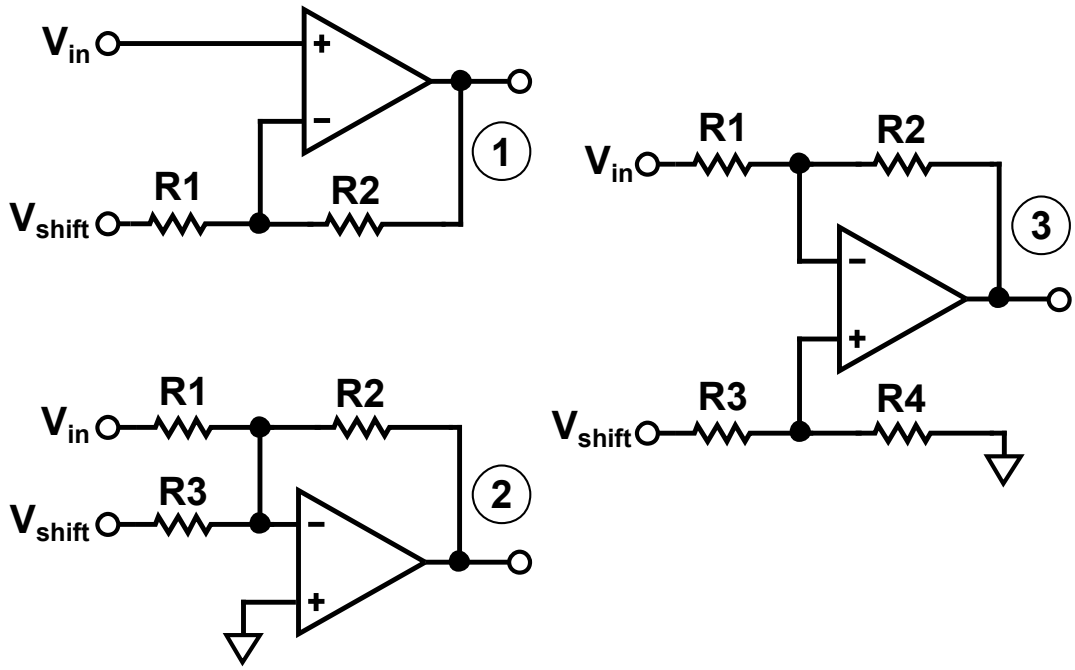


Fig. 2.7: Different topologies of the voltage level shifter [7]

1st Topology

The option one has an excellent input impedance, being dependent only on the input impedance of the op amp itself, which would perfectly drive the sensor at the first stage of the signal chain. The noise gain combines both resistors according to an equation 2.22, which will keep the noise of the stage low-enough. The only main disadvantage is in its transfer function:

$$V_{out} = \left(1 + \frac{R2}{R1}\right) \times V_{in} - \frac{R2}{R1} \times V_{shift} \tag{2.6}$$

As it is visible from the equation 2.6, the first topology does not attenuate the input under and extremely high shifting voltage would be needed to shift the considerably high input signal from down to desired $2.5\,V$. Also, an output impedance of the shifting voltage source affects the transfer function. [7]

2nd Topology

The input impedance of the second topology is significantly lowered and it is dependent on the values of the resistors. It does attenuate the input signal, since it is based on an inverting op amp, but increases the overall noise, by connecting another resistor to the signal path according to a following equation:

$$NG = 1 + \frac{R1}{R2 \,||\, R3} \tag{2.7}$$

In order to keep the system's noise as low as possible, this topology would not satisfy the needs of the project. Also, the shifting issue mentioned in the first topology is present and very similar here. [7]

3rd Topology

The final topology has a suitable noise gain, according to an equation 2.22. As same as above, the input impedance is lowered and resistor dependent. It can attenuate the input and shifting it down to the desired voltage level using voltages low-enough to meet the low-voltage supply design according to a following transfer function:

$$V_{out} = -\frac{R2}{R1} \times V_{in} + \left(\frac{R3}{R3 + R4}\right) \times \left(1 + \frac{R2}{R1}\right) \times V_{shift} \tag{2.8}$$

The third topology is very suitable, but it might be even improved. At this point, it is known that we want to use a DAC as the shifting voltage source. By doing so, the voltage divider $R3$, $R4$ is not needed any more, since the shifting voltage will be adjusted by the DAC, not by the resistor divider. Figure 2.8 shows improved or better said - simplified third topology of voltage level shifter. [7]

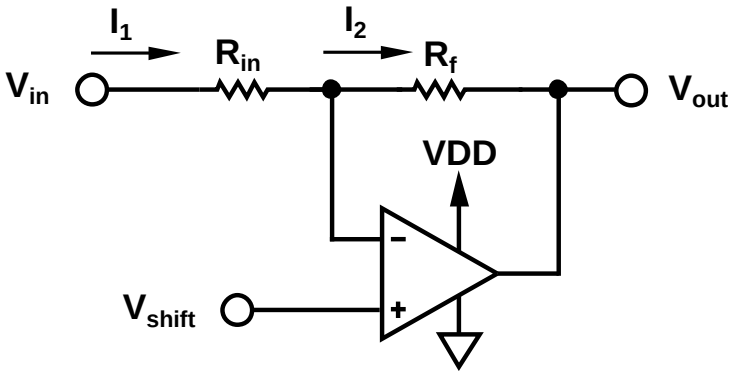


Fig. 2.8: Voltage level shifter

By applying the op amp laws to the schematic shown on figure 2.8, we can derive the transfer function of this topology. Let us start with comparing currents I_1 and

I_2. While we have ideal op amp, no current flows into inverting input of op amp, which means that currents are equal: $I1 = I2$. Which also means, that there is no voltage difference between non-inverting and inverting input and voltages on both inputs are equal. Now we can transform current equation to voltages and modify it to an equation 2.9:

$$\frac{V_{out} - V_{shift}}{R_f} = \frac{V_{shift} - V_{in}}{R_{in}} \tag{2.9}$$

$$V_{out} = (V_{shift} - V_{out})\frac{R_f}{R_{in}} + V_{shift} \tag{2.10}$$

$$V_{shift} = \frac{V_{out} + V_{in}(\frac{R_f}{R_{in}})}{1 + \frac{R_f}{R_{in}}} = \frac{V_{out} + V_{in} \times G}{1 + G} \tag{2.11}$$

The equation 2.10 is in a form of the well-known linear function $y = ax + b$. By comparing those two equations is clear, that the output common mode voltage depends solely on the voltage V_{shift}, the slope depends on subtraction of the voltages V_{shift} and V_{in} and the gain depends on ratio between R_f, R_{in}. The final equation 2.11 will be used, whenever the exact shifting voltage needs to be calculated.

2.5.5 Design of the voltage level shifter

The topology has been chosen, and the only thing what has left on the first stage block design is the attenuation level and the cutoff frequency of the pole for stronger anti-aliasing.

Starting with the attenuation 0.3 of the shifting op amp will give us maximum shifting voltage of $4.92\,V$ at the maximum input voltage level with $13\,V$ of DC offset according to the equation 2.11, but it attenuates the maximum input amplitude from $\pm 10\,V$ to only $\pm 3\,V$ which leads to loss the SNR since the ADC's full-scale range is $\pm 4.096\,V$.

Decreasing the attenuation to 0.35 in order to improve the SNR and improve the stability of the shifting op amp would cause the shifting voltage to be required more than $5\,V$ at the maximum input signal DC offset at $13\,V$ which is not acceptable, since the supply rail of the analog front-end is required to keep at $5\,V$.

Increasing the attenuation to 0.4 will cause the shifting op amp to be more unstable and will unnecessarily lower the amplitude, which has to be corrected to ADC's full-scale anyway.

The 0.3 attenuation turned out to be the best compromise. The SRN will be corrected in the next stage, where a small gain will be applied to maximize the input amplitude, to widen the amplitude from the first stage between the negative and

positive full-scale range of the ADC: $\pm 4.096\,V$. Applying the gain to the second stage would gain not only the input signal but noise from the input as well, thus keeping the first's stage noise of the signal chain at a low level is very important.

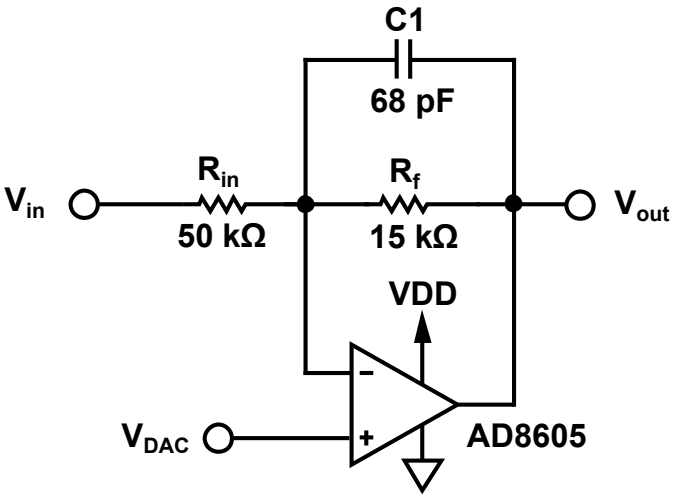


Fig. 2.9: Final design of the level shifter

The figure 2.9 depicts the final level shifter design with a capacitor in the feedback path creating a pole which strengthens the anti-aliasing effect and will be covered in a following section 2.6. The resistors values have been proposed, but the final decision about the values will be analyzed in a following subsections 2.5.6, 2.5.7 and 2.5.9.

The AD8605 has been chosen mainly due to its RRIO (Rail-to-Rail Input and Output) feature, high stability at unity gain and the fA input bias currents. The noise of the op amp is slightly higher than a noise of other op amp classified as a "low noise" ones, due to the RRIO which had higher priority than in choosing a suitable op amp for the first stage of the signal chain.

2.5.6 Input impedance

When interfacing a considerably high impedance output sensor, like the PCB 333B53 is, having the maximum output impedance of $500\,\Omega$, the input impedance of the signal chain must not limit the performance of the sensor. By not limiting the performance of the sensor is meant creating a voltage divider consisting of the sensor's output impedance R_s and the signal chain's input impedance R_{in}. Consequently, ensuring a maximal voltage drop across the input impedance and minimal across the R_s according to a following equation:

$$Input\,acuraccy\,error\,[\%] = 100\% - \frac{R_{in}}{R_{in} + R_s} \times 100 \tag{2.12}$$

The input impedance was proposed to be $50\,k\Omega$ which, according to the above equation 2.12 produces total accuracy error less than 1 %. Please note, that the 500Ω of sensor's output impedance is the worst-case scenario and the impedance is usually much lower.

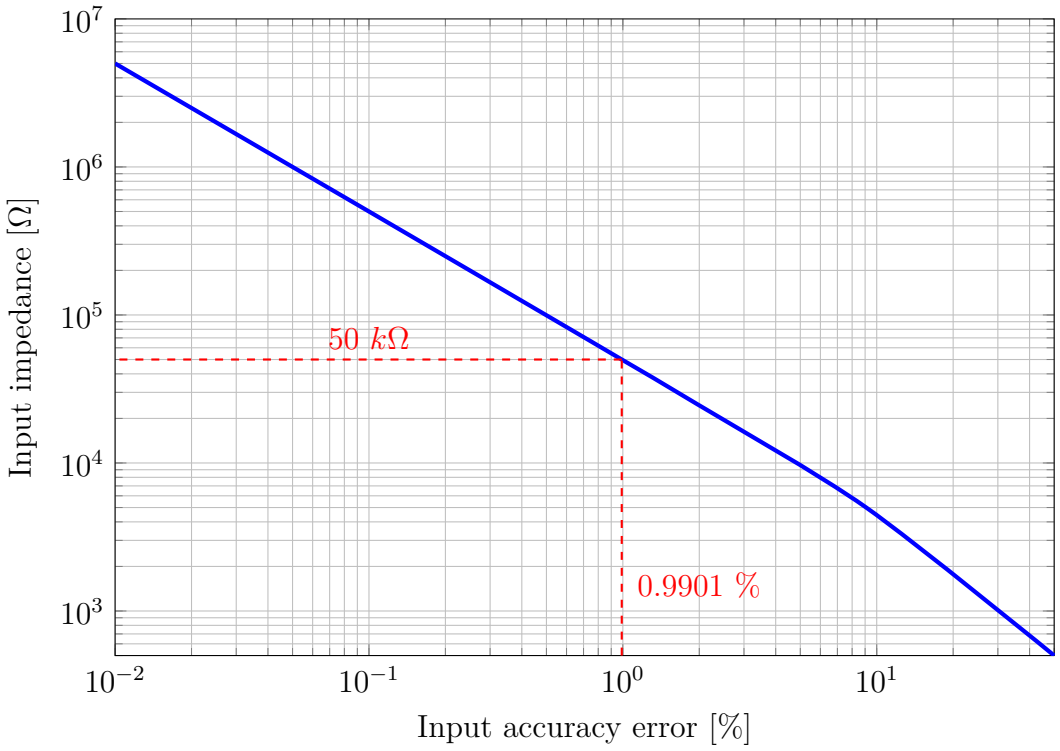


Fig. 2.10: Simulated input accuracy error for various input impedance

The chart above shows input impedance vs accuracy error on log-log scale simulated in the TLSpice. Accuracy error less than 1 % is very good result for that simple first stage. At this point it is difficult to say whether the error is acceptable or not and more evaluation measurements are required to decide it. As it is visible from the chart, doubling the input impedance to $100\,k\Omega$ would halve the input error down to about 0.5 %, but increase the first's stage noise considerably.

Thus, the input accuracy error is not the only concern when choosing the input impedance. Lowering the overall noise has a higher priority than a minor improvement of the accuracy, thus the impedance might not be changed even after the evaluation measurements after-all. A below subsection 2.5.9 deals with the input impedance related noise consideration.

2.5.7 First's stage noise calculation

The noise consideration of the CCS has already been simulated and described in the subsection 2.4.1 above. Now, a voltage noise of the level shifting structure depicted on the figure 2.9 with shorted inputs to the ground will be discussed. Shorting the inputs will simplify the noise formula and will give us an imagination about the noise level contributed solely by this structure. A following equation can be used for calculation of the voltage noise spectral density contributed by the level shifter:

$$e_{n,total}\,[VRMS] = \sqrt{(e_{n,WB})^2 \,+\, (e_{n,1/f})^2} \tag{2.13}$$

where $e_{n,WB}$ is the wide band noise and $e_{n,1/f}$ is the low frequency $1/f$ noise, which is usually lower compared to the wide band noise, but should not be underestimated.

1/f noise calculation

Starting with the $1/f$ noise, which is usually specified in data sheets as a V_{Pk-Pk} noise withing the bandwidth from $0.1\,Hz$ to $10\,Hz$, we can simply convert the V_{Pk-Pk} into $VRMS$ using a following formula:

$$e_{n,1/f}\,[VRMS] = \frac{e_{n,1/f}\,[V_{Pk-Pk}]}{6.6} \tag{2.14}$$

The AD8605 has quite a high $1/f$ noise of $2.3\,\mu V_{Pk-Pk}$ due to its RRIO ability. Thus, after substituting into the equation 2.14, we would get:

$$e_{n,1/f} = \frac{2.3\,[\mu V_{Pk-Pk}]}{6.6} = 348.5\,nVRMS \tag{2.15}$$

Wide band noise calculation

The $1/f$ noise has been set, now the wide band noise will be covered. The wide band noise has more sub-contributors, depending on a schematic. A below formula has been created using following notes ensuring a correct noise calculation [8, 9]:

$$e_{n,WB}\,[nV/\sqrt{Hz}] = \sqrt{(G \times e_{n,R_in})^2 + e_{n,R_f}^2 + (NG \times e_{n,AD8605})^2 + (NG \times e_{n,IN-})^2} \tag{2.16}$$

The e_{n,R_f}^2 and the e_{n,R_in}^2 are voltage noise densities contributed by the thermal noise of the resistors R_{in} and R_f. The thermal noise of a resistor is set as:

$$u_{noise}\,[V/\sqrt{Hz}] = \sqrt{4 \,\times\, k \,\times\, T \,\times\, R} \tag{2.17}$$

where k is the Boltzmann's constant, T is a temperature in Kelvins and R is the resistance, thus after a substitution:

$$e_{n,R_in} = \sqrt{4 \times k \times 237.15 \times 50\,k\Omega} = 27.46\,nV/\sqrt{Hz} \tag{2.18}$$

$$e_{n,R_f} = \sqrt{4 \times k \times 237.15 \times 15\,k\Omega} = 15.04\,nV/\sqrt{Hz} \tag{2.19}$$

To continue with the analysis of the equation 2.16, the $e_{n,AD8605}$ is the voltage noise density of the op amp AD8605 taken from the data sheet and it's typical value being $8\,nV/\sqrt{Hz}$ for mid-low frequencies around $1\,kHz$ and the $e_{n,i}$ is the input current noise density of the AD8605 [10]. The current noise density of the AD8605 is transformed into a voltage noise density as [8]:

$$e_{n,IN-} = i_{n,AD8605} \times R_f \,||\, R_{in} \tag{2.20}$$

where the $i_{n,AD8605}$ is the input current noise density of the AD8605. This noise current flows to the negative input of the op amp trough the parallel combination of both resistors, the R_f and the R_{in}, where the noise current density is being transformed to the voltage noise density for this calculation. The value of the current noise density si taken from the AD8605 data sheet, being as low as $10\,fA/\sqrt{Hz}$ thanks to an input stage offering a very high input impedance [10]:

$$e_{n,IN-} = 10\,fA/\sqrt{Hz} \times 50\,k\Omega \,||\, 15\,k\Omega = 115.3\,pV/\sqrt{Hz} \tag{2.21}$$

As visible from the equation 2.16, each contributor is multiplied either by the noise gain NG, signal gain G or by 1. It is because each one is gained to the output differently. The topic of gaining each contributor is covered in [8, 9]. The signal gain is calculated as simple as a ratio of the R_f and R_{in} being 0.3. The noise gain has already been covered in the equation 2.7, thus after substitution:

$$NG = 1 + \frac{R_f}{R_{in}} = 1 + \frac{15\,k\Omega}{50\,k\Omega} = 1.3 \tag{2.22}$$

Substituting all known parameters in $nV/\sqrt{Hz}$ units to the formula 2.16 would give us the final wide band voltage noise spectral density:

$$e_{n,WB} = \sqrt{(0.3\times27.46)^2 + 15.04^2 + (1.3\times8)^2 + (1.3\times0.115)^2} = 20.06\,nV/\sqrt{Hz} \tag{2.23}$$

The total wide band voltage noise density has been set, now the total integrated noise over a specific bandwidth can be calculated as:

$$e_{n,WB}\,[\mu V\,RMS] = e_{n,WB}\,[nV/\sqrt{Hz}] \times \sqrt{\frac{\pi}{2} \times \frac{1}{2\pi R_f C_f}} \tag{2.24}$$

The final integrated wide band voltage noise is set by the equation 2.24, where the first order low-pass filter created by the R_f and the C_f filters a huge portion of voltage noise out of the bandwidth of interest. The $\pi/2$ is an equivalent noise bandwidth correction factor for 1^{st} order filter. After substituting:

$$e_{n,WB} = 20.06\ nV/\sqrt{Hz} \times \sqrt{\frac{\pi}{2} \times \frac{1}{2\pi \times 15\,k\Omega \times 68\,pF}} = 9.93\,\mu V\ RMS \qquad (2.25)$$

The resulting noise given by the above equation 2.25 will give us an rough imagination about the noise levels present in the system. The above calculations are valid, but only for a very specific bandwidth. A next subsection analyzes the noise distribution over a wider bandwidth.

2.5.8 First's stage noise bandwidth of interest

Calculation from the previous subsection are valid, only when assuming the noise falls with a slope of $-20dB\,/\,Decade$ after the cutoff frequency, but it is not a case. Since at this point it is very difficult to make a hand calculation of the noise distribution as explained in [9]. The actual noise distribution will only be outlined in following lines, as it is important to understand the system, where the noise is coming from and how to limit it.

Looking at the schematic from the figure 2.9 we must consider the noise gain and the signal gain being dependent on the frequency, since there is a capacitor in the feedback loop we can adjust those two equations as:

$$NG = 1 + \frac{Z_f}{Z_{in}} = 1 + \frac{R_f \mid\mid X_{C_f}}{R_{in}} \qquad (2.26)$$

$$G = \frac{Z_f}{Z_{in}} = \frac{R_f \mid\mid X_{C_f}}{R_{in}} \qquad (2.27)$$

where the X_{C_f} is a frequency-dependent impedance of a capacitor, already defined by the equation 2.5. This means, that the noise gain NG will be approaching to value 1 and the signal gain to 0 as the frequency increases further even after the cutoff frequency. By applying the changes for higher frequency spectrum into the equation of the wide band voltage noise density 2.16 we would get:

$$e_{n,WB,hf}\,[nV/\sqrt{Hz}] = \sqrt{(1 \times e_{n,AD8605})^2 + (1 \times e_{n,IN-})^2} \qquad (2.28)$$

The $e_{n,Rin}$ is out of the equation after multiplying by 0, the $e_{n,Rf}$ is shorted by the C_f for the higher frequencies, thus its noise voltage is shorted as well. As a conclusion, only $e_{n,IN-}$ and $e_{n,AD8605}$ remain in the original formula for the higher

frequencies. We can even skip the $e_{n,IN-}$, having only negligible impact and the resulting formula would be as simple as:

$$e_{n,WB,hf}\,[nV/\sqrt{Hz}] = e_{n,AD8605} \tag{2.29}$$

The above equation 2.29 is however valid for a very specific bandwidth, as will be explained later in this subsection.

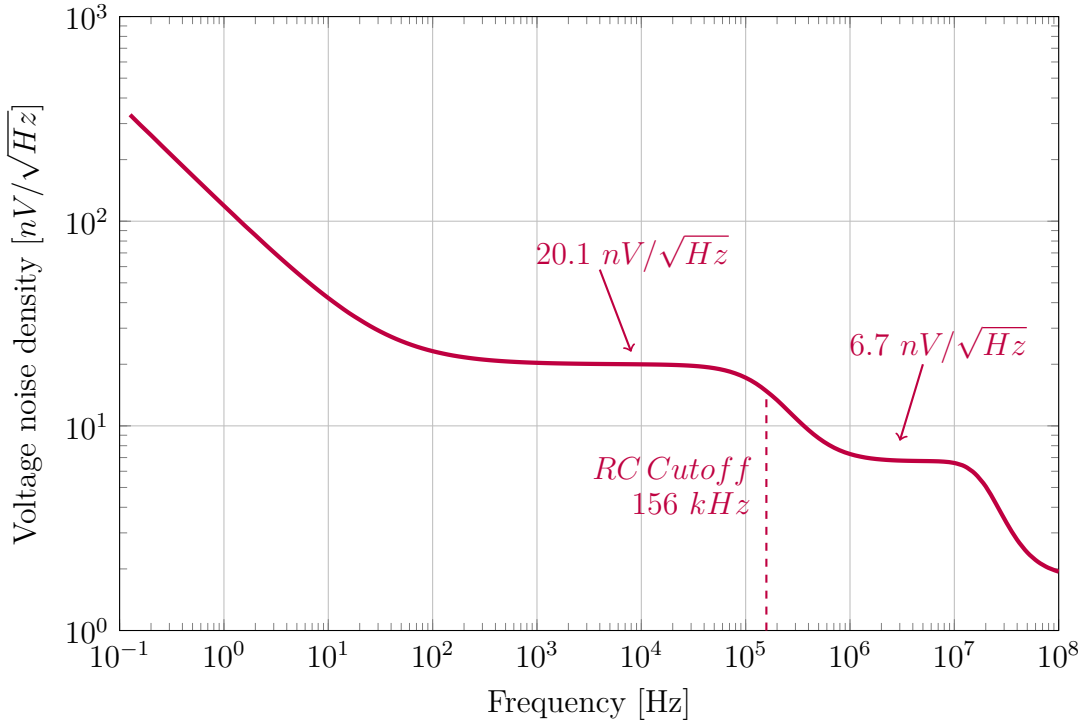


Fig. 2.11: Simulated wide band noise of the level shifter

The above figure 2.11 depicts simulated noise spectral density from a schematic at the figure 2.9, using a noise analysis in the TLSpice simulation software. A shape of the plot consists of 6 areas:

firstly it is the $1/f$ noise dominating at very low frequencies produced by semiconductors, secondly there is the flat area of white noise which depends on the noise of the op amp itself, but mainly on the thermal noise of the resistors, being the most significant noise contributors as seen from the subsection 2.5.7. The voltage noise spectral density of this area is calculated in 2.23, being approximately $20.1\,nV/\sqrt{Hz}$ as same as marked in the plot.

The 3^{rd} area is the RC filter roll-off which occurs at about $165\,kHz$, followed by an area after which the equation 2.29 starts to be valid. This is the area near the second corner frequency, where the $-20dB\,/\,Decade$ slope starts to flatten due to remaining $e_{n,AD8605}$ white noise. Position of this area depends on used parts values.

As the 5^{th} area, the second flat region occurs. It is caused by remaining noise gain and is equal to $6.7\,nV/\sqrt{Hz}$ which is very close to a typical voltage noise density from the AD8605 data sheet for frequencies at around $10kHz$ and higher, which proving the theory explained in this subsection. [10]

As further visible from the figure, there is the last area, the second slope after a frequency of $10\,MHz$ which is a limitation of the op amp, having the gain bandwidth product break point at about this frequency. The noise starts to fall rapidly.

To filter out the op amp's noise at lower frequencies (around the RC cutoff frequency) it is necessary either to use an external low-pass passive filter, which is due to increase of a system's offset and decrease of the shifting op amp stability not advised, or a second filtering stage might be used. In our case the next filtering stage is an AAF, which actively filters out the first's stage noise at the higher frequencies.

2.5.9 First stage noise

As the AD8605 used in te level shifter is an ultra-low noise op amp, we can see, that the biggest noise contributor is going to be the feedback resistors having resistance tens of kilo ohms. A following set of simulation for various input impedance was executed and depicted in a following chart.

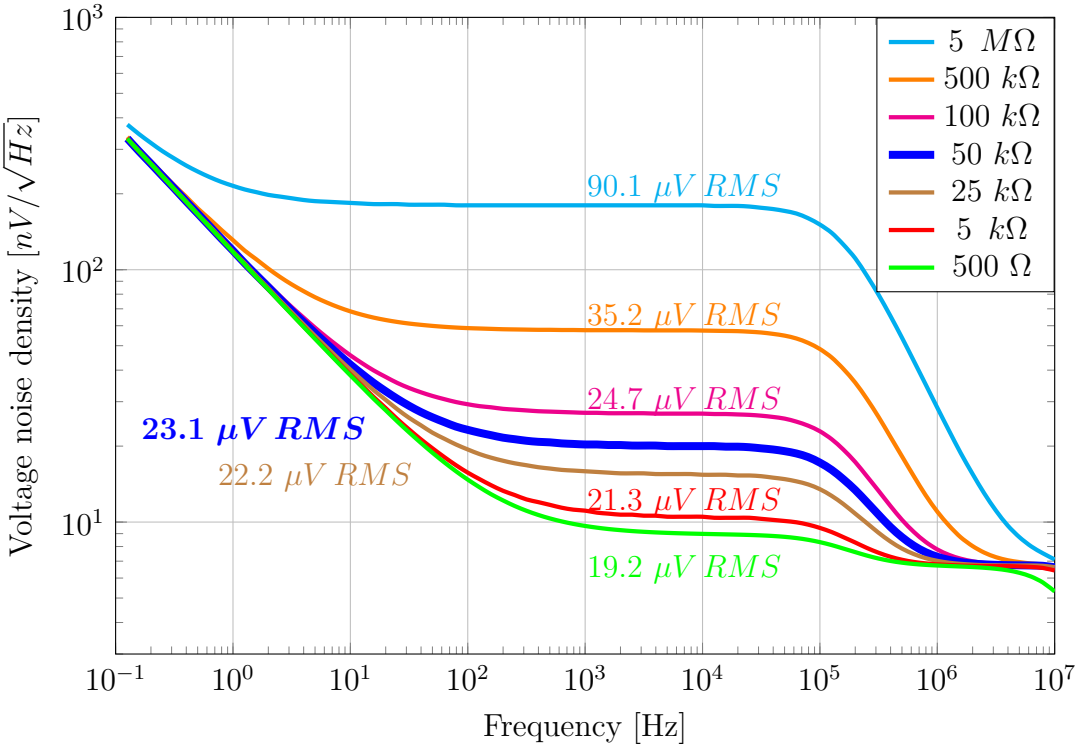


Fig. 2.12: Simulated wide band noise of the level shifter for various input impedance

A schematic from the figure 2.9 was simulated in LTSpice using noise analysis to fill the chart 2.12 above. Not only the R_{in}, representing the input impedance, was altered, but all the passive components with respect to the gain and cutoff frequency.

As visible from the chart, the resistor's thermal noise does affect the overall noise performance of the first stage significantly. In the subsection 2.5.6 it was proposed to choose the R_{in} to be $50\,k\Omega$ as a starting point. Going any lower than $50\,k\Omega$ with the R_{in} would increase the input accuracy error above 1%. To fulfill needs of the precise measurement demand, increasing the accuracy error with an intention of lowering the overall noise is not advised, but evaluation measurements are required to find out the capability of the system in this configuration. Thus, we can work with the value of $50\,k\Omega$ as the input impedance.

Comparing the simulated integrated noise result with the calculated one from the equation 2.25 is telling us, that the real wide band integrated noise is more than 2-times higher than the hand calculated one, where one would more likely to fail in assumptions about the wide band noise. The noises would be same if we set the stop frequency of the noise simulation to the flattening region which has been explained together with the figure 2.11. In our case, the next stage with the AAF will filter out the remaining op amp's noise even more aggressively.

2.6 Anti-aliasing filter

In order to protect the input of the ADC from unwanted high frequency signals, which might ruin the sampling process an anti-aliasing filter was engaged between the first stage of the signal chain and the ADC.

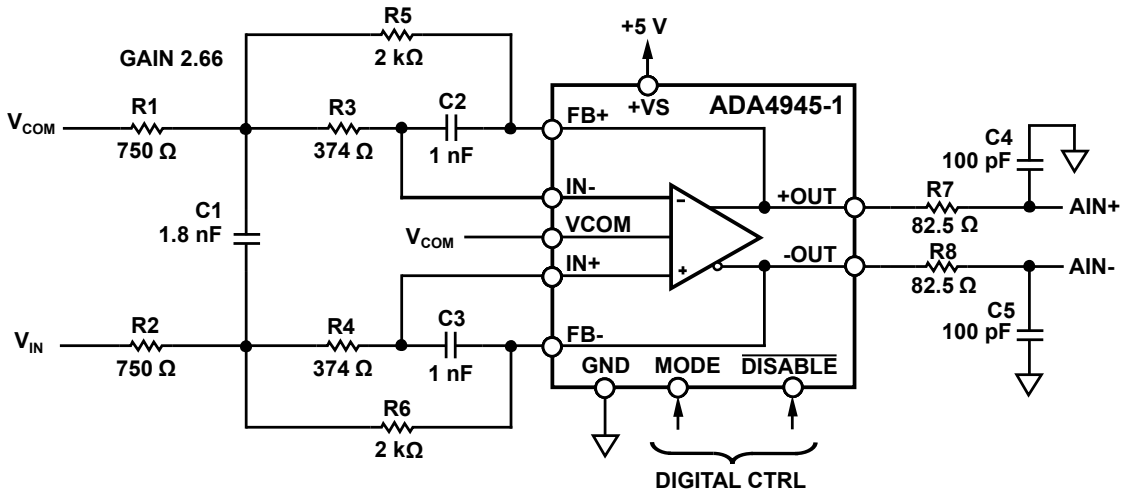


Fig. 2.13: Active 2^{nd} order differential multiple feedback anti-aliasing filter

The figure 2.13 shows a schematic of used AAF, which is a 2^{nd} order differential low-pass filter, using a multiple feedback topology and Butterworth-Bessel characteristic. The multiple feedback topology was chosen for its high-frequency stability and ability to transform a single-ended filter design into a differential one with ease. The low-q Butterworth-Bessel characteristic ensures a very smooth roll-off without any peaking in the frequency response. A more aggressive filter characteristic comes with additional peaking in the pass-band spectrum which might ruin the measurement. Since there are not as tight requirements for filtering the 2^{nd} Butterworth-Bessel characteristic gives us enough of filtering and nicely smooth pass-band as well as roll off.

Any resistor in the signal path impose noise and errors, especially offset errors in a form of voltage dropout across a resistor, when the currents are expected to be significantly higher. Keeping the resistor values small enough is essential. Passive component tolerance in the differential mode is important to lower the $CMRR$, thus resistors with 0.1 % and capacitors with 1 % relative tolerance were used for the AAF design.

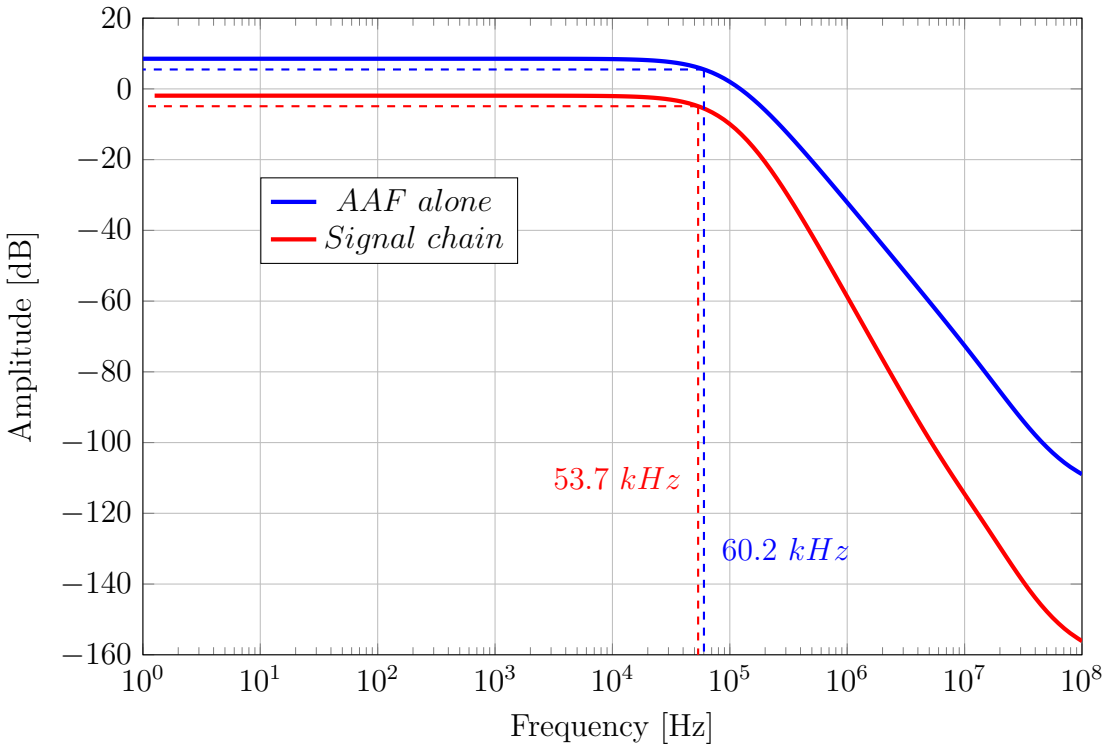


Fig. 2.14: Frequency responses of the AAF alone and the full signal chain

Frequency response of the full signal chain was simulated using the LTSpice using an AC analysis. An unified AC source was used for the frequency response measurement, shown in the figure 2.14 above having two separate readings with

different gains. The blue reading is simulated schematic from figure 2.13 and the red one is the full signal chain featuring the first stage from the figure 2.9 and the AAF itself. The resulting cutoff frequency was desired and designed to be around $50\,kHz$, its exact value is not crucial.

The stop-band was desired to be at least $-80\,dB$ at the $MCLK$ frequency of $16.384\,MHz$ to sufficiently reject the f_{MOD} and the $MCLK$ which are the same frequencies for the $MCLK_{DIV}$ factor to be 2. Thus, for the ADC in the fast mode.

The AAF alone (blue line) offers almost $-90\,dB$ of rejection at $16\,MHz$. Even better rejection of almost $123\,dB$ offers the full signal chain with one additional pole from the first stage, making the AAF a $3-pole$ filter in total.

Please note, that the rejection achieved by the analog AAF si even more enhanced by a digital filtering in the ADC. In this case a $64-order$ digital FIR filter was used for the vast majority of measurement, having the lowest ripple in the pass-band an maximizing the anti-aliasing protection. The FIR filter is intended to be used in precise measurements because of its quite long delay. On the other hand, a SINC filter (also available in the AD7768-1) is generally used for very wide bandwidth. [11]

The ADA4945-1 has been chosen as the active element in the filter design, not only in order to promote new products, but mainly due to its excellent linearity making it one of the top FDA's on the market right now. As visible from the figure 2.14, the FDA features with two power modes which are digitally accessible from the outside. Switching between the modes changes specifications of the FDA like consumption, bandwidth, linearity etc.

The output RC network from schematic 2.13 consisting of $R7$, $R8$, $C4$ and $C5$ performs a couple of tasks. The reason of employing the RC network between the FDA and the ADC is explained in [12]. The application note deals with the driving op amp selection as well.

2.7 Level shifting DAC

In order to achieve a fine calibration step, at least 16-bit DAC should be chosen. Choosing more than 16-bit DAC might be redundant since the sensor itself has a quite high level of voltage noise and the last LSBs of the DAC might be lost in the noise during the bias compensation process. To sustain a daisy-chain ability the I^2C is an ideal preference, since setting the output voltage of the DAC is not speed demanding. An DAC with very low 1/f noise is extremely important.

By substituting the sensor's bias voltage upper and lower ranges into the equation 2.11, the exact shifting voltages applied to the non-inverting input of the shifting op amp needed to fully cover the sensor's range will be set:

$$V_{shift,low} = \frac{2.5 + 7 \times 0.3}{1 + 0.3} = 3.53\,V \tag{2.30}$$

$$V_{shift,high} = \frac{2.5 + 12 \times 0.3}{1 + 0.3} = 4.69\,V \tag{2.31}$$

As visible from the above equations, the upper shifting voltage limit, which is needed to shift $12\,V$ senor's bias voltage down to $2.5\,V$ is about $4.7\,V$. Adding another (already 3^{rd}) reference voltage IC into the design would be irresponsible and would increase the cost tremendously. The best thing to do here, is to share the reference voltage output.

The highest reference voltage output already used in the design is the $4.096\,V$ output used by the ADC. The DAC output voltage must be therefore gained to fulfill the shifting range demanded. Theoretically a gain of 1.41 would be enough, but as nothing in this world is ideal, a decision has been made to apply a gain of 1.21, covering the full $0\,V\ -\ 5\,V$ shifting voltage range. Which might allow us to use a different sensor type with a slightly higher range of the bias voltage.

$$LSB_{DAC} = \frac{4.096\,V}{2^{16} - 1} \times 1.22 = 62.5\,\mu V \tag{2.32}$$

$$Total\ LSB_{DAC} = \frac{4.096\,V}{2^{16} - 1} \times 1.22 \times 1.3 \times 2.667 = 264.37\,\mu V \tag{2.33}$$

An LSB of the DAC with gained output is set by the equation 2.32, but the real LSB step "seen" by the ADC is set by the equation 2.33 because there are other gains in the path between the DAC output and the ADC input. Where the gain of 2.667 is the gain of the FDA and the gain of 1.3 is the gain of the shifting op amp, which acts like a non-inverting op amp in this case when a changing signal is brought to the non-inverting input and the actual gain is $1 + (R_f/R_{in})$. The above calculation gives us the maximal theoretical DC error caused by shifting the sensor's bias voltage.

To fulfill the above mentioned demands, a voltage output DAC LTC2606 with $15\,\mu V_{P-P}$ of voltage noise at the corner frequency of $10Hz$, external reference input, separate supply voltage and a I^2C bus has been chosen.

2.7.1 DAC buffer

As mentioned, the buffer must be employed to gain the DAC output voltage. It even might be used as an active filter, filtering the voltage noise coming out of the DAC output. As we do not need the DAC to provide us with the wide bandwidth signals, the DAC output bandwidth can be limited by a filter down to DC level, lowering the voltage noise.

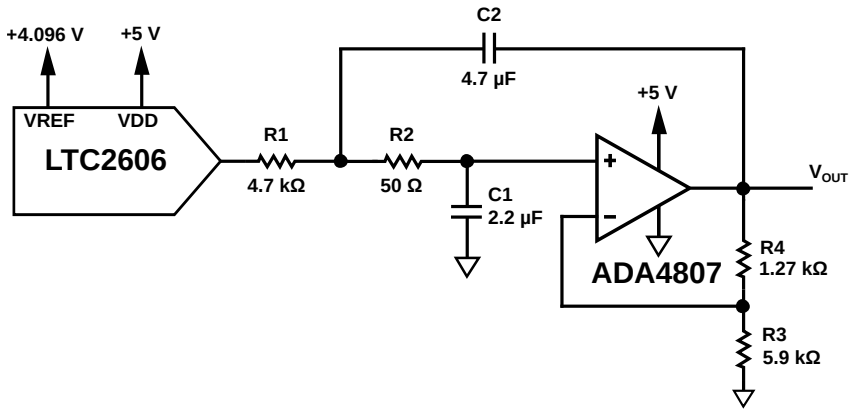


Fig. 2.15: DAC buffer with a low-pass Sallen-Key filter

The figure 2.15 above displays the DAC LTC2606 with the buffer in a gained Sallen-Key structure. The op amp used as the filter and the buffer is an ADA4807 which is a low power, very low noise, RRIO operational amplifier combining high speed and DC precision in one device. With its $1/f$ noise of 160 nV_{p-p} and RRIO configuration makes it a perfect fit for buffering the DAC output. The ADA4807 has been broadly used as a buffer across the business unit.

It is important to choose appropriate resistor and capacitor values. Selecting large resistor values causes an increase in the thermal noise. Also, the input structure of the ADA4807 causing a higher bias current flowing through the resistors into the inputs of the op amp, which leads to higher offset.

The resistors and capacitors are very important in determining the performance over manufacturing tolerances, time and temperature. At least 1% or better tolerance resistors and 5% or better tolerance capacitors are recommended for single-ended signal path.

$$f_c = \frac{1}{2\pi \sqrt{R_1 \times R_2 \times C_1 \times C_2}} \tag{2.34}$$

For the needs of limiting the noise, the easiest Sallen-Key structure has proven itself to be sufficient in other designs. The exact cutoff frequency is not crucial for this filter and has been experimentally set to 100 Hz using the above formula 2.34. The cutoff might have been even lover to achieve a better noise performance but the filter is only a 2-pole filter which might lead to phase delay problems by pushing the $-3dB$ point too close to the desired pass-band areal.

2.7.2 Stability of the DAC buffer

Besides the cutoff frequency of the buffer's filter, its stability must be taken care of since the gain is applied to the Sallen-Key low-pass filter topology. This particular topology is very likely to oscillate, when the stability is not being handled.

To ensure the stability of the buffer, the quality factor Q must remain positive, thus keeping the poles of the filter at the left side of the s-plane. Otherwise the circuit will oscillate. As the Q rises, the filter has better selectivity, but also higher resonance at the cutoff frequency causing the response in the pass-band not to be flat. The linear pass-band is more important, thus keeping the Q positive and close to zero is crucial.

$$Q = \frac{\sqrt{R_1 \times R_2 \times C_1 \times C_2}}{R_1 \times C_1 + R_2 \times C_1 + R_1 \times C_2 \times (1 - k)} \tag{2.35}$$

$$k = 1 + \frac{R_4}{R_3} \tag{2.36}$$

The equation 2.35 defines the Q factor of the schematic from the figure 2.15 and the equation 2.36 sets the k factor, which is the gain of the buffer. The Q is set and calculated according to the above equations to: $Q = 0.273$. This way both, the stability and the low resonance at the cutoff frequency is ensured. [13]

2.8 Voltage reference

Each design with an ADC must feature with a voltage reference, providing the ADC with an extremely stable and clean reference voltage. Sometimes, when an excellent performance is expected a low-pass filter is inserted between the ADC and the reference chip to filter out the already low voltage noise even more.

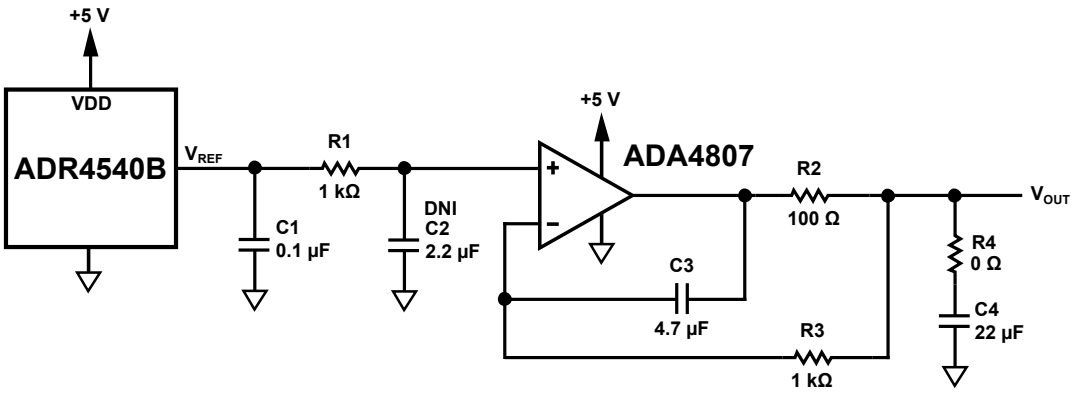


Fig. 2.16: Buffered voltage reference with a low-pass filter

The figure 2.16 depicts an extreme low noise reference voltage chip ADR4540B with a low-pass active filter featuring an RRIO op amp dedicated for active filtering. The $C1$ maintains stability of the ADR4540B and filters out the voltage noise. Must be a high-quality capacitor, not allowing the leakage current to affect the output reference voltage. The $R1$ lowers the output noise current from the reference chip. If desired, the $C2$ could be placed in order to create an additional passive low-pass filter in connection with the $R1$.

The rest of the part values were designed according to an application note [14]. As the application note offers a solid active low-pass filter design. Resistor $R4$ could be placed, in case of a stability issue where the op amp might have difficulties with driving a large capacitor on the output.

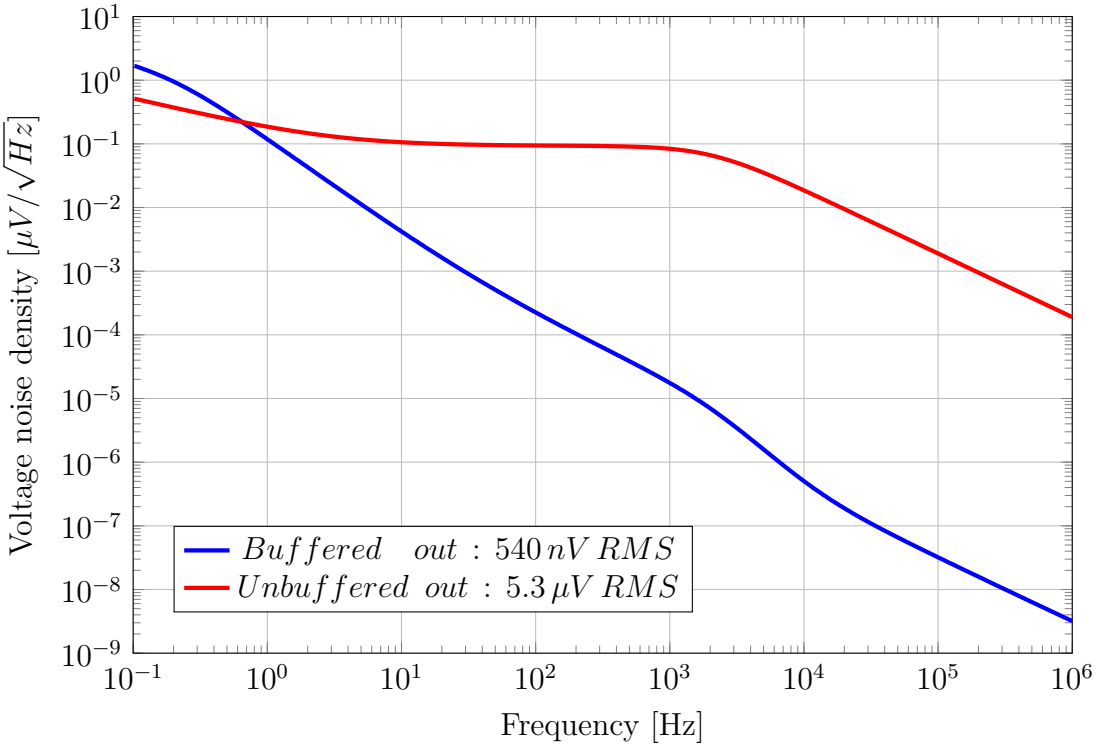


Fig. 2.17: Simulated voltage noise of buffered and unbuffered reference output

The figure 2.17 above depicts a simulated voltage noise difference between the buffered voltage reference from the figure 2.16 and an unbuffered output of the voltage reference ADR4540B. A noise analysis in the TLSpice software was used for the simulation. The buffered reference output enabled us to lower the total integrated noise almost 10-times. To satisfy the needs of the ADC reference input, it is important to keep the wide band noise low, thus the increase of the $1/f$ noise at the very beginning of the blue reading caused by the op amp itself will not affect the overall noise performance much.

2.9 Analog to Digital Converter

To decide which ADC to choose from the two biggest ADC families, the SAR ADC and the Sigma-Delta ADC we must consider a huge amount of factors like a bandwidth of interest, linearity, harmonic distortion, digital signal prost-processing, acceptable system noise, dynamic range etc.

As this thesis does not deal with the ADC to application fitting at first place only the basics will be outlined. The desired bandwidth of interest is very low for the vibration monitoring, an ADC with a few hundred of KSPS would be enough. A digital post-processing in form of a digital filtering is required to achieve a wide dynamic range allowing us to reveal any defect in the very initial stage. From what we already know, a Sigma-Delta ADC is the best fit for now.

As there are dozens of Sigma-Delta ADC offered by the Analog Devices, using a newly released parts is always promoted in order to show a capability of such a new parts. A 24-bit Sigma-Delta ADC AD7768-1 has been chosen mainly because of its excellent linearity, wide dynamic range and low harmonic distortion. [11]

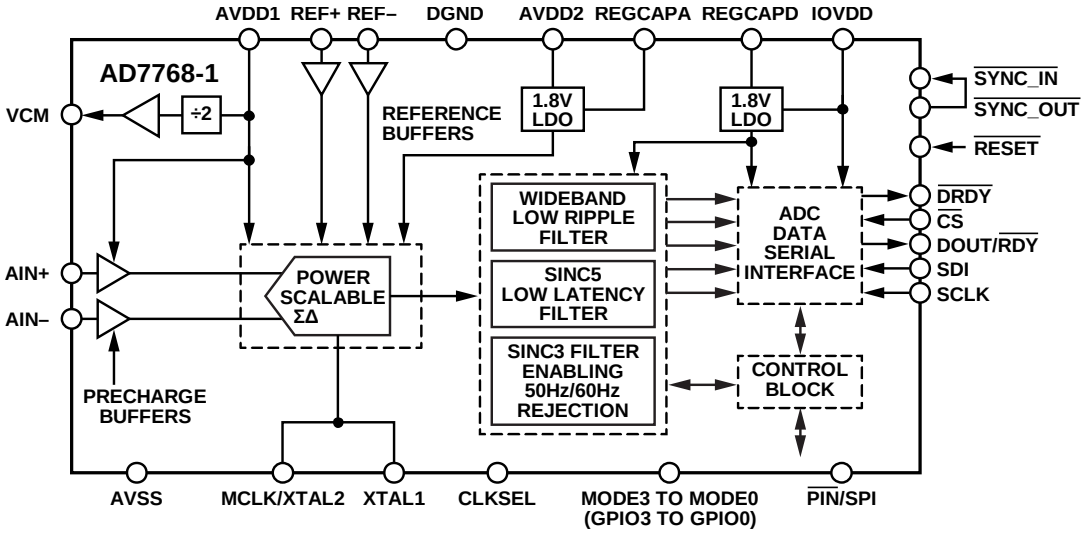


Fig. 2.18: AD7768-1 internal block diagram [11]

The figure 2.18 depicts internal structure of the Sigma-Delta ADC AD7768-1. As visible from the diagram, the ADC is a single channel, with several internal digital filters, reference and analog inputs are supplemented with precharge buffers and the SPI bus is used as an interface for communication. [11]

Output data rate of the AD7768-1 is set by a following equitation:

$$ODR_{AD7768-1} = \frac{f_{MCLK}}{MCLK_{DIV} \times Filter_{dec}} \tag{2.37}$$

where f_{MCLK} is the master clock frequency, $MCLK_{DIV}$ is the master clock divider set by an used power mode of the ADC and $Filter_{dec}$ is the decimation ratio of an used filter. [11]

2.10 Sensor bias compensating technique

If the DC coupling is used in a signal chain the input voltage is DC-shifted to a certain level. By doing so, an ADC ideally "sees" only the AC part of the input voltage without any DC offset. A precise DC-shifting is crucial for an accuracy in the DC and very low frequency measurements.

An exact shifting voltage need for a given input bias voltage can be found out using the equation 2.11. Following this approach, numbers of measurements at different temperatures must be taken, for each board and sensor separately ensuing accuracy and repeatability of the measurements, making this approach rather theoretical than practical.

Totally different, more precise and reliable technique has been implemented in order to find an exact shifting voltage. A custom successive approximation algorithm (SA) has been employed to do the job. Since the standard SA model, widely used in - SAR ADCs, is estimating the final value of an unknown voltage level using an DAC – ADC control loop. This algorithm, however, is trying to push a mean value (a DC offset seen by the ADC) as close to zero as possible again, by using the DAC – ADC loop. In other words: the main goal is to set the both input of the driving FDA (fig. 2.2) to the same voltage level, which is in this case VCOM = $2.5\,V$.

The table 2.2 above shows a process of the sensor bias voltage compensation using the custom successive approximation algorithm. Since the 16-bit DAC has been chosen, there will be 16 iterations, each for one bit weight. The DAC is initially set to a half-scale output in the very beginning of the process. Every time the DAC is set to a new value, the mean voltage at the input of the ADC is measured by the ADC. If the mean voltage is positive, one bit weight is added to the current DAC output, otherwise one bit weight is subtracted from the current DAC output. The process is inverted due to the first input stage, which is an op amp in the inverting configuration.

$$5^{th}step : DAC_{CODE} = (2^{15} - 1) + 2^{14} + 2^{13} - 2^{12} + 2^{11} = 55295 \tag{2.38}$$

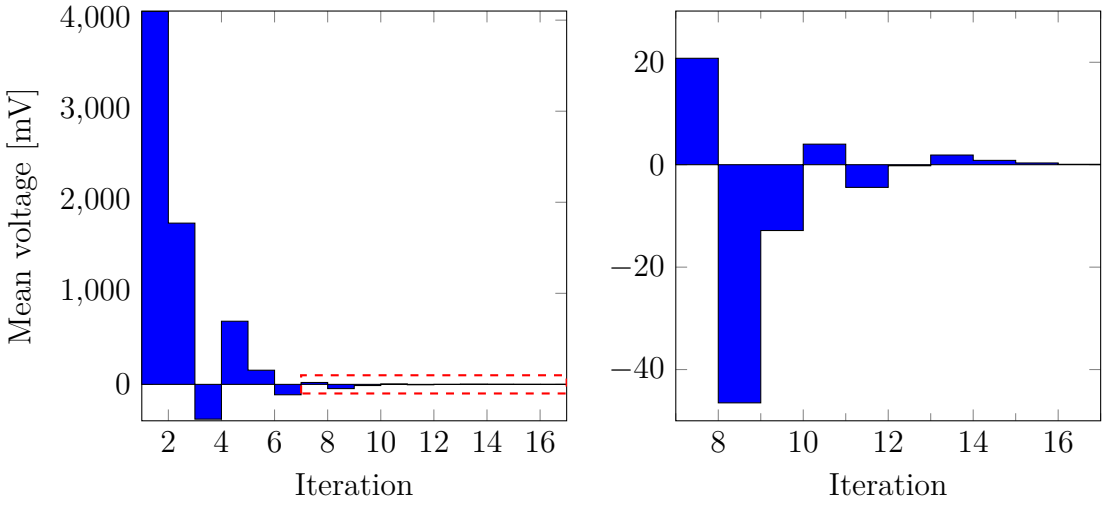
$$6^{th}step : DAC_{CODE} = (2^{15} - 1) + 2^{14} + 2^{13} - 2^{12} + 2^{11} + 2^{10} = 56319 \tag{2.39}$$

The above examples 2.38 and 2.39 show the bit weights being added or subtracted. In case of the 6^{th} step from the equation 2.39 the initial half-scale value $2^{15} - 1$ is

Tab. 2.2: Sensor bias voltage compensation process

Iteration	**DAC code [LSB]**	**Next move**	**Mean voltage [mV]**	**Shifting voltage [V]**
1	32767	UP	4095.99	2.499
2	49151	UP	1770.85	3.748
3	57343	DOWN	-381.94	4.372
4	53247	UP	693.44	4.061
5	55295	UP	155.42	4.216
6	56319	DOWN	-114.19	4.294
...	...	...	...	...
14	55883	UP	0.846	4.2611
15	55885	UP	0.338	4.2612
16	55886	FINAL	0.079	4.2613

followed by two “UPs” one “DOWN” and another two "UPs", which means that 14^{th} and 13^{th} bits are added, 12^{th} is subtracted, 11^{th} and 10^{th} are again added.



(a) Full compensation process

(b) Detailed cut of the process from the red dashed region

Fig. 2.19: Mean voltage levels during the bias compensation process

The plot 2.19 depicts gradual approximation of the mean voltage preset at the input of the ADC, beginning at the HS voltage and ending at less than $80\,\mu V$. The values are taken from the table 2.2.

The piezoelectric sensor itself produces a significant amount of voltage noise caused by the sensor's internal structure. An environmental noise is being picked up by the sensor once it is powered, resulting in even more noise converted from mechanical environmental events into the voltage noise. To extract only the DC bias voltage of the piezoelectric sensor and to remove quite significant amount of noise, lot of averaging is taking place during the DC-bias compensating process.

The AD7768-1's programmable SINC3 filter has been experimentally set to output data rate of $4\,Hz$ and up to 500 samples is being taken in order to properly perform the compensating process. The whole process takes several minutes, but once finished, the final value of the DAC code is stored and used for measurement. Keep in mind, that he bias voltage of the piezoelectric accelerometer is specific for each sensor and does not change over time.

2.11 Power supplies

The power supply system was designed, so it could be powered from any microcontroller or any FPGA development board providing a $3.3\,V$ output. The development board should be capable of delivering a current of $250\,mA$ or more from its $3.3\,V$ output.

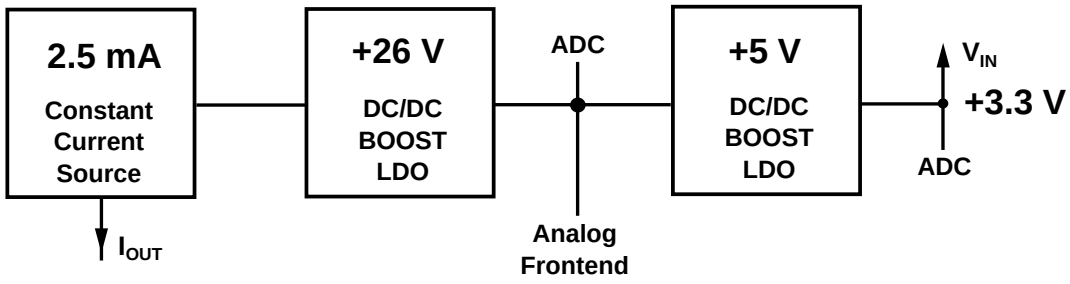


Fig. 2.20: Block diagram of the power section

As the figure 2.20 shows, the there are several boost DC-DC converters present on the PCB. Each converter was supplemented with an LDO lowering the voltage ripple produced by a converter. As the schematic A.1 shows, a headroom of $2\,V$ was chosen for the voltage ripple elimination for the sensor voltage source, ensuring enough noise reducing but a slightly higher power consumption produced by the LDO thermal dissipation. A user can bypass the section providing $5\,V$ output on the PCB, when such a voltage is present on the development board. But both, the $3.3\,V$ and the $5\,V$ voltage outputs are inevitable for the PCB.

3 Firmware design

The following chapter deals with the firmware design, explaining how the data are taken out of the ADC, processed by a digital host and displayed on a plot.

3.1 Frequency bin width

Whenever working with a frequency spectrum in general either in connection with the FFT, which is a special type of DFT, or with the DFT itself, a term 'frequency bin' must be defined, since it relates with a quantization of the spectrum.

$$Bin\,width\,[Hz] = \frac{f_s}{n} \tag{3.1}$$

The above equation 3.1 describes how the frequency bin width is defined, where f_s is the sampling frequency and n is the number of samples. Say, we have the sampling frequency of $1\,kHz$ and we take 100 samples, the frequency spectrum is divided into 100 even portions (frequency bins), where each bin represents an interval of $10\,Hz$, which is called a bin width. Thus, the frequency bins are quantified intervals of the frequency spectrum, separated by an even distances called the bin width.

The first frequency bin, the bin with the 0 index, in the frequency spectrum always belongs to the DC level present in the signal. Having a lower bin width increases the resolution of the frequency spectrum, allowing us to closely investigate the reconstructed shape of the input signal's spectrum.

3.2 ADC data format

Majority of precision AD-converters allow a user to read the data in two's complement form. The two's complement form must be converted to a signed integer form, which is more natural form of data for further investigation. As a following listing shows, the firmware was written in the C language.

Listing 3.1: Conversion from two's complement to signed integer

```
if(data[i] & 0x800000)                                    1
  shifted_data = (int32_t)((0xFF << 24) | data[i]);       2
else                                                      3
  shifted_data = (int32_t)((0x00 << 24) | data[i]);       4
```

The section of code from the listing 3.1 above explains a type conversion from the two's complement to the singed integer where *data[i]* is an array of the sampled

ADC codes and *shifted_data* is an auxiliary variable, into which the integer is stored. The *0x80* indicates a negative number in the two's complement and a sequence of *0xFF* is shifted into very beginning of a 32-bit integer variable making a negative integer number and the actual 24-bit ADC sample is pasted behind the *0xFF*. The AD7768-1 has a possibility to choose between either a 16-bit or a 24-bit data output length, but the above conversion routine is immune to different bit lengths.

3.3 FFT on DSP

Since this design is targeting a hand-held device, the FFT must be processed locally without any need of a PC. A digital host can process the data using either by a software (firmware) FFT or a hardware FFT. The software FFT is usually not very efficient on a microcontroller and would not satisfy a real-time measurement demand. Any FPGA would be powerful enough to integrate the hardware FFT, but a trade-off between performance and cost has been made for this application. A microcontroller with a cortex-core featuring a DSP module has been chosen.

The DSP module offers a variety of different mathematical and transform functions, but only the FFT will be discussed. All the DSP functionalities are supported in a set of libraries available from the microcontroller supplier. Working with the libraries is straightforward, for being well documented. A user has only to call a desired function and feed the function with correct set of data.

The DSP FFT module has following downsides worth mentioning:

- maximum number of samples - 4096,
- the highest precision variable - 32-bit floating point,

4096 number of samples is limited by a memory of the microcontroller itself, even with the chosen cortex-M7 core, the most powerful M core available at this time, the number of samples remains low, resulting in 2048 frequency bins in the frequency spectrum plot. The most accurate variable, the FFT can work with is a 32-bit floating point. A 64-bit would have been expected for a precise application.

An approximate execution time of the FFT for 4096 points and 32-bit floating variable is $1.3\,mS$. Theoretically, only 4 following lines of code are required for setting up the FFT module, according to an application note [15].

Listing 3.2: Setting up the FFT module on DSP

```
static arm_cfft_radix4_instance_f32 S;                    1
arm_cfft_radix4_init_f32(&S, sample_count, 0, 1);         2
arm_cfft_radix4_f32(&S, fft_data->fft_input);             3
arm_cmplx_mag_f32();                                      4
```

The listing 3.2 above shows setting initial settings of the FFT module. The first line is an instance of the desired FFT structure. The instance determines which type of FFT has been chosen. In this case, it is a complex FFT with a radix-4 and a 32-bit floating data type. The second line initializes the structure with desired sample count, selects direction of the transform and direction of the output. The third line is a calling of the transform function itself. The last line converts the complex output of the FFT function back to the real form.

3.4 FFT pre-processing

The sampled codes taken out of the ADC's output data register must be pre-processed, so the FFT DSP module could work with them. The pre-processing includes mainly code-to-voltage conversion and windowing. The pre-processing and subsequently the post-processing approach are following an internal standards set by the Analog Devices.

3.4.1 Waveform statistics

Before any action is applied to the ADC codes in a signed-integer form, a so-called waveform statistics is carried out. Following readings are made in this process:

- maximum amplitude,
- minimum amplitude,
- peak to peak amplitude,
- DC part,
- offset,
- transition noise.

For the maximum and the minimum amplitude, a maximum and a minimum code from the current set of data is found. Once the maximum and the minimum code is found, a peak to peak amplitude is calculated as a difference between those two readings. The DC part is extracted as a mean value of all the codes. Transition noise is calculated as a standard deviation of the set of codes according to a following equation 3.2:

$$Standard\ \ deviation\ = \sqrt{\frac{\sum_{i=1}^{n}(\,x_i\,-\,\overline{x})^2}{n}} \tag{3.2}$$

where the x is an ADC code, the $\overline{x}$ is mean value of the ADC codes from the current set of data and the n is the number of samples. All the above-mentioned readings are in codes, or in so called LSBs. The transition noise will be discussed later.

3.4.2 Offset of the ADC

Theoretically, any ADC with differential inputs should give us $0\,V$, which is also the mid-scale or the half scale equal to 2^{23} for 24-bit ADCs, when the ADC's input terminals are shorted. The AD7768-1 features an internal diagnostic multiplexer which connects input of the sigma-delta modulator either to internal temperature sensor, positive FS, negative FS or shorts the inputs to check HS. Using the multiplexer ensures that only the offset of the ADC will be measured. Similarly, the offset of the analog front end could be measured by shorting the inputs of the signal chain.

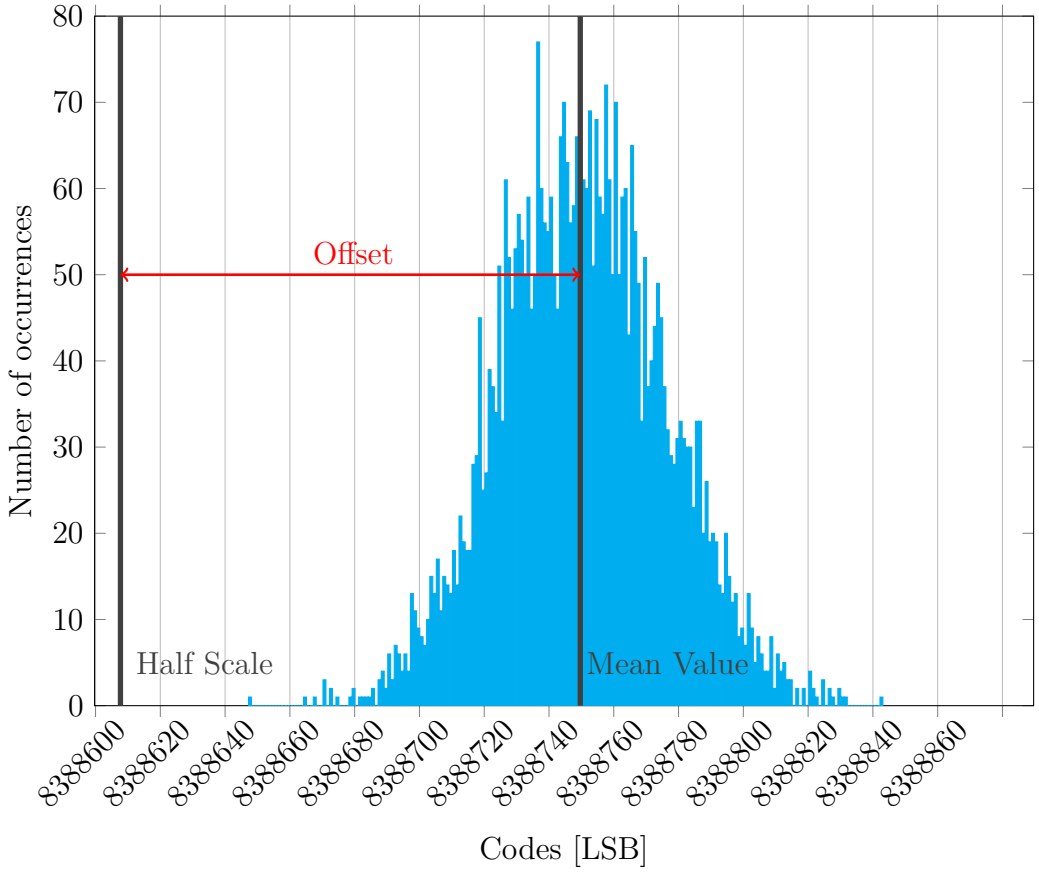


Fig. 3.1: Histogram of code occurrences with the shorted inputs of the AD7768-1

The above plot 3.1 shows a histogram of measured ADC codes distribution with the input terminals shorted. Histograms are usually used for investigating either offset of the ADC, or a so-called transition noise, which will be covered in a next chapter.

The offset is then calculated as a difference between the theoretical HS and the mean value of the code occurrence histogram. In this case, the ADC's offset shifts the HS from the expected theoretical 8388608 $LSBs$ to 8388750 $LSBs$, distributing the final offset of 142 $LSBs$, or 69 μV into the system.

3.4.3 Transition noise

Transition or RMS noise causes the ADC to provide a user with more than one output code for a fixed input voltage. It is measured as a code occurrence for a large set of measurements with a fixed voltage applied to the input of the ADC. It has the Gaussian distribution, thus using a histogram and statistics calculations is a perfect way to measure this kind of noise. Afterall, the RMS noise is nothing else than a standard deviation.

$$Trans.\,noise\,[LSB] = \sqrt{\frac{\sum_{k=0}^{n}(x_k[LSB] - \bar{x}[LSB])^2}{n}} \tag{3.3}$$

The above equation 3.3 is a standard deviation formula derived from the formula 3.2, where n is a number of samples, x_k is a k-th sample and $\bar{x}$ is a mean value of all the codes from the same set of measurement.

$$Trans.\,noise\,[V_p] = \frac{2 \times V_{REF}[V_p] \times Trans.\,noise\,[LSB]}{FS[LSB]} \tag{3.4}$$

The equation 3.4 converts the transition noise from LSB to peak voltage. The histogram from the figure 3.1 is a real measurement of the AD7768-1 code occurrence. For this particular measurement, the transition noise is equal to $25.5\,LSB$ or $12.45\,\mu V$. Which is according to the statistic standard deviation of one σ, telling us that the total RMS noise would be $24.9\,\mu V$ with a probability of 68 %.

3.4.4 Getting voltage from ADC codes

A well-known mathematics expression used whenever any ADC is mentioned, for conversion from ADC codes to volts would look like a following equation 3.5:

$$V_{IN_{Pk-Pk}}(V) = \frac{code}{FS} \times V_{REF} \tag{3.5}$$

where *code* is an actual ADC reading in codes, FS is the full-scale input range and V_{REF} is the reference voltage. This equation is correct, but one must be more careful about using it. The ADC input architecture and the actual connection might not make this equation valid anymore. The AD7768-1 offers a possibility of connecting the input signal differentialy. The connection benefits mainly for a wider dynamic range. Since the differential input configuration is used, the equation must be modified as follows, according to a formula 3.6:

$$V_{IN_{Pk-Pk}}(V) = \frac{code}{FS} \times 2 \times V_{REF} \tag{3.6}$$

where the only difference between the two equations the 3.5 and the 3.6 is multiplying by 2 due to the differential input. This equation is used in the firmware only for

a conversion from codes in single readings - like the maximum amplitude when is displayed in $Volts$ and in $LSBs$ as well. The equation is being adjusted even more to satisfy and to maximize the FFT module performance, into the following form of an equation 3.7:

$$V_{IN_{Pk-Pk}}(V) = \frac{code}{FS} \times 2 \times 1 \tag{3.7}$$

The V_{REF} was removed from the above equation 3.7, because the DSP FFT processing must be as general as possible - not targeting any specific application so the V_{REF} has been unified and replaced with 1. Thus, all codes are referred to 1 as a full-scale range. Not only generality is a case, but also each singe multiplication takes a certain processing power. Referring codes to 1 makes the processing bit more efficient. One last change in the code-to-voltage equation is desired according to a following equation 3.8:

$$V_{IN_{Pk-Pk}}(V) = \frac{code}{HS} \tag{3.8}$$

where the HS is a half scale of the ADC. In the last step, the multiplying by 2 was removed and the full-scale was replaced by the half-scale, making the equation bit easier to process. For example a 24-bit AD-converter has a full scale of 2^{24} and a half scale of 2^{23}, which is just dividing by 2, thus this division was removed.

3.4.5 Coherent sampling

A pure sinusoidal tone is usually brought to the input of the ADC to evaluate the dynamic performance of the converter. Coherent sampling can be used to accurately evaluate and correctly display the frequency spectrum of the signal. In a vast majority of cases, it is not possible to use the perfect coherent sampling and a windowing must be employed, helping to resolve the frequency spectrum and minimize the spectral leakage.

The idea of achieving the perfect coherent sampling is, that the FFT expects the input signal to be periodic over its length, which is rarely a case. Any inequality between the very first and the very last sample of the data record would introduce an error into the final frequency spectrum. The introduced error must not be ignored. Usually the error is that huge, so it does not allow a user to see the frequency spectrum at all, when plotted.

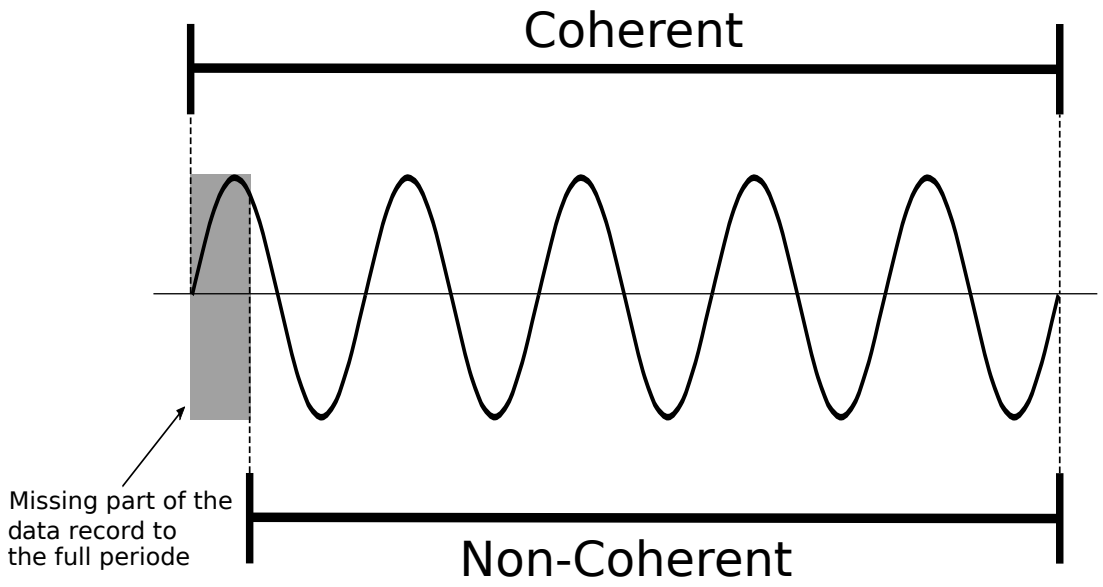


Fig. 3.2: Comparison of coherent and non-coherent sampling in a time domain

The picture 3.2 above shows a difference between coherently and non-coherently sampled data record in a time domain. Notice, in a case of the coherent sampling, exactly five periods of the sine wave are present in the data record and the sampling starts and ends at the same y-axis levels, at the same voltage levels. The non-coherently sampled data record contains a fraction, a non-integer number, of periods which introduces a coherency error into the frequency domain.

$$\frac{f_{in}}{f_s} = \frac{M_{cycles}}{N_{samples}} \tag{3.9}$$

The above equation 3.9 describes the criteria which must be accomplished to achieve the coherent sampling, where f_{in} is the input signal frequency, f_s is the sampling frequency, M_{cycles} is the number of cycles in the sampled window eg - number of full sine waves and $N_{samples}$ is the number of samples taken. Fulfilling the needs of the equation 3.9 is rarely a case. Having a perfect coherent sampling is barely possible in a real-world measurement.

A following figure 3.3 displays a difference between nearly coherently sampled, non-coherently sampled and coherently sampled with a windowing applied to an input signals. During all three sampling processes, the very same conditions were ensured. The non-coherency was achieved by changing the input signal's frequency from initial $1\,kHz$ to $1.1\,kHz$.

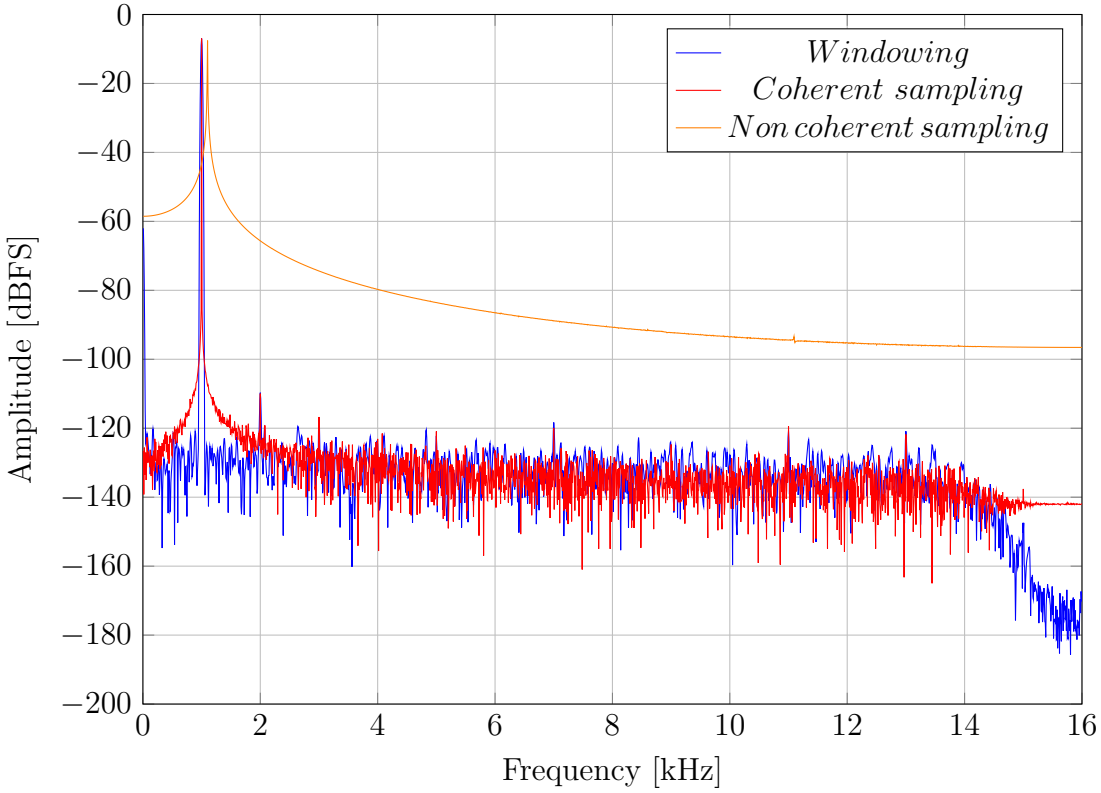


Fig. 3.3: Frequency spectrum of a signal sampled by the AD7768-1 using different sampling approaches

The coherently sampled spectrum has a significant main lobe leakage, which is very expected. Frequency spectrum of the non-coherently sampled signal cannot be used for further processing since the spectrum is hiding possible spurs.

3.4.6 Windowing

Since the perfect coherent sampling cannot be ensured for the real world-measurements, the windowing must be employed to meet the SRN requirements. The windowing is a mathematical filter which lowers an amplitude of the input sampled signal from the center towards to the edges of the data record - lowering the amplitude at the edges of the data record - reducing introduced error.

When choosing the correct windowing function for the application, usually two main aspects are considered:

- main lobe width - affects the power leakage of the fundamental,
- peak side lobe level - affects the overall noise level.

The power leakage can be easily corrected to a sufficient final error, thus more critical is the level of the side lobes. There are many different windowing functions available with certain pros and cons. Each one fits perfectly to a certain type of assignment.

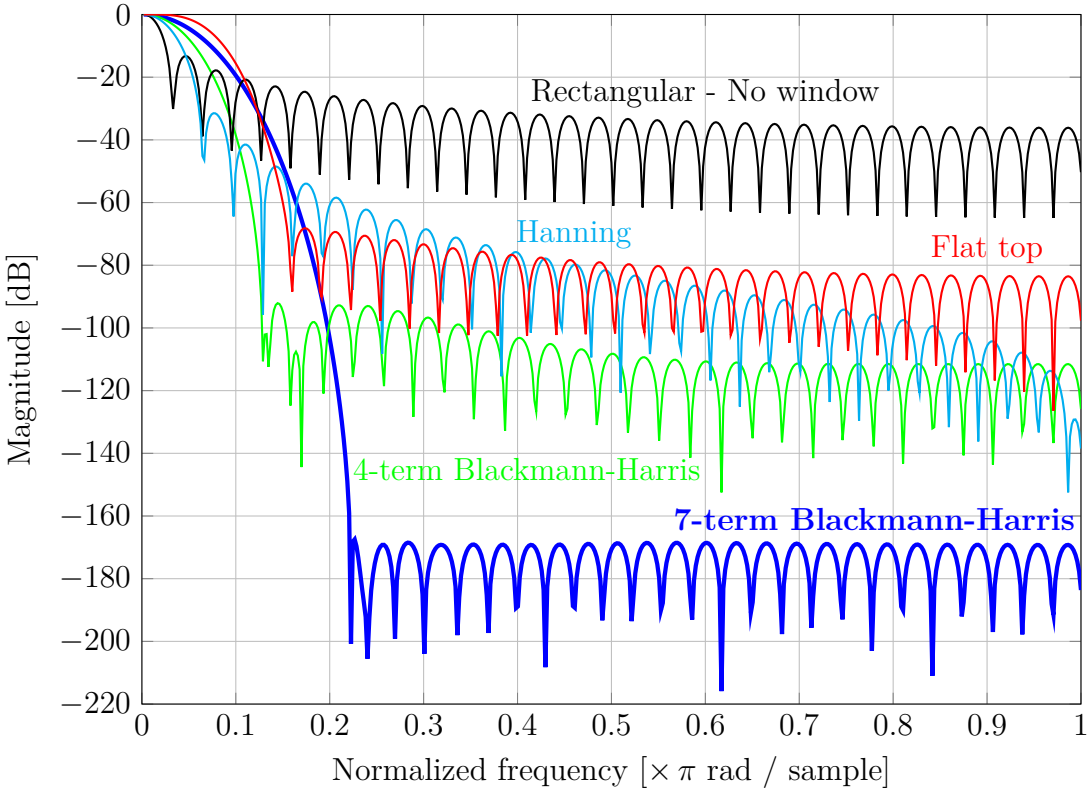


Fig. 3.4: Frequency domains of different windowing functions

A scientific software GNU Octave was used for frequency domain comparison of different windowing functions. The chart 3.4 above depicts frequency domains of five windowing functions. All the functions are 64-points long and were gain-corrected to $0\,dB$, as each window has different gain. Widely-used types of windows, like Hanning or Flat-top are usually officially supported in scientific softwares, but the 7-term Blackmann-Harris is very specific and its frequency domain was generated after creating a custom function in GNU Octave using an equation 3.10.

As it is visible from the chart 3.4, the 7-term Blackmann-Harris window has excellently low level of the side lobes - a perfect ability to suppress the overall noise in the signal spectrum, making it the most suitable windowing function. Unfortunately, it comes with the widest side lobe, but it can be easily corrected.

The toll for the function's excellent noise performance is its power and time demanding calculation, which is surely one of the main reasons why it is not so widely used. Sometimes, even the Hanning window is enough, which is approximately 6 to 7-times faster to calculate. In this case the Hanning window would limit the ADC'c dynamic range, thus cannot be used.

A below equation 3.10 belongs to the 7-term Blackmann-Harris windowing function. The equation was taken from the official LabVIEW documentation provided by the National Instruments [16]:

$$w[n] = \sum_{k=0}^{6} a_k \times cos\left(\frac{2k\pi}{N}\right) \tag{3.10}$$

where a_k is a windowing coefficient provided in a list of coefficients 3.11 below, N is the number of samples.

$$\begin{aligned} a_0 &= 0.27105140069342 \\ a_1 &= -0.43329793923448 \\ a_2 &= 0.21812299954311 \\ a_3 &= -0.06592544638803 \\ a_4 &= 0.01081174209837 \\ a_5 &= -0.00077658482522 \\ a_6 &= 0.00001388721735 \end{aligned} \tag{3.11}$$

Please note, that for a single sample a sum of seven cosine functions must be calculated to apply the windowing function. For 4096 samples long set of data, over 25-thousand of cosine functions must be calculated, slowing the pre-processing down significantly. To accelerate it a table of pre-calculated coefficients was stored into a flash memory of the microcontroller as a set of constants. Instead of 25-thousands cosine function calculation, only 4096 multiplication is needed for one set of data.

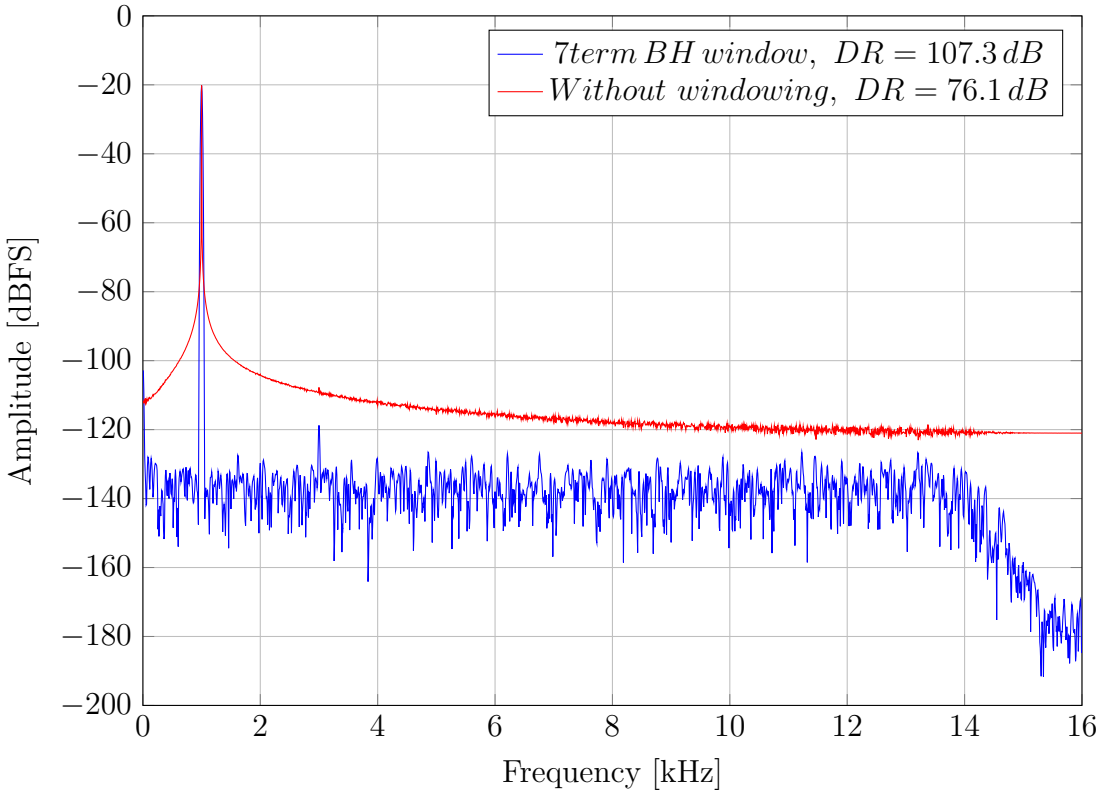


Fig. 3.5: Comparison of windowed and non-windowed frequency spectrum

The figure 3.5 above shows the same input signals with and without windowing applied. The windowed spectrum significantly pushes the noise down, offering the dynamic range as good as $107\,dB$, more than $30\,dB$ better than the non-windowed signal. Also revealing all kind of hidden frequency spurs and the digital filter roll-off at the end of the frequency spectrum, which is impossible to spot with the non-windowed signal

Feeding the FFT routine

The data is ready to be processed by the FFT routine. As already mentioned in the listing 3.2, the FFT function being used is a complex FFT and it expects the input in the complex form. Thus, the real part of the complex number is an amplitude and the imaginary part is a phase shift. Since the ADC provides us only with the amplitude, the imaginary part of the complex number must be equal to 0 for each sample.

3.5 FFT post-processing

After the FFT is done, the very first step is to convert the complex output of the complex frequency spectrum back to the real form, by using the last command from the listing 3.2. An array with the real frequency spectrum is ready to be further processed.

3.5.1 Correction factor

Windowing, from the most basic point of view, is just a multiplying each sample by a certain coefficient which depends on the number of samples and a window type. Whenever doing windowing, it is necessary to compensate power loss in the frequency spectrum caused by the windowing itself. There are couple of different methods of compensating the power loss. For example, the LabVIEW uses pre-defined constants for each type of window. A completely different approach has been chosen due to an insufficient integrity into the system. This correction factor has two parts:

- **Nyquist frequency power loss** - the full frequency spectrum is divided into two halves with the center point in the Nyquist frequency. We are naturally interested only in one half (the left one), since the second one is completely the same but, mirrored around the center point, which makes it a redundant information. Each sample which is going to be displayed and further worked with (usually the entire left half of the frequency spectrum) must be multiplied

by 2 to compensate the power loss caused by not considering the right half of the spectrum.

- **Windowing power loss** - is defined as each sample is being divided by sum of the window coefficients. In a case of the rectangular window (no window) each sample is divided by the FFT length. In a case of any other window, each sample is divided by a sum of all coefficients which had been applied to each sample separately before the FFT was done.

The final correction formula has a following form:

$$X_k = \frac{X_k \times 2}{\sum window} \tag{3.12}$$

where X_k is a k-th sample of the frequency spectrum and it is all divided by the sum of the windowing coefficients. By applying the formula 3.12, a correct power level is ensured across the considered frequency spectrum.

3.5.2 Magnitude - decibels conversion

Converting from magnitude present in V_{Pk-Pk} is simply done by a following formula 3.13, because the full-scale value has been chosen to be 1.

$$mag\,[dB] = 20log(mag[V_{Pk-Pk}]) \tag{3.13}$$

where $mag[dB]$ is the magnitude in decibels and $mag[V_{Pk-Pk}]$ is the magnitude in V_{Pk-Pk}. A formula 3.14 for the full-scale related decibels $[dBFS]$ conversion is the same as the previous one 3.13 due to an assumption which has been made between formulas 3.7 and 3.8. The peak to peak full scale is 1 even though the ADC has differential inputs but normally the the peak to peak full scale would have been chosen to be 2.

$$mag\,[dBFS] = 20log(\frac{mag[V_{Pk-Pk}]}{1}) \tag{3.14}$$

For an independent converting from the full-scale decibels back to V_{Pk-Pk} - still not assuming the real reference voltage connected to the ADC a following formula 3.15 is used:

$$mag\,[V_{Pk-Pk}] = 1 \times 10^{\frac{mag[dBFS]}{20}} \tag{3.15}$$

For a reference voltage dependent conversion from the full-scale decibels back to V_{Pk-Pk} a following formula is used:

$$mag\,[V_{Pk-Pk}] = 2 \times V_{ref}[V_P] \times 10^{\frac{mag[dBFS]}{20}} \tag{3.16}$$

where the V_{ref} is the voltage reference level connected to the ADC. It can be either in the peak multiplied by 2 form, or in peak to peak form.

3.5.3 Spectral leakage correction

Spectral leakage is a result of the non-coherent sampling in a frequency spectrum. It cannot be removed, but it can be very effectively minimized by the windowing as already proved in the figure 3.5. By applying the windowing function, the actual wide band leakage is squeezed into a few frequency bins.

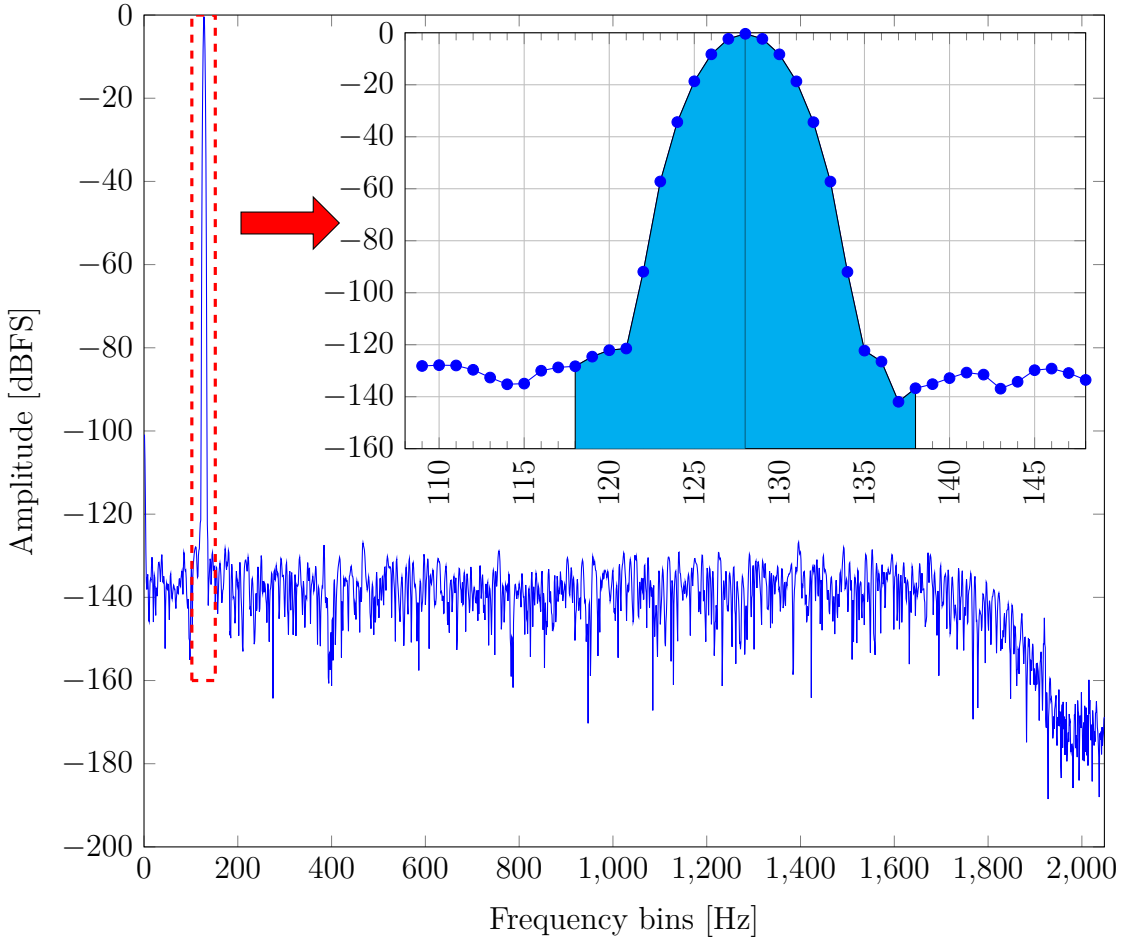


Fig. 3.6: Detailed cut of the fundamental amplitude spectral leakage

The figure 3.6 shows a close look of how the spectral leakage affects the fundamental amplitude. Ideally - for a perfect coherent sampling, the fundamental should consist only of the single frequency bin and the frequency bins from either side of the fundamental should be at the level of the noise floor. But as the detailed cut from the figure 3.6 shows, the leakage has occurred and the fundamental amplitude has spread over more frequency bins. The leakage is showed as the blue filled area below the curve and the blue dots are boundaries of the frequency bins. The leakage possessed at least 7 frequency bins from either side of the fundamental.

As the leakage has occurred, claiming that the power under the fundamental

frequency bin equals the power of the fundamental amplitude would introduce an error into the measurement. In order to correct the power of the fundamental amplitude we must consider additional powers under the frequency bins around the fundamental bin. The firmware considers 10 frequency bins from either side of the fundamental as the correction - making sure all the bins possessing higher power than the noise floor are taken into account. In case of the harmonics, it is 3 bins because the harmonics tend to have much lower amplitude, thus less frequency bins are affected by the leakage.

Once the leaked bins are distinguished, an RSS according to an equation 3.22 is applied to the considered bins to calculate the total power of the leaked fundamental magnitude which is comparatively equal to the power under the fundamental frequency bin without the leakage.

3.5.4 Distinguishing bins

Every time a set of fresh data is received, the firmware is investigating the frequency bins and sorting them out into different categories, so the bins could be handled differently in the post-processing.

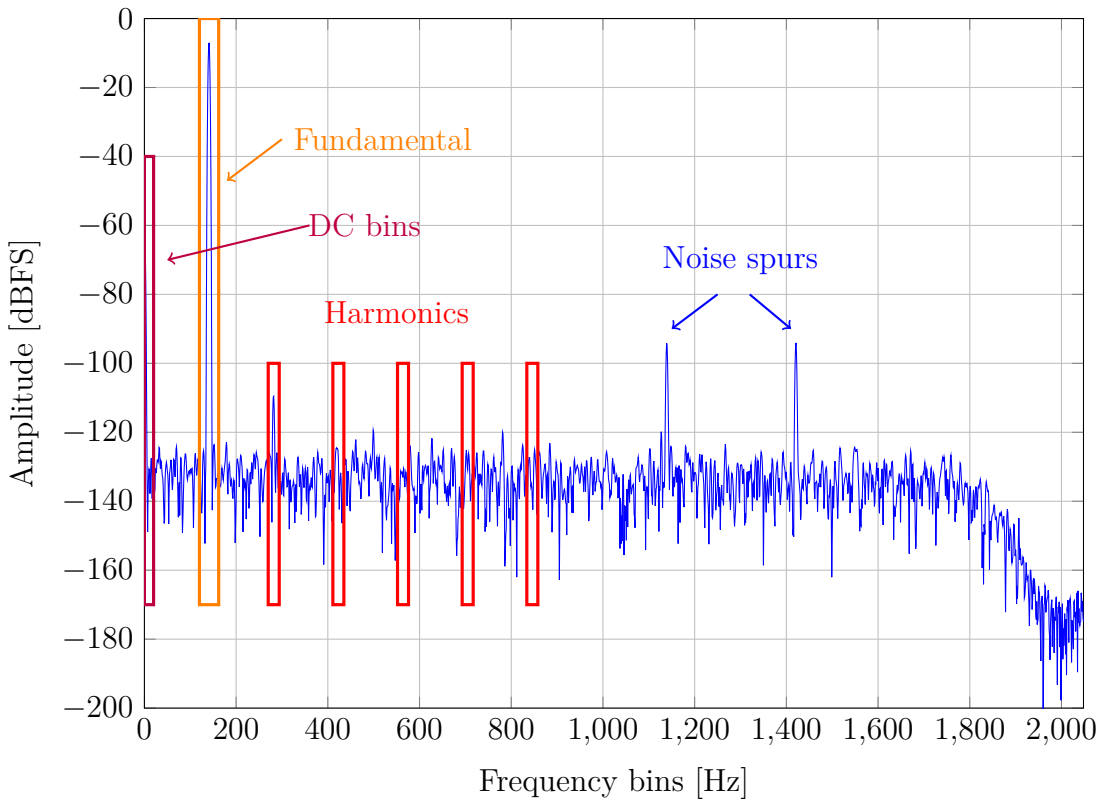


Fig. 3.7: Sorting out frequency bins from the spectrum into categories

As the figure 3.7 shows, in a case of 4096 samples, which makes a 2048 frequency bins long spectrum, the firmware sorts the bins into a following categories:

- **fundamental**: one center bin plus 20 side bins,
- **DC part**: first 10 bins of the spectrum,
- **harmonics**: one center bin plus 6 side bins for each harmonic,
- **noise**: rest of the bins, which makes 1982 noise bins.

Even if there is a bin with a significantly high amplitude and is not a multiple of the fundamental bin, it is considered as a noise bin. The case is depicted in the figure 3.7 as the noise spurs.

3.5.5 Picking up the fundamental frequency

In order to get the THD, SRN or other fundamental frequency dependent readings, a position of the fundamental magnitude must be found. The firmware simply goes through the frequency spectrum and picks the highest magnitude, ignoring first 10 frequency bins, which tend to be quite significant and might affect the fundamental picking process.

3.5.6 THD calculation

The firmware considers 6 harmonics when calculating the THD to achieve a sufficient precision. Expected position of the n-th harmonics is estimated by multiplying the fundamental frequency by n-th number of harmonics. Consequently, the exact position of the harmonic is found by determining the searching interval as 7 frequency bins - having the estimated frequency bin as the center bin and 3 bins from either side of the center frequency bins. The highest magnitude within the interval is picked as the final position of the harmonic. The figure 3.7 shows a graphic location of the harmonics referred to the fundamental. The THD is consequently calculated using a following equation:

$$THD\,[dB] = 20log\left(\frac{\sqrt{\sum_{k=1}^{5} P_{k_{harm}}^2[V_{Pk-Pk}]}}{P_{fund}[V_{Pk-Pk}]}\right) \tag{3.17}$$

where $P_{k_{harm}}$ and P_{fund} are spectral leakage corrected powers of the harmonics and the fundamental.

3.5.7 Folding of the harmonics

An ability to pick up folded harmonics must be employed, in order to precisely calculate the THD. Following formulas are explaining how the firmware picks the folded harmonics in the first Nyquist zone:

$$Alias_{odd}[bin] = 1^{st}ZoneBW[bin] - (1^{st}ZoneBW[bin] \times Zone - Fund[bin] \times n) \quad (3.18)$$

$$Alias_{even}[bin] = 1^{st}ZoneBW[bin] \times Zone - Fund[bin] \times n \quad (3.19)$$

where $1^{st}\,Zone\,BW$ is a quantity of frequency bins in the first Nyquist (in any Nyquist) zone, $Fund$ is a position of the fundamental magnitude, n is n-th harmonics. The $Zone$ is determined as a no-remainder (decade) division of the real frequency of the harmonic multiplied by two and the sampling frequency and is calculated using a following equation:

$$Zone = 1 + \left(\frac{f_{real}[Hz] \times 2}{f_s[Hz]} \right)_{DEC} \quad (3.20)$$

As an example of the harmonics folding, let us have an input signal with a frequency of $10\,kHz$, sampling frequency of $30\,kHz$ and 4096 samples, which will give us $7.8125\,Hz$ bin-width according to the equation 3.1, and 2048 frequency bins in the first Nyquist zone. A following table 3.1 is filled using equations 3.18 and 3.19 for odd and even zones. Applying the formula 3.18 to the fourth row of the table 3.1 to determine folded position of the 4^{th} harmonic present in the third zone Nyquist zone:

$$4^{th}\,harm = 2048 - (2048 \times 3 - 1280 \times 4) = 1024 \quad (3.21)$$

Tab. 3.1: Folding of the harmonics

Harmonic	**Real freq. [kHz]**	**Frequency bin**	**Nyquist zone**	**Alias freq. [kHz]**	**Aliased bin**
Fund.	10	1280	1	10	1280
2^{nd}	20	2560	2	12	1536
3^{rd}	30	3840	2	2	256
4^{th}	40	5120	3	8	1024
5^{th}	50	6400	4	14	1792
6^{th}	60	7680	4	4	512

The table 3.1 above shows how the real out-of-band frequencies fold into a particular frequency bin present in the first Nyquist zone.

3.5.8 Noise parameters calculation

In the following points it is described, how the noise parameters are calculated [17].

Root sum squared

The root sum squared is a statistical method used mainly in a tolerance analysis. Since the noise is a statistical quantity, a statistical method must be applied in order to get as close value to the real noise as possible. Also the spectral leakage described in the subsection 3.5.3 has the Gaussian shape, so the RSS can be applied for spectral leakage correction. The RSS is nothing else than a geometric summation and is determined by a following equation 3.22:

$$RSS[V_{Pk-Pk}] = 2\sqrt{2}\sqrt{\sum_{k=0}^{n}\left(\frac{P_k[V_{Pk-Pk}]}{2\sqrt{2}}\right)^2} \tag{3.22}$$

As the equation above shows, the RSS can be applied only to an amplitude in the RMS form, not in the $P_k - P_k$ form. Conversion from RMS to $P_k - P_k$ is done by dividing by $2\sqrt{2}$ and then the RMS is converted back by multiplying by the same number.

Dynamic range

The universal definition of the dynamic range is the ratio between the largest and the smallest value that can be detected by a device, a sensor, in our case it is the ADC. The theoretical dynamic range of the ADC is set by a following equation:

$$DR\,[dB] \approx 6.021 \times N + 1.763 \tag{3.23}$$

where N is the number of bits. According to this equation, the dynamic range of the AD7768-1 would be more than $146\,dB$, which is very far from the truth, since the equation does not consider any noise, not the ADC's noise, nor the noise introduced by the rest of the parts.

$$DR\,[dB] = 20log\left(\frac{1}{P_{noise}\,[V_{Pk-Pk}]}\right) \tag{3.24}$$

The real DR of the ADC is calculated as the ratio between the FS, which has been unified to 1 in the equation 3.7 (for the needs of this specific firmware) and the noise floor according to the equation 3.2. The P_{noise} from the equation 3.24 above is the RSS power of the noise bins, sometimes called a noise floor. [17]

Signal to noise ratio

The SRN is a special case of the DR, in which the unified FS signal is replaced with the power of the fundamental magnitude. The SRN is set by an equation 3.25 as follows:

$$SNR\,[dB] = 20log\left(\frac{P_{fund}\,[V_{Pk-Pk}]}{P_{noise}\,[V_{Pk-Pk}]}\right) \tag{3.25}$$

where the P_{fund} is power of the fundamental after the power leakage correction and the P_{noise} is the power of the noise floor. [17]

Signal to noise ration and distortion

SINAD gives a user a complex dynamic performance of an ADC, including noise, input signal and distortion into one specification. It includes THD together with SRN into one equation [17]:

$$SINAD\,[dB] = -10log\left(10^{\frac{-|SNR[dB]|}{10}} + 10^{\frac{-|THD[dB]|}{10}}\right) \tag{3.26}$$

Effective number of bits

SINAD is often converted to ENOB according to an equation 3.27 showing how many bits can be used for measurement and how many are hidden in the noise [17].

$$ENOB\,[LSB] = \frac{SINAD[dB] - 1.76[dB] + 20log\left(\frac{mag_{FS}[V]}{mag_{input}[V]}\right)}{6.02[dB]} \tag{3.27}$$

The above equation for ENOB is used in a case, when a non-full-scale signal is present at the input of the ADC. For the FS signal scenario, the log element is skipped. [17]

Spurious free dynamic range

Spurious free dynamic range or SFDR is a dynamic range of the ADC which does not contain any noise spur and it's noise floor sits at the top of the highest noise spur present in the frequency spectrum. An example of the noise spur is shown in the figure 3.7.

$$SFDR\,[dBFS] = P_{spur}[dB] \tag{3.28}$$

Commonly, the SFDR is shown in decibels related to full scale or $dBFS$, which is a power under the frequency bin with the highest amplitude, as the equation 3.28 shows.

$$SFDR\,[dBc] = P_{spur}[dB] - P_{fund}[dBFS] \tag{3.29}$$

Sometimes the SFDR is shown in decibels related to carrier dBc, as it is done in the equation 3.29, where the carrier is a power under the fundamental amplitude. [17]

3.6 Data reception

The AD7768-1 offers several data conversion modes. The most used mode is a continuous conversion mode, in which the ADC is converting the input voltage continuously and delivers the result in a specific time interval determined by the ORD. An internal signal, which has its dedicated pin on the AD7768-1 package called $\overline{\text{DRDY}}$ is normally low, but once the filter finishes the conversion, the $\overline{\text{DRDY}}$ rises high, signalizing that the data is prepared to be read from the ADC. [11]

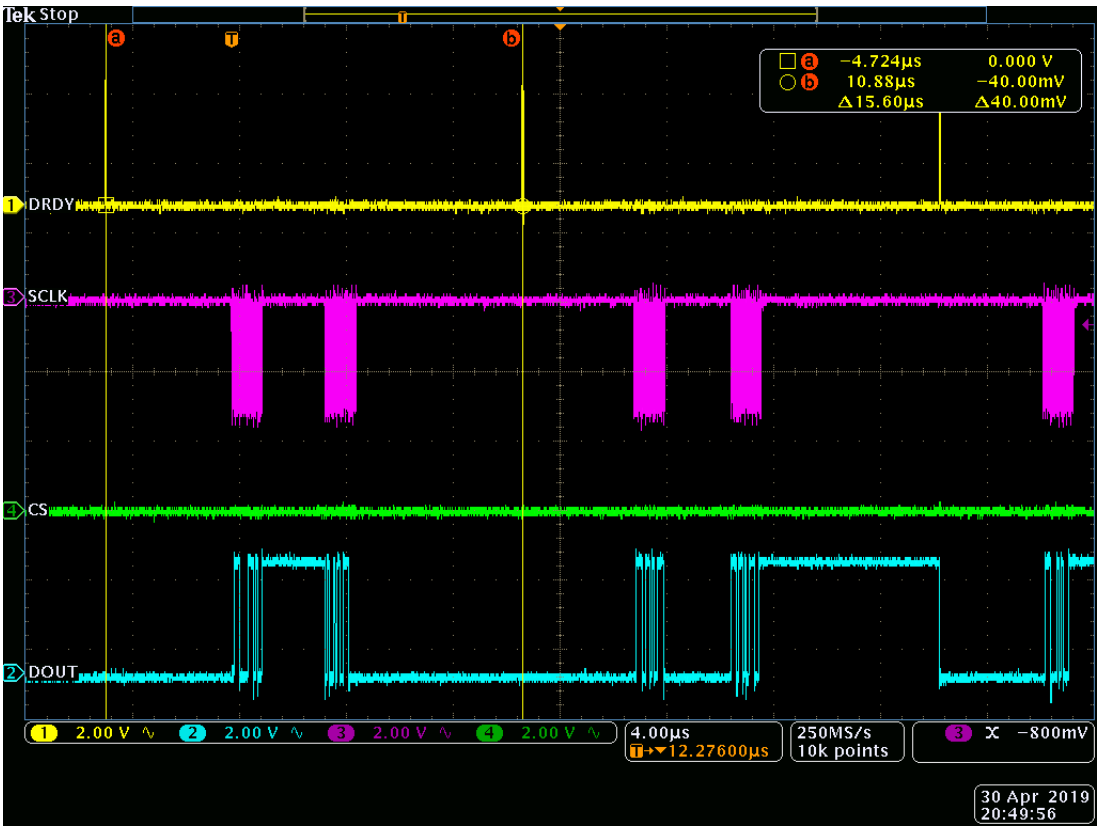


Fig. 3.8: SPI data reception frame with the ODR at 64 kHz

The figure 3.8 was captured by a digital oscilloscope Tektronix DPO4104B-L and shows a data reception frame, with $\overline{\text{DRDY}}$, SCLK, CS and DOUT signals. The $\overline{\text{DRDY}}$ has been connected to a MCU pin, to which an interrupt has been bounded

in the firmware. The interrupt is a logic level change sensitive. Every time the $\overline{\text{DRDY}}$ goes high, the data are received from the ADC. The data reception frame must be quick enough, to fit between two $\overline{\text{DRDY}}$ signals, not to lose any data.

An ADI's internal requirement for the firmware environment, was to use MBED libraries for the development, allowing the firmware to be cross-platform compatible. The MBED is a set of libraries provided directly by the ARM company. A development board STM32F746G was used, but any MBED compatible board would do. A significant delay is introduced into the data reception routine by the MBED system. By investigating the firmware, following downsides have been found:

- not possible to generate a 32-bit long SPI frame, the frame was automatically cut into two 16-bit frames by the MBED,
- a 1.5 μS delay between the frames, not depending on the SPI speed,
- a 5 μS delay from the logic change of the $\overline{\text{DRDY}}$ to start of the data reception,
- a 5 μS delay from the end of the data reception to the end of the firmware interrupt routine.

From the above mentioned downsides, it is obvious, that the total delay of the data reception frame is more than 11 μS. The introduced delays are visible at the figure 3.8.

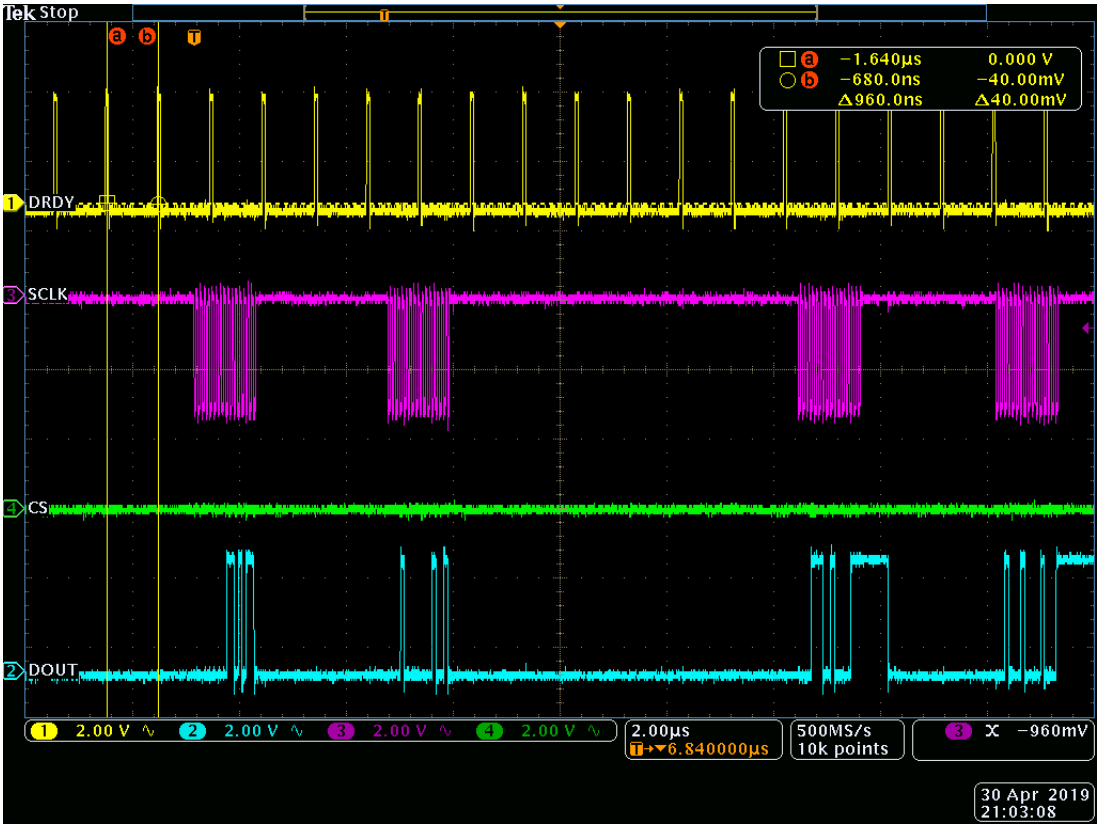


Fig. 3.9: SPI data reception frame with the ODR at 1 MHz

The figure 3.9 displays the highest possible sampling frequency, which can be achieved by the AD7768-1 with a 16.384 MHz clock. The ODR is set to 1 MHz, which makes the window for the data reception only 1 μS. In this case, the window is not wide enough for the data reception frame.

The system was tested without use of the MBED libraries. All the delays were successfully removed, and the data reception took only about 2.3 μS, which is a time interval needed for the SPI to receive a 32-bit long word, plus calling of the firmware interrupt routine. It is clearly visible, that even that short reception interval does not fit into the $\overline{\text{DRDY}}$ window, but this time the limitation is caused by the MCU itself. It is recommended to use an MCU with rapidly faster clock, or an FPGA for that fast data receptions.

Even though the results achieved by the MBED libraries are not ideal, the results are good enough. The band of interest lays in rather lower frequencies spectrum. The highest possible sampling frequency with the MBED is 64 kHz which makes a 32 kHz frequency spectrum. This frequency range is totally enough, since the used piezoelectric accelerometer has the bandwidth of 3 kHz.

3.7 Results evaluation

All the calculations from this chapter were evaluated using an existing FFT processing core written in LabView, being used in a vast majority of evaluation software provided by Analog Devices. Process of the evaluation compares the very same ADC codes processed by two different FFT algorithms. There will be no board-to-board mismatch, neither the time variation, since the very same set of sampled codes is compared. The main goal of this FFT processing on the DSP was to show and to prove, that the DSP processing is capable of precise measurements. The used LabView FFT processing core is considered to be the most accurate FFT processing across whole company.

The table 3.2 compares results from the DSP and the LabView processing algorithms. The biggest mismatch between them is 2.3 dB of SFDR. In case of DSP, the SFDR is clearly defined in 3.5.8 according to a most recent internal standards. After a quick double math check using the formula 3.29, the SFDR is correct. In the LabView case, the SFDR is defined according to a slightly older standard, which has not been updated yet, it is unclear how it has been defined.

In addition, the DSP code offers ENOB, SFDR related to the carrier and SFDR related to full scale. These measurements are not available (yet) in the AD7768-1 LabView evaluation software.

Achieved results proving reliability of the DSP FFT processing algorithm. 4096 as the maximum number of samples is although a very low sample count for any

24-bit precision AD-converter in general, but still a high level of precision with such a number of samples has been achieved.

Tab. 3.2: DSP and LabView FFT processing comparison

Measurement	**DSP**	**LabView**	**Unit**
Fundamental frequency	1000	1000	Hz
Fundamental amplitude	-0.389537	-0.389559	dBFS
SNR	107.12	107.118	dB
THD	-123.076	-123.637	dB
SINAD	107.011	107.008	dB
SFDR	-126.334	-124.041	dBc
DR	107.786	107.785	dB
Peak spurious frequency	10906.25	10906.2	Hz
Peak spurious noise	-126.724	-126.706	dBFS
Average bin noise	-138.142	-137.868	dB
Transition noise	2.76928	2.76961	V
	5671486.5	5672180	LSB
Max amplitude	3.90248	3.90251	V
	16380900	16380900	LSB
Min amplitude	-3.90240	-3.90240	V
	396484	396484	LSB
Peak-Peak amplitude	7.80493	7.80491	V
	15984500	15984500	LSB
DC part	1.46484E-05	1.47941E-05	V
	8388638	8388640	LSB
Fundamental	-0.389537	-0.389559	dBFS
	1000	1000	Hz
2^{nd} harmonic	-136.073	-135.603	dBFS
	1984.38	1984.37	Hz
3^{rd} harmonic	-127.412	-127.299	dBFS
	3000	3000	Hz
4^{th} harmonic	-132.689	-132.677	dBFS
	4015.63	4015.62	Hz
5^{th} harmonic	-133.223	-133.189	dBFS
	5023.44	5023.44	Hz
6^{th} harmonic	-136.961	-136.883	dBFS
	6023.43	6023.44	Hz

4 Evaluation measurements

The following chapter deals with accomplished results, offering a complete overview of the system behavior in terms of noise, distortion, or power consumption.

4.1 Total noise of the signal chain

The total noise of the signal chain was measured in different scenarios to understand how the noise is being introduced into the system.

Tab. 4.1: Signal chain noise for different conditions

Condition	**MCLK/16**		**MCLK/8**	
	Noise [μV RMS]	**DR [dB]**	**Noise [μV RMS]**	**DR [dB]**
AC Coupled, CCS en.				
Shorted IN	13.3	107.1	14.8	106.3
1 $k\Omega$ at input	25.8	102.1	34.1	99.1
AC Coupled, CCS dis.				
Shorted IN	13.3	107.4	15.1	106.1
1 $k\Omega$ at input	13.5	107.2	14.9	106.4
DC Coupled, CCS en.				
Shorted IN	23.8	105.9	24.2	104.6
1 $k\Omega$ at input	33.2	100.8	39.2	98.4
DC Coupled, CCS dis.				
Shorted IN	21.3	105.7	22.1	105.4
1 $k\Omega$ at input	22.2	105.9	22.1	105.2

The table 4.1 was filled with measurements, when the default system settings from a section 4.11 were established. The noise parameters were measured without the sensor connected. The measuring medium was the PCB itself after evaluation of the DSP processing.

Widening the bandwidth by changing the MCLK divider does not add much noise into the frequency spectrum, meaning the wide band noise is very low - the DR changes only within a 1 dB, which is very acceptable.

A 1 $k\Omega$ resistor was placed across the CCS to the ground to find out how the current noise from the CCS affects the overall noise performance. When the input of the signal chain is shorted the CCS does not contribute any noise into the system.

The current noise from the CCS is transformed into the voltage noise on the resistor and multiplied by the resistance of the resistor. Thus, the resistance-dependent noise level itself is not an useful reading, but it shows how important and significant the CCS current noise contribution is. The difference in DR between the CCS being enabled or disabled is as high as $5\,dB$. The CCS noise quieting experiment from the subsection 2.4.1 was in place.

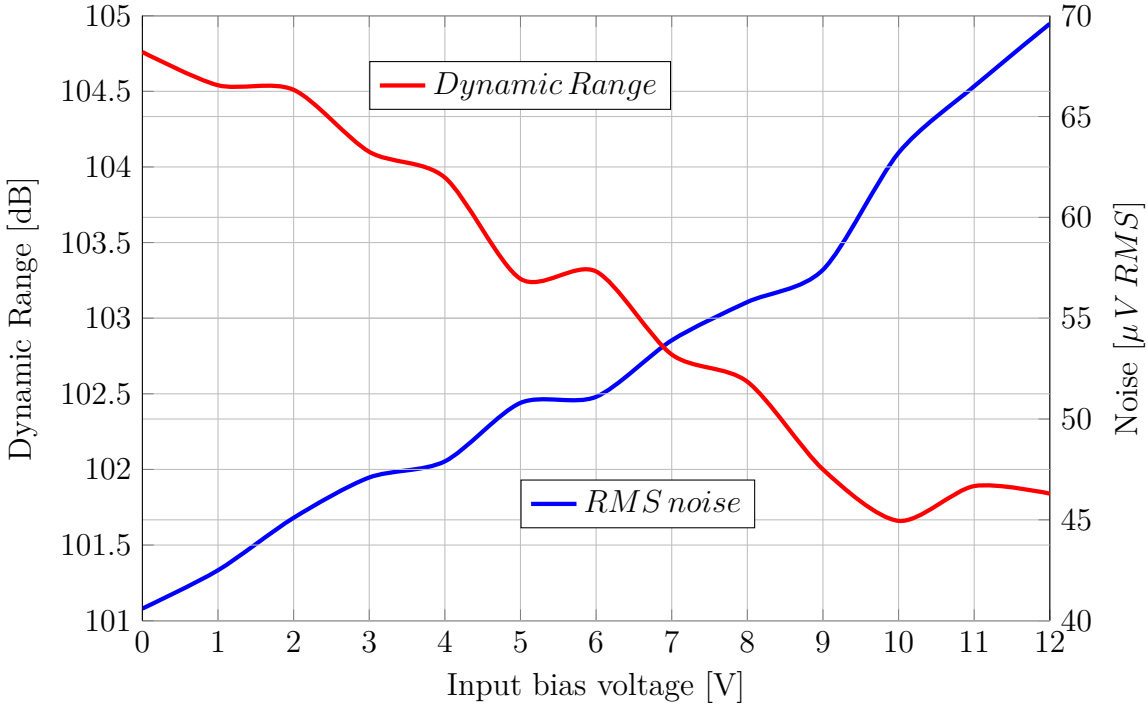


Fig. 4.1: Measured noise and dynamic range of the DC coupled signal chain vs. input bias voltage

The plot 4.1 depicts how the noise of the DC coupled signal chain changes with the input bias voltage at a stable temperature, simulating different accelerometer bias voltages. The input bias voltage was set by a very low noise, high precision DC voltage calibrator DVC-8500, which output noise is comparable with an output noise of a reference chip. Since the RMS noise is a static reading, only a DC bias was applied to the input of the signal chain. In order to get the dynamic range, the DC calibrator in connection with the sine wave source Audio Precision SYS-2522 was used. The AC input signal was chosen to be a $1\,V_{Pk-Pk}$ and $1\,kHz$.

Even though, the calibrator has a very low output impedance, a current from the CCS flows into the voltage source, transforming the current noise to the voltage noise on the output-voltage dependent output impedance. Thus, the noise of the signal chain is proportional to the input bias voltage. The DR changes in only about

$3\,dB$ within the range of $12\,V$ of the input bias voltage. Every time the input bias voltage changes, the DAC compensates the analog inputs of the ADC.

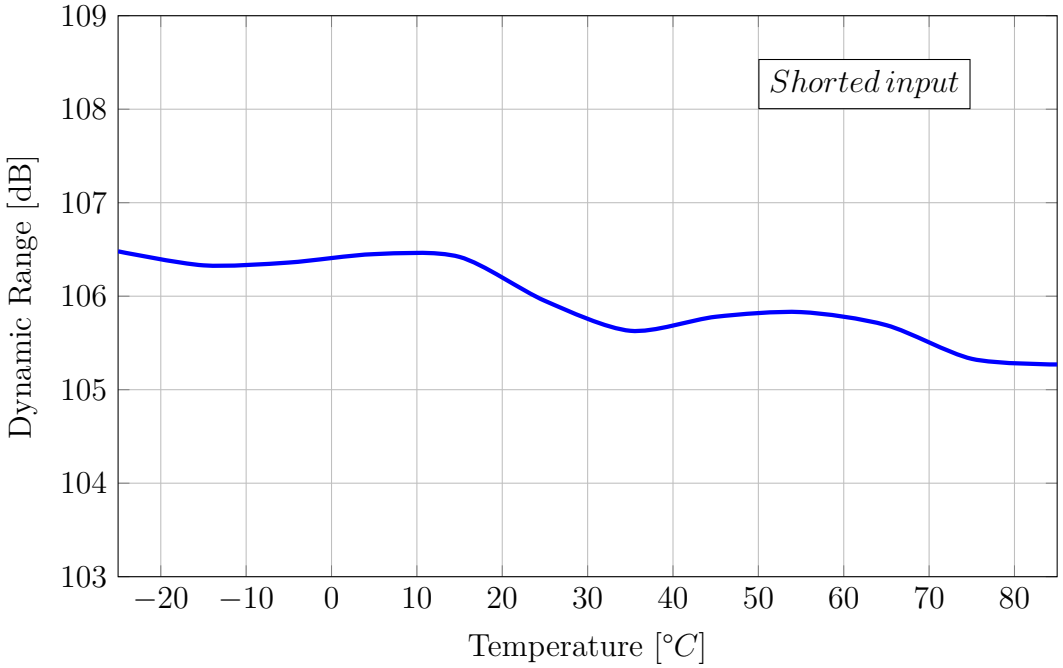


Fig. 4.2: Measured dynamic range of the DC coupled signal chain with the input terminals shorted vs. temperature

The DC coupled signal chain dynamic range dependency on temperature was measured with the shorted signal chain input and the DAC set to HS. The results depicts the figure 4.2. DR is excellent over the wide range of temperature, not dropping below $105\,dB$.

4.2 DAC buffer noise

Buffering a reference chip, or a DAC voltage output is always a trade-off between noise performance and cost. As explained in the section 2.7, buffering this DAC output was unavoidable due to the applied gain. Even though, the chosen DAC has a very low output voltage noise, the noise filtering has taken the place here which, as shows a following table 4.2, turned out to be a vital decision.

The table deals with the DAC output noise. It was measured, using an official evaluation AD7768-1 board, featuring an extremely low noise analog front-end. The DAC output was sequentially set from 0, through a quarter-scale, half-scale, 3-quarter-scale and finally tu the full-scale. From the table it is visible, that for $0\,V$ output there is only very light difference between the buffer and the buffer-less

solution and the DR of both reading is very close to the DR of the signal chain with the shorted inputs. The buffer itself is contributing only about $1\,\mu V\,RMS$ of noise, by subtracting the two RMS noise readings from the first line of the table.

Tab. 4.2: DAC output noise for different DAC output voltages

DAC code	**Without buffer**		**With buffer**	
	Noise [μV RMS]	**DR [dB]**	**Noise [μV RMS]**	**DR [dB]**
0x0000	12.7	107.3	13.1	107.5
0x3FFF	24.5	101.9	13.4	107.2
0x7FFF	25.2	101.1	13.6	107.5
0x9FFF	26.4	101.2	13.6	107.3

As the voltage rises, the buffer-less solution suffers with a significant noise growth and the DR drops in $6\,dB$, contrary to the buffered output, where the noise remains more-less stable. From the buffer-less solution one can see the noise has an inverted-exponential behavior. The noise has doubled in the very beginning between the 0 and the quarter-scale output. Consequently, the noise is rising very lightly showing that the DAC has a quite low noise to output code dependency. The buffer helped to widen the DR of the signal chain significantly.

4.3 PCB implementation

A hardware implementation in terms of PCB(s) might seem bit unusual and unnecessarily complicated to split one design into more separate PCBs, when looking at an appendix C. From the appendix is visible, that the design has been split into two boards: a data acquisition board C.2 and a piezo sensor conditioning board C.1.

There is more than one reason behind the splitting. Firstly, there was a demand to create a universal AD7768-1 board with the Arduino connectors based on an already existing design. A fraction of the design is visible on schematic A.2 but the ADC front-end is not covered in this thesis neither was used for any of the measurements.

Secondly, as the AD7768-1 Arduino board needed to be universal, it would not target any specific design. To keep the board universal the piezo sensor conditioning board C.1 was implemented into separate PCB. A full schematic of the piezo sensor conditioning board displays an appendix A.1.

Since this project was only a demo version at that time, the idea was to create one universal board with the ADC featuring the Arduino connectors and more switchable boards targeting specific applications, like piezoelectric accelerometer board, MEMS accelerometer board etc. An already planned merging of the two designs into a single PCB is not covered in this thesis.

4.4 Offset error drift measurement

In order to find out how the voltage offset of the system drifts with the temperature for a stable input bias voltage, the whole design excluding the DC voltage supply simulating the sensor's bias, was placed into an oven. The real sensor's bias voltage is stable across a wide range of temperatures.

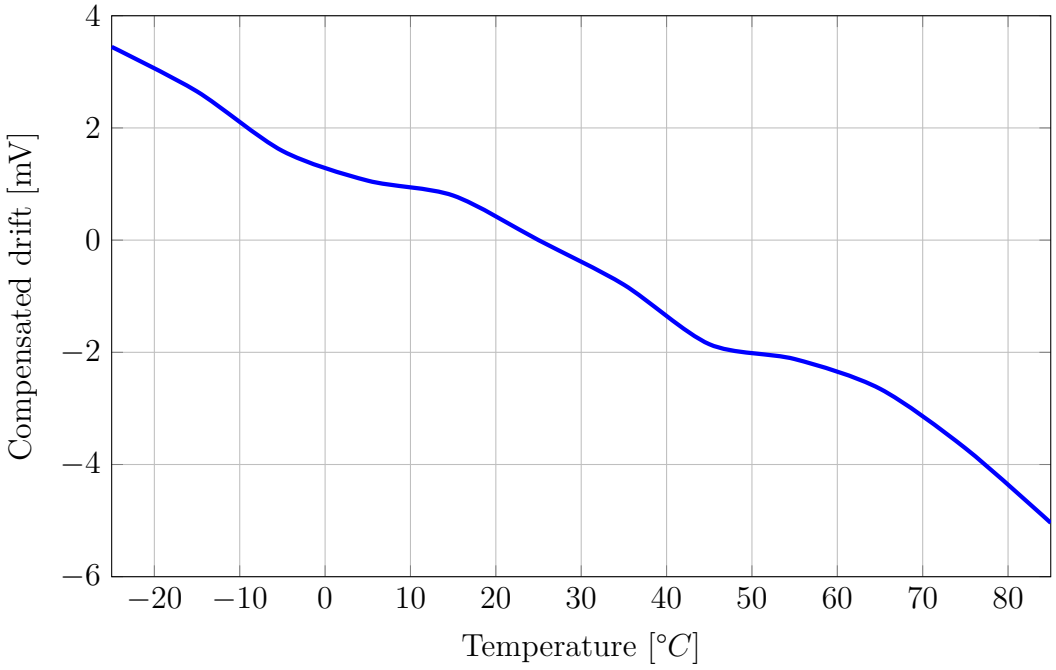


Fig. 4.3: Compensated offset error drift vs. temperature referred to 25 °C

For each temperature reading, the "sensor bias compensating process" explained in the section 2.10 was launched in order to compensate the system's temperate drift. Meaning, that the shifting DAC was compensating the temperature drift. Readings from the plot in the figure 4.3 are just DAC output codes multiplied by the gains present in the signal path from the DAC to the ADC as in the figure 2.33 with the center point at a temperature of 25 °C. The offset voltage seen by the ADC is as close to zero as possible for each temperature thanks to the DAC compensating loop, which means that some voltage output is moving significantly with the temperature.

The most significant voltage temperature drift contributors are the voltage reference ICs. The temperature drift of the REF1 from the figure 2.2 providing the reference voltage for both, the ADC and the DAC has a very low drift - only $901\,\mu V/110\,°C$, also the ADC dynamically reacts to the voltage temperature drift of its reference IC. Thus, the temperature drift of the REF1 is negligible.

On the other hand, the temperature drift of the REF2: $2.75\,mV/110\,°C$ is much more significant and affects the V_{COM} directly. Consequently the V_{COM}, connected to the one side of the FDA, is moving with the temperature and the DAC, connected to the one side of the FDA, is compensating this temperature change. The drift itself is multiplied by the FDA's gain of 2.667 resulting in a total temperature drift of $7.3\,mV$ over the tested temperature range of $110\,°C$.

The overall drift from the figure 4.3 is $8.48\,mV$ within the measured temperature range, which is very close to the drift contributed by the REF2, taking in account other minor drift contributors. It is highly recommended to change the REF2 IC from the current ADR441ARMZ to an ADR441BRMZ, having significantly lower temperature drift. [18]

4.5 Harmonic distortion measurement

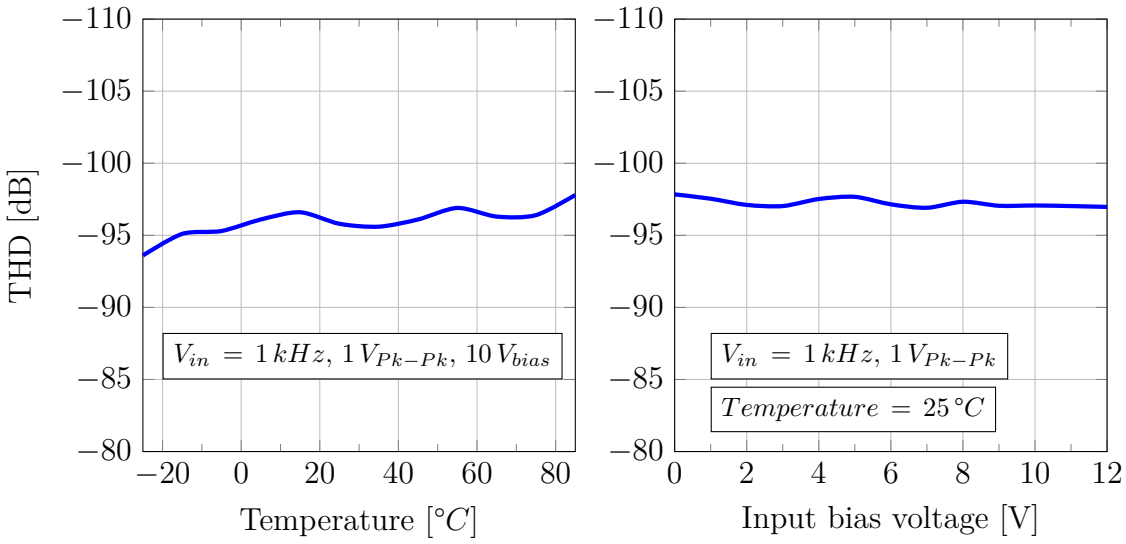


Fig. 4.4: Measured THD vs. input bias voltage and temperature

Harmonic distortion was measured in dependence with temperature and input offset voltage. For both measurements a sine wave with a frequency of $1\,kHz$ and amplitude of $1\,V_{Pk-Pk}$ was generated using a high precision source Audio Precision

SYS-2522. For the temperature measurement a DC level of $10\,V$ was set by the DC calibrator DVC-8500, since it is the most common accelerometer bias voltage value.

Both charts from the figure 4.4 are pretty much flat over the wide range of temperatures and input bias voltages, which is the most important knowledge from the measurement. The overall THD is poor and is most likely still limited by the op amp AD8605. It is very important to have an excellent THD performance since it cannot be averaged out as the noise can be. A high THD helps to recognize defects at the very initial stage. A better op amp, offering better THD performance is recommended to use.

4.6 Linearity measurements

The linearity of the signal chain was measured within the full-scale input range of the signal chain, using the end points of the full-scale range as the reference points. 21 measurements were taken as one half-scale point and 10 points from either side of the half-scale.

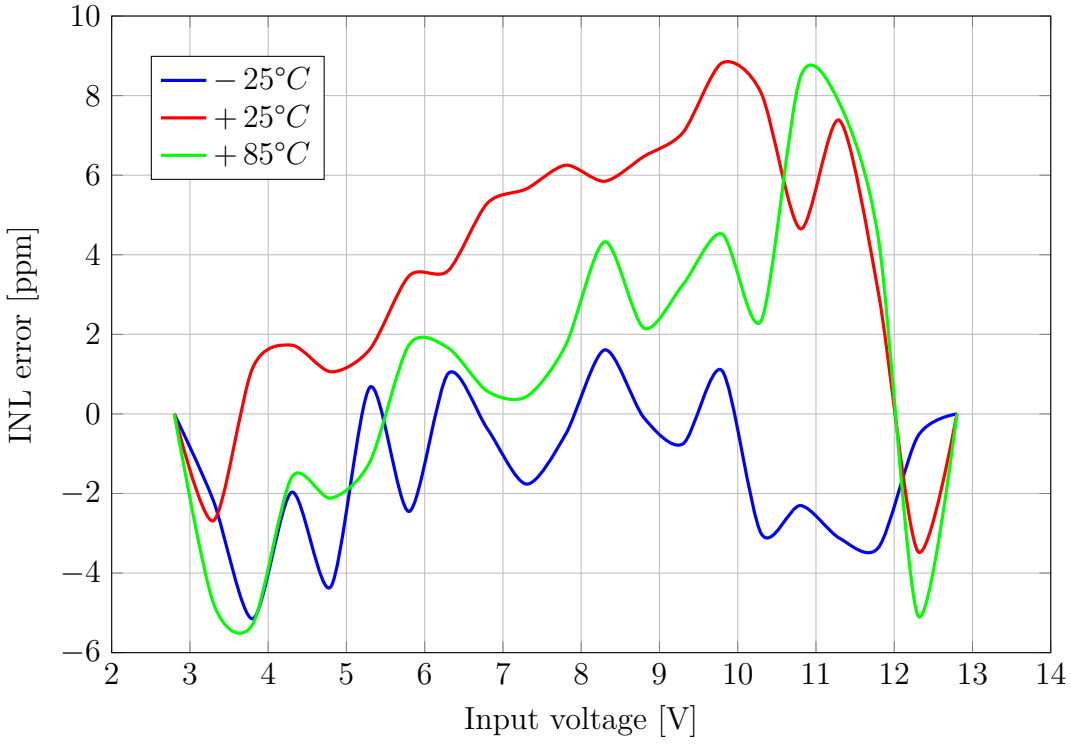


Fig. 4.5: Measured INL error vs. input voltage for various temperatures

As the plot 4.5 shows, the total INL error results in about $14\,ppm$. A precise $8\,1/2$ digit multi-meter HP3458A was used for this measurement with two voltage loops: one for the input voltage of the signal chain and the other for the reference

voltage allowing even more precise measurement. Very good linearity results have been achieved mainly by due to the ADC AD7768-1, which has been chosen for this project because of its excellent linearity, besides other attributes.

4.7 AC-coupling capacitor selection

Even though this design deals with the DC coupled solution, the hardware was designed in a way that a user can easily switch between the AC and the DC coupled variant. The AC coupled solution is explained and measured, only to compare the two solutions. When the AC coupled solution is used a proper type of capacitor must be used to achieve the best performance. There are two main effects worsening the linearity and the noise performance.

Relative permittivity change

The first effect, which must be taken into account when designing a precision AC coupled signal chains is a change of a capacitor's relative permittivity. The relative permittivity of a capacitor depends on an electric field strength, which affects capacitance of a capacitor as follows in 4.1:

$$\varepsilon_r = \varepsilon_r(E) \quad \rightarrow \quad C = C(U) \tag{4.1}$$

where ε_r is the relative permittivity, E is the electric field strength and C is the capacitance. It is obvious that given the same external voltage, thinner dielectric layers found in capacitors with lower voltage ratings will worsen the effect. A persistent DC bias voltage introduces a significant distortion in coupling capacitors.

This effect is more visible when an extremely low frequency signals are applied to the coupling capacitor. Having the frequency low enough, the AC signal is not considered as AC anymore (depends on an input high-pass filter cutoff frequency), but behaves more like the DC signal and the amplitude of the slow AC signal sums with the actual DC bias voltage resulting in even higher DC voltage applied to the coupling capacitor, which may even exceeds the voltage rating of the capacitor.

Piezoelectric noise

Other potential source of error is a piezoelectric noise. Only ceramic capacitors suffer with this phenomenon, since ceramic capacitors are made of crystal-based materials. The piezoelectric effect either generates mechanical displacement after applying an electrical energy to it, or vice versa. Meaning, either mechanical stress of a board can introduces a noise into the system or dielectric layers contract or

expand with applied voltage, which is directly affecting a capacitor's capacitance by a following equation 4.2:

$$C = \frac{\varepsilon \times A}{d} \tag{4.2}$$

where A is an area of a dielectric layer and d is a distance between the layers. The piezoelectric effect in ceramic capacitors is more visible at very low frequencies and very high amplitudes applied to the coupling capacitors. Some of the capacitors can easily lose 80 % of their nominal capacitance and introduce huge portion of noise into the system.

Combining the two above mentioned effects together: not only the cutoff frequency of a high-pass filter is moving significantly, but also electrical noise is introduced.

A polyester or a better C0G ceramic capacitor would improve the linearity significantly, but only small values of C0G capacitors are manufactured (tens of nF), which would not satisfy a noise consideration of signal chain's input impedance. Tantalum capacitors are not as good as the C0G's, for this specific use case, but do not suffer with any of the mentioned phenomenon and wide range of capacitance values are manufactured as high as tens of µF.

Three different types of capacitors were tested with a worst-case input signal scenario, where the input frequency is limited by a precision sine source used for the measurements: Audio Precision SYS-2522. The parameters of the used signal were: $10\,V_{Pk-Pk}$ input AC signal with a frequency of $12\,Hz$ and an input bias voltage of $10\,V$. Achieved distortion performance displays a table 4.3 below The f_c column is the high-pass filter cutoff frequency in connection with the $50\,k\Omega$ resistor acting as the input impedance.

Tab. 4.3: Coupling capacitor selection according to their physical attributes and measured harmonic distortion with input frequency of $10\,Hz$

Type	**Value [μF]**	**Voltage [V]**	**Package**	**f_c [Hz]**	**THD [dB]**
Tantalum	10	35	Leads	0.32	-112.7
X5R	10	25	0603	0.32	-51.6
X7R	3	50	0805	1.06	-67.2
DC coupled	-	-	-	0	-113.0

As the table shows, the poorest performance is achieved by ceramic $X5R$ and $X7R$ capacitors - as expected. The $X7R$ option holds better because of the higher voltage rating, significantly larger total area of capacitor electrodes where nor the

piezoelectric effect, neither the voltage-capacitance dependency is as strong as in the $X5R$ option. Also, the $X7R$ dielectric, having capacitance only $3\,\mu F$ fitted into a significantly large package, is not so dense and is well spread across the package which contributes to the better performance. Please note, that the difference of performance between the $X5R$ and the $X7R$ capacitors is not affected by their slightly different material types but is only affected by their physical dimensions.

The tantalum capacitor achieves nearly as excellent results as the DC coupled variant but at the input signal's frequency of only $12\,Hz$. Once the frequency of the input signal approaches or falls below the cutoff frequency of the high-pass filter, the the DC coupled solution starts prevailing rapidly. This behavior is very natural an expected since there is no sense in measuring or simulating this scenario.

4.8 AC vs. DC-coupled solution

The main difference between the 2 solutions is complexity of a signal chain, which goes along with a price, and precision at DC and low frequencies. Where the AC coupled requires less complexity and lacks precision at low frequencies.

A higher noise is also expected in DC coupled solution due to the DAC output and lack of a high-pass filter at the input of the signal chain. The X7R capacitor from the table 4.3 was used in the input high-pass filter for a following measurement.

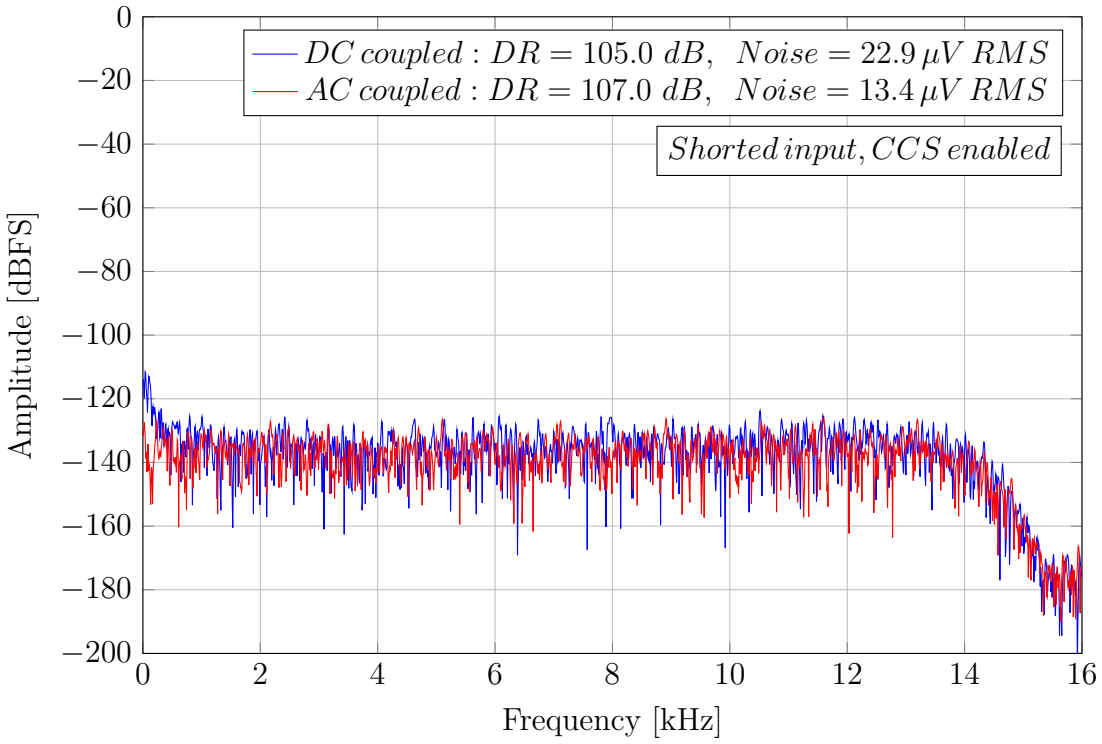


Fig. 4.6: AC vs. DC coupled solution wide band noise comparison

The difference between the two plots is mainly the noise performance. As the plot 4.6 above shows, the DC Coupled solution (blue trace) is passing more 1/f noise to the system, lowering the dynamic range of the frequency spectrum. The difference in DR is only in about of $2\,dB$ which is less than 50 % change.

4.9 Coupling capacitor impact

The theory behind selection of the coupling capacitor explained in a subsection 4.7 was proven with real measurements displayed in a plot below.

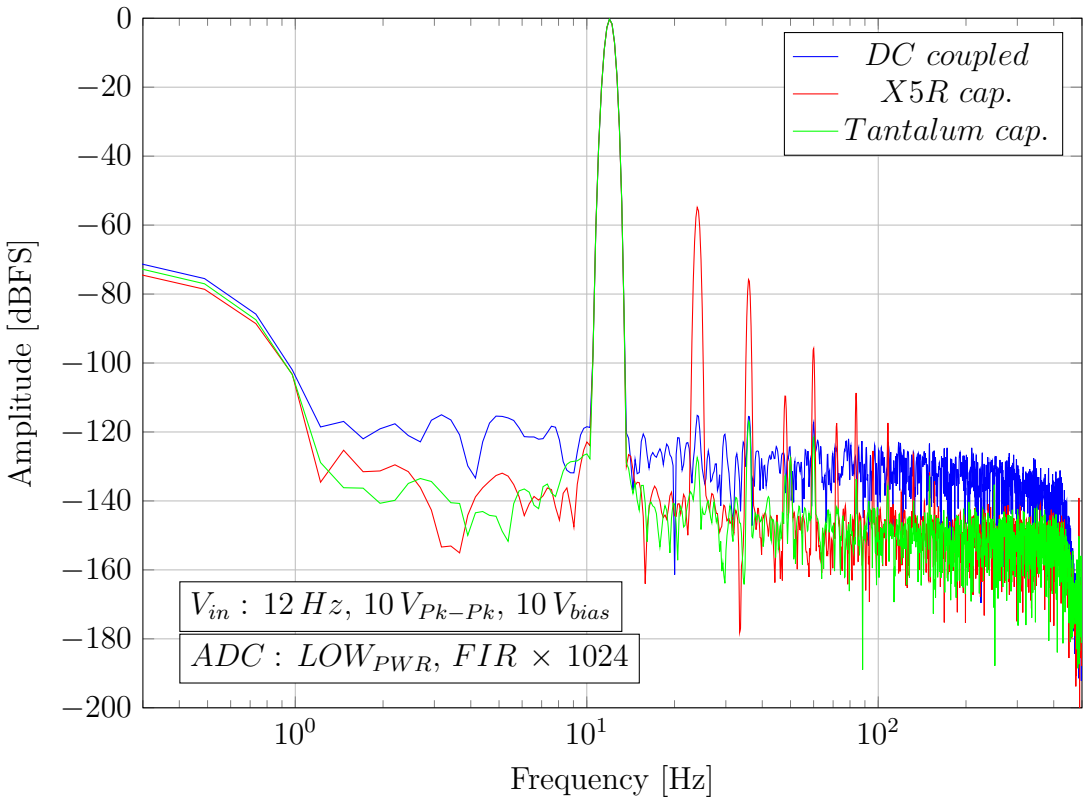


Fig. 4.7: Frequency spectrum comparison of different coupling approaches

A plot on the figure 4.7 above compares three coupling scenarios: DC coupled, AC coupled with a tantalum capacitor and with a $X5R$ capacitor. The capacitor types and the results from the 4.3 are related to this set of measurement. The x axis of the plot is in logarithmic scale allowing the very low frequency area to be depicted clearly.

The measurement was taken with the ADC's FIR filter OSR set to very high 1024, resulting in a $500\,Hz$ wide frequency spectrum according to the formula 2.37, allowing the spectrum to be investigated in detail at the very low frequencies. The testing signal was chosen to be as high as the full-scale input range of the signal

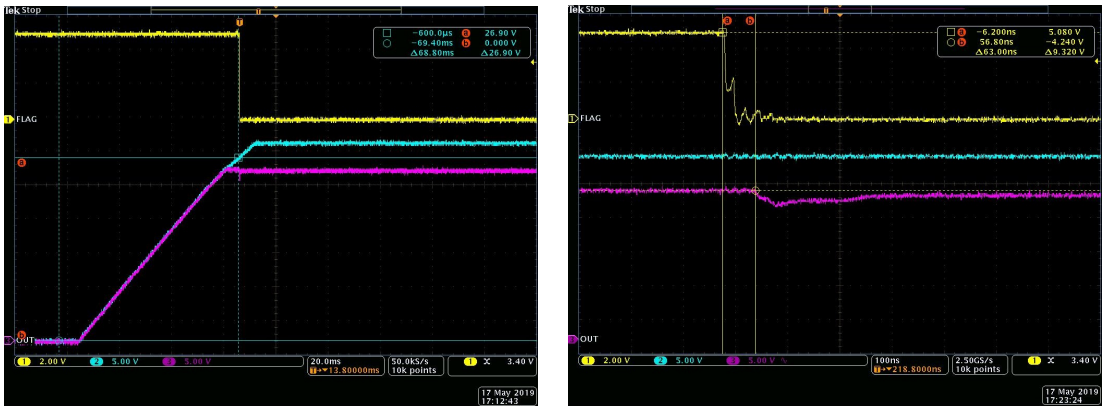
chain with the frequency of 12 Hz due to possible interference with the 50 Hz from the mains which might affect the 5^{th} harmonic and ruin the THD measurement - not allowing us to measure the distortion caused solely by the capacitor, which might have occurred for a 10 Hz input signal frequency, being the lower frequency limit of the used signal generator.

The red trace produces the worst response in terms of linearity, proving the concepts from 4.7, where the X5R capacitor was expected to have the worst linearity results. The green trace representing the tantalum capacitor has an excellent noise and very good linearity performance, mostly because the input frequency is still as high as 12 Hz. The DC coupled, blue trace, has the best linearity, but significantly higher noise having the noise floor at about only $-102\,dB$ in contrary with the noise floors of the AC coupled solutions having it as low as $-117\,dB$. The noise floor of the red trace is as poor as $-88\,dB$. Please note, that the noise floor as low as $-117\,dB$ was achieved by the OSR set as high as 1024, averaging the noise out of the frequency spectrum.

The higher noise floor of the DC coupled solution is caused by the 1/f noise coming mainly from the CCS, input signal source, the DAC and practically from any semiconductor component. Looking at the plot 4.7, the corner frequency of the 1/f noise might be assumed to be at as high as 700 Hz and it is quite significant in the plot 4.7 displaying the frequency spectrum of only 500 Hz.

4.10 Input protection switch test

As explained in the subsection 2.3, a protection switch from the figure 2.5, was used in the design for both, the ESD and over-voltage protection. Following pictures are oscilloscope logs showing the protection switch being activated and tested.



(a) Protection switch being activated

(b) Detailed activation of the switch

Fig. 4.8: Input fault switch protection test

The pictures from the figure 4.8 was captured by a digital oscilloscope Tektronix DPO4104B-L. The figure depicts three signals: the yellow trace is a Fault Flag (FF, Flag) from the protection switch, the cyan is the switch input voltage and the magenta output voltage. The over-voltage protection is activated (for this specific circuit scenario) whenever the input voltage oversteps VDD (of the switch IC) by a threshold voltage V_t which is $0.7\,V$ for this chip.

A slowly rising voltage with maximum level of $29\,V$ was connected to the input of the switch. As the input voltage rises, the output voltage is copying its pattern to the level of $25\,V$, where the output voltage does not rise any more, but the switch is still open. This point is a limitation of the CCS, in which the current stops flowing out of the CCS due to the rising input voltage which is pushing to the CCS from below, not leaving a room for the voltage dropout across the R_{out}. The dropout voltage defined in 2.4 was limited to the dropout over the LT3092 itself, being $1.2\,V$.

At the voltage level of $26.9\,V$, which is marked in the oscilloscope log a) in the figure 4.8, the switch is finally activated, since the following voltage threshold has been achieved:

$$VDD + V_t = 26.2\,V + 0.7\,V = 26.9\,V \tag{4.3}$$

The input voltage continues to rise, but the output voltage seems to be at the same level. In fact, the output voltage is falling so slowly, that the oscilloscope set to this time domain, cannot capture it. In order to quiet the output current noise from the CCS a large capacitor C_{SET} and a big resistor R_{SET} from figure 2.6 were placed into the design, creating a time constant, which is at this scenario very slowly discharging:

$$\tau = R_{SET} \times C_{SET} = 120\,k\Omega \times 10\,\mu F = 1.2\,s \tag{4.4}$$

This extraordinary long time constant affects the start-up time as well as recovery time after the CCS was externally limited. The time constant does not affect the performance of the protection switch though.

As the oscilloscope log b) from the figure 4.8 shows, the switch is successfully turned off after about $63\,nS$. At this point measured from the moment when the flag starts to fall, a voltage glitch is visible at the magenta output voltage reading, caused by the switching event.

4.11 Power consumption

As the figure 2.20 shows, the whole design is powered from $3.3\,V$ rail. There are few DC-DC converters present on the board, where the most used power rail is the $5\,V$

rail, from which the analog front-end, the ADC and the CCS is powered.

A typical configuration of the system was established for a narrow bandwidth measurement, in which the power consumption was measured:

- ADC register settings:
  - Power scaling mode: LOW power mode,
  - MCLK divider: MCLK/16,
  - VCM output: (AVSS - AVDD) / 2,
  - Digital filter: FIR filter with OSR at 32,
  - AIN buffers: precharge ON,
  - REF buffers: precharge ON,
  - GPIO: disabled,
- DAC settings:
  - DAC buffer: enabled,
  - DAC output: set to HS,
- External MCLK: 16.384 MHz crystal,
- FDA: enabled in the full power mode.

This configuration has been used for most of the measurements, ensuring consistent measurement results. Changing any of the above-mentioned settings affects not only the performance, but the current consumption as well. The most significant consumption contributors which can be scaled and changed are the FDA and the power scaling register of the ADC.

Tab. 4.4: Current consumption of the 5 V rail for different ADC power modes

ADC power mode	**FDA power mode**	**Typical speed (kSPS)**	**Conspumption (mA)**
Fast	Full	256	16.3
Median	Low	128	12.4
Low	Low	32	12.1

The table 4.4 above displays the current consumption of the analog front end with the ADC solely, for different ADC power modes. For this measurement, the always-present DC-DC converter providing a high voltage output for the sensor was disabled, since it the most significant current consumption contributor on the PCB. Its bulky consumption would hide the fine consumption changes introduced by the ADC which were meant to be shown.

For these measurements the input and reference buffers were disabled. By switching from the FDA's low to full power mode, the FDA would provide a user with wider

bandwidth and better noise and linearity performance. By enabling the buffers, user will achieve better linearity and better noise performance, for the cost of a higher current consumption. For more information about matching a diver amplifier and consumption scaling of the analog front end, with the AD7768 family please visit an Application Note AN-1384, provided by the Analog Devices. [12]

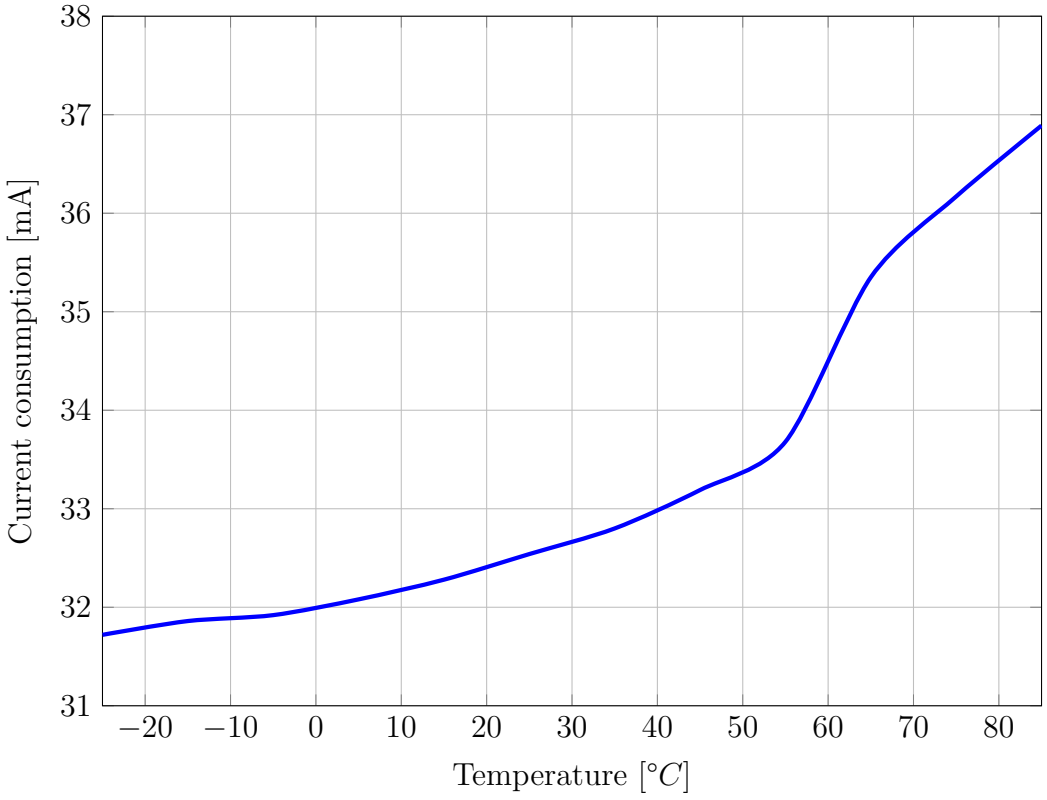


Fig. 4.9: Measured power consumption of the 5 V rail vs. temperature

As the chart from the figure 4.9 shows, the whole system underwent a current consumption test over the temperature range, ensuring a stability at the higher temperatures. For this measurement, the $26\,V$ DC-DC converter was enabled and a $1\,k\Omega$ resistor was placed across the CCS to the ground, loading the CCS and simulating the sensor consumption. The consumption raised in $5\,mA$ within the temperature interval over $110\,°C$ without any unexpected current peaks, which is very acceptable

5 Vibration spectrum analysis

The following chapter deals with characterization of a vibration frequency spectrum and defining possible types of faults, which might occur in certain scenarios.

5.1 Vibration measurement background

As the whole thesis is about designing a system capable of predicting rotating machine defects from vibration spectrum of the machine itself, it would be shame not to include any vibration measurements. Since there was only limited time for the project to complete and the project started from scratch, the main demand was to focus more into hardware design and firmware data processing, rather than the measuring of the vibrations itself since the vibration measurement is already known process with plenty of studies behind it.

The priority number one in this project was to show to a customer that our solution is capable of low-noise and high linearity vibration measurement, rather than the solution can recognize a specific defect from a frequency spectrum.

For a reliable acceleration amplitude measurement, it is necessary to possess a shaker table, which provides an user with a known amount of acceleration. A measurement system, like this one, can be calibrated using the shaker table. A business unit covering this project did not have the shaker table at that time, thus following measurements serve only as a demonstration.

A quick setup for the vibration measurement on a real device was created using a small PC blower with the accelerometer attached to it. The setup is shown on appendixes C.5 and C.6. One might state an objection about attaching and fastening the sensor to the blower with a considerably loose connection using a zip tie, which might introduce errors into a measurement. This setup although, is only a demonstration.

5.2 Looseness

To find the looseness in a frequency spectrum one must look for a long set of considerably high amplitude harmonics, where the harmonics might be even higher than the carrier frequency, but tend to fall with rising frequency.

A figure 5.1 shows a typical example of looseness measured on the PC blower without inducing the defect. According to the theory, amplitude of harmonics goes lower with rising frequency except the 3^{rd} harmonic, which amplitude is higher than the amplitude of the 2^{nd} one, but this behavior is very acceptable and expected in some cases of measurement.

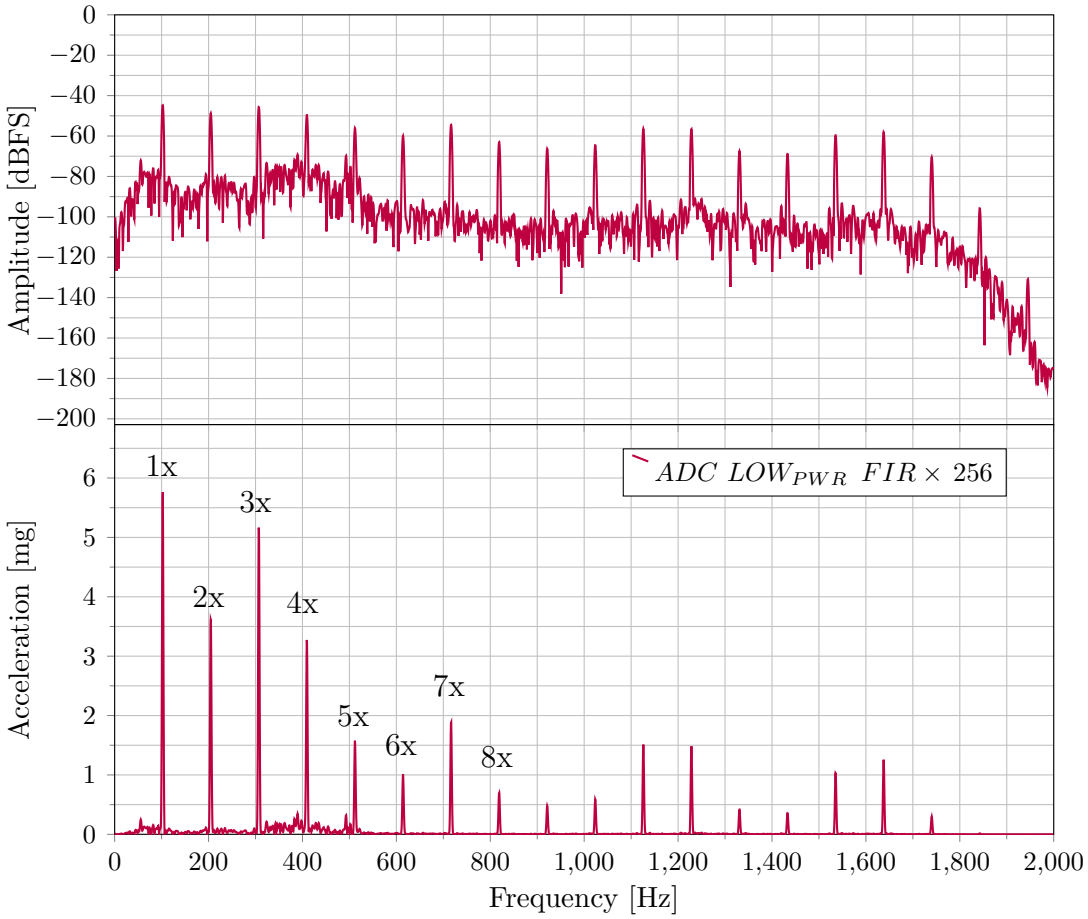


Fig. 5.1: Frequency spectrum showing looseness

In this specific type of measurement it is very comfortable to actively narrow the frequency spectrum by changing the OSR of the digital filter, as we do not need to take a look a the full spectrum. Narrowing the bandwidth will lower the bind width leading to an increased precision in the lower frequencies. After substituting into the equation 2.37, the resulting ODR will be $4\,kHz$, which is a $2\,kHz$ wide frequency spectrum.

The frequency spectrum in the figure is displayed as an amplitude in decibels and as an acceleration in gravity units 'g', just to show the difference between the two plots. Generally, the decibels are more preferable fro any ADC measurement, but for example in this type of acceleration measurement it is more convenient not to use decibels, because a user is interested only in peaks position and amplitude, not in a overall frequency spectrum shape. It is also more obvious to spot amplitude difference in gravity units than in decibels.

Sensitivity of the used sensor PCB 333B52 is $1000\,mV/g$. The conversion from decibels, as the standard output of the ADC down to volts and consequently to gravity units is very straightforward. The equation 3.16 for converting decibels related

to FS must be used in order to get the correct, voltage reference dependent voltage, which is already the result in the gravity units thanks to the sensor's sensitivity. [5]

5.3 Imbalance

The imbalance was artificially induced by anchoring a little weight to one of the fan's blades. The defect was clearly visible and audible even without measuring it. If the defect were unknown to us, it would be very easy to detect, as the amplitude of imbalance reacts to the rotation speed.

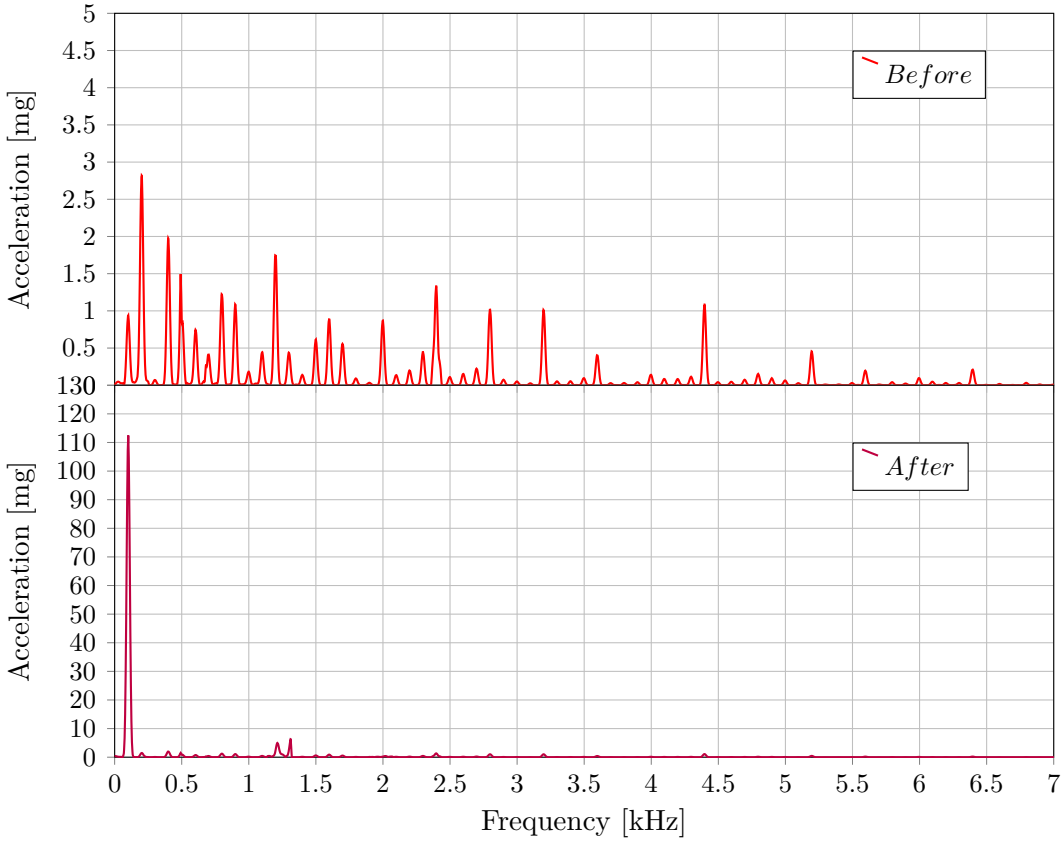


Fig. 5.2: Frequency spectrum showing imbalance before and after inducing the defect

The figure 5.2 consists of two charts depicting a before and an after scenario. In the before scenario, the amplitude of the fan's rotation frequency is not any higher than $1\,mg$, the 2^{nd} harmonic has even higher amplitude than the carrier. The amplitude of the carrier rises more than 110-times after inducing the defect.

Please note, that amplitudes of other visible peaks and their positions might differ in the two scenarios, since the sensor was taken off and then put back allowing a user to induce the defect. There are several defects present in the before scenario frequency spectrum, which although will not be covered.

6 Conclusion

The main challenge of the thesis was to investigate, to design and consequently to prove, that the DC coupled signal chain offers better performance, especially in a very low frequency spectrum than the AC coupled one. The hardware has been designed in a way, that a user can easily switch between the two variants on the same PCB. A special care has been taken to deliver a low noise and high linearity design. Used parts selection was highly affected by the company, where the Analog Devices is trying to promote newly released parts and test certain parts and topologies in a specific application.

Thanks to the shifting DAC, the sensor bias voltage compensation process is done automatically without a need of a manual trimming for each sensor separately. The DAC - ADC successive approximation control loop allowed us to compensate the system's offset voltage introduced by the sensor's bias voltage down to less than $80\,\mu V$, allowing the amplitude measurements to be eminently accurate at the very low frequency spectrum and DC levels.

The FFT processing carried out locally on a microcontroller's DSP module did not seem to be the most accurate at the first glance. But it has proven itself to be remarkably accurate, when compared to the FFT core offered by the Analog Devices to the customers in a form of a LabView code. Comparing the SNR results from the table 3.2 we can see the variation is only $2\,mdB$. As the only limitation of the FFT processing was very low number samples available on the DSP module which has been used, being only 4096.

As expected, the total integrated noise of the DC coupled solution is slightly higher, looking the table 4.1, caused mainly by the DAC voltage output, resulting in a DR difference of about $1.7\,dB$ in a wider frequency range of $64\,kHz$, making the dynamic range as good as $105.4\,dB$ with the input terminals of the signal chain shorted.

The THD is quite poor over the wide range of frequencies and input bias voltages for both solutions. Even though the table 4.3 shows the THD to be $-113\,dB$, which is very close to considerably enough, but the result is for the FS, low frequency input signal, thus the THD is expected to be very good at this configuration. For a wide range of scenarios it is not any better than $100\,dB$ according to the figure 4.4. This limitation is most likely to be caused by a non-sufficient harmonic distortion capability of the op amp AD8605 used in the first stage of the signal chain. To meet the high THD measurement requirements, it is highly recommended to replace the op amp in the following revision fo the PCB.

The cutoff frequency of the AC coupled solution's input high-pass filter has been experimentally set to $1\,Hz$, allowing us to investigate effect caused by the presence

of the capacitor in the signal path, not effect caused by the actual position of the $-3\,dB$ point. Changing the cutoff frequency from actual $1\,Hz$ to a higher frequency, just to prove that the DC coupled solution is superior to the AC, would not make any sense, since this behavior is very natural and expected. Further tweaking of the cutoff frequency in order to push the $-3\,dB$ point closer to zero and finding out the lowest frequency, at which the DC coupled design starts to prevail over the AC is AC-coupling related, since it is not covered in this thesis.

The lowest frequency used for the designs comparison was $12\,Hz$ depicted in the figure 4.7 and the THD results of the two solutions were very close, with the DC coupled solution slightly prevailing. That very close match of the THD results has only been achieved by a very carefully chosen physical structure, package and material of the coupling capacitor.

Vast majority of the included measurements were taken using the data acquisition board itself, running the already evaluated firmware. The five-layer PCBs were designed by a third person - a skilled PCB designer from the company. A sensitive layout areas like ADC analog inputs layout was taken from an existing PCB design of the original AD7768-1 evaluation board to minimize board-to-board performance mismatch. The schematics are included in the appendix A and the physical layout with the parts placement are included in the appendix B.

Lastly, some demonstration measurements have been included into the final chapter 5, showing capability of a mechanical defect detection on a pc blower. Only the most common defects: looseness and imbalance are shown, where the imbalance was artificially induced by putting a small weight on the pc blower's blade to strengthen the effect of imbalance. Photos of the demonstration measurement setup as well as photos of the hardware solution are included in the appendix C.

The results of this thesis demonstrate, that the DC coupled solution is more challenging, but the additional effort is returned in significantly improved performance. All the demanded instruction from the topic of the thesis have been successfully elaborated and fulfilled. The designed solution is capable of precision vibration measurement.

Since this project has proven itself to be potentially successful, judging from the achieved results, it has already been handed over to another skillful designer, to finish the job. Next steps including merging the hardware design into one PCB, amplitude calibration using a shaker table, more robust software support and integration etc. are required to work on. From my point of view, the internship in such a great and recognized company as Analog Deices truly is was very beneficial. Not only in terms of significant amount of acquired technical knowledge, but also in terms of English language improvement and knowing other cultures. It was a great experience.

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List of symbols, physical constants and abbreviations

AAF	Anti-Aliasing Filter
ADI	Analog Devices (the company)
AIN	Analog Input
CCS	Constant Current Source
DAC	Digital to Analog Converter
dBc	Decibels related to the carrier
dBFS	Decibels related to the Full Scale
DFT	Discrete Fourier Transformation
DR	Dynamic Range
DSP	Digital Signal Processor
ENOB	Effective Number Of Bits
ESD	Electro Static Discharge
FDA	Fully Differential Amplifier
FFT	Fast Fourier Transformation
FIR	Finite Impulse Response
FS	Full Scale
HS	Half Scale
LDO	Low-dropout (voltage regulator)
LSB	Least Significant Bit
MCLK	Master Clock
MSB	Most Significant Bit
ODR	Output Data Rate
OSR	Oversampling Ratio
PCB	Printed Circuit Board
RMS	Root Mean Square
RPM	Revolutions Per Minute
RRIO	Rail-to-Rail Input and Output (operational amplifier)
RSS	Root Sum Squared
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SINAD	Signal to Noise And Distortion ratio
SNR	Signal to Noise Ratio
SPS	Sample Per Second
THD	Total Harmonic Distortion

List of appendices

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A Schematics

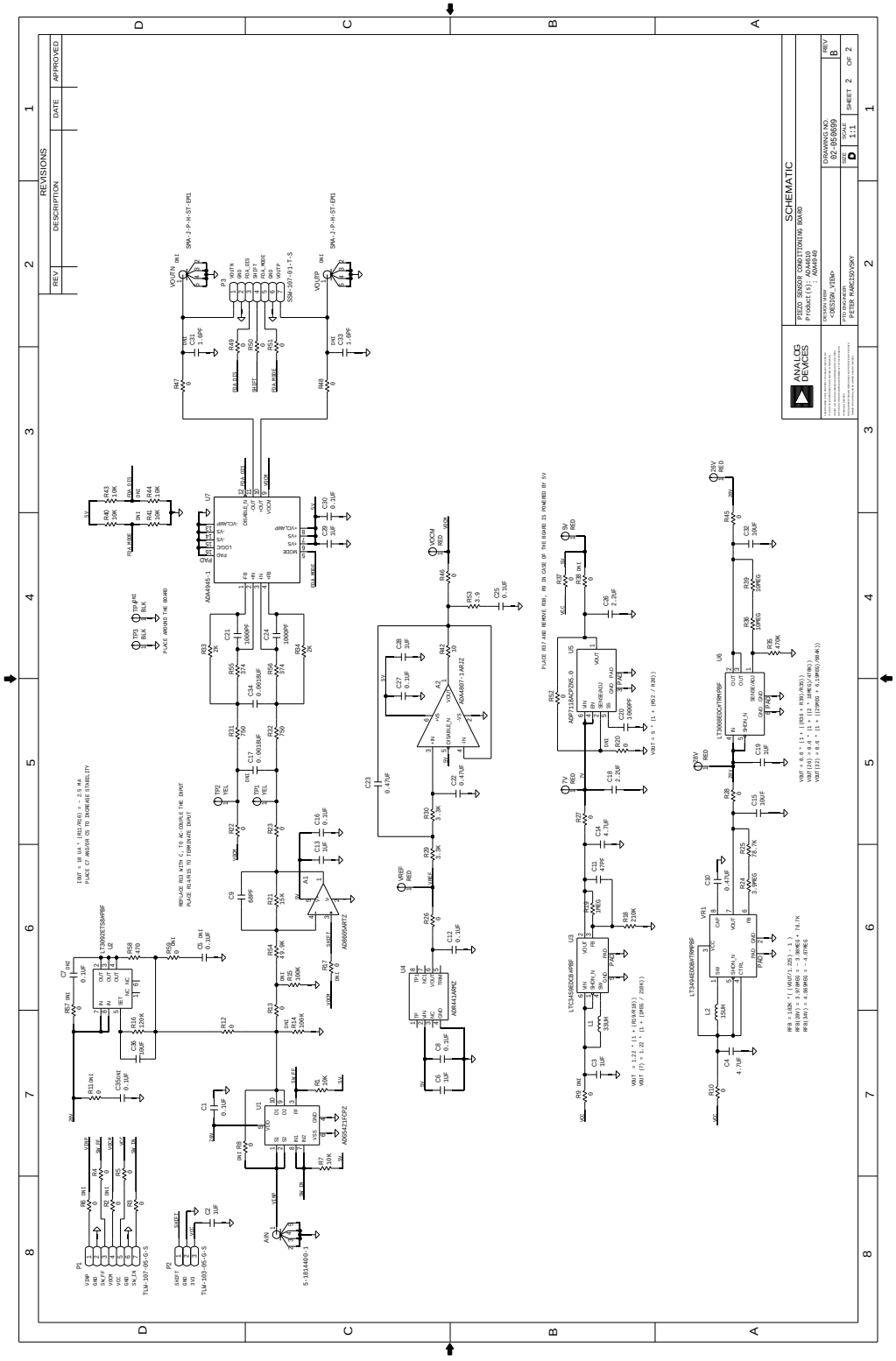

Fig. A.1: Full schematic of the piezo sensor conditioning board

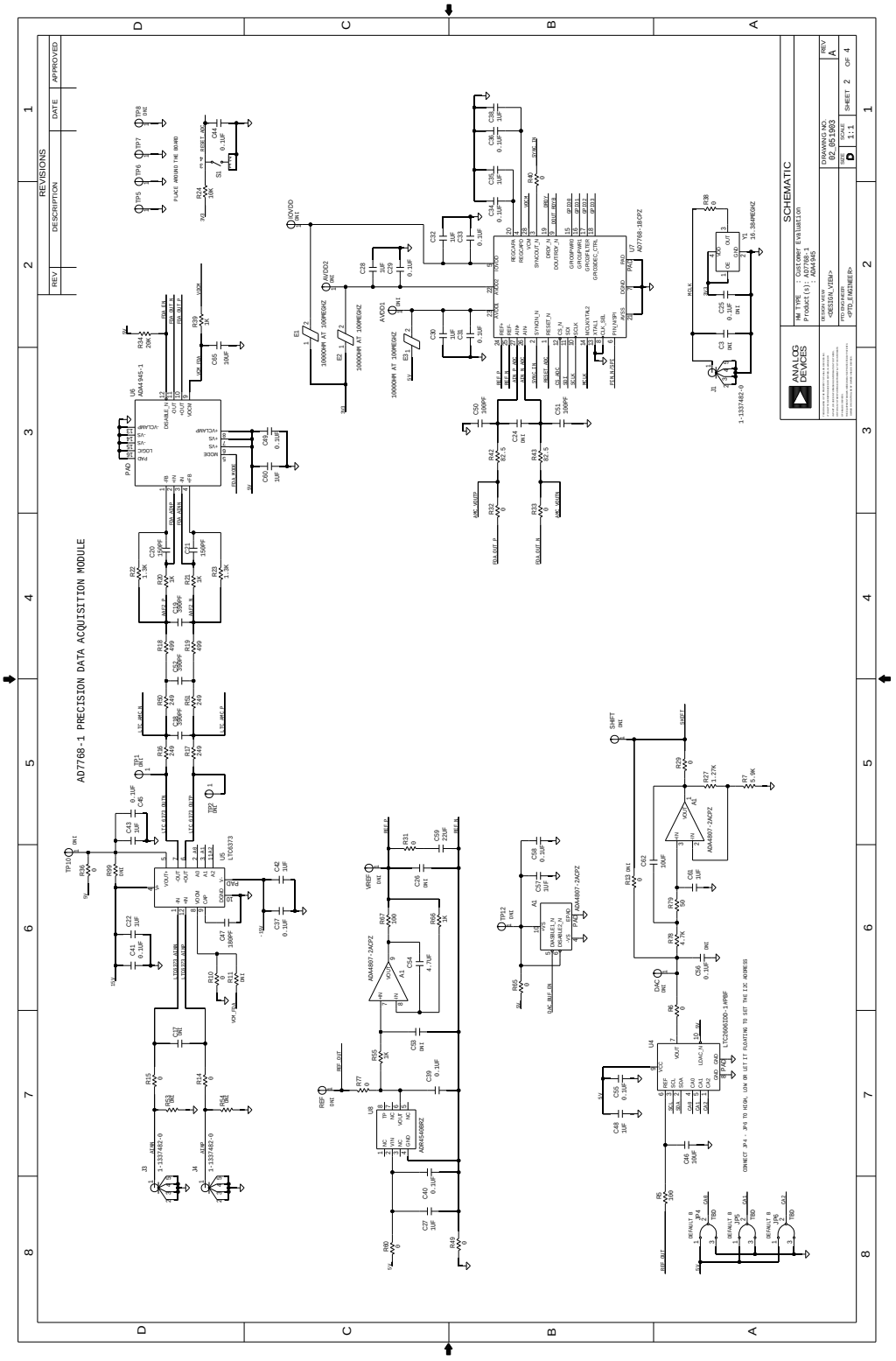

Fig. A.2: Main schematic part of the data acquisition board

B Parts placement

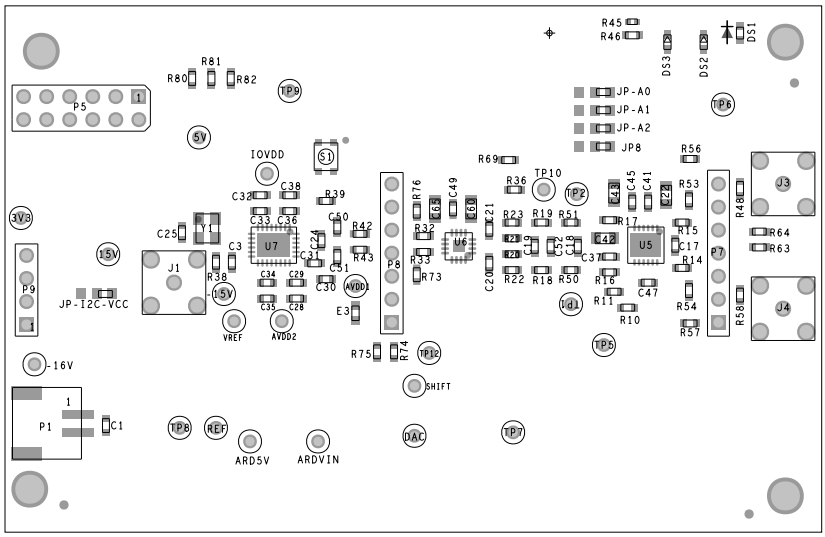

Fig. B.1: Parts placement of the data acquisition board from primary side

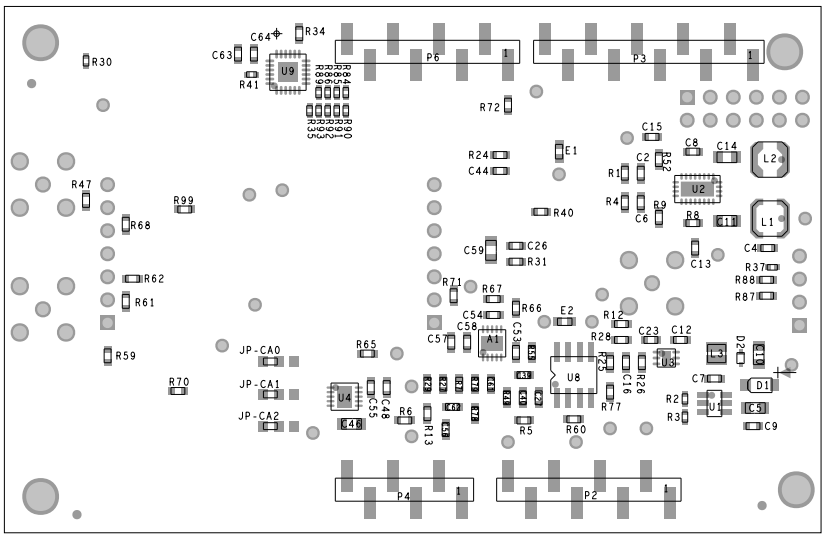

Fig. B.2: Parts placement of the data acquisition board from secondary side

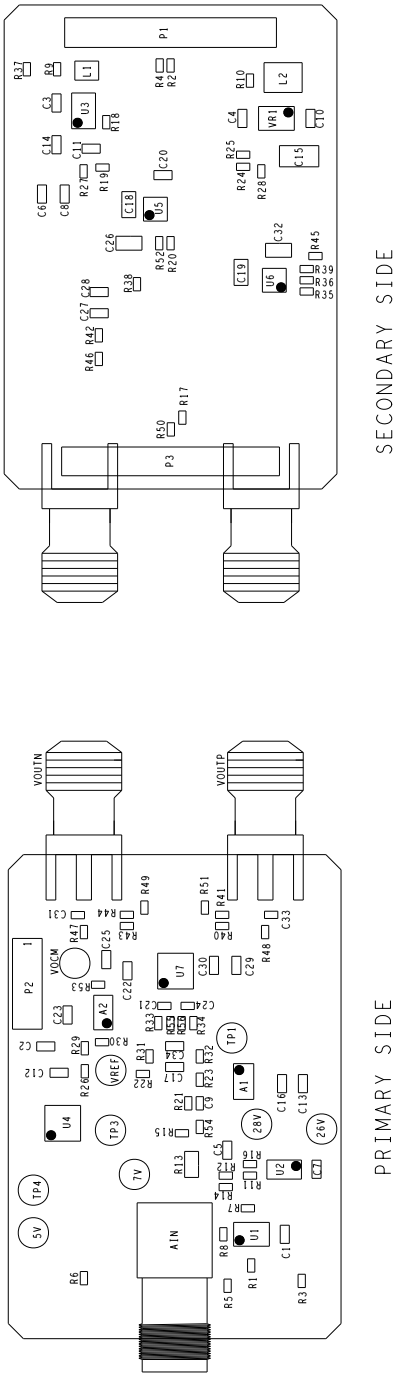

Fig. B.3: Parts placement of the piezo sensor conditioning board from both sides

C Photos of hardware implementation

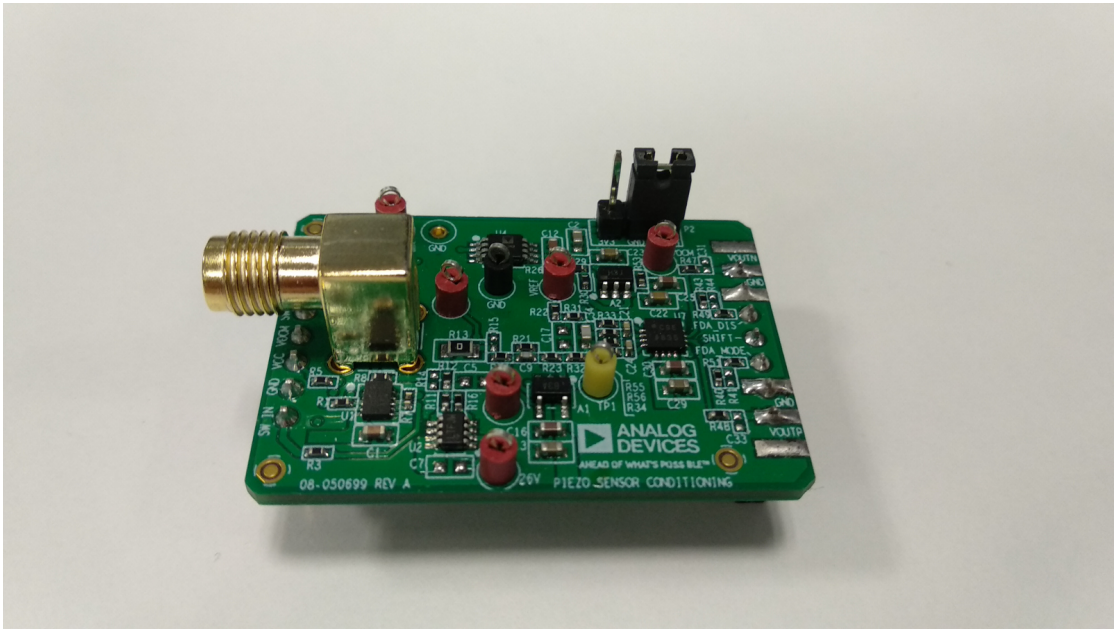

Fig. C.1: Piezo sensor conditioning board

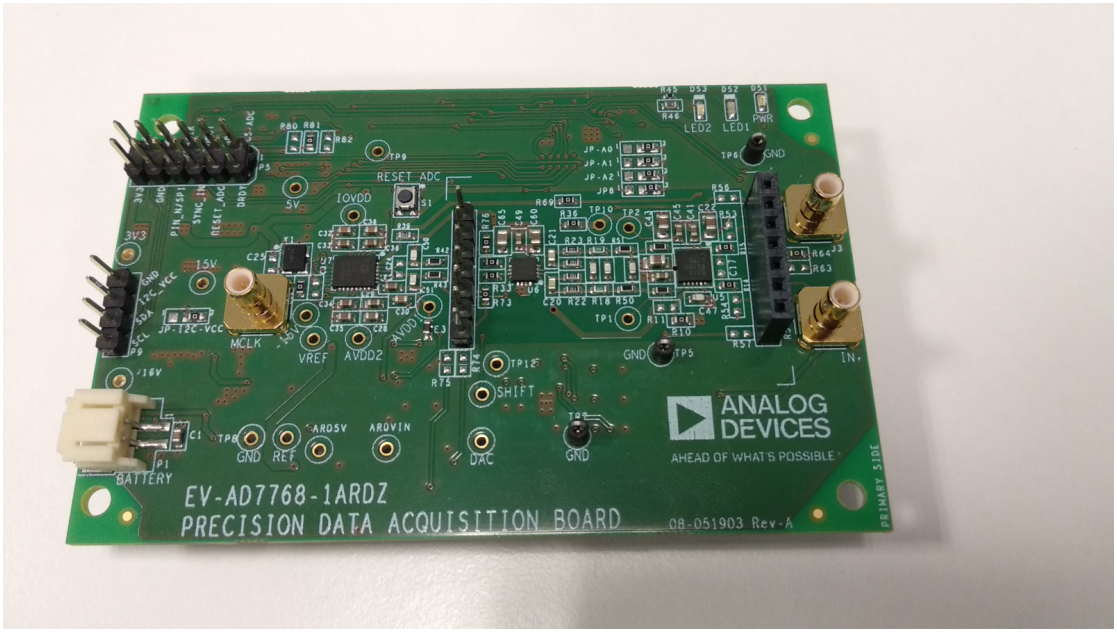

Fig. C.2: Data acquisition board

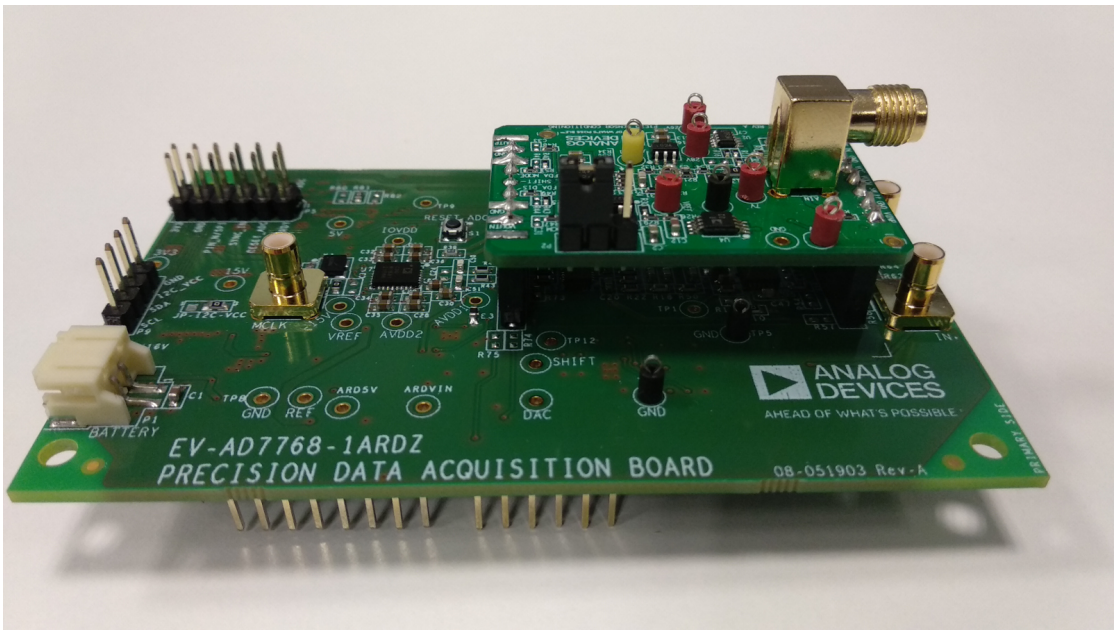

Fig. C.3: Both, the piezo sensor conditioning board and the data acquisition board connected together

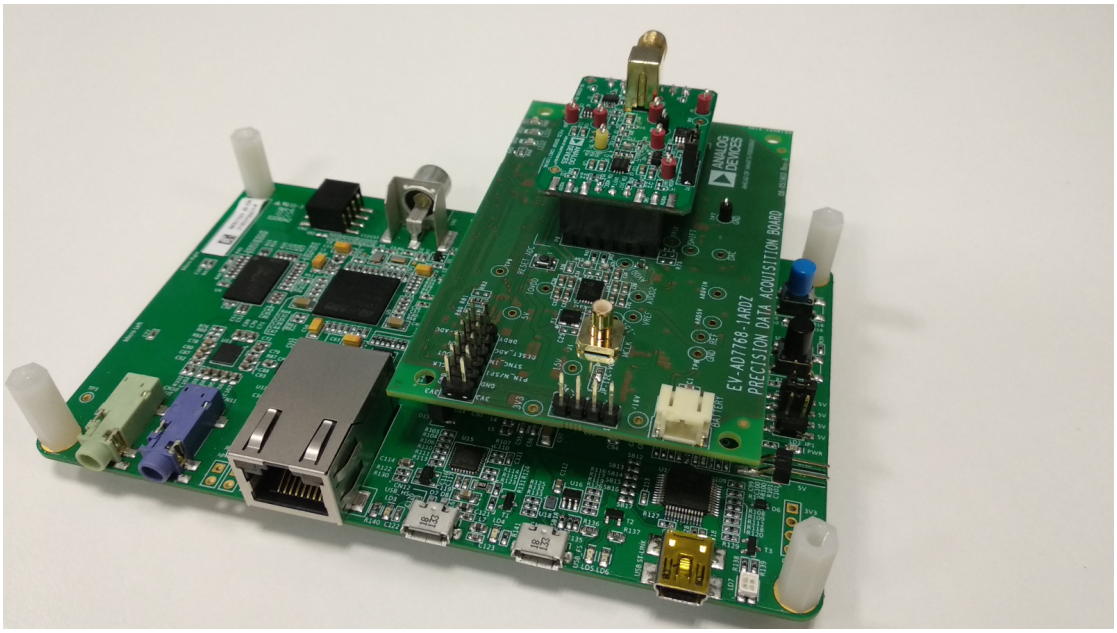

Fig. C.4: Both boards connected to the STM development board

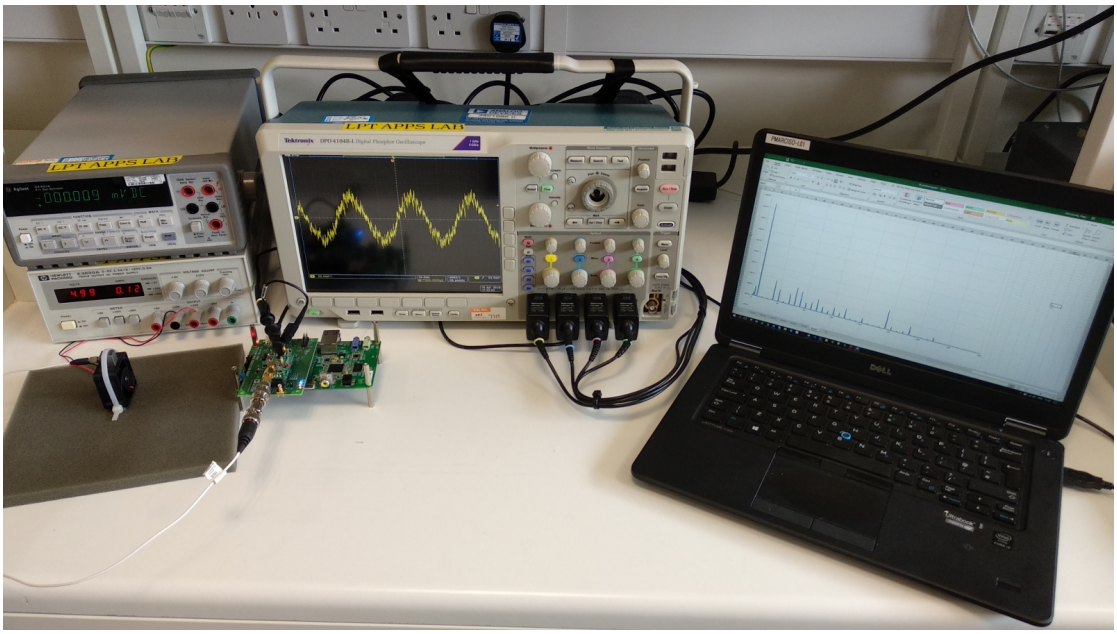

Fig. C.5: Testing setup for vibration monitoring

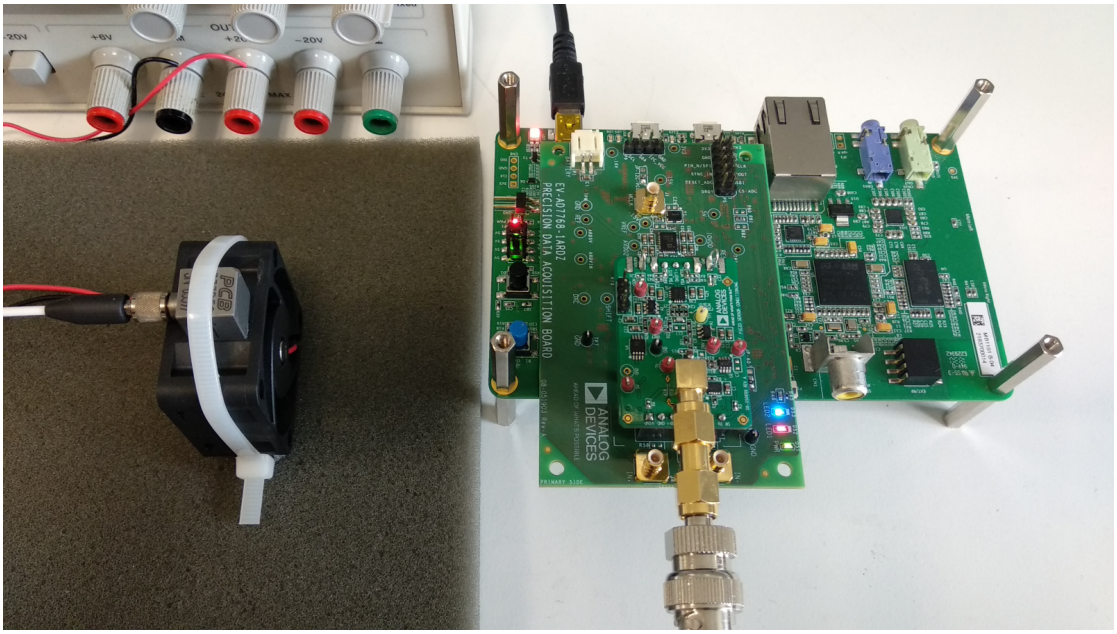

Fig. C.6: Detail of the testing setup for vibration monitoring

D Content of the attached CD

The attached CD contains schematics, assembly documents and bill of materials for both PCBs. It also contains all vector graphics used in this thesis in both, .pdf and .svg formats, together with used and some additional photos and oscilloscope captures in full resolution.

```
/ ..... root of the CD
├── PCB_data_acquisition
│   ├── data_acquisition_brd_BOM.xlsx ..... Bill Of Materials
│   ├── data_acquisition_brd_schematic.pdf
│   └── data_acquisition_brd_assembly.pdf ..... Components placement
├── PCB_piezo
│   ├── piezo_brd_BOM.xlsx
│   ├── piezo_brd_schematic.pdf
│   └── piezo_brd_assembly.pdf
├── photos ..... Photos in full resolution
└── graphics ..... Used graphics in both, .pdf and .svg formats
```