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COMPARISON AND OPTIMIZATION OF DC/DC POWER CONVERSION TOPOLOGIES USING GAN FET TECHNOLOGY FOR HIGH EFFICIENCY AND POWER DENSITY POWER CONVERTERS

SROVNÁNÍ A OPTIMALIZACE TOPOLOGIÍ PRO DC/DC KONVERZI ENERGIE S POUŽITÍM TECHNOLOGIE GAN FET PRO MĚNIČE S VYSOKOU ÚČINNOSTÍ A OBJEMOVOU HUSTOTOU VÝKONU

DOCTORAL THESIS
DIZERTAČNÍ PRÁCE

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BRNO 2021

Abstract

Focus of this thesis is the analysis of the current state of GaN semiconductor technology in power electronics and its application on DC/DC converter, optimized for high efficiency and high power density with the intention to use it in server and telecom applications.

The theoretical part analyzes problems and challenges related to novel GaN technology, such as gate driving for various internal structures, layout optimization for cooling of minimized surface mount packages without constraining parasitic elements affecting switching performance. Precise losses calculation for totem-pole power factor correction converter using novel GaN technology is included. Results and ideas resulting from theoretical analysis of various problems are applied in the design of prototype and verified by series of measurements, proving the benefits of novel technology and its potential to impact power electronics applications around us. Deep description of current measurement technique with high bandwidth, control loop operation and its implementation in digital signal processor is included.

Abstrakt

Táto práca je zameraná na analýzu súčastného stavu GaN polovodičovej techniky vo výkonovej elektronike a jej aplikáciu v DC/DC meničoch, optimalizovaných na účinnosť a vysokú objemovú hustotu výkonu s cielom použitia v serveroch a telekomunikačných zariadeniach.

Teoretická časť analyzuje problémy a výzvy spojené s novou technológiou GaN, ako napríklad riadenie hradla pre rôzne vnútorné štruktúry dostupné na trhu, optimalizácia plošných spojov pre chladenie minimalizovaných púzdier pre povrchovú montáž s cielom minimalizovať parazitné prvky. V práci je zahrnutý presný výpočet strát pre aktívny usmerňovač realizovaný pomocou novej technológie GaN. Výsledky a nápady získané teoretickou analýzou rôznych problémov sú aplikované pri návrhu prototypu a overené sériou meraní, ktoré dokazujú výhody novej technológie a jej potenciál ovplyvniť aplikácie výkonovej elektroniky okolo nás. Zahrnutý je podrobný popis merania prúdu s veľkou šírkou pásma, fungovania regulačnej slučky a jej implementácie v digitálnom signálnom procesore.

Keywords

Gallium Nitride semiconductors, Cooling of minimized surface mount devices, Novel R_{DSon} Measurement method, Dynamic R_{DSon}, High Efficiency GaN half bridge, GaN Totem Pole converter

Kľúčové slová

GaN polovodiče, Chladenie minimalizovaných púzdier pre povrchovú montáž, Nová metóda merania dynamického R_{DSon}, Dynamický R_{DSon}, Vysoko účinný menič s GaN

Bibliographic citation

ŠÍR, Michal. *Comparison and Optimization of DC/DC Power Conversion Topologies Using GaN FET Technology for High Efficiency and Power Density Power Converters*. Brno, 2021. Available also at: https://www.vutbr.cz/studenti/zav-prace/detail/137332. Doctoral Thesis. Vysoké učení technické v Brně, Fakulta elektrotechniky a komunikačních technologií, Department of Power Electrical and Electronic Engineering. Supervisor Pavel Vorel.

Author ’s Declaration

I declare that I have written this doctoral thesis „Comparison and optimization of DC/DC power conversion topologies using GaN FET technology for high efficiency and power density power converters” independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the project and listed in the comprehensive bibliography at the end of the project.

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Prehlásenie

Prehlasujem, že svoju dizertačnú prácu na tému „Srovnání a optimalizace topologií pro DC/DC konverzi energie s použitím technologie GaN FET pro měniče s vysokou účinností a objemovou hustotou výkonu“ som vypracoval samostatne pod vedením vedúceho dizertačnej práce a s použitím odbornej literatúry a dalších informačných zdrojov, ktoré sú citovańe v práci a uvedené v zozname literatury na konci práce.

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Brno, August 22, 2021

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Acknowledgments

I would like to thank supervisor of doctoral thesis doc. Pavel Vorel for methodological, pedagogical and professional help and valuable advice in the elaboration of my dissertation.

Poďakovanie

Ďakujem vedúcemu dizertačnej práce doc. Pavlovi Vorlovi za účinnú metodickú, pedagogickú a odbornú pomoc a dalšie cenné rady pri vypracovaní mojej dizertačnej práce.

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INTRODUCTION

After years of evolution and domination on the power electronics market, the Silicon semiconductors are reaching their physical limit, which opens space for the new technologies. In the last few years, amount of available GaN switching devices for power electronic applications has significantly increased. The number of emerging devices with a different internal structure has a growing tendency. Devices are offered not only by small/startup companies but also by well-known manufacturers of semiconductors (Infineon, Panasonic). The higher bandgap of Gallium Nitride (3.4eV) material offers potentially higher operating temperatures, fast switching capability and therefore generates less power loss than widely used Silicon or SiC devices.

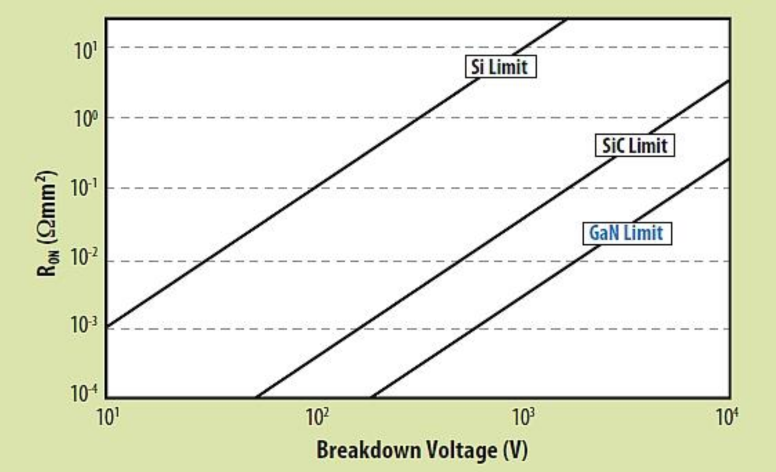


Fig. 1: Theoretical limits of Si, SiC and GaN material, [7]

GaN Transistors are well-known from low voltage, high frequency (MHz, GHz Range) applications (RF amplifiers in cell phones, *consumer* electronics, and many more). Improved manufacturing technology allows to use GaN in power electronics, which sets a brand-new benchmark in power converters´ parameters. Nowadays markets provide relatively narrow portfolio of GaN devices with 600V rating focused on power supply applications (consumer electronics, server and telecom applications…). First transistors with 1200V rating exist too, which makes them usable in electric drives and automotive applications. General requirements on power conversion systems are moving to smaller, higher dense solutions (60-100W/inch^3) to reduce the overall size of the system and overall cost of the power supply.

In following chapters the structure and parameters of currently available GaN transistor part numbers will be described. As the manufacturers are choosing different way how to proceed in the development of new devices in terms of internal semiconductor structure, closer look will be taken onto analysis of those structures with intention to compare.

MOSFET Gate driving principles are well known in power electronics. With new absolute maximum ratings for Gallium Nitride semiconductors, new challenges and possibilities are being introduced into design. This thesis aims to analyze and name these problems, with intention to propose solutions applicable to power converters design for various applications with GaN.

Roadmap in packages development is leading into size minimized packages, designed for surface mount technology. This style of packaging fixes problem with gate driving and improves switching performance of the device, on the other hand makes cooling design of the power chip challenging. Finite element method simulations together with measurement on prototypes of printed circuit boards designed for high performance cooling of small packages, which give a reference for industrial designs, are included.

Introduction of innovative devices, with brand new production technology and semiconductor structure should have different qualification process, comparing to settled Silicon MOSFETs used nowadays. The reason is simple, new phenomena might be present and might affect device performance in different operating conditions, which are not included in qualification process for semiconductors nowadays. This might affect long term reliability, which poses a high risk for pioneers introducing new technology into their commercial products. One of these phenomena is dynamic on-channel resistance, varying with time and various conditions. Analysis of this particular problem and collection of results measured on existing, commercially available samples, is one of base topics of this thesis.

Main result of this thesis is supposed to be the application of gained knowledge into prototype of DC/DC converter using Gallium Nitride devices, optimized for high efficiency and high-power density. This converter is operated as power factor correction in totem pole configuration with output power 3kW at output voltage 400V. Results show real benefits of this new technology, with immediate introduction into industrial application possible.

Study and analysis of certain topics related to GaN in this thesis, resulted in potential application of integrated circuit used primarily for this technology in different field. Penultimate chapter shows example of recuperative gate driver for silicon MOSFETs in synchronous rectifier for high efficiency resonant converter. This shows, that using novel/high-speed integrated circuit originally designed for GaN transistors, might bring significant improvements in various electronic problem categories.

1 PRESENT GAN TECHNOLOGY OVERVIEW

Nearly every manufacturer on the market is presenting his own GaN technology, with a different internal structure on a semiconductor level and with different performance. Internal structures of the transistors promoted for a usage in power electronics are - Cascode (Transphorm, VisIC), Enhanced mode (GaN systems, EPC) and Gate insulated transistors (Panasonic, Infineon). Different internal structures have different levels of complexity of the chip and different driving requirements. As per documentation of the aforementioned manufacturers, it is clear, that current common production technology is creating GaN structures on a silicon wafer. This technology is borrowed from manufacturers of optoelectronic components (LED, low wavelength lasers), where it has a long tradition and provides a good start point for GaN development. In this sector, two major companies (Veeco U.S., Aixtron Germany) are well known, providing automated solutions for manufacturing of GaN on Si structures.

1.1 D-mode GaN

The basic GaN HFET (Heterostructure Field Effect Transistors) functional structure is grown on the silicon substrate with thin layer of Aluminum Nitride (Fig. 2), in some sources this type of transistor is also called depletion or d-mode transistor. As in every power Field Effect Transistor, there are Gate, Source and Drain contacts. Due the Gate electrode placed on the top of the AlGaN, we need to apply negative voltage bias on Gate-Source to turn the device OFF. This is caused by Schottky contact on the top of the surface, which becomes reverse biased by negative voltage and the electrons underneath are depleted. This device is “normally ON”.

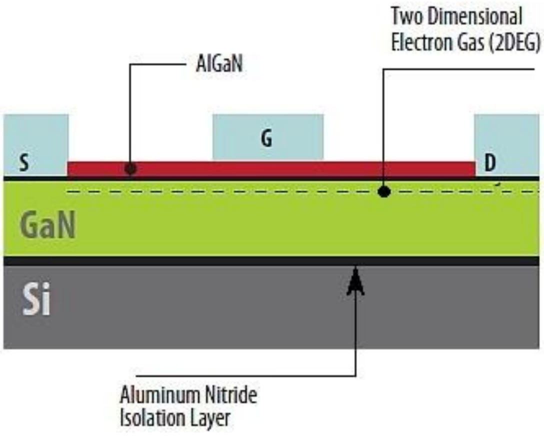


Fig. 2: Depletion mode GaN transistor structure, [7]

In power conversion applications this device obviously could not be used. The negative bias voltage on Gate-Source contact must be present before the power bus voltage. This may be hard to achieve in many applications and can result in driver circuit complexity, which affects the system reliability. To make GaN transistor useful in real application, manufacturers were forced to deal with the mentioned problem by developing new structures while maintaining the performance.

1.2 E-mode GaN

GaN Systems, EPC works with enhancement mode field effect transistor (FET) structure. Basic enhanced mode manufacturing process starts with silicon wafers with thin aluminum layer (AlN) growth on it. This thin layer allows the growth of gallium nitride heterostructures (AlGaN) and creation of the whole transistor structure. The result is the structure shown on picture below, which is similar to silicon metal oxide semiconductor FET (MOSFET) with some exceptions. To enhance this FET, positive voltage must be applied between Gate and Source contact, same as in standard power MOSFET transistor.

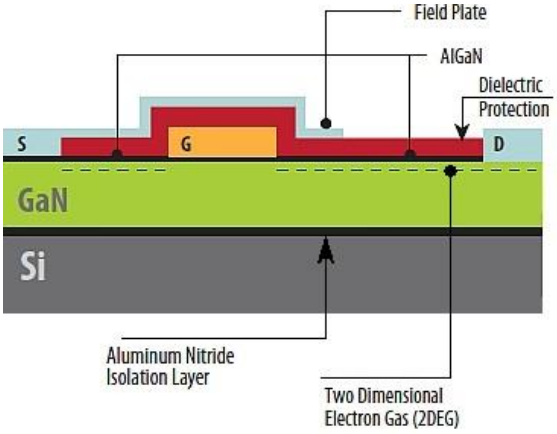


Fig. 3: Enhanced mode GaN transistor structure, [7]

With voltage present on the gate electrode, device can operate in two quadrants (forward and reverse current), with voltage drop equivalent to product of channel resistance in open state and drain-source current. Important difference between Si MOSFET and the GaN is the absence of natural body diode, which was causing serious problem with its reverse recovery charge in hard-switched topologies. In reverse mode (U_{GS}=0 V), the voltage drop is defined by the channel resistance in reverse mode plus voltage on fictive inner diode, the forward voltage of which is the same as the one of the gate threshold voltage (1.1-1.5 V) (the situation is properly described in Fig. 4). In case of reverse conduction with negative bias on Gate electrode (U_{GS}<0 V), this diode voltage is increased to the value of negative bias. This will result in significantly increased conduction losses in reverse operation mode. As it will be further described in Chapter 3, due to the low gate threshold voltage and the impossibility of operation in reverse mode, special requirements are needed for gate driver loop impedance.

Absence of diode reverse recovery charge known from silicon MOSFETs in thousands of nano-coulombs (nC), has only decreased on few dozens of nC, while this effect was caused by capacitive charge of semiconductor junction capacitance. This fact together with reduced Coss capacitance brings theoretical assumptions to operate at higher frequency with low switching losses also in hard-switched topologies.

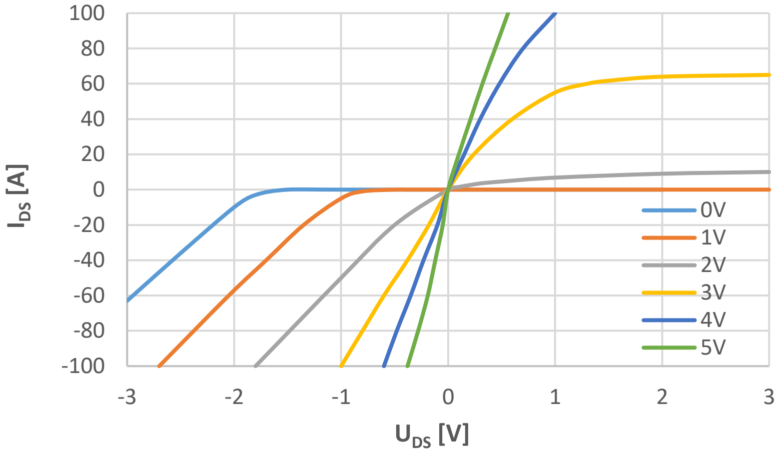


Fig. 4: Enhanced mode GaN output characteristics

1.3 GaN Cascode

Transphorm, ON Semi, VisIC are developing the cascode GaN transistors. Cascode is combination of low voltage fast silicon transistor (typically N-MOSFET) with “normally ON” GaN transistor (d-mode) connected as in picture below.

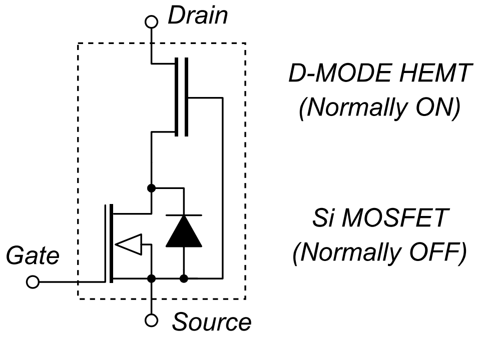


Fig. 5: GaN Cascode power transistor

Main benefit of the GaN cascode is the higher Gate-Source threshold voltage (3-4.5 V) – as the gate drive parameters are defined by silicon MOSFET in “bottom” part. GaN cascode can conduct reverse/forward current with voltage present on the Si MOSFET Gate electrode (Fig. 6, case a. and b.). Voltage drop is then defined by the forward current and the sum of the low voltage Si MOSFET and the depletion mode GaN channel ON resistance. In reverse operation mode with no voltage on Gate (U_{GS}=0V) the current is flowing through intrinsic body diode of silicon MOSFET and depletion mode GaN transistor – reverse voltage is then equal to reverse body diode voltage plus product of reverse resistance of d-mode transistor and flowing current (Fig. 6, case c.). There is no difference between reverse conduction with zero gate voltage, and negative bias on gate electrode (U_{GS}< 0V) – using negative Gate voltage during device driving is possible, but has no effect on an overall drain-source performance.

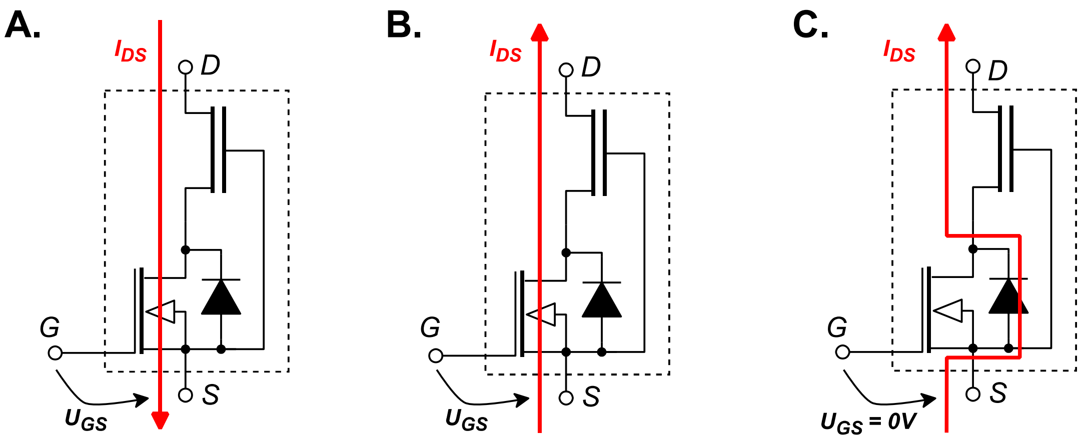


Fig. 6: GaN Cascode operating modes

Accurate control of drain voltage slope during turn-on and turn-off is not possible with Cascode structure. By changing Gate resistance, the control of du_{DS}/dt is only possible in limited extent. Output characteristic of GaN transistor is the conjunction of two independent output characteristic of low voltage Si MOSFET and d-mode GaN, and correlation between them. Example of the cascode output characteristic is on picture below, where sharp edge around Si MOSFET Gate threshold voltage can be seen.

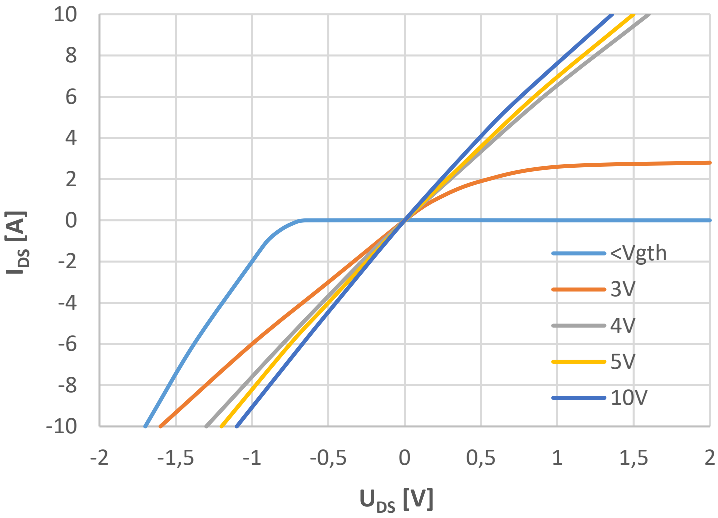


Fig. 7: GaN Cascode output characteristics

Israel manufacturer VisIC is promoting GaN cascode with the best parameters at the time in terms of on-state resistance (22 mΩ), outstanding peak forward (180A) and reverse current capability in 650V class of transistors. This manufacturer also provides first GaN 1200V 40mΩ cascode transistor. Disadvantage of cascode devices is a need of two chips in one device (d-mode GaN and Silicon MOSFET), which can influence reliability and have negative price impact.

1.4 Gate injection transistor

GIT transistor promoted by Panasonic, Infineon is normally off transistor based on high electron mobility principle, similar as d-mode using two-dimensional electron gas forming at an AlGaN-GaN layer. The transistor is being produced in the same way as the other structures on silicon substrate, with a buffer layer to allow reliable creation of GaN structures.

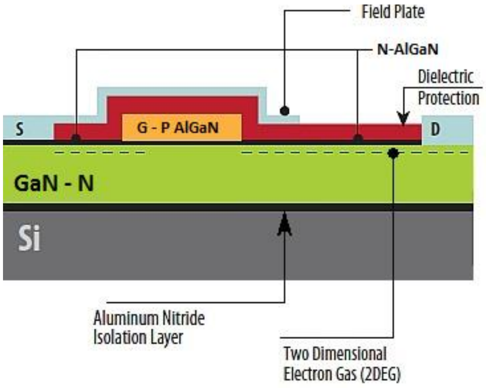


Fig. 8: Gate injection transistor structure, [7]

Same as e-mode transistor, GIT is forced to conducting state by increasing gate-source voltage above threshold voltage, typically around 1-1.3V. Major difference between e-mode and GIT is the on state behavior of Gate – while e-mode acts similarly to unipolar MOSFET transistor, GIT is above threshold voltage acting as a diode (P type Gate), therefore requires on state current (typically dozens of mA) which is defining the on state channel resistance of the Drain-Source. Thanks to the diode behavior in the on-state is gate electrode rugged (up to the current rating) against high dv/dt transients on drain-source. As transistor does not have a parasitic body diode, the current is flowing in reverse conduction mode through the channel – reverse drain-source voltage is dependent on gate-source voltage, minimum corresponding with the threshold voltage and increasing with a negative gate bias. The transistor therefore acts as a combination of bipolar transistor (in forward mode) and e-mode unipolar transistor (in reverse mode). As the reverse current is conducted over the channel, the reverse recovery charge minimized – key feature of GaN technology.

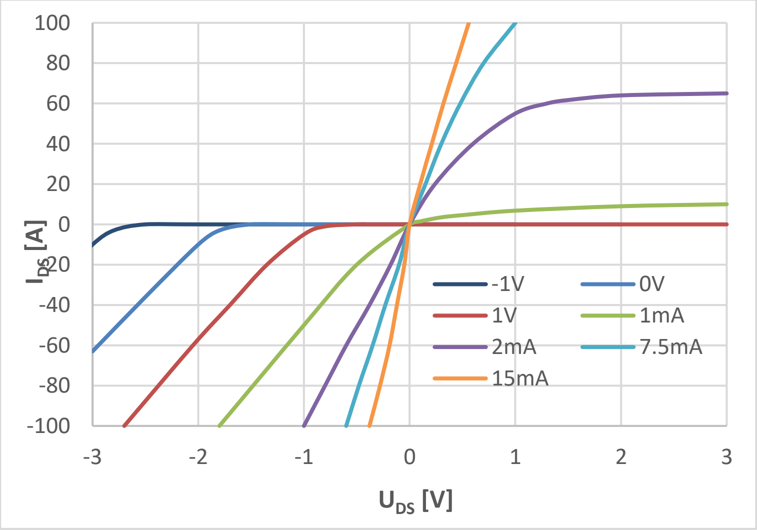


Fig. 9: GIT transistor output characteristics

1.5 Absence of avalanche mode

In general, high electron mobility GaN transistor does not have an avalanche mode, or in other words, nondestructive breakdown in overvoltage. Avalanche mode means ability to clamp voltage above certain drain-source voltage in non-conducting state, known from MOSFET devices. MOSFET breakdown of the channel is nondestructive up to certain time defined by robustness/thermal capacity of the chip and operating conditions (specified avalanche energy). The transistor typically enters this mode during switching in high current condition (FAULT) and not well designed, highly inductive layout. Up to some extent, this behavior might be considered as a self-protection of device in circuit.

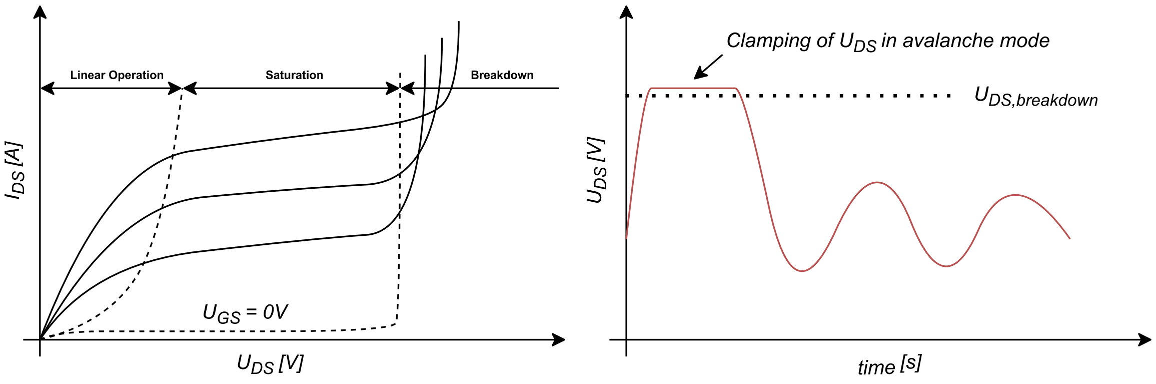


Fig. 10: Output characteristics and Avalanche mode of MOSFET

Applying the same conditions on GaN transistor will result in failure. Exceeding the voltage rating is in case of GaN wide bandgap devices (WBG) leading to immediate channel breakdown, although this voltage is from practical experiences much higher, than rated voltage. Manufacturers claim that devices are able to withstand transients 20-40% above specified rating. Therefore, for reliable operation it is not recommended to use any type of GaNs in topologies, which principally allows overvoltage in case of control circuit failure (e.g. single switch flyback). Non inductive layout with proper drain-source rating check in all operating conditions is mandatory, to avoid random failures during product lifetime.

Another aspect of the overvoltage effect on GaN is reduction of mean time to failure. This problem is well described in JEDEC JEP180 (Global Standards for the Microelectronics industry) where part of the qualification includes lifecycle testing with elevated drain-source voltage in combination with temperature.

2 THESIS GOALS

1.) **Study of Gate driver requirements analysis of nowadays available GaN semiconductors**
With rise of novel technology, several different structures of Gallium Nitride power chip exist. While some of the parts are manufacturers developing based on combination of two independent chips in one package, others are investing effort into advanced single chip solutions, with different layout and production technologies. Different principle of operation means different parameters and requirements for driving and its application in power converter, which is a target of the analysis.

2.) **Design and optimization of innovative cooling solutions for minimized surface mount packages, used for novel GaN devices**
Voltage driving levels and fast switching performance of the GaN high electron mobility transistor are a motion for packaging style change, as large lead packages are no longer suitable and are limiting the performance of a chip. Goal of this chapter is to develop innovative solutions for cooling of minimized surface mount packages without constraints related to increased inductance of input terminals.

3.) **Characterization of dynamic R_{dson} problem related to certain production technologies**
Based on published articles of different authors, electron trapping under Gate contact of high electron mobility transistor exists. As this misbehavior might significantly affect performance of switch in final application, further analysis and characterization of this problem is crucial. Special experimental test setup is being built, and test results will be compared.

4.) **Application of gained sub-results in practical case of innovative DC/DC power converter and its optimization for high efficiency while maintaining high power density**
Multiple of partial improvements gained within this thesis are being verified in totem pole power factor correction converter. Detailed steps of optimization for high efficiency at certain operating conditions are explained, to comply with 80plus certification required by the European Union regulations for computer and server appliances. Goal of this section is to present gained results with all the improvements applied.

5.) **Application of novel GaN integrated circuits in various applications**
Evolution in production of Gallium Nitride based semiconductors results in development of novel integrated circuit, capable of parameters never seen before. This chapter shows application of integrated driving circuit in special application of recuperative Gate driver of high Current synchronous rectifier in resonant converter, resulting in US patent.

3 STUDY OF GATE DRIVER CONSIDERATIONS FOR VARIOUS TECHNOLOGIES

Successful implementation of GaN transistors into power conversion topology requires reliable driver circuit, while fulfilling requirements of driven chip. As mentioned in previous chapter, gate structures of available transistors are different in terms of construction, therefore various requirements for the driver design exist.

3.1 Overcurrent protection by Driver

The saturation protection known from the IGBT driver technology is in theory possible with every transistor as with rising current across the conducting channel, at some point, voltage starts to rise too. To gain maximum reliability, it would be nice to construct driver of the device, which is able to protect the device in case of short circuit. Detectable voltage increase over the channel will appear for available GaN transistors only at high current, exceeding the peak rating of the device. In addition, during short circuit we can assume full voltage of the voltage bus across the device. Power loss is in this condition extreme, comparing to transistor parameters. To prevent the thermal failure, protection circuit must act in range of nano-seconds, which is nowadays not possible to achieve – when using circuit which consists from available integrated circuits placed on printed circuit board.

In terms of protection, innovative solution is presented by Texas Instruments LMG3410 device, where the driver of the power transistor is integrated together with overcurrent, overtemperature protection in single package. Manufacturer claims, that this protection is capable of acting in 20ns range and is able to protect device in case of low ohmic short at input. This part foresees a future of integrated driver on chip, and shows its impressive possibilities.

3.2 Voltage transient immunity requirements – CMTI

Fast transients from on to off state and vice versa are the key benefit of GaN semiconductors, leading to improved efficiency of power converter. In most of the power electronic topologies is the base stone half-bridge, where top side switch is “floating” and requires isolation against power ground. Assuming high dv/dt across this isolation barrier, any capacitance of the driver against ground is resulting in significant currents, being pushed over kelvin node of driven device, which might lead to false turn-on and oscillations. Low inter- winding capacitance of supply path for floating driver (transformer) is necessary.

As the GaN might be considered with designs operating at high frequency, deadtimes need to be optimized up to last nano-second, gate command signal is transferred typically by digital isolator with very low propagation delay (light or planar transformer principle). The path of the control signal isolation must be designed to withstand fast transient voltage – common mode transient immunity (CMTI) must be higher than expected dv/dt in designed application. High performance digital signal insulators are providing 100-150kV/µS (TI’s ISO78XX) and are already on the limit comparing to GaNs switching performance. Further development is necessary.

3.3 E-mode

High electron mobility, enhancement mode transistor can be in terms of control compared to a silicon unipolar transistor. Major difference to commonly used MOSFETs is lower Gate threshold voltage (typ. 1.3V, Miller Plateau 3.0V) and different behavior in reverse conduction. With intention to minimize switching losses, it is important to speed up the transitions from on to off state and vice versa. With high di/dt in drain source path the voltage on common driving inductance (gate-source loop) is easily reaching threshold voltage, which can lead into positive voltage present on Gate electrode.

Transistor is exposed to voltage transient du$_{DS}$/dt at conduction state change of opposite device in half bridge configuration. While the voltage is rising steeply, inductance in driving path act as a high impedance element. Gate is charged via miller capacitance and channel might become open. Voltage transients might be caused by external events, like input surge of power supply. In this state driver should keep gate electrode shorted to kelvin contact with low impedance during normal operation and even if it’s not powered, which is not true for many nowadays available integrated drivers. Mentioned parasitic elements are further explained in the picture below – transients might lead into cross conduction in half bridge topologies, which with high probability will result in permanent damage.

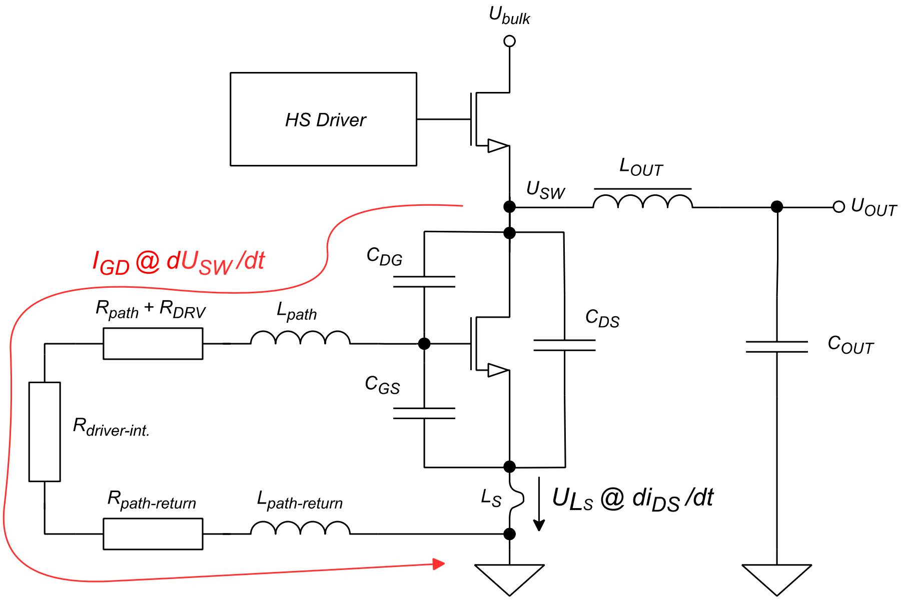


Fig. 11: E-mode Gate Driving circuit with parasitic elements

Gate charge (C$_{GD}$) is for WBG transistors significantly smaller; therefore, the driving is faster and efficient. Drain-Gate capacitance (C$_{DG}$) is present, and pushes current (I$_{GD}$) to gate during high dv/dt transients on drain. As the e-mode transistors have typically low absolute maximum voltage rating for a Gate electrode (max. 7V), long term reliability might be affected if spikes are present on Gate drive loop impedance. Stability of driving voltage over temperature and time is necessary, typically a precise linear regulator is used. Another major difference to the Silicon MOSFET drivers is undervoltage lockout, which is for most of the commercially available GaN drivers set to 4V. Usage of high current capable gate driver compatible with e-mode voltage driving levels is recommended (e.g. UCC27511 from Texas Instruments).

Common inductance in driving path is problem which does not allow to use lead packages for driving devices anymore and explains why properly designed GaN power chips are packaged into size optimized surface mount packages with kelvin node connection. While one problem is fixed by proper packaging, gate loop impedance is fully in hands of the designer. Design techniques for low inductive layout should be applied.

3.4 GIT

For best switching performance of a Gate Injection Transistor it is important to provide positive/negative current pulse (3-7 times higher than steady state gate current) during turn-on/off. From test experiences and manufacturers documentation, the higher the current peak is, the faster is the transition. Channel resistance in conducting state is defined by Gate current (20-50mA), disadvantage is additional power loss in the driver, as it is acting as linear regulator with small output voltage while transistor is conducting. Same as for e-mode transistors, the gate threshold voltage is small but requires certain power to activate as the input can be represented by diode (from Gate do Source) - ruggedness against false trigger is higher when compared to e-mode technology. To avoid device false turn on during voltage transient on drain-source it is recommended to keep gate voltage negative. As generation of positive and negative pulses together with precise steady state current limitation are relative complex for embedded solution, the manufacturers are providing integrated circuit fulfilling requirements of specific power chip (e.g. 1EDF5673 + IGO60R070D1). Integrated driver uses H-bridge configuration and external ceramic capacitors to generate positive and negative current pulse, set by series resistors (picture below). Negative bias for driver is not needed, as it is equipped with capacitive charge pump. From operation of the driver it is clear, that isolated power supply from power ground of the transistor must be used in any case, as the driver is reversing the bias voltage. This might be considered as complication with cost impact for budget sensitive applications. Transistor is sold together with the driver, no second sourcing is possible – solution is strongly dependent on designer relationship with the supplier.

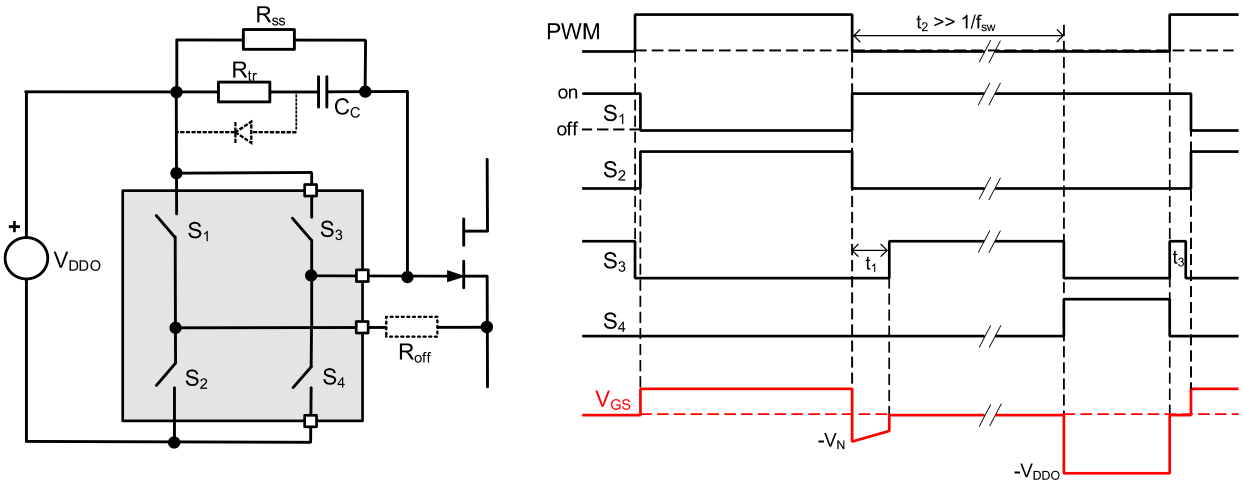


Fig. 12: Proper GIT driver with control diagram, [1EDF5673 Datasheet]

Negative Gate bias voltage can be present during whole off state of switching period, or can be present only temporarily (Fig. 12, time t_1), during switch on/off of opposite transistor in a half-bridge – time of the deadtime + maximum length of transition. “Negative bias time” is - according to datasheet of existing parts - programmed by external resistor, which is convenient. In terms of PCB layout, same recommendations are applied for GIT, as described for e-mode.

3.5 Cascode

GaN cascode power transistor - from driving requirements point of view - is basically the same as silicon MOSFET (typ. +/- 20V max. from Transphorm specification), as only low voltage normally off MOSFET is driven and controlling the d-mode GaN in internal structure. One of the major advantages is high peak voltage rating for Gate, which makes cascode most rugged GaN technology. Total gate charge is significantly smaller, comparing to silicon transistor with same drain source capability. From cascode internal structure it can be seen, that drain-source voltage dv/dt can be controlled over gate drive only in limited range, which is acceptable.

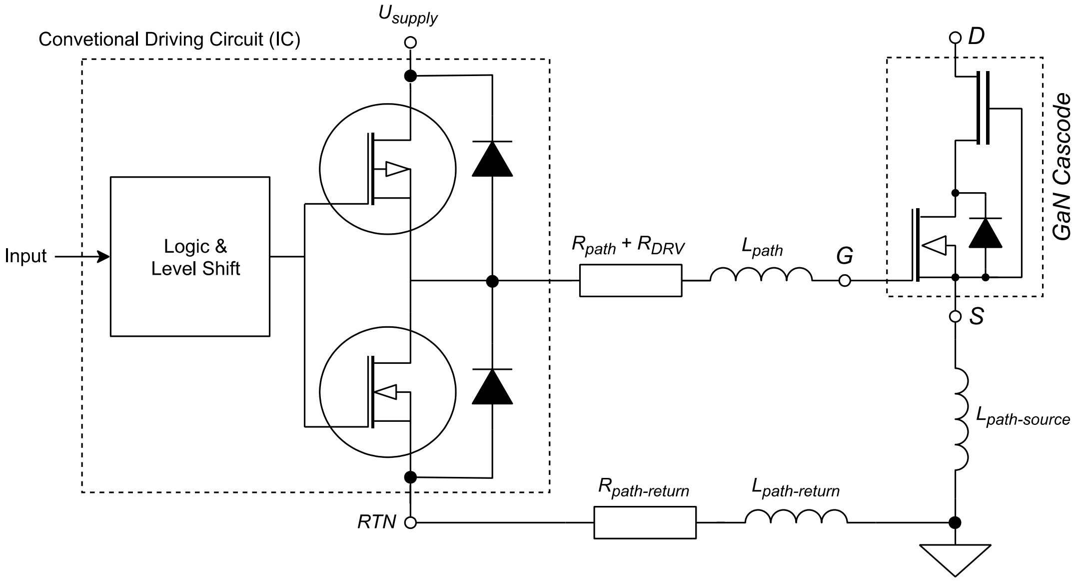


Fig. 13: Cascode Gate Driving circuit with parasitic elements

Thanks to the series combination of low voltage MOSFET and d-mode GaN, is the C_{OSS} higher and more nonlinear at low voltages, comparing to other GaN transistor structures, which has negative impact on switching performance and control complexity in resonant converters.

Same packaging style and driving levels allow the use of GaN cascode as a substitution in existing designs of power converters, which might improve efficiency parameters without significant redesigning effort.

4 COOLING OF MINIMIZED SURFACE MOUNT PACKAGES

Reducing parasitic elements is leading to size minimized, surface mount packages. On the one hand improved switching performance helps to reduce power loss of the device, on the other hand it makes cooling of the device much more challenging. Comparing to standard lead packages (TO-220, TO-247), which were in most of the cases directly attached to the heatsink over insulating thermal interface. With minimized surface mount packages it is necessary to design more sophisticated structure, in special case as a part of the printed circuit board itself. If we take a look at the current portfolio of GaN devices available on the market, we can split it into two groups - TOP and BOTTOM cooled surface mount packages. Several manufacturers are designing semiconductors packages in a mirrorable way, only shape of electrical connections is defining cooling requirements (for example Infineon's PDSO package). Both solutions provide pros and cons, which will be analyzed in this chapter.

4.1 Top side cooling

For a package where a cooling plate is located on the top side (opposite to soldering pads), the heatsink is a part of the PCB assembly, or the opposite way, the PCB is mounted to the heatsink. Problem seems too obvious and easy to resolve. But, for long term reliability in certain pollution degree (2-3) it must be taken into account, that for high voltage (typical bus voltage 400V DC) the creepage and clearance distance defined by IPC9595 are relatively high (>3mm), comparing to device size itself. This distance must be maintained between all electrical poles, mechanical fixings of the heatsink to the PCB tracks and connectors. To get stable results in production, tolerances of package dimensions same as soldering process itself need to be considered as well. Mechanical assembly to support heatsink mounted to the PCB requires at the end bigger area than needed by cooled component itself – benefit of the possibly high-power density disappears. In any cases, heat is transferred over the thermal conductive material directly to heatsink. If the heatsink is galvanically connected with a cooling pad, highly conducting material can be used as a gap filler. For this configuration the top side cooling is the most efficient way – nearly no temperature difference on Cooling Pad-Heatsink thermal resistance.

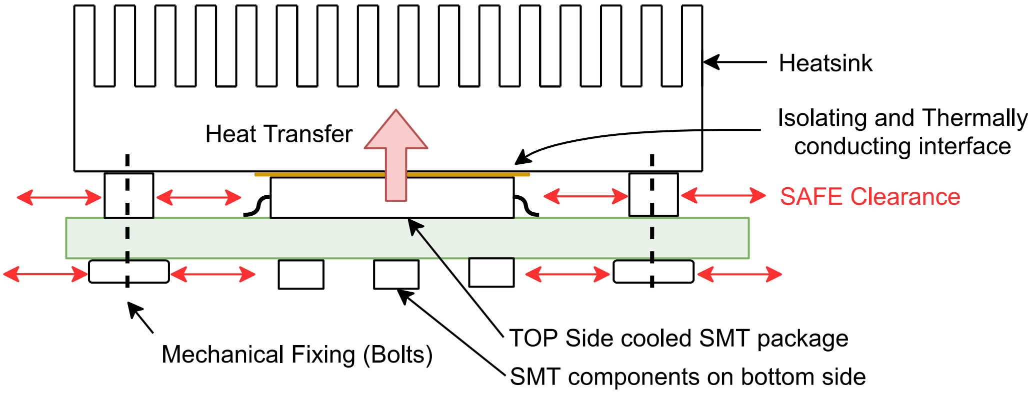


Fig. 14: Top side cooling mechanical construction

VisIC company producing GaN Cascodes is promoting very special hybrid package, most probably with military background, which has insulated cooling pad from other contacts of the device (part number V22TC65S1A). Manufacturer claims that part provides basic isolation up to 2.5kV which might bring significant benefits for Top cooling approach. Disadvantage is a package height (approx. 3mm), which is not compliant with IPC9592 recommended distances for advertised isolation voltage level.

4.2 Bottom side cooling

Second group of devices is manufactured with bottom side cooling pad, on the same side as electrical connection. Heat transfer is performed over PCB to the heatsink attached over thermal interface/foil on opposite side of the device. Mechanical interface is in this case not needed, PCB is assembled in simple single sided SMT assembly process and afterwards assembled over sticky/insulating interface to the heatsink. Bottom side solution is possible, in case the thermal resistance over the PCB thickness is minimized to acceptable value – power loss of the cooled device will create temperature rise, which together with temperature of the heatsink (ambient temperature) have to stay below maximum ratings of the chip.

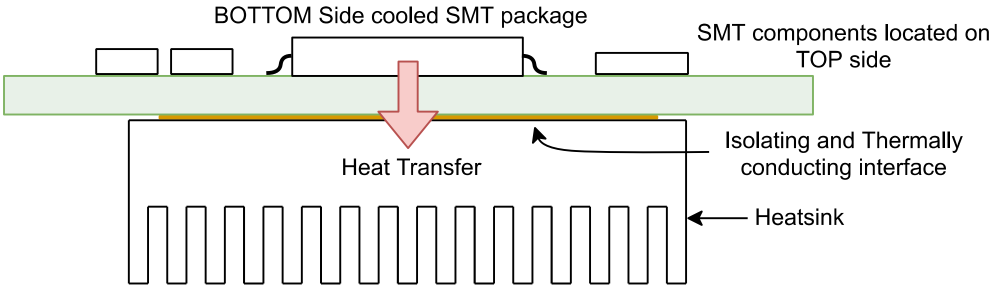


Fig. 15: Bottom side cooling mechanical construction

Heat transfer over PCB can be done over base/core material and over tracks and vias – copper part. In case of standard printed circuit board made from FR4 the core contribution to cooling is very low (0,35Wm^{-1}K^{-1}). On the opposite side is the ceramic material base - Aluminium Nitride ceramic (140Wm^{-1}K^{-1}), which has other disadvantages as brittleness, cost and only single layer PCB is supported by manufacturers. In case of low thermal conductivity of core material the right strategy is to bridge the PCB by conductive material and add additional insulating layer, which can provide fixing of the PCB to the heatsink at the same time (e.g. Sticky foil Arlon Secure 1500KT2). Thermal conductivity for a thermally conductive and electrically insulating foil (functional insulation, at least 30kV/mm) is in high performance material reaching 3Wm^{-1}K^{-1}, which is hardly comparable with non-insulating phase changing materials or thermal conductive pastes. Contribution of layers and vias to the cooling is mainly in Z direction, but can be extended to heat distribution in planar (X, Y) direction too, which increases area of heat transfer over insulating interface with lower thermal conductivity. In high frequency switching applications one has to keep the capacitance of cooling pad to the ground in mind (typ. Heatsink), as it is affecting device performance and adding switching losses, described in Chapter 3. Therefore, increase of cooling pad area is possible only in limited extent.

All of these assumptions can be considered as a start point for a successful cooling design and are based on well-known formula:

$$R_{\vartheta} = \frac{1}{\lambda} \cdot \frac{l}{S} \tag{1}$$

In following lines, several bottom side cooling solutions will be presented, using different printed circuit board manufacturing techniques with their performance evaluation.

4.3 PCB with copper inlays

Using standard core material FR4 should be the target for all designs, as the technology of PCB manufacturing on fiberglass is well developed and cost effective. Therefore, we are looking for a way how to create area of higher thermal conductivity from top side of the PCB to the bottom, to the isolating thermal interface/heatsink. These requirements are well fulfilled by Copper inlay technology - which is a copper element protruded over pre-milled opening in standard, several layer PCB. This design style is ideal for carrying high currents over PCB, seen in automotive applications nowadays, but ideally fits for this case, as the copper is a good heat conductor (400Wm^{-1}K^{-1}).

Before proceeding to prototype phase and testing, solution is to be verified by Finite Element Method simulation in ANSYS ICEPAK. In simulated case the cooled surface mount device is directly soldered to the copper inlay and the heat is transferred through the foil (Arlon Secure 1500KT2) to the heatsink over copper block. Simulated model contains layers of FR4 and bottom copper pour, with intention to spread heat in X/Y direction – increase area of heat transfer over isolating interface. Simulation result is displayed in picture below, FR4 layers are turned off for better visibility (Fig. 31). Power losses assigned to the four devices are 20W, assuming two transistors in parallel in a half bridge application (5W for every transistor chip). Ambient temperature is 25 °C, overall temperature increase is 23 °C – including isolation between heatsink and device thermal resistance between chip and case.

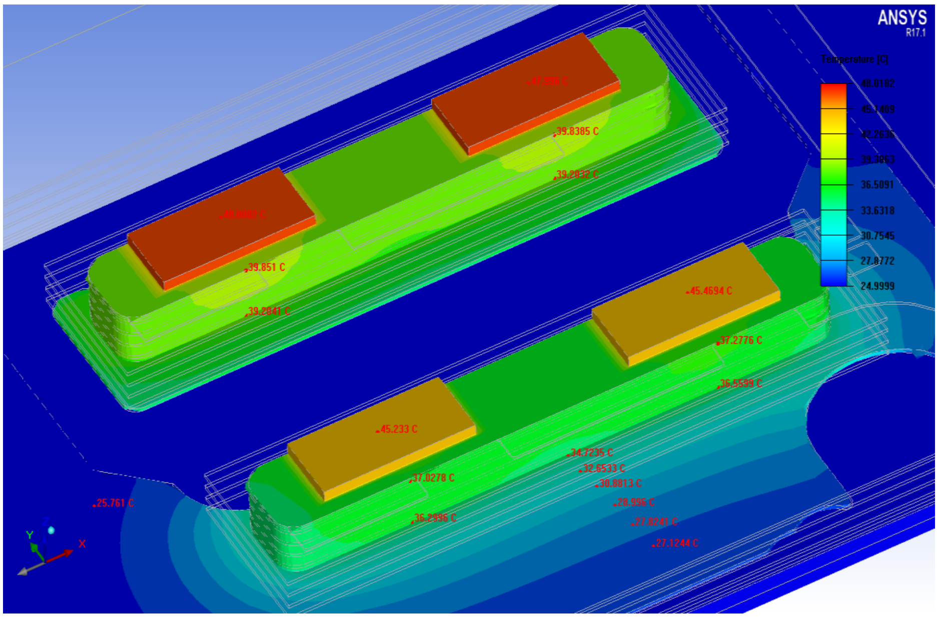


Fig. 16: Copper inlay thermal simulation

Improving of heat flow over insulating interface is possible by increasing copper on bottom layer, which is in contact with insulating foil. As the copper is good thermally conductive material, the heat will “travel” more far away from copper inlay, therefore lower temperature increase is expected. Situation can be analyzed by formula for thermal resistance, modified for situation of two electrodes on thermally isolated metal plate with concentrated power loss:

$$R_{\vartheta A-B} = \frac{1}{2.\pi.\lambda_{Cu}.d}.ln\frac{r_B}{r_A} \tag{2}$$

Where λ_{Cu} is thermal resistivity of copper and r_a and r_b are radius of two virtual electrodes in certain distance from centralized power loss. As the surface is not fully isolated, but surrounded by thermal conductive material, exponential drop of temperature with rising distance from edge of the copper inlay is expected:

$$\Delta T(r) = T_M.e^{-\frac{r}{r_0}} \tag{3}$$

Where r is certain distance from copper inlay, T_M is temperature increase at the edge of copper inlay vs. ambient and constant r_0 is defined as:

$$r_0 = \sqrt{\frac{\lambda_{Cu}.d}{\alpha}} \tag{4}$$

And means a distance, where the temperature drops to 1/e of its original value. In formula the thickness of copper is - d (approx. 70µm) and α is a heat transfer coefficient, depended on surrounding materials. As the copper is in this case surrounded by FR4 from one side and high voltage insulating foil from the other side, estimation of this coefficient is complex. From FEM simulation results it (Fig. 16) is assumed, that distance r_0 where temperature drops to half of original value is approximately 3mm. Therefore, it does not make sense to enlarge bottom copper pour over this value, as there is a negative effect of increased capacitance of switching node to the heatsink, described in details in Chapter 2.

Overall $\Delta\vartheta$ from surface of printed circuit board to the heatsink temperature is 12.3°C – thermal resistance is calculated with power 10W is $R_\vartheta = 1.23\ KW^{-1}$. Majority of the temperature increase is on the thermal insulating foil, while PCB is bridged with temperature difference 5.4°C ($R_{\vartheta PCB} = 0.54\ KW^{-1}$). This result shows major disadvantage - high tech PCB technology used, but overall performance is lost on high voltage insulating layer. Simulated case and tested prototype are representing primary power stage of 3kW resonant converter (LLC). Prototype using copper inlay technology was produced, and results were evaluated (Fig. 23). Power losses assigned to the four devices are 20W (5W for every transistor chip) – same situation as ICEPAK simulation on previous page. Heatsink temperature is 30.8°C, PCB surface temperature is 39.3 °C, resulting in thermal resistance from PCB surface to the heatsink side $R_{\vartheta PCB} = 0.85\ KW^{-1}$ (without insulating foil).

Measured increase is worse on prototype comparing to simulation, which might be explained by measurement error (different emissivity of materials) together with temperature increase on thermal conducting paste, which was used to attach bear PCB to the heatsink. Experiment was conducted without foil, as pressure during application of insulating foil is hard to control, variances of Arlon material properties and PCB by itself are present. Some of the produced prototypes were randomly showing significantly higher thermal resistance, which was caused by air bubbles, trapped in foil during application. Root cause of this problem seems to be copper inlay production tolerance (flatness of area), as the PCB production process contains materials with different height – copper shape and FR4 thickness defined by pressure during lamination of layers. This phenomenon can lead to problems in mass production, and potential unit failure by insufficient cooling of power semiconductor.

4.4 PCB with thermal vias

Alternate solution to copper inlays is the PCB with high amount of vias, with an intention to transfer heat efficiently to the heatsink. Design and effectivity of this solutions are hardly dependent on printed circuit board manufacturer capabilities – especially maximum hole/via plating thickness (Fig. 17 - c), distance between drilled holes (Fig. 17 - k) and the hole diameter itself (Fig. 17 - D). Considering dimensions displayed in the drawing below (Fig. 17) - for lowest thermal resistance of the PCB in Z direction, highest area of copper should be achieved (1). Triangular organization of vias is using manufacturing capabilities in the most effective way. Comparing to frequently seen square pattern [18][26], brings triangular pattern 15.5% more copper vs. area ratio, which is directly reflected in performance. By comparing area of the “useful” copper transferring heat to the total PCB area, following formula can be constructed (5). Derivation (=0) of this equation shows the optimum for a defined via plating thickness and drilled hole distance, which is feasible by standard manufacturing process – point A and B displayed in Fig. 19 and Fig. 18. As centralized power losses are expected (transistor assembled on PCB), thickness of top layer is not negligible, as it is distributing heat in X/Y axis and making vias on a side effectively contributing to heat transfer.

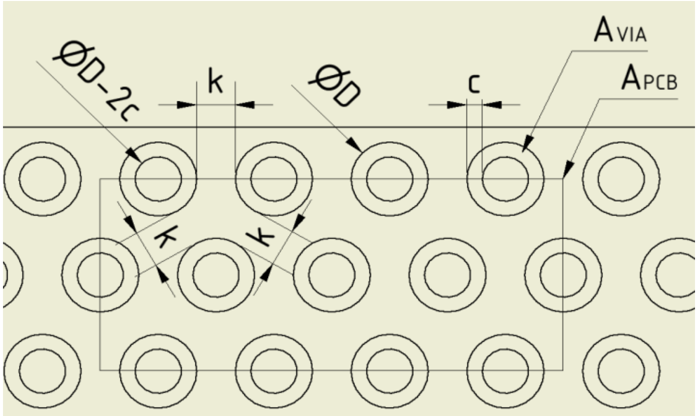


Fig. 17: Copper fill factor

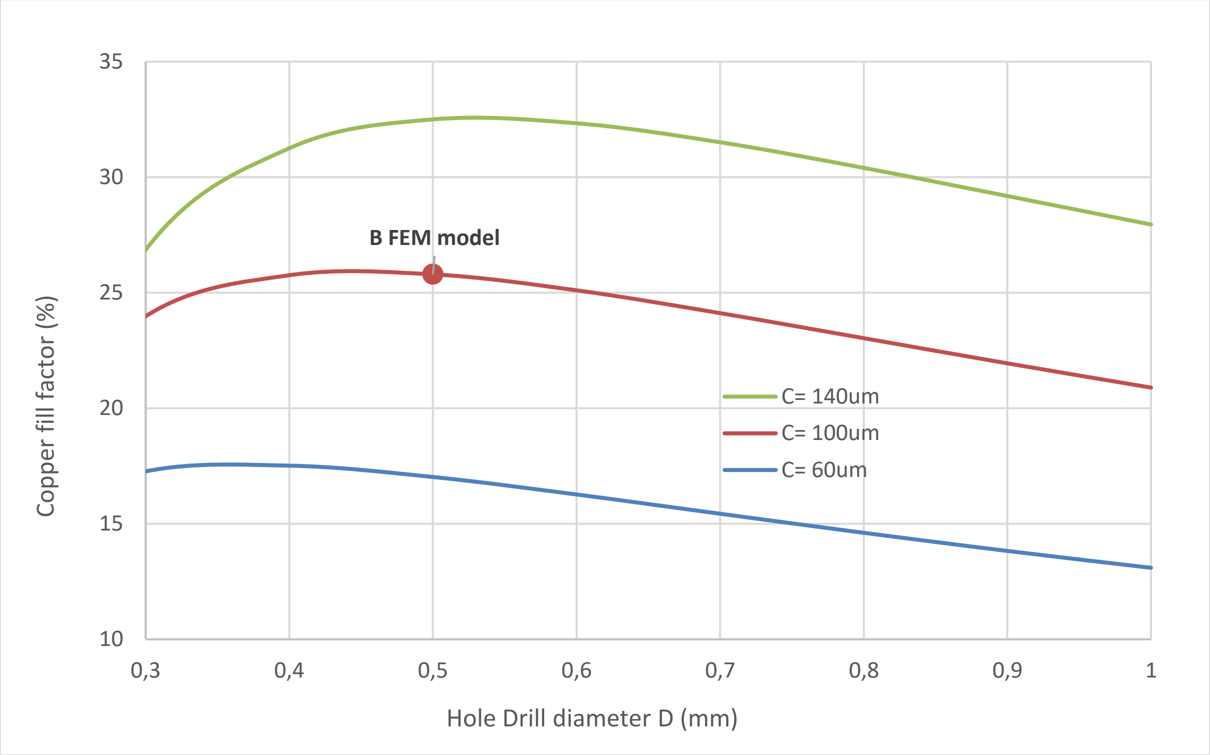


Fig. 18: Plot of copper fill factor for three different via wall plating thicknesses, k = 0.25mm

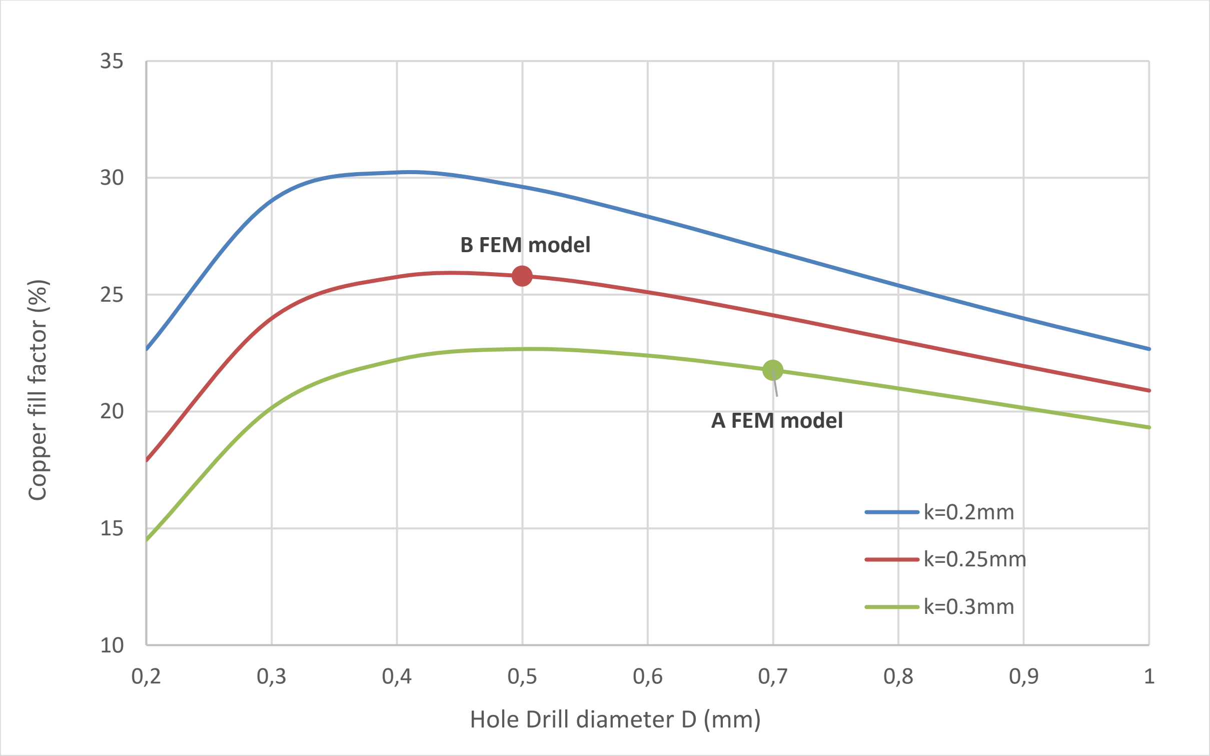


Fig. 19: Plot of copper fill factor for three different drill hole distances, c = 100µm

Ratio between the area of thermal conducting copper versus total PCB area:

$$\frac{A_{Cu}}{A_{PCB}} = \frac{8\ x\ A_{VIA}}{A_{PCB}} = \frac{2.\pi.(D.c - c^2)}{\sqrt{3}.(D + k)^2} \tag{5}$$

If the thickness of the top layer is sufficient (>50µm) and parameter k is in optimal range, the thermal resistance of across PCB can be calculated using following formula:

$$R_{\vartheta} = \frac{1}{\lambda_{Cu}} \cdot \frac{l_Z}{N.\pi.(D.c - c^2)} \tag{6}$$

Where N is the total amount of vias in cooled area, l_z is the overall PCB thickness – the vias length.

Same as for copper inlays, development started with thermal simulation of solution in ICEPAK. Simulation of model requires significant amount of mesh elements and computation power. Certain simplification had to be taken to make simulation possible – vias as a “barrel shape” were replaced by simple hexagons. Conductivity of material for simplified vias was recalculated over area of new hexagon and parameters of “real via” and its smaller than conduction of electroplated copper. Extra care was taken to make sure, that the mesh settings are set optimally and that the mesh follows the surface of objects (Fig. 20). “Mesh leak” - Overlapping of mesh assigned to object with low thermal conductivity (e.g. insulation foil) with copper element might lead to incorrect results.

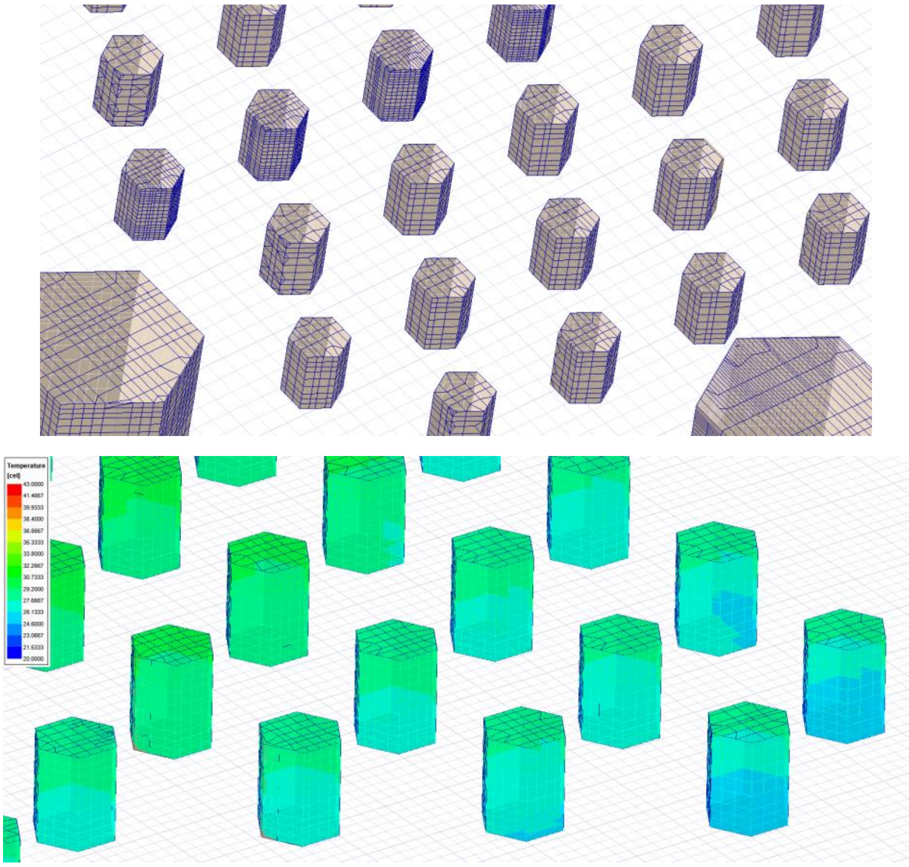


Fig. 20: High resolution mesh of simulated thermal vias

For simplification of the model special software was used, as manual replacement of vias by hexagonal shape can take a while. Raw data for simulation have been exported in ODB format, and brought to 3D by Artwork NETEX and 3DVu, which makes the job easy. After these operations it is necessary to clean model from small objects and objects which are not necessary for simulation.

To find the optimum before releasing the PCB for production, two variants were simulated. Version A and B for different parameters k, D showed on picture below. With same conditions (5 W per chip, 25°C ambient) as in case of copper inlay simulation, is the temperature increase higher, but comparable. Variant B shows smaller temperature increase, which is expected as the copper fill factor is higher and PCB thickness is reduced. In both simulations the temperature increase on thermal conductive material between heatsink and PCB is significant comparing to drop on a PCB itself, further optimization is losing effect.

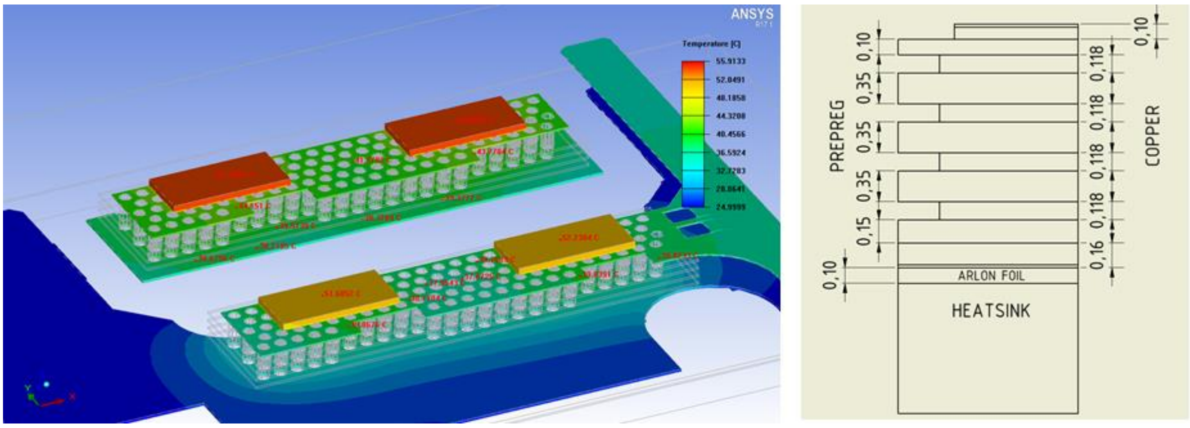


Fig. 21: Thermal Simulation of PCB variant A, k=0.3mm, D= 0.7mm, c= 100µm, PCB thickness= 2mm

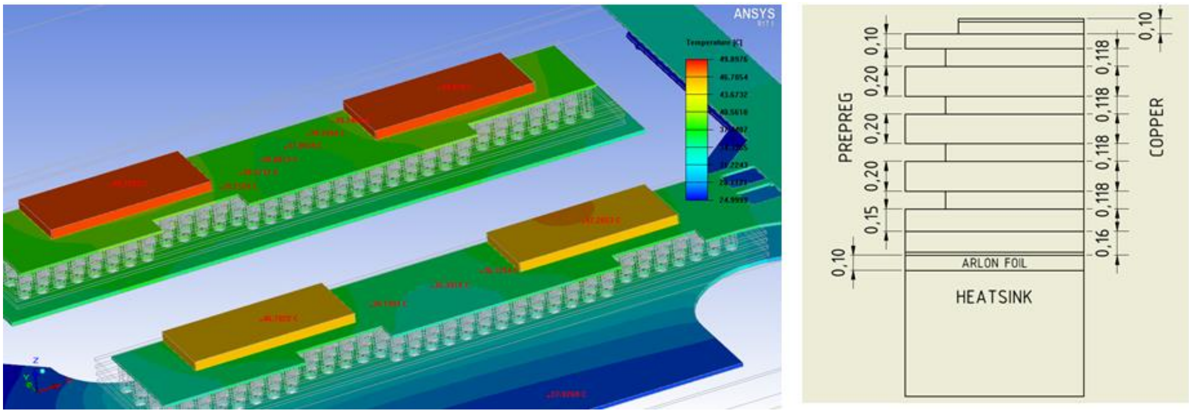


Fig. 22: Thermal Simulation of PCB variant B, k=0.25mm, D=0.5mm, c=100µm, PCB thickness= 1.5mm

For model B which shows better results and is preferred by the PCB manufacturers, heatsink temperature is 25.0°C and PCB surface temperature is 39.9 °C, resulting in thermal resistance from PCB surface to the heatsink side $R_{\vartheta FR4\text{-}VIASB} = 1.49\ KW^{-1}$. Temperature resistance on the PCB itself is based on cursors under chip and on opposite side is $R_{\vartheta PCB} = 0.87\ KW^{-1}$. Further improvement of thermal vias might be achieved by filling of the vias by thermal conductive material, but this a non-standard process which is not offered by many PCB production houses.

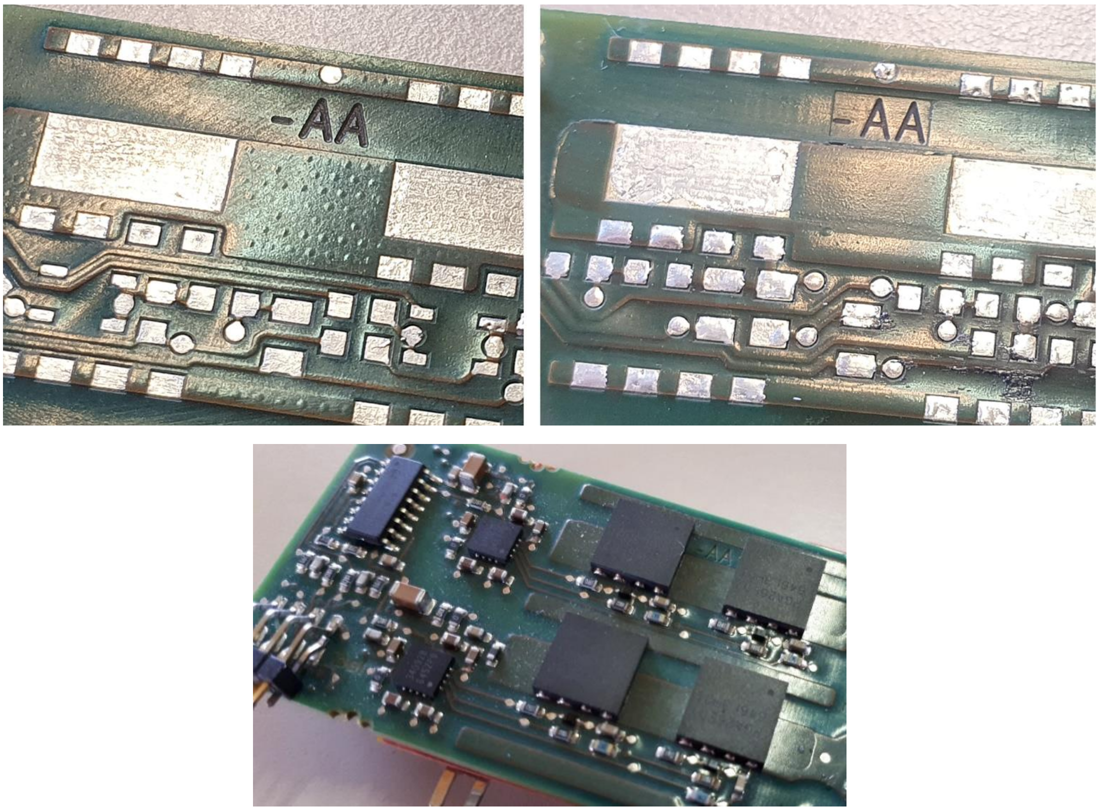


Fig. 23: Pictures of prototypes – printed circuit board with thermal vias technology (left), PCB with copper inlay (right) and assembled prototype

Pictures of prototypes evaluating technology of the PCB with copper inlay and with thermal vias, on practical example of half bridge power stage are displayed above. Thermal camera photos of both solutions showing devices under operation, with the same cooling conditions and same power loss as assigned in thermal simulation 20W, are below. As it was foreseen by thermal simulations result, thermal vias are cheap substitution for copper inlay technology in this particular setup, as most of the thermal resistance is in the high voltage insulating thermal conductive foil. For low voltage converters which do not require high voltage barrier or secondary side related circuits, copper inlays are the right choice, especially in case of high power losses.

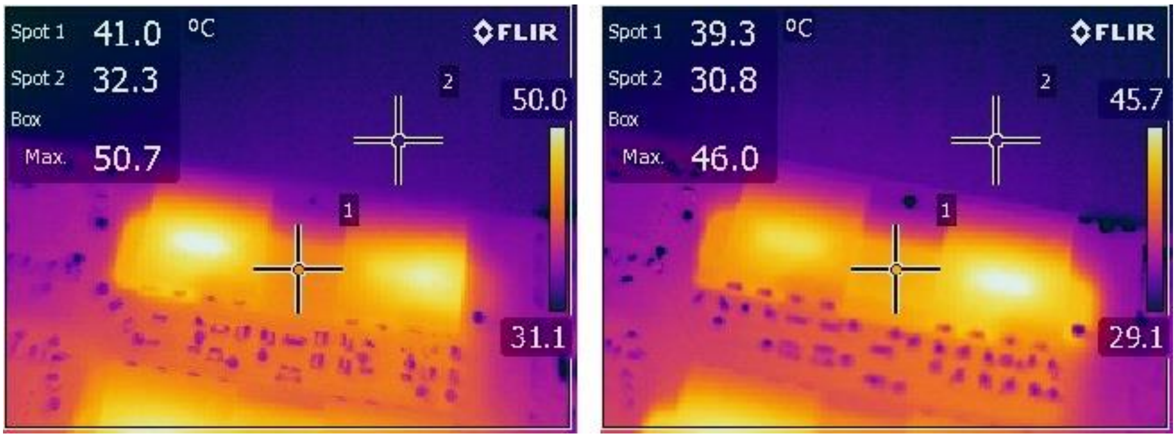


Fig. 24: Thermal camera picture of FR4 based PCB – copper inlay (right), optimized thermal vias (left). Power loss 5W/device, spot no.2 represents the heatsink temperature

4.5 Idea of PCB on Insulated Metal Substrate for power electronics

For further performance improvement, temperature increase over electrically insulating interface between PCB and the heatsink needs to be reduced – by technology of printed circuit board on insulated metal substrate (IMS). Insulated metal substrate printed circuit board is produced the same way as board with FR4, by process of vacuum lamination, high voltage insulation is integrated “inside” the PCB and done by insulating layers. This technology is well adopted in automotive lighting application for the same purpose – cooling of surface mount devices. This technology can be found in modern LED car lights, typically with single layer stack up and aluminum substrate. For use of the IMS board in power electronics it is necessary to use material between layers and substrate with proper voltage insulation, dielectric parameters and to keep distances of components/traces from edges to meet sufficient creepage/clearance according to IPC9592.

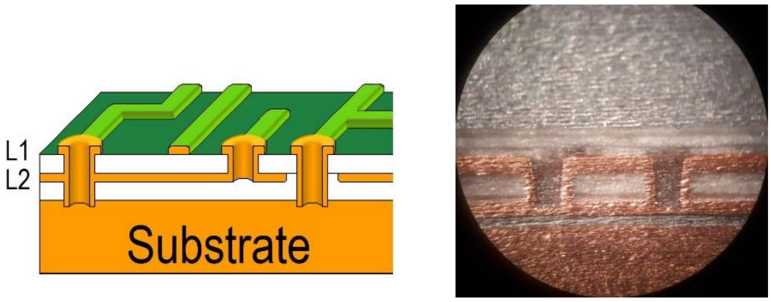


Fig. 25: Cross section of dual layer IMS board, suitable for power electronics application

From cooling point of view it is optimal to place driver and power semiconductor in surface mount package on a single layer IMS board. In such a case the heat travels only through one layer of high voltage insulating material, which can be thanks to novel ceramic-filled epoxy materials and production processes very thin, considering 400V operational voltage (typ. from 70-150µm). One of the suitable materials is named 92ML (ceramic-filled epoxy) and can provide thermal conductivity 1.6 WmK^{-1} in Z direction, which is ten times more than FR4.

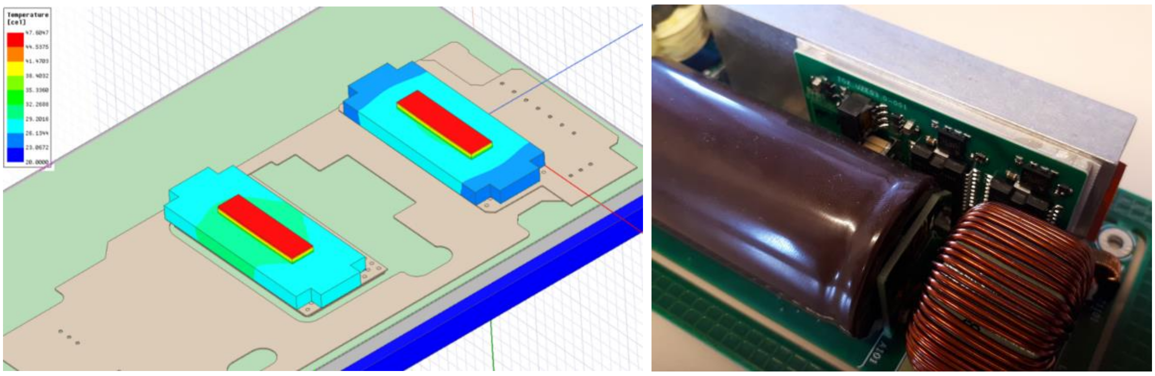


Fig. 26: Thermal simulation of Insulated Metal Substrate PCB

Routing proper low inductive layout for GaN gate driver and for power path is without doubts not possible on a single layer. Therefore, at least two-layer board should be used to achieve switching performance with minimized parasitic elements in the circuit.

This solution has significant disadvantage, as the heat needs to travel through two layers, while layers in between need to provide high voltage insulation, the initial benefit of IMS is lost.

By using thermal vias described in previous chapter is possible to "gain back" part of the performance of single layer solution, by bridging the intermediate insulating layer (Fig. 7.). Same equations as in previous chapter can be applied, therefore higher copper fill factor of vias pattern should lead to a better thermal performance.

Experiment started with relatively big Infineon package named PDSO with cooling pad area comparable to lead package TO-247. Power losses assigned in the simulation (Fig. 26) are set to 14W per chip (28W total) – overall temperature increase is 27°C, mainly on chip-package resistance. Increase from top layer of PCB to metal substrate is only 7°C (for a 14W), resulting in $R_{\vartheta PCB}$ = 0.5 KW^{-1}. FEM simulation indicates great performance, as the thermal resistance is from surface of the PCB to heatsink, including high voltage isolation, which is significantly better comparing to previous solutions. IMS board might be attached to the heatsink over non insulating thermal interface, paste, or highly conductive phase changing material. The model was using the same vias matrix as for solution B from previous chapter. Results are displayed in Fig. 26.

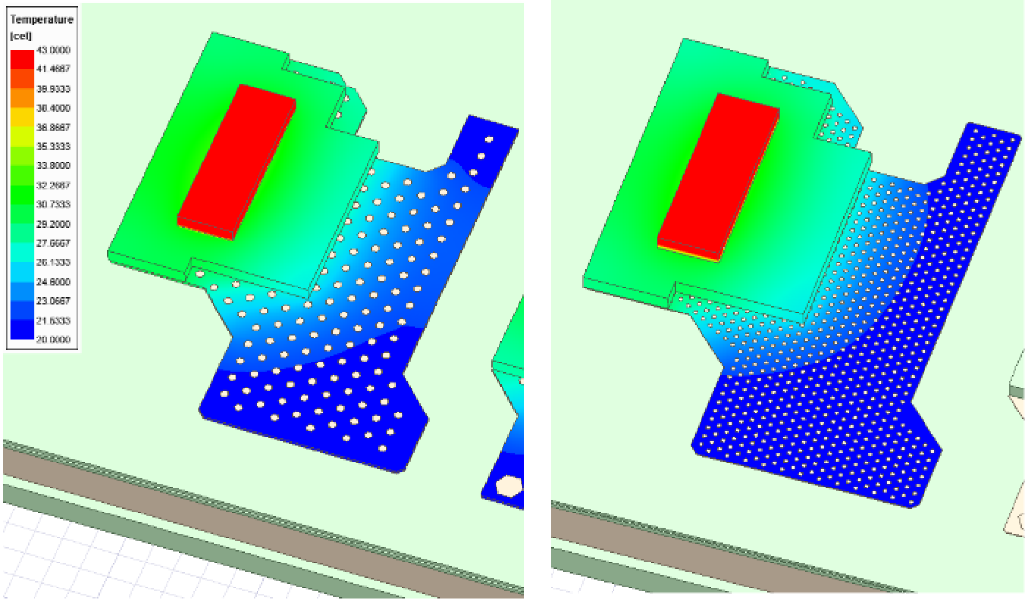


Fig. 27: Thermal simulation of Insulated Metal Substrate PCB

First prototype of IMS PCB (Fig. 26) had proved great capabilities in terms of cooling, but major disappointment comes with PDSO package. The manufacturer is using the same chip for multiple package case styles (TO leadless, QFN) which are much smaller – the chip must be small to simply fit in. For PDSO used in first prototype are gate and kelvin pads placed on the side of package and chip is located in the middle. Around 5mm long bonding wires are used for driving path, which resulted in problems while trying to achieve fast switching. As the transistor technology is GIT, current pulses necessary for turn on and off were reduced, switching speed drops (400V-45ns) and switching losses were increased – target efficiency was not achieved. This example shows how important it is to keep inductance of driving path low.

As the IMS cooling capabilities were proven, next design steps follow smaller SMT packages, from the same manufacturer.

Thermal simulations for Infineon TOLL package show slightly higher thermal resistance $R_{\vartheta PCB} = 0.91\ KW^{-1}$, mainly thanks to smaller area of cooling pad of the device itself. Based on results of FEM simulation two optimized variants of thermal vias pattern, manufactured with different production processes were selected:

Variant A – drilled vias with diameter D = 0.5mm with industrial standard plating c = 40um, distance between holes k = 0.25mm. Thickness of layers 150µm/150 µm (fill factor k_{vias} = 11.87%)

Variant B – high dense laser drilled D = 0.15mm copper filled micro-vias, distance between holes k = 0.2mm (k_{vias} = 16.66%). As the laser drill technology was used, the middle layer thickness needs to be reduced to avoid any defects in micro-vias plating. Therefore, the layer thickness is 100µm/150µm.

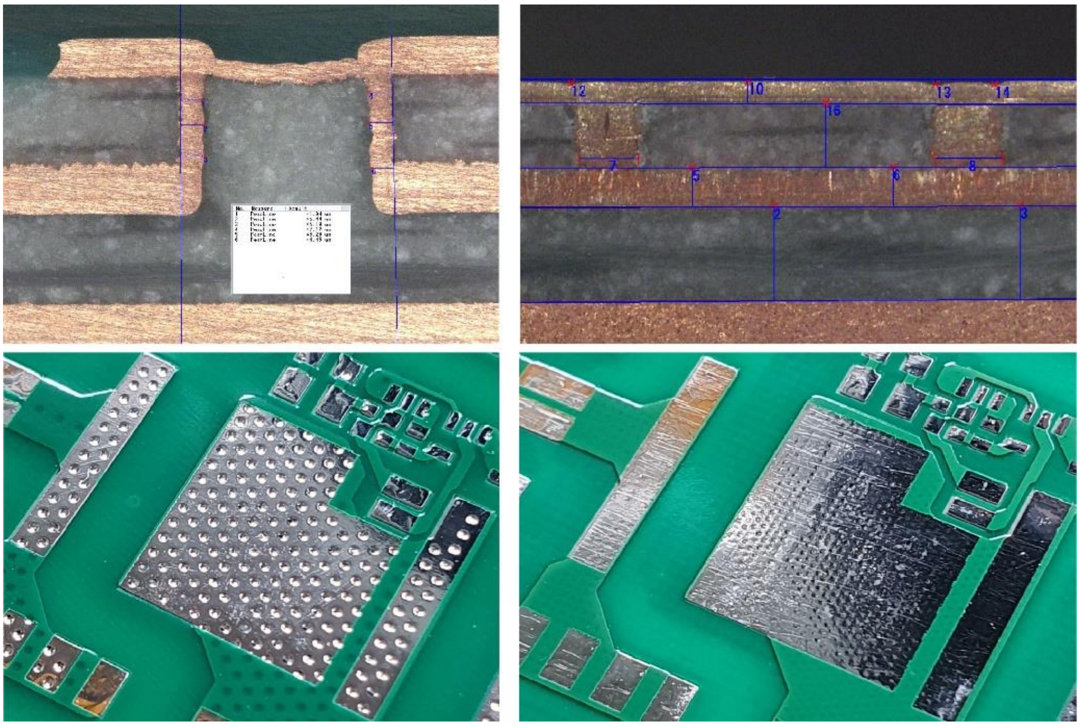


Fig. 28: Micro-section analysis and surface photos of tested prototypes - variant A (left), variant B (right)

Thermal camera pictures of variant A and B are shown in Fig. 29. MOSFETs are carrying current in reverse conduction mode – current and voltage drop on device is measured by calibrated multimeters - power loss is precisely set to 10W for both devices. Note that power assigned is the same as for thermal simulation created again in Ansys ICEPAK 2020 R1, with results visible in Fig. 27.

From thermal camera snapshot, chip size inside the package is nicely visible, same as the distribution of heat in X/Y direction caused by massive, 1.5mm thick, copper substrate.

With small difference caused mainly by production tolerances of prototypes, results are matching the simulation. Differences between tested variants A and B are not significant, as the vias are affecting the heat transfer only over part of the total thickness. As expected, higher copper fill factor shows lower thermal resistance. Disadvantage of laser drilled microvias is the reduction of first insulating layer to 100µm, which is on the edge of material performance in terms of isolation, therefore classic drilled vias technology is preferred from the reliability point of view.

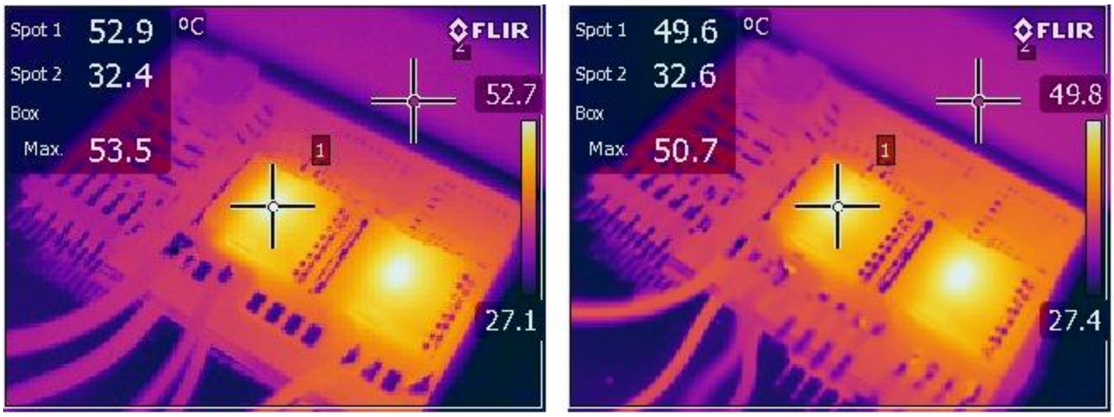


Fig. 29: Thermal camera picture of IMS PCB - variant A (left), variant B (right). Spot no.2 represents the heatsink temperature.

As the vias are making production process slightly complicated for PCB manufacturers, extra FEM simulation was performed to evaluate difference without any thermal via and two-layer IMS configuration. Difference with and without vias is significant – nearly 50% of performance. Impact of thermal vias on performance of the cooling solution is visible.

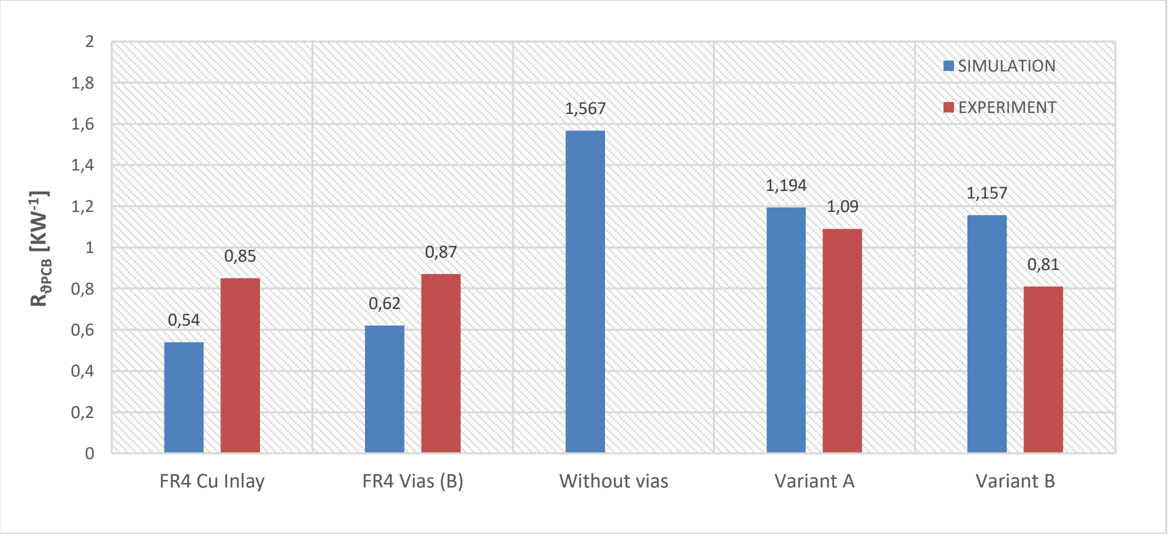


Fig. 30: Summary of the temperature rise on the PCB (w/o insulating foil) for all simulated and tested solutions

4.6 Summary

Several configurations of printed circuit board for cooling of minimized surface mount packages in power electronics application were presented. Result of the development is presented by thermal simulation results and measurement on physical prototypes with various constructions.

The best results in terms of thermal resistance from PCB surface to the heatsink can be achieved by using insulated copper metal substrate technology. In addition, performance might be improved by using optimized thermal vias matrix down to outstanding 0,81KW^{-1}. Presented examples contain insulated GaN gate driver, routed on two layers without any design constraints. Solutions based on multilayer FR4 PCB are suitable mainly for applications, where cost saving is the main decision factor. Achieved thermal resistance over PCB (Fig. 30) itself is comparable to IMS and sufficient for applications, where high voltage insulation is not required. By adding additional thermal insulating interface the overall performance of FR4 variants is significantly reduced and limiting the performance of the device.

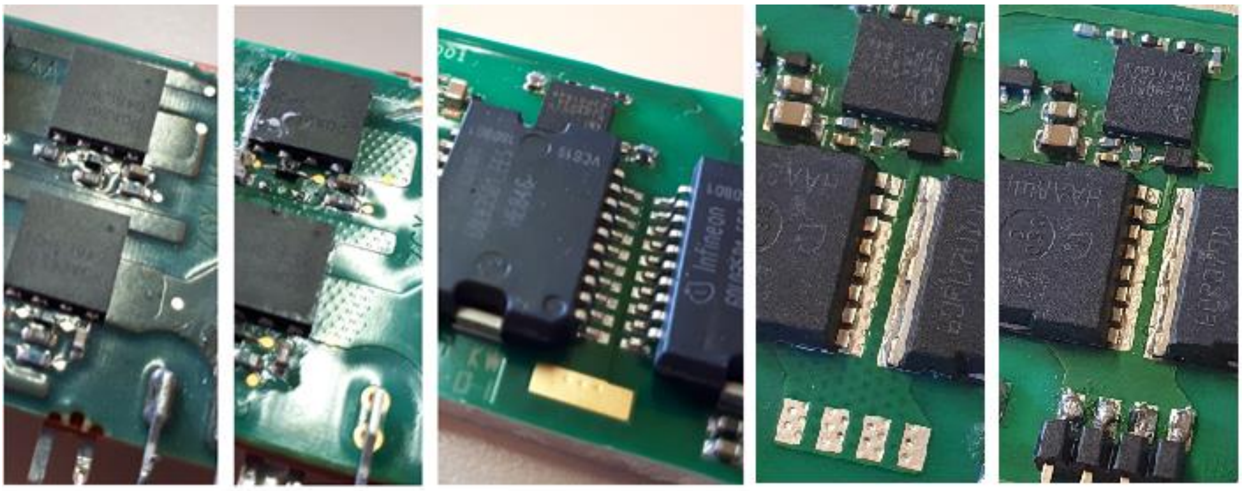


Fig. 31: Physical construction of simulated samples (Copper Inlay, Thermal Vias B, IMS)

Chapter presents innovative solutions for cooling of minimized surface mount packages, used nowadays mainly for novel wide bandgap devices for power electronics using GaN and SiC material. Author believes that cooling is one of the major design constraints affecting lifetime of devices in the application and its resolution requires step to more advanced technology of printed circuit board comparing to what the industrial standard is nowadays.

Further improvements might lead to advanced manufacturing process – bonding chip of power semiconductor device directly on insulated metal substrate board, which might be significant improvement - by removing some of the thermal resistances and reducing the ones, which are present by shortening the distance (e.g., chip to PCB surface).

5 ASPECTS OF PCB CONSTRUCTION FOR HIGH OPERATING FREQUENCY CONVERTERS

Not only thermal performance is the main driver for printed circuit board design. Other aspects as minimum inductance of loops conducting pulse currents, optimization of materials used for core of the PCB and designing layout for full utilization of copper are part of the game. All mentioned topics are well known in power electronics since beginning of the switch mode operation designs - With Gallium Nitride and move to fast switching and potentially high operating frequencies of switching converters, extra care should be taken to avoid design problems and performance limitations.

5.1 Low inductive layout

Certain nodes of circuits where discontinuous current flows need to be optimized for parasitic inductance. As energy can be accumulated in parasitic elements, parasitic resonant circuits between inductance and capacitors (layout or components) are present in the circuit:

$$f_{res,p} = \frac{1}{2\pi\sqrt{L_P C_P}} \tag{7}$$

This might result in voltage or current oscillations, which put additional voltage stress on switching device, or simply radiate magnetic field and create problems with electromagnetic compatibility by disturbing other devices in surroundings.

Based on third Maxwell equation:

$$\int_l E(t).dl = -\frac{d}{dt}\int_S B(t).dA \tag{8}$$

or Faraday law of induction it can be said, that around wire connected to voltage changing in time, magnetic field is always present. Parasitic inductance in circuit cannot be removed from physical structure with real dimensions, but if we follow the manual described by equation, it can be minimized. The inductance is dependent on quantity named total magnetic flux, which needs to be minimized:

$$\Psi = \int_S B(t).dA \tag{9}$$

Based on the formula above, this can be done by minimizing A, or loop area around wire with flowing current. For practical performance this means, that path of the current should be always routed above its return path. This can be achieved by using ground planes connected to low equivalent series resistance (ESR) capacitors placed as close as possible to the switching device.

Insulated metal substrate board might be improved in terms of low inductive layout by using special manufacturing processes, metal part of IMS (1.5mm thick copper plate) can be connected to ground (Fig. 32), by blind or through hole vias. Per manufacturing process, vias connected to substrate from top layers require relatively high diameter (>1mm), which might not be a problem by using filled and caped technology, or often called via in pad technology. Placing vias between the top two layers and substrate in proper nodes, results in minimization of “loops” without significant PCB layout effort and space constrains, as the connection to ground pad might be added in pads of capacitors, switches and other components requiring low impedance connection – compromise between cooling and switching performance is achieved. In addition, base plate is connected to “silent” node, which can provide shielding function for other circuits in unit and improve performance in radiated electromagnetic spectrum.

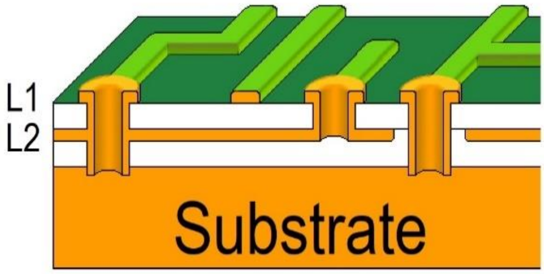


Fig. 32: Stack up of IMS PCB ideal for reduction of loop inductance

5.2 Dielectric losses and parasitic capacitance

One of the drawbacks of reducing thickness of layers for optimization of thermal performance is increased capacitance between tracks on the printed circuit board

According to well-known formula for the capacitor with two electrodes:

$$C = \varepsilon_0 . \varepsilon_r . \frac{A}{d} \tag{10}$$

represents situation on the PCB, where d is the thickness of insulating layers, ε is permittivity of insulating material and S is the area of the overlap. For switching node on IMS board, the area of the overlap is the complete size of polygon pour, as the ground plane (substrate) is under complete board. For prototype displayed at Fig. 32 the capacitance between switching node (output of totem pole) and substrate of board is 57pF, resulting in power loss 0.64W at 70kHz (400V bus voltage), which is dissipated in power MOSFETs during switching cycles. The result is acceptable, but especially for high efficiency converters operating at higher switching frequency not negligible.

As there exists capacitive current flowing through insulating material/core of the PCB, certain losses will be produced by “series” resistance of dielectric described by tanδ parameter. This problem might result in dielectric failure caused by overheating especially for high frequency operating converters (>1MHz).

5.3 Utilization of copper for low power losses

As the energy accumulated in parasitic inductance of circuit tries to stay minimal, current flows over path with minimum loop size, minimum inductance. Result of unwanted proximity effect is that current is concentrating in areas, not expected by original design intention, not all copper available on PCB is fully utilized. This might lead to significant increase of conducting losses in certain areas of the PCB, especially for high current circuits (>100A) and create hotspots.

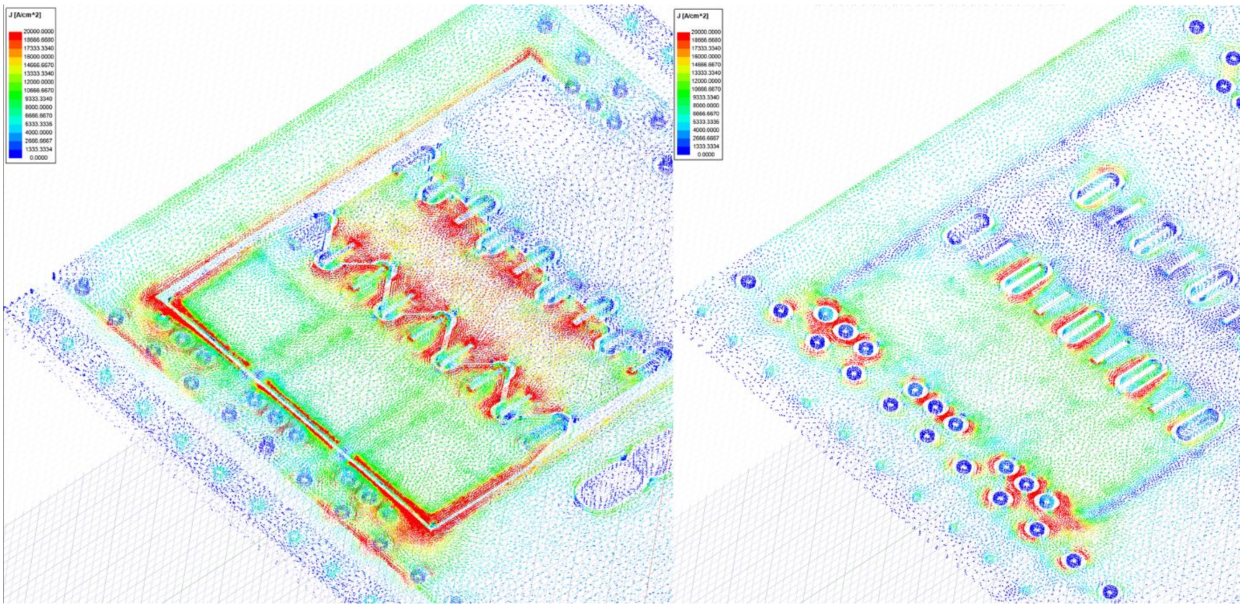


Fig. 33: Distribution of alternating current in PCB layers (before optimization)

For transformers and winded components this might be a problem resolved by using stranded wire, which is not possible in case of PCB. Distribution of current in layers is affected mainly by order of signals on the planes, shape of the plains, position of the vias interconnecting the layers and PADs of the components.

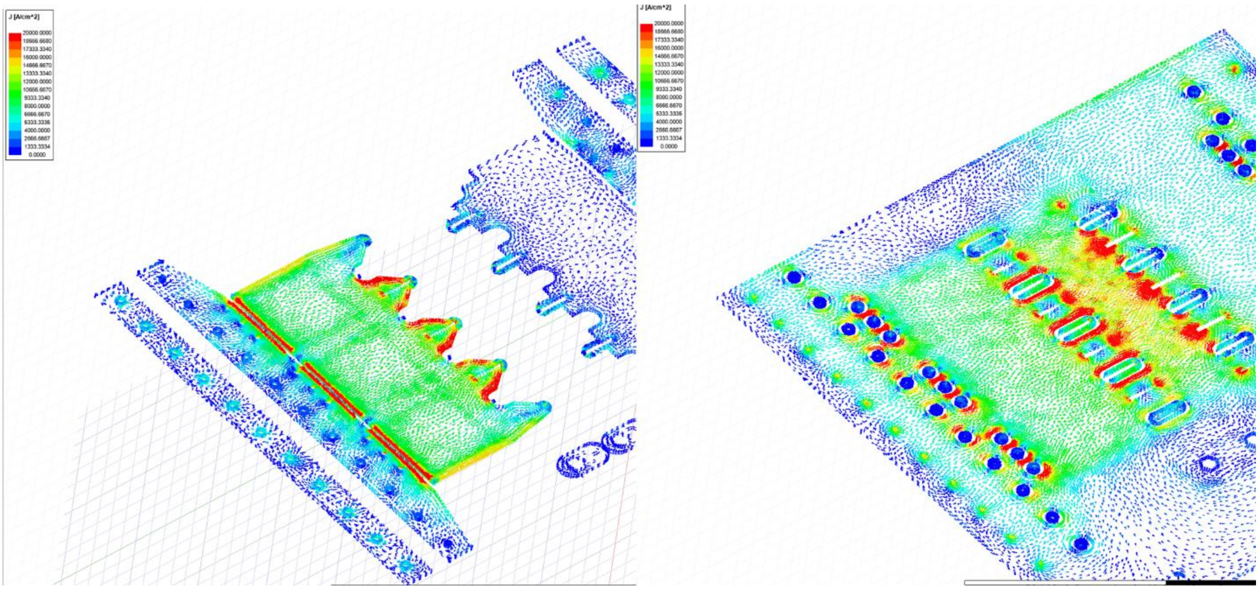


Fig. 34: Distribution of alternating current in PCB layers (after optimization)

Debugging of skin and proximity effect and other problems related to eddy currents on prototype of printed circuit board is difficult. As the thermal conductivity of copper is high, problem is not visible by thermal camera and measuring voltage differences in range of mV inside switch mode power supply is hardly affected by noise in the background.

The only executable way is electromagnetic FEM simulation which provides ability to plot a current density on PCB layers, before it is actually produced. Great example is shown in Fig. 33 before optimization and after optimization in Fig. 34. The plot shows top and middle layer of six-layer PCB - termination of transformer optimized for high power density - resonant converter with 12V/240A continuous output current (physical size of transformer is 50x50x40mm). The plot shows distribution of current on layer by the vector of current density, brighter red color means higher current density.

On non-optimized design in Fig. 33 in the middle layer it is visible, that current blindly follows its current in opposite direction on top layer, even if the whole layer is the same ground potential. By PCB design engineer this return path was reinforced on top layer, with good intention to reduce the conduction losses by increase of active copper cross section. FEM simulation shows that opposite is the truth. By simply cutting the part of copper pour on top layer, distribution of current is suddenly very different, visible in Fig. 34 on previous page marked as optimized version.

Simulation of this example was done in Ansys Maxwell. Difference of losses calculated by FEM, not considering temperature change of current exposed areas, is more than 7W (33W total for optimized version), which is more that 20% improvement.

This particular example shows that optimization of PCB for high dense switch mode power supplies with electromagnetic FEM simulation bring savings in terms of power losses and overall efficiency and might improve thermal management of the converter significantly.

6 DYNAMIC $R_{DS\text{-}ON}$ OF GAN DEVICES

The power loss in a semiconductor switch can generally be divided in two parts - switching and conduction power loss:

$$\Delta P = \Delta P_{Sw.} + \Delta P_{Cond.} \tag{11}$$

The switching power loss $\Delta P_{Sw.}$ is defined by energy dissipated during switching event multiplied by switching frequency. The conduction loss $\Delta P_{cond.}$ is defined as a product of squared rms current and resistance in conductive state of semiconductor device. It is assumed that the switching loss is linearly increased with switching frequency and conduction loss is in many cases considered to stay constant – as the on-state resistance and the device rms current remains the same over the frequency. As shown further in this chapter, due to defects in the semiconductor structure, the on-state resistance of a device is not constant and should be considered nonlinear at higher switching frequencies.

6.1 Theory of Measurement

In order to obtain a plot of the on-state resistance during a device operation cycle in a power electronic circuit, the Ohm law is applied:

$$v_{DS(t)} / i_{DS(t)} = r_{DSon(t)} \tag{12}$$

The current through the device $i_{DS(t)}$ and the voltage over the drain source terminals $v_{DS(t)}$ are measured during the device switching operation. Let’s consider following conditions for further analysis:

- a typical continuous conduction mode (CCM) operation
- the $v_{DS(t)}$ high voltage transition has settled before the $r_{DSon(t)}$ is measured
- inductor with a low inter-winding capacitance is used to connect the device switching node with the rest of the circuit

In this case we can consider the current through the device constant in a short time scale and the bandwidth of the current probe not critical. Therefore, a 50MHz BW current probe used in the inductor path is sufficient to emulate the device current. This allows to avoid the current sensor in the switching loop what is essential for a representative emulation of the normal device operation.

Sensing of the $v_{DS(t)}$ voltage is however a critical point. During device off time, the $v_{DS(t)}$ voltage reach a level of hundreds of volts while after a switch-on transient the $v_{DS(t)}$ quickly drops to few millivolts. Therefore, it is essential to use a $v_{DS(t)}$ sensing with a high dynamic range. When taking the speed requirements into account, the task is getting quite challenging.

An alternative option is to use a clamping circuit which protects the $v_{DS(t)}$ sensing device to saturate in off-state and enables the transfer of a signal in mV range to the sensing device in on-state conditions. Typically, a HV signal diode is used to clamp the $v_{DS(t)}$ voltage as shown in [3][4][16]. The common issue of this solution is the diode drop voltage which is not easy to characterize / calibrate when taking the very fast transient conditions the diode is exposed to into account.

To avoid issues mentioned above a novel clamping circuit was developed. The circuit features following advantages:

- Very low impedance clamping capability to block the high voltage propagation into the sensing device
- Effectively zero-voltage drop between the DUT and the $v_{DS(t)}$ sensor resulting in precise R_{DSon} evaluation
- A capability to measure $r_{DSon(t)}$ down to 70-100ns after the DUT switch on
- A high $r_{DSon(t)}$ sensing BW

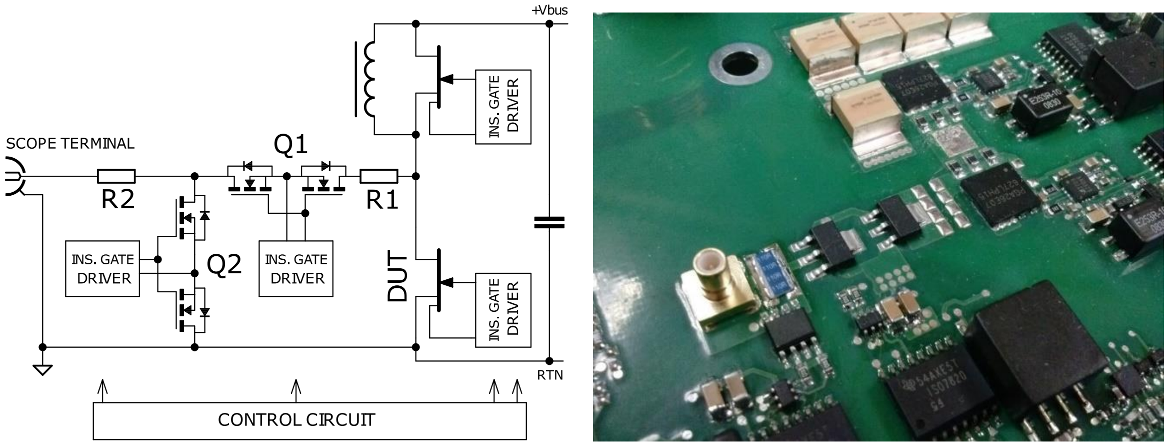


Fig. 35: Block diagram of dynamic R_{DSon} measurement setup

6.2 Description of Test Setup

The proposed $r_{DSon(t)}$ tester (Fig. 35) consists of two parts – the power circuit and the measurement circuit.

6.2.1 Power circuit

To get test conditions which are relevant and as close as possible to the end application of the semiconductor device, the power circuit of the tester consists of a half-bridge, which is common for power topologies (totem pole PFC, DC/DC converters, inverters, etc.). For the gate control a fast gate driving circuits are used. Both HS and LS switch drivers are equipped with isolated power supplies to avoid parasitic noise coupling into the control and signal sensing circuits.

6.2.2 Measurement circuit

The measurement block of the tester consists of two low capacitance switches (Fig. 35): A clamping device Q2 which protects the scope input from saturation during DUT off-state and a coupling switch Q1 which connects the $v_{DS(t)}$ to the scope input during DUT on-state.

The Q1 is rated to withstand the bulk voltage +Vbus which supplies the HB circuit of the tester. The switch is turned off during DUT off time. It is important to select a device with a very low Q_{oss} capacitance to minimize the capacitive current flowing through the clamping switch Q2 during switching transients. Two 500V rated silicon FETs in anti-series configuration are used to meet requirements.

Two low voltage EPC GaN transistors (Q2) are used to clamp the $r_{DSon(t)}$ voltage during DUT off-state. Low Q_{oss} of these GaN devices is essential to keep parasitic capacitance in the measurement signal path low, because the Q_{oss} together with series resistors (R1, R2) operates as a low pass filter in the signal path.

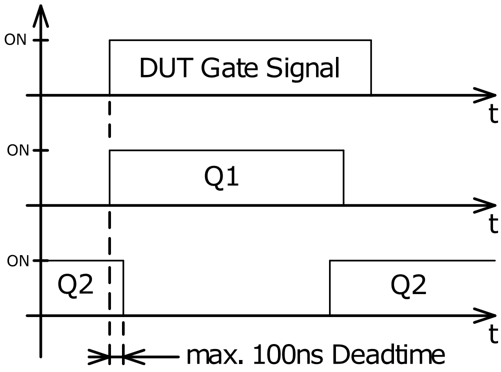


Fig. 36: Switching diagram of Q1 and Q2 vs. DUT timing

Referring to Fig. 36 the operation of the tester is explained by control waveforms which ensure the scope input is protected from the HV overload and can detect $v_{DS(t)}$ at 20mV/div setting. The series resistors in the signal path are designed to provide required SWR and therefore a relatively flat transfer function. The 50Ω scope termination together with series resistors in the measurement signal path creates however a voltage divider which is taken into account in on state resistance calculation. To obtain a maximum measurement precision the $v_{DS(t)}$ voltage sensing is calibrated in DC mode. Fig. 37 shows the transfer function of the signal path between DUT drain-source terminals and the scope input in range of 500MHz, measured by the network analyzer Agilent 4395A. Signals for gate drivers are generated by TI Picollo DSP – TMS320F280049.

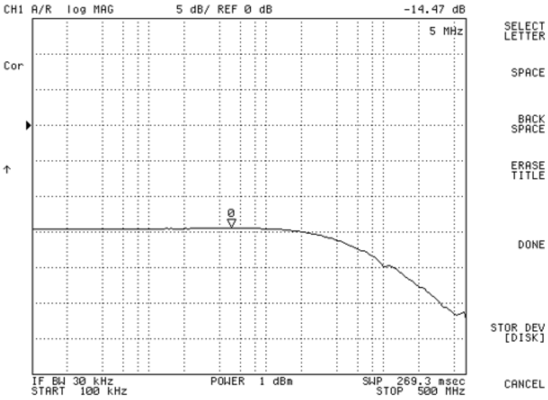


Fig. 37: Transfer function of the measurement signal path

6.3 Test Results

Three samples of GaN transistors from three different manufacturers were tested. The test was conducted at 2 different bulk voltage levels. The test sequence consists of three switching cycles to increase the current through the choke to the test level. The voltage and current data acquisition is conducted during the last pulse sequence. The length of the pulse sequence, the peak current and the test voltage is for all samples the same. Consequently the $r_{DSon(t)}$ plot is constructed starting shortly (70-100ns) after DUT turn-on transient. Because all tested devices have a different static R_{DSon} figure, the resistance displayed in graphs is normalized to the value in steady state (DC conditions) to emphasize the comparison (Table 1). The R_{DSon} in steady state is matching the datasheet specification for all samples (note the datasheets are often preliminary and manufacturers continuously updates the data). Fig. 39 and Fig. 40 summarize $r_{DSon(t)}$ results while $v_{DS(t)}$ in off-state is a parameter.

Based on test results the following findings can be formulated.

6.3.1 Short transient increase

A short transient/dynamic on state resistance was detected for samples #1 and #3. This behavior is affected by the test voltage (e.g. voltage present on a DUT before the turn-on transient). The effect is more pronounced at high test voltage. Sample #2 however does not exhibit the short transient increase.

6.3.2 Long transient increase

A long transient increase is detected on sample #1 and #2, where the on-state resistance drops down to the static value over a long time (time range couple of *ms*). The only sample with no long transient increase is the sample #3.

Fig. 38: Scope snapshot of GaN R_{DSon} tester operation

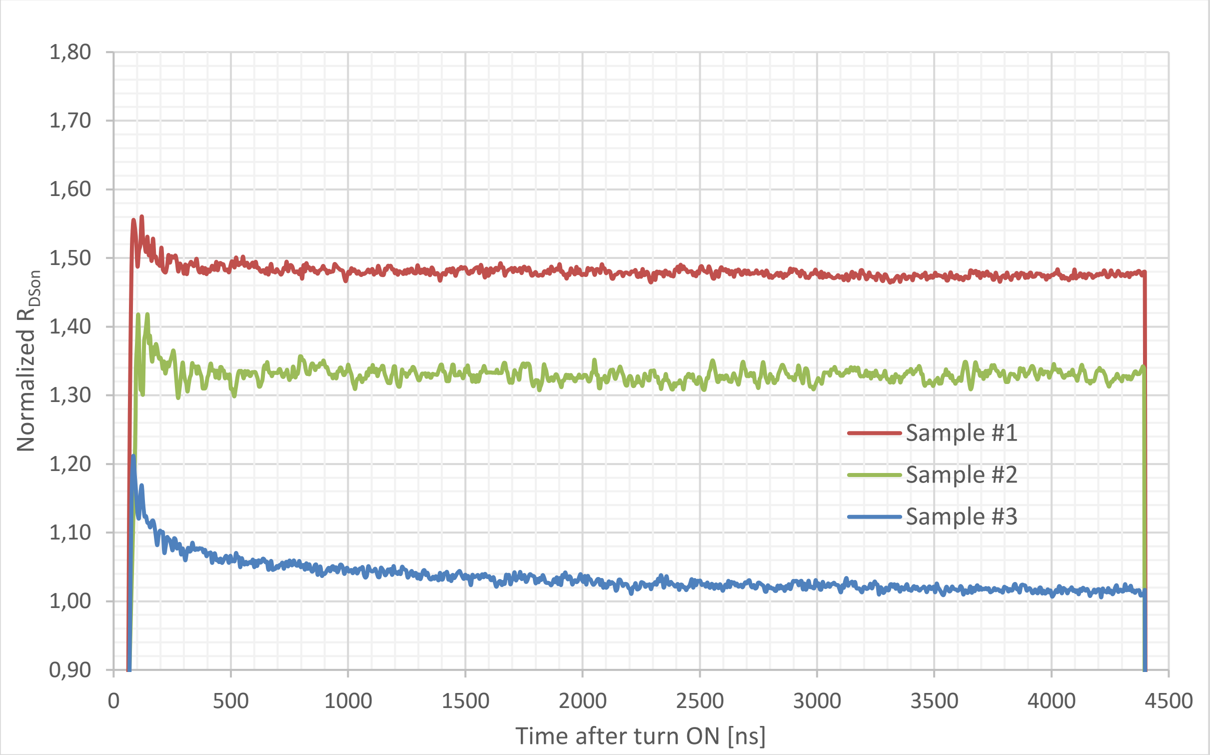


Fig. 39: Plot of normalized R_{DSon} vs. time after turn-on of three tested samples, bulk voltage 200V

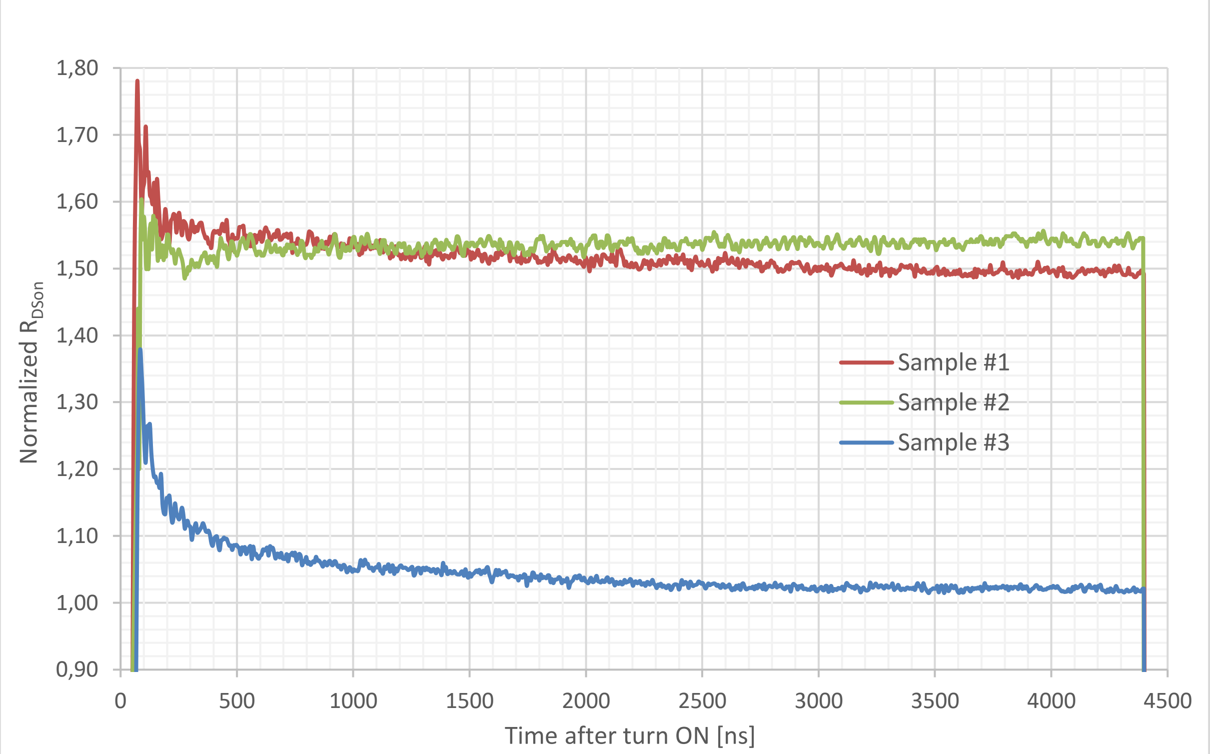


Fig. 40: Plot of normalized R_{DSon} vs. time after turn-on of three tested samples, bulk voltage 400V

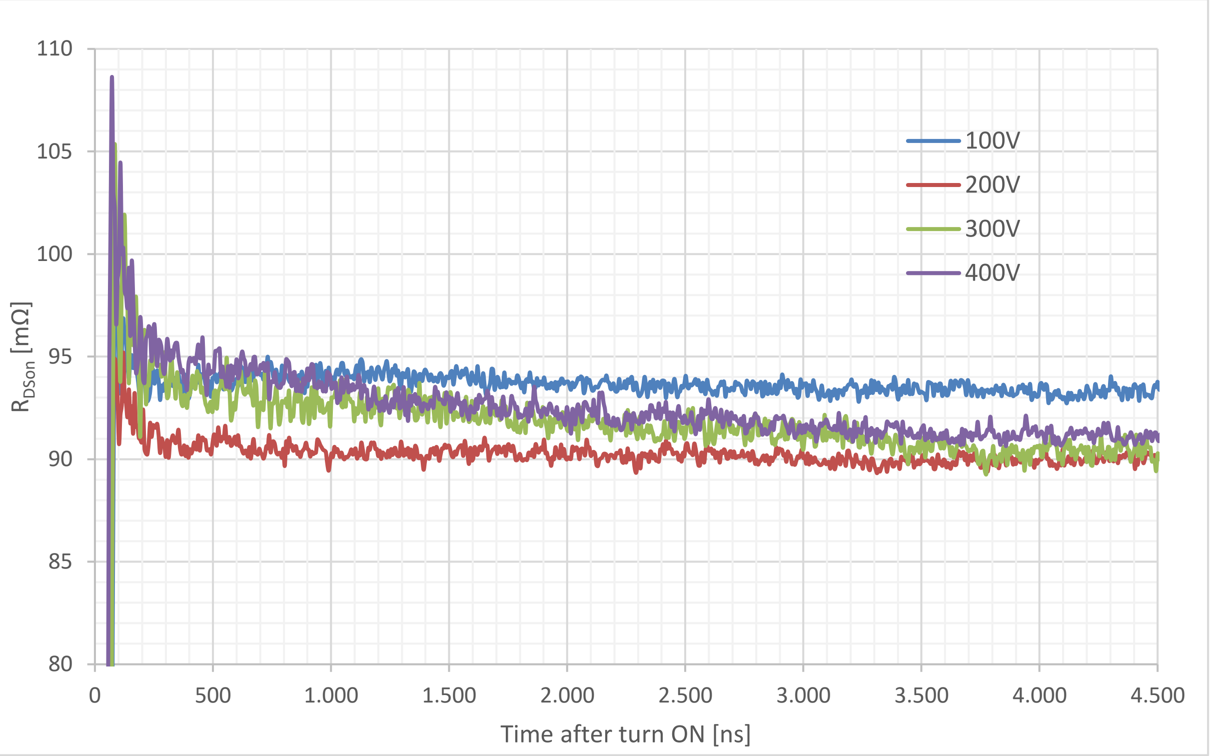


Fig. 41: Plot of R_{DSon} vs. time after turn-on of sample #1, for four different bulk voltages

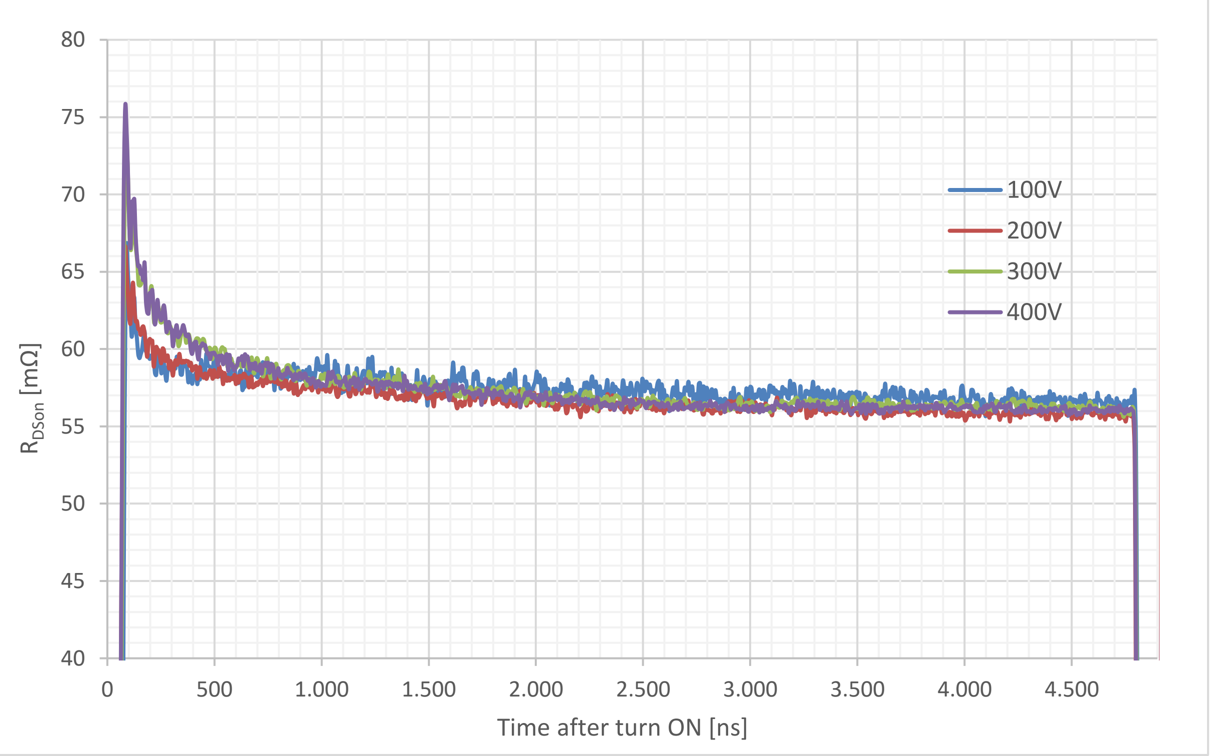


Fig. 42: Plot of R_{DSon} vs. time after turn-on of sample #3, for four different bulk voltages

Because all tested samples have a different internal structure, the mechanism of dynamic R_{DSon} is likely different. Root cause for the dynamic R_{DSon} is the electron trapping in crystal defects [14], however the test results indicate that each provider of the sample handles the electron trapping in a different way.

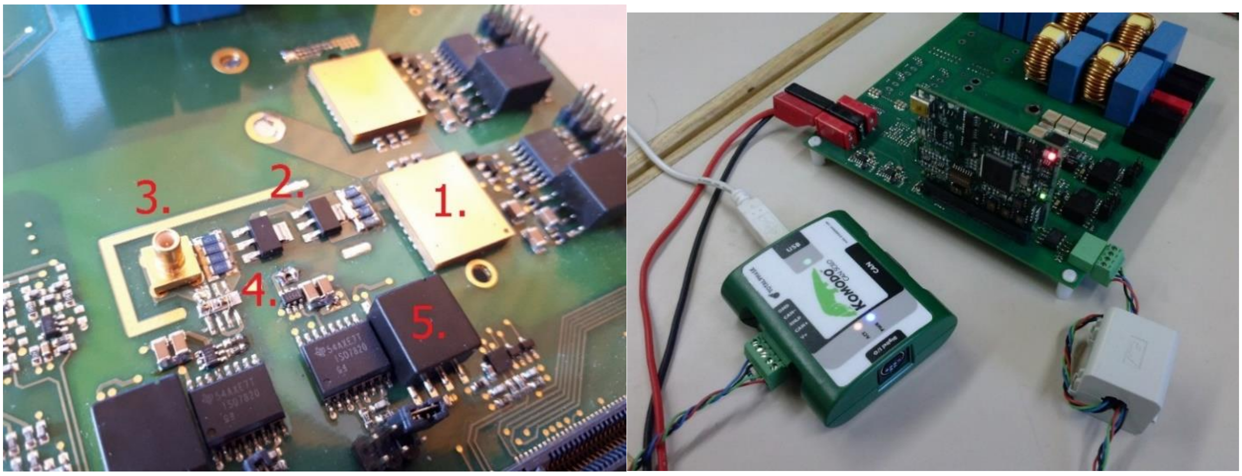


Fig. 43: Detail of the proposed tester (during sample #2 test)

1. - Device under test, 2. - Q1, 3. - Scope terminal, 4. - Q2, 5. Gate Drivers

The conclusion is that all the samples will exhibit an increased conduction loss in the application and the effect cannot be predicted from the manufacturer’s datasheet. On the other hand, the relative increase will be more significant at higher operating frequencies (>1MHz) in case of sample #3. In case of sample #1 and #2 the increase is permanent during the on state.

Table 1: Part numbers and catalogue R_{DSon} of tested samples

Sample	***Part Number***	***Datasheet R_{DSon}***	***Normalized/DC R_{DSon}***
#1	GaN Systems GS66506T	67mΩ	61mΩ
#2	VisIC V22N65A	22mΩ	22mΩ
#3	Panasonic PGA26E07	56mΩ	55mΩ

To prove that the test setup is not affected by parasitic elements, PCB was reworked with standard silicon MOSFET and the measurement of R_{DSon} vs. time after turn-on was performed in the same way as for GaN samples. As tested device the silicon MOSFET STD1NK60 available on market for several years was used, therefore proven technology without any variable R_{DSon} is expected, which is confirmed by measured results (Fig. 44). Rising curve of on state channel resistance is caused by output characteristics of the device – current through device drain-source is rising as the connected load is inductor. Measured characteristics is matching the one stated in the device datasheet.

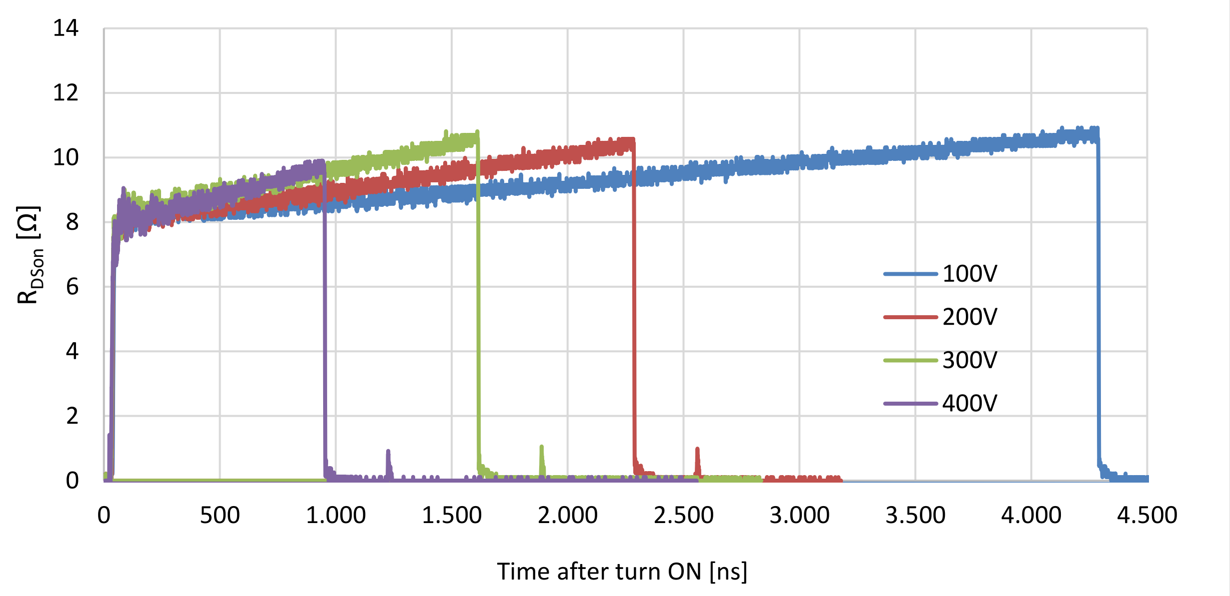


Fig. 44: Plot of R_{DSon} vs. time after turn-on of silicon transistor STD1NK60, for four different bulk voltages

Measurement of dynamic R_{DSon} is the part of JEDEC standard for qualification of wide bandgap devices. As can be seen from currently defined standard JC-70 available online [9], the exact definition of measurement setup is missing. Proposed method does not require special equipment for operation, therefore design and implementation to qualification process should be straightforward.

Design data of GaN R_{DSon} Tester (Schematic + PCB and BOM), created in student version of PCB design software Eagle (Autodesk), is available in electronic appendices to this thesis.

7 OPTIMIZATION OF DC/DC CONVERTER USING GAN SEMICONDUCTORS FOR HARD SWITCHING APPLICATIONS

Gained knowledge by investigating parameters of Gallium Nitride semiconductors and implementing of novel cooling methods in previous chapters, will be applied in a design of a power converter in this chapter. Based on parameters of available GaN power MOSFETs and a possible improvement of switching losses mainly, high voltage (400VDC) DC/DC converter is a scope of focus.

As the majority of nowadays produced electronic devices have to contain power factor correction, is for analysis chosen totem pole topology (Fig. 45) suitable for middle range power (3kW). Converter is designed for operating voltage range meeting one phase European mains voltage with tolerance. With certain power derating, operation starting from 90VAC input voltage (USA, JAPAN) is possible.

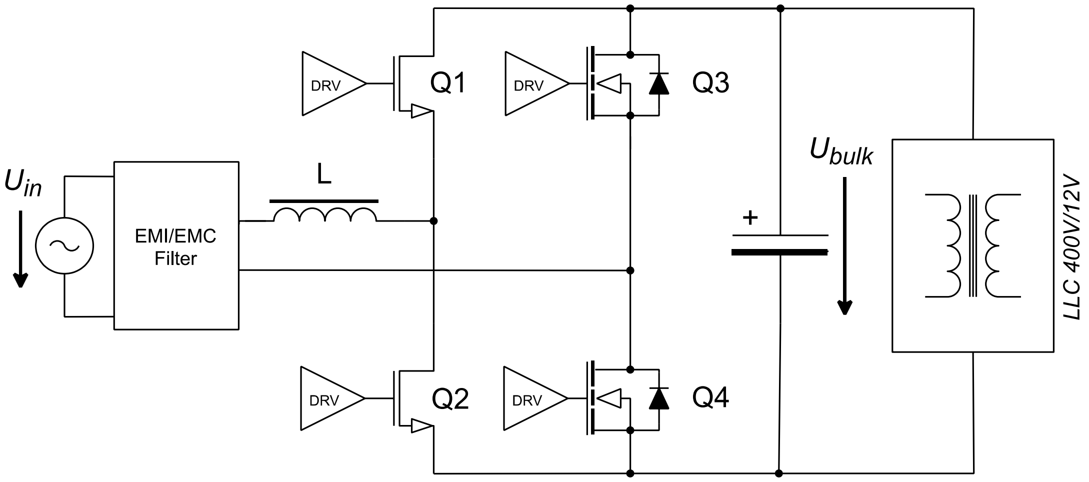


Fig. 45: Simplified block diagram of totem pole power factor correction converter with a DC/DC converter on the output

Input power factor correction with this input and power requirements can be found nowadays mainly in power supplies for Server, Data center and Telecom applications. Quantity of power supplies produced for the aforementioned markets is rising significantly, as the demand for data storage is enormous due to rise of various social media and streaming services.

To make this growth in energy demand sustainable, innovative technology steps are needed. On one hand, development of carbon-dioxide free/environmentally friendly energy sources to cover the rising demand for electricity, on the other hand pushing for improvement of existing solutions to make them more effective, therefore less energy demanding. In applications where high volume of power supplies is used, every watt of power loss is multiplied by quantity of installed systems – by improving single unit overall saving is significant.

This simple fact is recognized by European Union Commission, which is pushing for efficiency of power supplies used for computer applications. Those requirements are evolving over time, which works partially as a booster for the economy. Nowadays, all power supplies sold on European market need to be compliant with 80plus Platinum certification. From year 2026, new regulations are applicable, requesting for 80plus Titanium certification, which might be challenging and expensive to meet without improvements in semiconductor technology. Table below shows required efficiency levels to fulfill the certificate – efficiency is measured input to output including all power stages inside with control circuits consumption and auxiliary converter load (standby output). Power consumption of FAN used for cooling installed inside power supply is excluded, FAN is supplied during the test externally.

Load condition	80 PLUS BRONZE	80 PLUS SILVER	80 PLUS GOLD	80 PLUS PLATINUM	80 PLUS TITANIUM
	Efficiency limit				
10%	-	-	-	-	90%
20%	81%	85%	88%	90%	94%
50%	85%	89%	92%	94%	**96%**
100%	81%	85%	88%	91%	91%

Table 2: 80plus efficiency limits, 80plus titanium applicable from 2026

As can be seen from the table, highest efficiency limit is always at half load. This requirement has origin in server applications, where redundancy of input power is required to avoid any data loss or operation failure in case of single PS unit failure. Therefore, during significant part of the lifetime power supply is operating in parallel with 50% load, where optimization makes highest effect from the system point of view. For the mentioned reasons, the intention is to show and explain design of converter optimized for highest efficiency and power density with novel semiconductors, which might be used as a reference for future designs of power supplies.

Designed PFC converter in this thesis is divided into several sub-blocks, to be able to fit into 40mm form factor, high dense power supply. Power stage for cooling and space reasons is designed on separated vertical board, which is soldered into main board. Power stage displayed in figure (Fig. 72) is using optimized thermal vias analyzed in this thesis. Optimization in terms of low inductive layout were taken into account. On the main board are located components as coils and capacitors and connectors, visible on simplified block diagram on previous page (Fig. 45). As the cooling is realized by high power FAN providing high air stream, heatsinks are relatively small and produced from aluminum sheet. For rectification of current in low-speed branch (Fig. 45 - Q3, Q4) is used low R_{DSon} silicon MOSFET in lead package.

7.1 Power stage design

For power factor correction converter design in this chapter, we are looking for power GaN transistor with R_{DSon} range from 30-70mΩ, to keep conduction losses in reasonable range, especially at minimum of input voltage. At the time of writing this thesis, there are only three candidates from three different manufacturers available:

Manufacturer and Part number	**Declared R_{DSon} at 25°C**	**Package style**
VisIC V22N65A	22mΩ/650V	Top – Manuf. Specific
GaN Systems GS66516B	25mΩ/650V	Bottom – Manuf. Specific
Infineon IGO60R070D1	70mΩ/600V	Bottom – PG-DSO

Table 3: Available GaN parts suitable for 3kW PFC

As the top side cooling has higher space requirements, for high speed/switching branch the GaN Systems GS66516B enhanced mode power MOSFET is chosen. Part from Infineon manufacturer is slightly underpowered for designed application which means lower efficiency, but as it is gate injection transistor technology, it is evaluated as a second candidate. From background information it is known, that Infineon manufacturer is developing 22mΩ GIT which should be available in year 2022, in the same package variant.

To reach the maximum switching speed, optimization of driving paths, together with implementation of negative driving voltage is necessary. Driver configuration is according to GaN MOSFET manufacturer proposal available online, with difference in gate charge resistors values (R_{ON} =3.3Ω, R_{OFF} =0Ω) which leads to significantly increased switching speed.

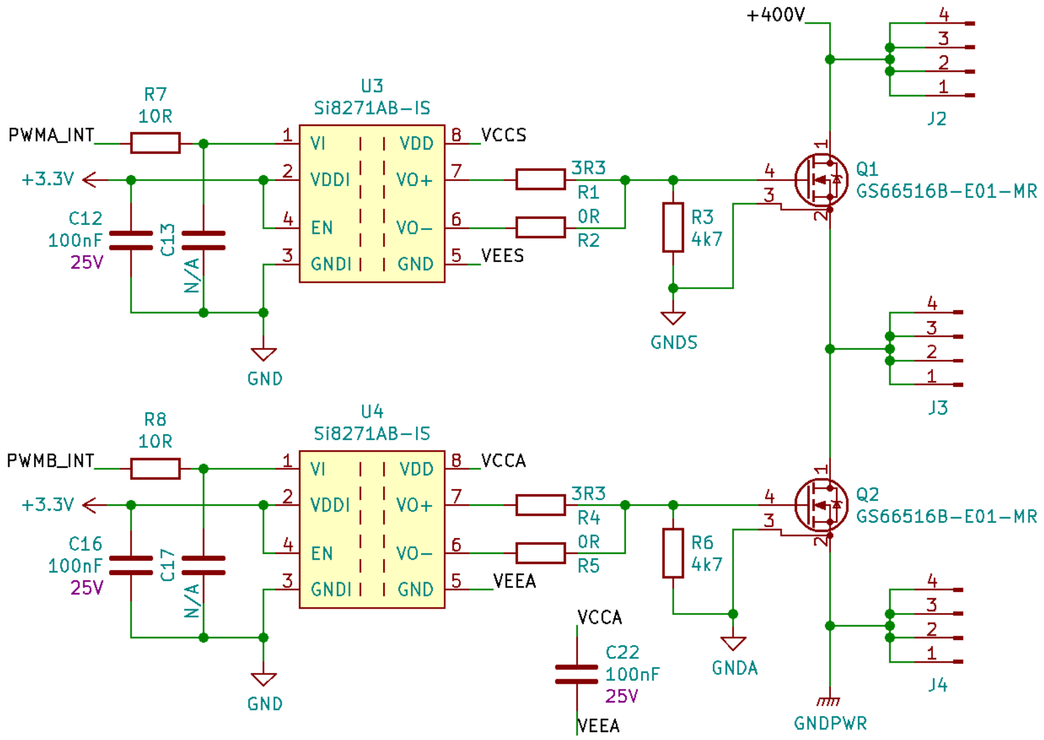


Fig. 46: Schematic of GS66516B gate driver

As a Gate driver integrated circuit the Silicon Laboratories part SI8271AB suitable for e-mode GaN driving voltage levels is chosen. Power for both, high and low side driver, is galvanically insulated over low inter-winding capacitance transformer. Supply voltage is generated by insulated transformer, positive and negative bias for driver is generated using Zener diode according to schematic below.

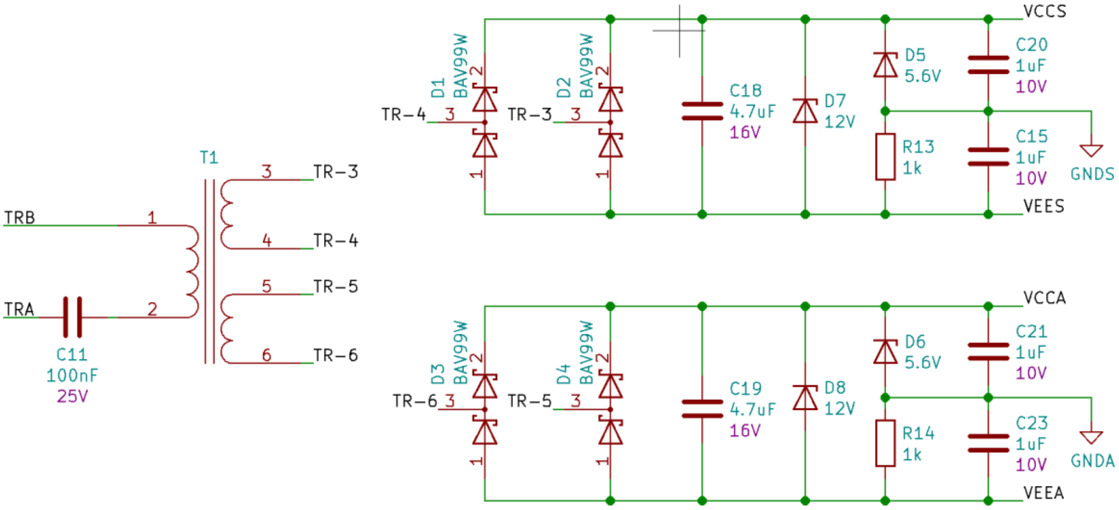


Fig. 47: Schematic of isolated driver power supply

Capacitance of the switch node against power ground, especially part of the circuit which is connected to kelvin contact of the transistor, needs to be optimized. This is one of the design criteria of the driver schematic, as actual size of components and its count need to be minimized as much as possible.

Power losses characterization of each component is necessary, to understand, if the cooling by insulated metal substrate board will be sufficient in all operating conditions. For analysis it is assumed, that control circuits are operating properly and input voltage and current are following sinusoidal shape and there is no phase shift (reactive power = 0):

$$U_{in}(t) = \sqrt{2}.U_{in,RMS}.\sin(2.\pi.f_{in}.t) \tag{13}$$

$$I_{in}(t) = \sqrt{2}.I_{in,RMS}.\sin(2.\pi.f_{in}.t) \tag{14}$$

Where $U_{in,RMS}$ and $I_{in,RMS}$ represents RMS value of input voltage/current. Assuming sine wave shape of input voltage and current without phase shift, input RMS current is defined from output power and expected efficiency of the converter:

$$I_{in}(U_{inA}, P_O, t) = \frac{P_O}{\eta.U_{inA}} \tag{15}$$

Based on the reason stated above, the target is to achieve optimal design of the converter with high efficiency with maximum at half load operating condition. This optimization is at the same time optimization for cost, as the semiconductors are major cost driver - descending curve of efficiency after half load means optimal usage of semiconductors and reasonable ratio between switching and conducting losses. Rising curve or stagnating curve at point of half load means, that converter is overrated and can deliver higher power than designed.

They way how to achieve this target is, obviously, to reduce the converter losses:

$$\Delta P = \Delta P_L + \Delta P_T + \Delta P_{T,R} + \Delta P_{AD} \tag{16}$$

Where ΔP_L represents losses in power inductor, ΔP_T represents losses in power switch, $\Delta P_{T,R}$ represents losses in synchronous rectifiers and in additional losses ΔP_{AD} are included conductor and dielectric losses in PCB, connectors and others. Detailed analysis and optimization separately for each part is necessary.

7.2 Inductor optimization for High Efficiency at half load

One of the major contributors into overall power loss is power inductor. Distribution between power losses in inductor core and winding is depended on various parameters as number of turns, switching frequency of the converter and operating point in terms of input and ambient conditions. Ripple current is changing over operating conditions and affecting rms value of the current, which flows through power semiconductors. Therefore, it is varying conduction/switching losses in different parts of the circuits, especially at light load conditions. From this thought it is clear, that there exists certain optimum for power losses and parameters chosen.

As one of the design inputs we assume powder core material for its cost effectivity and easy of manufacturing. Disadvantage of powder core material is relatively strong dependency of permeability of core on magnetic field, therefore inductance is not stable and varying with input current of converter.

Manufacturer of core states in the datasheet dependency of magnetic permeability versus magnetic field H (core material HighFlux 26μ):

$$\mu_{eff}(H) = \frac{1}{0{,}0385 + 6{,}84.10^{-8}.\left(\frac{H}{1\boldsymbol{Oe}}\right)^{2.196}} \tag{17}$$

According to documentation, parameters in equation were gained empirically, by measurement on the “average” core.

With knowledge of magnetic permeability and core dimensions, inductance can be calculated based on formula:

$$L(I,N) = \frac{N^2.\mu_{eff}\left(H_{DC}(I,N)\right).A_e}{l_m} \tag{18}$$

To determine power loss in inductor winding, rms current at input of the converter needs to be calculated. For fast, simplified calculation of rms value formula (15) might be considered, which is not considering rms value of the ripple current. It depends on peak-to-peak value of the ripple current, RMS addition to line current might be significant, causing additional ohmic losses. Ripple current is determined by duty cycle of the converter and operating conditions (U_{IN}, f_{sw}) for each switching cycle. As the voltage in the bulk capacitor is set intentionally higher than peak of an input voltage, to keep capability to regulate current based on input voltage reference, totem pole converter operates as a boost converter. Duty cycle equation can be derived from equal power between input and output, assuming 100% efficiency of conversion:

$$\begin{gathered} P_{IN} = P_{BULK} \\ U_{IN}.I_{IN} = U_{BULK}.I_{BULK} \end{gathered} \tag{19}$$

Output current of the converter can be replaced by input current multiplied by duty cycle D, representing percentage of switching period, where inductor is demagnetized:

$$U_{IN}.I_{IN} = U_{BULK}.I_{IN}.D \tag{20}$$

Expressing duty cycle:

$$D_{HS\_CCM}(U_{RMS}, t) = \frac{U_{Bulk} - U_{in}(t)}{U_{Bulk}} \tag{21}$$

During magnetizing cycle, switch Q2 and Q4 (Fig. 45) is closed, input voltage is present on inductor terminals. With DC bias of the inductor core caused by input current, inductance value is changing over the period of input voltage. This variation affects value of ripple current significantly. Based on simplified formula, ripple current with respect to input operating conditions can be calculated:

$$\begin{gathered} di_L = \frac{U_L.dt}{L} \\ \Delta I_{CCMpk-pk}(U_{RMS}, P_{OUT}, N, t) = \frac{U_{in}(t).D_{HS\_CCM}(U_{RMS}, t)}{f_{sw}.L(I_{in}(U_{RMS}, P_{OUT}, t), N)} \end{gathered} \tag{22}$$

Peak inductor current is calculated as sinusoidal input current increased for half of the ripple current:

$$I_{pk}(U_{RMS}, P_{OUT}, N, t) = I_{in}(U_{RMS}, P_{OUT}, t) + \frac{\Delta I_{CCMpk-pk}(U_{RMS}, P_{OUT}, N, t)}{2} \tag{23}$$

Rms current is calculated as integral of actual current over period of input voltage increased for ripple current part:

$$\Delta I_{L,RMS}(U_{RMS}, P_{OUT}, N) = \sqrt{\frac{1}{T}\int_0^T \left(I_L(U_{RMS}, P_{OUT}, N, t).\sqrt{1 + \frac{\delta^2}{3}} \right)^2 .dt} \tag{24}$$

Where parameter δ shows relation between ripple current $\Delta I_{CCMpk-pk}$ and average current, which is in this case equal to actual value of input, sine wave current I_{in}:

$$\delta = \frac{\Delta I_{CCMpk-pk}(U_{RMS}, P_{OUT}, N, t)}{I_{in}(U_{inA}, P_O, t)} \tag{25}$$

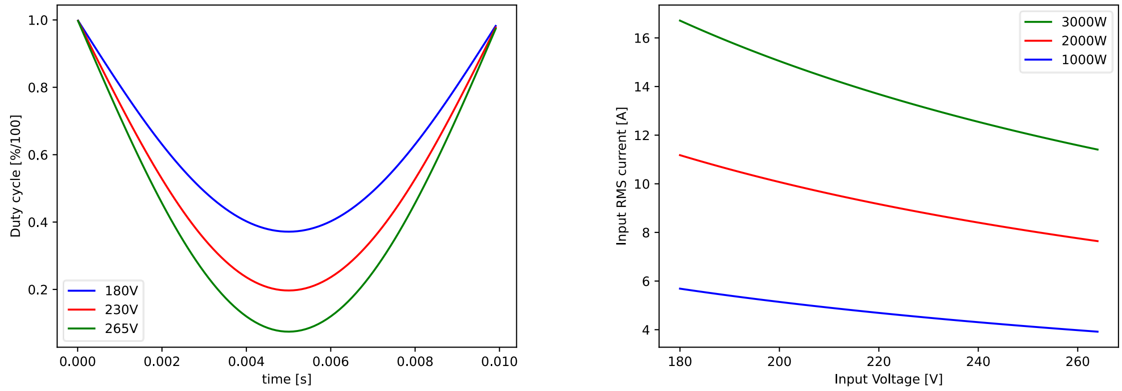


Fig. 48: Plot of duty cycle of totem pole converter during half period of input voltage (left), plot of input current RMS value in various operating conditions (right)

To define conduction losses in the winding, wire diameter needs to be specified. Assuming that window of toroid core can be filled with round copper wire up to certain percentage of the area defined by copper fill factor:

$$\frac{\pi . d_w{}^2}{4} . N = \frac{\pi . ID^2}{4} . k_{Cu} \tag{26}$$

Where ID is internal diameter of the core window, $d_w$is diameter of wire and N is for number of turns. Copper fill factor is for toroidal core relatively small (k_{Cu}= 0.2-0.4), as place for arm of a winding machine needs to be reserved. From this equation wire diameter based on number of turns can be calculated:

$$d_w(N) = ID . \sqrt{\frac{k_{Cu}}{N}} \tag{27}$$

Electrical resistivity of copper wire is changing with temperature and therefore with operating conditions of the converter. Assuming operating temperature υ_W of winding at worst conditions, means lowest operating input RMS voltage and maximum output power, resistance of wire is calculated by following formula:

$$\varsigma_{Cu}(\upsilon_W) = 1{,}68 . 10^{-8} . (1 + 0.0039 . (\upsilon_W - 20)) \tag{28}$$

$$R_{Cu}(U_{RMS}, P_{OUT}, N) = \varsigma_{Cu}\left(\upsilon_W \cdot \frac{P_{OUT}}{P_{OUT,MAX}} \cdot \frac{U_{IN,MIN}}{U_{IN,RMS}}\right) \cdot \frac{N . MLT}{\frac{\pi . d_w(N)^2}{4}} \tag{29}$$

Where MLT represents mean length of turn.

Power loss is a function of operating conditions (U_{RMS}, P_{OUT}), number of turns N and can be calculated as:

$$\Delta P_{Cu}(U_{RMS}, P_{OUT}, N, d) = R_{Cu}(U_{RMS}, P_{OUT}, N, d).\Delta I_{L,RMS}(U_{RMS}, P_{OUT}, N)^2 \tag{30}$$

This simplified formula for power loss in the inductor winding is not considering increase of resistance due to the proximity effect at higher frequencies. With high ripple current and switching frequency of power converter power loss increase might be significant comparing to DC value, which is not expected in this particular design and is neglected.

Manufacturer of powder core provides results of empiric measurements of volume power losses (W/m^3) based on operating frequency and magnetic flux density:

$$\Delta P_{HF}(B, f) = \left(\frac{B}{1000G}\right).(3{,}4.f + 0.0006.f^{2{,}736}) \tag{31}$$

From formula of the magnetic flux:

$$\phi = N.B.A_e \tag{32}$$

Magnetic flux density can be calculated using duty cycle of the converter and actual input voltage (V.s), core parameters and switching frequency:

$$B_{pk}(U_{RMS}, P_{OUT}, N, t) = \frac{1}{2}.\frac{U_{in}(t).D_{HS\_CCM}(U_{RMS}, t)}{f_{sw}.N.A_e} \tag{33}$$

Using empiric formula defining power losses ΔP_{HF} and volume of a core V_e, power loss over period of input voltage can be calculated:

$$\Delta P_{Core}(U_{RMS}, P_{OUT}, N) = \frac{1}{T_{in}}\int_0^{T_{in}} V_e.\Delta P_{HF}\big(B_{pk}(U_{RMS}, P_{OUT}, N, t), f_{sw}\big)dt \tag{34}$$

With defined core and wire power losses, graph displaying relation between number of turns and total power loss at half load and nominal input voltage can be plotted (Fig. 49):

$$\Delta P_L(U_{RMS}, P_{OUT}, N) = \Delta P_{Cu}(U_{RMS}, P_{OUT}, N, d) + \Delta P_{Core}(U_{RMS}, P_{OUT}, N) \tag{35}$$

Optimal wire turns for lowest inductor power losses can be found by derivation of equation for variable N equal to zero:

$$\Delta P_L(U_{RMS}, P_{OUT}, N)' = 0 \tag{36}$$

As the optimum of the losses is relatively flat between 40-44 turns, for easy of manufacturing 42 turns of round profile, isolated wire was chosen with diameter 1.4mm, which results to power loss at the point of optimization:

$$\Delta P_L(230VAC, 1500W, 42T.) = 3.32\text{W}$$

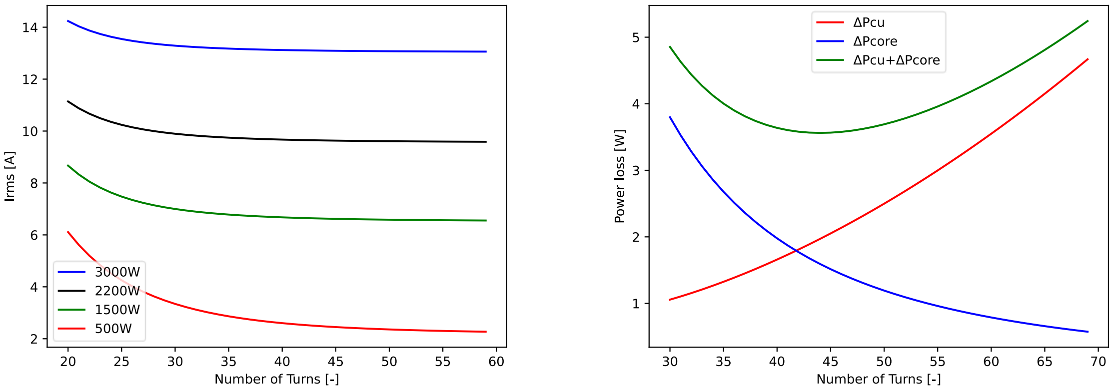


Fig. 49: Plot of input RMS current versus number of turns and various output operating conditions (left), Plot of inductor total power losses versus number of turns at nominal operating condition (right)

7.3 GaN power stage losses evaluation

Power loss of GaN power MOSFETs can be divided into following parts:

$$\Delta P_T = \Delta P_{T,R_{DSon}} + \Delta P_{T,Sw} + \Delta P_{T,RevC} \tag{37}$$

Where $\Delta P_{T,R_{DSon}}$ is representing conduction losses depended on the square root of the current flowing through the device, $\Delta P_{T,Sw}$ are switching losses and $\Delta P_{T,RevC}$ are losses caused by reverse conduction of the current. To calculate conduction losses, precise value of RMS current needs to be calculated first. The current is flowing through the device during period only for limited time defined by duty cycle, which is changing based on actual input voltage and bulk voltage (Fig. 48). Ignoring ripple current which is added on top of the operating current, rms value of a current can be calculated by following equation:

$$I_{H,RMS}(U_{RMS}, P_{OUT}) = \sqrt{\frac{1}{T}\int_0^T \left(i_L(U_{RMS}, P_{OUT}, N, x).\sqrt{D_{HS_{CCM}}(U_{RMS}, t)}\right)^2 .dt} \tag{38}$$

$$I_{L,RMS}(U_{RMS}, P_{OUT}) = \sqrt{\frac{1}{T}\int_0^T \left(i_L(U_{RMS}, P_{OUT}, N, x).\sqrt{D_{LS_{CCM}}(U_{RMS}, t)}\right)^2 .dt} \tag{39}$$

While looking at half-period of line voltage, duty cycle for high side and low side switch is not the same. As the RMS value is calculated over period of the line voltage, input voltage polarity is changing and second half-period is the opposite of the first. Therefore, conducting power losses are not equivalent for both devices during half period – but both equations will return exactly the same value as integration is done over the line period.

Losses difference can be observed by thermal camera while operating converter with high DC input voltage (240-380VDC), typical for telecom applications where system is supplied by high voltage battery. Different power losses mean different cooling requirements comparing to AC operation – certain input/output power derating is applied.

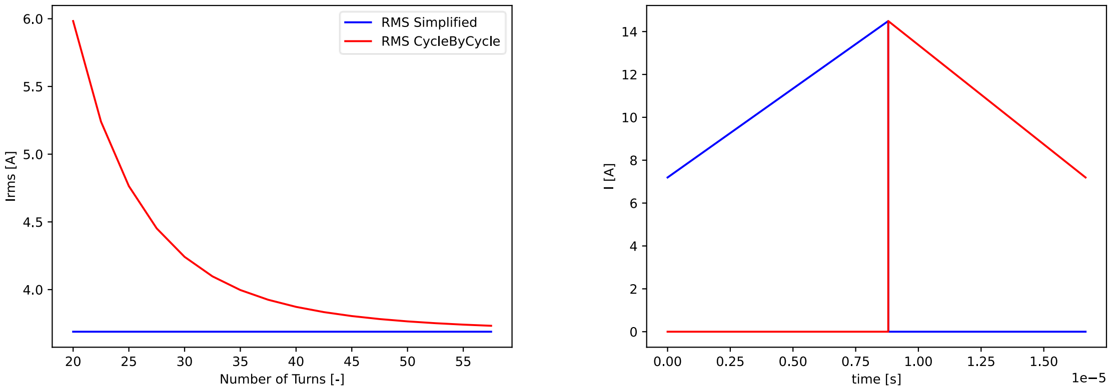


Fig. 50: Difference in RMS current flowing through power switch versus number of turns calculated by simplified and cycle by cycle calculation (left), Plot of current waveform in one switching cycle (T_{line}=2ms, N=40, 230V_{in}/3kW) (blue-high side, red-low side switch)

To avoid error introduction in calculation of the RMS current, cycle by cycle calculation method using scripting language Python is used. This method simply integrates square root of current over every switching cycle (Fig. 50) during period of the line voltage with consideration of ripple current:

$$I_{RMS,Cycle}(U_{RMS}, P_{OUT}, N, t) = \sqrt{\frac{1}{T_{SW}}\int_0^{T_{SW}} i_{Switch}(U_{RMS}, P_{OUT}, N, t)^2 . dt_{SW}} \tag{40}$$

In second step the period RMS is calculated by summing all switching cycles in line voltage period (T/T_{SW}):

$$I_{T,RMS}(U_{RMS}, P_{OUT,}N) = \sqrt{\frac{1}{T}\int_0^{T} I_{RMS,Cycle}(U_{RMS}, P_{OUT}, N, t)^2 . dt} \tag{41}$$

Results comparing simplified calculation method and cycle-by-cycle calculation are visible in Fig. 50. By reducing ripple current down to 0 by increasing inductor wire turns, both equations return same value, which is correct.

With knowledge of RMS current through power switch, conduction losses can be calculated for high and low switch in the power stage:

$$\Delta P_{TH,R_{DSon}}(U_{RMS}, P_{OUT}, N) = I_{T,RMS}(U_{RMS}, P_{OUT}, N)^2 . R_{DSon}(Tj) \tag{42}$$

$$\Delta P_{TL,R_{DSon}}(U_{RMS}, P_{OUT}, N) = I_{T,RMS}(U_{RMS}, P_{OUT}, N)^2 . R_{DSon}(Tj) \tag{43}$$

For the half-bridge:

$$\Delta P_{T,R_{DSon}}(U_{RMS}, P_{OUT}, N) = \Delta P_{TH,R_{DSon}}(U_{RMS}, P_{OUT}, N) + \Delta P_{TL,R_{DSon}}(U_{RMS}, P_{OUT}, N) \tag{44}$$

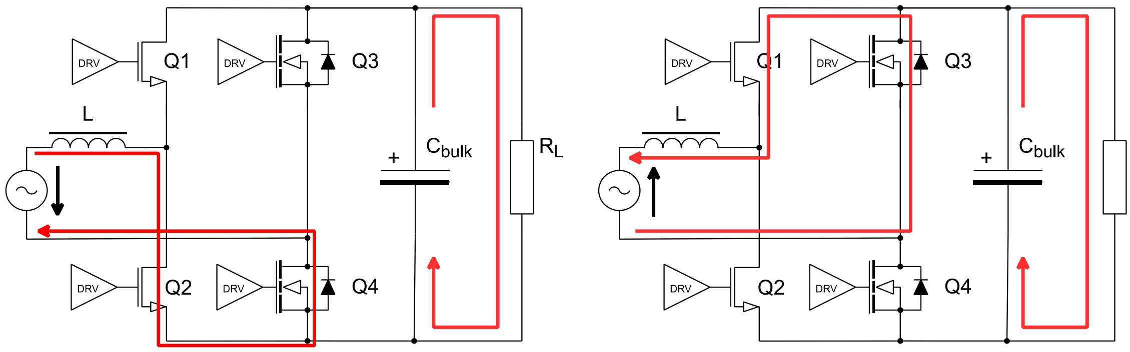
As the on-state channel resistance is strongly dependent on temperature of the chip, curve provided by manufacturer of GaN transistor is approximated by:

$$R_{DSon}(Tj) = 0.025.(0.6875 + Tj.0.0125) \tag{45}$$

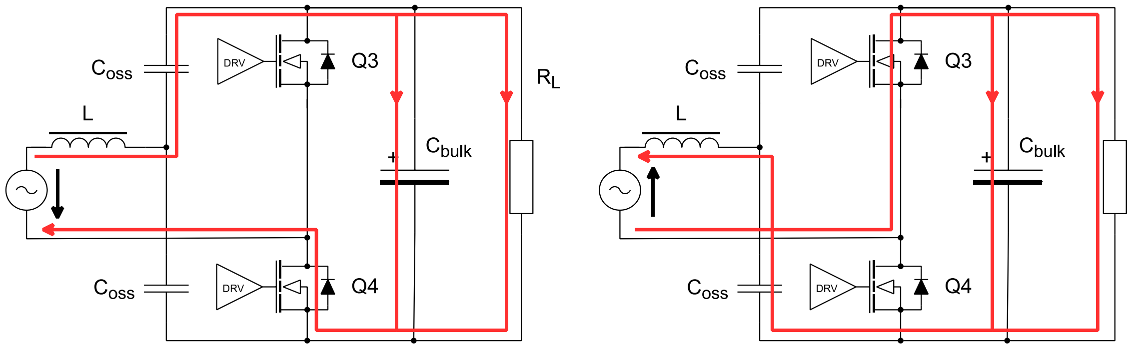
Switching losses can be calculated by analyzing separately turn-on and turn-off event:

$$\Delta P_{T,sw}(U_{RMS},P_{OUT},N)=\frac{\Delta E_{OnSwitch}(U_{RMS},P_{OUT},N)+\Delta E_{OffSwitch}(U_{RMS},P_{OUT},N)}{\frac{T_{in}}{2}} \tag{46}$$

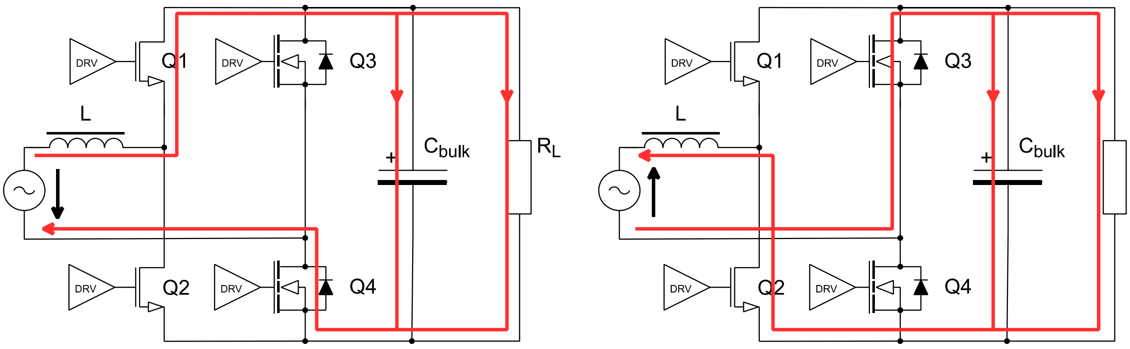
From operating states of the totem pole converter can be seen, that only one switch in half-bridge configuration is operating with switching power losses during half-period of the line voltage. After hard commutation, C$_{oss}$ is fully charged up to bulk voltage level and current continues to flow through opposite switch in reverse direction - zero voltage switching is achieved and switch works in rectifier mode. As the reverse recovery charge of GaN devices does not exists (according to manufacturer's specification), power dissipated during turn on is significantly smaller comparing to Silicon MOSFETs.



A. Positive Cycle - charging mode **D. Negative Cycle - charging mode**



B. Positive Cycle - commutation **E. Negative Cycle - commutation**



C. Positive Cycle - boost mode **F. Negative Cycle - boost mode**

Fig. 51: Totem pole converter operating states

Therefore, energy lost at turn-on event can be calculated by formula:

$$\Delta E_{On}(U_{RMS}, P_{OUT}, t) = \frac{1}{4} U_{BULK}.I_{SW}(U_{RMS}, P_{OUT}, t).t_{sw}(U_{RMS}, P_{OUT}, t) + E_{oss} + E_{qoss} \quad (47)$$

Where first part of the equation assumes, that drain-source voltage starts to drop after current reaches inductor value, energy pulse has triangular shape for certain time t_{sw}. As the current changes its value during the line voltage period, t_{sw} is varying with current. Assuming that transistor switching speed di/dt (3A/ns) and delay time td defined by manufacturer are constant, duration of turn-on power pulse can be calculated as:

$$t_{sw}(U_{RMS}, P_{OUT}, t) = \frac{I_{SW}(U_{RMS}, P_{OUT}, t)}{didt} + tf \quad (48)$$

Second part defines energy lost by charge of nonlinear intrinsic capacitance (C_{OSS}):

$$E_{oss} = \int_{0}^{U_{BULK}} u_d . C_{OSS}(u_d)^2 . du_d \quad (49)$$

And third part represents charge of nonlinear capacitance of opposite device in half bridge configuration [33]:

$$E_{qoss} = \int_{0}^{U_{BULK}} (U_{BULK} - u_d) . C_{OSS}(u_d)^2 . du_d \quad (50)$$

For purpose of calculation, nonlinear drain-source capacitance stated in manufacturers datasheet was converted into array of values using free web tool (WebPlotDigitizer by Ankit Rohatgi). Therefore, calculation of integrals stated above can be performed by python script (see Appendix no.7). Calculating E_{oss} by formula state above gives same value (17µJ) as stated in the datasheet (using same conditions), which is correct.

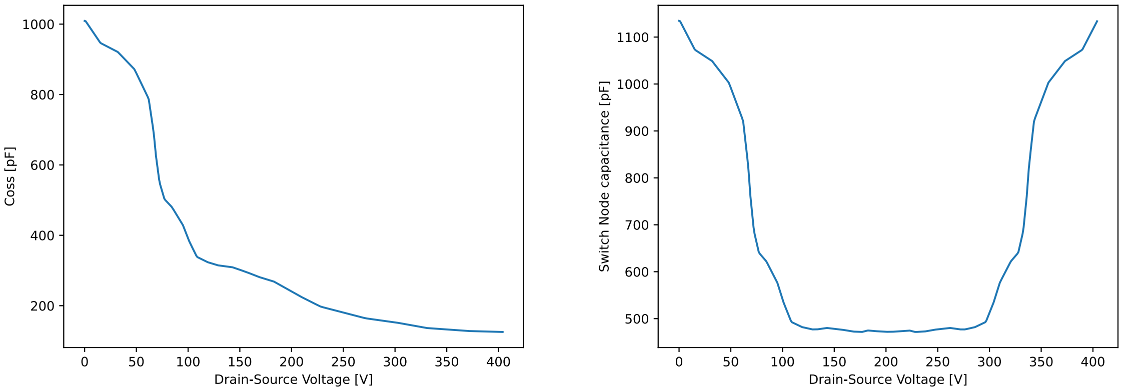


Fig. 52: Digitalized C_{oss} capacitance used for calculation (right), Switch node capacitance (excl. PCB layout, left)

Energy lost at turn-off event can be calculated according to:

$$\Delta E_{Off}(U_{RMS},P_{OUT},t)=\frac{1}{4}U_{BULK}.I_{SW}(U_{RMS},P_{OUT},t).t_{sw,off}(U_{RMS},P_{OUT},t) \tag{51}$$

Assuming same *didt*, $t_{sw,off}$ is partially depended on the current same as for turn on event:

$$t_{sw,off}(U_{RMS},P_{OUT},t)=\frac{I_{SW}(U_{RMS},P_{OUT},t)}{didt}+tr$$

Total energy lost during turn-on and off events over half period of line voltage can be calculated as sum of energy lost in every switching cycle:

$$\Delta E_{OnSwitch}(U_{RMS},P_{OUT})=\sum_{X=0}^{\frac{f_{sw}}{2.f_{in}}}\Delta E_{On}\left(U_{RMS},P_{OUT},\frac{f_{in}.x}{2.f_{sw}}.T_{in}\right) \tag{52}$$

$$\Delta E_{OffSwitch}(U_{RMS},P_{OUT})=\sum_{X=0}^{\frac{f_{sw}}{2.f_{in}}}\Delta E_{Off}\left(U_{RMS},P_{OUT},\frac{f_{in}.x}{2.f_{sw}}.T_{in}\right) \tag{53}$$

During transition between high and low side switch, is for certain time one of the switches conducting current in reverse mode. For e-mode and GIT transistor structure is the source-drain voltage in reverse conduction mode directly depended on the Gate-Source bias, voltage drop in reverse mode can be approximated by nonlinear curve:

$$V_{S\rightarrow D}\sim(V_{TH}-V_{GS})+I_{SD}.R_{SD}$$

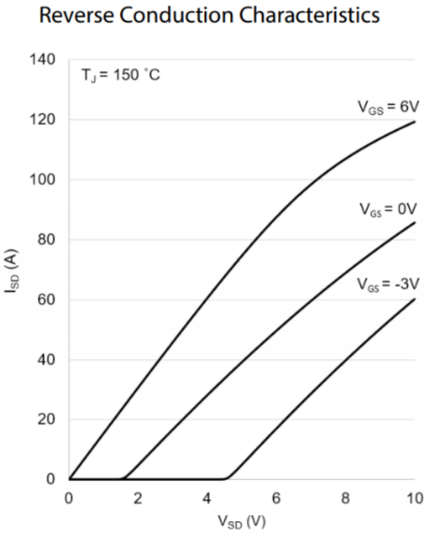


Figure 10: Typical I_{SD} vs. V_{SD}, $T_J = 150\,^{o}C$

Gate-source voltage at turn-off is for driver designed in previous chapter -3V, behavior of transistor in reverse mode can be characterized by equation:

$$V_{S\rightarrow D}(I_{S\rightarrow D})=4{,}3V+I_{S\rightarrow D}.0{,}095\Omega \tag{54}$$

Therefore, energy dissipated by reverse conduction can be calculated as:

$$\Delta E_{RevC}(U_{RMS}, P_{OUT}, t) = V_{S\rightarrow D}\big(I_{SW}(U_{RMS}, P_{OUT}, t)\big).I_{SW}(U_{RMS}, P_{OUT}, t).t_{deadtime} \qquad (55)$$

where $t_{deadtime}$ is fixed and its value is 50ns for both edges. Power loss assigned to reverse conduction of current can be calculated as sum of all events divided by half period of line voltage:

$$\Delta P_{T,RevC}(U_{RMS}, P_{OUT}, N) = \frac{\sum_{X=0}^{\frac{f_{sw}}{2.f_{in}}} \Delta E_{RevC}(U_{RMS}, P_{OUT}, t)}{\frac{T_{in}}{2}} \qquad (56)$$

As the control circuits of the experimental converter are supplied from external power supply, gate driving losses are not included in the total transistor losses. As the Total Gate Charge is 14.6nC and driving voltage 6V, is power required to supply gate driver very small, only ~50mW per device. This gives advantage for design of isolated power supply for gate driver.

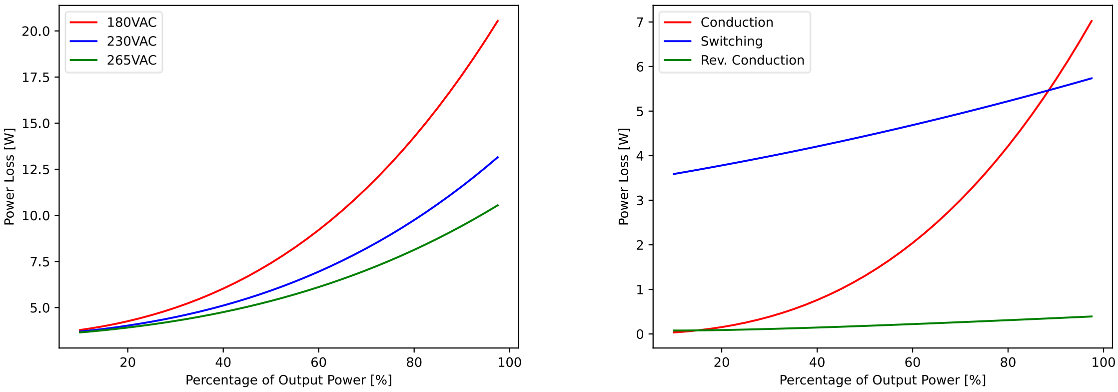


Fig. 53: Results of power losses calculation of GaN MOSFETs in 3kW totem-pole converter, dependency on output power and input voltage (left), overview of power losses at nominal operating conditions (right)

7.4 Synchronous rectifier

Instead of diodes in low-speed branch of the totem-pole the low on state resistance MOSFETs IPP60R022S7 are used, with intention to reduce power losses. Both of the rectifiers are conducting sine wave current (incl. ripple part) only for half of the line voltage period, no switching losses are present as the device is “permanently” ON. Power loss for synchronous rectifier can be calculated as:

$$\Delta P_{T,R}(U_{RMS}, P_{OUT}, N, t) = R_{DSon,R}(Tj).\frac{1}{T}\int_0^T i_{T,R}(U_{RMS}, P_{OUT}, N, t)^2.dt \qquad (57)$$

$R_{DSon,R}$ for device IPP60R022S7 can be characterized as:

$$R_{DSon,R}(Tj) = 0{,}020 + 0{,}027.\frac{(Tj-25)}{125} \qquad (58)$$

7.5 Additional losses

GaN power stage is assembled on insulated metal substrate board with optimized thermal performance – distance between copper of switch node to ground plane is minimized to 150µm. Measured capacitance between switch node and ground plane without parts assembled is $C_{PCB} = 149pF$ ($C_{PCB,IMS} = 57$pF), which corresponds with constant power losses:

$$\Delta P_{C,PCB} = f_{sw}.C_{PCB}.U_{bulk}{}^2 = 1.47W \tag{59}$$

Thickness of PCB copper layers together with solder joints and connections between main board and IMS board create parasitic resistance, which was by measurement defined to $R_{PCB} = 22.3\ m\Omega$, which correspond with additional conduction losses:

$$\Delta P_{R,PCB}(U_{RMS}, P_{OUT}, N) = R_{PCB}.\Delta I_{L,RMS}(U_{RMS}, P_{OUT}, N)^2 \tag{60}$$

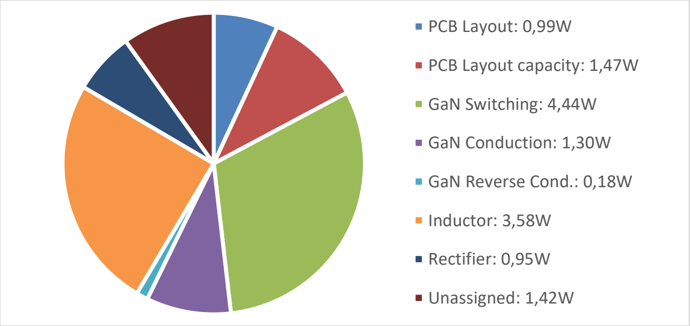


Fig. 54: Power losses distribution at nominal operating conditions

From losses distribution it is obvious, that even with GaN devices used the switching losses are still dominating. As in hard switching converts the losses are linearly dependent on operating switching frequency, further increase will lead only to lower efficiency, which is confirmed by measured data in Fig. 88. Therefore, it is the choice of operating switching frequency always to compromise between efficiency and required power density (W/inch3).

7.6 Control loop design

Nowadays trend in the power converters, starting from few kilowatts, is a digital control – calculating control loop in the software programmed typically into Digital Signal Processor (DSP) or Field Programmable gate array (FPGA) in connection with system control microcontroller.

This concept gives several major advantages. Any changes in the control loop do not require printed circuit board modification or any hardware changes, once the signal is sampled in good quality, possibilities are practically unlimited. At the same time noise sensitivity is reduced in the same way as the complexity of the hardware – higher integration of control circuit = cost reduction is possible. One of the key advantages used by many engineers worldwide is possibility to fix existing issue in the field without physical intervention to the hardware. By “bootloading” new firmware, issues related to operation of the converter or state machine, might be fixed globally. Usually, system powered by multiple kilowatt power supply is connected to world wide web – downloading and updating to the new version is possible in any part of the world.

For designed power converter, the newest (at this time) and cost optimized 32-bit floating point DSP from Texas Instruments TMS320F280041 is selected. Though, similar DSP can be found in portfolio of NXP (Freescale) or ST Micro.

As manufacturing processes of silicon chips are evolving very quickly, specific arithmetic-logical functions are not anymore significant cost contributor to the total price of the device. Therefore, DSPs capable to calculate with floating point numbers known as a luxury solution in the past, are becoming a standard nowadays. This makes control loop calculations design much easier, as voltages/currents can be represented in the floating-point numbers directly and all calculations are straight forward and easy to code in the software. Debugging time is reduced, as typical bugs as overflow of number caused by multiplication of two integers, or multiplication of mixed types (int, unsigned int) well known from fixed point cores are forever avoided.
Applications which require high calculation power, can use Control Law Accelerator (CLA), which is practically second core with limited access to the hardware. To maximize its performance, it is beneficial to execute the program written in assembly. With this feature, calculation of control loop within few microseconds is possible, independent from program in the "main" core – for example, control loop for Totem Pole PFC designed in this chapter, can be calculated two times over switching period – sampling at rising and falling edge of the current. Therefore, thanks to fast control loop calculation using powerful DSP feature, converter can be operated with minimized inductance.

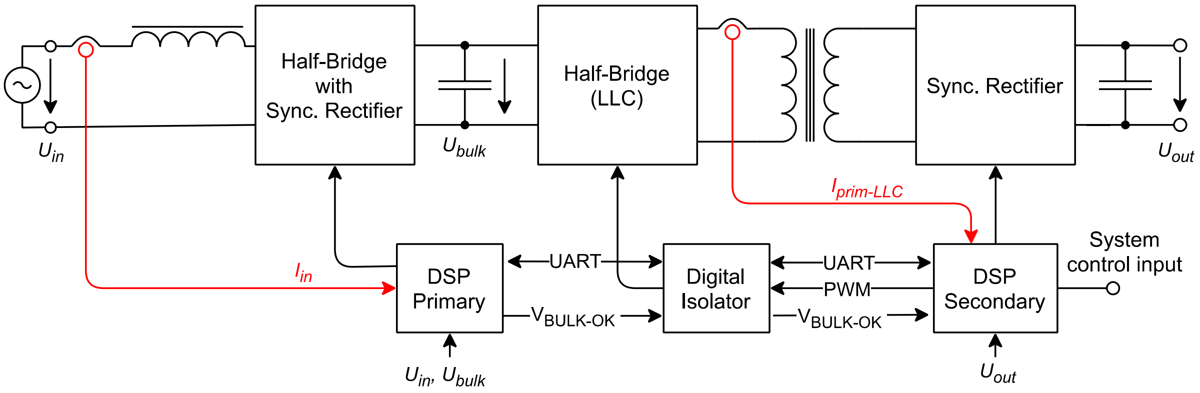


Fig. 55: Block diagram of digitally controlled power converter with galvanic isolation

DSP typically combines powerful core (with CLA) able to run program written by the user with several specific hardware peripherals, optimized for power electronics. In the latest generation of DSPs, advanced pulse width modulation (PWM) module can be combined with fast, integrated analog comparators with variable internal reference. Therefore, some of the functions to control power stage are executable only by correct configuration of the hardware peripherals, without high calculation power required.

7.6.1 Transition mode power factor correction

Boost converter (Totem-pole PFC) can be operated in several ways, the “classic” one – continuous conduction mode is used for converter designed in this thesis. Although, the possibilities of control in discontinuous mode are part of the research work conducted, with results shown in following lines.

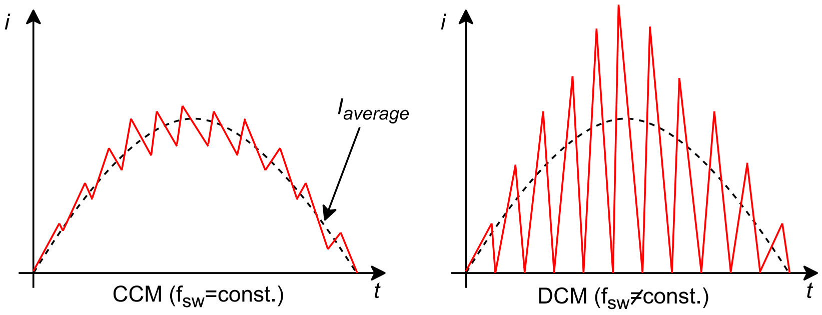


Fig. 56: Comparison of PFC inductor current in CCM and DCM mode of operation

In transition mode, current over the inductor reaches zero in every switching cycle. This operating mode is in terms of control circuit design challenging, especially for converters operating at high switching frequency (>1MHz) where minimization of magnetics together with efficient switching of GaN semiconductors might lead to maximization of power density of the power converter.

For this purpose, possibilities of latest DSPs generation (F28004x series) were explored. As the DSP is equipped with the set of fast analog comparators with 12bit variable reference, able to act within 20ns and PWM modulator block with resolution of 10ns (at 100MHz clock). Therefore, combining these two blocks together with dead time generation block inside the DSP gives hardware ready for operation in fast hysteresis mode capable of switching frequency up to 1.5MHz including period synchronization/reset, without significant calculation power needed. Program updates values of DACH and DACL registers for comparator block references values, to achieve sinusoidal waveform of input current. Hysteresis mode of control gives additional reliability in case of line voltage transients, as the fast reaction to input current is fundamental for each operating cycle. Principles of settings are displayed in Fig. 57, example code describing extensive configuration of DSP hardware modules can be found in the appendices.

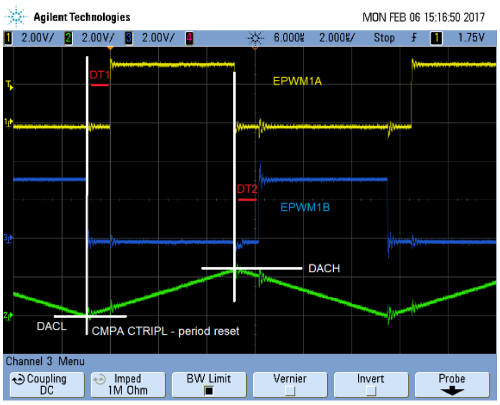


Fig. 57: Scope snapshot of DSP in/out signals configured for DCM mode

Significant disadvantage of critical conduction mode is size of the input filter, to meet electromagnetic compatibility standards. Power density of the total solution is therefore the same as in continuous conduction mode.

7.6.2 Control loop of Totem Pole Converter

Control algorithm of the power stage designed in this chapter consists of voltage and current regulator in cascade configuration. Complete block diagram is displayed in Fig. 61, and it is explained block by block in this chapter.

Control loop program starts with grabbing samples of input quantities – converter input voltage, bulk voltage and input current. Analog to digital (A/D) conversion for following samples is triggered exactly at the middle of the on time of high side switch, which is configured by PWM hardware module. As the DSP has 3 separated A/D converters with independent sample and hold circuits, samples can be taken simultaneously. Offset is subtracted from taken sample and multiplied by gain, numeric results are directly in the unit of sampled quantity:

$$sampled\ quantity = (ADCresult - offset).gain\ [sampled\ quantity\ units] \tag{61}$$

Two A/D channels A&B are used for simultaneous, periodic sampling of voltages and current (by f_{sw}), third channel is used for “slow” measurements, such a temperature from the sensors or bias voltages. Round robin priority management of TI devices provides possibility to use single channel for multiple triggers with different priority, from practical experience this usually results in increased sample noise.

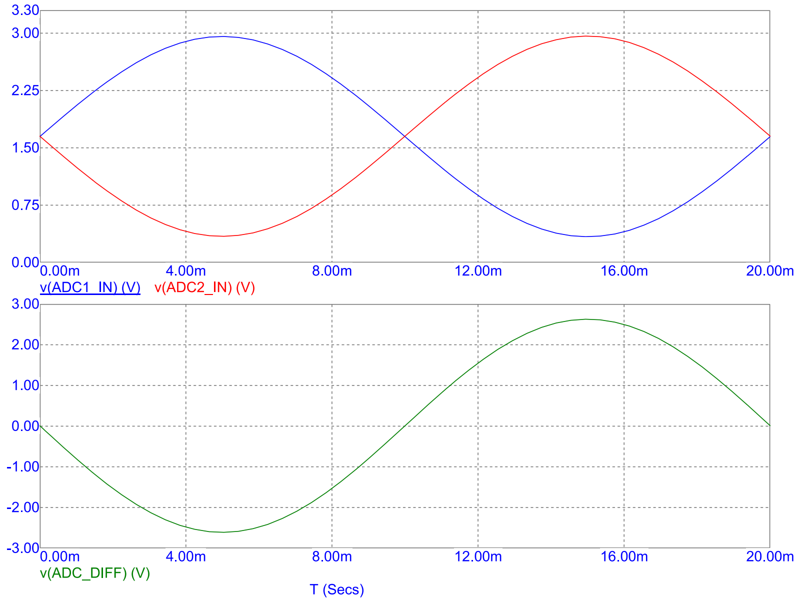


Fig. 58: A/D resolution increase by simultaneous sampling of two channels

Simultaneous sampling of input current is critical for precision - as described later in this thesis, HW circuit is designed in a way to double the resolution of sampled value by inverting one of the channels. Therefore, any delay in the sampling between two channels introduces error, caused by noise and common mode currents in the circuit. Error introduced by passive components in operational amplifier feedback circuit needs to be eliminated by calibration for both polarities of input current after manufacturing process – any inequality in gains can result in DC offset – which will be reflected over control loop to real input current during operation. With simultaneous sampling of two channels, input current is calculated as:

$$iin = ((ADCresult_A - ADCresult_B) - offset).gain \tag{62}$$

Waveforms of voltages on the inputs of microcontroller, representing current, are in Fig. 58.

Rms value of the input voltage is calculated by collecting samples over half-period of the line voltage – by zero crossing detection, square of the sum is calculated and *vin_rms* is updated.

$$vin\_rms = \sqrt{\frac{1}{N}\sum_{0}^{N} vin\_sample^2} \tag{63}$$

Cascaded structure of regulators requires several “tweaks”, to achieve fast response in case of line voltage transients or load steps from converter transferring power to secondary side. As the load steps on the output of server power supply can be above 50% of total converter power and are unpredictable, feedforward carrying information about output power (*pout_sec*) is transferred between primary and secondary control loop. Data are transferred via internal communication bus with high baud rate (>500kbps) - in this case by asynchronous serial line isolated with digital isolator with high CMTI.

$$irms\_ff = \frac{pout\_sec}{vin\_rms} \tag{64}$$

Obtaining nearly immediate information about load of the converter gives several advantages for fast control – calculated RMS current using input rms voltage can be directly added to the output of the voltage controller. Thanks to feedforward is operation around “0” achieved and integral part of the voltage controller is compensating only differences caused by readback tolerances and efficiency of the PFC power stage. Therefore, step response performance is defined only by the current loop bandwidth.

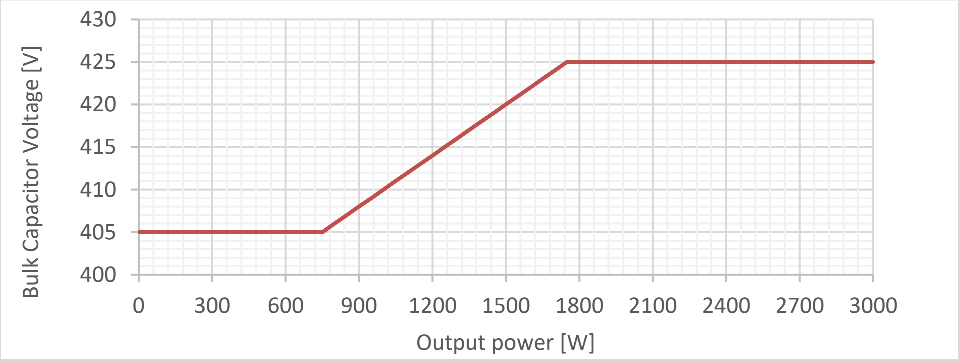


Fig. 59: Adaptive bulk capacitor voltage curve

To optimize the light load efficiency in order to achieve 80+ Titanium rating, bulk voltage needs to be reduced to minimize switching losses in the power stage. On the other hand, hold-up time of power supply load needs to be the same over loading conditions to guarantee safe shutdown of server equipment connected to DC/DC stage output. Hold-up time is defined by formula:

$$t_{hold-up} = C_{BULK}.\frac{\eta.({U_{BULK}}^2 - {U_{REG,min}}^2)}{P_{out}} \tag{65}$$

Therefore, to fulfil both requirements, reference of the voltage controller is adaptive and based on output power of the power stage according to graph displayed in Fig. 59.

Typical analogue design of PFC output voltage controller has bandwidth significantly below 100Hz – reason is the bulk voltage ripple, which needs to be suppressed to avoid disturbance of reference for the current regulator – affecting THD of input current. One way how to solve this problem in digital controller is to create estimator of bulk voltage capacitor and subtract estimated voltage from the regulation error.

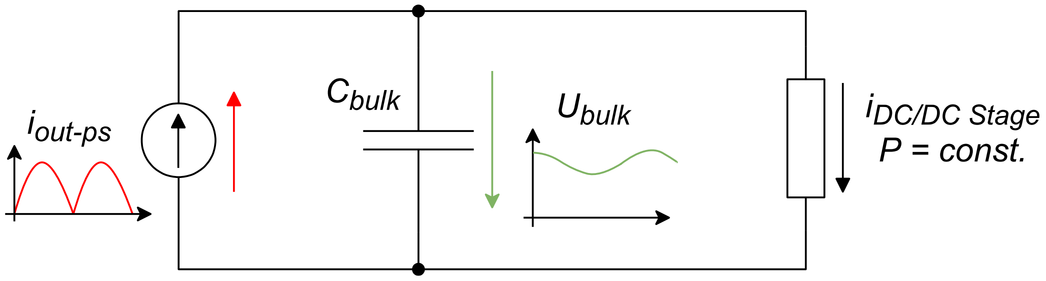


Fig. 60: Equivalent schematic of bulk voltage ripple estimator

Using information about secondary converter power, power stage current can be calculated:

$$iout\_ps = \frac{pout\_sec}{vout\_adc} \tag{66}$$

Based on equivalent circuit displayed in figure above, bulk capacitor ripple voltage can be calculated:

$$vbulk_{ff} = \frac{iout\_ps}{2.\pi.C_{bulk}.f_{in}}.\cos(\varphi) \tag{67}$$

As the bulk voltage correction, power feedforward is not enough to cover certain situations, hiccup protection needs to be implemented as a last instance to prevent overvoltage on the bulk capacitor. Hiccup protection is a fast comparator with hysteresis permanently monitoring bulk capacitor voltage, stopping the PWM pulses above defined threshold. Independent hardware overvoltage circuit able to shut down PWM signals as a redundant protection is required as per safety standards, as bulk capacitor (820µF/450V) is component with risk of fire and explosion.

On top of the control loop is operating software state machine, controlling inrush relay, under- and over- voltage and managing startup and shut down of a power stage with cooperation of control loop of DC/DC converter transferring power to secondary side over the transformer. With control algorithm implementation described in this chapter, control of 3kW totem pole PFC is possible in compliance with Network Equipment Building System (NEBS) standard (specifying dropouts, surge and distortion). Performance of the control loop can be seen on oscilloscope plots in the chapter Design verification.

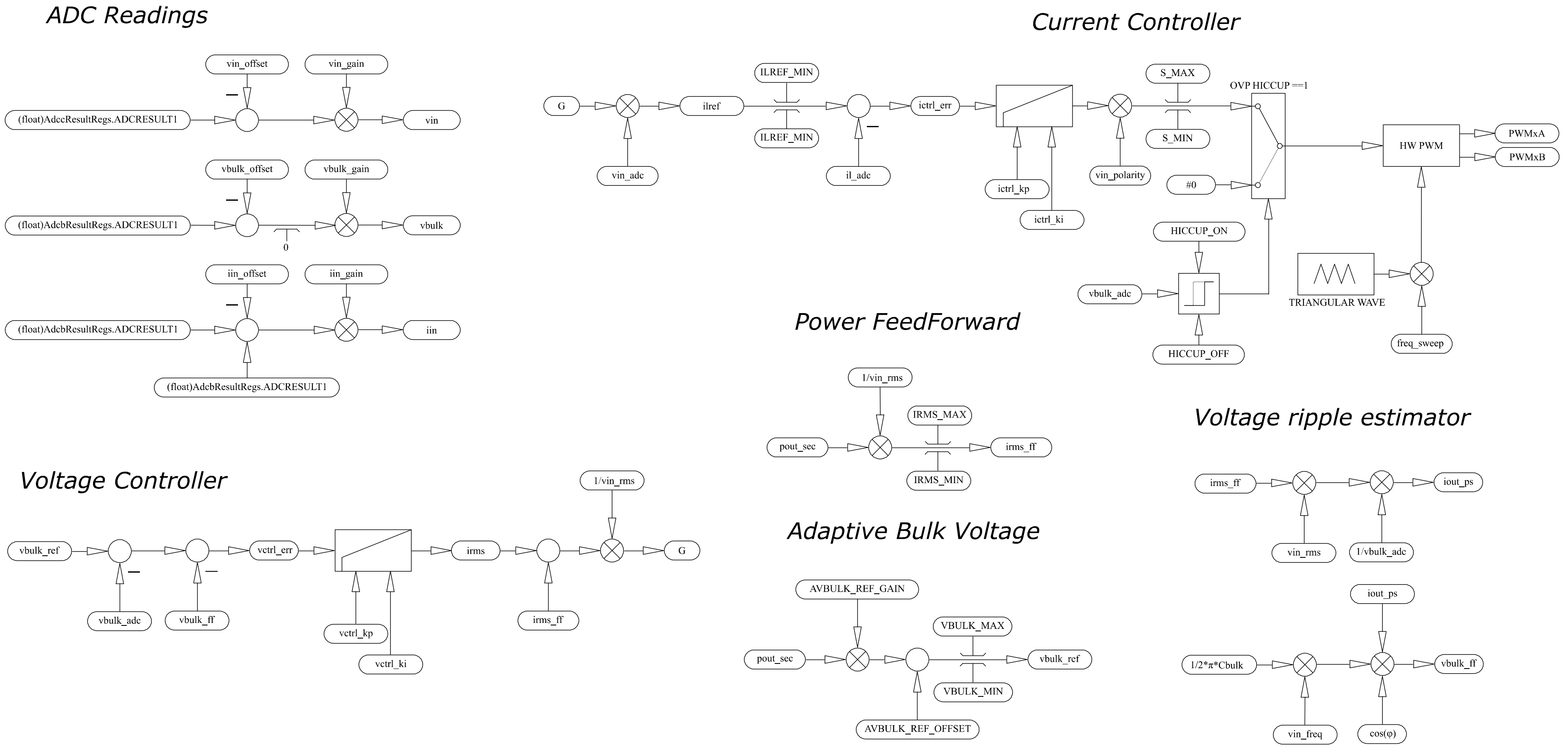


Fig. 61: Totem Pole PFC Control loop block diagram

7.6.3 Debug tool for digitally controlled systems

Debugging issues in digitally controlled power systems might be a big challenge for hardware electrical engineer, as measuring something inside the DSP is not directly possible. While verification of sampled value, tuning the control loop or simply detecting the root cause of the issue might be the daily business.

As the dealing with digital control is a base of this thesis, tool to display “variables” on the oscilloscope screen was designed by author in free PCB design tool KiCad - design files together with STL file for 3D printed box are public and available in the appendices.

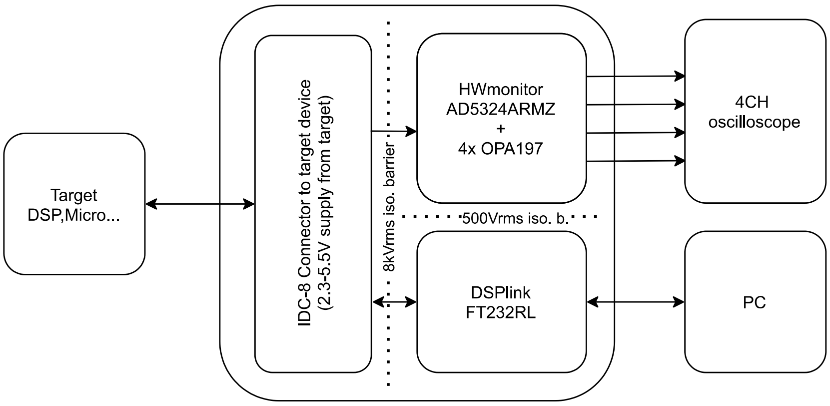


Fig. 62: Block diagram of debug tool for digitally controlled systems

Heart of the debug tool is four channel buffered analogue to digital converter AD5324ARMZ from Analog Devices, controlled over serial peripheral interface with clock rate up to 30MHz. As the bandwidth of the analogue part of D/A converter together with operational amplifiers used for post processing of the signal is 200kHz, most of the signals related to control of the converter can be displayed in “real-time” on oscilloscope screen. Delay to real value processed by control loop can be within micro-second, dependent mainly on communication speed and the software design.

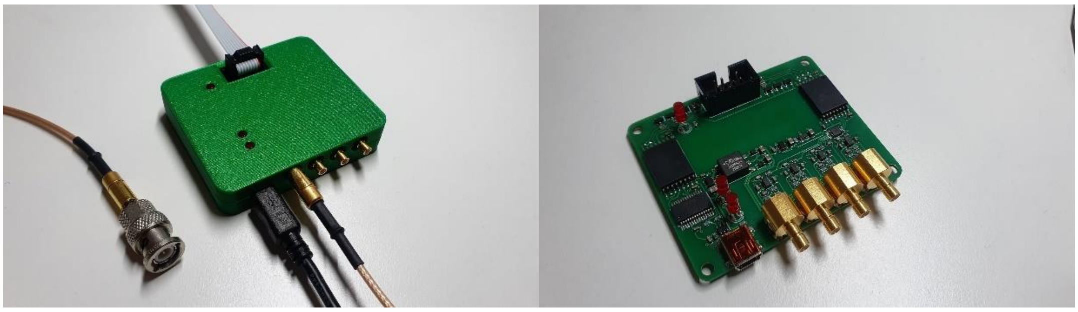


Fig. 63: Picture of debug tool prototype

All signals between debug target, oscilloscope, DSP are galvanically isolated with high-speed digital isolators. In addition, one serial interface (COM port) is available to allow user to read/write variables inside program by using MAP file (contains addresses and type information for each public variable) – or simply to change address of variable to be “send out”.

7.7 Current sense technique

Cost effective, reliable and space effective current sense circuit with sufficient bandwidth for regulation is a challenge. In practical power electronics there are three ways, how to measure switching converter current:

1.) Shunt resistor
2.) Sensing of magnetic field – hall effect sensors (open/closed loop)
3.) Current transformer

In the designed Totem pole converter, sensing of the current through the inductor needs to be galvanically isolated, as control circuits (DSP) are referenced to negative pole of bulk capacitor. While bandwidth of the sensor needs to be high (BW>500kHz) to achieve fast current regulation loop response in critical events such a surge or input voltage dropouts.

Using shunt resistor in this application might be feasible only with isolated operational amplifier (e.g., TI AMC1200), which requires isolated power and shunt with certain power losses (~2.5W for 150mV signal, at low line operation). Shunt power loss is not negligible comparing to converter output power, especially in case of optimization for highest efficiency. Due to input voltage range of isolating amplifiers (standard +/- 250mV), to gain sufficient signal to noise ratio resistor ohmic value must be on higher side. In addition, bandwidth and noise immunity (typ. CMTI < 10kV/µs) of this solution is not extraordinary and might be a limiting factor. Required PCB space is not negligible, which is another obstacle for high power density power converters (if the cooling of the shunt is considered).

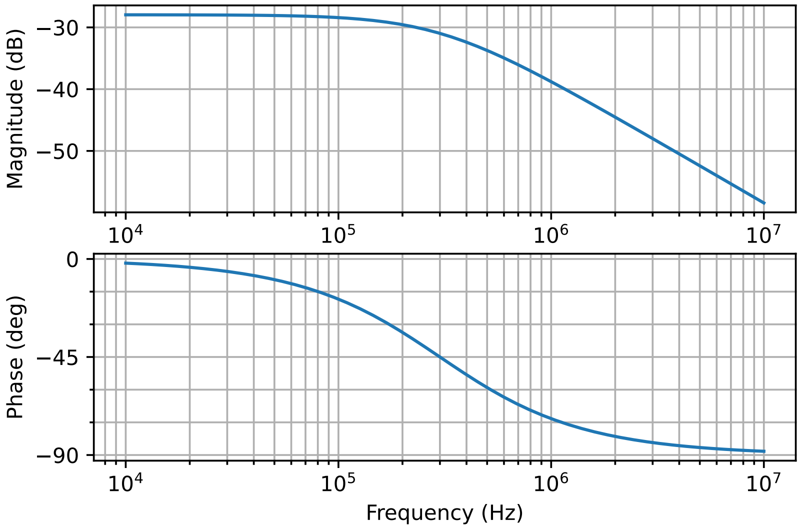


Fig. 64. Amplitude and phase characteristic of hall effect sensor (approximated)

Leading manufacturers of hall effect current sensors nowadays are Allegro Microsystems, Sensitec and well-known Swiss company LEM. Nowadays available high-end devices designed for integration in printed circuit board are capable of bandwidth above 400kHz (e.g., ACS37002) with acceptable phase shift.

Unfortunately, pressure for cost in power supply business (typ. 5c$/W) is not allowing its usage – choice falls to lower performance devices. Popular device for mid-range power converters is cost optimized open loop sensor LEM GO-20 SMS, integrated in small SO-8 package for surface mount assembly. Sensor provides bandwidth typ. 300kHz (@-3dB), with certain transport delay.

LEM GO-20 SMS Sensor behavior can be approximated as low pass filter with BW of the sensor - displayed in Fig. 64. From practical measurement it is clear that the phase shift varies over frequency range, however the manufacturer is unfortunately not providing exact phase shift curve versus frequency in the datasheet. Transfer function of hall current sensor:

$$F_{HALL}(p) = \frac{I_{SNS}(p)}{V_{SNS,hall}(p)} = \frac{V_{Gain}}{\frac{1}{2.\pi.BW}p + 1} \tag{68}$$

Where voltage gain V_{Gain} (0.04V/A) and Bandwidth of the sensor BW (300kHz) are stated in manufacturers datasheet.

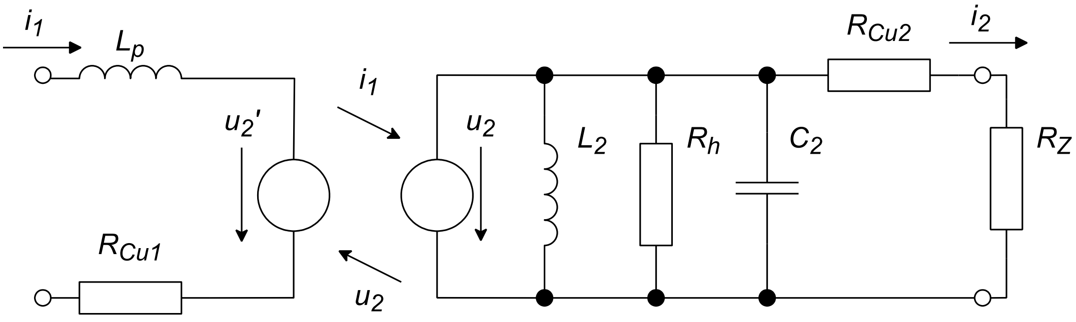


Fig. 65. Equivalent circuit of current transformer, [11]

Third option is a current transformer. Equivalent schematic of the current transformer consists from the high pass filter created by magnetizing inductor and low pass filter defined by parasitic capacitance of winding and its resistance. Therefore, transformer is capable to operate only with alternating signals above certain frequency. For lower frequencies the magnetizing current is significant in comparison to current flowing over resistive load, measurement error is high, core is reaching saturation. For small current transformers the capacitance between windings is relatively small, therefore achievable frequency bandwidth might be over 1MHz.

Transfer function of current transformer, defined from substitute circuit diagram:

$$F_{ICT}(p) = \frac{I_{prim}(p)}{V_{SNS}(p)} = \frac{L_2.p}{L_2.C_2.p^2 + \frac{L_2}{R_z}.p + 1}.\frac{N_1}{N_2} \tag{69}$$

Where is L_2 magnetizing inductance, R_z represents load resistor and is C_2 interwinding capacitance. Primary N_1 and secondary N_2 winding turns.

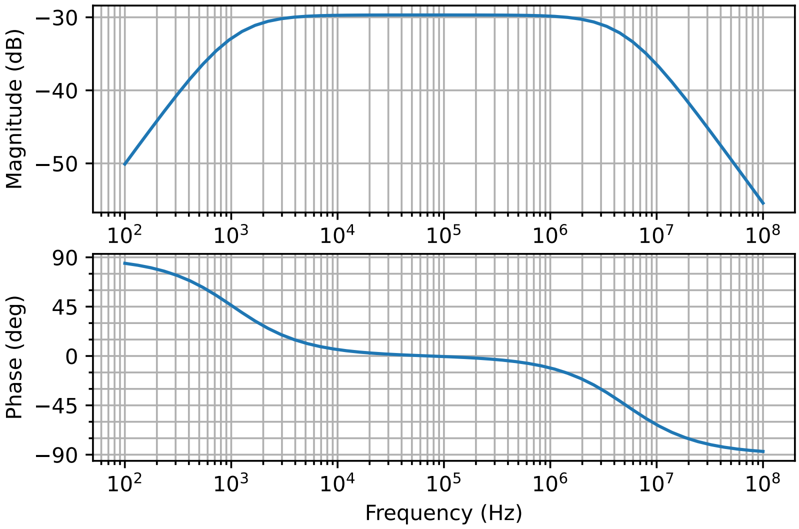


Fig. 66. Amplitude and phase characteristic of current transformer

Aim of this chapter is to present high performance current sense circuit solution, using well known principles briefly described in previous lines. By merging behavior of open loop hall effect sensor and current transformer in suitable way, galvanically isolated sensor capable of measuring DC current (0Hz) and AC current up to 1MHz is created, which gives a key advantage for regulation loop of designed totem pole converter. In other words, “slow” sinusoidal waveform of regulated line current is measured by precise hall effect sensor and “fast” ripple current is superimposed on top of it by current transformer.

As the transformer is operating with high “DC” bias in this application, gaped toroid solution is needed to avoid saturation of the core. In principle, introducing air gap in the current transformer does not make sense as the reduction of magnetizing inductance is leading to increased error of the measurement. As the minimized solution is a target, in this special case the air gap is needed to decrease magnetic flux in the small toroid core. Current transformer in build prototype has one primary turn and 94 secondary turns.

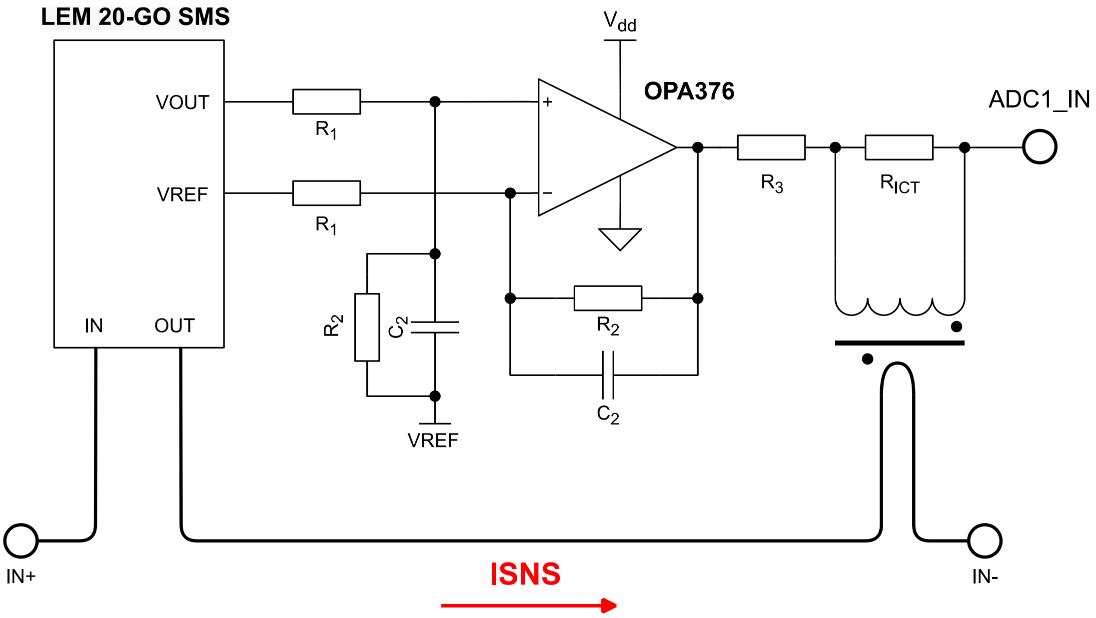


Fig. 67. Simplified schematic of designed current sensor

Merging analogue outputs of two independent sensors is possible with operational amplifier shown in the schematic above. Root of the operation is the same “gain” from both inputs. Product of shunt resistor and current transformer output current must give the same voltage as output of hall effect sensor amplified by operational amplifier. As majority of microcontrollers are equipped with 12bit A/D converters, is required to invert gathered signal and increase the precision of current information by using two A/D channels in simultaneous sampling mode (see details in control loop block diagram). By slightly slowing down hall current sensor with filter capacitor in feedback loop of operational amplifier, perfect match of transfer functions is achieved, resulting in step response representing real current with minimum transfer delay and high bandwidth.

Transfer function of differential operational amplifier:

$$F_{OpAmp}(p) = \frac{V_{SNS,hall}(p)}{V_{SNS,gained}(p)} = \frac{\frac{R_2}{R_1}}{R_2.C_2.p+1} \tag{70}$$

For schematic in Fig. 67, transfer function representing complete current sensor path can be created by merging all previously defined elements:

$$F_{ISNS}(p) = F_{HALL}(p).OpAmp(p).F_{ICT}(p) \tag{71}$$

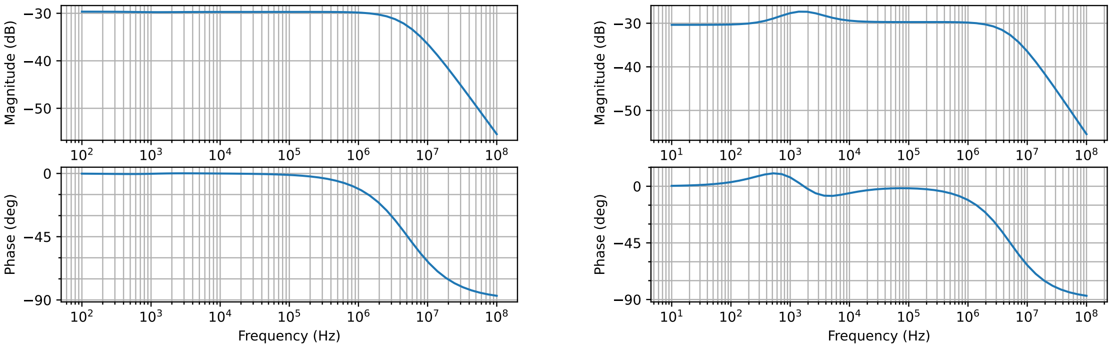


Fig. 68. Amplitude and phase characteristic of designed current sensor using merged outputs of two measurement methods, simulated tolerance of the feedback components (right)

Usage of precision component with tight tolerance is recommended, as any detuning in speed/gain of operational amplifier will lead into difference between measured current and output of the merged sensors, which might disturb operation of current regulator by incorrect interpretation of real value of the current through power inductor. Difference is well visible on transfer function and step response – simulated deviation in the feedback capacitor C_2 value using Python (Pyplot and Control module).

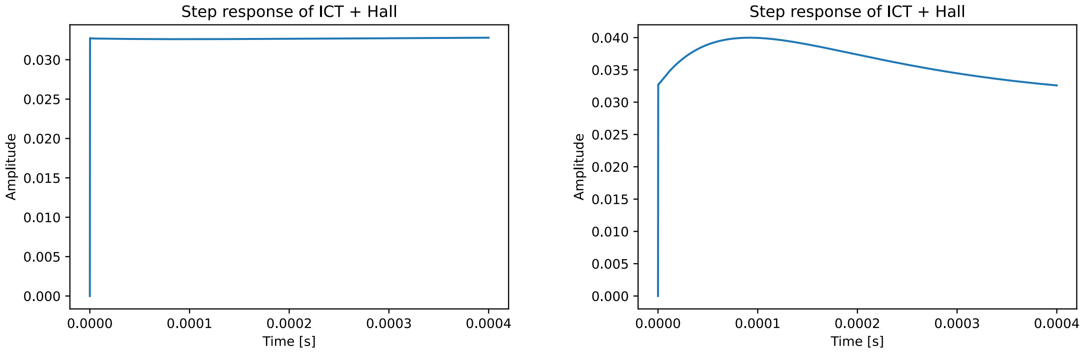


Fig. 69. Step response of designed current sensor using merged outputs of two measurement methods, simulated tolerance of the feedback components (right)

By using surface mount packages a complete circuit can be designed on approximately 2cm^2, significant percentage of the space is taken by restricted areas for THT wave soldering. Further optimization by placing hall effect sensor on opposite side leads to a current transfer trough the PCB over vias, which might affect hall current sensor operation by elevated temperature and field distortion. According to manufacturer’s documentation, offset and reference voltage are temperature dependent – too high swing in sensor ambient temperature might lead to offset of measured current – DC part in PFC input current might be present in certain conditions.

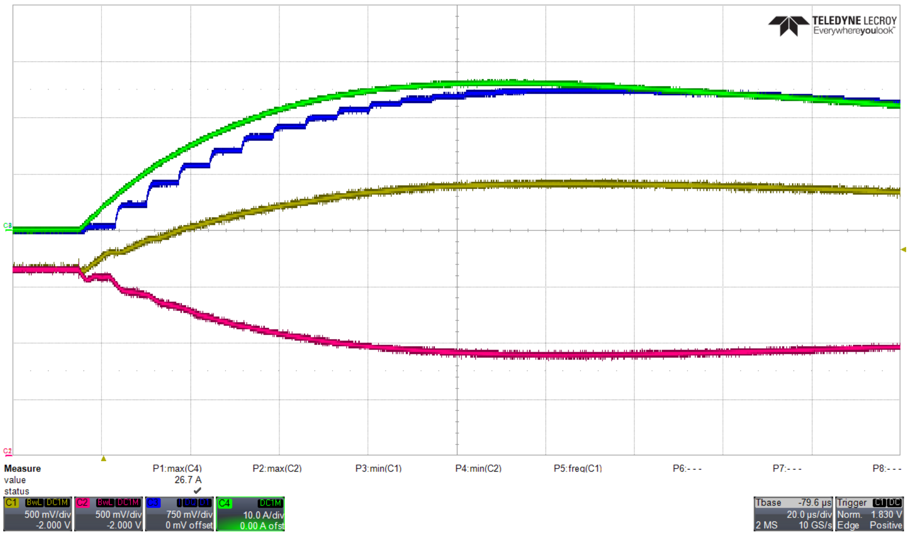


Fig. 70: Operation of the current sensor prototype (DC current step), measured current (Green), Output of operational amplifier - positive (Yellow), Output of operational amplifier - negative (Red), Digitalized current measured by DSP (Blue), timebase 20µs/div

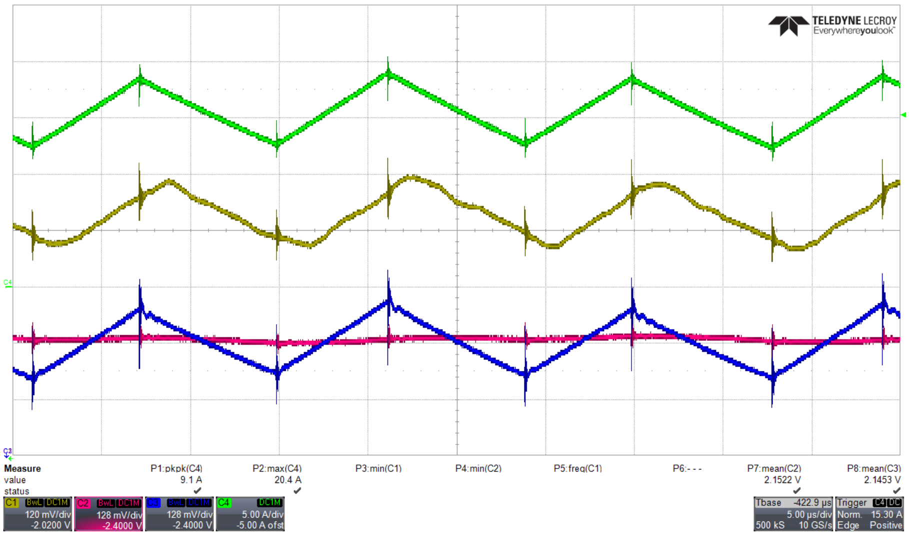


Fig. 71: Operation of the current sensor with GaN PFC converter (Blue), current measured with 50MHz current probe (Green), Output of operational amplifier (Red), Output of Hall effect sensor (Yellow), timebase 5µs/div

Fig. 70 show function of the designed current sensor together with inverted channel by operational amplifier, especially show the “sampled” current seen by the DSP. Current measured by DSP is visualized using SPI debug tool described in Chapter 7. Delay and steps visible on the waveform are caused by approximately 10µs update rate, which is the same as update rate of control loop calculation. *Fig. 71* show sensor in operation with designed totem pole GaN PFC converter, phase shift and distortion of cheap hall effect sensor signal is present – merged solution with current transformer provides signal with high quality (input of A/D converter - blue curve).

Biggest benefits of the presented solution are low space requirements and good cost/performance ratio allowing precise operation of power converter in low-cost product. Low power loss operation gives significant advantage to overall efficiency optimization of the converter.

7.8 Design verification

After characterization of all power losses, verification of voltage and current rating of all components, verification of cooling concept by FEM simulation and finalization of schematic for control circuits and main board, design can proceed to phase of printed circuit board design and assembling of the prototype. Before powering up of the assembled unit, all supply voltages and signals are verified. Verification of voltage and current measurement circuit by data readout over communication from DSP, testing the hardware overvoltage protection circuit and its interaction with gate driver circuit are essential for safety while powering up the converter operating with high voltage.

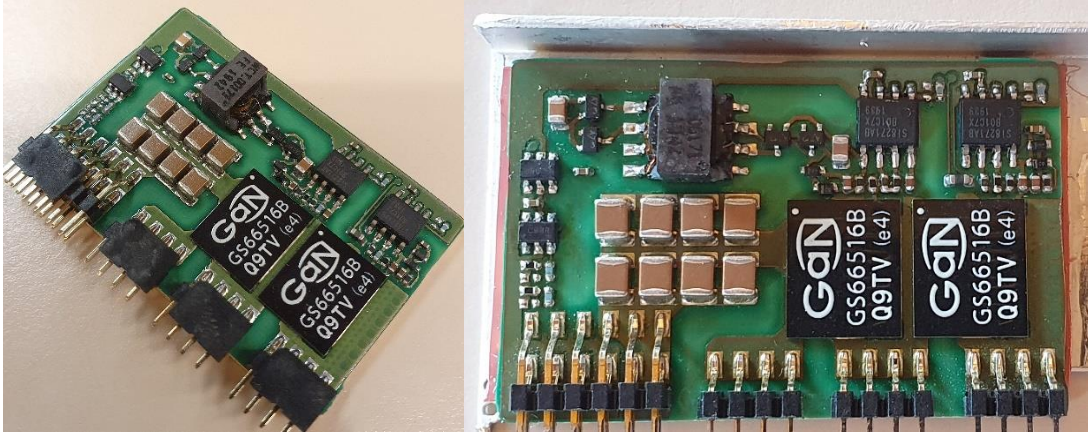


Fig. 72: Tested prototype – Insulated metal substrate board with GaN (GS66516B) half-bridge and insulated gate drivers after SMT assembly (left), assembled to the aluminum heatsink (right)

Single side insulated metal substrate board assembled with GaN Half Bridge and isolated gate driver is assembled on aluminium heatsink. Finished sub-board is therefore assembled into “mainboard”, which is 6-layer PCB providing connection between rest of the power components, such as inductor, bulk capacitor, EMC filter and the second power stage of the power supply – resonant converter (known also as LLC) providing 12VDC output voltage.

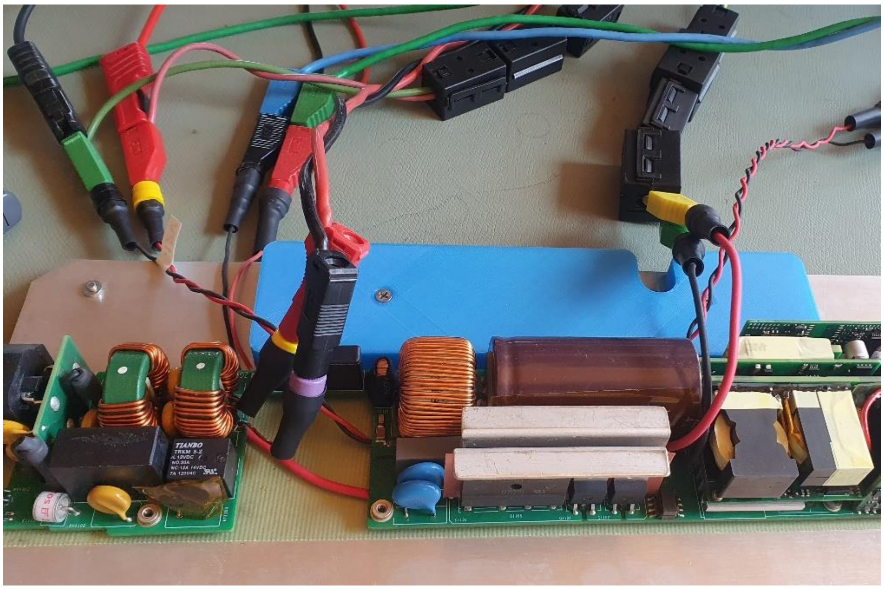


Fig. 73: Tested prototype – Efficiency measurement test setup

Synchronous rectifier is attached on the same heatsink profile as GaN board and is visible in Fig. 83. Aluminium heatsink is simple L shape, which might look insufficient for calculated power losses – as the power density is high priority in case of this power supply form factor, cooling is managed by high power FAN, providing strong airflow (~5ms^{-1}). Together with efficient heat transfer from cooled devices to heatsink the maximum temperature is not exceeding safety certification ratings. For reasons mentioned in second chapter of this thesis, GaN transistors gate driving circuit is designed to operate with negative voltage in off-state. Operation of the gate drive is displayed on scope picture below (Fig. 74). According to GS66516B specification, absolute maximum ratings of gate driving voltage (7V) are very close to the nominal rating (6V), VCC supply for the gate driver integrated circuit must be stabilized with linear regulator and properly decoupled with ceramic capacitors.

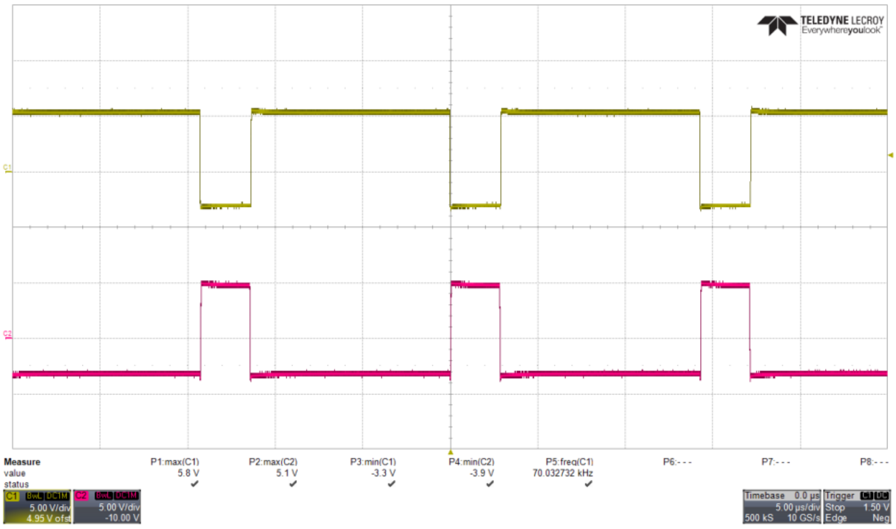


Fig. 74: Gate driving signal for High and Low side device in Half-Bridge at U_{DS}=0V, timebase 5µs/div

Powering up procedure of Totem Pole PFC is starting with DC voltage at the input terminals, which is necessary to safely connect oscilloscope to primary ground of bulk capacitor and monitor drain-source voltage of power switches during the operation.

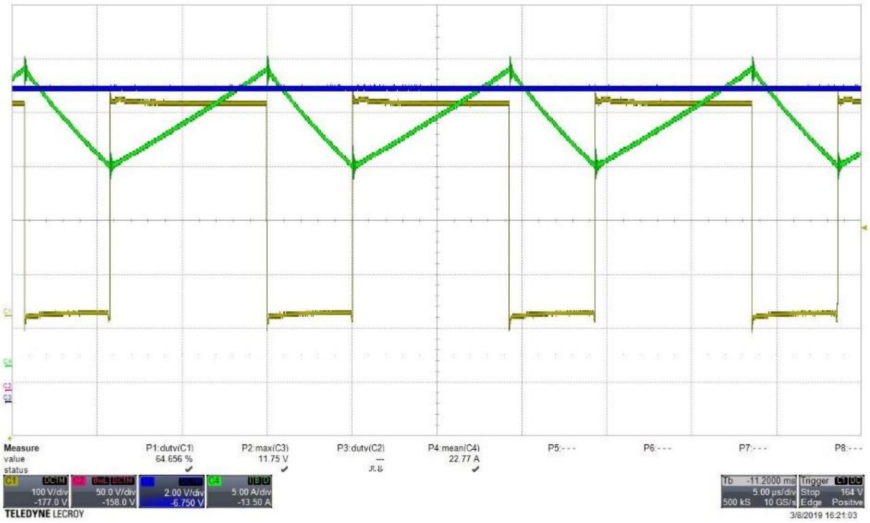


Fig. 75: Drain-Source voltage (Yellow) of GaN Half-Bridge at DC input voltage, green waveform is power stage current, timebase 5µs/div

As Totem-pole topology contains rectifier on its input, primary ground is "jumping" versus PE potential with 100Hz frequency and amplitude of Bulk voltage (405V). As the line transformer providing isolation for oscilloscope has high interwinding capacitance, connection of scope probes to ground of the bulk capacitor generates significant common mode currents during AC operation, disturbing measurement itself and might lead into malfunction of control circuits in power converter. Therefore, verification of converter operation with DC voltage (in both polarities) is more convenient.

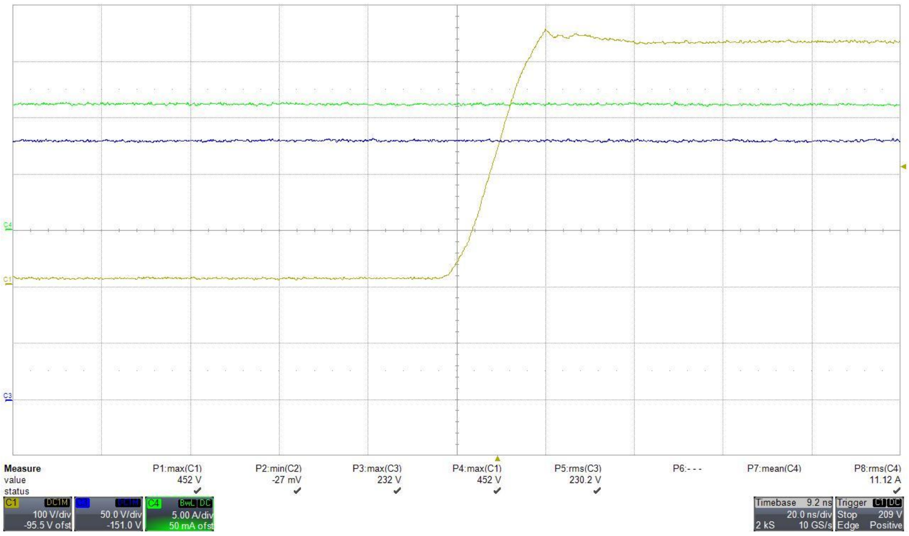


Fig. 76: Drain-Source voltage (Yellow) of GaN Half-Bridge at DC input voltage with detail on rising edge, green waveform is power stage current, timebase 20ns/div

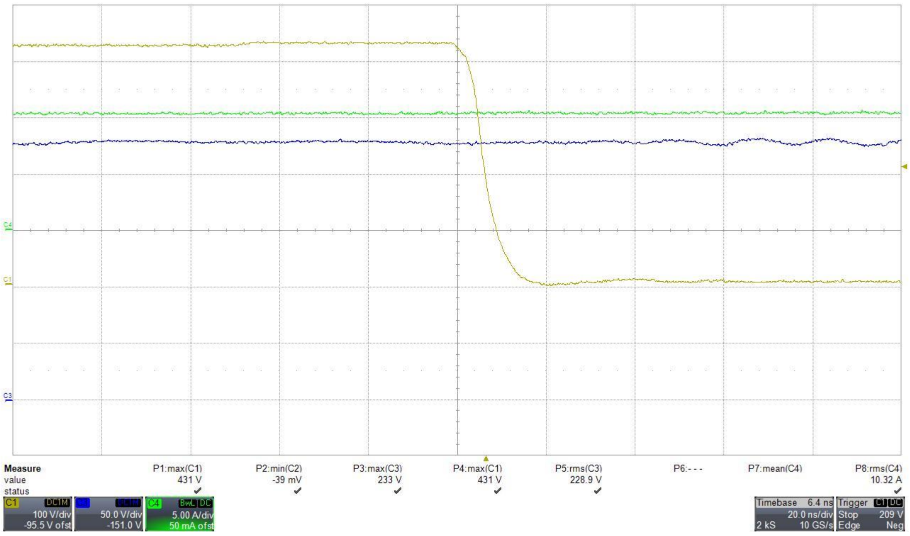
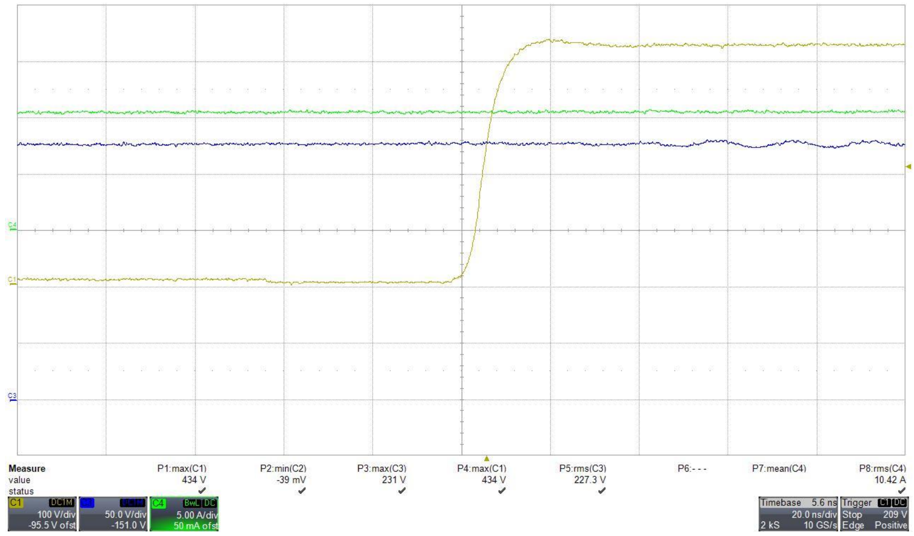


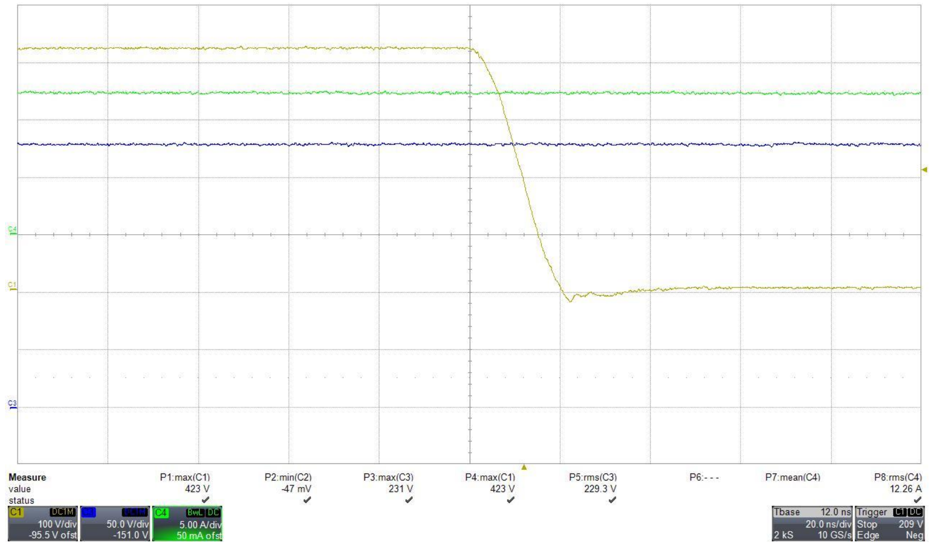
Fig. 77: Drain-Source voltage (Yellow) of GaN Half-Bridge at DC input voltage with detail on falling edge, green waveform is power stage current, timebase 20ns/div

Verification of drain-source voltage at maximum operating input current is critical for long term reliability. This step is at the same time verification of PCB layout, as any parasitic inductance introduced will cause oscillations on drain-source voltage. Construction of IMS with special vias down to metal makes connection to low impedance ceramic capacitors short, which is visible on the switching behavior (measured with Agilent 250MHz 100:1 passive probe).



Measure	P1:max(C1)	P2:min(C2)	P3:max(C3)	P4:max(C1)	P5:rms(C3)	P6:- - -	P7:mean(C4)	P8:rms(C4)
value	434 V	-39 mV	231 V	434 V	227.3 V			10.42 A
status	✓	✓	✓	✓	✓			✓

Fig. 78: Drain-Source voltage (Yellow) of GaN Half-Bridge at DC input voltage with detail on rising edge, green waveform is power stage current, timebase 20ns/div



Measure	P1:max(C1)	P2:min(C2)	P3:max(C3)	P4:max(C1)	P5:rms(C3)	P6:- - -	P7:mean(C4)	P8:rms(C4)
value	423 V	-47 mV	231 V	423 V	229.3 V			12.26 A
status	✓	✓	✓	✓	✓			✓

Fig. 79: Drain-Source voltage (Yellow) of GaN Half-Bridge at DC input voltage with detail on falling edge, green waveform is power stage current, timebase 20ns/div

In Fig. 76, Fig. 77, Fig. 78, Fig. 79 four detailed scope snapshots of rising and falling edge are displayed. First two waveforms are displaying operation with positive voltage/current on the input, second two pictures with reversed polarity of input voltage (simulation of AC operation). Reverse conduction of GaN MOSFET is clearly visible (Fig. 77, Fig. 78) for deadtime duration - 50ns (reverse voltage might be in this case around 7V).

Measurement of voltage overshoot on drain-source for all combinations is important, as current is circulating over different tracks on the printed circuit board – inequality in the parasitic components might be present.

Output (bulk) voltage regulator and current regulator might be tuned in DC operation as the transfer function of power stage is the same, if bulk capacitor voltage ripple rejection works properly. From the gained experience, by simulating power stage in analogue/digital circuit simulator (Python, PSpice, Microcap), the current/voltage regulator tuning might be avoided, as modelling of hard switching converter is exact and gives result well representing reality.

After verification of power stage and regulators operation, converter should be ready for operation with AC voltage. To ensure proper operation, two stage common mode filter is connected at the input of the converter. Oscilloscope snapshots showing AC operation of PFC converter at the minimum and nominal input voltage and maximum load are displayed below.

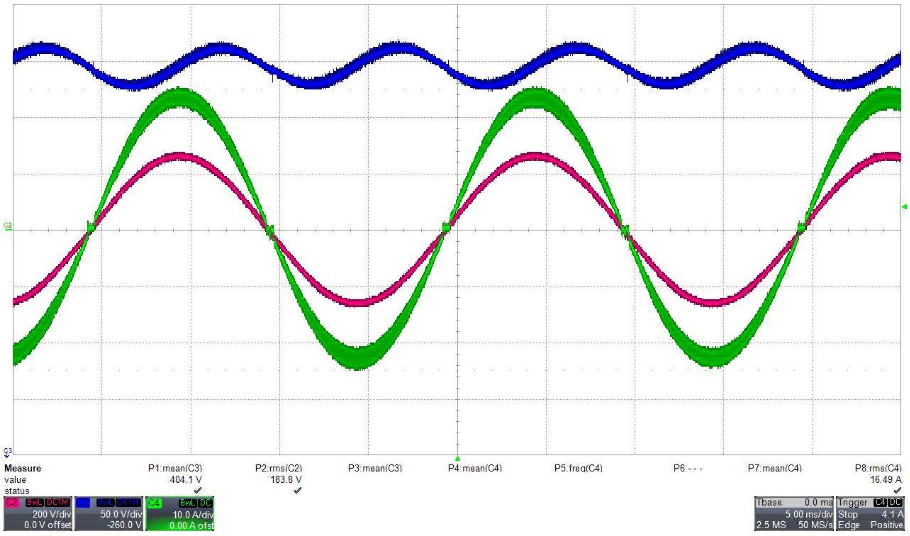


Fig. 80: Input voltage, bulk voltage and current waveform at 180VAC input voltage and 3kW output power (90kHz switching frequency), timebase 5ms/div

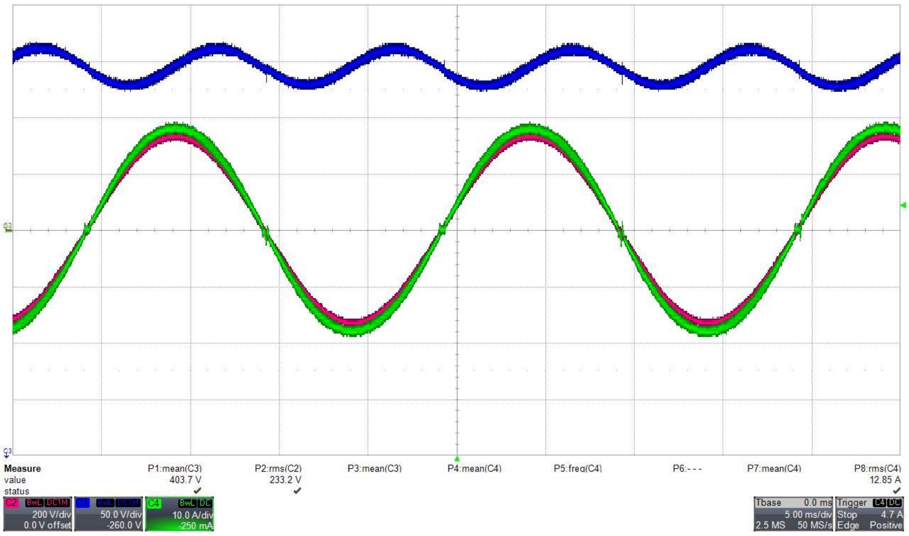


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Fig. 81: Input voltage, bulk voltage and current waveform at 230VAC input voltage and 3kW output power (90kHz switching frequency), timebase 5ms/div

Thermal camera snapshot below shows converter operation at minimum input voltage and full load 3kW, with improvised FAN cooling on the test bench. As the heatsinks are designed for high airflow in its surroundings, the measured temperatures are higher than one in the enclosure.

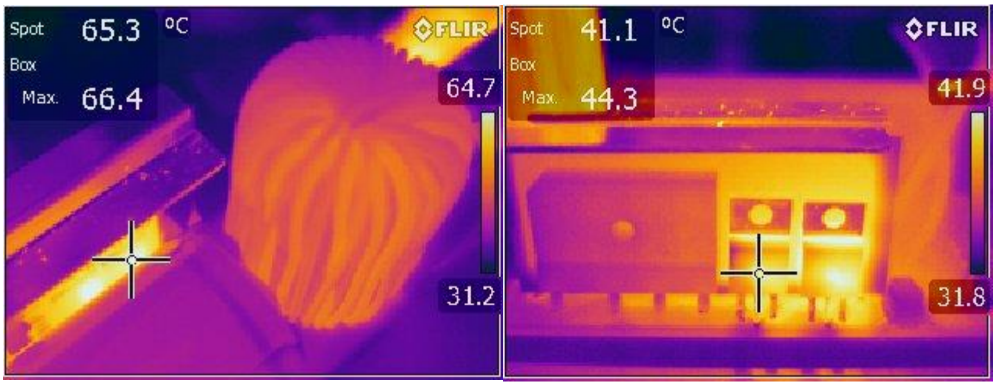


Fig. 82: Thermal camera picture of power stage during operation at full power 3kW – GaN half bridge on insulated metal substrate board (left), synchronous rectifiers (right)

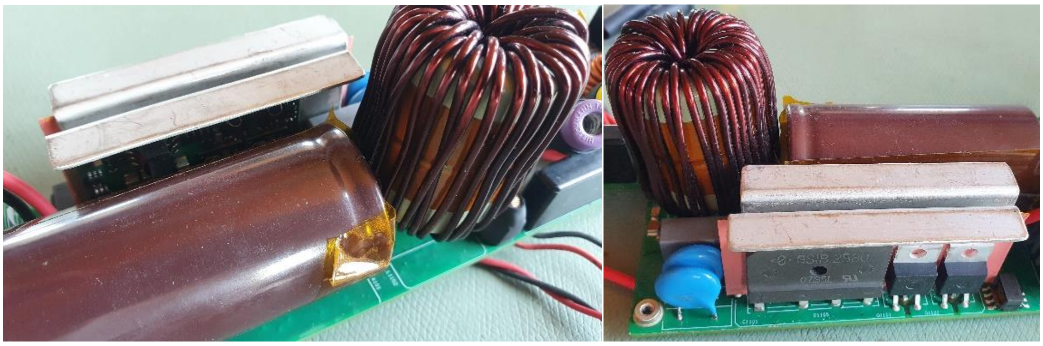


Fig. 83: Pictures of prototype with optimized inductor – reference for thermal camera picture

Proper verification of unit thermal performance is performed in thermal chamber with regulated ambient temperature. Temperature is measured by thermocouples attached to critical components in which power loses are concentrated.

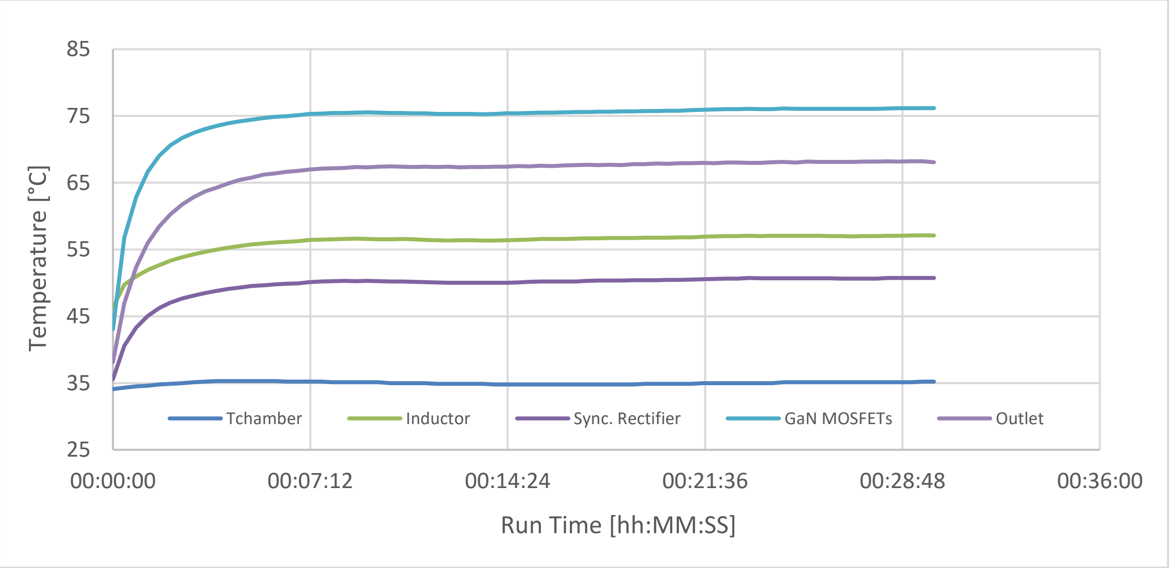


Fig. 84: Verification of thermal performance at corner operating conditions (180VAC,3kW)

Testing in the thermal chamber with elevated ambient temperature is a proper way to verify overtemperature protection. Results from testing of prototype equipped with thermal chamber are displayed in Fig. 84. As the cooling is performed by high airflow stream, time required to stabilize components temperature is relatively short (thermal time constant τ~100s).

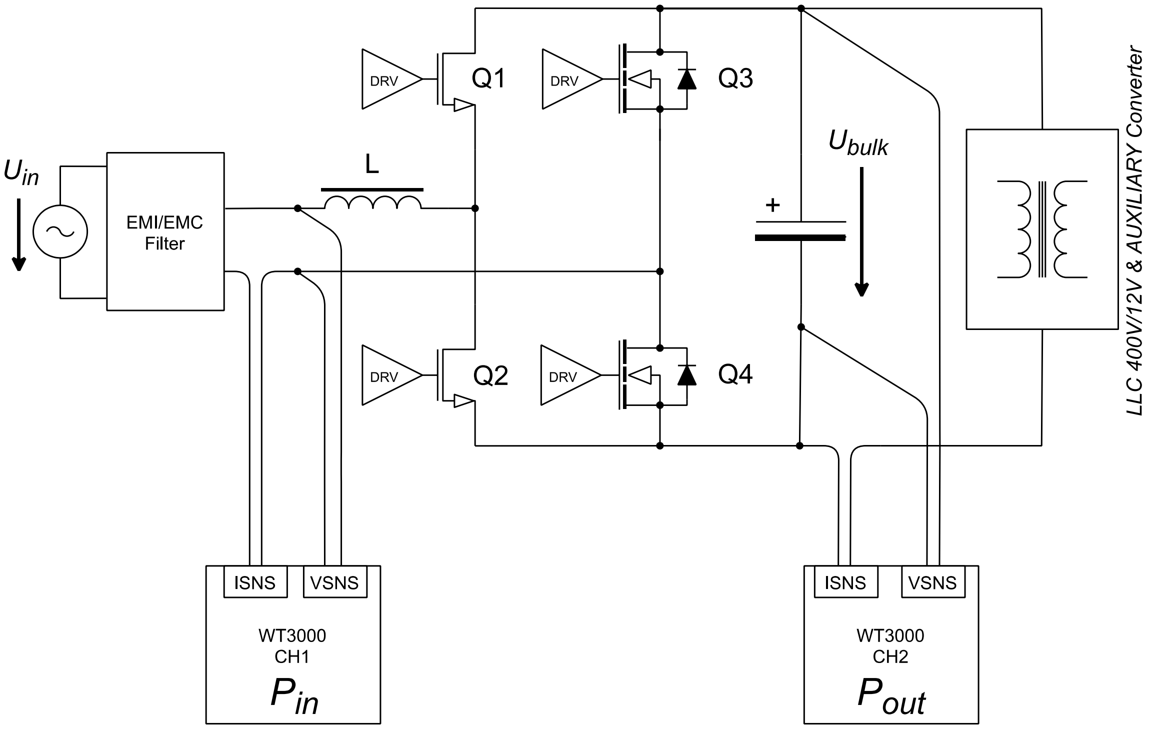


Fig. 85: WT3000 power analyzer connection for efficiency measurement

Design verification continues with characterization of power losses in various operating conditions and its comparison with calculated values to ensure, that no hidden problem is present. Efficiency data displayed in Fig. 86 were measured with calibrated power analyzer Yokogawa WT3000, based on schematic shown in Fig. 85. Input power is measured directly at totem pole input terminals – in series with inductor. Output power is measured at the bulk voltage, circuit is loaded with high voltage electronic load Chroma 63204. As the internal shunts of WT3000 are used to measure the current, voltage sense lines are connected in a way to exclude cable losses from the result. To avoid disturbance of connected instruments during voltage transient caused by synchronous rectifier (zero crossing of AC voltage) and current flowing over the capacitance of connected instruments to Ground, low pass filter is placed in series with electronic load.

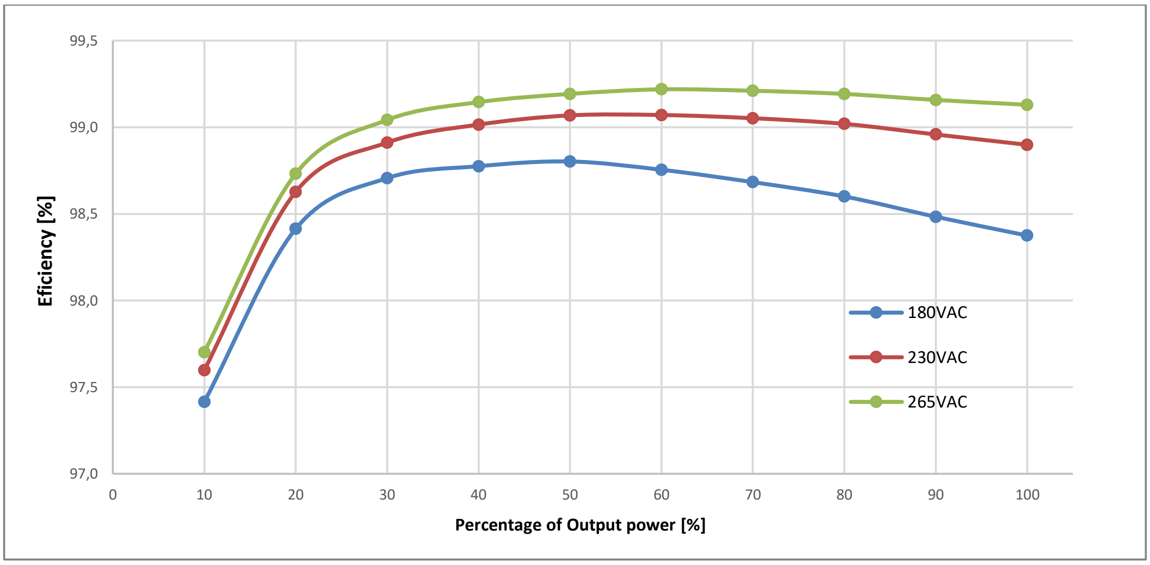


Fig. 86: Measured efficiency curves of tested prototype for various input voltage and output power conditions (at 60kHz)

Using scripting language and equations for power losses of all components, efficiency curve can be calculated for various input voltages and output power. As can be seen from both graphs, calculated curve is matching measured with +/-2W tolerance in power loss over the whole range of loads. Converter is reaching peak efficiency between 50-60% of load at the nominal conditions, optimization target is achieved. Maximum point of efficiency moved above half load of power factor corrector might be useful, as converter efficiency in 80Plus certification is qualified based on power present on the output terminals, therefore some margin for power losses of second DC/DC power stage is present.

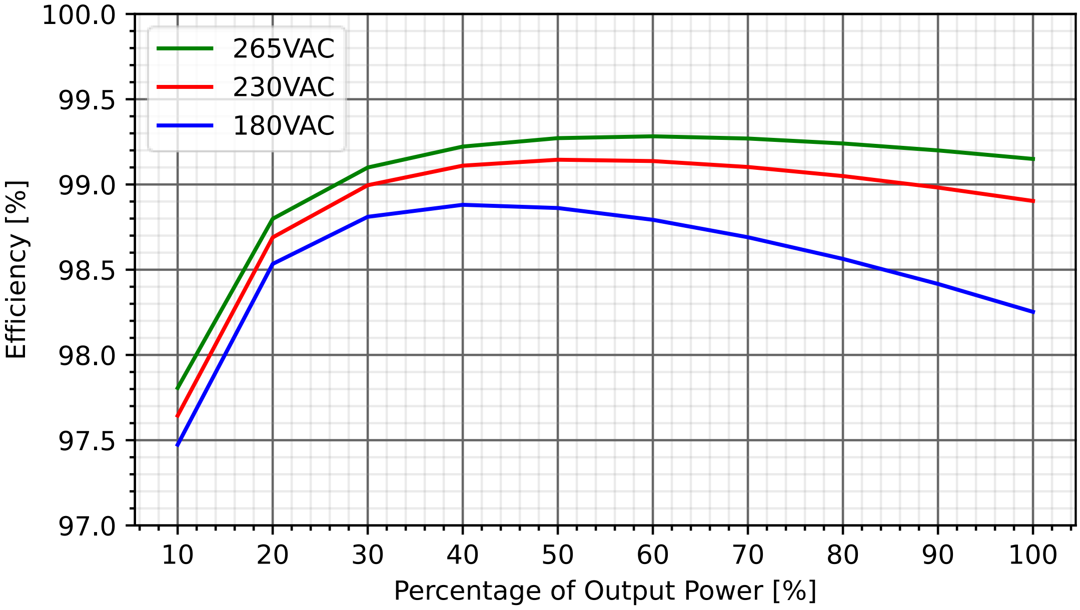


Fig. 87: Calculated efficiency curves of tested prototype for various input voltage and output power conditions (at 60kHz)

Second conducted experiment is related to verification of calculation of GaN switching losses. Prototype is measured with various switching frequencies from 60-90kHz at nominal operating input voltage 230VAC and on half/full load output power. As the input voltage and output power is the same, input RMS current should stay the same, therefore conducting losses on all components should be equivalent too. Gained results are again compared with calculated value, and the difference, especially at half load is visible. Root cause of the difference might be inaccurate switching power losses calculation or measured values are affected by changing amplitude of ripple current. Skin effect might take place in conductors and increase conducting power losses at lower switching frequency. Difference in power loss is small (<2W), therefore analysis is difficult and on the border of WT3000 power analyzer precision.

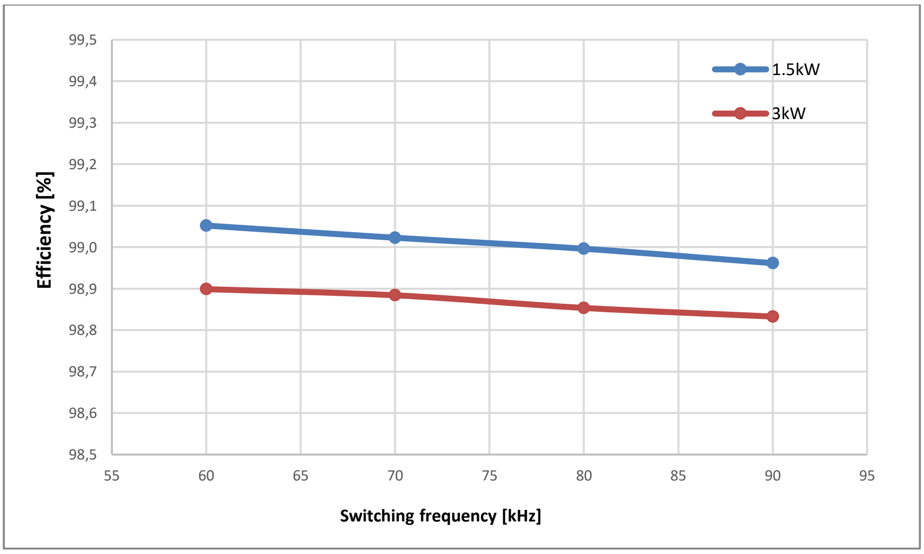


Fig. 88: Measured efficiency curves of tested prototype for switching frequency and output power conditions

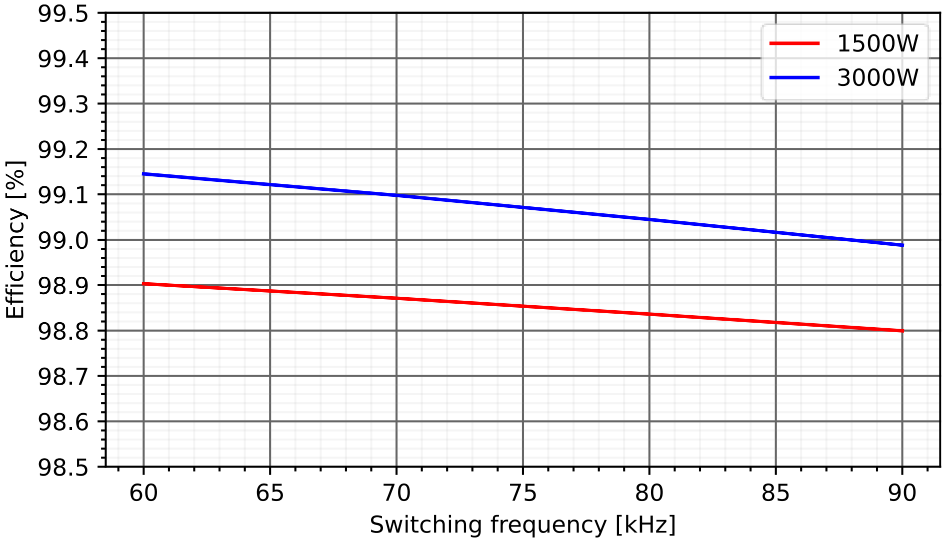


Fig. 89: Calculated efficiency curves of tested prototype for switching frequency and output power conditions

Meeting required limits of conducted and radiated emission spectrum according to Federal Communications Commission (FCC-USA), it is essential for product certification (CE-mark) and its introduction to the market/customer. Therefore, designed unit has to contain appropriate differential and common mode filter to pass the certification process.

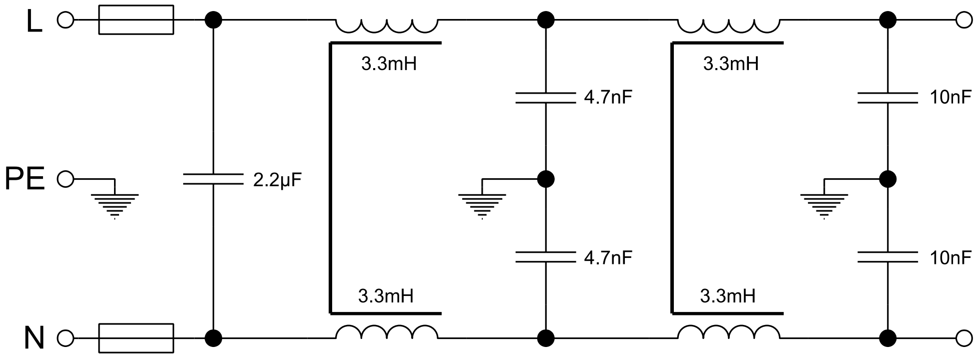


Fig. 90: Schematic of EMC filter used

Input filter schematic is visible in the figure above - consisting of two common mode inductors L1 and L2 and Y capacitors connected over bolts to the PE/chassis. Leakage inductance of common mode inductor together with X capacitors attenuate the differential noise, caused by operation of totem pole converter. As the PFC supplies isolated resonant (LLC) DC/DC converter, which transformer has certain interwinding capacitance, the common mode attenuation is necessary. Position of the PE termination of Y capacitors plays significant role in performance of the filter, as the path of the returning common mode currents is affected. As the bulk capacitor return is bouncing against PE with 100Hz frequency due to rectification of the input voltage, Y capacitors cannot be terminated at positive or negative terminal of bulk capacitor.

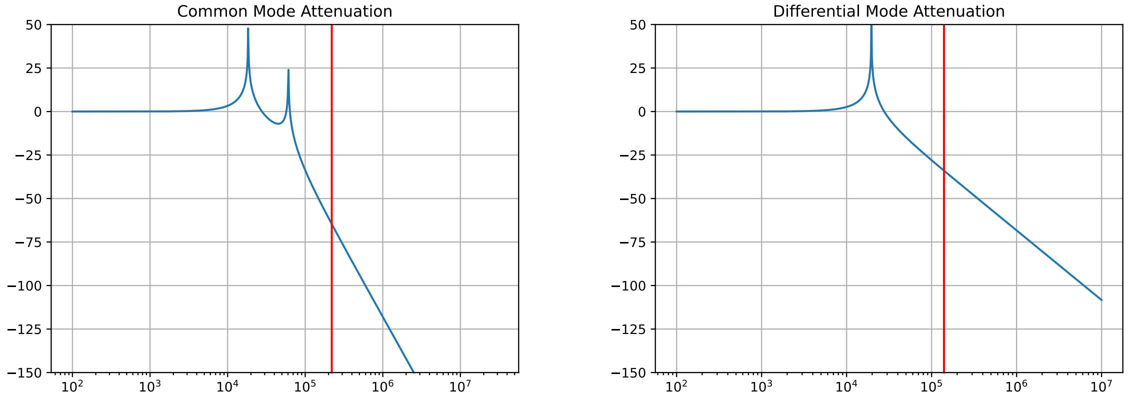
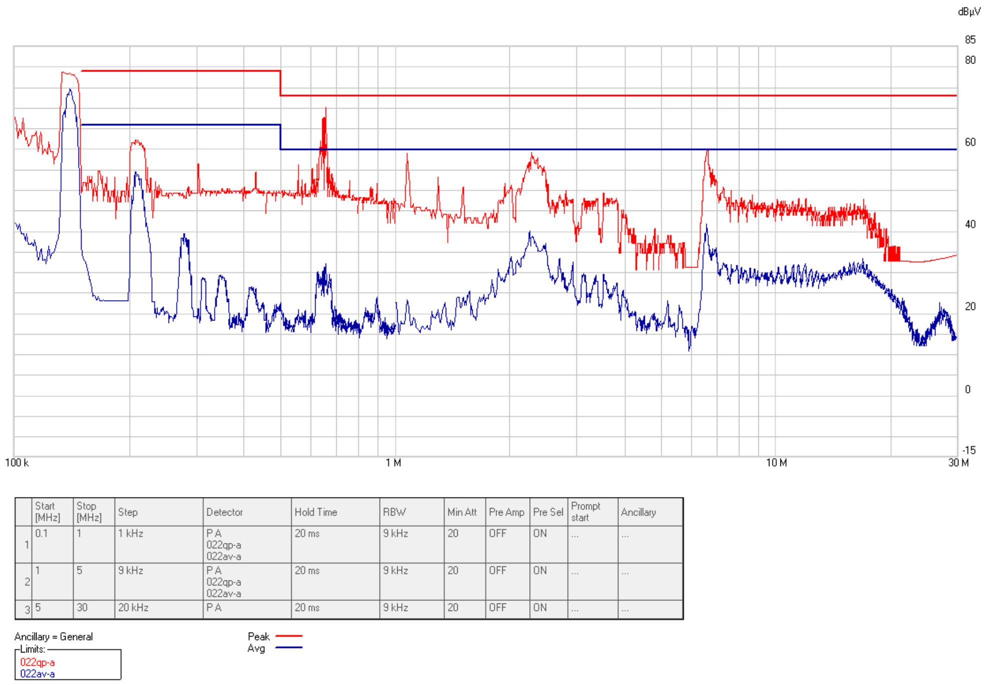


Fig. 91: Calculated attenuation of EMC filter

As the differential attenuation of the filter is relatively low at third harmonic of PFC operating frequency, dithering is used in order to spread the spectrum – reducing the emission on operating frequency of the PFC, while keeping the same volume of the input filter.

Setup for conducted emission measurement is using Line Impedance Stabilization Network according to standard, and emission are measured with PM9010 receiver



	Start [MHz]	Stop [MHz]	Step	Detector	Hold Time	RBW	Min Att	Pre Amp	Pre Sel	Prompt start	Ancillary
1	0.1	1	1 kHz	P A 022qp-a 022av-a	20 ms	9 kHz	20	OFF	ON	...	...
2	1	5	9 kHz	P A 022qp-a 022av-a	20 ms	9 kHz	20	OFF	ON	...	...
3	5	30	20 kHz	P A	20 ms	9 kHz	20	OFF	ON	...	...

Ancillary = General
Limits:
022qp-a
022av-a

Fig. 92: Conducted emission spectrum of GaN totem pole PFC operating with LLC converter, measured at Line input, nominal input voltage 230VAC (70kHz switching frequency)

Conducted emission spectrum was measured for prototype of the unit with GaN PFC converter, in order to search for possible influence of the spectrum by fast switching. Picture displayed above shows results for combination of resonant converter together with PFC – complete power supply unit. As the devices are operating at different frequencies, analysis of spectrum is possible:

- Power factor correction operates in measured case at frequency 70kHz, therefore first two peaks in the spectrum, second (140kHz), third (210kHz) and forth (280kHz) harmonic is related to current ripple present in the input current. This is expected and well predictable – attenuation of the two-stage filter is well visible.
- Peak visible between 600-700kHz is related to PFC switching performance – to small overshoot visible on top of drain-source voltage at hard switching edge Fig. 77, Fig. 78. This was figured out by multiple experiments, by changing input voltage at the same output load condition
- The rest of the spectrum is related to operation of LLC converter, operating at 220kHz with its higher harmonics

Prototype of the converter is compliant with FCC class A, without any special input filter requirements different to Silicon PFC used in many appliances nowadays.

8 RECUPERATING GATE DRIVE SOLUTION

Progress in GaN power semiconductor development capable of high frequency switching, is moving forward in other areas of integrated semiconductors, required for its application in circuit.

To support operation and gain benefit of GaN, many novel Gate driver devices are developed setting new benchmark for rise and fall time of output signal, propagation delay from input to output and switching current capability. Some of the Gate driver integrated circuits are using low voltage GaN technology with novel manufacturing processes (GaN on Si). One of the examples of revolutionary devices is LMG1020 capable of 4.5ns maximum propagation delay and 210ps rise and fall time, with peak driving current +7A (Source) /-5A (sink) current rating. This device is capable to work with GaN voltage levels up to outstanding 60MHz.

Many of these novel devices are originally designed for operation with GaN power semiconductors, but what if those outstanding parameters are useful somewhere else?

In high power and high efficiency resonant converters ($P_{out} = 6kW$, $\eta > 99\%$), every Watt of power loss needs to be treated carefully. Very high efficiency is needed in applications designed for high energy savings or for cases where cooling possibilities are significantly limited (space applications). From industrial experience, there is demand for this kind of power supplies on the market. In this specific application, optimization methods for switching and conductive losses are tuned to maximum, most of the further improvement is based on improving and tuning of parasitic elements (removing snubbers), reducing consumption of control circuits or inventing recuperative solutions for parts of the circuit, which are lossy.

Many of mentioned improvements might be achieved by novel integrated circuits - following lines shows example of improvement of synchronous rectifier of high output current resonant converter, by using special recuperative Gate driver circuit for Silicon MOSFET, using very fast GaN Gate driver.

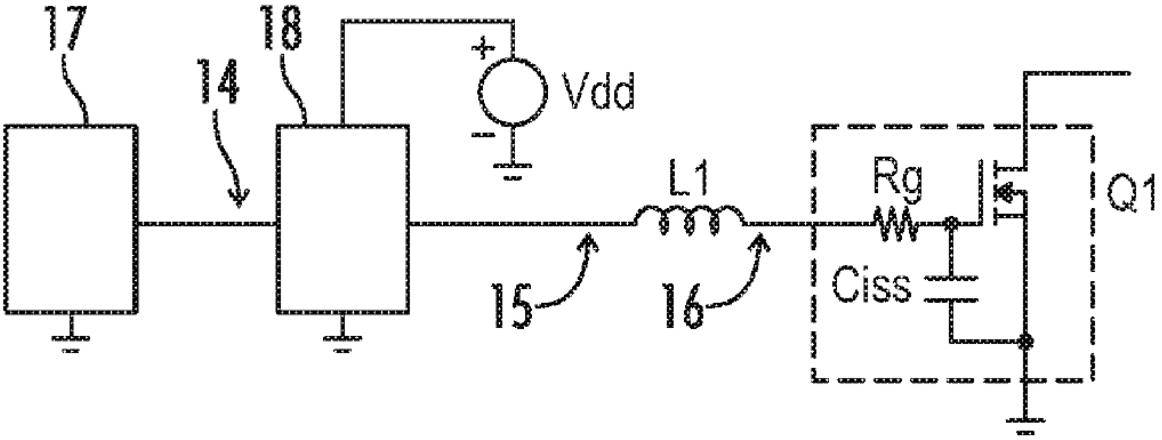


Fig. 93: Recuperative Gate driver for high current synchronous rectifier

To achieve higher efficiency of the synchronous rectifier in resonant converters, lower R_{DSon} of devices needs to be used. As there are basically no switching losses (commutation is done by primary), typically Silicon MOSFETs are connected in parallel, to achieve minimum possible resistance and minimum possible conduction losses, as the RMS value of current is typically high.

$$\Delta P_{drive} = X_{par}.\,Q_G.\,f_{sw}.\,U_{Vdd}^2 \tag{72}$$

$$\Delta P_{rect-cond} = \frac{R_{DSon}}{X_{par}}.\,I_{rect-RMS}^2 \tag{73}$$

With more switches in parallel the R_{DSon} is lower, but Gate driving losses are higher. Low voltage MOSFETs (30-40V) designed for high current capability have usually high area of active Silicon channel, high Gate-Source capacitance is present. With more MOSFETs in parallel Gate charge losses are getting significant, especially if it needs to be driven with high frequency. Typical range of operating frequencies for resonant converters is from 100kHz up to 500kHz at no load, problem of driving power loss is significant. At some point, adding more devices in parallel is no longer reasonable, as the difference saved in conduction loss (at half load) is compensated by Gate driving loss, effect on overall efficiency is not visible. The problem of Gate driving losses might be partially eliminated by reducing driving voltage up to approximately 6-7V, total charge is smaller.

More advanced solution might be using recuperative circuit, which is able to return Gate charge into driver power supply rail and reuse it in next cycle. By using novel gate driver designed for GaN LMG1020, providing very high efficiency of switching at low voltage, following circuit might be constructed (Fig. 93).

Principle of operation can be explained as one cycle buck-boost converter, inductor L1 is used for energy accumulation during switching cycles. By proper sequence of driving pulses for GaN driver can be achieved, that resonant waveform between inductor and Ciss of MOSFETs, damped by Rg, ends exactly at desired point – at maximum of Vdd during turn on cycle, at minimum voltage during turn off – “big” silicon MOSFET Gate discharge.

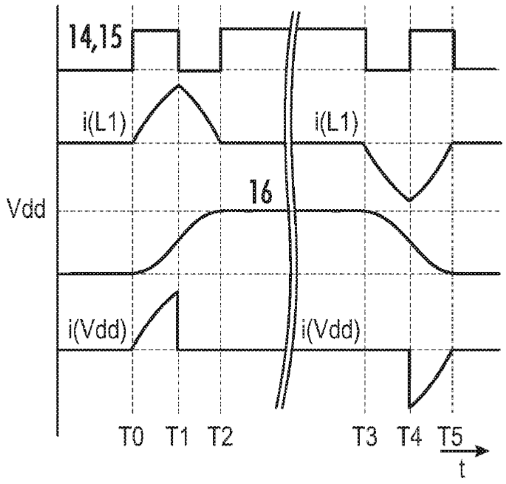


Fig. 94: Recuperative Gate driver control diagram

To create driving pulse sequence displayed on picture above, DSP operating at 100MHz with minimal resolution 10ns per bit is required to be able to precisely tune resonant cycle, therefore achieve the best efficiency of recuperation. In general, efficiency of this solution is depending on following factors:

1.) Internal Gate resistance of driven silicon power MOSFET
2.) Winding resistance of the inductor
3.) Internal resistance and switching speed of the driver
4.) Properly tuned pulse sequence to achieve ideal waveforms

Gate-Source capacitance Ciss is unfortunately for Silicon MOSFET not linear, and is depended on channel Drain-Source current. Therefore, there is a detuning effect, pulses need to be tuned online based on the output current of the converter, optimized especially for half load condition of converter – point of efficicency qualification.

Fig. 95: Scope snapshot of recuperative gate driver during operation (left), Detuning effect of Miller capacitance (right)

Internal gate resistance of available low voltage MOSFET might be high (eg. 3.3Ohm), search for optimized component is needed. At the time of investigation, best components were provided by TOSHIBA (series TPHR...), with internal resistance below 1Ω.

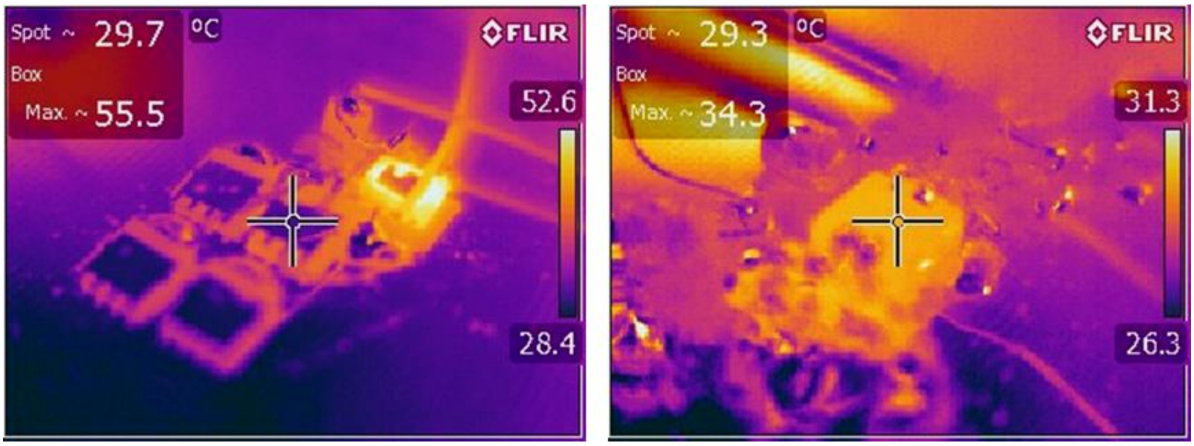


Fig. 96: Obvious difference in gate driver efficiency – conventional (left) and recuperative driver solution (right)

To test the idea of recuperative gate driver, prototype using LMG120 and TPW2R508NH (4x) MOSFET was build and power consumption was measured, results scaled for 32x TPW2R508NH MOSFETs representing the application of existing power supply, are displayed in the graph above. Accumulator of energy standard molded inductor Vishay IHLM2525 was used. Input power was measured using power analyzer Yokogawa WT3000 with external calibrated shunts suitable for low currents. As a main control element DSP TMS320F280049 with external logic gates was used.

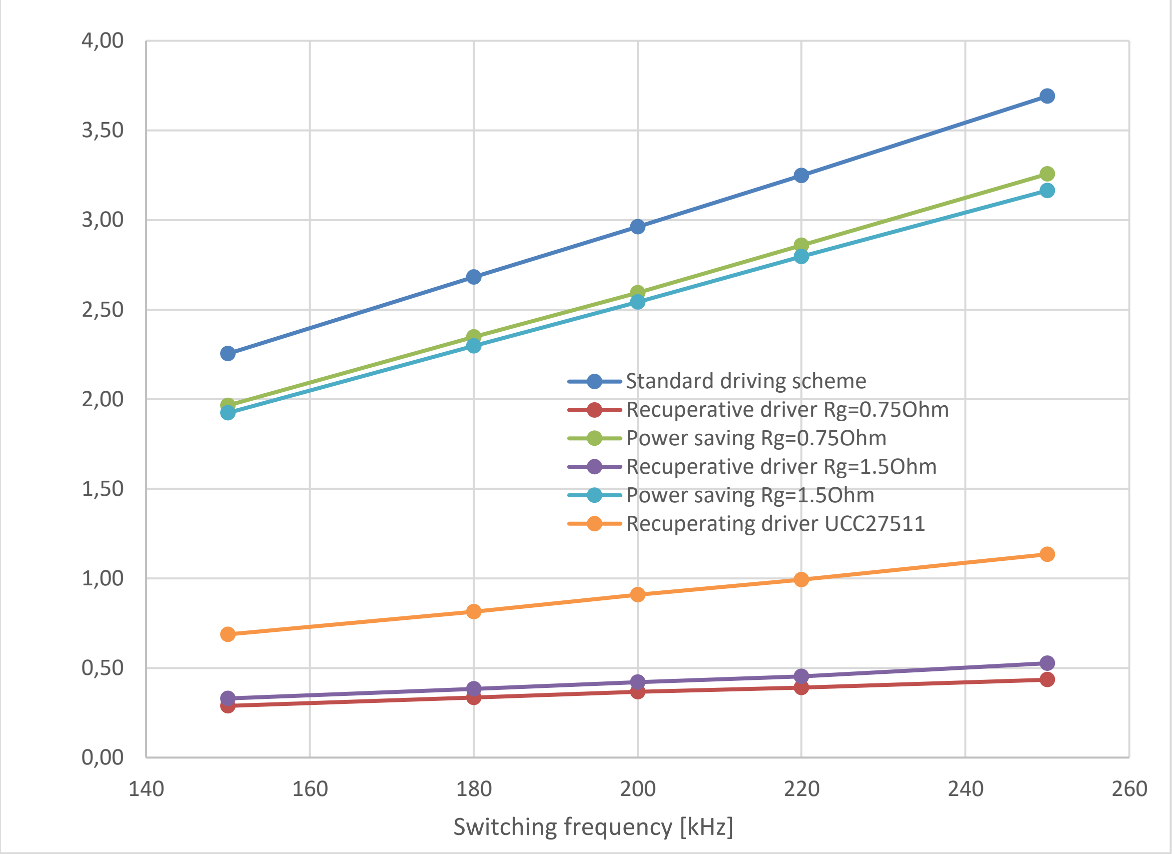


Fig. 97: Recuperative Gate driver power savings in different configuration

At 250 kHz operating frequency can recuperative driver using standard, available parts save 1.1W of power loss, when compared to classic Gate driving scheme. Differences in power losses are nicely visible on thermal camera snapshot Fig. 96, while in „classic“ solution the energy is stored in gate charge fully dissipated in driver (SO8-LM5101), in recuperative solution the maximum temperature is significantly lower – only losses in parasitic elements are contributing to the temperature rise.

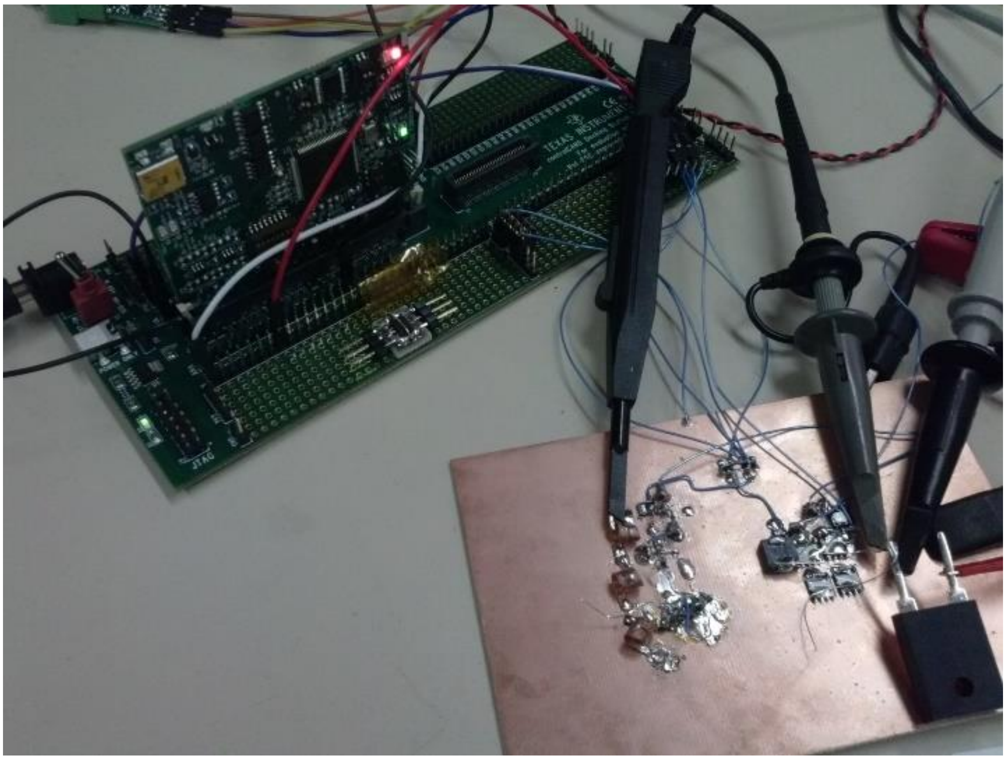


Fig. 98: Evaluation of recuperative gate driver

With future evolution of components, as lower internal gate resistors, lower internal resistance of driver, further improvement is possible. Power savings are getting more significant with higher frequencies. Although it is important to note, that implementation of special pulse generation together with compensation of detuning effect described in previous chapters might require calculation power of FPGA. Recuperative Gate drive solution presented in this chapter is suitable only for synchronous rectifier application, where the risk of entering hard switching mode does not exists. As the inductor is in series with the Gate, for high frequencies during du/dt in hard switching application the driver is not able to provide low impedance driving signal.

This solution of Recuperative Gate Drive Circuit and Method is registered by United States Patent US10250249B1, owned by Bel Power Solutions Inc. Santa Clara US.

9 CONCLUSION

Aim of this thesis is to explore and analyze advantages of Novel Gallium Nitrite wide bandgap transistors technology in switch mode power supply applications. Special focus is high power density and high efficiency power supplies used for server and telecom applications, as optimization in this field of power consumption brings significant power savings worldwide, reduction of carbon dioxide production is possible. Due to Author´s tight cooperation with industry, given goals and investigated topics are related to major problems related to successful implementation of novel technology into commercial products.

Partial goals of this thesis are fulfilled and have following conclusions:

1. Portfolio of currently available GaN devices is limited, but growing constantly and attacking higher ratings with every newly released device. Nearly all nowadays available transistors are produced as GaN structures on standard Silicon wafers – which gives advantage for ease of implementation into production for chip manufacturers, on the other hands limits the possibilities of price reduction, therefore attractiveness of GaN for commercial products. Conducted analysis shows, that one of the most promising structures is enhanced mode transistor, although also the most challenging for gate driver performance. Future of GaN switching devices might lead to on chip integrated drivers aiming to maximize the device performance in custom designs.

2. Gate driving requirements are minimizing package sizes dramatically. Third Chapter shows novel methods and design principles to achieve high performance cooling of minimized surface mount packages, widely used for recently released GaN devices. Special insulated metal substrate printed circuit board stack-up, developed in cooperation with PCB manufacturing company, optimized for cooling and switching performance is presented and proposed as reference for industrial designs. For cost sensitive applications, lower performance methods of cooling are presented and optimized using FEM simulations. Extensive research is proven by measurement on various physical prototypes.

3. One chapter of this thesis is related to deep analysis of the problem related to early samples of GaN devices from all manufacturers - electron trapping under the gate electrode of high electron mobility transistors. As a result of this phenomena is on state channel resistance variation over the time shortly after the switch event present, resulting in possible higher conduction losses in high switching frequency operating converters. To characterize this problem, special tester able to operate with standard equipment was developed and measurement on three different samples from three different manufacturers was conducted. Gained results show, that certain increase in on state channel resistance is present and might impact the end application. Test setup was published and proposed to JEDEC committee, as one of the points stated in standard JC-70 required for successful qualification of wide bandgap devices is dynamic R_{DSon} measurement.

4. Results of research from previous chapters are now applied in design of totem pole converter for power factor correction with 3kW output power. Application of fast switching GaN transistors gives biggest advantage in hard switching applications, where the efficiency and power density improvements are significant. Choice of power and input voltage range is not random - 80Plus Titanium mark in server/computer applications is requested by upcoming European Union regulations, therefore optimization of PFC stage together with isolated DC/DC converter is needed for all newly designed power supplies entering mentioned sectors. Peak efficiency of designed converter is after optimization of all components achieved at half load and exceeding 99% at nominal input conditions, which gives good margin and it is fulfilling defined target.
   High power density of the converter is achieved by integrating gate driving circuit together with power stage on insulated metal substrate board. Optimized control technique performed by digital signal processor reduces the needs for hardware complexity and size of the components used. Complete design verification measurements - including oscilloscope snapshots, thermal measurement and emission analysis of totem pole converter using novel Gallium Nitride technology are included.

5. Outstanding parameters of components developed specifically for GaN transistors, might give advantages in different fields of electronics – example can be seen in eight chapter of this thesis. Further efficiency optimization of resonant converters might be particularly difficult, if ultra-high efficiency needs to be achieved. For this purpose, innovative recuperative gate driving method for secondary side silicon rectifier of resonant converter was developed, resulting in successful US patent application.

One of the major drivers for success of GaN technology in commercial applications is optimization of its cost, which is comparing to its robust SiC counterparts still questionable. Author’s research will continue by exploring transition mode of operation, which together with Gallium Nitride semiconductors and advanced control algorithm might give various advantages in specific converter topologies. Analysis of the reliability data related to converters based on GaN semiconductors operating in the field might be interesting topic for future research.

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SYMBOLS AND ABBREVIATIONS

Symbol	Description	Unit
A	Area	[m^2]
$A_{e\text{-}min}$	Minimal cross section of the core	[m^2]
B	Magnetic flux density	[T]
C	Electrical capacitance	[F]
$CMTI$	Common mode transient immunity	[Vs^{-1}]
D	Duty cycle	[%/100]
d	Distance	[m]
d_w	Wire diameter	[m]
E	Energy	[J]
f	Frequency	[Hz]
f_{res}	Resonant frequency	[Hz]
f_{sw}	Switching frequency	[Hz]
H	Magnetic field intensity	[Am^{-1}]
I	Current	[A]
I_{AV}	Average value of current	[A]
I_{pk}	Peak value of current	[A]
I_{RMS}	Rms (root mean square) value of current	[A]
J	Current density	[Am^{-2}]
k_{cu}	Copper fill factor - winding	[%/100]
k_{vias}	Copper fill factor of vias	[%]
L	Inductance	[H]
L_m	Magnetizing inductance	[H]
N	Number of turns	[-]
P	Power	[W]
Q	Electric charge	[C]
R	Resistance	[Ω]
r	Radius	[m]
r_{DSon}	On-state channel resistance (variable)	[Ω]
R_ϑ	Thermal resistance	[KW^{-1}]
T	Period	[s]
t_f	Fall time	[s]
t_r	Rise time	[s]
U	Voltage	[V]
U_{bulk}	Bulk voltage	[V]
V	Volume	[m^3]
ΔP	Power loss	[W]

Symbol	Description	Unit
ΔP_{cond}	Conducting Power loss	[W]
ΔP_{sw}	Switching Power loss	[W]
$\Delta \vartheta$	Temperature difference	[°C]
ε	Relative permittivity	[-]
ε_0	Permittivity	[Fm^{-1}]
η	Efficiency	[%]
ϑ	Temperature	[°C]
λ	Thermal conductivity	[Wm^{-1}K^{-1}]
λ_{cu}	Thermal conductivity of copper	[Wm^{-1}K^{-1}]
μ_0	Permeability of vacuum	[Hm^{-1}]
μ_r	Relative permeability	[-]
ς	Resistivity	[Ωm]
Ψ	Magnetic flux	[Wb]

Abbreviations

BW	Bandwidth
CCM	Continuous conduction mode
DSP	Digital signal processor
DUT	Device under test
FEM	Finite element method
GaN	Gallium Nitride
MOSFET	Metal oxide semiconductor field effect transistor
PCB	Printed circuit board
PFC	Power factor correction
SiC	Silicon Carbide

LIST OF APPENDICES

Appendix no. 1: Dynamic RDSon tester – Eagle design files (Schematic & PCB)

Appendix no. 2: Dynamic RDSon tester – DSP software and Control GUI

Appendix no. 3: TMS320F28004x – Transition mode PWM setup example (C code)

Appendix no. 4: GaN GS66508 Halfbridge – KiCad design files (Schematic & PCB)

Appendix no. 5: PFC calculations in python (Jupyter notebook)

Appendix no. 6: DSP Debug tool KiCad design files (Schematic & PCB), latest version always available on Github.com (project name: PCB-HWmonitor_DSPlink)

LIST OF AUTHOR'S PUBLICATIONS

Author´s Publications related to topic of this Thesis

[1] ŠÍR, M.; FENO, I. Efficiency optimization of totem pole PFC with Gallium Nitride semiconductors. Przeglad Elektrotechniczny, 2021, roč. 2021, č. 6, s. 151-154. ISSN: 0033-2097.

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