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HIGH EFFICIENCY N-TYPE MONOCRYSTALLINE SILICON SOLAR CELLS

SOLÁRNÍ ČLÁNKY Z MONOKRYSTALICKÉHO KŘEMÍKU TYPU N S VYSOKOU ÚČINNOSTÍ

DOCTORAL THESIS
DIZERTAČNÍ PRÁCE

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Abstract

This dissertation is deals with searching and verifying of new processes contributing towards increase in efficiency of bifacial solar cells based on monocrystalline silicon *n*-type material. This work brings new knowledge about improvements in processes and methods used during its production at the ISC Konstanz. Within this work high efficiency *n*-type PERT (Passivated Emitter Rear Totally diffused) solar cells were made using standard mass-production facilities as in industrial production. This allows to show possibility of production high-quality *n*-type solar cells using almost the same equipment as for *p*-type solar cells. The efficiency increase was based on enhancing and balancing of individual production steps which were the same as in standard mass-production. Experiments described in this work vouch for the improvements in boron diffusion process, adjusting the passivation layer composition and its properties to new emitter design, and changes in metallization in term of using pure silver paste for emitter metallization, printing layout, and firing sequences. The structure and composition of ARC and passivation layer was investigated to reduce the process of Potential Induced Degradation (PID). The highest efficiency of the produced photovoltaics cells based on *n*-type material and made at standard process-line was 20. 9 %.

Key words

Solar cell, silicon, *n*-type, boron emitter, diffusion, passivation layer, metallization.

Abstrakt

Tato dizertační práce je zaměřena vývoj a ověřování nových postupů přispívajících ke zvýšení účinnosti bifaciálních solárních článků založených na monokrystalickém křemíku *n*-typové vodivosti. Tato práce přináší nové poznatky o vylepšených výrobních procesech a postupech použitých během výroby článků v ISC Konstanz. V rámci práce byly vyrobeny solární články typu *n*-PERT (Passivated Emitter Rear Totally diffused) s vysokou účinností, a to pomocí standartních procesů a zařízení používaných běžně při průmyslové výrobě. Zapojení těchto průmyslových postupů a metod umožnilo ověřit možnosti výroby *n*-typových článků za použití téměř totožného vybavení, jaké je potřeba pro výrobu *p*-typových článků. Zvýšení účinnosti bylo založeno především na vylepšení jednotlivých procesních kroků. Experimenty popsané v této práci dosvědčují zlepšení procesu difúze bóru, přizpůsobení parametrů pasivační a antireflexní vrstvy nově navrženému emitoru, zlepšení procesu metalizace ve smyslu využití past neobsahujících hliník, testování tisku rozličných motivů spolu s různými sekvencemi výpalu. V rámci práce byla testována možnost zamezení jevu potenciální indukované degradace (Potential Induced Degradation – PID) pomocí vhodného složení ARC a pasivační vrstvy. Vyrobené *n*-typové solární články dosáhly maximální hodnoty účinnosti 20,9 %.

Klíčová slova

Solární článek, křemík, *n*-typový, bórový emitor, difúze, pasivační vrstva, metalizace.

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Declaration

I declare that I have written my doctoral thesis on the theme of "High Efficiency n-type Monocrystalline Silicon Solar Cells" independently, under the guidance of the doctoral thesis supervisor and using the technical literature and other sources of information which are all quoted in the thesis and detailed in the list of literature at the end of the thesis.

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Ing. Barbora Mojrová, Author's signature

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Introduction

In the near future, the global growth of electricity consumption cannot be met solely by the current technologies, based on fossil-fuel power plants and nuclear power plants. The fossil-fuel depletion and the social and environmental problems associated with these energy sources mean that renewable energy sources, e. g. hydro, ocean, wind, geothermal, and solar, will need to play a bigger role than they do today. Use of renewable energy dramatically reduces global warming emissions, improves public health and provides jobs and other economic benefits. And since most renewables do not require water for cooling, they dramatically reduce the water consumption requirements for power production compared to fossil-fuelled power plants. The Renewable Electricity Futures Study found that an 80 % renewable energy future is feasible with these currently available technologies. For that reasons it is necessary focus on suitable renewable sources with respect to their distribution over the world.

Photovoltaic solar energy conversion is recently widely studied as one of the sources of renewable energy, which could play a dominant role in the future. For the most of middle European countries, including the Czech Republic, the photovoltaic-based power-plants are suitable solutions thanks to mild climate. The photovoltaic systems can be placed almost everywhere, they do not require either building dams or high pylons. The rooftop photovoltaic systems are becoming more popular i.a. for family houses, also thanks to fact, that after 2020 all newly built buildings must meet the requirements for passive buildings. Building up photovoltaic power plant on fields, which was popular 10 years ago, is thankfully not very probable in the future.

Because of the reasons mentioned above, it is necessary to deal with the improvement of solar cell efficiency, which in case of using the most widely spread technology based on silicon is about 32 %, according to the Shockley Queisser Efficiency Limit [1]. This technology is interesting due to well-known processes, production speed and thus very low price compared to other technologies. From the chart published by National Renewable Energy Laboratory [2] showing the best research-cell efficiencies through all technologies it is clear, that with the highest efficiency of 26.1 % (cell made by Fraunhofer-ISE) the silicon-based technology is not ready for the scrap heap yet. The improvement within the mass-production is focused on using different solar cells structures and adjusting particular processes during production to reach this aim, together with respect to the total costs.

Despite the fact, that the first solar cell was based on an *n*-type silicon wafer, much of the research, development and technological advances in solar photovoltaics were focused around a *p*-type based technology. This is coming from the earlier use of a solar cell, which was mainly focused on the outer space. The *p*-type solar cells are much more resistant to the radiation and degradation from cosmic environment [3].

During the past decade, the focus has returned to the *n*-type cell variants. Some years ago, there were just a few companies making *n*-type solar panels, with efforts spread across three main approaches: back-contact, heterojunction, and *n*-type designs that are more analogous to regular *p*-type solar cell processing but have a rear passivation/diffusion. Now, there are approximately 20 meaningful *n*-type cell producers and many other institutes are engaged at the R&D levels. Consequently, the global cell production of the *n*-type solar cells and modules has grown from the 2 GW-level in 2013 to what is projected to be more than 5GW this year (2018) [4]. The International Technology Roadmap for Photovoltaic predicts that the market share of *p*-type monocrystalline silicon cells will hold around 30 % through 2028, while *n*-type monocrystalline silicon solar cells will increase to about 28 % from barely 5 % in 2017 [5].

This work is dedicated to the high-efficiency monocrystalline solar cells based on the *n*-type silicon, which seems to be more promising material for further investigation than the standard *p*-type material, because *n*-type substrates are, among other things, less prone to various degradation mechanisms occurring here on Earth. This advantage transfers directly into reliability and lifetime performance.

Most of the experimental work took place at the International Solar Energy Research Center in Konstanz (ISC Konstanz) in Germany where a pilot scale solar cell manufacturing line is set up, providing testing conditions identical to those in the mass production together with measurement of solar cells parameters during fabrication. This institution looks into development methods leading to increase solar cell efficiency at “industrial” level, using standard industrial devices, which have been often set up for *p*-type-based production. The ISC Konstanz and similar institutions bridge a gap between highly-specialised development at research centres and common use in the industry. The aim, why experimental part took place there, was to show possibilities of using these usual methods and equipment for creation high-efficiency solar cells. The topography pictures of solar cells surface were taken at Fill Factory (formerly Solartec) in Rožnov pod Radhoštěm.

1 State of the art

Despite the rapidly increasing number of materials and technologies used for solar cell production the silicon and silicon-based technology stays as the photovoltaics mainstream. This is due to good electrical properties of silicon and also an established technology of electrical components production from silicon.

First part of this chapter is dedicated to comparison of the *p*-type and the *n*-type silicon and their advantages and disadvantages in a solar cell production. Further the basic high efficiency solar cell concepts are introduced, aimed at the *n*-type architecture. It also gives an introduction to the manufacturing steps, which are involved in the industrial *n*-type solar cell manufacturing, basic parameters of solar cells, and the characterization methods used in this work.

1.1 Comparison of an *p*-type and an *n*-type solar cell

The first solar cell fabricated by Bell Laboratories in 1954 was made of an *n*-type silicon wafer. Despite this promising start much of the research, development and technological advances in solar photovoltaics were focused around *p*-type silicon (Si) wafers. The *p*-type technology is still dominant today in spite of the fact that the two technologies featuring the highest efficiencies in the industrial production are based on *n*-type Czochralski (Cz) silicon wafers.

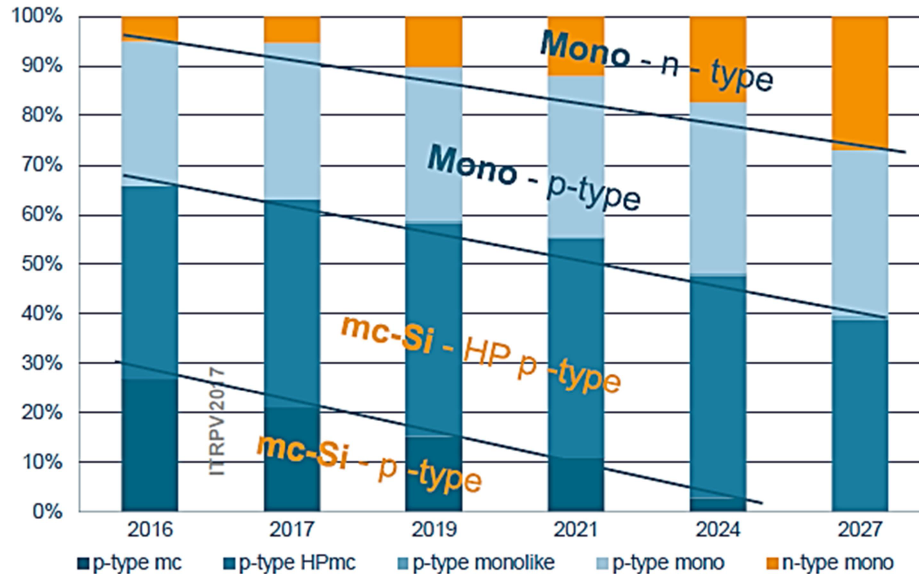


Fig. 1: Trend in the market share of crystalline silicon material types [6].

The reason has mostly historical background and most probably the *n*-type technology will gain more and more importance in the share of technologies as many companies will upgrade their facilities. The *n*-type cells are forecast to increase steadily by 2020, from a minority 3 % market share in 2015 to reach 14 % by 2020 [7]. According to the

International Technology Roadmap for Photovoltaic the photovoltaic market will be divided into high-perfomance (HP) *p*-type multicrystalline (mc) silicon solar cells with efficiency above 22 % and *n*-type solar cells with efficiency over 25 %, see **Fig. 1**. However, due to the low price and existing facilities, around 1/3 of production will be covered by *p*-type solar cells [8].

There are two main advantages of using the *n*-type silicon instead of the *p*-type:

1) Due to the absence of boron there is no light induced degradation (LID) occurring in the *p*-type silicon wafers, caused by boron-oxygen complexes. The LID in the *p*-type solar cells occurs when oxygen impurities in the silicon wafer react with the doped boron in the first few hours/weeks of an illumination of the cell. This effect causes degradation in the carrier lifetime and immediately reduces cell efficiencies by 2 % - 4 %. The absence of boron in phosphorus-doped *n*-type substrates eliminates the boron oxygen defects even for the higher oxygen concentration and thus this drop in efficiency and power output is not evident [3] [9].

2) The *n*-type silicon is less sensitive to prominent metallic impurities, such as the interstitial iron (Fe), which can capture electrons much more effectively as it has a positive charge. The minority carriers in the *n*-type silicon are holes instead of electrons, as in the case of the *p*-type silicon. Therefore, it offers a higher minority carrier diffusion length in comparison to the *p*-type crystalline silicon wafers with similar impurity concentrations [10] [11] [12].

The fabrication of solar cells with an efficiency of over 20 % requires wafers with high electrical quality. However, producers of the *n*-type cells can rely on using lower quality and thus cheaper wafers (in particular thanks to the higher minority charge carrier diffusion length) [8].

Moreover, the use of a phosphorus-doped back surface field (BSF) with convenient surface passivation for such *n*-type cells results in a higher diffusion length and better rear internal reflection. The use of a boron-doped front emitter with a rear side phosphorus-doped BSF on *n*-type substrates offers a bifacial type cell structure which can be fabricated on thinner wafers. Convenience of making such bifacial designed solar cells and modules using phosphorus-doped BSF also generates opportunities to produce cells with higher efficiencies [12].

Last but not least, there is the evidence that the *n*-type devices are more sensitive to a low light intensity, as well as having a lower temperature coefficient, mostly due to a higher V_{OC}. Also, the *n*-type silicon is less prone to degradation during high temperature processes, e.g. boron diffusion [12] [13].

Based on these advantages the *n*-type seems to be highly suitable for advanced high efficiency cell concepts like interdigitated back contact (IBC) cells and passivated emitter and rear cell/locally diffused (PERC/PERL) type cells, as well as bifacial passivated emitter and rear totally diffused (PERT) type cells, which are described in the following chapter.

1.2 Advanced crystalline silicon solar cell concepts

An aluminium back surface field (Al-BSF, **Fig. 2**) created by a co-fired screen-printed method and front side doped with phosphorus is currently dominating monocrystalline and multicrystalline silicon solar cell structure. However, there are numbers of solar cell structures with high efficiency based on the *n*-type substrates that have been successfully implemented into the mass production. These cell structures can be categorized according to the techniques used for cell processing (**Fig. 3**):

- front surface field (FSF) Al rear-emitter cells (n^+np^+ cells) can either have the contacts from both sides or from the rear side only and normally has phosphorus diffused FSF,
- back surface field (BSF) front-emitter cells (p^+nn^+ cells) can also have the contacts either from both sides or from the rear side only and are commonly boron-doped emitters with phosphorus-doped BSF,
- ion implanted emitters cells have the emitter formed by ion implantation process and can be realized for both front and rear contact schemes on n^+np^+ and p^+nn^+ structures,
- heterojunction with intrinsic thin-layer (HIT) cell structure [12].

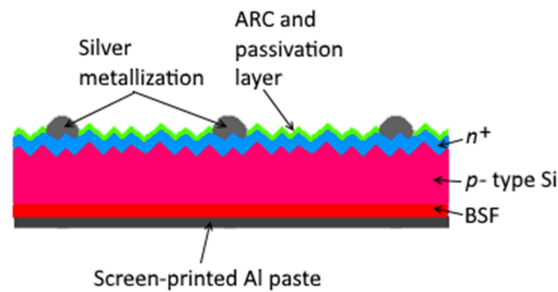


Fig. 2: Schematic drawing of standard *p*-type Al-BSF solar cell.

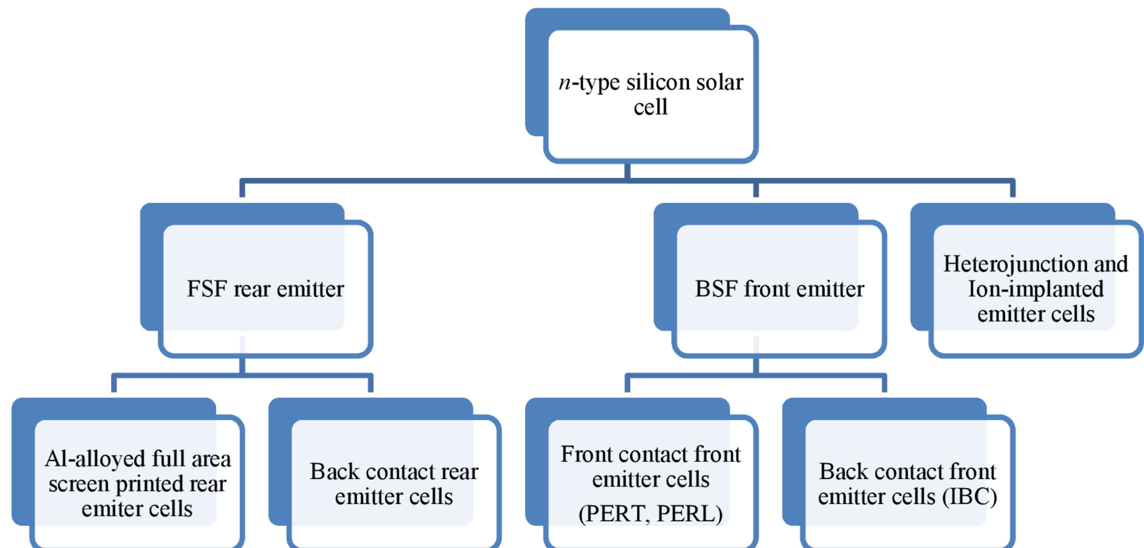


Fig. 3: The flow chart of the possible cell structures using *n*-type silicon substrates.

1.2.1 PERC concept

In comparison to the standard solar cell concept the PERC (Passivated Emitter and Rear Cell, **Fig. 4**) concept reduces rear surface recombination by combining the dielectric surface passivation and reducing the metal/semiconductor contact area, together with simultaneously increased rear surface reflection by dielectrically displaced rear metal reflector. The *p*-type monofacial PERC is currently entering into mass production, but the efficiency of this type of cell is affected by LID.

If the PERC architecture is transferred from the *p*-type to the *n*-type silicon, a cell structure contains many small local point-formed aluminium emitter regions, which are alloyed into the passivated silicon back surface of the cell. As a result, the first large-area (144 cm^2) *n*-type cells prepared in this way achieved the efficiency of 19.7 % [14]. Another approach is a concept called BiCoRE (Bifacial Co-diffused Rear Emitter, **Fig. 5**), which combines the PERC-type cell process with the *n*-type wafers. Being illuminated from the front, the best BiCoRE cells achieved efficiency of 20.6 % [15].

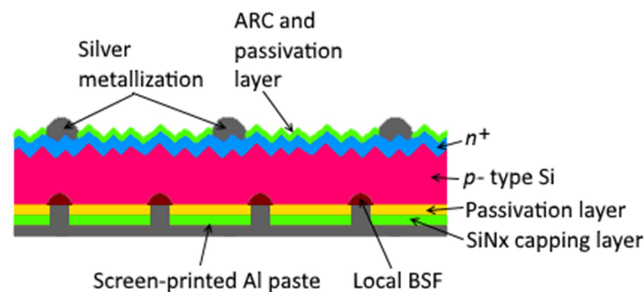


Fig. 4: Schematic drawing of standard *p*-type PERC solar cell.

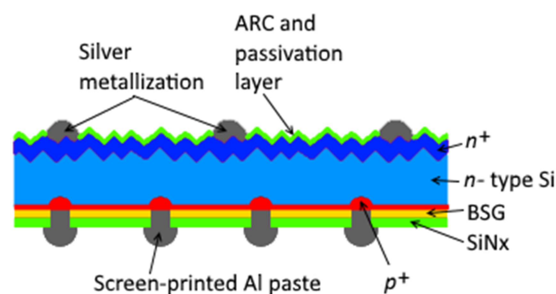


Fig. 5: Schematic drawing of the BiCoRE cell with PECVD BSG/SiN_X layer as rear-side diffusion source and passivation [15].

1.2.2 PERL concept

The PERL (Passivated Emitter, Rear Locally Diffused, **Fig. 6**) concept uses micro-electronic techniques to produce cells with efficiencies approaching 25 % under the standard AM 1.5 spectrum. The passivated emitter refers to the high quality oxide at the front surface, which significantly lowers the number of carriers recombining at the surface. The rear side is locally diffused only at the metal contacts to minimise recombination there while maintaining good electrical contact [16].

The *n*-type PERL cell, featuring local n^+ BSF fabricated with the use of photolithography processes, involves many different process steps. To simplify the

formation on the n^+ BSF the new process called PassDopp [16] has been invented, where a phosphorus containing passivation layer is locally opened by a laser under the simultaneous diffusion of phosphorus atoms into silicon. Using this process the efficiency of 23.2 % was reached [17].

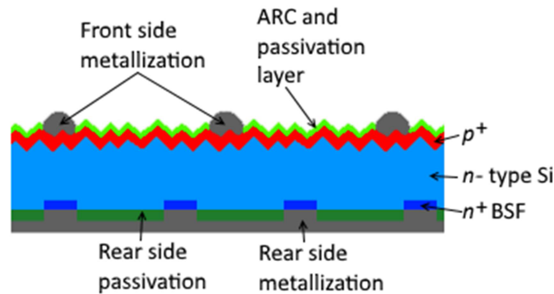


Fig. 6: Schematic drawing of standard *n*-type PERL solar cell.

1.2.3 PERT concept

The PERT (Passivated Emitter, Rear Totally Diffused, **Fig.** 7) cell concept cell can be easily modified to *n*-type substrates and offers a high efficiency potential. It can be fabricated with the front emitter or as back junction cells with the emitter on the rear side. The company Imec announced that they have realized bifacial *n*-PERT solar cells using an industrially-compatible process with an average front-side conversion efficiency of 22.4 %, with the best cell topping 22.8 %. Under standard front illumination conditions in conjunction with an additional 0.15 sun rear illumination these bifacial cells can produce energy equivalent to 26.2 % at monofacial cells [18].

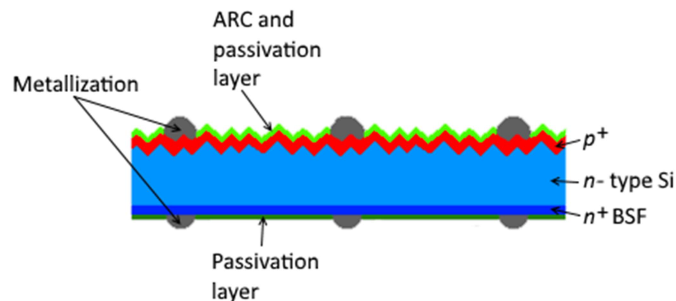


Fig. 7: Schematic drawing of *n*-PERT solar cell.

1.2.4 IBC cell concept

For the interdigitated back contact (IBC) cell concept (**Fig. 8**) it is characteristic that all metal contacts can be found on the rear side of the cell. The higher efficiency potentially results from the reduced shading on the front side of the cell. By using a thin solar cell made from a high quality material, electron-hole pairs, generated by the light absorbed at the front surface, can still be collected at the rear of the cell [19]. Such cells are especially useful in concentrator applications where the effect of the cell series resistance is greater. These advantages stand in opposition to the higher process complexity due to the requirement of patterned diffusions and the risk of fatal cell shunting due to the proximity of n^+ and p^+ doped regions [20]. The company Trina Solar

reached total efficiency of 24.13 % for a large-area ($156 \times 156\ mm^2$) *n*-type mono-crystalline silicon IBC solar cell [21].

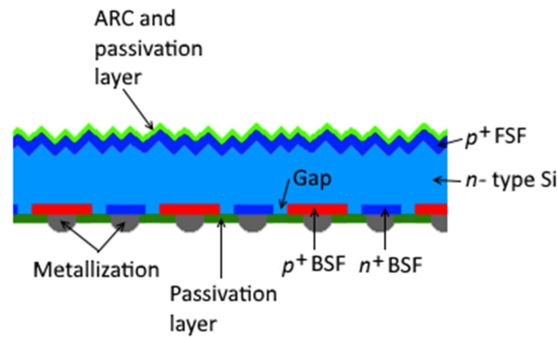


Fig. 8: Schematic drawing of *n*-type IBC solar cell.

1.3 Standard process flow

The majority of industrially produced crystalline silicon solar cells are fabricated from multicrystalline (mc-Si) and monocrystalline (mono-Si) grown silicon wafers. The main advantages are the cheaper production cost and the potential for higher efficiencies. Silicon wafer based PV technology accounted for about 93 % of the total production in 2015. The share of multicrystalline technology was about 69 % of the total production (**Fig. 9**) [22].

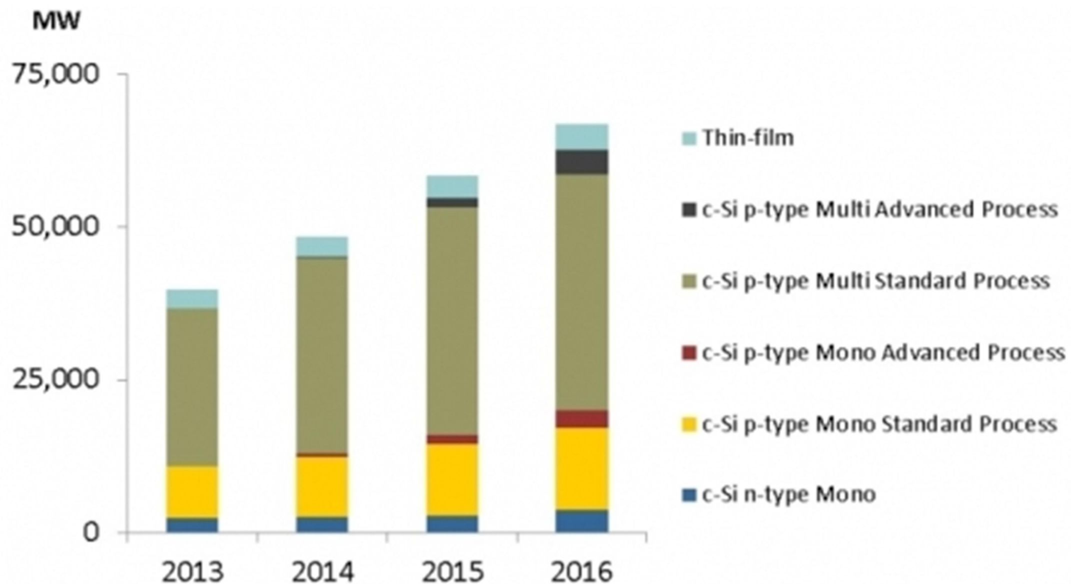


Fig. 9: Annual production by cell technology type [23].

The main process steps in production of solar cells from silicon in industry highly resemble each other. It begins with treatment of bare silicon wafers, continues with boron/phosphorus diffusions and depositions of ARC and passivation layers, and finishes with metallization. The typical production process of *n*-type PERT crystalline silicon solar cells, used in solar cell industry, is characterised by a limited number of process steps, which are shown in **Fig. 10**.

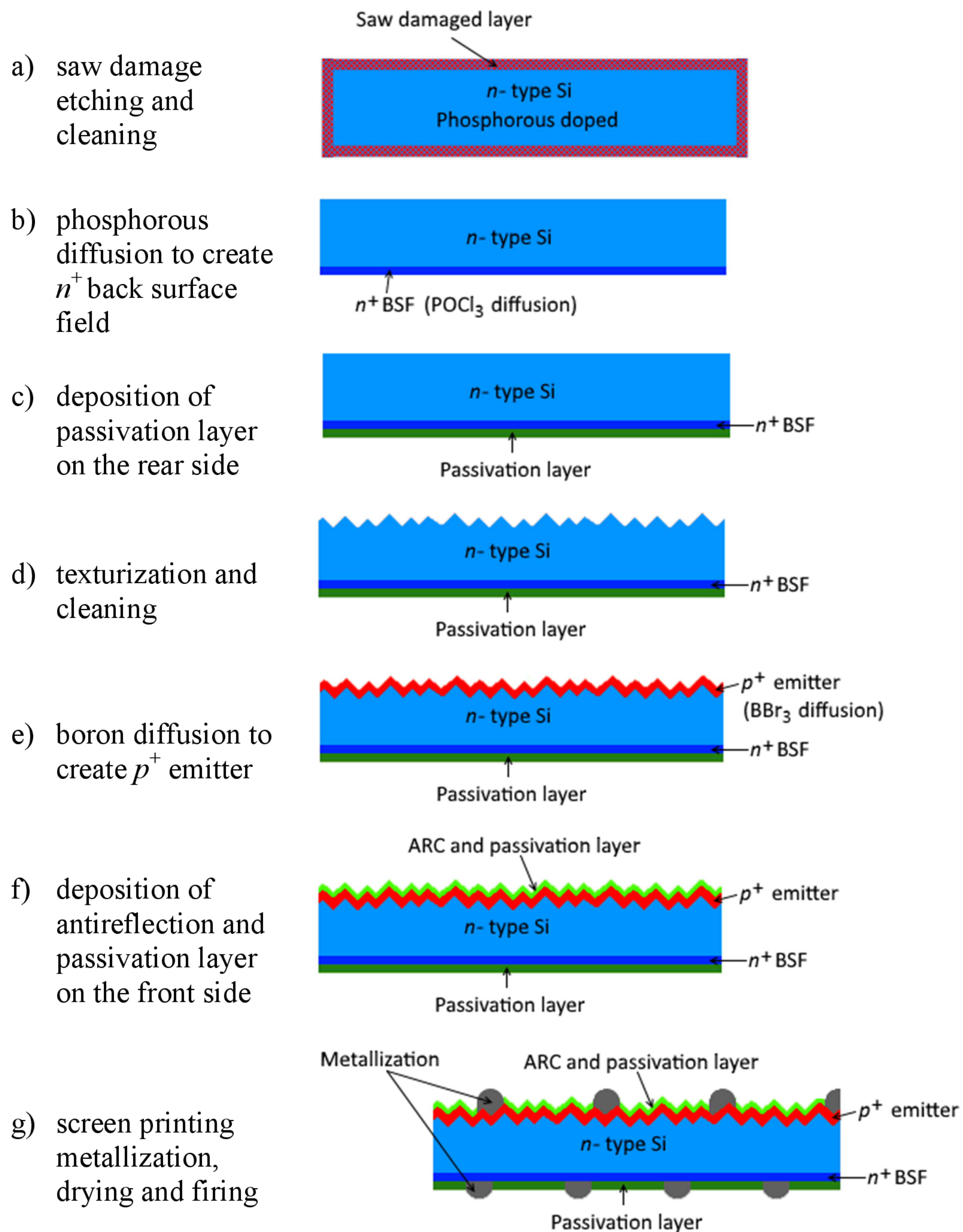


Fig. 10: Standard industrial *n*-PERT solar cell manufacturing process.

1.3.1 Material

The base material for crystalline silicon solar cell production is a high-quality silicon (solar grade purity is 99.9999 %) distinguished into two main classes – monocrystalline or multicrystalline. For the *n*-type solar cells mostly the phosphorus doping wafers from Czochralski grown ingots are used. The most common size used in production is currently 156 × 156 mm^2 for monocrystalline and multicrystalline cells. Because of the

lower segregation coefficient k of phosphor ($k = 0.35$) compared to boron ($k = 0.8$) the range of base resistivity ρ_{base} is higher in case of *n*-type ingots [24] [25].

The doping concertation C_s along the ingot is described by the eq. 1:

$$C_s = kC_0(1 - f_s)^{k-1}\ [cm^{-3}] \tag{1}$$

where C_0 = total doping concentration in the melt; f_s = solidified fraction [26].

The monocrystalline ingots are sliced up into wafers with thickness approximately 180 μm with a wire saw. The crystallographic orientation preferred in the solar cell industry is <100> as this can be easily textured to produce pyramids reducing the surface reflectivity. The wafers from one ingot are divided into sets of 25 pieces. During the production of one solar cells batch, wafer sets coming from one part of ingot are processed. This enables to perform the destructive testing on a few wafers only and it is presumed that the rest of the wafers have the same properties.

Measuring methods used at these production steps

The main parameter of the wafer except for its dimensions is the base resistivity. The *n*-PERT solar cells are made from a material with lower base resistivity (ρ_{base} around 2 Ωcm) whereas for example IBC cell are done using higher-resistivity material (ρ_{base} around 10 Ωcm) [27].

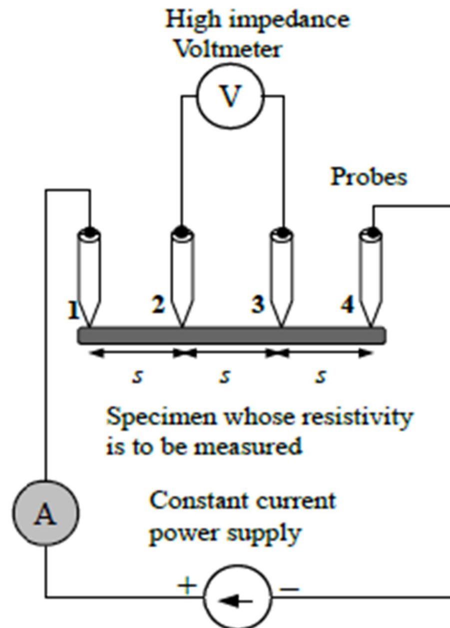


Fig. 11: Four probe method for measuring resistivity of a wafer.

The base resistivity is usually measured on wafers after high-temperature annealing with four-point probe method. During annealing at temperature above 850 °C thermal donors, negatively influencing base resistivity measurement, are annihilated. The

four-point probe method is based on current passing through two outer probes and measuring the voltage through the inner probes [28].

The base resistivity is then calculated using eq. 2:

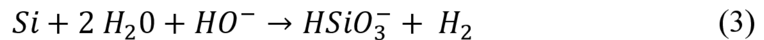
$$\rho_{base} = \frac{V_{fp}}{I_{fp}} \cdot 2\pi s \ [\Omega cm] \quad (2)$$

where V_{fp} = floating potential difference between the inner probes, I_{fp} = current through the outer pair of probes, s = spacing between point probes [29].

1.3.2 Saw damage removal, texturization and cleaning

Silicon wafers contain a surface layer with most of defects and impurities, coming from cutting ingots into silicon wafers by wire saw. Alkaline or acidic solutions, as well as plasma etching, can be used for this saw damage removal (Saw Damage Etch, SDE) at the beginning of the solar cell production. However, the alkaline etch is preferred due to an easier waste disposal of potassium hydroxide (KOH) or sodium hydroxide (NaOH) solutions. After etching the wafer is cleaned to remove metal and organic contaminants that would cause an increase of surface and bulk recombination during the following high-temperature process steps [30] [31] [32].

The SDE using NaOH or KOH results in an optically flat and highly reflective wafer surface (**Fig. 12**). The next step – texturing is done by a reduction of the light reflection. Together with the surface texturing and ARC deposition the overall reflection can be brought down to within 3 % [30]. The wet etching texturing processes are the most frequently used techniques in an industrial production. Type of the etching solution, its composition and process conditions affect texture properties very significantly. The etching reaction can be summarized as:



$$Si + 2\,H_2 0 + HO^- \rightarrow HSiO_3^- + \,H_2 \quad (3)$$

and it takes place in three reaction steps – oxidation of silicon, formation of a solvable salt, and dissolving of the salt in water [31].

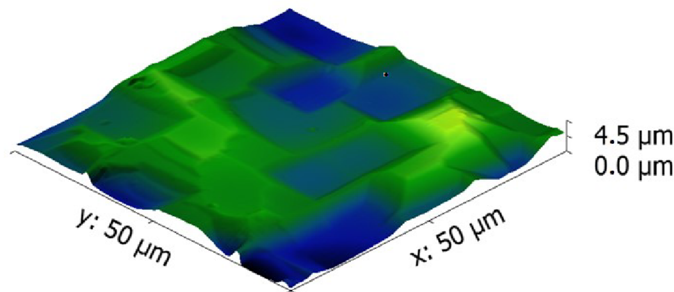


Fig. 12: Monocrystalline silicon wafer after saw damage removal in solution of KOH [32].

The silicon etching rate in alkaline solutions (NaOH, KOH, and tetramethylammonium hydroxide – TMAH) depends on the crystallographic orientation of the silicon substrate.

Etching is faster in the <100> direction than the <111> thereby a typical pyramidal structure for mono-Si substrates is created (**Fig. 13**). The average pyramid size varies from 2 µm to 10 µm and the corresponding reflectivity is in the range from 14 % to 15 %. In general, isopropyl alcohol (IPA) is added to the alkaline etchants to improve the uniformity of the textured surface by removing hydrogen bubbles sticking on the etched surface [33] [30].

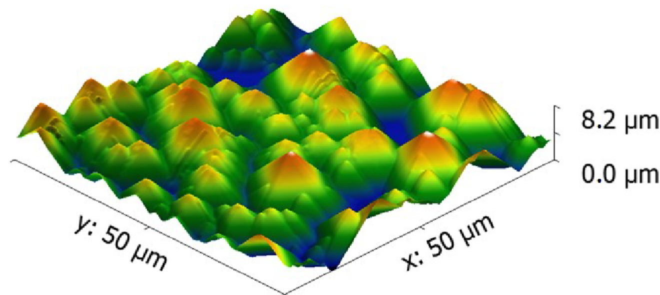


Fig. 13: Monocrystalline silicon wafer after texturing in solution of NaOH [32].

Because of the anisotropic nature of the etching process, it is not very effective for mc-Si wafers. This is caused by distribution of individual grains with different crystallographic orientation on the surface. The total overall reflectance remains in the order of 30 % to 36 %. The uniform texture throughout the surface can be achieved only by acidic isotropic etching, reactive ion etching or by mechanical texturing. In the industry the acidic etching is preferred due to easier implementation to the production line. Acidic texturing is more difficult to control because of the composition change of the etching bath due to the ongoing consumption of the two main components to water and its exothermic nature requiring effective cooling. A temperature-rise can drastically increase the etching rate [34] [30].

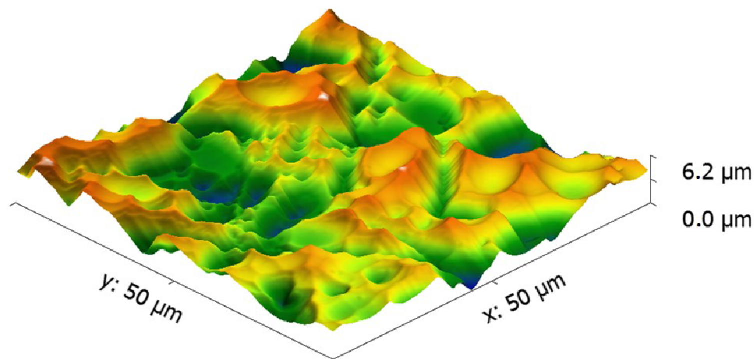


Fig. 14: Multicrystalline silicon wafer after texturing in acidic solution [35].

After saw damage removal and before every high temperature or passivation step one of the cleaning sequences is required. The standard cleaning procedure contains etching in hydrochloric acid (HCl), which removes metal impurities from the wafer surface, and in hydrofluoric acid (HF), which etches the native silicon dioxide off, removes metals with this surface, and forms a hydrophobic surface [31].

For phosphorous diffusion or other high temperature steps this cleaning is sufficient. However, in case of p^+ doped Si the cleanliness of the surfaces before deposition of the passivation layer is extremely important for a good passivation quality. Two cleaning processes with similar levels of surface cleanliness are used – “Piranha” cleaning, mostly used in laboratory style processes, and cleaning in HF/O_3 solution, which is commercialized as an industrial in-line process. “Piranha” bath consists of a solution of hydrogen peroxide (H_2O_2) and sulphuric acid (H_2SO_4), which is creating a thin silicon dioxide (SiO_2) layer on the wafer removing the impurities from the surface. This layer is removed in a second HF dip that removes the SiO_2 formed before [13].

Measuring methods used at these production steps

The quality of texturization, size of pyramids and other parameters related to surface topography can be measured using microscopy techniques, e.g. optical microscopy, atomic force microscopy or laser scanning microscopy [36]. After SDE the minority carrier lifetime τ_{eff} could be measured on samples with chemical passivation using Microwave-detected Photoconductive Decay (μ-PCD, **Fig. 15**). This method is based on the pulse of the laser light, which generates carriers. Excited carriers change the conductivity of a semiconductor. The microwave reflection is related to the change in conductivity, therefore decaying of conductivity is measured. It allows also defect investigation and mapping of wafers (see **Fig. 16**) [37].

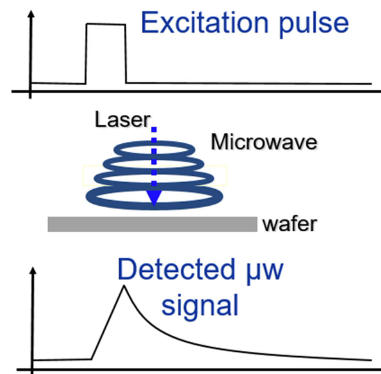


Fig. 15: Principle of Microwave-detected Photoconductive Decay (μ-PCD) method [37].

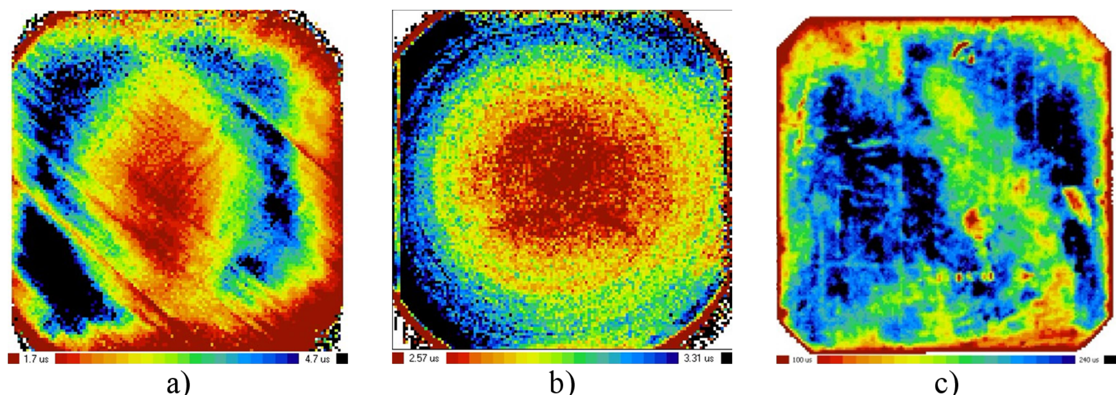


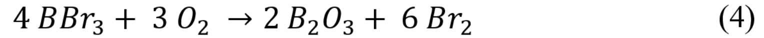
Fig. 16: μ-PCD images of: a) insufficient SDE; b) presence of oxygen; c) good material [36].

1.3.3 Boron diffusion

Creation of *p-n* junction is fundamental for the whole conversion and power generation of a solar cell under illumination. The quality of the emitter is important for achieving higher efficiency, thus it determines mainly the lifetime value resulting in the generated open circuit voltage (V_{OC}).

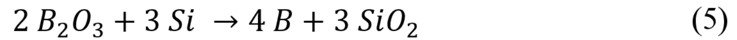
In the industry two main systems are used – ion implantation and high temperature diffusion from liquid source. In the case of using *n*-type silicon substrates the best technology for the industry seems to be batch mode facilities – direct thermal diffusion in open quartz tube furnace using boron tribromide BBr_3 or boron trichloride BCl_3. It is because of the price, cleanliness, homogeneity, and stability of the process [38].

Process of thermal diffusion can be divided into two phases – deposition (pre-deposition) and drive-in. Dopant precursor (BBr_3 or BCl_3) is transported to the silicon wafers via a carrier gas (usually N_2). In the tube the BBr_3-N_2 blend is mixed with O_2 which creates the liquid boron trioxide (B_2O_3) and bromine (Br), see eq. 4 [39] [40].



$$4\,BBr_3 + 3\,O_2 \rightarrow 2\,B_2O_3 + 6\,Br_2 \quad (4)$$

The B_2O_3 reacts with silicon and create the elemental boron and SiO_2 (5). At the silicon surface boron silicate glass (BSG), acting as quasi-infinitive diffusion sources, is formed due to the reaction of SiO_2 with B_2O_3 [39] [40].



$$2\,B_2O_3 + 3\,Si \rightarrow 4\,B + 3\,SiO_2 \quad (5)$$

During the drive-in step a very high concentration of boron occurs at the wafer surface. This results in formation of undesirable Si-B compound (see eq. 6), which is called the boron rich layer (BRL). This BRL layer could be converted during oxidation to B_2O_3 and SiO_2, which leads to formation of BSG [39] [40].

$$Si + 6\,B \rightarrow SiB_6 \quad (6)$$

In in-line facilities the diffusion source is sprayed or printed on the wafer. After drying, the wafer is exposed to heat in an infrared heated conveyor belt furnace [41].

Measuring methods used at these production steps

The main parameter of a diffused layer is the shape of a doping profile, its depth and surface or peak concentration, and emitter sheet resistance R_{Sh}, which depends on the doping concentration and the junction depth. In the case of using the BSG layer as a part of ARC and passivation coating, its thickness and refractive index have to be measured.

The doping profile is usually measured by Electrochemical Capacitance-Voltage (ECV) profiling technique, which enables measurement of the active carrier concentration in semiconductor layers. The technique uses an electrolyte-semiconductor Schottky contact formed on the surface and a reverse bias is applied to incrementally deplete thin

regions of the semiconductor (**Fig. 17**). Depth profiling is achieved by electrochemical etching of the semiconductor between the capacitance measurements where the etched depth can be calculated from the integrated charge of the etching current [42] [43].

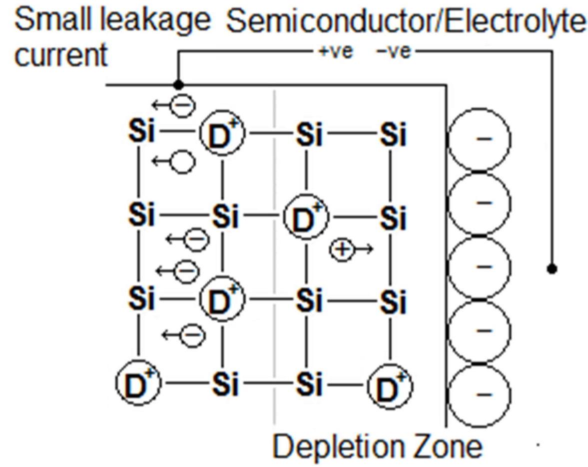


Fig. 17: Carrier's distribution for the *n*-type semiconductor in semiconductor/electrolyte junction under reverse bias [44].

The carrier concentration N is then calculated as:

$$N = -\frac{2}{q\varepsilon_0\varepsilon_r A^2 \frac{dC_{junction}{}^{-2}}{dV_{applied}}} \quad (7)$$

where q = unit charge of the electron; ε_0 = permittivity of the vacuum; ε_r = relative permittivity; A = effective contact area; $C_{junction}$ = measured capacitance; and $V_{applied}$ = bias voltage [42].

There are two main approaches to measure the emitter or BSF sheet resistance R_{Sh} – a traditional four-point probe method (more described in 1.3.1 Material) and a non-contact measurement using light excitation. The four-point probe method is based on a current passing through the outer probes and induces a voltage in the inner voltage probes. The junction between the *n*-type and *p*-type materials behaves as an insulating layer. During the measuring the sample has to be kept in the dark.

One of the non-contact method for sheet resistance measurement is based on the light excitation of the n^+p or p^+n layer structure and pick up of the resulting surface potential by capacitive probes. The detected potential is determined by the sheet resistance of the material (**Fig. 18**). Another method uses the non-destructive eddy current technique. When AC current flows in a coil, its magnetic field induces circulating (eddy) currents in the sample. The eddy current measurement is actually the measurement of the electrical loss in the material. From the distance value and the eddy signal, the sheet resistance value can be obtained (**Fig. 19**) [45] [46].

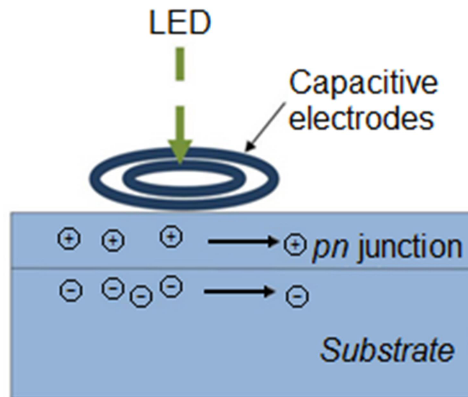


Fig. 18: Sheet resistance measurement based on light excitation and measurement of resulting surface potential [46].

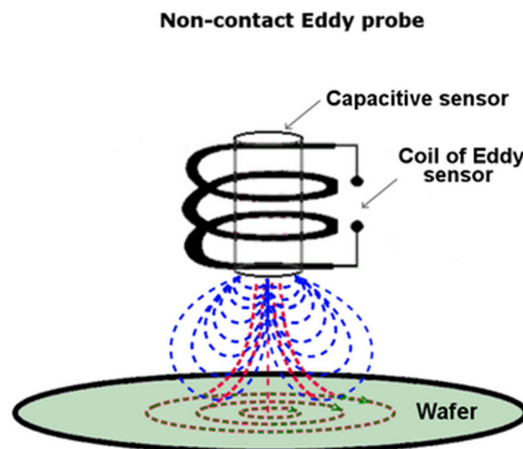


Fig. 19: Sheet resistance measurement based on measurement of eddy current [45].

1.3.4 Comparison of atmospheric and low pressure boron diffusion

The most of diffusion processes take place at atmospheric pressure (AP). However, for high-efficiency solar cell processing the low pressure (LP; pressure range from units to tens of kPa) diffusion seems to be more suitable. Here, the main reasons why low-pressure diffusion is more suitable for industrial production than the atmospheric-pressure diffusion are given:

- The reduced-pressure operating conditions in the tubes prevent over-saturation of the doping sources and result in a more homogeneous flow distribution. To achieve good homogeneity of the layer in the case of atmospheric pressure diffusion it is necessary for the distance between wafers to be 4.3 mm (one pitch) while in the case of low pressure process it is possible to use a boat with a half pitch distance (2.15 mm) between wafers. This results in a greater throughput and to lower costs owing to smaller consumption of gases (see **Tab. 1**).

- When using the low pressure process, it is easier to achieve good homogeneity of diffusion over the wafer and over the boat. It is possible to reach a higher sheet resistance (150 Ω/sq).
- Shorter typical process duration in the case of boron diffusion (AP: > 120 min; LP: 100 min).

The main disadvantage is a higher cost of equipment and the need for fine control of all process parameters.

Tab. 1: The comparison of the gas flow for the atmospheric pressure and the low pressure boron diffusion at Centrotherm furnace.

Type of Gas	Gas flow [slm]	
	Atmospheric pressure	Low pressure
N_2	12	0.3 – 0.5
N_2-BBr_3	0.06 – 0.67	0.06 – 0.07
O_2	0.06 – 0.67	0.06 – 0.07

1.3.5 Back surface field

The presence of a built-in electric field, coming from a higher doped region at the back surface of the solar cell, can improve the cell performance. This back surface field (BSF) minimises the impact of the rear surface recombination velocity on voltage and current if the rear surface is closer than a diffusion length to the junction. The interface between the high and low doped regions behaves like a *p*-*n* junction. An electric field is formed at the interface, which introduces a barrier to minority carrier flow to the rear surface (**Fig. 20**) [36] [47].

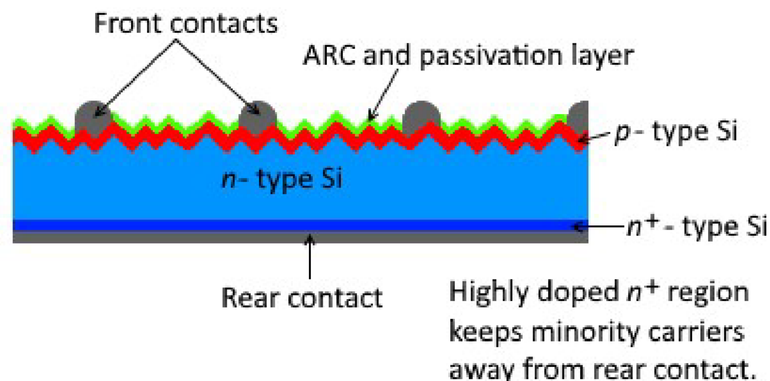
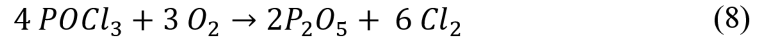


Fig. 20: Principle of the back surface field effect.

Tube furnace diffusion using phosphorus oxychloride ($POCl_3$) as dopant precursor is the dominating BSF formation technology for *n*-PERT solar cells, although the in-line

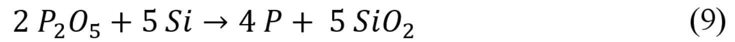
conveyor furnace has been investigated where a spray of phosphorus dopant needs to be sprayed on the wafer surface [48].

The diffusion process in the tube furnace consists of two steps – predeposition and drive in. During the predeposition an N_2 carrier gas is saturated in $POCl_3$ by bubbling through a $POCl_3$ tank before entering a furnace. The P_2O5 is then formed through oxidation as a source of phosphorus [49]:



$$4\,POCl_3 + 3\,O_2 \rightarrow 2P_2O_5 + \ 6\,Cl_2 \qquad (8)$$

The P_2O_5 deposited on silicon is reduced to phosphorus with formation of SiO_2:



$$2\,P_2O_5 + 5\,Si \rightarrow 4\,P + \ 5\,SiO_2 \qquad (9)$$

These reactions result in formation of phosphosilicate glass (PSG) on the silicon surface, as well as provide phosphorus atoms, which diffuse into silicon. During the drive-in the PSG acts as the source of phosphorus atoms thus the uniform formation of the PSG across the wafer is important while PSG acts as an infinite source of phosphorus [48] [49].

1.3.6 Passivation and antireflection coating

The surface of silicon wafer can be imagined as a big crystal defect. Due to non-saturated “dangling” bonds, a large density of defects “surface states” within the bandgap exists at the surface of the crystal. These defects are highly prone to different recombination mechanisms and lead to a significant reduction of the effective minority carrier lifetime and so to a lower conversion efficiency of solar cells. Therefore all surfaces need to be passivated in order to reduce the recombination activity and to prolong the charge-carrier effective lifetime. Surface passivation is achieved by using two complementary approaches – with field effect passivation, described in the previous chapter 1.3.5 Back surface field, or using chemical passivation which reduces the density of defect states in the bandgap [50].

The passivation layer also works as an antireflection coating (ARC). The thickness of the ARC layer is chosen so that the wavelength in the dielectric material is one quarter of the wavelength of the incoming wave (area of maximum photosensitivity: ca. 400 – 1100 nm). The basic calculations are usually done for the wavelengths around 600 nm, because it is close to the peak power of the solar spectrum [51]. The optimum thickness of ARC layer d_{ARC} can be calculated by:

$$d_{ARC} = \frac{\lambda_0}{4\,n_{ARC}} \qquad (10)$$

where n_{ARC} = refractive index of ARC material; and λ_0 = free-space wavelength [52].

Reflection is further minimized if the refractive index of the ARC layer is the geometric mean of that of the materials on either side; that is glass or air, and the silicon. A further reduction in reflectivity is achieved through a double layer antireflection coating [52].

There are different materials used as the passivation and antireflection layer for the *n*-type silicon (alone or in combination to get the double ARC coating). The most often used materials are hydrogenated SiN_X with amorphous character (a-SiN_X:H) deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) or SiO_2 created by thermal wet or dry oxidation. Other possibilities are materials TiO_2 or Ta_2O_5, Si_3N_4 deposited by Low Pressure Chemical Vapour Deposition (LPCVD), or PECVD SiC_X (a-SiC_X:H) [53] [51].

The *p*-type silicon wafers cannot be passivated with pure SiO_2 or PECVD SiN_X. The SiO_2 is unusable due to the high boron solubility combined with the presence of a small fixed positive charge density. Alike the PECVD SiN_X does not passivate highly doped *p*-type material due to the high concentration of build-in positive charges. As the most promising technology seems to be coating with Al_2O_3 synthesized by atomic layer deposition (ALD) or PECVD. Another approach is based on using an intermediate SiO_2 or Al_2O_3 layer between SiN_X and the *p*-type layer. Also alternatives such as a-Si:H and a-SiC_X:H are under the development [53] [54].

After deposition, an annealing at temperatures around 300 – 750 °C for several minutes is necessary in order to reach a good surface passivation. Usually the air or nitrogen atmosphere is used or the annealing can be done in forming gas atmosphere. A possible explanation for the need of the annealing step is the diffusion of hydrogen to the silicon interface and a saturation of the dangling bonds for H_2 containing dielectrics [55].

Measuring methods used at these production steps

The implied open circuit voltage (iV_{OC}) has been used for the evaluation of the passivation quality since it has been proven that this parameter can predict the open circuit voltage of the finished solar cell very accurately. It is a parameter determined from the carrier concentration at the edge of the depletion region. To measure iV_{OC} the Quasi Steady State Photoconductivity method (QSSPC) is often used. This photoconductance-based contactless measurement technique uses a RF sensor to measure sheet conductivity of the sample and a light sensor to measure intensity of the flash with a whole light spectrum to which sample is exposed. These measurements are then used to calculate the effective carrier lifetime of the samples [56] [57].

The iV_{OC} is calculated from the photoconductance measured at 1 sun illumination using:

$$iV_{oc} = \frac{kT}{q} \ln \left[\frac{(N + \Delta n)\Delta n}{{n_i}^2} \right] \tag{11}$$

where k = Boltzmann's constant; T = temperature; q = unit charge of the electron, N = dopant density, Δn = injection level calculated from the sheet photoconductance under 1 sun illumination; n_i = intrinsic carrier concentration.

The ellipsometry is an indirect method used for measurement of thickness and refractive index of a thin layer – in this case of passivation and ARC layer. It is based on the measurement of change in light polarization (amplitude ratio ψ and phase difference Δ) when light reflects or transmits from a material structure (**Fig. 21**, **Fig. 22**) and compares it to a model. The incident light wave is linearly polarized, when the light wave reflects off the surface, the polarization changes to elliptical polarization, thereby the name "ellipsometry". The form of the ellipse can be measured by a detector and data processing can relate this to the ellipsometric parameters ψ and Δ [58] [59].

To get the thickness and refractive index, a layer model must be established, which considers the optical constants and thickness parameters of all individual layers of the sample, including the correct layer sequence. Using an iterative procedure, unknown optical constants and/or thickness parameters are varied, and ψ and Δ values are calculated using the Fresnel equations. The calculated values, matching the experimental data the best, provide the optical constants and thickness parameters of the sample. Thus the thickness of thin layer deposited on top of substrate can be calculated only when the refractive indexes of the film and substrate are known (**Fig. 23**) [58] [59].

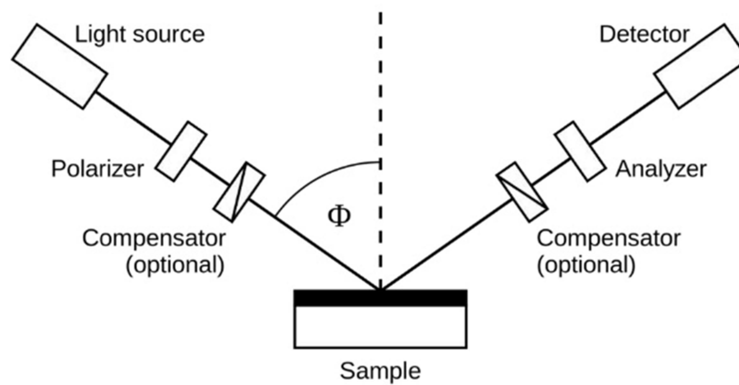


Fig. 21: Schematic setup of an ellipsometry measurement [59].

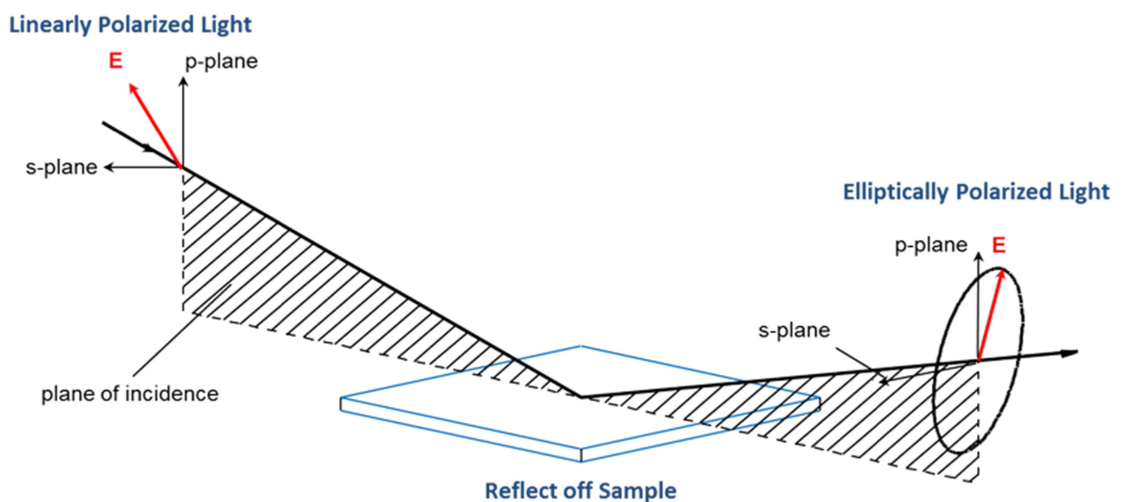


Fig. 22: The general principle in ellipsometry [59].

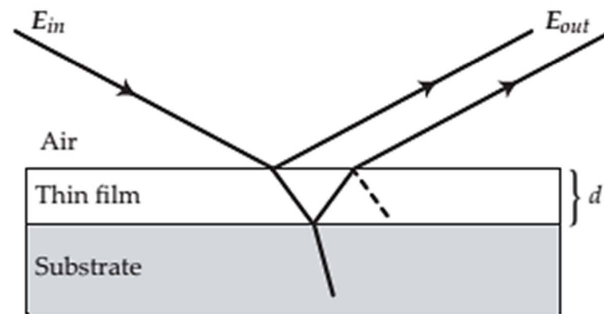


Fig. 23: Simplified model of thin film measurement on the top of crystal [58].

1.3.7 Metallization

The last step of the solar cell production is the application of metal contacts. A screen-printed metallization is still the dominant technique in solar industry for contacting crystalline silicon solar cells due to its simplicity, high throughput, and low price. The main requirements for contacts are low contact resistance to silicon, low line resistance, a negligible effect on the substrate, good line resolution, solderability, good adhesion, and a low price.

Identically to other industrial screen-printing processes at electronics the metallization is printed with conductive thick-film pastes. These pastes are mostly silver (Ag) pastes based on a glass system suitable to fire through the passivation layer during a rapid thermal process. Using a glass frit with low transformation temperatures (typically lead-borosilicate glass) allows peak firing temperatures below $\vartheta_{peak} = 850°C$. In addition to that the pastes specified for contacting *p*-type silicon contain usually aluminium (Al) to form a direct crystallite contact during the firing process [60] [61].

Owing to the short firing cycles, sintering kinetics gains a huge impact on the microstructure formation. The simplified model of contact formation is shown in **Fig. 24**. During the firing, the organic ingredients of the paste are thermally decomposed; the glass frit melts and wets the wafer surface. The fluidized glass frit etches through the ARC and passivation layer and gets into direct contact with silicon. The Ag crystallites then precipitate onto the Si surface upon cooling. Their shape is defined by the Si crystal orientation-dependent back-bonding strength. Thin glass layers are typically embedded between the silicon surface, Ag crystallites, and the sintered metal finger. Current paths are provided by means of multistep tunnelling into the metallization across nano-Ag colloids in a glass layer close to the emitter or through the Ag crystallites or possibly in direct contact with the silver finger (**Fig. 25**) [60] [61] [62] [63].

Fire-through metallization often yields macroscopically non-uniform contact quality over the cell area, degrading the cell performance and causing cell-to-cell variations of the conversion efficiency in a cell production line. This is called “grey finger” phenomenon. As one possible cause of non-uniform contact resistance was recently proposed to be the short circuit spots that were formed during contact firing Ag paste. These spots were located between the silver grid and the emitter. [64].

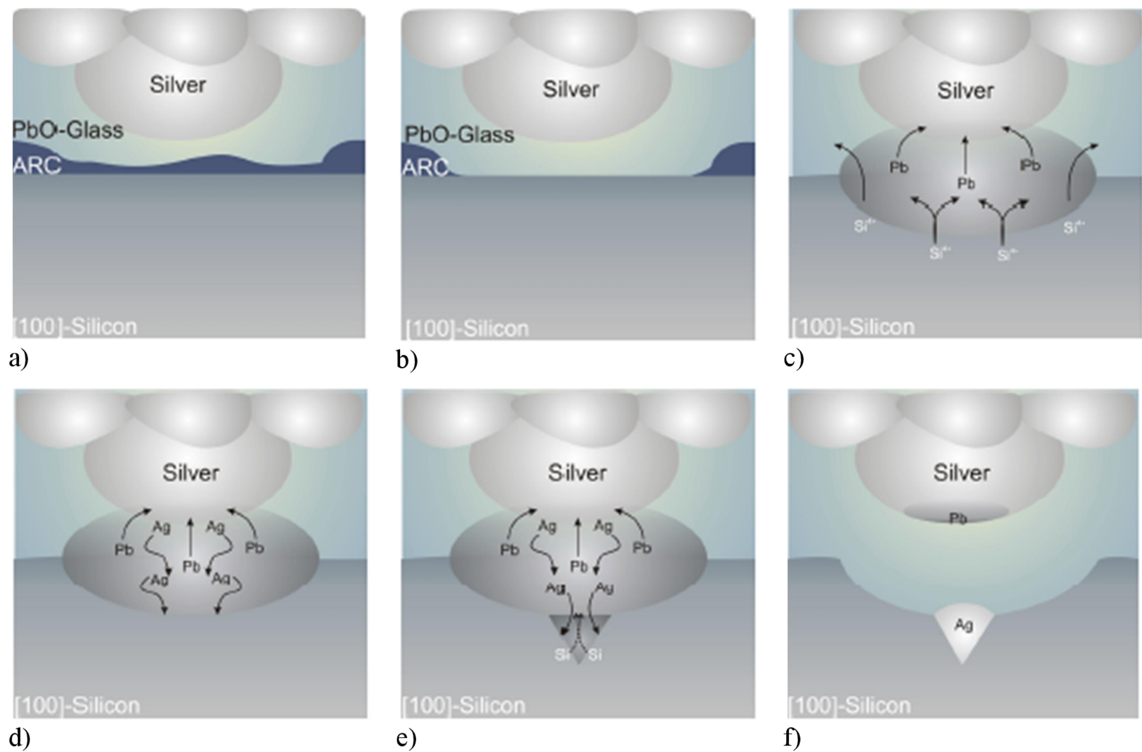


Fig. 24: Simplified model of contact formation: a) schematic cross section of Ag thick film paste on <100> Si after combustion of organics; b) glass etches through SiN_X layer; c) redox reaction between Si and glass, lead (Pb) is formed; d) liquid Pb starts to melt Ag; e) Ag-Pb melt reacts with Si, inverted pyramids are formed; f) on cooling down Ag recrystallises on <111> Si planes [60].

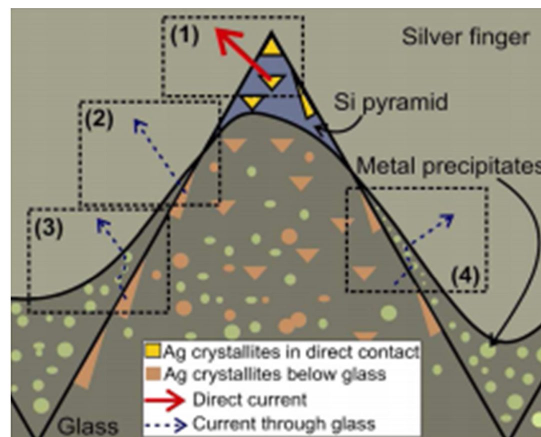


Fig. 25: Possible current transport mechanisms in alkaline textured silicon solar cells: (1) direct current transport and (2)–(4) current transport through glass [65].

Measuring methods used at these production steps

A lot of different measurements can be done on finished metallized solar cells to characterize their properties, such an IV measurement, electroluminescence, photoluminescence, or internal/external quantum efficiency.

A solar simulator is typically used for IV measurements to get a current voltage curve under forwards bias and illumination, where the current of the solar cell is plotted against the applied voltage. Main parameters obtained by this measurement are short circuit current (I_{SC}), open circuit voltage (V_{OC}), maximum power (P_{max}), fill factor (FF) and conversion efficiency (η). The V_{OC} of the solar cell is the maximum voltage that the solar cell will supply – it is the voltage without any load applied. The J_{SC} is the maximum current of the solar cell under conditions of a zero resistance load - a free flow or zero volt potential drop across the cell. The FF and η are metrics used to characterize the performance of the solar cell. The fill factor is defined as eq. 12. The conversion efficiency is defined as the ratio of P_{max} to the product of the input light irradiance (E) and the solar cell surface area (A_{cell}) (see eq. 13) [66]:

$$FF = \frac{P_{max}}{V_{OC}\, J_{SC}} \qquad (12)$$

$$\eta = \frac{P_{max}}{E\, A_{cell}} \qquad (13)$$

The "quantum efficiency" is the ratio of the number of carriers collected by the solar cell to the number of photons of a given energy incident on the solar cell. The "external" quantum efficiency (EQE) of a silicon solar cell includes the effect of optical losses such as transmission and reflection. “Internal” quantum efficiency (IQE) refers to the efficiency when photons are not reflected or transmitted out of the cell. By measuring the reflection and transmission of a cell, the external quantum efficiency curve can be corrected to obtain the internal quantum efficiency curve. This measurement is performed by impact of a monochromatic light beam onto the sample and recording the photocurrent generated as a function of the wavelength. The beam power of the probe is characterised using a detector of known responsivity (AW^{-1}). Subsequent measurement of the photocurrent generated by the device under test as a function of wavelength allows for the determination of spectral responsivity [52] [67].

Electroluminescence (EL) is a useful characterisation technique as it is fast, non-destructive and sensitive to the material and process defects – e.g. effects of shunt or series resistance and recombination parameters are clearly visible. The infrared light emitted by biased solar cell is detected with CCD camera. There is a proportional relationship between the intensity of the emitted light and the number of minority carriers in the base layer, thus giving information on intrinsic and extrinsic cell parameters influencing them, e.g. minority carrier lifetime, and diffusion length. The light output increases with the local voltage so that regions with poor contact show up as dark, so the resistive losses like series and shunt resistances are visible as areas of

lower intensity in the EL image. Other defects like micro cracks and broken contact fingers are also easily identified in the EL images [52] [68].

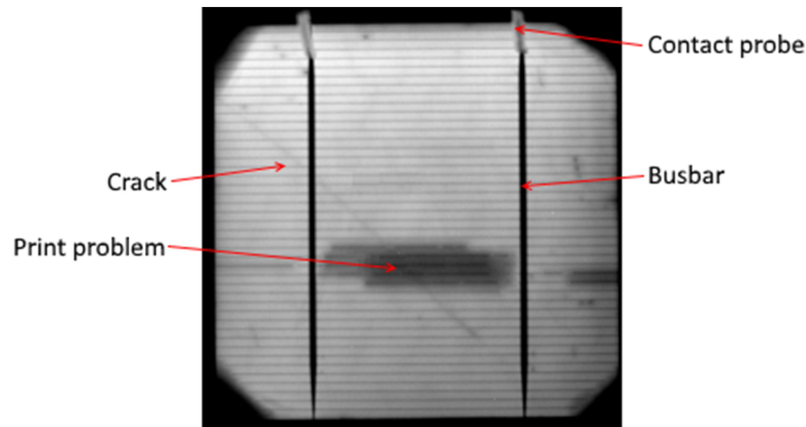


Fig. 26: Example of EL image of a monocrystalline silicon wafer. The intensity of the light given off is proportional to the voltage. Poorly contacted and inactive regions show up as dark areas. The micro crack and printing problem are not detectable with visual inspection [52].

Photoluminescence (PL) is a contactless and non-destructive imaging method, which can be applied to both unfinished and fully processed silicon solar cells of any practical size. PL imaging uses external optical excitation with single wavelength, which stimulates spontaneous emission of light from the homogeneously illuminated sample. This emitted light, associated with the semiconductor bandgap, is detected with an infrared camera. Lower counts in a PL image usually indicate regions with lower electrical quality, such as lower minority carrier lifetime and local shunts. This way, the PL can detect and highlight various types of defects in the material of solar cell, characterize the bulk quality, or quantitatively imagine the distribution of the local series resistance and of the local saturation current density [69] [70].

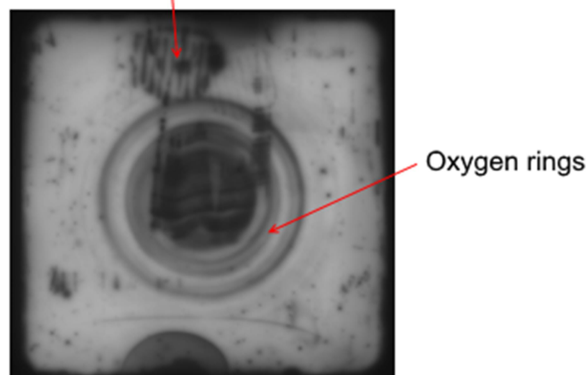


Fig. 27: Example of PL image of silicon wafer after annealing.

1.4 Potential induced degradation

The Potential Induced Degradation (PID) is an undesirable phenomenon at solar cell modules occurring in the photovoltaics systems due to high-voltage stress across the module layer stack between framing/glass surface and solar cells and leads to significant power losses (**Fig. 28 a**). This high-voltage stress may cause leakage current between the solar cells and the module frame through the front glass and encapsulation, being responsible for degradation effects [71]. The polarity of voltage causing PID depends on the type of module (**Fig. 28 b**). The factors that enable PID (voltage, heat and humidity) exist on all photovoltaic systems, but the effect does not occur on all or even most of PV systems.

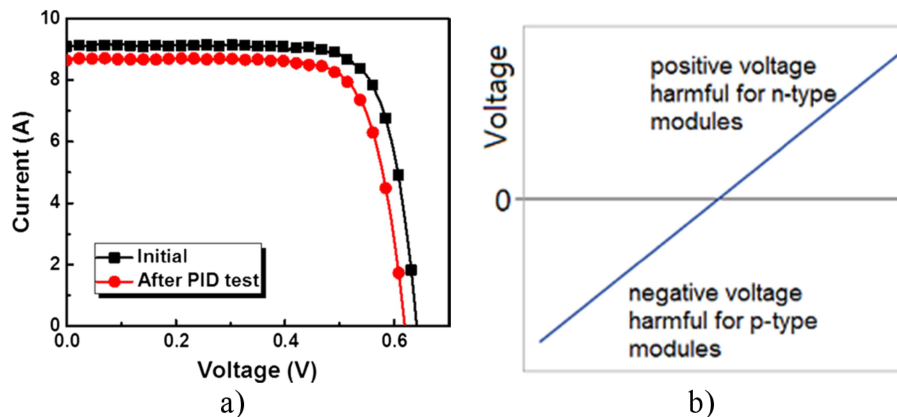


Fig. 28: IV curves of the n-type silicon solar cell before and after the PID test; b) dependence of voltage causing PID on the type of collar cell [72].

The leakage current origins from the cell to the earth (**Fig. 29**). As a result, over time a negative charge is left on the front surface of the solar cells, which activate the surface transistor, attracting positive charge carriers to the front surface where they recombine with electrons and are lost. These charge carriers will therefore not contribute to the conduction of the solar cells which results in efficiency decreases [72].

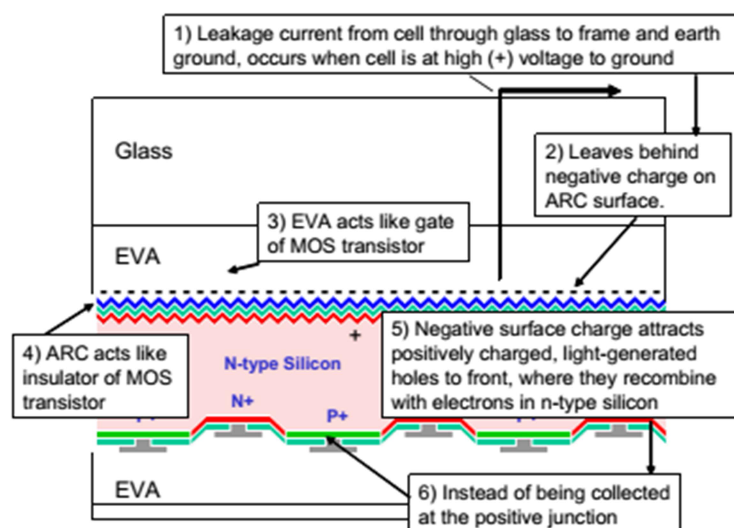


Fig. 29: PID degradation process of *n*-type solar panels [73].

2 Goals of the dissertation

This dissertation is oriented on bifacial solar cells based on monocrystalline silicon *n*-type material. The aim of this work was to prepare high efficiency photovoltaic cells based on the *n*-type substrate using the standard production line, which have originally been designed for production on *p*-type substrates. Resulting cells could be used in standard as well as advanced bifacial applications. As it was mentioned before, the *p*-type substrate technology was very well elaborated in past decades, whereas technology of solar cells based on the *n*-type substrate encounters problems caused by different material parameters of the *n*-type substrate comparing with the *p*-type substrate. Therefore, this enhances new structures that need a new approach in use of standard or new materials and their combinations.

The experimental work took place at the ISC Konstanz in Germany where a pilot-scale manufacturing line for production of solar cells in various types, including technologies based on both – *p*-type and *n*-type material, is placed. Research teams at the ISC Konstanz are focused on developing of methods leading to increase efficiency of solar cells manufactured at standard industrial devices, which have been mostly set up for *p*-type-based production. The production line there is based on batch processes.

The production of a photovoltaic cell consists of many steps, which often influence one another. Therefore, for the successful development of the solar cells structure using the *n*-type substrate and implementation of new particular process steps leading to the high efficiency solar cells it is indispensable to reach following goals in technology design and validation.

1) New ways of diffusion and oxidation processes

   Diffusion processes affect the crystal structure near the surface and hence the magnitude of the fixed charge and the increased or decreased intensity of surface processes. Selection between available types of diffusion processes is therefore needed and the influence of both dry oxidation and wet oxidation processes should be studied.

   Further, evaluation of possible interactions between diffusion and oxidation processes is indispensable. Also the influence of low pressure and atmospheric pressure boron diffusion on resulting parameters of the cells should be investigated. The resulting structure will be a compromise between the optimal profile of boron diffusion (its shape, depth, sheet resistance etc.), good passivation properties and low contact resistance.

2) Design of the optimal structure of passivation layers and antireflective coating

   Good properties of the used passivation and ARC layer are essential for the reduction of the recombination losses and preservation of the light trapping effect. The passivation and ARC structure is in case of *n*-type cells more

complex than in the case of the classic *p*-type solar cell as it is a combination of a layer separating p^+ boron emitter and the antireflective layer (see chapter 1.3.6). Usually, SiO_2 or BSG serves as the separating layer between SiN_X and the boron emitter and its optimal thickness must be investigated and thereafter ensured.

Further, refractive index of the ARC layer is the carefully monitored parameter. Consequently, the dependence of refractive index on stoichiometry of deposited layers, density of the layers and interface states, as well as the amount of positive interface fix charges on respective process parameters and on the deposition rate must be investigated.

Special attention should be paid to creating an optimal back surface field configuration by means of the n^+ BSF layer prepared by phosphorus diffusion. Passivation SiN_X layer has here the same function as on the front side. Nevertheless, both SiN_X layers, for the front and the rear side, will have different parameters. Therefore two deposition processes, that is, for the front and rear side must be investigated.

3) Minimization of energy losses caused by contact resistance

   There are many factors having influence on resulting properties of contacts. The most important ones are the type of texturization, the topology of contacts, the sequences of printing processes, the material composition of the paste, the temperature profile during contact firing, the boron emitter concentration and the doping profile.

   As contact phenomena are very complex they are influenced not only by firing process but also by thickness of passivation and ARC layer and by printing processes and topography of the contacts. Apart from the composition of contact material also influence of oxygen concentration during the firing process must be well explored.

   The temperature required for burning through the passivation and ARC layer could be derived by in-situ resistance measurements and from the resistance profile which results from resistance measurements. Using the in-situ resistance measurement method brings the possibility of relatively accurate capture and description what happens during firing of contact structures. The goal is to record resistance changes during firing of metallization under different conditions and determine the temperature required for burning through the dielectric layer.

4) Minimization of the short-circuit effects

   In photovoltaic cells short circuits occur as a result of structural disorders. These disorders can origin in almost all production steps. Therefore, the occurrence of short circuits could be a measure of the quality of the production processes. For suppression of short circuit effects, the attention must be paid to the processes

taking place during the contact firing, to surface topographies of the contacts, to thickness of SiN_X layer and also to doping concentration and doping profile.

5) PID prevention at the solar cell level

   To ensure the reliability of prepared photovoltaic cells and their durability in solar panels, cell protection with respect to the Potential Induced Degradation (PID) must also be addressed. As an addition to the above-mentioned technological steps ensuring high cell efficiency here the results are important in practical use of the cells.

   According to literature, the prevention of Potential Induced Degradation could be solved at the cell level using a special composition of ARC and passivation layer, deposited on flat/textured emitter. Optimal ARC and passivation stack preventing PID must ensure good passivation and optical properties to preserve the cell efficiency at the same time. There it is necessary to determine how this effect is influenced by the composition of ARC and passivation layers, by the concentration profile of boron emitter and by the type of the surface texture.

3 Results

Cost competitive industrial production of high efficiency *n*-type solar cells is based on using low-cost techniques with high throughput such as the thermal diffusion in the quartz tube, CVD processes used for deposition ARC and passivation layer and screen printed metallization.

The following chapters describe experiments conducted with the aim to increase *n*-PERT solar cell efficiency or to better understand the mechanisms of contact formation. In order to achieve better description continuity, the chapters are arranged according to the production process, not as the experiments were conducted. This structure was chosen because there are many process and technologic steps and standard arrangement (motivation, experiments, and results) would make reading much harder.

3.1 Boron diffusion

Boron diffusion is required to form the emitter and thus it is one of the most crucial steps in the production. One of many problems impeding industrial production is realization of the emitter on the substrate. The most applicable technology seems to be direct thermal diffusion in quartz tube furnace using BBr_3 or boron trichloride (BCl_3) due to the price, cleanliness, homogeneity, and stability of the process [13] [53] [39]. Since without presence of a quality emitter it makes no sense to make improvements on higher stacks of solar cells, this chapter is dedicated to optimizing a doping profile and comparison of different processes used for its production.

Within chapter 3.1.1, the influence of boron emitter properties (surface carrier concentration, depth, and sheet resistance) on the final solar cell parameters (V_{OC}, J_{SC}, FF, and efficiency) is presented. These parameters are the main indicators of solar cell efficiency. Chapter 3.1.2 deals with possibility of replacing dry oxidation with a wet oxidation process using low pressure diffusion of BBr_3 with regard to the solar cell production. Under the terms of this experiment the suitability of replacing atmospheric boron diffusion with low pressure process was done.

3.1.1 Optimization of emitter doping profile

The following chapter describes the optimization of boron diffusions from a liquid BBr_3 source in a tube furnace. The low-cost metallization technique used in industry – screen printing and firing through – limits the open-circuit voltage V_{OC} due to high recombination losses at p^+ diffused emitters [74] [75] [76]. The following experiment was carried out to establish better diffusion profile than the previous "standard" which enables to gain high efficiency even if the screen printing is used.

To optimize the boron emitter doping profile for screen-printed solar cells, we used 6-inch *n*-type monocrystalline Si wafers with as-cut base resistivity ρ_{base} 2.5 – 3 Ωcm, measured before any processing to include the influence of thermal donors. The wafers were textured using wet chemical alkaline process, followed by cleaning in HCl, HF, and Piranha solutions. In the next steps diffusion in quartz tube furnace containing $POCl_3$ or BBr_3, followed to create n^+ BSF layer with average sheet resistance

R_{Sh} 75 Ω/sq, or p^+ emitter with various parameters described in the next statement. Afterward, the deposition of thermal SiO_2/SiN_X stack by PECVD was done, followed by screen-printing of the silver finger grid on both sides. The cell process was finished by drying and co-firing in an infrared heated belt furnace. The testing structure is shown in **Fig. 30**.

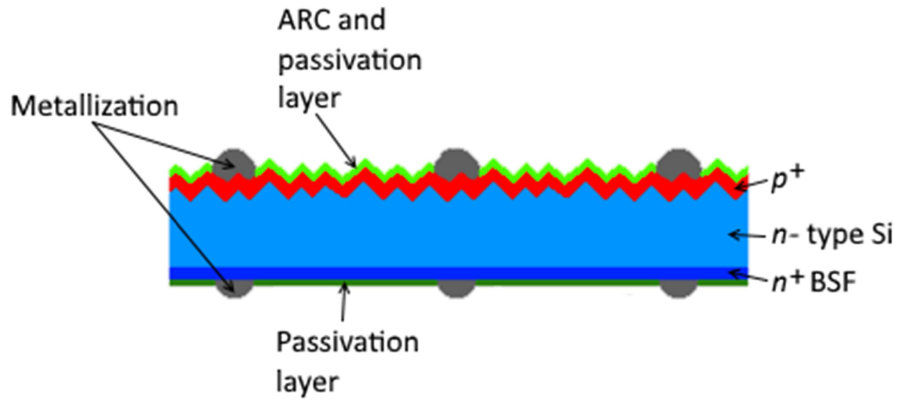


Fig. 30: Schematic cross-section of the samples.

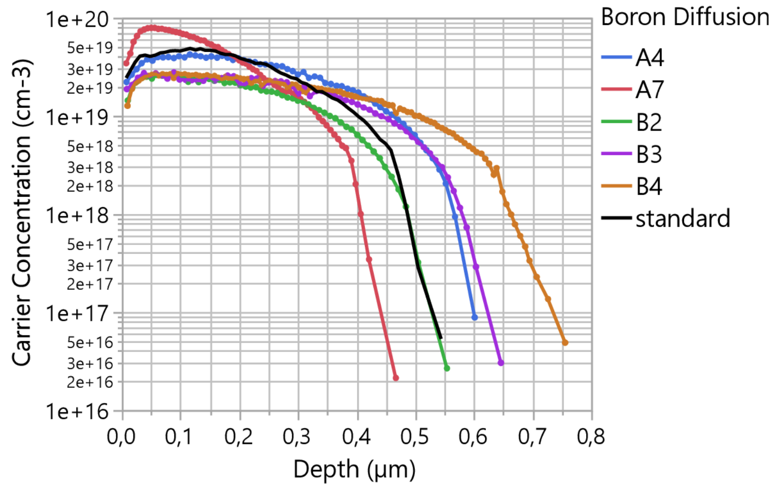


Fig. 31: Doping profiles of boron emitters measured by ECV at central position of the boat. Profiles B vary in the junction depth $d_{emitter}$ whereas profiles A vary in the peak concentration $N_{A\ peak}$ and junction depth.

For this study, boron emitters with different emitter doping profile and resulting sheet resistance were realized to see which parameter had more significant influence on final parameters of the solar cell, see **Fig. 31** and **Tab. 2**. The profiles named B2, B3, B4 had the same surface concentration ($N_{A\ peak} \approx 2.5 \cdot 10^{19}$ cm^{-3}) and they differed from each other in the emitter depth $d_{emitter}$. The profile A4 has same depth as B3, but with higher surface concentration ($N_{A\ peak} \approx 4 \cdot 10^{19}$ cm^{-3}). The profile A7 is the shallowest profile with the highest surface concentration of boron ($N_{A\ peak} \approx 8 \cdot 10^{19}$ cm^{-3}). However, the sheet resistance of the profile A7 was almost the same as A4. The "standard" emitter

profile had the same depth as the profile B2 but with higher surface concentration ($N_{A\,peak} \approx 5.0 \cdot 10^{19}$ cm^{-3}).

The carrier concentration profiles (**Fig. 31**) of these emitters were measured by the electrochemical capacitance-voltage (ECV) method [42] at wafers in the central position of the boat. The decrease in the boron concentration near the BSG-Si interface was caused by different segregation coefficients of B-Si and B-SiO_2 – the boron accumulates more in the SiO_2 than in the top Si layer, which leads to the surface depletion. The emitter sheet resistance R_{Sh} (**Fig. 33**) was measured using the four point measurement method on 5 wafers, coming from different positions over the boat, (**Fig. 32**) in 5×5 points per wafer. The maximum deviation of sheet resistance did not exceed 5 %, which is one of the requirements needed for good quality of metallization.

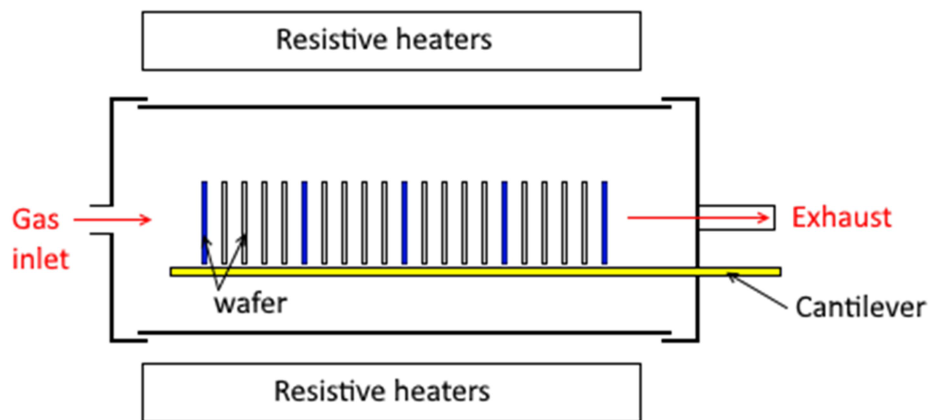


Fig. 32: Schematic drawing of diffusion boat. Blue highlighted wafers were used for sheet resistance measurement.

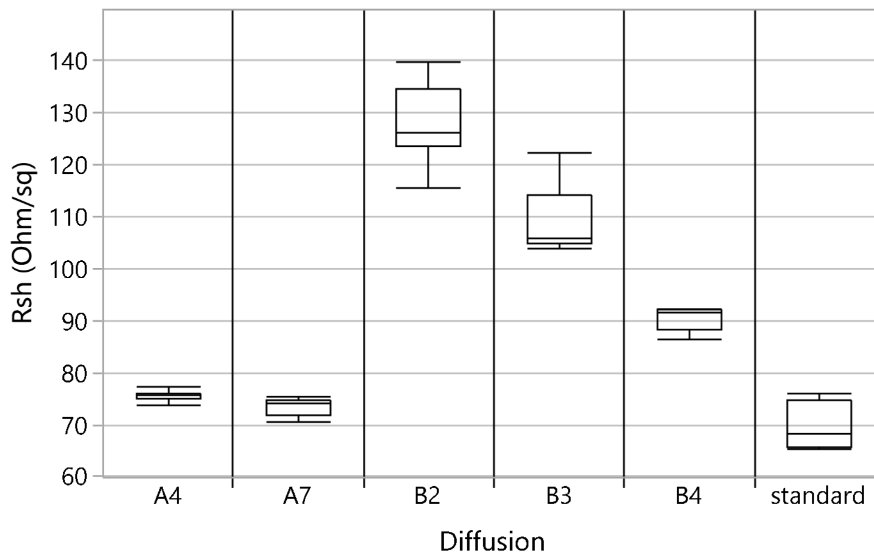


Fig. 33: Sheet resistance R_{sh} was measured using four point measurement method at 25 points per wafer.

Tab. 2: Overview of used boron diffused emitter profiles.

Doping profile	R_{Sh} [Ω/sq]	$d_{emitter}$ [µm]	$N_{A\ peak}$ [10^{19} cm^{-3}]
A4	76	0.60	4.1
A7	74	0.44	7.9
B2	127	0.53	2.5
B3	105	0.62	2.5
B4	91	0.73	2.5
standard	70	0.53	5.0

Before printing the metallization grid, but after a firing step, the implied V_{OC} and dark saturation current density J_0 of the samples were measured using QSSPC to see how the passivation quality of PECVD SiO_2/SiN_X stack is influenced by the shape of the doping profile. Values of iV_{OC} and J_0 were obtained at 1 sun illumination and at injection level of $\Delta n = 3 \cdot 10^{15}$ cm^{-3}. The measured values of each sample are compared in **Fig. 34**.

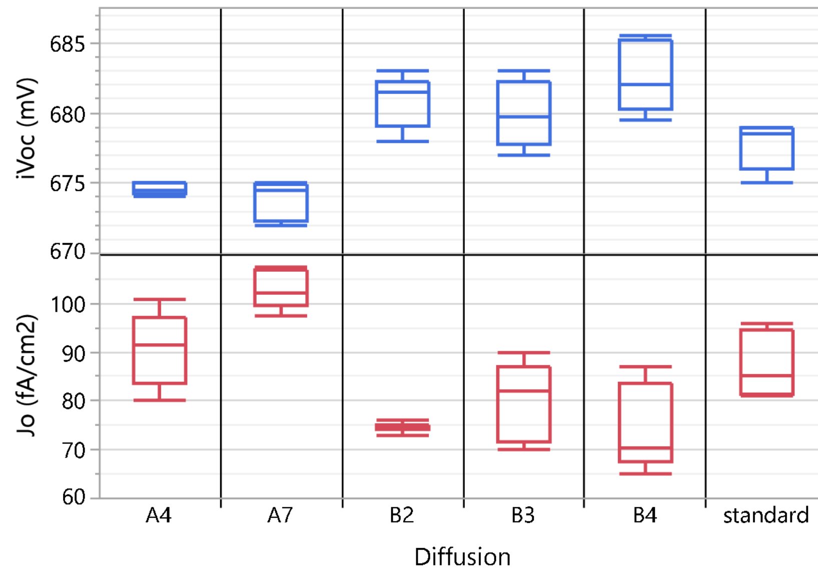


Fig. 34: iV_{OC} at 1 sun and J_0 of the cell precursors (before metallization). The J_0 was extracted at an injection level of $\Delta n = 3 \cdot 10^{15}$ cm^{-3}.

From the iV_{OC} and J_0 results measured on cell precursors it is obvious that profiles with lower emitter surface concentration and higher sheet resistance (B2 – B4) give better passivation (higher iV_{OC} and lower J_0) compared to the profiles A4, A7, and the standard with higher surface concentration. Also, the emitter depth has a less significant influence on the passivation quality on cells without metallization. The best passivation (iV_{OC} = 682 mV, J_0 = 73 fA/cm^2) was achieved on profile B2 with low surface concentration ($2.5 \cdot 10^{19}$ cm^{-3}), shallow emitter ($d_{emitter}$ = 0.53 µm), and thus high sheet resistance (127 Ω/sq). The worst passivation quality of profiles A and the standard with higher surface concentration was caused by the increased recombination. This

recombination came from a stronger band-gap narrowing and thus a higher effective intrinsic charge carrier density.

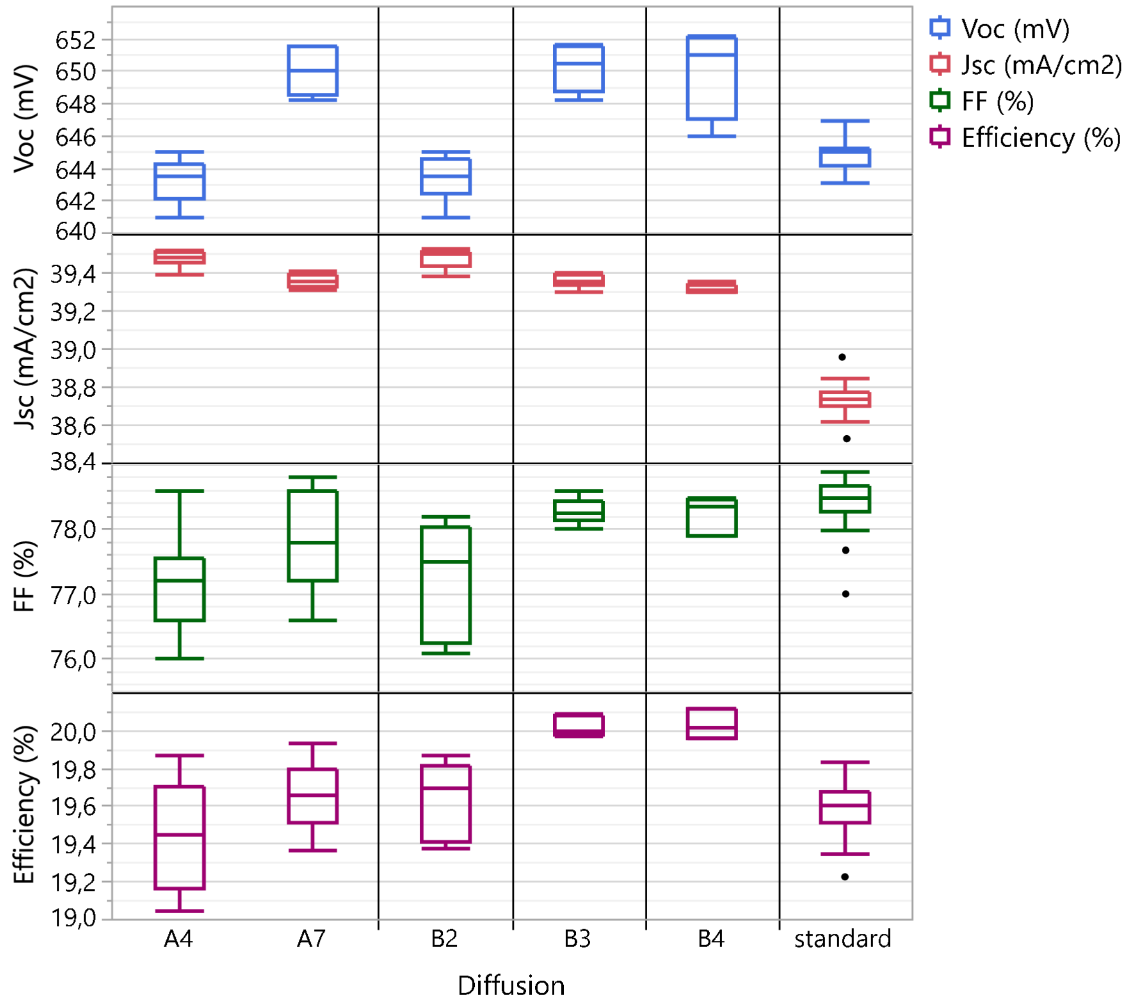


Fig. 35: Solar cell parameters obtained by IV measurement at 25 °C and under AM 1.5 spectrum with illumination intensity of 1000 W/m^2.

The metalized solar cells were examined by IV measurements to determine the values of short-circuit current (J_{SC}), V_{OC}, fill factor (FF), and efficiency. These results are shown in **Fig. 35**. The solar cells were measured under AM 1.5 spectrum with illumination intensity of 1000 W/m^2 and temperature of 25 °C. The samples with doping profile B3 and B4 achieve the lowest J_{SC} and the best V_{OC}, efficiency, and fill factor (B3: 39.4 mA/cm^2 and 650 mV; B4: 39.3 mA/cm^2 and 650 mV). The high value of J_{SC} (39.5 mA/cm^2) in the case of samples with doping profile B2 and low V_{OC} (643 mV), related to this value, is caused by insufficient emitter depth, which leads to higher recombination under the metal contacts.

This enhanced recombination is caused by additional defects in a region below the silicon-metal interface [75] (for more details see chapter 3.3.2 Metallization induced losses). Other hypothesis are based on boron segregation into glass contained in the paste or by local inhomogeneity of the emitter doping profile, which both lead to increase of minority carrier concentration near the surface [77].

This experiment led to optimization of emitter doping profile used at *n*-PERT solar cells with respect to following process steps – particularly metallization. The results from IV measurement showed that, for screen printed and firing contacts, there is a trade-off between efficiency potential, demonstrated by the cell precursors and metalized cells. The best compromise is achieved for emitter profiles with low surface concentration (which gives better surface passivation) and emitter with higher depth (which prevent high contact recombination losses). As the new standard boron emitter profile, the profile B3 was set up, and used in following experiments. From the processability point of view it is necessary to mention that the maximum deviation of sheet resistance did not exceed 5 %, which is needed for good quality of metallization in further process steps.

3.1.2 Comparison of dry and wet oxidation at low pressure boron diffusion

The final price of solar cells depends, among other things, on the process time. In case of the previous experiment, there is almost no difference between "new" B3 diffusion and the "old" one in the process time. Modifying the process to incorporate the maintenance could help decreasing final costs. After certain amount of boron diffusion, it is essential to clean the tube because the liquid boron trioxide (B_2O_3), the product of a chemical reaction during diffusion, condenses not only on wafers but also on the walls of the quartz tube. This cleaning could be done by evaporation of water into the tube after unload or, in order to make the production time shorter, by replacing the dry oxidation with wet oxidation process. To verify this idea, experiment using wet oxidation instead of dry oxidation was carried out. At the same time the possibility of replacing atmospheric pressure diffusion with low pressure process was explored.

For this experiment, 6-inch monocrystalline phosphorus-doped *n*-type silicon wafers with ρ_{base} within the range 1 and 3 Ωcm were used. All samples were etched in 22% NaOH solution to carry out a saw damage removal. In this experiment 4 different low-pressure (LP) boron diffusion recipes were tested – named LP-1, LP-2, LP-3, and LP-4 (see **Tab. 3**). To compare the emitter quality between low-pressure and atmospheric-pressure (AP) process the samples with "standard" emitter were made. The samples were placed in the quartz boat in positions represented in **Fig. 32**. The position nearest to the gas inlet was labelled 1, the position closest to the door was labelled 5. The rest of positions were filled up with clean dummies to achieve the same gas flow as in common production. The wet or dry oxidation process took place between deposition and drive-in. The diffusion process for all LP recipes was the same except for the parameters of oxidation, which are mentioned in the **Tab. 3**.

Tab. 3: The overview of used diffusion processes (LP = low-pressure diffusion, standard = atmospheric-pressure diffusion).

Diffusion	Type of Oxidation	Steamer	
LP-1	Dry	No	–
LP-2	Wet	Yes	4 min
LP-3	Wet	Yes	6 min
LP-4	Dry	No	
standard	Dry	Yes	

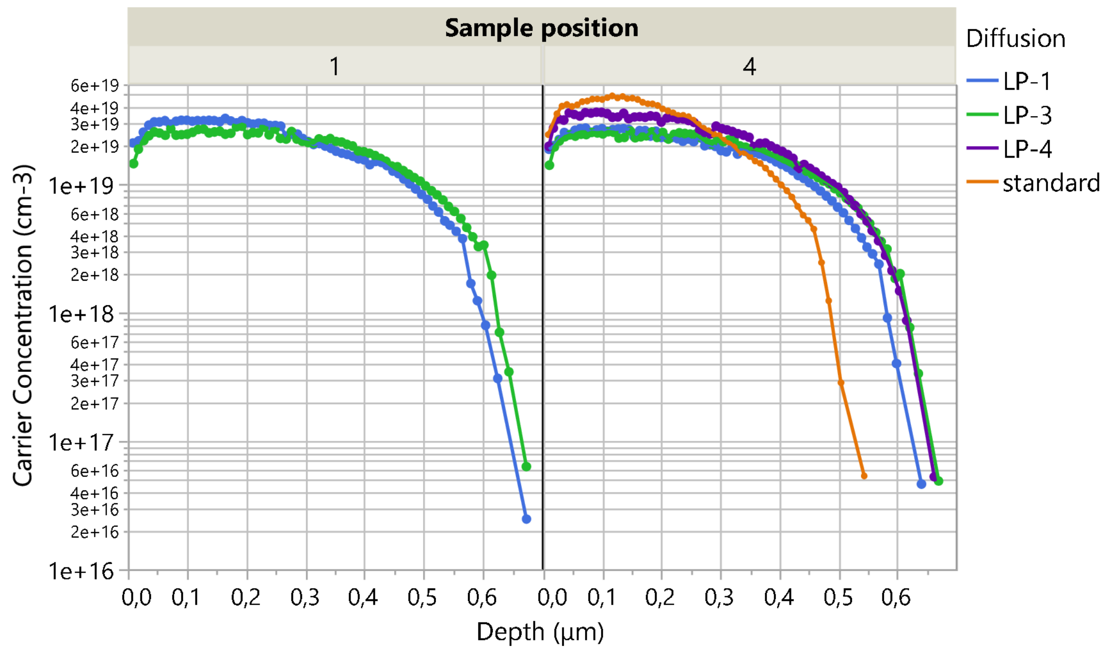


Fig. 36: The comparison of doping profiles for recipes LP-1 and LP-4 (dry oxidation), LP-3 (wet oxidation), and atmospheric pressure diffusion (standard).

On samples where the sheet resistance and the emitter doping profile were measured, it was necessary to remove the BSG layer which was created by etching out in a solution composed of HF, HCl, and demineralised water. To obtain the shape of emitter doping profile (**Fig. 36**) and its parameters (**Tab. 4**) the ECV measurement was taken only for standard, LP-1, LP-3, and LP-4 diffusion, while LP-2 and LP-3 differ from each other only slightly in the steam duration and it was assumed that their emitters had the same properties. The ECV measurement of samples LP-1 and LP-3 was taken for two different positions of the boat to obtain the homogeneity of the doping profile over the boat. From **Fig. 36** it is obvious that there were no significant changes in the emitter doping profile over the boat. The decrease in the boron concentration near the BSG-Si interface, which is caused by different segregation coefficients of B-Si and B-SiO_2, was more noticeable at the standard profile with the highest boron concentration $N_{A\,peak} \approx 5.0{\cdot}10^{19}$ cm^{-3}. In the case of the LP diffusions, the highest boron concentration was $N_{A\,peak} \approx 3.2{\cdot}10^{19}$ cm^{-3} for LP-1 recipe, $2.5{\cdot}10^{19}$ cm^{-3} for recipe LP-3, and

$3.5 \cdot 10^{19}$ cm^{-3} for recipe LP-4 respectively. The emitter was slightly deeper in the case of LP-3 and LP-4 process ($d_{emitter}$ = 0.66 μm) than LP-1 ($d_{emitter}$ = 0.63 μm). The shallowest emitter was the standard ($d_{emitter}$ = 0.53 μm).

Tab. 4: Overview of boron emitter parameters.

Doping profile	R_{Sh} [Ω/sq]	$d_{emitter}$ [μm]	$N_{A\ peak}$ [10^{19} cm^{-3}]
LP-1	76	0.63	3.2
LP-2, LP-3	127	0.66	2.5
LP-4	75	0.66	3.5
standard	70	0.53	5.0

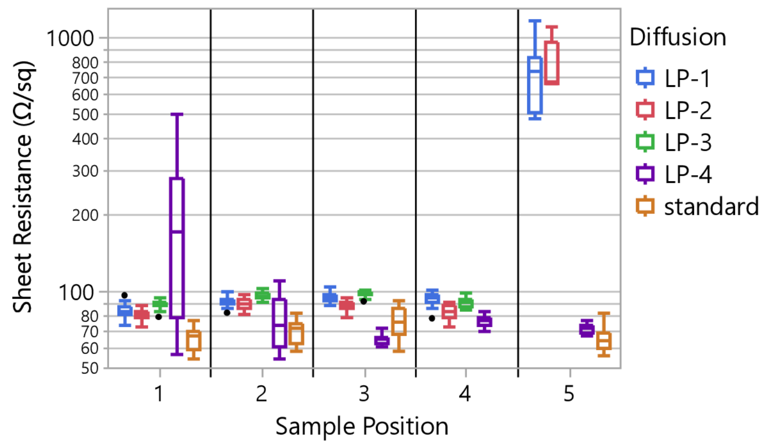


Fig. 37: The comparison of emitter R_{Sh} of all diffusion recipes. The position of wafer nearest to the gas inlet = 1, the position closest to the door = 5.

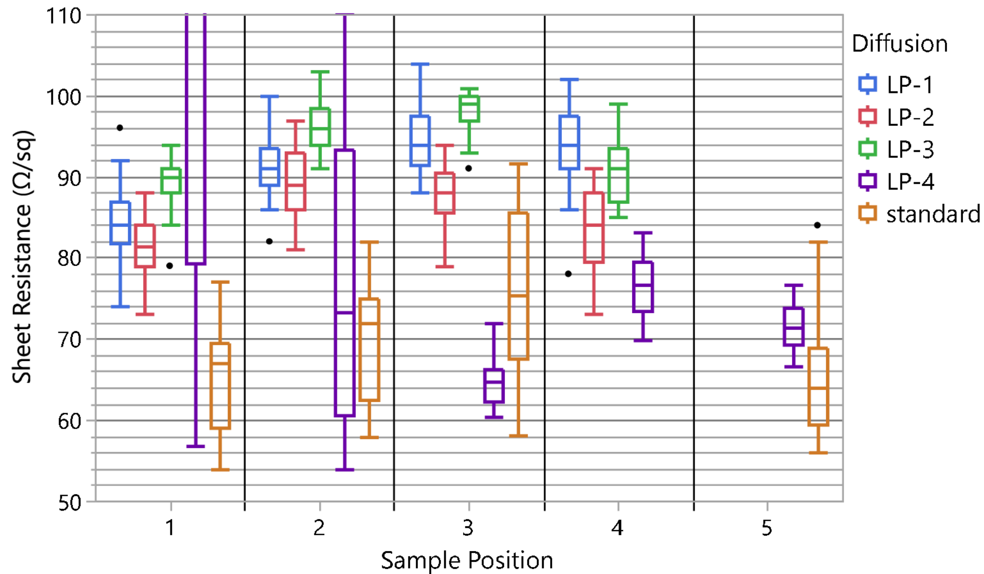


Fig. 38: Detail of R_{Sh} values for samples with R_{Sh} deviation below 5 %, and standard diffusion.

The resulting sheet resistance was measured by the four point measurement on the front side of the wafer in 5×5 points per wafer side in order to ascertainment the average value and its uniformity. To compare the R_{Sh} over two boats with different number of slots the same labelling scheme as in previous measurements was used: the position of wafer nearest to the gas inlet was labelled 1, the position closest to the door was labelled 5.

In **Fig. 37** there are shown measured values of the sheet resistance. Due to failure to achieve good homogeneity of the diffusion over the boat, only results for samples with R_{Sh} deviation of R_{Sh} below 5 % are mentioned further. The maximum deviation of R_{Sh} should not exceed 5 %, required for good quality of metallization. From detailed view of R_{Sh} (**Fig. 38**) it is evident that the homogeneity of the boron layer was sufficient for samples placed in positions 1 – 4 (boat slots from 10 to 300) in case of diffusions LP-1, LP-2, and LP-3, and in positions from 3 – 5 (boat slots from 200 to 390) for recipe LP-4.

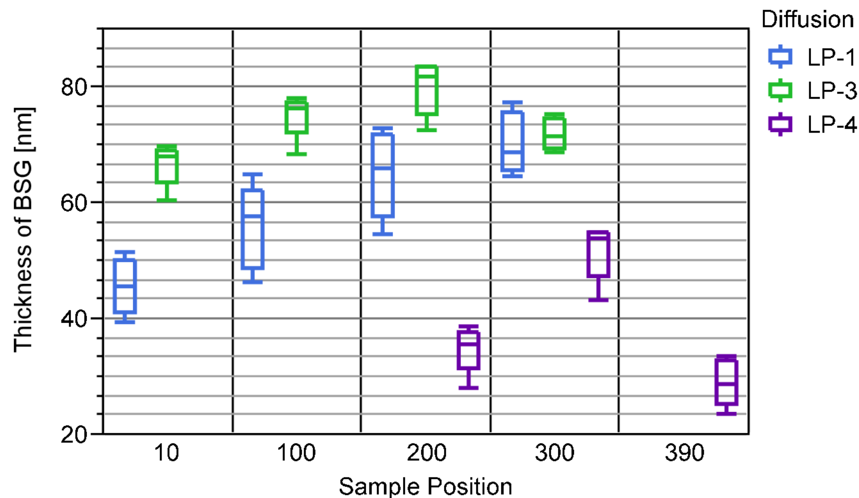


Fig. 39: The thickness of the BSG layer.

Ellipsometry was used for detection of the thickness of the BSG layer (t_{BSG}) for recipes LP-1, LP-3, and LP-4. The thickness was always measured in five points on the front surface of the polished sample – one point was measured in the middle of the wafer, and remaining 4 points were situated in the corners of the wafer, about 1 cm from the edge. The values of BSG thickness are shown in **Fig. 39**. The average value of t_{BSG} was ranging from 45 nm to 70 nm for LP-1, from 66 nm to 80 nm for LP-3 and from 29 nm to 52 nm for recipe LP-4. Owing to much better homogeneity of the BSG layer, the recipe LP-3 seemed to be a more suitable process.

After the measurement of BSG layer, the deposition of passivation layer (PECVD SiN_X) was done except or samples LP-4. These LP-4 samples were left out due to their high inhomogeneity near the gas inlet. On the rest of cell precursors the iV_{OC} and J_0 was measured before and after annealing using Quasi-Steady-State Photoconductance to establish the influence of annealing on passivation quality. The measurements were

taken on the front side of each sample in five points. The resulting values of iV_{OC} and J_0 for all measurements are shown in **Fig. 40**, detailed view for samples after annealing is in **Fig. 41**.

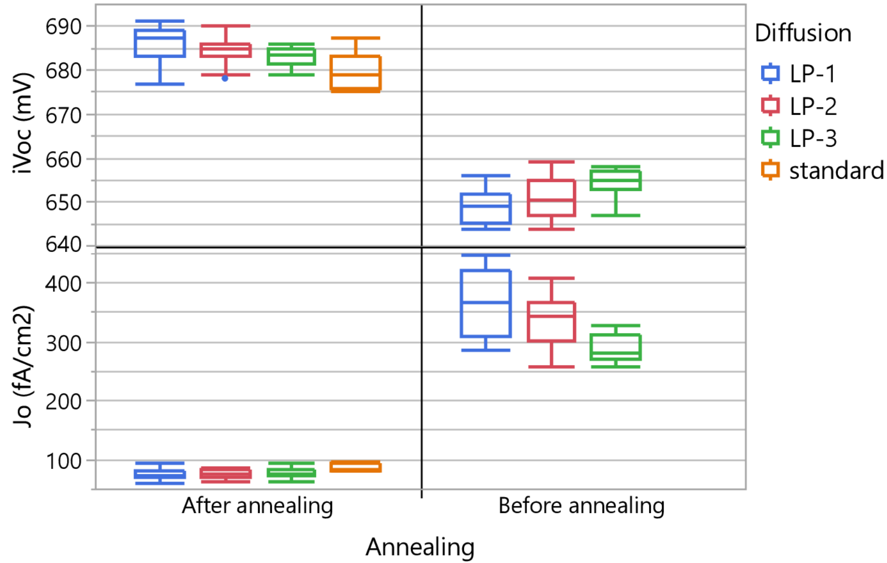


Fig. 40: iV_{OC} at 1 sun and J_0 of the cell precursors (before metallization) before and after annealing. The J_0 was extracted at an injection level of $\Delta n = 2 \cdot 10^{15}$ cm^{-3}.

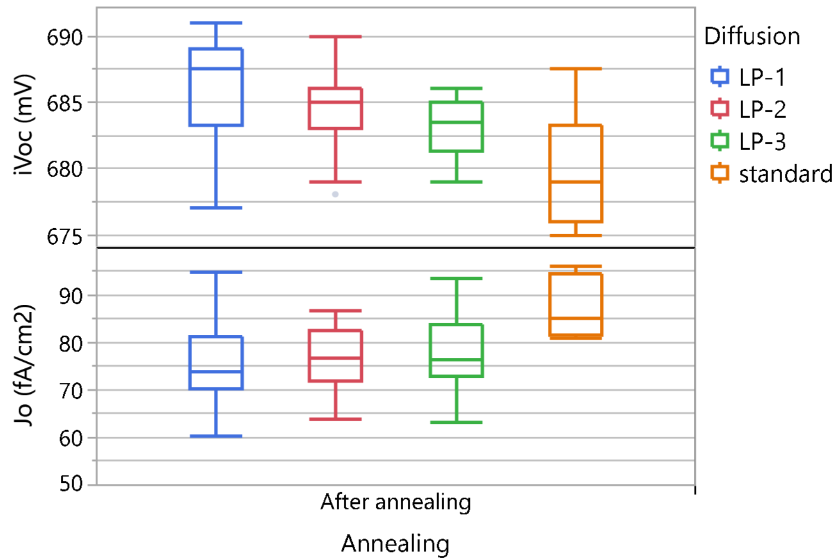


Fig. 41: Detailed view of iV_{OC} at 1 sun and J_0 of the cell precursors (before metallization) after annealing. The J_0 was extracted at an injection level of $\Delta n = 2 \cdot 10^{15}$ cm^{-3}.

The quality of the passivation layer before annealing was insufficient, low values of iV_{OC} and high values of J_0 indicated high recombination rate. The iV_{OC} was ranging between 644 mV and 659 V. The J_0 values were from 260 fA/cm^2 to 450 fA/cm^2. After annealing, the implied V_{OC} values increased and J_0 decreased. This improvement of

passivation came from releasing hydrogen during the hydrogenation process. The highest value was reached in the case of diffusion LP-1 (iV_{OC} 691 mV), but the best uniformity over boat was reached using recipe LP-3, where the average value of iV_{OC} was ranging between 679 mV and 686 mV. The lowest recombination and thus the lowest value of J_0 were achieved in the case of diffusion LP-1 (J_0 60 – 90 fA/cm^2), but generally there were not significant differences between LP diffusions. However, all low pressure processes showed better passivation (lower J_0, higher iV_{OC}) in comparison with standard atmospheric pressure diffusion.

Based on results from this experiment, it could be stated that dry oxidation process can be replaced with wet oxidation. Also, all low pressure processes showed better passivation (lower J_0, higher iV_{OC}) in comparison with standard atmospheric pressure diffusion and thus applicability for production of high efficiency *n*-type solar cells. Unfortunately, due to several technical problems with low pressure diffusion furnace there was no continuance in low-pressure diffusion processes.

3.2 Passivation layer

Surface recombination can have a major impact both on the J_{SC} and on the V_{OC}, and thus on solar cell efficiency. Passivation of the surface enhances the overall cell efficiency by prolonging the charge-carrier effective lifetime due to lowering the high top surface recombination. For n^+(phosphorus) doped regions sufficient surface passivation is achieved by using e.g. SiN_X film deposited by PECVD. However, on p^+ boron doped regions, SiN_X does not passivate the surface. Some of the reported approaches to solving this problem are based on using the intermediate layer of SiO_2 or Al_2O_3 between SiN_X and the p^+ diffused emitter, or even by using PECVD silicon carbide SiC_X as a passivation layer instead of SiN_X. Also, the boron silicate glass, grown on the *p*-type emitter during all the diffusion processes described in the two previous subsections, could be used as the passivation layer, as it is a mixture of SiO_2, partly dissolved B_2O_3, and some amount of elemental boron.

In the following parts of this chapter the experiments examining stack of SiO_2 or BSG and PEVCD SiN_X are described to determine the optimal composition with regard to the emitter structure and subsequent metallization. Chapter 3.2.1 is dedicated to the study of the minimum thickness of SiO_2 layer between p^+ boron emitter and SiN_X, necessary to obtain a good passivation quality. In preparation for this experiment, the BSG etching rate in relation to its composition was measured. The aim of the experiment described in 3.2.2 was the study of the passivation quality of different BSG/SiO_2 layers in connection with varied PECVD SiN_X capping layers, in order to achieve an optimal composition of ARC and passivation stack of boron emitter. Within chapter 3.2.3 an experiment focused on impact of SiN_X thickness simultaneously with firing profile on resulting contact resistance was done to establish an optimal setting for solar cell production. The experiment in 3.2.4 explores the possibility of preventing the PID effect on the cell level by combination of layers creating the ARC and passivation layer.

3.2.1 Minimal SiO_2 thickness and BSG etching rate

At the beginning it was necessary to set up a passivation layer or a stack of different layers, which can passivate the *p*-type emitter. Currently there is a wide variety of options how the p^+ surfaces can be effectively passivated. Unfortunately, only a few of them are available for industrial use. One of the reasons for the relatively poor surface passivation of p^+ surfaces by SiN_X is related to the very high fixed charge density in PECVD SiN_X. It was observed that the fixed charge density can be reduced by adding a thin silicon oxide layer between the crystalline silicon and the SiN_X film. The experiment described below was done to ascertain the minimum thickness of SiO_2 layer required for good passivation. During the first part of this experiment the etching rates of BSG and SiO_2 were measured for further use of BSG as the intermediate layer between p^+ and SiN_X, because the passivation of the BSG layer alone is insufficient.

The first part of this experiment was focused on measurement of etching BSG rate and it was carried out using 6-inch monocrystalline phosphorus-doped *n*-type silicon wafers with ρ_{base} within the range 1 and 3 Ωcm. The SDE was done in 22 % NaOH solution, the B-clean (HF/O_3 and HCl/HF) and texturization in KOH solution was done afterwards. Three different boron emitters varying in doping profile were deposited to get different thickness of BSG layer with different content of boron in it – see **Fig. 42** (A5: R_{Sh} = 85 Ω/sq; B7: R_{Sh} = 130 Ω/s). The DEP profile (R_{Sh} > 200 Ω/sq) is not shown there, as this diffusion was done only to create very thin BSG layer. To see how the etching rate changed with the modification of BSG composition, an oxide with similar thickness was created on the *n*-type wafers using dry oxidation. The process of oxidation was the same as in the diffusion in the oxidation furnace. The BSG/oxide layer was made thinner by etching in bath containing 2% HCl and 2% HF solutions.

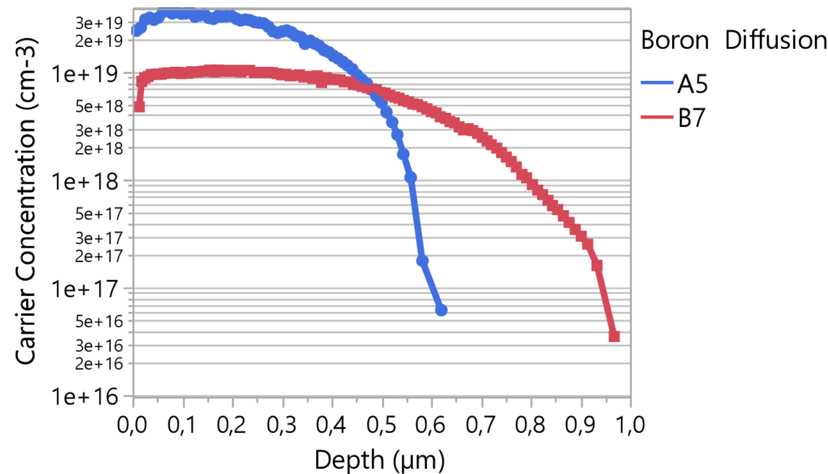


Fig. 42: Doping profiles A5 and B7 of boron emitter measured by ECV at central position of the boat.

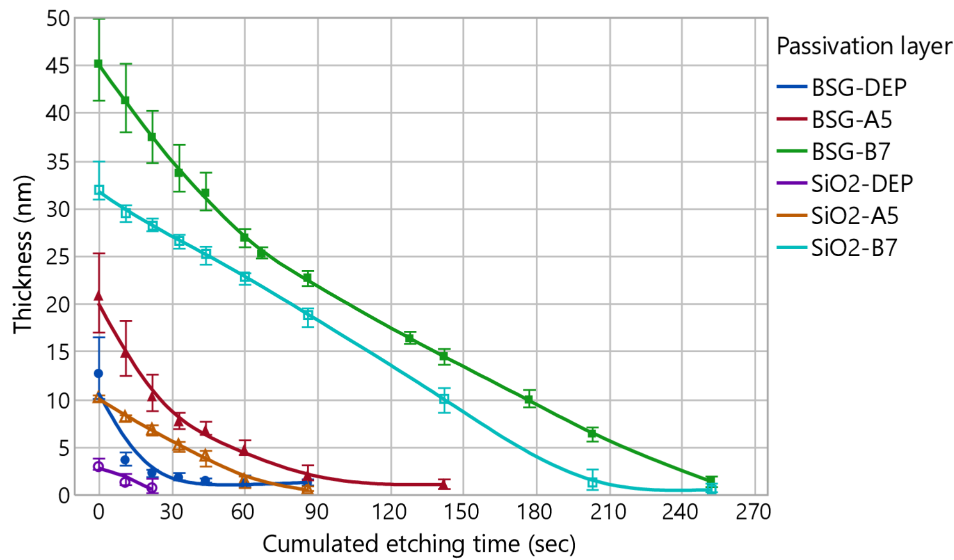


Fig. 43: The dependence of BSG/SiO_2 thickness on cumulated etching time.

The dependency of layer thickness on cumulated etching time is shown in **Fig. 43**. The thickness of SiO_2 decreased during the etching almost constantly, the etching rate was ca. 0.2 nm/s. The etching rate in the case of BSG layers changed according to the boron content in it (etching rate depends on local B_2O_3 content in the BSG and is higher than etching rate of the SiO_2 layer) and thus was higher in the first third of its thickness. This is important because towards the edges of the cell the BSG layer grows thicker than in the centre and this variation in the thickness leads to changes in the reflectivity and thus to non-homogeneous absorption. The etching process enables unification of the BSG thickness over the wafer. In case of layer BGS-DEP the speed was about 8 nm/sec.

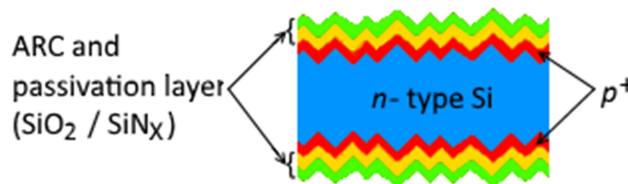


Fig. 44: Symmetrical $p^+/n/p^+$ test structures for QSSPC measurement.

In the second part of this experiment samples with symmetrical boron diffused test structure (**Fig. 44**) were created to find out the minimum SiO_2 thickness necessary for good passivation of boron layer. The 6-inch *n*-type mono-Si wafers with ρ_{base} ca. 2.5 Ωcm were processed by SDE, wet chemical alkaline texturization, and cleaning by HCl, HF, and HF/O_3 solutions. The p^+ layer (B7: R_{Sh} = 130 Ω/sq) was created by diffusion in quartz tube furnaces containing BBr_3, then the thermal SiO_2/ SiN_X stack was deposited and finally the samples were annealed in IR belt furnace.

In the first part of this experiment the BSG etching rate was measured. Determining this rate was necessary either for the 2nd part of this experiment or for experiments described

in the following chapters to control the thickness in the case of different diffusion processes. The iV_{OC} values obtained by QSSPC measurement were used to find the optimum thickness of the SiO_2 in the stack (**Fig. 45**). The minimum thickness of 10 nm SiO_2 or BSG appears to be necessary to achieve good passivation of boron emitter in the *n*-PERT cell concept. This value was used in the following experiments.

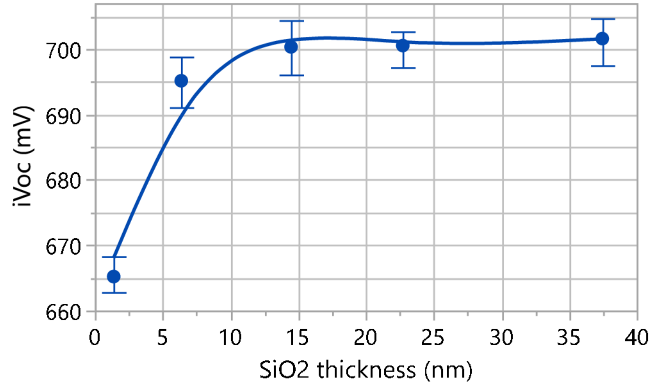


Fig. 45: iV_{OC} of symmetrical $p^+/n/p^+$ test structures with thermal SiO_2/SiN_X passivation stacks as a function of SiO_2 interfacial layer thickness

3.2.2 Boron emitter passivation by SiO_2 / PECVD SiN_X stack

As has been mentioned in previous chapter 3.2.1 , using PECVD hydrogenated silicon nitride resulted in poor or no passivation for p^+ emitters. Therefore, the stack of layers comprising of a thin SiO_2 and SiN_X film is commonly used to passivate boron doped regions. The SiO_2 layer can be replaced by BSG, as the BSG layer in combination with a PECVD SiN_X can passivate the surface equally well as thermal oxide based passivation.

The aim of this experiment was to study the passivation quality of BSG and PECVD-SiN_X stack at different boron diffusion. For this purpose two different structures were prepared **(Fig. 46)** – on the one hand an *n*-PERT cell with a homogeneous diffused front boron emitter and a phosphorus BSF; and on the other hand corona charge test structure. Both structures were fabricated on 6-inch *n*-type monocrystalline Si wafers with base resistivity of 2.5 Ωcm. Standard industrial processes were used, which included wet chemical alkaline texturization, cleaning by HCl, HF, and HF/O_3 solutions and diffusion in quartz tube furnaces containing $POCl_3$ (n^+ BSF, 75 Ω/sq) or BBr_3 (p^+ emitter, 130 Ω/sq). For the solar cell devices the rear side was chemically polished and the n^+ BSF diffusion was passivated by a thermal SiO_2/SiN_X stack. Screen printing and firing through of commercial silver containing pastes were applied to both sides for metallization.

All solar cells were processed identically, with the exception of boron emitter passivation. For the boron emitter 5 different passivation stacks were investigated and compared, as described in detail in **Tab. 5**. The thickness and refractive index of SiO_2 or SiN_X layer were measured using ellipsometry on polished wafers on which these layers were created together with samples.

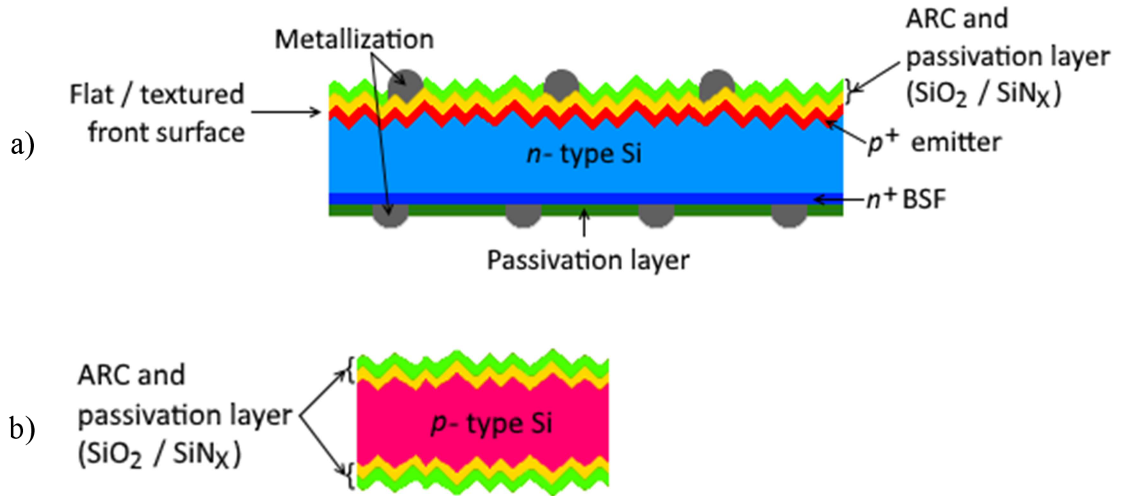


Fig. 46: Schematic cross-section of the investigated *n*-PERT cells (a) and test structure to corona charge measurement (b).

Tab. 5: The overview of investigated ARC layers. The thickness of layers was measured with ellipsometry on polished Si wafers which were deposited together with samples.

	G1	G2	G3	G4	G5
Emitter	p^+	p^+	p^+	p^+	p^+
1st layer	SiO_2 (10 nm)	SiO_2 (30 nm)	NAOS (1.5 nm)	SiO_2 (10 nm)	SiO_2 (10 nm)
2nd layer	SiN_X ($n = 2.0$)	SiN_X ($n = 2.0$)	SiN_X ($n = 2.0$)	SiN_X (n = 2.08)	SiN_X (n = 2.22)

First, the stacks G1 and G2 aimed to investigate the effect of SiO_2 interfacial layer thickness on the passivation quality of the SiO_2/SiN_X stack. Here, a thermal SiO_2 was grown in-situ during the BBr_3 diffusion on boron emitter surface with a thickness of about 40 nm. Subsequently, the thick SiO_2 layer was partially etched (thinned) in 2% HF solution to yield various SiO_2 thicknesses, followed by a 62 nm PECVD SiN_X antireflection coating (ARC; n ≈ 2) deposition of the capping layer to complete the passivation stack.

Then, the stacks G1 and G3 aimed to compare different SiO_2 interface passivation layers, whereas the SiN_X capping layer was kept the same (ARC; n ≈ 2). Stack G3 contained a 1.5 nm chemical SiO2 interfacial layer grown by nitric acid oxidation of silicon (NAOS), as it is known from literature that such stacks can passivate boron emitters [78]. Finally, in the stacks G1, G4, and G5, the interfacial layer was kept constant while the chemical composition of the SiN_X capping layer was varied. Layers

with higher Si- and hydrogen-content were achieved by changing the NH_3:SiH_4 gas ratios during deposition.

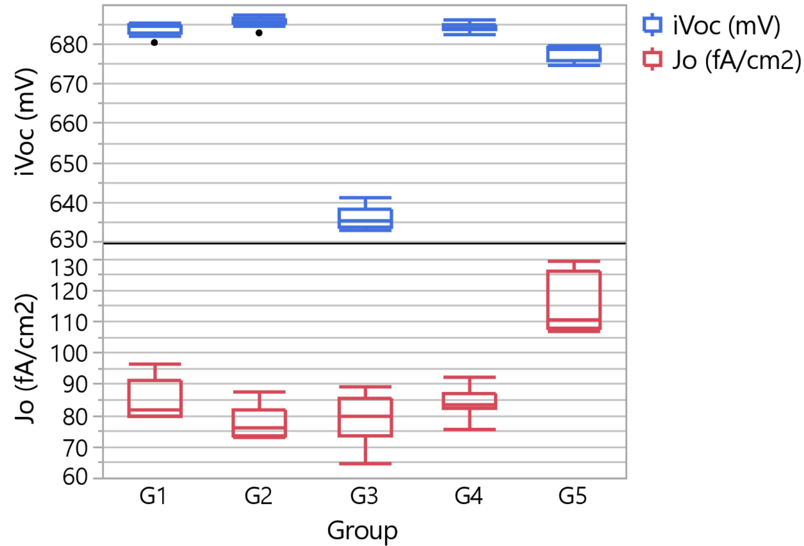


Fig. 47: iV_{OC} of the cell precursor (before metallization) obtained at 1 sun illumination and J_0 extracted at an injection level of $\Delta n = 3 \cdot 10^{15}$ cm^{-3}.

Before printing the metallization grid, but after annealing, the iV_{OC} and J_0 (**Fig. 47**) was measured using QSSPC to establish how the passivation quality of PECVD SiN_X/SiO_2 stack influenced the passivation quality. From iV_{OC} values it is obvious that the best passivation quality on the cell precursor level was achieved with G2, where the passivation stack was composed of 30 nm SiO_2 and 62 nm SiN_X with refractive index $n = 2.0$. Slightly lower iV_{OC} values were measured on samples from groups G1 and G4, where the ARC layer was made up of 10 nm SiO_2 and SiN_X with low refractive index (62 nm with $n = 2.0$ or 54 nm with $n = 2.08$).

On finished solar cells the IV measurement (**Fig. 48**) was taken, and internal quantum efficiency (IQE), density of interface traps (D_{it}), and total fix interface charge (Q_{tot}) was measured (**Fig. 49**). The lower values of FF and efficiency were caused by not optimal grid structure. The passivation stacks G1 and G2 showed the best passivation quality, as there was no decrease at short wavelengths in contrast with the samples from G4, which had J_{SC} and V_{OC} values almost on the same level. The absorption in SiN_X due to higher refractive index is not corrected in the IQE curve. So the reduction in IQE for G4 compared with G1 should be in SiN_X due to the additional absorption and not necessarily to the poorer passivation. It has to be said that the interface quality is very high (low D_{it}) although the interface charge of thermal oxide is very low.

The difference in IV results between G1 and G2 arises from different optical properties of passivation stack. The G2 gives slightly better passivation (higher V_{OC}) but the J_{SC} value was lowered due to higher optical losses caused by worse light coupling.

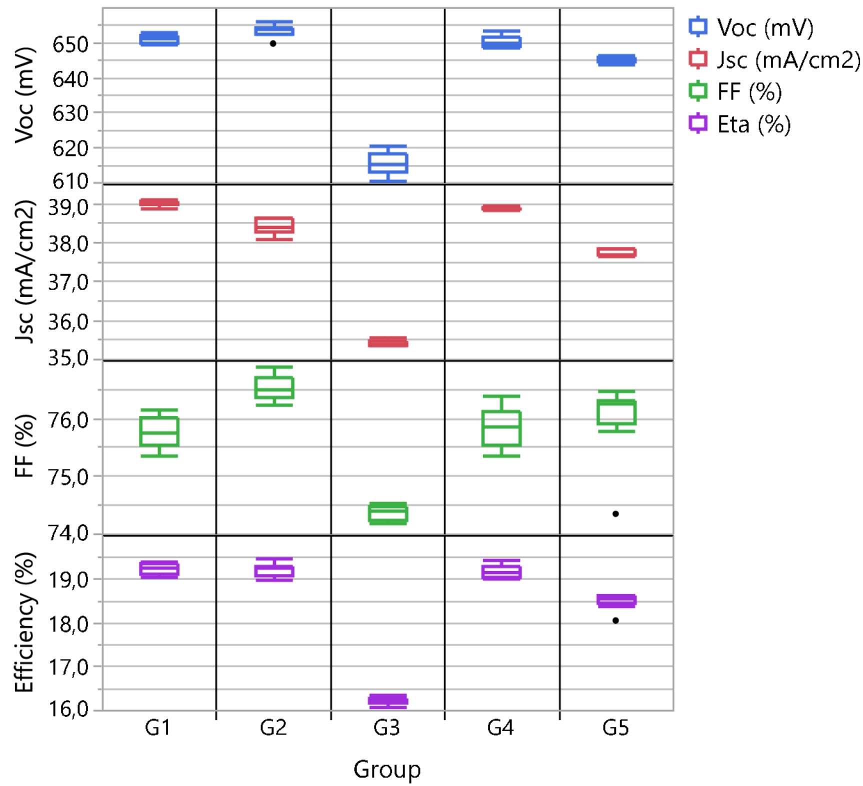


Fig. 48: V_{OC}, J_{SC} , FF, and efficiency values measured on metallized solar cells were obtained by IV measurement at 25 °C and under AM 1.5 spectrum with illumination intensity of 1000 W/m^2.

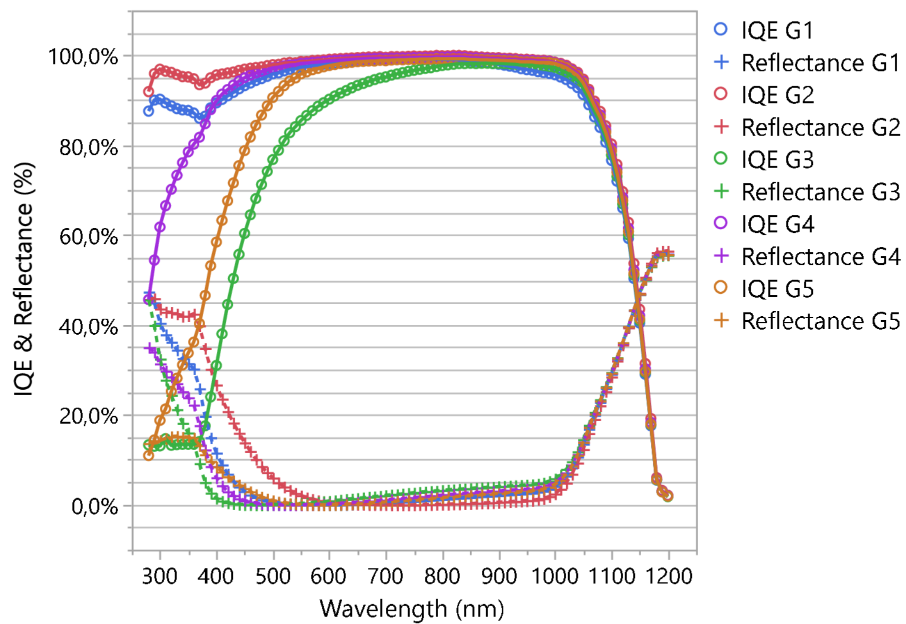


Fig. 49: Internal quantum efficiency (IQE) of the solar cells with different front boron emitter passivation stacks.

From the IQE results in the (**Fig. 49**)) it is obvious that the passivation quality was worse in the case of SiN_X capping layers with higher refractive index (n = 2.08 or 2.22) despite the fact that these layers might be better for good passivation due to higher content of hydrogen. The reason is that the deposition SiN_X with higher refractive index also increased the density of interface states and positive interface charge (**Fig. 50**), which both had a negative effect on boron emitter passivation.

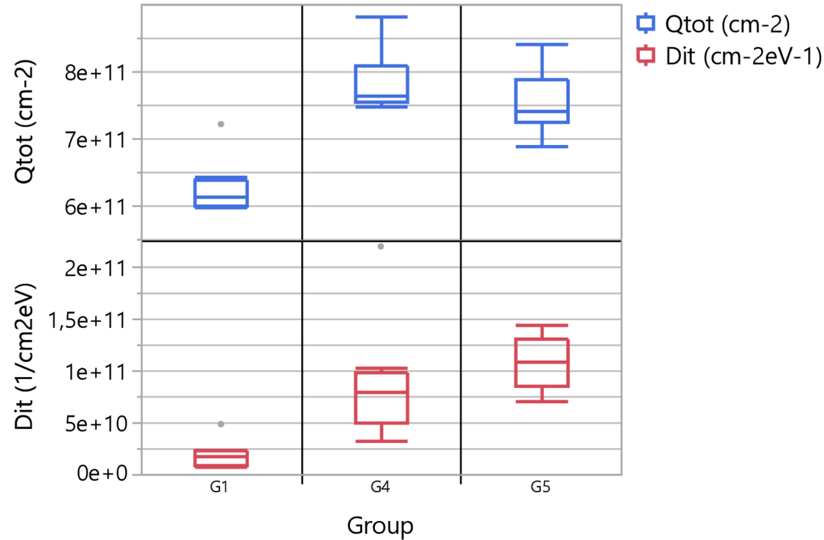


Fig. 50: Density of interface traps (D_{it}) and total fix interface charge (Q_{tot}) for different composition of SiN_X capping layer determined by corona charge measurements. The measurements were performed using Semilab PV2000 tool on un-diffused *p*-type c-Si wafers passivated by similar stack structures of G1, G4, and G5.

This experiment followed up on the previous experiment aimed to improve the SiO_2/SiN_X passivation stack. The results show that the optimum passivation in this case is achieved by a stack layer of a thermal SiO_2, with a thickness of at least 10 nm, and a SiN_X layer with a low refractive index. This is in conformity with research done by Mack *et al.* [79], who found out that SiO_2 layer of thickness > 15 nm ensures a high degree of chemical passivation together with 70 nm PECVD SiN_X (n = 1.90). Using SiN_X layer with high refractive index (n > 2.30) would most probably required SiO_2 layer of thickness around 60 nm [80]. From the passivation results it is observed that the chemical SiO_2 deposited by NAOS method does not show good passivation quality. This could be caused by PECVD deposition of SiN_X, which could damage the thin SiO_2 layer.

Also the chemical composition of SiN_X capping layer plays an important role for surface passivation. A more Si-rich SiN_X layer shows significant degradation in surface passivation of the stack due to the increase in the density of interface states and fixed positive charges at the interface. However, there is still a difference between quality of BSG passivation and passivation by PECVD Al_2O_3, which usually shows better results than passivation based on thermal SiO_2. This difference results from the field effect

arising from the negative fixed charge in Al_2O_3. The biggest advantage of BSG approach is the cheaper "metal-free process".

3.2.3 Optimization of SiN_X thickness

Previous chapters focused only on passivation layer regardless of the next process step – metallization. This experiment attempted to establish the optimum between high-quality passivation and fine metallization, as their requirements are not fully corresponding. The solar cell efficiency is closely related to short-circuit current and contact resistivity, which in turn strongly depend on thickness of antireflection and passivation layer [74] [81]. However, the passivation is present also on the rear side of the solar cell. To investigate the impact of the rear silicon nitride thickness on the passivation quality and contact resistivity, and to determine the optimal thickness of passivation layer afterwards, the following experiment was done.

As a starting material for this experiment the 6'' monocrystalline phosphorus-doped *n*-type wafers were used. The average base resistivity ρ_{base} = 2.3 Ωcm was ascertained using four point measurement on both sides of the wafer in 5×5 points per wafer side on annealed wafers. A schematic cross-section of the samples is presented in **Fig. 51**. As the passivation layer on the rear side is composed from two layers, where one is with various thickness (**Fig. 51** a), it was necessary to prepare samples dedicated only for measurement of varied SiN_X layer, see **Fig. 51** b.

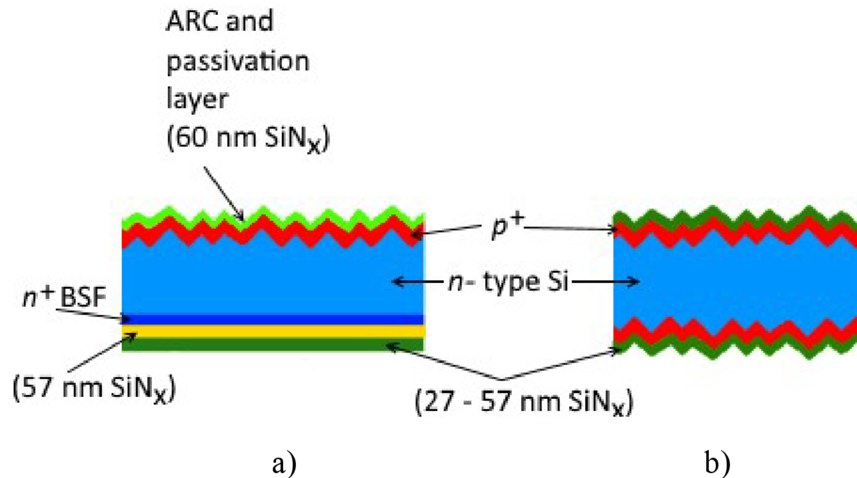


Fig. 51: a) The structure of cell precursor (solar cell without metallization); b) Sample used for measurement of SiN_X thickness.

All samples were processed using 22% NaOH for SDE and mixture of KOH/H_2O_2 for wet chemical alkaline texturization using, followed by cleaning in HCl and HF solutions. The diffusion processes were done in a quartz tube furnace containing $POCl_3$ or BBr_3 as a doping gas. During the phosphorus diffusion, the n^+ BSF layer with resulting sheet resistance R_{Sh} around 60 – 65 Ω/sq was created. Boron diffusion was used to create p^+ emitter of the front side with R_{Sh} in the range 70 – 80 Ω/sq. In the case of the symmetric samples only boron diffusion was realized.

The p^+ and n^+ regions were subsequently passivated by SiN_X layer deposited by PECVD for the each side separately. The 60 nm SiN_X layer was deposited on the front side. The deposition on the rear side was composed of two steps – firstly the base 57 nm layer was created and after that depositions with various times were done ($t_{deposition}$ was set up to 280 s, 380 s, 480 s, 580 s, and 680 s). During these last depositions, measurements of SiN_X thickness were taken on the passivation layer samples. Thermal donor annealing in the IR belt furnace at peak temperature ϑ_{peak} = 815 °C followed after deposition of all SiN_X layers.

For the determination of thickness of SiN_X layer (d_{SiNX}) deposited on textured surface, a method based on the measurement of a reflectance spectrum of a wafer was used. The detector was inclined by 8° perpendicular to the sample. The dependence of reflection on the wavelength of incident light is shown in **Fig. 52**.

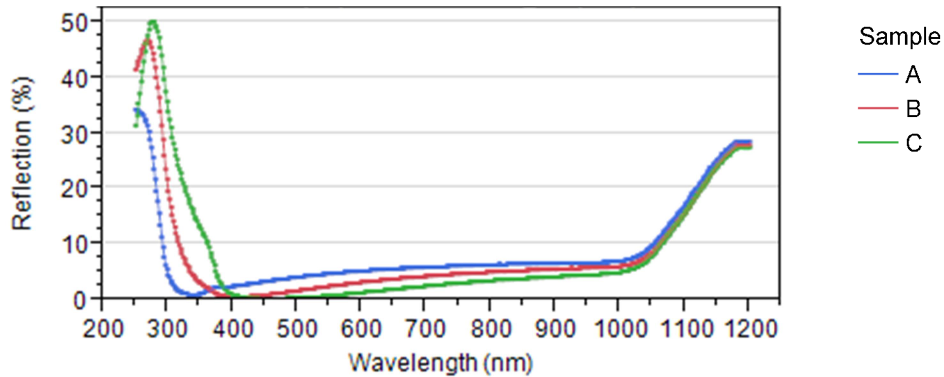


Fig. 52: The reflectance of samples with $t_{deposition}$ 480 s, 580 s, and 680 s.

The thickness was calculated from the wavelength λ_{min} at the minimum of the reflectance curve according to:

$$d_{SiN_X} = \frac{\lambda_{min}}{4n_1}\sqrt{1 + \frac{{n_0}^2}{{n_1}^2}[\sin(90 - \theta)]^2} \qquad (1)$$

where n_0 was the refractive index of air ($n_0 = 1$), n_1 was the refractive index of SiN_X ($n_1 = 2.03$), and θ was the angle of incident beam ($\theta = 8°$) [81]. The resulting SiN_X thickness is given in Tab. 6. In the case of samples with $t_{deposition}$ 280 s and 380 s the SiN_X thickness was evaluated from extrapolation based on deposition time (**Fig. 53**).

Tab. 6: Calculated of SiN_X thickness for samples.

Sample	$t_{deposition}$ [s]	λ_{min} [nm]	d_{SiNX} [nm]
X	280	_	27.2
Y	380	_	34.8
A	480	341	42.1
B	580	406	50.1
C	680	462	57.0

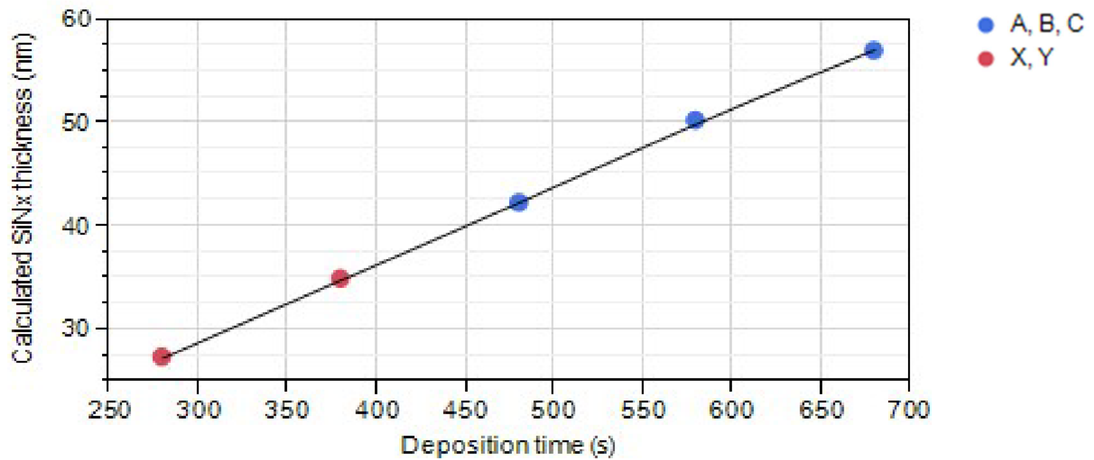


Fig. 53: The dependence of SiN_X thickness on deposition time.

To compare the passivation quality of different SiN_X stacks, the implied V_{OC} and J_0 was measured before printing the metallization grid using QSSPC. The measurements were taken on the front side of each sample in five points. In **Fig. 54** there is shown dependence of iV_{OC} and J_0 on the total thickness of the SiN_X layer on the rear side.

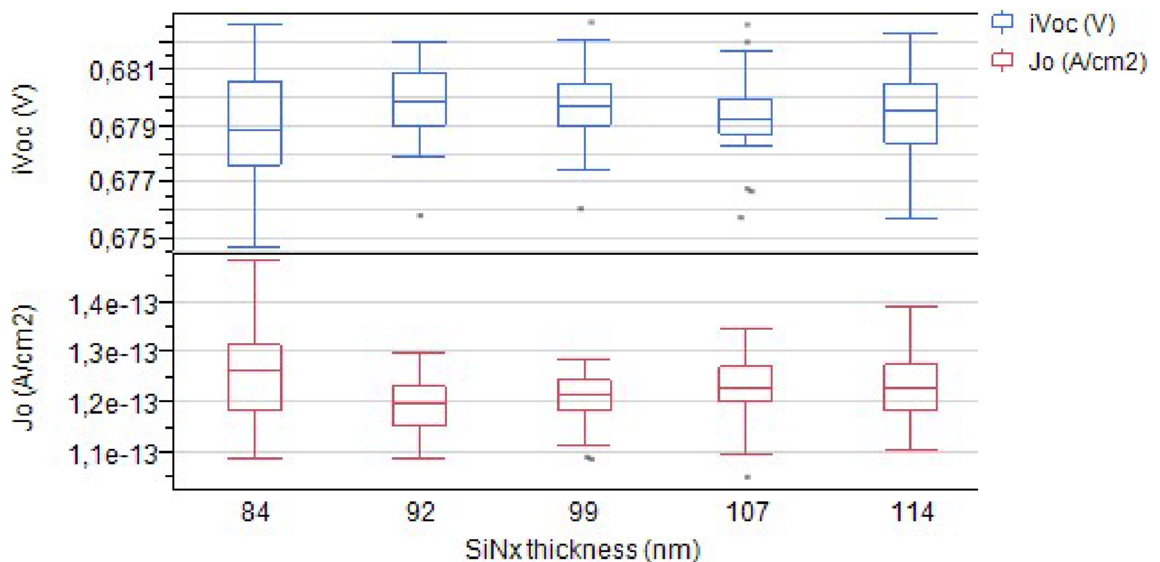


Fig. 54: iV_{OC} at 1 sun and J_0 of the cell precursors (before metallization).
The J_0 was extracted at an injection level of $\Delta n = 2{\cdot}10^{15}$ cm^{-3}.

It is obvious that the best passivation quality (high iV_{OC} and low J_0) is achieved in the SiN_X layer with average thickness of 92 nm and 99 nm. The mean values of iV_{OC} and J_0 were 679.8 mV and 11.98 fA/cm^2 in the case of SiN_X thickness of 92 nm, or rather 679.7 mV and 12.10 fA/cm^2 for samples with SiN_X thickness of 99 nm.

In the last step, the silver finger grid at the front side and the rear side were screen printed using commercially available silver paste. The cell process was finished by

drying and subsequently co-firing the metal contacts in an infrared belt furnace. The three used temperature profiles differed from each other in the maximum temperature to evaluate the influence of firing metallization on contact resistivity. The peak temperature was set to 780 °C, 795 °C, and 815°C.

The contact resistivity (ρ_C) characterizes the interfacial perfection between a conducting material and an underlying semiconductor. After printing and firing step, the dependence of contact resistivity on SiN_X thickness and firing temperature was detected by the Transmission Line Model (TLM) method. The contact resistivity was measured in 15 points per sample. The dependence of contact resistivity on total SiN_X thickness on the rear side of a solar cell and on the peak firing temperature is shown in **Fig. 55**.

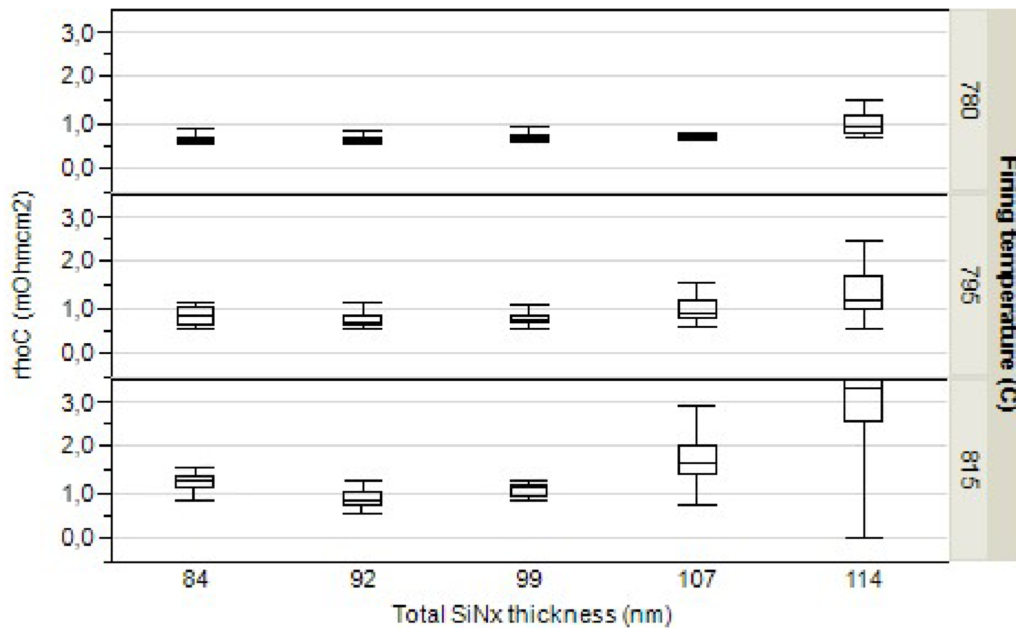


Fig. 55: The influence of SiN_X thickness and firing temperature on resulting contact resistivity.

The lower contact resistivity (below 1 mΩcm^2) was achieved for combination of lower peak firing temperature (780 °C and 795 °C) and SiN_X thickness in the range of 84 nm and 99 nm (or 107 nm for ϑ_{peak} = 780 °C). The lowest contact resistance ($\rho_C = 0.65$ mΩcm^2) was reached for combination of thickness 84 nm and temperature ϑ_{peak} = 780 °C.

The results of this experiment show that the value of contact resistivity depends mainly on the firing profile (in this case υ_{peak}) and much less on SiN_X thickness, which had big impact on passivation quality, as the best passivation quality (high iV_{OC}, and low J_0) results in SiN_X layer with average thickness $d_{SiNX} = 92$ nm. The lowest contact resistivity was achieved for combination of low firing temperature and total SiN_X thickness of 84 nm. Based on this experiment the peak firing temperature of 780 °C was used in solar cell production.

3.2.4 Potential induced degradation

As sollar cells and modules are expected to work for a long time without changing their characteristics, it is also necessary to deal with problems caused by different degradation mechanism. This work is based on experiment concerning different properties of different passivation stacks (described in chapter 3.2.2).

The choice of glass, encapsulation, and diffusion barriers has been shown to have an impact on PID on the module level [82] [83]. On the cell level, properties of the antireflection and passivation layer have also impact on the PID [84]. The cause of PID in *n*-type solar cells, however, is still unclear and needs to be verified. This work is focused on the influence of different composition of ARC layer on PID at *n*-PERT cell concept. A schematic cross-section of the studied solar cells is presented in **Fig. 56**.

For the experiment, 6-inch *n*-type monocrystalline silicon substrates were used. Wafers were processed using standard industrial process, which includes wet chemical alkaline texturization, diffusion in a quartz tube furnace containing $POCl_3$ (n^+ BSF, 65 Ω/sq) or BBr_3 (p^+ emitter, 75 Ω/sq), deposition of ARC layer, screen printing of Ag finger grid on both sides and co-firing. Half of the samples had textured front side, the rest of them had flat front side.

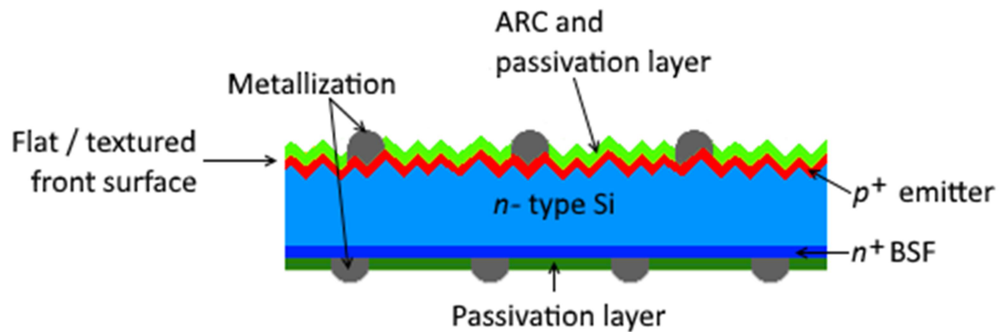


Fig. 56: Schematic cross-section of the investigated *n*-PERT cells.

Tab. 7: The overview of investigated ARC layers.

	G1	G2	G3	G4	G5	G6	G7
Emitter	p^+	p^+	p^+	p^+	p^+	p^+	p^+
1st layer	SiO_2 (10 nm)	SiO_2 (30 nm)	NAOS (1.5 nm)	SiO_2 (10 nm)	SiO_2 (10 nm)	SiO_2 (10 nm)	NAOS (1.5 nm)
2nd layer	SiN_X (n = 2.0)	SiN_X (n = 2.0)	SiN_X (n = 2.0)	SiN_X (n = 2.08)	SiN_X (n = 2.22)	SiN_X (n = 2.22)	SiO_2 (20 nm)
3rd layer						SiO_2 (100 nm)	SiN_X (n = 2.0)

In this experiment, 8 different compositions of ARC layer, labelled G1 – G7 were tested (**Tab. 7**). The same ARC and passivation layers labelled G1 – G5 were used as in experiment 3.2.2 Boron emitter passivation by SiO2 / PECVD SiNX stack.

For groups G1 and G4 – G6 the 10 nm thick layer of thermal SiO_2 was deposited on boron emitter, then PECVD SiN_X layer with different refractive index followed, and in the case of G6 samples, PECVD SiO_2 was deposited as the 3rd layer. For samples from groups G3 and G8 a 1.5 nm thin layer of SiO_2 was formed by the NAOS method and then PECVD SiN_X/ SiO_2 layers were deposited. The thickness of layers was measured with ellipsometry on flat silicon wafers, which were deposited together with the samples.

Full-size 3 busbar single cell modules were fabricated using solar textured cover glass, ethylene-vinyl acetate copolymer (EVA-S88) for the encapsulation, and standard transparent back sheet material. The structure of module is shown in **Fig. 57**.

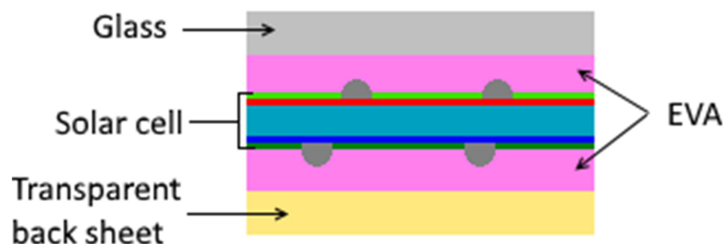


Fig. 57: Schematic cross-section of the investigated module.

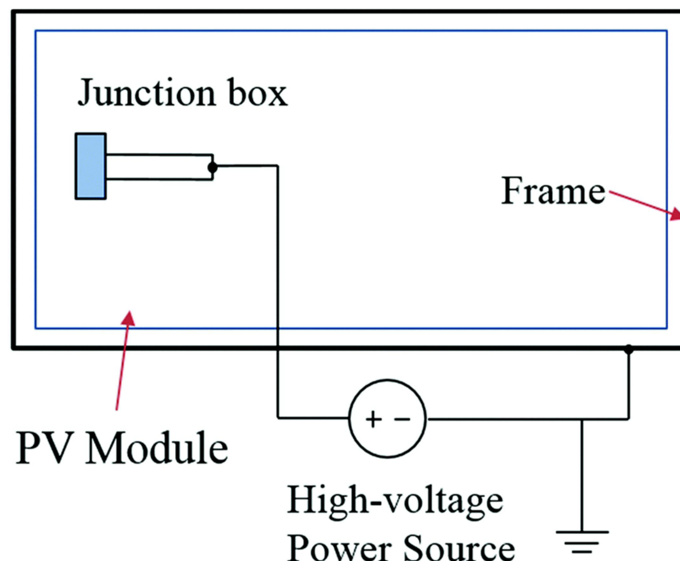


Fig. 58: Schematic diagram of the PID test setup in a climate chamber.

The PID tests were performed according to technical specification IEC 62804-1 [85] by applying high voltage (-1000 V) to modules for 23, 46 or 59 hours. The modules were placed in a climatic chamber on the metal base plate, with the glass side facing down. The conditions were 85 ± 2°C and RH 85 ± 5 %. An aluminium foil between the plate and the module front side simulates the module frame and guarantees proper contacting (**Fig. 58**).

The modules were characterized before and after PID testing by electroluminescence (EL), IV measurements, reflection and IQE. Measurements were taken on both sides of the module to establish whether the degradation was occurring on the front side, rear side or both.

The IV measurements of modules were done to determine changes in J_{SC}, V_{OC}, efficiency, FF, and pseudo-fill factor pFF (**Fig. 59** and **Fig. 60**). The origin of the power drop in the PID effect is a decrease of J_{SC} and V_{OC}. Fill factor and pseudo fill factor stay nearly constant for all samples, which indicates that PID does not cause cell shunting. The severe J_{SC} degradation measured in experiments suggests an additional effect, e.g. a decrease of the diffusion length in the emitter due to contamination by in-diffused ions. More detailed characterization is needed to identify the root cause of this degradation mechanism.

The EL measurements were taken to obtain the impression of the behaviour of solar cells under PID stress. **Fig. 61** shows examples of EL images for the mini-module before and after the PID test. The EL reveals localized defects of the module after PID state where lower signal means that the non-radiative recombination in the solar cell has increased. This is another indication that the power drop stems from a loss of front surface passivation.

Due to damage of some modules it was not possible to measure IQE after 46 hours at all samples. Comparison of the IQE of the front versus rear side (**Fig. 62** and **Fig. 63**) indicates that the degradation process is related to the degradation of the front side of solar cell. The type of texturization has no significant influence on the degradation. The IQE decreased in the range from 400 nm to 700 – 800 nm, although no change was observed from 800 nm to 1100 nm. This could be caused by the increase of the value of the front surface recombination velocity, which leads to the decrease of spectral response in the short-wavelength region (λ < 500 nm). Short-wavelength photons are absorbed in the heavily doped part of the emitter. Therefore the change of IQE spectrum could be caused by the enhanced front surface recombination.

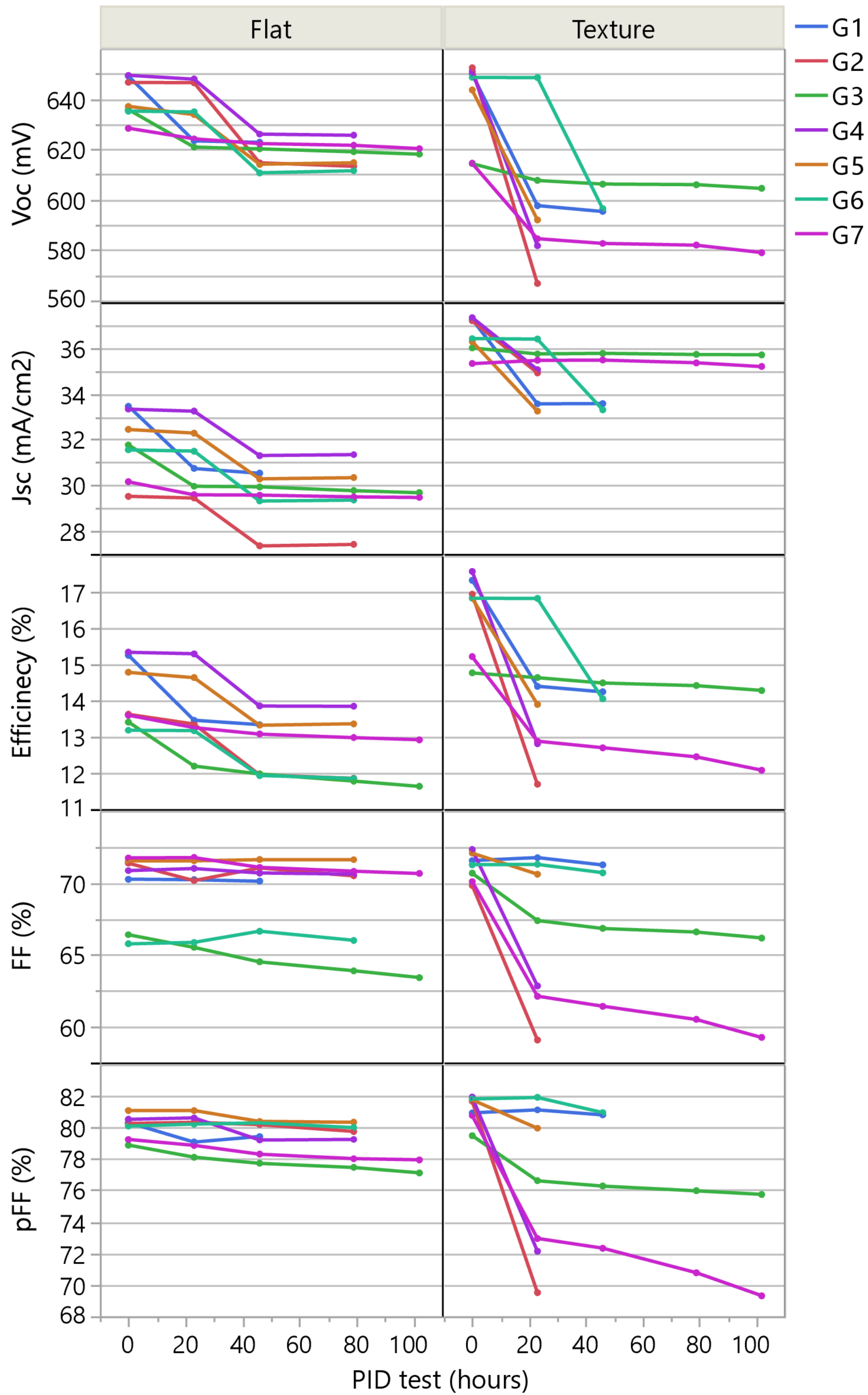


Fig. 59: IV results measured on module level during PID test on the front side of the solar cell. The IV measurements were done at 25 °C and under AM 1.5 spectrum with illumination intensity of 1000 W/m^2.

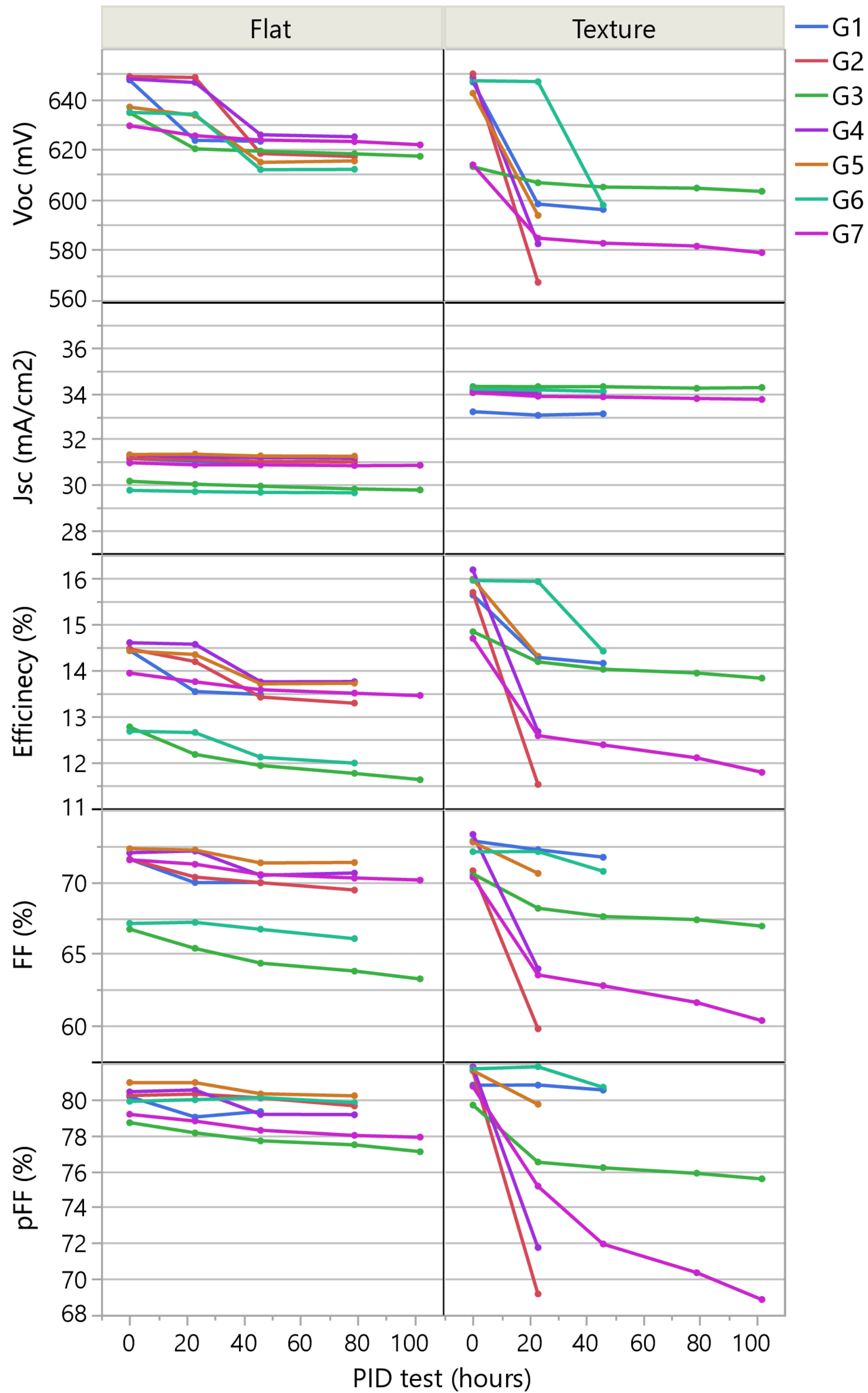


Fig. 60: IV results measured on module level during PID test on the rear side of the solar cell. The IV measurements were done at 25 °C and under AM 1.5 spectrum with illumination intensity of 1000 W/m^2.

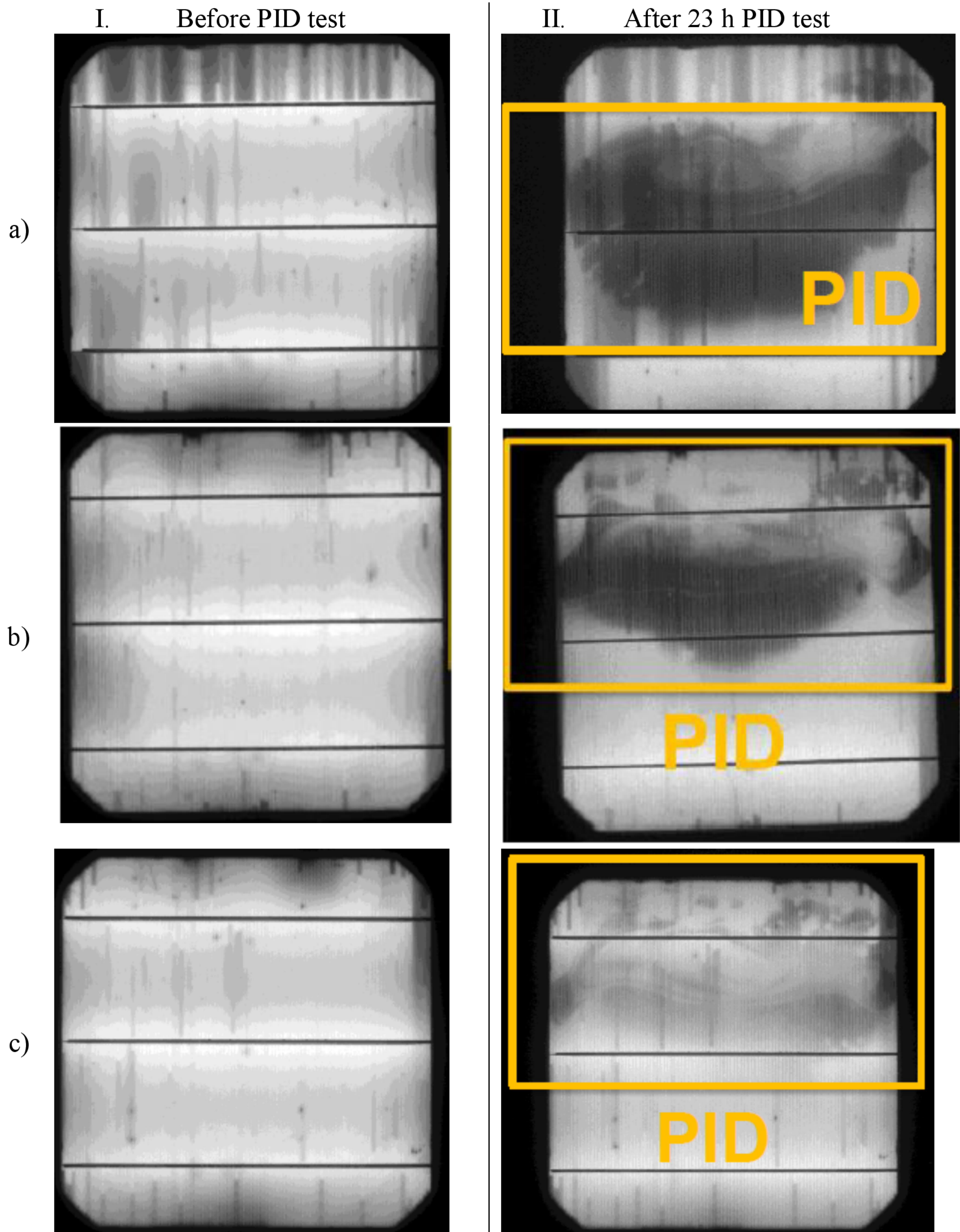


Fig. 61: EL picture of samples G2, G4, and G5 with textured surface in the initial state (I.) and after 23 h degradation (II.)

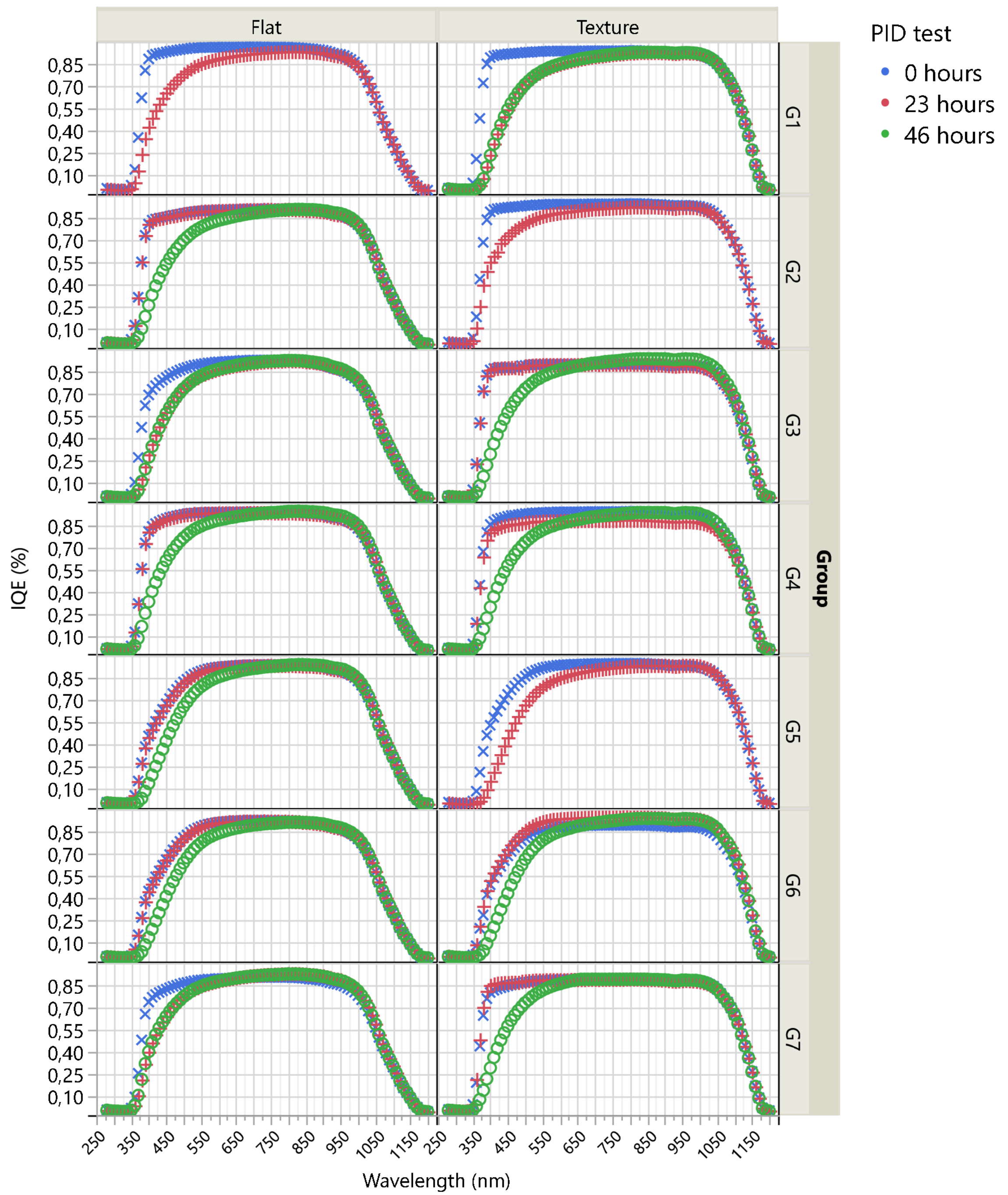


Fig. 62: The internal quantum efficiency IQE measured on the front side of the solar cell where this side was textured or flat.

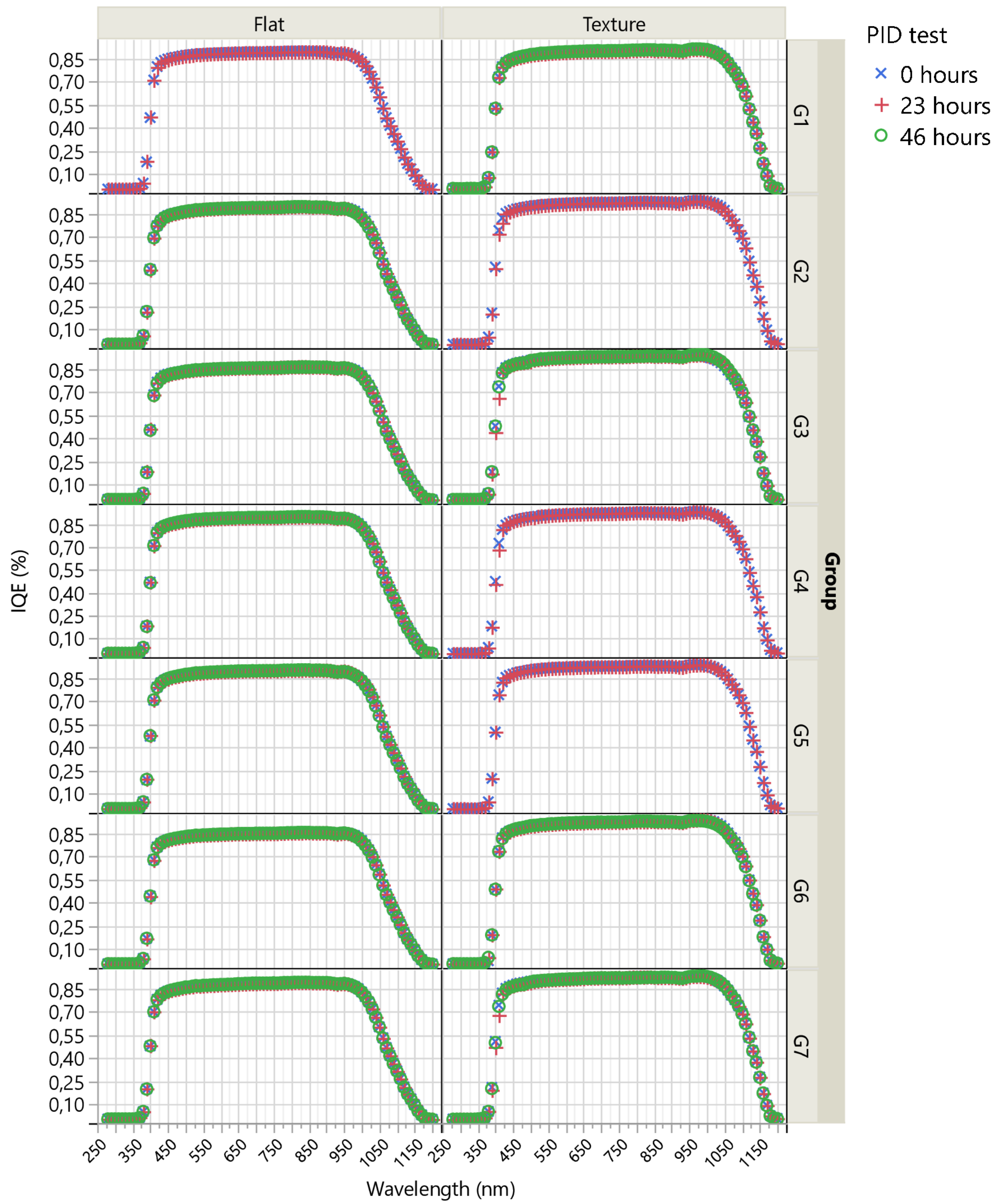


Fig. 63: The internal quantum efficiency IQE measured on the rear side of the solar cell where the front side was textured or flat.

3.3 Metallization of boron emitter

One way to increase crystalline silicon solar cell efficiency is based on optimized metallization. These main loss mechanisms are related to metallization – optical shading losses, electrical series resistance losses and losses arising from recombination under metal contacts. Uniform and low contact resistances between the metallization grids and emitters are very important for achieving high FF for screen printed silicon solar cells. Therefore, many studies have been dedicated to the process of metallization, finding optimal conditions or metallization pattern for each cell design.

At the beginning, differences in behaviour of metallization paste during firing depending on temperature profile or composition of process atmosphere were examined. This was the aim of the experiment, described in chapter 3.3.1, which was focused on differences in behaviour of metallization paste during firing, among other things, in different atmosphere. Chapter 3.3.2 is a follow-up of this experiment (3.1.1) and analyses the comparison of metallization induced recombination losses on *n*-PERT emitter caused by pure silver and silver-aluminium paste.

Among the above mentioned, there are other possibilities how to reduce metallization induced losses and lowering of contact resistivity, e.g. double print, point-contact, and floating busbars. The investigation of these alternatives to the standard printing scheme is carried out in chapter 3.3.3.

However, the firing process has also big impact on the resulting properties of metallization. The influence of the wafer and fingers/busbars orientation during firing in the infrared belt furnace is described in chapter 3.3.4.

3.3.1 In-situ resistance measurement

Changes in the contact microstructure affect the electrical resistance in various ways. The in-situ contact resistance measurement is a method allowing observation of some basic changes in the paste during firing. This is important because the mechanism of contact formation is not completely described and using this measurement method gives an opportunity to investigate the process of sintering in real time.

In this case, the influence of sintering conditions on the formation process of screen printed contacts on passivated boron doped p^+ emitters was measured by resistance R_C changes during firing. Two thick film pastes (pure silver and silver-aluminium) were compared at two different temperature profiles described later, and at atmospheric concentration of O_2. Further, the influence of the O_2 concentration on resistance was investigated for one temperature profile.

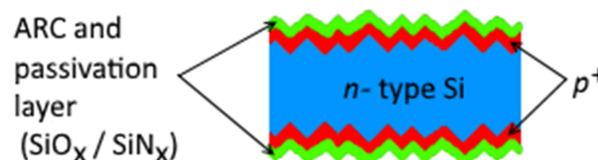


Fig. 64: Schematic cross-section of the symmetric samples.

For this experiment, 6-inch *n*-type mono-Si substrates after IMEC cleaning, saw damage removal in a KOH solution and texturing in a NaOH solution were used (**Fig. 64**). The emitter was created by atmospheric pressure diffusion using BBr_3 as a source. The resulting sheet resistance of emitter was measured by four probe method, and the result was R_{Sh} = 75 Ω/sq on the average. The emitter depth was measured using ECV measurement and it was ca. $d = 0.6$ µm. A 70 nm thick passivation and antireflection stack of PECVD SiN_X/SiO_2 was deposited.

The influence of sintering conditions was observed using two different silver pastes from various producers (named A and B). Both pastes are designated for fine line front side metallization – boron emitter metallization. Paste A was pure silver paste, paste B was silver-aluminium paste. The testing structure was created by 4 mm × 1 mm screen printed spots at 50 mm distance (**Fig. 65**). This structure was chosen due to its simple positioning of measuring contact.

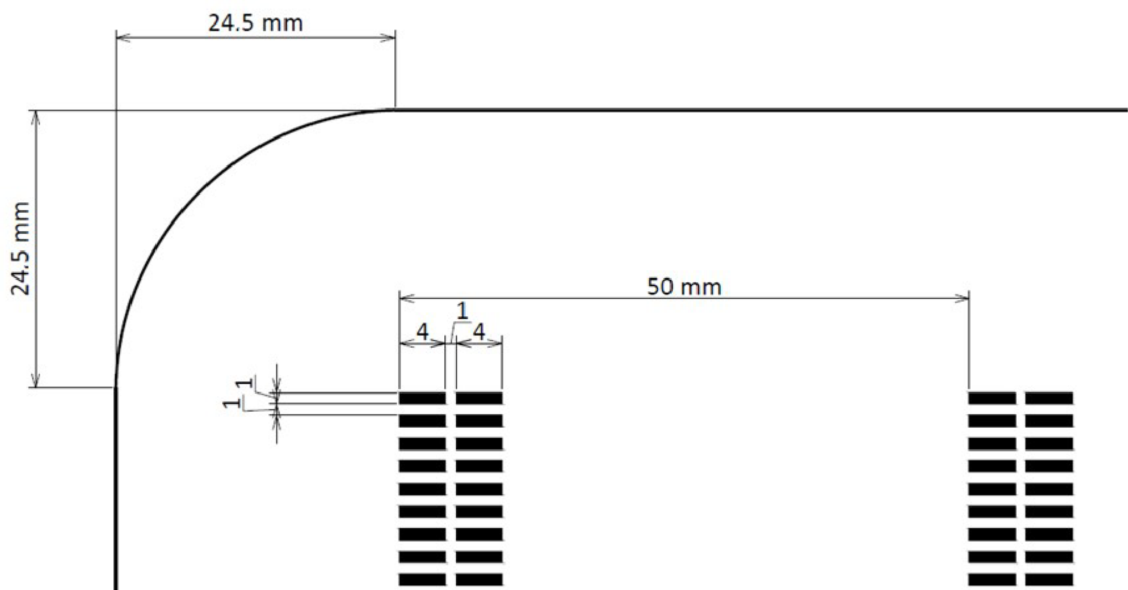


Fig. 65: Metallization pattern used for in-situ resistance measurement.

This experiment was done with a rapid thermal processing (RTP) furnace modified for in-situ resistance measurements (**Fig. 66**), where the change of resistance was measured simultaneously with the temperature. The resistance was measured using four point method. Two molybdenum alloy probing wires were encapsulated in a ceramic guide jacket and contacted the paste spots on the substrate from the top. K-type thermocouples contacted the sample from the front and rear side to control the temperature during the process. The course of resistance was recorded for temperature above ca. 300 °C.

Fig. 66: RTP furnace modified for in-situ resistance measurement.

Tab. 8: The main parameters of used temperature profiles.

	Time	48 sec	208 sec	Oxygen content
Profile 480	Target Temperature	ϑ_H = 480 °C	ϑ_{peak} = 800 °C	21 %, 10 %, 5 %, 0 %
Profile 400	Target Temperature	ϑ_H = 400 °C	ϑ_{peak} = 800 °C	21 %

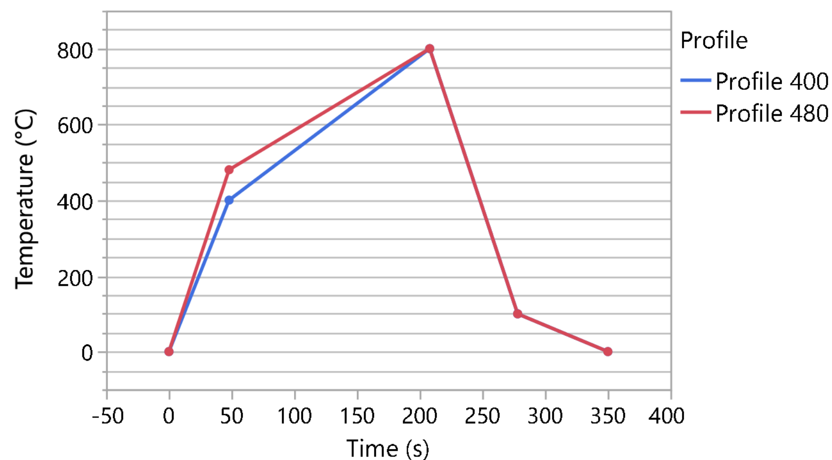


Fig. 67: Used temperature profiles.

In this experiment two different temperature profiles labelled Profile 480 and Profile 400 were used (see **Fig. 67** and **Tab. 8**), which varied in the first temperature ϑ_H. In the case of Profile 480, the first temperature was set up to ϑ_H = 480 °C with a heating rate of 10 °C / sec. The second temperature was set up to ϑ_{peak} = 800 °C with a heating rate of 2 °C / sec. Immediate cooling then took place with a cooling rate of 10 °C / sec

down to 100°C. Profile 400 differed from Profile 480 in the first set up temperature $\vartheta_H = 400$ °C and in a heating rate, which was set to 8.33 °C / sec. The second temperature was set up to $\vartheta_{peak} = 800$ °C with a heating rate of 2.5 °C / sec. The cooling was identical with Profile 480.

The firing of metallization was done in an atmosphere of N_2/O_2 gas mixture. In the case of Profile 480, the composition of the process gas was changed using the O_2 concentration between 21 % and 0 % keeping the total gas flow constant. The required concentration of O_2 was achieved by controlling the variation of the O_2 concentration in the N_2 atmosphere. The O_2 concentration at the first measurements for both profiles was coincident with the concentration in the atmosphere (21 % O_2). Afterwards, it moved downwards to 10 %, to 5 %, and finally to 0 %. In the case of Profile 400, only the measurements with 21 % O_2 were taken.

The resistance changes for Profile 480 are shown in **Fig. 68**. The resistance was alternating between conductive states and insulating states during firing. From the resistance dependence on the temperature it is obvious that at the beginning there was no conductive connection between testing spots. They were separated from the substrate by deposited antireflection and passivation layer. The burning through the passivation layer at temperature ϑ_{BT} is indicated by the first conductive state.

From graphs of paste A (pure silver paste) it is evident, that with the reduction of O_2 concentration, the first insulating state became shorter and the temperature ϑ_{BT} decreased from 525 °C (21 % O_2), over to 519 °C (10 % O_2), and 513 °C (5 % O_2), to final 465 °C (0 % O_2). Between 750 °C and 800 °C fluctuations occurred between insulating and conductive state in the case of all samples. These fluctuations were most probably caused by rearrangement of silver particles in the liquid glass phase.

In the case of paste B (silver-aluminium paste), the reduction in time of the first insulating state was more significant compared with paste A. The reduction of O_2 concentration decreased the temperature ϑ_{BT} from 665 °C (21 % O_2) to 491 °C (10 % O_2), hereafter to 494 °C (5 % O_2) and finally to 398 °C (0 % O_2). Between 750 °C and 800 °C, fluctuations occurred between insulating and conductive state in the same way as in the case of paste A.

From comparison of **Fig. 68** a) and **Fig. 69** it is obvious, that the reduction of the first target temperature ϑ_H had a bigger impact on the resistance profile of the paste B. Time necessary to burning through the ARC and passivation layer became shorter in both cases. The temperature ϑ_{BT} decreased from 525°C to 480 °C for paste A, and from 665°C to 368 °C for paste B. Up to 630°C, the paste B became conductive and no further insulating state was found.

It is clear that in-situ resistance measurements proved to give insight in the kinetics of contact formation and showed differences in the contact formation process for different O_2 concentrations and temperature profiles. The temperature required for burning through the dielectric layer could be determined from the resistance profile.

a)

b)

c)

d)

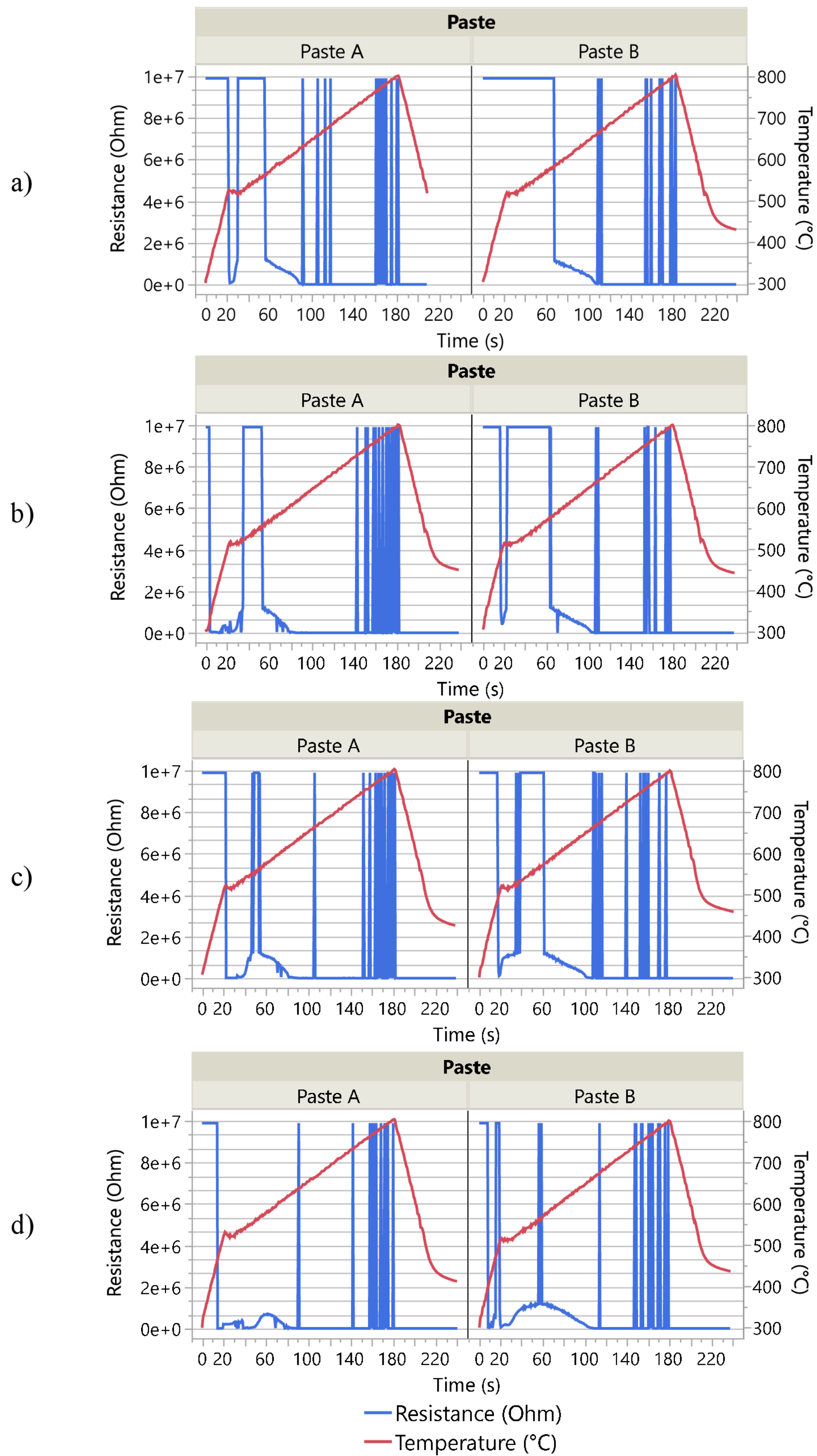


Fig. 68: In situ resistance measurement using Profile 480 with: a) 21 % of O_2; b) 10 % of O_2; c) 5 % of O_2; d) 0 % of O_2 in process atmosphere.

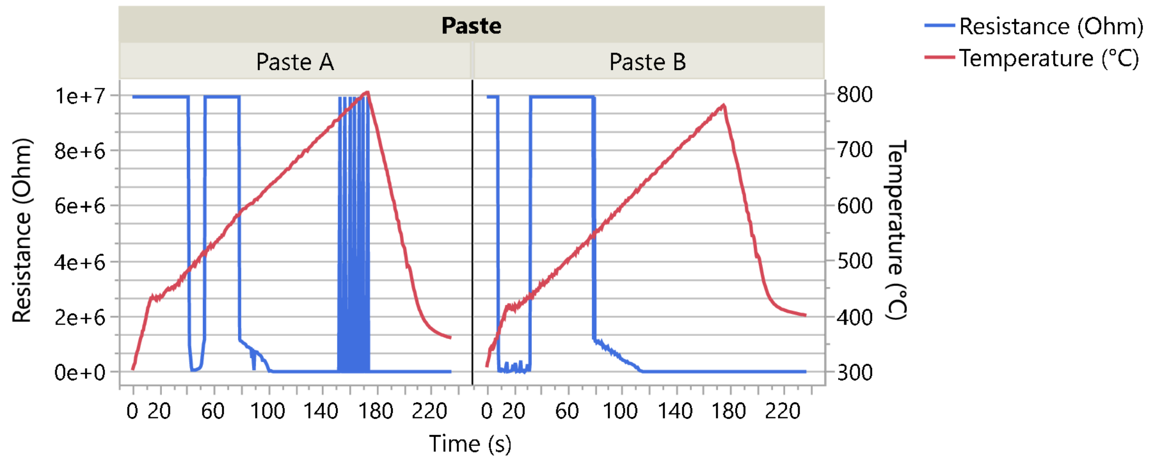


Fig. 69: In situ resistance measurement using Profile 400 with 21 % of O_2 in process atmosphere.

3.3.2 Metallization induced losses

As the metallization is one from the major sources causing decrease in efficiency, the following experiment focused on metallization induced losses was done to find the balance between doping profile and composition of metallization paste. The metallization induced recombination losses of bifacial silicon solar cells were investigated by examining saturation current densities $J_{0\text{-}met}$ underneath the metal contacts. The $J_{0\text{-}met}$ losses were determined for pure Ag paste and AgAl paste to establish the possibility of printing metallization by pure silver paste on boron emitter.

The experiment was done using *n*-PERT solar cells (**Fig. 30**) with homogeneous boron diffused emitter and phosphorus diffused BSF on *n*-type mono-Si wafers. The 6-inch Cz-Si wafers (239 cm^2) with base resistivity 2.5 – 3.0 Ωcm were processed using standard industrial processes. All wafers were textured using wet chemical alkaline process, followed by cleaning in HCl, HF, and Piranha solutions. In the next steps, diffusion in a quartz tube furnace containing $POCl_3$ (75 Ω/sq n^+ BSF) or BBr_3 (p^+ emitter,) and deposition of thermal SiO_2/PECVD-SiN_X stack was done.

For this study, five different boron emitters were realized with different doping profile, and resulting sheet resistance. The boron emitters varied in the depth $d_{emitter}$ (in the range 0.53 µm and 0.73 µm), and the peak surface carrier concentration N_A and so the resulting sheet resistance R_{Sh} ranged between 70 Ω/sq and 127 Ω/sq (**Fig. 31**, **Tab. 2**). To determine the saturation current densities $J_{0\,E\,pass}$ of the passivated boron emitter, symmetric life-time samples (**Fig. 64**) were fabricated in parallel with the solar cells.

In the last step, the finger grid at the front side and the rear side was screen printed using a commercial firing-through silver-aluminium paste (only front side) or a pure silver paste (both sides). The metallization fraction was variable on the front side to extract the $J_{0\text{-}met}$ under the metal contact for each combination of emitter/paste (**Fig. 70**,

Tab. 9) while it was kept constant on the rear side of the solar cell. The cell process was finished by co-firing of the metal contacts in the infrared heated belt furnace.

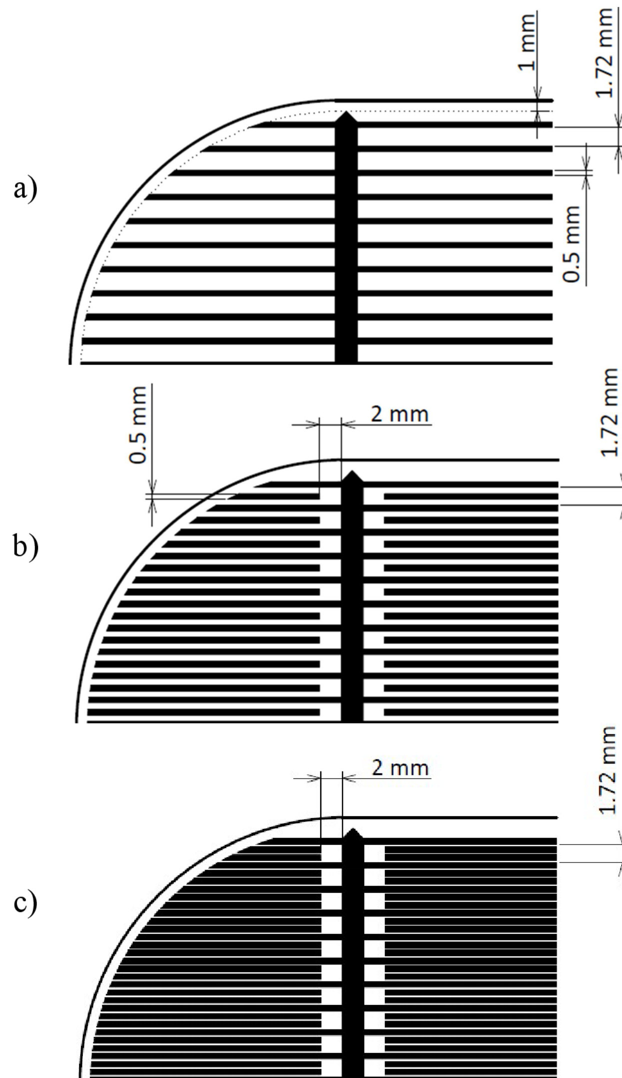


Fig. 70: Metallization patterns used for $J_{0\text{-}met}$ calculation.

Tab. 9: Overview of used metallization fraction F_M.

Paste	Metallization fraction F_M [%]		
AgAl	4.43	12.29	20.16
Ag	4.51	12.52	20.53

The metalized solar cells were investigated by IV measurements to determine the values of J_{SC} and V_{OC}. The solar cells were measured under AM 1.5 spectrum with illumination intensity of 1000 W/m^2 and temperature of 25 °C. The metallization induced

recombination losses for different boron emitters were calculated from IV data using method described in [75]. The dependency of $J_{0\text{-}met}$ on the junction depth $d_{emitter}$ is shown in **Fig. 71**, dependency on the peak surface carrier concentration $N_{A\ peak}$ is in **Fig. 72**.

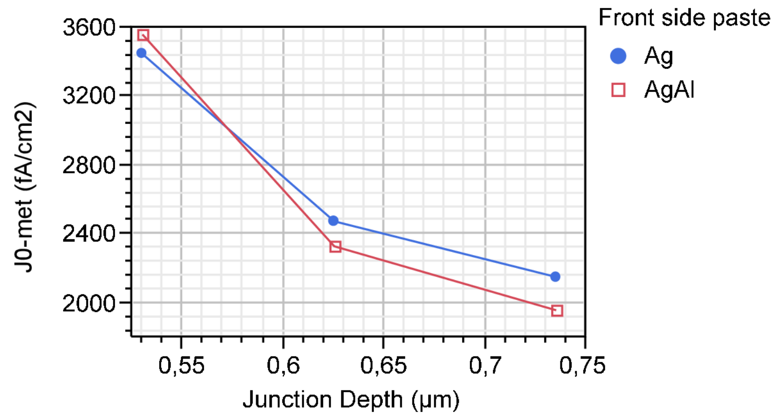


Fig. 71: The dependency of metallization induced losses $J_{0\text{-}met}$ on the junction depth $d_{emitter}$.

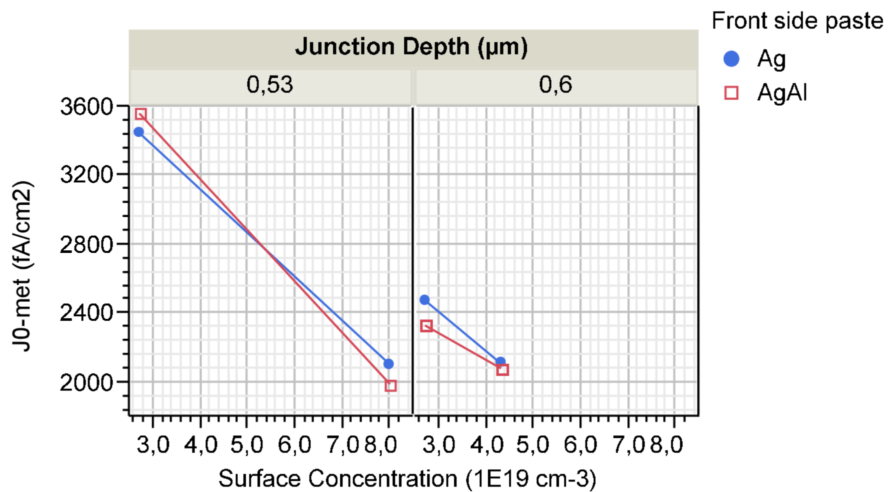


Fig. 72: The dependency of metallization induced losses $J_{0\text{-}met}$ on the peak surface carrier concentration $N_{A\ peak}$ for two different junction depths $d_{emitter}$.

From the results in **Fig. 71** and **Fig. 72** it is obvious that almost similar $J_{0\text{-}met}$ values were obtained when boron emitters were contacted by silver-aluminium firing-through paste (industrial state-of-the-art) or pure silver paste. Deeper junction ($d_{emitter}$ more than 0.6 µm) led to the lower recombination underneath the metal contacts. The lowest $J_{0\text{-}met}$ values were obtained for doping profile A7 with high surface carrier concentration N_A, and for doping profile B4 with high emitter depth. However, the results A7 were in a strong contrast with the results described in chapter 3.1.1, where low surface carrier concentration was the optimum. Based on these results, the possibility of metallization printing by pure silver paste on both sides was included to the standard process.

3.3.3 Metallization variation

Finger dimensions change or use of non-firing paste give another approach to how the negative effect of metallization can be reduced. A strong loss in V_{OC} for solar cells using this metallization has been observed when comparing the iV_{OC} of passivated cell precursors with the actual V_{OC} of the finished solar cells [86] [87]. This could result from the high emitter surface recombination at the contacts, which can be overcome by decrease of the area metallized by firing-through paste. On that account, the following experiment was done.

The *n*-PERT solar cells (**Fig. 30**) with homogeneous boron diffused emitter (standard profile, R_{Sh} = 70 Ω/sq) and phosphorus diffused BSF (R_{Sh} = 75 Ω/sq) on *n*-type monocrystalline Si wafers were made. The 6-inch Cz-Si wafers with base resistivity 2.5 – 3.0 Ωcm were processed using standard industrial processes. All wafers were textured using wet chemical alkaline process, followed by the B-clean (HF/O_3 and HCl/HF). In the next steps diffusion in quartz tube furnace containing $POCl_3$ (n^+ BSF) or BBr_3 (p^+ emitter) and deposition of thermal SiO_2/PECVD-SiN_X stack was carried out.

Tab. 10: Overview of used finger width and metallization steps.

Group	1st print paste A	2nd print paste B	2nd print paste C	Distance between fingers
G1	50 µm	only busbars		1.719 mm
G2	pads 20 µm	38 µm + busbars		1.719 mm
G3	20 µm	38 µm + busbars		1.719 mm
G4	20 µm	38 µm + busbars		1.719 mm
G5	38 µm + busbars			1.719 mm
G6	20 µm		38 µm + busbars	1.719 mm

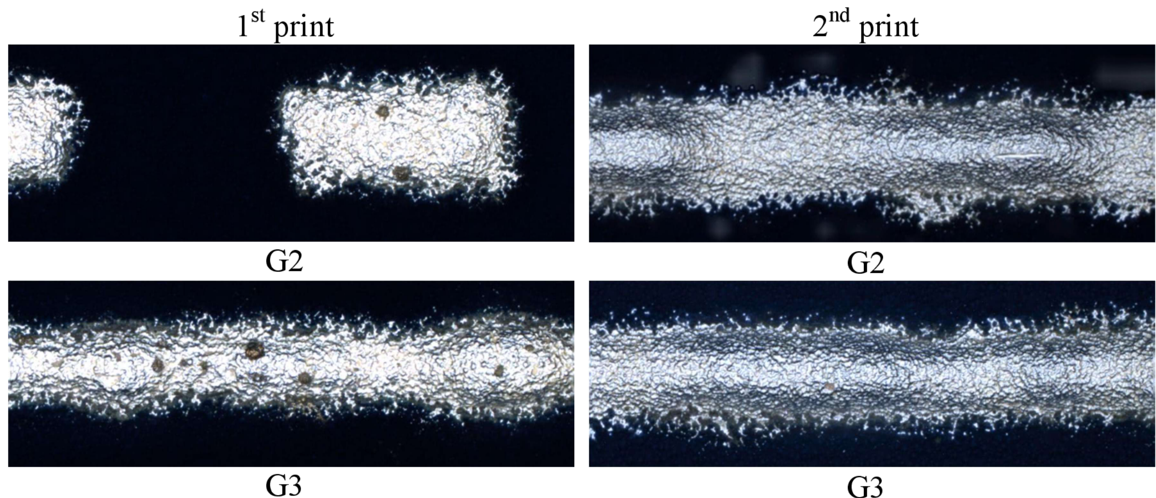


Fig. 73: Examples of printed patterns.

For this study, six different metallization schemes were realized; see **Tab. 10** and **Fig. 73**. The group G1 underwent the standard metallization. The metallization of

samples G2 was carried out by 20 µm pads connected by 38 µm finger to see the possibility of metal paste reduction in comparison. The metallization in the case of G3 and G4 was carried out from 20 µm fingers covered by the 38 µm fingers printed together with busbars but using screens with different mesh. Therefore, the fingers in the case of G3 consisted of more metal paste than samples G4. The metallization in the case of samples from group G5 was printed in one step including printing busbars and finger together. The samples G6 were used to establish the possibility of reduction fired-through area using non-firing paste. This non-firing paste was used to get the same metal amount on finger as in samples G3.

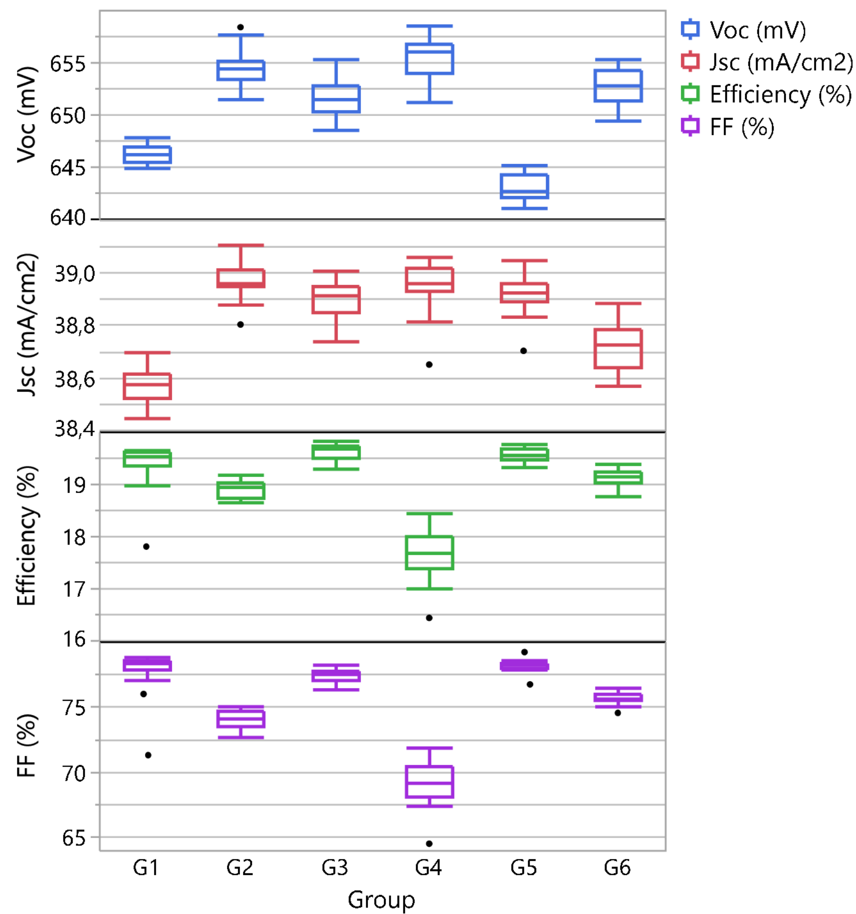


Fig. 74: Solar cell parameters obtained by IV measurement at 25 °C and under AM 1.5 spectrum with illumination intensity of 1000 W/m^2.

After firing metallization, the IV measurement **(Fig. 74)** and PL measurement **(Fig. 75)** were taken. The V_{OC} is around 5 mV to 12 mV better for all double printed groups (G2 – G4, G6). From comparison between G1 and G5 follows small V_{OC} gain if the busbars are printed separately. This phenomenon was investigated separately in the experiment described in the following chapter (3.3.4). The J_{SC} values for all groups except G1 and G6 are comparable between ca 38.85 mA/cm^2 and 39.00 mA/cm^2. The lower value in case of G1 is mainly caused by shading. The lower J_{SC} of G6 probably results from the existence of oxide layer created during firing between firing through

and non-firing pastes. The best efficiency and FF were achieved by samples from G3 using double print 20 + 30 µm. All other groups performed worse. From PL images (**Fig. 75**) it is clear that the highest V_{OC} was achieved in the case of G2 and G4 samples.

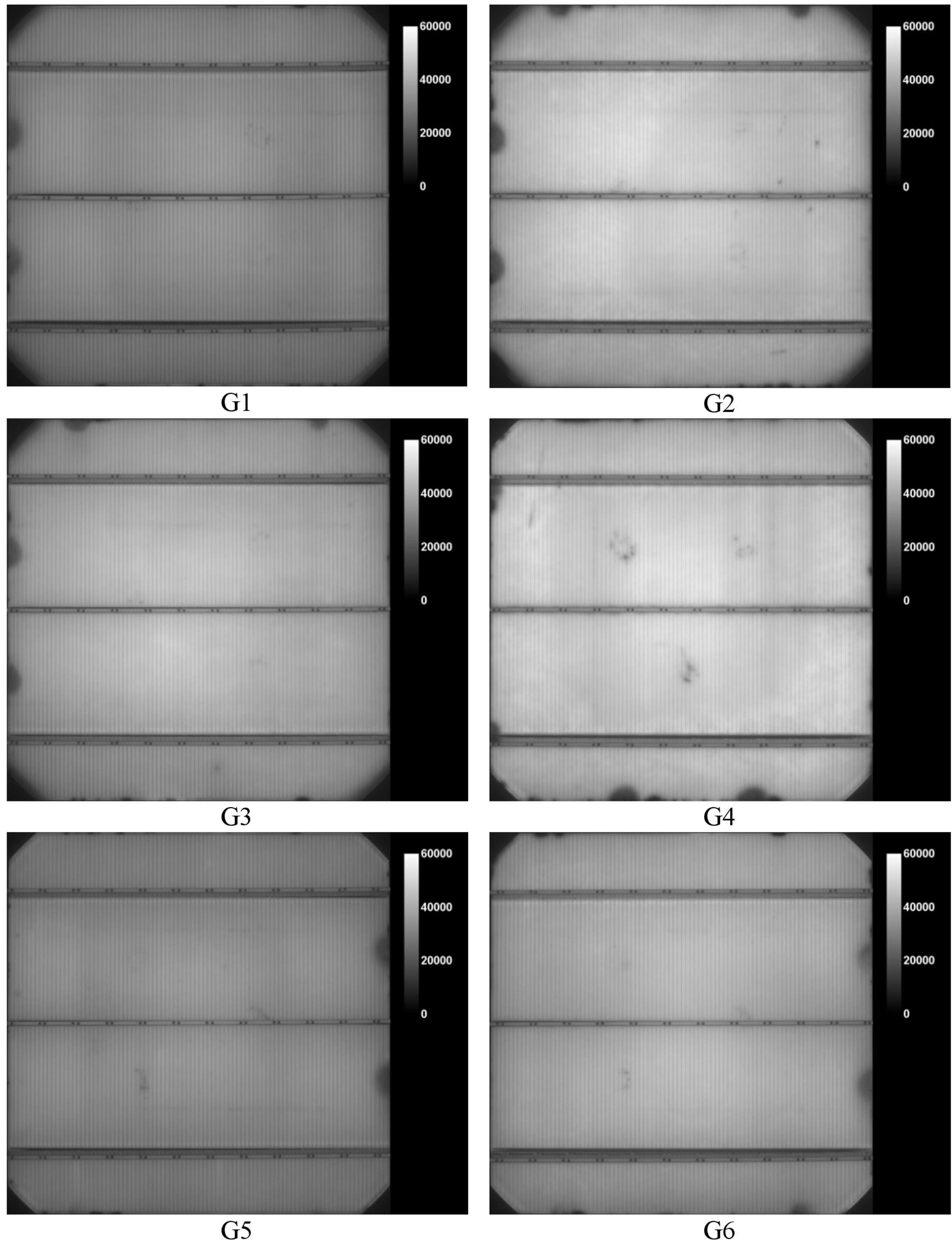


Fig. 75: Examples of solar cells PL images with different metallization. The light intensity correlates with V_{OC}.

After the IV and PL measurements, the samples were laser-cut and the line resistivity RL was measured using four point probe method. High R_L values for group G6 were caused by low conductivity of the non-firing paste. Other three double printed groups (G2 – G4) show comparable line resistivity results. The group G1 has the lowest R_L, owing to the line width of 50 µm instead of 38 µm (in total) used in the rest of the samples. Difference between G3 and G4 results from lower amount of paste printed on G4 samples.

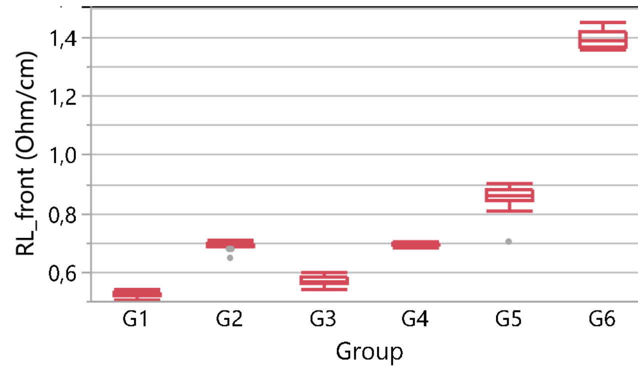


Fig. 76: Line resistivity of front side metallization.

3.3.4 Wafer orientation during firing

Apart from the dimensions of the busbars and fingers and the paste composition, there is another factor influencing the final contact resistivity – firing, where the result depends, apart from other things, on the orientation of the wafer on the belt and on the presence of the busbars during firing. In this work the „grey finger“ phenomenon, related to this problem [64] was studied on boron doped surfaces. By measuring contact resistivity, the impact of short-circuit effect was quantified.

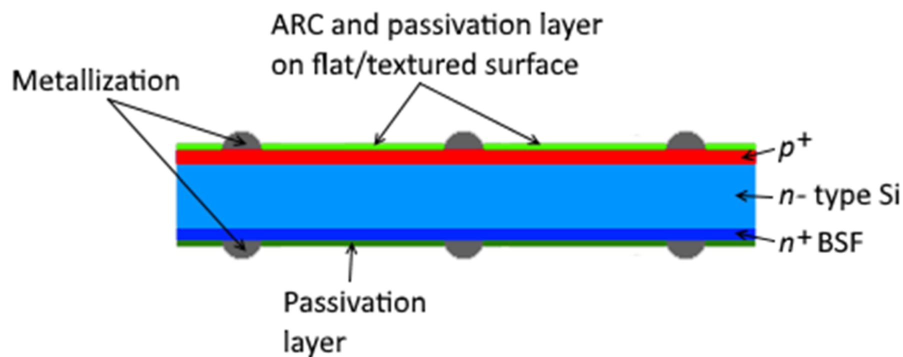


Fig. 77: Schematic cross-section of the samples with different surface topography.

The samples (**Fig. 77**) were fabricated using 6-inch monocrystalline Cz-Si wafers with base resistivity 2.5 – 3.0 Ωcm. All wafers were textured using wet chemical alkaline process, which led to alkaline textured surface, followed by cleaning in HCl and HF solutions. In the next steps diffusion in quartz tube furnace containing $POCl_3$ (n^+ BSF) or BBr_3 (p^+ emitter, 85 Ω/sq), and deposition of stack of thermal SiO_2/PECVD-SiN_X was performed.

After annealing, but before the metallization step, the QSSPC measurement was taken to obtain the iV_{OC} and J_0 values (**Fig. 78**). There were no significant differences between groups, thus it can be expected that resulting differences would come from firing process.

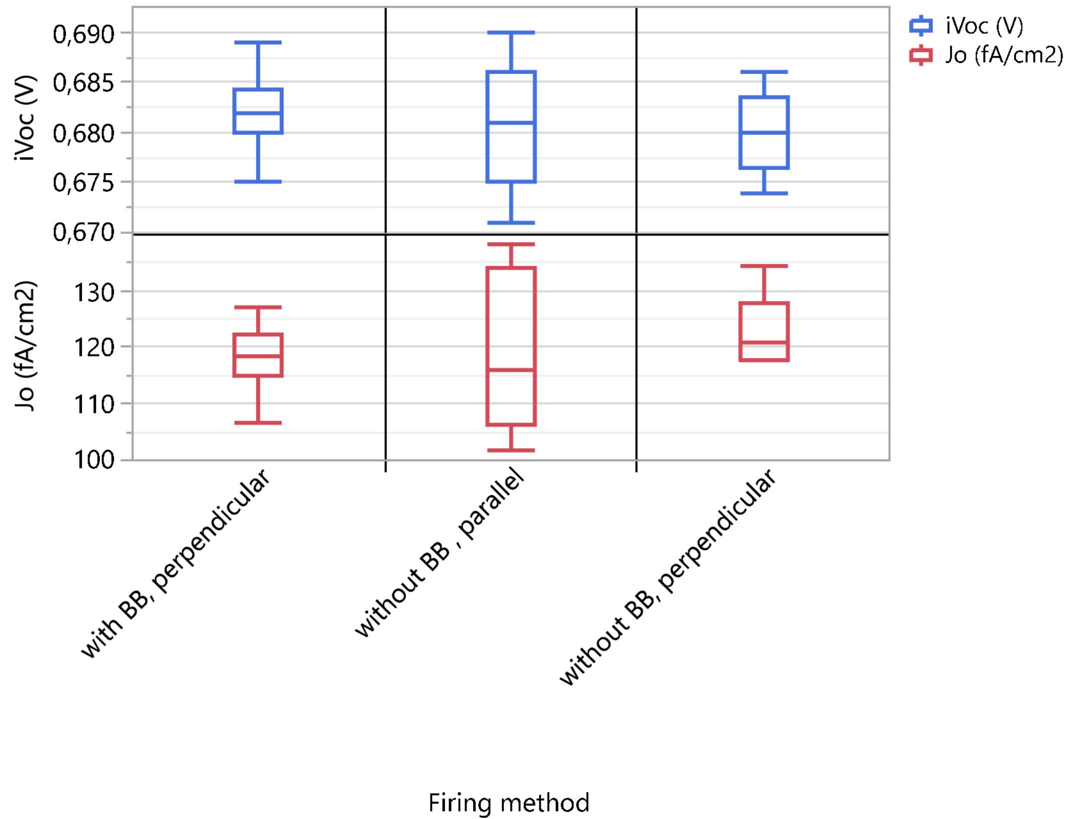


Fig. 78: iV_{OC} at 1 sun and J_0 of the cell precursors (before metallization). The J_0 was extracted at an injection level of $\Delta n = 3 \cdot 10^{15}$ cm^{-3}.

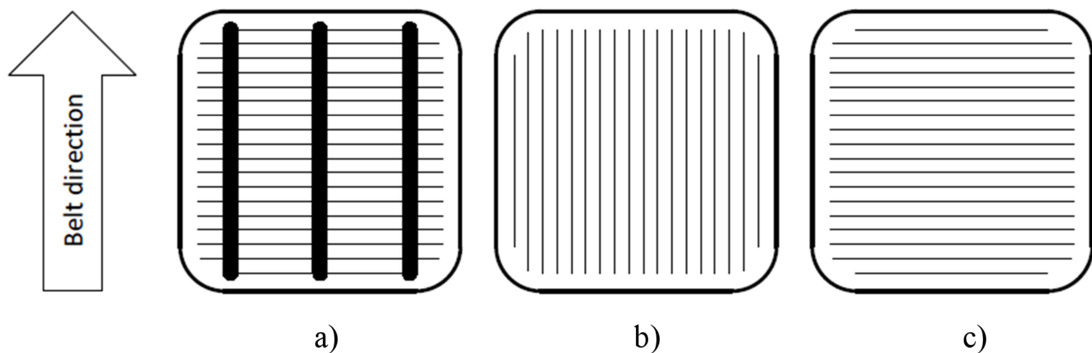


Fig. 79: Simplified screen layout that includes fingers and 3 busbars, and layout that excludes the busbars to mitigate the short-circuit effect.

A commercially available firing-through pure silver paste or silver-aluminum paste were applied for metallization, where two screens were used. The first screen had a conventional H-pattern with 3 busbars (**Fig. 79** a). To mitigate the so called "short-circuit" effect, the H-pattern layout was modified so that only fingers were printed and fired (**Fig. 79** b, c). The metallization was dried and subsequently fired in an infrared-heating belt furnace. To establish the influence of wafer orientation during firing, the wafers were positioned with finger perpendicular (**Fig. 79** a, c) or parallel to the belt (**Fig. 79** b). On the cells where only finger were fired, the busbars were created afterwards by a non-firing paste which was only dried

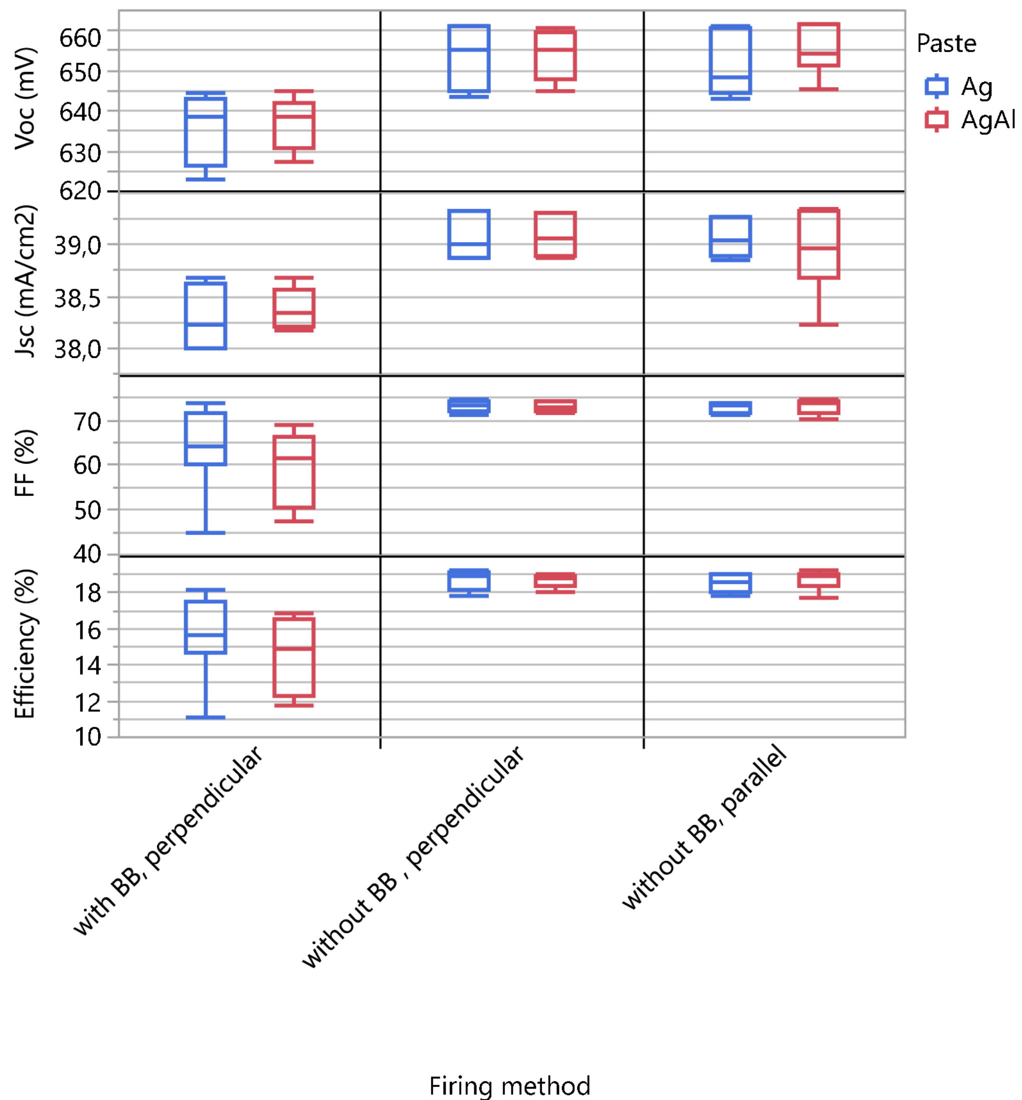


Fig. 80: Solar cell parameters obtained by IV measurement at 25 °C and under AM 1.5 spectrum with illumination intensity of 1000 W/m^2.

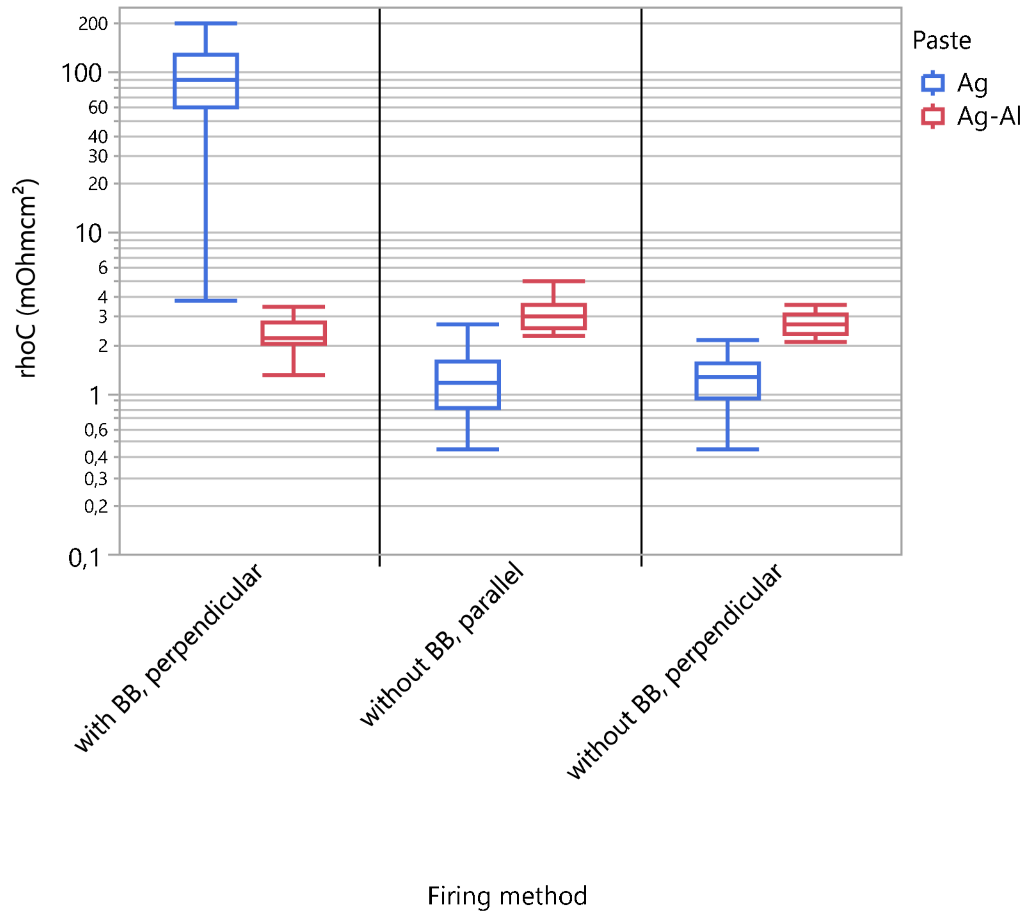


Fig. 81: Contact resistivity ρ_C of Ag and AgAl metallization on boron emitter.

After firing metallization, the IV measurement was taken and from the results in **Fig. 80** it is clear that the worst combination of printing and firing was printing of Ag paste with busbars (average values: V_{OC} = 639 mV, J_{SC} = 38.3 mA/cm^2, FF = 62 – 65 %; η = 15.5 %). In the case of the cells fired without busbars the orientation didn't play important role (average values: V_{OC} = 650 – 655 mV, J_{SC} = 39 mA/cm^2, FF = 73 %; η = 18.5 – 19.0%).

Finally, the samples were laser-cut and the contact resistivity was measured using transfer length method. Totally 12 points distributing evenly over the wafer were measured on each sample. **Fig. 81** shows the measured contact resistivity ρ_C of metallization. The best contact (the lowest contact resistivity) was achieved on samples being fired without busbars, independently on the wafer orientation. The ρ_C was in the range 0.5 mΩcm^2 and 3 mΩcm^2. This is in correlation with the results obtained by IV measurement.

Firing with silver printed busbars led to a very high contact resistivity (over 60 mΩcm^2) and it is clearly not suitable for solar cells. The lower value of ρ_C was measured on the textured surfaces metallized by silver-aluminium paste and it is disused later.

The high values of ρ_C on boron doped surface can depend on the amount of electrons in the doped silicon surface, which plays a key role in the silver-ion reducing reaction [88]. Due to the lack of free electrons in the boron layer, the conditions for creating silver-silicon contact on this surface are much stricter. The use of pure silver paste to contact boron emitter in the combination of low electron concentration and short circuit effect is only possible for firing without busbars.

For silver aluminium paste there was no significant difference on contact resistivity between firing with and without busbars. The contact resistivity was measured around 3 mΩcm^2 which was slightly higher than in the case of pure Ag paste.

The results of this work supported the applicability of short-circuit effect in the case of boron emitters. Based on the stated facts, the possibility of printing and firing metallization without busbars was considered. However, high difficulty of contacting non-firing paste on module level forestalled the implementation for the standard process.

Conclusion

This dissertation thesis describes newly introduced additional processes and methods for preparation *n*-PERT solar cells using standard production line, equipped almost equally like the one for production *p*-type solar cells. I had the great opportunity at the International Solar Energy Research Center Konstanz (ISC Kontanz) to do the experimental part of work there. The purpose of the work was to apply newly set up processes and ways to improve the structure of the cell and obtain good resulting parameters of the cell with focus on using standard mass-production facilities such wet alkaline texturization, atmospheric BBr_3 and POCl tube diffusion, passivation by BSG / PECVD SiN_X stack, screen printed and fired through metallization. This means to find the most suitable boron emitter profile, define the parameters and composition of passivation and antireflection coating, and last but not least decrease losses caused by metallization. All these steps had to be changed with regard to other parts of production.

This dissertation thesis made a useful contribution to clarification and describing connections between the main production steps. Particular influences of production steps were thoroughly considered for the final structure of solar cell. This improved design and to it related adjusted process parameters were finally put into practice. Moreover it was found out, that silver-aluminium paste for contacting boron emitter can be replaced by pure silver paste without detrimental effect on efficiency.

Because of using standard production devices not laboratory, the main goal was not to fabricate *n*-PERT cell achieving record efficiency within its category, but to set up all processes to increase the cell efficiency within the ISC Konstanz. Used methods and processes were restricted to those which are designated for industry and allow “cheap” mass-production. Simultaneously, the metal-free process for passivation was preferred to the one containing Al_2O_3.

Efficiency and to it related parameters V_{OC}, J_{SC}, and FF were chosen to compare finished cells between each other. In 2014 the best cell achieved J_{SC} 39.5 mA/cm^2, V_{OC} 654 mV, FF 79.0 %, and efficiency 20.4 %. It is obvious that the set goal was achieved, when the parameters of the best solar cell described in this dissertation achieved in the end of 2016 these values: J_{sc} 39.3 mA/cm^2, V_{OC} 663 mV, *FF* 80.1 %, and efficiency 20.9 %. For the case of a cheap full-size solar cell, produced at the standard mass-production line, such parameters could be regarded as sufficient.

It is worth mentioning that newly introduced processes and methods not only helped to increase the efficiency, V_{OC}, and *FF* of prepared cells but also bring considerable improvement in other parameters. The better quality of passivation and ARC layer has an impact on J_0 and iV_{OC} values, which were iV_{OC} = 684 mV, J_0 = 81 fA/cm^2 respectively. The line resistivity R_L of metallization on the front surface decreased below 0.8 Ω/cm, largely due to double printed fingers. Firing only fingers without busbars led to the contact resistivity ρ_C of silver metallization around 1.25 mΩcm^2 and

from 2.8 to 3.0 mΩcm^2in case of silver-aluminium. The results can be summarized in following points, matching individual technological steps.

Diffusion and oxidation processes

For the proposed *n*-PERT solar cell concept it was necessary to find new ways of diffusion and oxidation processes to obtain the most suitable boron emitter profile on the front surface. The possibility of using wet oxidation process was also explored together with comparison between low pressure and atmospheric pressure boron diffusion. The results from this part can be summarized as follows:

1) The highest efficiency of cell was achieved for those with emitter profiles combining low surface carriers concentration and high junction depth. Low carrier surface concentration ensures good surface passivation and its optimal value was found close to $N_{A\ peak}$ ca $2.5 \cdot 10^{19}$ cm^{-3}. The junction depth $d_{emitter} = 0.6$ µm at least contributes to the reduction of contact recombination losses (see chapter 3.1.1).

2) From the experiment focused on metallization induce losses emerged, that the lowest $J_{0\text{-}met}$ values were obtained for doping profile with high surface carrier concentration. Consequently, it is necessary to set up the balance between these two opposing requirements very carefully (see chapter 3.3.2).

3) Regarding the comparison of diffusion recipes with dry or wet oxidation process, there was a minimal difference in the shape of doping profile and maximal boron concentration between them. The method of wet oxidation was successfully validated (see chapter 3.1.2).

4) All low pressure processes showed high quality passivation (low J_0, high iV_{OC}) therefore, it is applicable to the production of *n*-type high efficiency solar cells (see chapter 3.1.2).

Passivation layers and antireflective coating

Design and subsequent verification of new optimal structure or passivation layers and antireflection coating was performed and it significantly improved the cell efficiency thanks to reduction of recombination losses while maintaining the light trapping effect.

1) As the first step it was necessary to establish the minimum thickness of the SiO_2 or BSG layer, which serves as separating layer between emitter and SiN_X layer. To achieve a good passivation quality, a 10 nm thick layer of SiO_2 is needed as minimum, together with PECVD SiN_X layer with a low refractive index ($n = 2.0$) (see chapter 3.2.1).

2) The passivation degrades if the chemical composition of SiN_X changes towards more Si-rich (higher refractive index), despite the fact that the layer contains more hydrogen, which would have been expected to enhance good passivation. The reason seems to be that, at the same time, the deposition of SiN_X increases

the density of interface states, as well as the positive interface fix charges (see chapter 3.2.2).

3) The most suitable combination of PECVD SiN_X thickness and peak firing temperature allowing achievement of low contact resistance was defined. At combination of SiN_X thickness 84 nm and temperature ϑ_{peak} = 780 °C the contact resistance ρ_C was below 1 mΩcm^2 (see chapter 3.2.3).

PID prevention

According to literature, the prevention of Potential Induced Degradation (PID) could be solved at the cell level using different composition of ARC and passivation layer, deposited on flat/textured emitter. A new structure respecting this founding was proposed and verified in experiments. Although the intended results have not been achieved, few common conclusions can be drawn (for more details see chapter 3.2.4)

1) From the results it is obvious, that the degradation process is related to the degradation of the front side passivation stack layer, where the boron emitter is present.
2) The PID is caused by the enhanced front surface recombination.
3) The type of texturization has no significant influence on degradation on the front side.

The design of this part is complicated by the fact that optimal ARC and passivation stack preventing PID must ensure good passivation and optical properties to preserve the cell efficiency at the same time. Successful completion of this part is likely to take a lot of time and can be addressed in the continuation of work.

The kinetics of screen printed contact formation

Using the in-situ resistance measurement method brings the possibility of relatively accurate capture and description what happens during firing of contact structures. This part is described in chapter 3.3.1.

1) Thanks to this technique it was possible to record resistance changes during firing of metallization under different conditions. The temperature required for burning through the dielectric layer was determined from the resistance profile.
2) Using this in-situ method, the differences in behaviour of pure silver and silver-aluminium paste during firing in different process atmospheres were observed.

The contact resistivity and to that related short-circuit effect

Contact phenomena are very complex. Among other things they are influenced by firing process, by SiN_X thickness, paste composition and by printing scheme. The proposed design of contacts has been tested in many experiments. This part of work clarified the influence of the main technological parameters to the metallization.

The results showed that:

1) The metallization properties depend primarily on the firing profile and much less on the SiN_X thickness (see chapter 3.2.3).
2) The metallization induced losses were similar regardless of the paste composition (Ag or AgAl). It was established that pure silver paste can be used for contacting both sides of solar cell instead of silver-aluminium paste for the emitter side and pure silver only for the rear side (see chapter 3.3.2).
3) Double printed metallization with firing-through paste gives better results than single printed metallization (see chapter 3.3.3).
4) Separately printed fingers and busbars can increase cell performance, together with right wafer positioning on the belt during firing. This is closely related to the „grey finger“ phenomenon causing short circuit effect, which was confirmed in *n*-type solar cells by different authors [64] [88] [89] (see chapter 3.3.4).

Resulting cell parameters and comparison of achieved results

The newly introduced processes and methods helped to increase the efficiency of the best cell from 20.4 % to 20.9 %. The improvements in other parameters were not negligible, for example V_{OC} from 654 mV to 663 mV, FF from 79.0 % to 80.1 %. For the case of the cheap 6-inch solar cell, produced at standard mass-production line such result could be regarded as sufficient. The J_{SC} slightly decreased from 39.5 mA/cm^2 to 39.3 mA/cm^2. This small decrease can be considered as insignificant because the value 39.3 mA/cm^2 is still high enough. Nowadays increasing efficiency of solar cells is mainly connected with increasing of V_{OC} which is technologically much easier than increasing J_{SC}. What concerns other parameters, the iV_{OC} reached 684 mV and and J_0 81 fA/cm^2, R_L was reduced below 0.8 Ω/cm. The average value of ρ_C was ranging between 1.25 mΩcm^2 and 3.0 mΩcm^2, depending on wafer orientation during firing and paste composition.

The experiments were finished in the end of 2016 and since then the *n*-PERT cell concept has been in focus of many companies and research teams. The record *n*-PERT cell from IMEC (made 2017) has the average batch efficiency of around 22.4 % (the best cell 22.8 %), using electro-plated NiAg metallisation on both sides, which is not very suitable for low-cost production [18]. Their industry-compatible solar cells developed in 2018 within the collaboration of EnergyVille, and Jolywood have average batch efficiency of 21.9 %. This design uses Ag screen printed metallisation on the front and Al screen printed metallisation on the rear side [90].

The team members of the ISC moved from the standard *n*-PERT structure towards upgraded design called *n*-type Passivated Emitter and Rear Totally diffused Rear Junction (*n*-PERT-RJ), achieving efficiency of 21.78 % [91].

Challenges for future work

Although the achieved cell efficiency of 20.9 % is, as stated before, in the case of cheap full-size solar cell, produced at standard mass-production line, quite sufficient, there are few other ways for further improvement. One way consists in the field of metallization, including grid pattern and material for metallization allowing easy interconnections between cells on the module level, or point-contacts to minimize resistance losses.

Regarding the passivation and ARC layer, it is necessary to establish the optimal composition allowing high quality passivation, easy contacting and preventing PID on the cell level.

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List of abbreviations

ALD	Atomic Layer Deposition
AP	Atmospheric-Pressure
a-SiN_X:H	Hydrogenated SiN_X with Amorphous Character
BiCoRE	Bifacial Co-diffused Rear Emitter
BSG	Boron-Silicate Glass
Cz	Czochralski
ECV	Electrochemical Capacitance-Voltage Measurement
EL	Electroluminescence
EQE	External Quantum Efficiency
EVA	Ethylene-Vinyl Acetate Copolymer
IBC	Interdigitated Back Contact
IQE	Internal Quantum Efficiency
HET	Heterojunction
HP	High-Perfomance
IQE	Internal Quantum Efficinecy
LID	Light Induced Degradation
LP	Low-Ppressure
LPCVD	Low Pressure Chemical Vapour Deposition
mc	Multicrystalline
mono	Monocrystalline
μ-PCD	Microwave-Detected Photoconductive Decay
NAOS	Nitric Acid Oxidation of Silicon
PEVCD	Plasma Enhanced Chemical Vapour Deposition
PERT	Passivated Emitter, Rear Totally Diffused
PID	Potential Induced Degradation
PL	Photoluminescence
PSG	Phosphosilicate glass
PV	Photovoltaic
QSSPC	Quasi-Steady-State Photoconductance Technique
SDE	Saw Damage Removal
Si	Silicon
TLM	Transmission Line Model Method

List of symbols

A	Area
A_{cell}	Solar cell area
$C_{junction}$	*p-n* junction capacitance
C_s	Doping concertation along the ingot
C_0	Total doping concentration in the melt
d_{ARC}	ARC layer thickness
$d_{emitter}$	Emitter depth
d_{SiNX}	Thickness of SiN_X layer
E	Input light irradiance
FF	Fill factor
f_s	Solidified fraction
I_{fp}	Current through the outer pair of probes
I_{SC}	Short circuit current
$\mathrm{i}V_{OC}$	Implied open-circuit voltage
J_0	Dark saturation current density
k	Segregation coefficient
k	Boltzmann's constant
N	Dopant density
$N_{A\,peak}$	The highest boron concentration
n_{ARC}	Refractive index of ARC material
n_i	Intrinsic carrier concentration
n_0	Refractive index of air
n_1	Refractive index of SiN_X
P_{max}	Maximum power point
p_{FF}	Pseudo fill factor
q	Unit charge of the electron
s	Spacing between point probes
R_{Sh}	Sheet resistance
T	Temperature
t_{BSG}	Thickness of the BSG layer
$t_{deposition}$	Deposition time
$V_{applied}$	Bias voltage
V_{fp}	Floating potential difference between the inner probes
V_{OC}	Open-circuit voltage

Δ	Phase difference
Δn	Injection level
ε_0	Permittivity of the vacuum
ε_r	Relative permittivity
η	Conversion efficiency
Θ	Angle of incident beam
ϑ_{peak}	Peak temperature

ϑ_H	First target temperature
λ	Wavelength
λ_0	Free-space wavelength
λ_{min}	Wavelength at the minimum of the reflectance curve
ρ_{base}	Base resistivity
ρ_C	Contact resistivity
τ_{eff}	Minority carrier life time
ψ	Amplitude ratio
V_{fp}	Floating potential difference between the inner probes
V_{OC}	Open-circuit voltage