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NOVEL APPROACH TO POLYMORPHISM IN GATE-LEVEL DIGITAL CIRCUITS

NOVÝ PŘÍSTUP K POLYMORFISMU ČÍSLICOVÝCH OBVODŮ NA ÚROVNI HRADEL

EXTENDED ABSTRACT OF A PHD THESIS
ROZŠÍŘENÝ ABSTRAKT DISERTAČNÍ PRÁCE

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Abstract

Nearly twenty years ago, a non-conventional approach to implementation of multifunctional circuits called polymorphic electronics was proposed. The concept of polymorphic electronics allows to implement two or more functions in a single circuit, whereas the currently selected function depends on the state of the circuit operating environment. Key components of such circuits are polymorphic gates. Since the introduction of polymorphic electronics, several dozens of polymorphic gates have been published. However, a large number of them do not meet reasonable parameters. As a result, perspective of their utilisation for real applications becomes rather bleak. This dissertation introduces a new approach to the polymorphic electronics. It is based on gates whose behaviour depends on polarity of dedicated power supply rails. The goal of this thesis is to show that such approach allows to design gates with significantly better parameters. In order to systematically design proposed gates at the transistor level, an evolutionary method based on Cartesian genetic programming was proposed. That allowed to design several sets of efficient polymorphic gates employing conventional MOSFET and emerging double-gate ambipolar transistors. These gate sets were arranged into a library which is currently freely available for other researchers. Furthermore, a number of more complex circuits based on proposed gates were designed in this thesis. It is demonstrated at various levels of circuit design (gate, RTL, application) that the proposed gate-level polymorphism provides significant advantages compared to the first generation of polymorphic gates, but it can also be competitive or even better compared to the conventional CMOS solutions.

Keywords

Polymorphic electronics, multifunctional gate, polymorphic gate, ambipolar transistor, MOSFET, digital circuit, PoLibSi.

Reference

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Chapter 1

Introduction

Nowadays, significant majority of logic circuits is typically realised by means of using widespread CMOS technology. Although the first physical implementation of CMOS-based logic circuit has been successfully demonstrated more than 55 years ago [71], this technology still prevails as the major choice even in case of cutting-edge electronic devices.

In fact, last several decades have brought only a minor advancement regarding the structural and implementation aspects of basic Boolean functions (logic gates) in CMOS technology. When it comes to the target implementation size of logic circuitry, CMOS gates seem to be very optimal (only a few transistors are needed to implement a Boolean function). Thus, even very complex behaviour can be realised on a small silicon die.

In certain classes of applications, it is required to have more different functions implemented in a single circuit, whereas just one of them is always active. In such situations it makes sense to think about optimisation of the circuit size. The easiest possible implementation of such a circuit is to implement all functions separately on the silicon die and to switch their outputs according to the current needs. In order to accomplish higher functional density (more features within a similar chip area or number of transistors), the reconfiguration scheme is sometimes utilised [7].

Reconfigurability brings more effective ways how to implement certain applications and allows new applications of electronics. It makes the hardware more flexible. This is one of the features that make software so popular as a way to implement various systems. However, a wide range of applications still needs to be implemented in hardware. Thus, the reconfiguration is (and will be henceforward) very important for a significant class of applications.

Typical implementation of hardware reconfiguration consists of a field of reconfigurable elements connected by a changeable interconnection network, a reconfiguration controller and a memory that serves as a storage for different configurations. This approach allows to implement two or more digital circuits using one hardware. The field of reconfigurable elements might usually assume various granularity levels – from coarse-grained elements like functional units or data processing units on RT level to a transistor-level fine-grained field of elements [78]. It allows not only the classic reconfiguration scheme (the hardware changes its structure and behaviour according to the configurations created beforehand), but also implementation of so-called evolvable hardware (new configurations are being created just as a direct response to the actual circumstances) [28].

The flexibility of described reconfiguration approach is paid by overhead in the time domain. The change of function consumes certain period of time. It is caused by presence of only one hardware (field of configurable elements) for more configurations. Previous

configuration must be replaced by a new one. Naturally, some space is also required for the reconfigurable circuit, the memory and the reconfiguration controller.

In 2001, Stoica et al. proposed somewhat non-conventional approach to the implementation of multifunctional digital circuits called *polymorphic electronics* [64]. This approach could be understood as another (and quite different) conception of hardware reconfiguration. On the contrary to the conception of classic reconfiguration, where reconfigurable elements are connected by means of an universal interconnection network, polymorphic circuits look like ordinary digital circuits (just tightly coupled elements) and the change of the circuit function is triggered only by the change of behaviour of its elements (typically gates). If these multifunctional elements are implemented effectively and the circuit synthesis is performed cleverly, the final circuit is very efficient in both area and time domains. In fact, the function change is almost immediate and, moreover, overhead in the size domain for an additional circuit function could also be very low. Neither additional memory nor any reconfigurable controller or reconfigurable network is needed.

1.1 Polymorphic electronics

Polymorphic electronics [64] can be characterised as a relatively new discipline in the field of digital circuits and systems. Its notion depicts a group of digital circuits that have the ability to perform more than one function, while the wiring of a given circuit keeps the same layout in all the intended operating modes. Selection of the corresponding function, which the circuit is going to execute, depends on the actual state of the target operating environment. Because the basic building blocks of polymorphic electronics (polymorphic gates) are sensitive to the target operating environment directly, there is no need for any central reconfiguration controller, nor any dedicated control signal connected to all multifunctional components, which would cause the reconfiguration. That increases the efficiency in implementation of polymorphic circuits.

All modes (functions) of the polymorphic circuits are designed inside the circuits completely intentionally. No mode results from any fault, caused e.g. by exceeding operating parameters of the circuit. Polymorphic circuits are usually synthesised from the polymorphic gates. The change of function of the whole circuit is caused by the change of Boolean functions performed by individual polymorphic gates. In the first generation of polymorphic gates, the change of gate function was reached by the change of operating points of the employed transistors – by such factors or environment, which influence the operating points of transistors. It can be physical quantities like a supply voltage level [45, 61, 65, 63], voltage of a dedicated control signal [42, 64, 75, 76], chip temperature [48, 62, 64, 70] or even its illumination [64].

Interconnection of all circuit components remains always the same. Switching of the circuit modes (functions) happens thus naturally and immediately. There is no need to wait for completion of any reconfiguration or any other sequential operation. Because the detection of environment state is a built-in feature of the individual gates themselves, no part of the polymorphic circuits can be identified as a sensor, which is sensitive to the physical quantity and which would serve for distribution of the measured values into the remaining parts of the circuit. Polymorphic circuits could be thus much smaller than similar circuits created by conventional design methods (circuits consisting of several monofunctional blocks and multiplexers) in terms of the overall number of transistors or layout size [44].

Although the concept of polymorphic electronics generally admits several equally important functions implemented in a single circuit, just one main and one or more auxiliary functions are often considered in practice. The mechanism responsible for the change of polymorphic circuit function implies the existence of some application domains, in which such kind of behaviour may help to get significant advantages. In general, these circuits can be used e.g. for adaptation of the circuit behaviour to variable conditions of target environment [43], for reduction of power consumption or heat dissipation in order to preserve at least the essential circuit functionality, when energy goes low or temperature goes high [46], for storing or hiding „extra“ functions used as a watermark or other special features [53], for embedded diagnostics [55], etc. Note that the environment could be both intentionally driven (to initiate the reconfiguration) or utilised as a driver of change (the circuit responds to changed circumstances).

1.2 Open problems of polymorphic electronics

The characteristic features of polymorphic electronics described above show the advantages, which could be useful for instance in certain classes of circuits, which require to change their function during the runtime. Thus, polymorphic electronics seems like a perspective research area.

Since 2001, several tens of publications have been devoted to the field of polymorphic electronics. There were designed more than thirty building blocks for polymorphic circuits (usually polymorphic gates). Two of them were even fabricated and tested with real applications of polymorphic electronics. Furthermore, several methods for synthesis of polymorphic circuits were created. A detailed state-of-the-art in polymorphic electronics is given in Chapter 2 of this thesis.

In general, a research related to the polymorphic electronics focuses on three problems of polymorphic electronics [44]:

1. Existence of suitable polymorphic components (usually polymorphic gates) with parameters competitive to the parameters of conventional gates used in the digital circuits.

2. Design of more complex polymorphic circuits using the basic components (i.e. problem of synthesis methods, which should be reliable, scalable, etc.).

3. Identification of appropriate classes of applications, where the polymorphic electronics could be more beneficial than a conventional solution.

1.3 Research objectives

This thesis deals with the first mentioned problem of polymorphic electronics – with design of the polymorphic gates as basic building blocks for polymorphic circuits.

One of the main issues behind the adoption of polymorphic electronics is given by the analogue nature of the phenomenon (quantity) influencing the circuit behaviour. It consequently leads to rather analogue design concepts of the polymorphic gates rather than staying in a purely digital domain (see Chapter 2.3). The result is that some transistors work in a linear mode or could short the power rails. That brings a lot of shortcomings (not all the published gates have all of the listed ones): High power consumption, high

propagation delay, output levels weak or even incompatible with CMOS voltage levels, long transient phenomenon, large size (in case of big differences in transistor sizes), etc. However, without enough polymorphic gates offering good properties, conventional electronics will be most likely the preferred way to polymorphic electronics in application scenarios targeting multifunctional behaviour or reconfiguration.

With the emergence of ambipolar transistors, a few bi-functional circuits were published, whose behaviour depends on the polarity of power supply voltage [73, 68]. Although such a principle seems to be promising due to the discrete nature of the control variable, it was not further investigated for design of the multifunctional digital circuits.

The following hypothesis was formulated for this thesis:

It is possible to design a complete set of two-input gates created from the existing types of transistors (MOSFET, ambipolar, etc.), where each gate in the set is able to realise two Boolean functions, where the current function is given by the polarity of the power supply rails, and where each gate from the set is better than a conventional solution of such bi-functional circuit (two conventional gates implemented in parallel + multiplexer) in terms of the overall number of transistors.

The main objective of the thesis can be divided to the following partial goals:

1. To identify possible issues or limitations related to the design of circuits controlled by the polarity of power supply voltage, if any.
2. To propose and implement a method which allows to design polymorphic circuits controlled by the polarity of power supply voltage at the transistor level, with regards to the overall transistor count.
3. To experimentally evaluate the proposed method using selected types of transistors and to tune and accelerate the design algorithm in order to speed up the circuit design process.
4. To design complete sets of two-input polymorphic gates for various types of transistors and various design constraints.
5. To evaluate other important non-functional properties of the proposed gates besides the number of transistors being used (e.g. propagation delay, power consumption).
6. To compare obtained results with the conventional implementations of such bi-functional circuits.
7. To show the advantages of proposed gate set(s) on selected applications of polymorphic electronics.

1.4 Motivation

There are two main motivations for the research connected with this thesis.

The first one is to create a set of gates with more efficient implementations (a new generation of polymorphic gates). Gates sensitive to some continuous quantity were designed by an analogue approach. That usually resulted in non-optimal parameters of such gates when attempting to keep the gates size small. Moreover, time for switching of the

circuit function could be (especially in large circuits controlled by the chip temperature) not negligible.

If the circuit function will be controlled by polarity of the power supply voltage, the behaviour of such circuit will be predictable most of the runtime due to a negligible time required for switching the polarity. Discrete nature of the control quantity could also simplify a design of such gates and could have a positive influence on their properties – all transistors can work as switches, transistors can have common dimensions, etc. That would lead to higher possible operating frequency, lower power consumption and operation without a transient phenomenon during the function change.

The second motivation is related to the synthesis of polymorphic circuits. Synthesis methods can be various in the future and therefore it is difficult to estimate which polymorphic nodes (gates) will be required by the methods. If the proposed set of gates will be complete (i.e. if the set will implement all possible combination of two-input Boolean functions), proposed gate set can be utilised by any synthesis method, regardless of the circuit representation (PolyBDD [19], PAIG [12], etc.). For each method, a suitable subset of gates can be selected.

1.5 Abstract outline

This extended abstract summarizes author's doctoral thesis. The thesis is composed as a collection of five accepted author's papers with an accompanying introductory part.

The extended abstract is organised as follows. The first chapter introduces the research area and research objectives. Chapter 2 surveys the state-of-the-art in polymorphic electronics already published in the literature. Chapter 3 summarises the research contribution and introduces the selected papers. Finally, Chapter 4 summarises the obtained results.

Chapter 2

Survey of the state of the art

As it was already outlined in Chapter 1.2, three research areas can be identified in the field of polymorphic electronics: Identification of applications, where the polymorphic electronics can bring an advantage in comparison to the conventionally designed circuits, development of suitable synthesis methods and, finally, design of suitable polymorphic components (usually polymorphic gates).

This chapter summarises the current state-of-the-art in all three research areas. With respect to the objectives of this PhD thesis, the biggest attention is paid to the currently published polymorphic gates. Note that a detailed survey of the state-of-the-art in polymorphic electronics by 2011 can be found in Růžička's habilitation thesis [44]. Although, many papers related to the polymorphic electronics have been published later, no other publication summarising the state-of-the-art in the polymorphic electronics has been created since 2011.

2.1 Applications of polymorphic electronics

Polymorphic electronics is not inherently suitable for all kinds of applications, but we believe that it can bring some improvement or advantage over conventional solutions in certain classes of applications. One of the open problems of polymorphic electronics is the identification of such suitable classes of applications.

Several possible areas of application of polymorphic electronics are already mentioned by the Stoica's team in the publication which introduced polymorphic electronics [64]. The advantage is seen in circuits having one primary function, where it would be nice to have one or more other auxiliary functions, which can be used when needed. Polymorphic electronics could be the way how to add the secondary function(s) for a low additional price. The use of added functions could be primarily in security applications according to Stoica's team: Authentication mechanism or watermark for identification, protection against the reverse engineering, where the main circuit function only occurs under certain conditions, or protection against unauthorised use by encoding sensitive data into the circuit. The publication also mentions a potential in applications where faults tolerance needs to be increased or the circuit needs to be adapted to worse conditions such as decreasing supply voltage. However, no specific application was investigated by Stoica and his team. A high number of real applications were later shown by the team of scientists from Brno University of Technology.

Stareček et al. proposed a method for improving the testability of digital circuits, where the substitution of selected conventional gates by polymorphic gates allows to generate a significantly shorter test sequence (lower number of test vectors) to test the failures than it would be necessary when using the original gates [60]. Other applications in the field of test and diagnostics are the self-checking circuits [45], for example self-checking adders that provide error information within the circuit on their outputs in the second polymorphic mode [50].

Compact dimensions and the fact, that circuit function depends on the environment conditions, predetermine the use of polymorphic electronics also in applications where the system's collapse due to unfavourable environmental conditions (high chip temperature, low supply voltage, etc.) can be prevented by timely adaptation of its behaviour, e.g. reduction of power consumption. The team of A. Stoica came up with the idea of an application that will reduce the resolution and frequency of an A/D converter during adverse conditions [64], but it has never been realised.

Similar application was proposed and implemented e.g. by L. Sekanina et al. They published a FIR filter with two operating modes [51]. The first mode was considered as a standard mode in which the filter performs a normal operation. In the other one, the filter operates with reduced power supply voltage – some filter coefficients were reconfigured, and some parts of the filter were disconnected. The experimental results indicated that while power consumption can significantly be reduced when half of the taps is suspended, the filter is still able to achieve a reasonable quality of filtering.

Růžička presented a design approach to gracefully degrading digital circuits that provides an increased chip operation reliability when battery goes low or a chip temperature cross some safe level [43, 46]. It is based on a circuit controller which decreases number of its states in the second mode. After the end of reconfiguration phase, the controller ensures only necessary functions. By this arrangement, the power and heat dissipation of the circuit is reduced until the chip temperature falls again under certain level. When the chip is cooled down appropriately, the controller returns to normal operating mode automatically. The principles of polymorphic electronics ensured fast reconfiguration, compact and cost-effective design with embedded sensors.

Since the polymorphic electronics implements multiple functions within a single circuit and it is not possible to identify parts performing individual functions, polymorphic electronics can also be used in the field of circuit security. The device may have one more hidden function that can serve for instance to identify a particular instance of a circuit. This was demonstrated by implementation of the physically unclonable function producing a unique chip ID [53].

Other published applications are e.g. transition function of cellular automaton [58] or bi-functional graphic filters [54]. Implementations of the mentioned graphical filters were further significantly improved with use of gates controlled by the polarity of supply voltage by the author of this thesis (see Chapter 3.4).

Some polymorphic gates can also be successfully used as monofunctional gates in conventional circuit design. Gajda designed a 2-bit full adder and a five-input majority function where gates controlled by a dedicated signal were utilised as conventional three-input gates. Both solutions are more efficient than the conventional solutions in terms of the overall number of transistors being used [18].

Polymorphic electronics can also be used in sequential digital circuits. Sequential controllers intended for gracefully degrading digital circuits designed by Růžička [43, 46] mentioned above were designed using a combination of polymorphic combinational circuits and

conventional flip-flops. Stoica's team created polymorphic JK flip-flops assembled from a combination of conventional and polymorphic gates [77]. An asynchronous counter allowing up- and down- counting or counter reset (i.e. three different functions) according to the target environment is provided as an example of such flip-flop usage. Following the up- and down- counter, the author of this thesis proposed combinational increment/decrement (notation with slash is typical for polymorphic circuits; increment is a function in the first mode, decrement in the other one) and adder/subtractor circuits which can be used in a wide scale of polymorphic applications [33].

2.2 Synthesis of polymorphic circuits

The problem of polymorphic circuit synthesis lies in the efficient design of circuit having desired functions from the basic polymorphic components. This problem is more complex compared to the design of conventional circuits, since more than one circuit function needs to be considered, and one common graph (circuit structure) needs to be found for all functions. Only a change in the component behaviour ensures that the circuit function is changed. This significantly reduces number of solutions in the (large) state space.

Small and simple polymorphic circuits can be designed by the *ad-hoc* approach directly by hand, just using the designer experience. However, most of the gates and circuits presented in Chapters 2.1 and 2.3 are results of the evolutionary design. Evolutionary techniques are sometimes able to find unconventional, interesting, yet functional solutions – both in the design and optimisation of digital systems [49]. It is done by searching in the state space using techniques based on Darwin's idea of gradual evolution of species with natural selection. Cartesian Genetic Programming (CGP) [29] was utilised for representation of almost all complex polymorphic circuits during the design. A high number of publications are focused on evolutionary design and optimisation of polymorphic circuits at both the transistor [65, 74, 34, 36, 35] and gate level [19, 54, 56, 79, 23]. Unfortunately, evolutionary methods are poorly scalable. Finding of more complex circuits requires larger chromosomes and thus searching in a larger state space. That makes finding of a suitable solution very time-consuming task and the probability of the finding decreases.

Synthesis methods that do not use any evolutionary algorithm nor any other heuristics to search the state space can be called as conventional. Two conventional synthesis methods were proposed by Gajda in his PhD thesis [17]. The simplest one is *polymorphic multiplexing*. It is based on polymorphic multiplexers (pmux) which propagate first input signal in the first mode and the other signal in the second mode, according to the current state of the target environment. A conventional approach is used to synthesise both circuit functions independently. The outputs of the synthesised circuits are then multiplexed using polymorphic multiplexers as shown in the left part of Figure 2.1. In order to reduce the number of gates, goal of the synthesis can be to maximise the amount of gates that are shared by both circuits (see the intersection in the right part of Figure 2.1). The other method proposed by Gajda, *PolyBDD*, is based on binary decision trees. Both methods generate functional circuits. However, it may not be optimal in terms of circuit size, so Gajda recommends the subsequent use of evolutionary optimisation techniques to obtain more optimal circuits.

Another three conventional synthesis methods were proposed by Adam Crha. The first one is based on formal Boolean representation of corresponding functions and can be successfully used for technology mapping of small polymorphic circuits for platforms based on NAND/NOR gates [10], e.g. for REPOMO32 [52]. The second method is based on

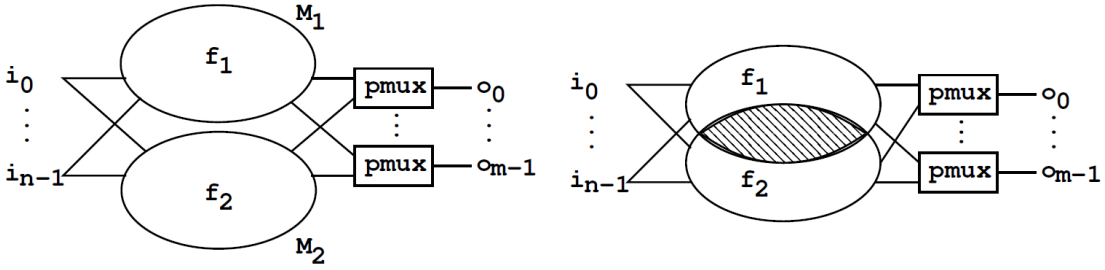

Figure 2.1: Multiplexing of conventional circuits by polymorphic multiplexers: Independent circuits (left) and sharing gates between modules (right) [17].

Boolean divisor identification and function kernelling technique [11]. Unfortunately, the method allows also only two-level circuit representation (sum of products or products of sum) and it would be poorly scalable for complex polymorphic circuits.

It seems that the most promising synthesis method could be the last method proposed by Crha [13], where the circuit is represented by so-called PAIG format – AIG representation (And-inverter graph) extended by polymorphic edges. Optimisation of such circuit is done by rewriting – replacing 4-input 1-output parts of the circuit by more efficient implementations. For an efficient mapping from PAIG to the target technology, polymorphic gates with various functions can be useful, not just common AND/OR or NAND/NOR gates. The PoLibSi library [38] created by the author of this thesis is suitable for this purpose because it provides an efficient implementation of each pair of two-input Boolean functions for three target technologies including the conventional MOSFET transistors.

2.3 Polymorphic gates

Digital circuits are mostly designed by a composition of smaller circuit structures. Parameters of such structures (delay, size, power consumption, etc.) are known during the synthesis. That can allow to generate circuits optimal for a given application. Such structures can be gates, flip-flops, various types of adders, multipliers, RTL components or for example memory cells.

Design of the polymorphic circuits is based on the same approach. As the basic components for design of polymorphic circuits, two-input gates are mostly considered. An example of larger circuit blocks can be found in [54] where 8-bit components (min/max, min/mean, max/add, etc.) were synthesised out of two-input gates.

For design of more complex polymorphic circuits, a combination of conventional and polymorphic two-input gates is mostly considered. In order to assess whether the polymorphic gates can be integrated into the conventional CMOS circuits, properties and criteria which should be fulfilled by polymorphic gates were defined in [44]. They correspond to the properties usually required from the conventional gates:

- high input resistance (the gate must avoid an excessive load applied to the preceding logic net caused by its inputs),
- low output resistance (the aim is to achieve unambiguously defined logic levels at the gate output irrespective of a given output load caused by subsequent logic net),
- power supply voltage in the range typical for CMOS circuits,

- acceptance of input signal levels in the range typical for CMOS circuits,
- output signal levels in the range typical for CMOS circuits,
- short time of signal propagation,
- low power consumption,
- small dimensions.

All polymorphic gates published so far are briefly introduced in this chapter together with their properties (if known). Note that some of the presented gates were not marked by the term *polymorphic* originally by their authors. However, their behaviour is polymorphic and thus they are also included in the state-of-the-art.

The most natural classification of polymorphic gates is a classification according to the phenomenon the gates are controlled by, i.e. according to the quantity which primarily influences the gate behaviour. The first three sub-chapters are devoted to the gates belonging to the first generation of polymorphic gates: Gates controlled by supply voltage level, chip temperature or dedicated control signal, i.e. by continuous control variables. These phenomena were proposed already by Stoica et al. in the publication introducing polymorphic electronics [64]. Such gates are based on MOSFET transistors and mostly designed as analogue circuits. Only two of them have been fabricated so far. The rest was simulated or tested in a field programmable transistor array [78].

The emergence of so-called post-silicon devices (especially ambipolar transistors) opened a path towards gates controlled by the polarity of supply voltage. The following sub-chapter pays an attention just to these gates. Because of discrete nature of the control variable and because of significantly better properties of such gates, they can be classified as a second generation of polymorphic gates.

The last sub-chapter shows other gates based on unconventional structures, which could be denoted as polymorphic (or at least multifunctional).

2.3.1 Gates controlled by supply voltage level

One of the possible approaches, how to control the polymorphic circuits, is related to the supply voltage level. The main idea is to have different functions of the circuit available for different supply voltage levels (voltage ranges). At the first sight, this approach seems very promising – the supply voltage rails are connected to all gates in the circuit and there is no need for any other dedicated signals. Such gates can be used for example in applications, which must reflect a decrease or an increase of the power supply voltage by different functions in order to prevent a circuit failure caused by a lack of energy [43]. However, the range of applications where gates controlled by supply voltage level can be utilised is actually much wider.

The existing gates controlled by supply voltage level can be identified as a special type of analogue circuits which behave as digital circuits from the outside. Not all the transistors in such gates work in the saturation mode, compared to the conventional CMOS gates [72]. The gates must contain some part sensitive to the supply voltage level. With regards to the requirements for small dimensions of polymorphic gates, such part usually consists of few transistors working in a linear mode.

If a polymorphic gate can perform two (or more) different functions, then its design must be able to change the output value for certain input combinations when the power supply

level changes. Let's show it on a NAND/NOR gate: When the gate inputs are different (0 1 or 1 0), the gate should deliver logic zero output value in case of NOR function and logic one for the NAND function. In order to keep the transistor count low, in several gates, the output value is ensured by more transistors opened at the same time, which deliver different logic values (both zero and one at the same time!) to the output. The resulting output voltage is then given by a ratio of channels conductivity of the opened transistors.

Besides the transistors working in a linear mode, different sizes of transistors are thus also typical for polymorphic gates controlled by supply voltage level. Such gates can contain less transistors than it would be needed for a separate (parallel) implementation of its functions. Although the transistor count seems promising, usage of transistors with different channel sizes can lead to larger layout of the gate (compare e.g. Figure 2.2b and Figure 2.2c). Mentioned switching of both logic zero and logic one to the output at the same time results in longer switching time and static current between the power rails for some gate inputs – power consumption of such gates can be then relatively high.

Table 2.1 shows all polymorphic gates controlled by the supply voltage level and published yet. Besides the pass-logic AND/OR gate, the rest of gates (NAND/NORs) has high input impedance. The output impedance usually depends on the current gate input values.

Table 2.1: A survey of polymorphic gates controlled by supply voltage level.

Functions	**Control value**	**Transistors count**	**Ref.**
AND/OR	1.2/3.3 V	8	[65]
NAND/NOR	3.3/1.8 V	6	[63]
NAND/NOR	3.3/1.8 V	10	[61]
NAND/NOR	5/3.3 V	8	[45]

The NAND/NOR published in [45] has both input and output levels compatible with the CMOS standard, and signal propagation time about 80 ns. Switching of both logic zero and logic one to the output at the same time (i.e. making the power rails short) results in a static current over 120 μA for some inputs [44]. For the other gates, neither valid input voltage ranges, signal propagation time nor power consumption were published. However, higher power consumption compared to the conventional gates is expected for all of them.

Two polymorphic gates controlled by the power supply voltage level were physically produced. NAND/NOR gate published in [63] is the first one. It was implemented by the Stoica's team with use of HP 0.5 μm technology. Few years later, another NAND/NOR was designed by the team from Brno University of Technology and implemented with CMOS AMIS 0.7 μm technology [45]. The latter one (shown in Figure 2.2) is most probably the most thoroughly explored polymorphic gate ever. Although its parameters (summarised above) are not ideal and the gate is not usable for commercial purposes, experiments with it took polymorphic electronics a big step forward. It was incorporated into the reconfigurable polymorphic module called REMOMO32 [52] containing 32 configurable logic elements where each of them can behave as AND, OR, XOR or polymorphic NAND/NOR. That allowed to design and test many polymorphic applications controlled by the supply voltage level, e.g. [45, 53, 57, 58].

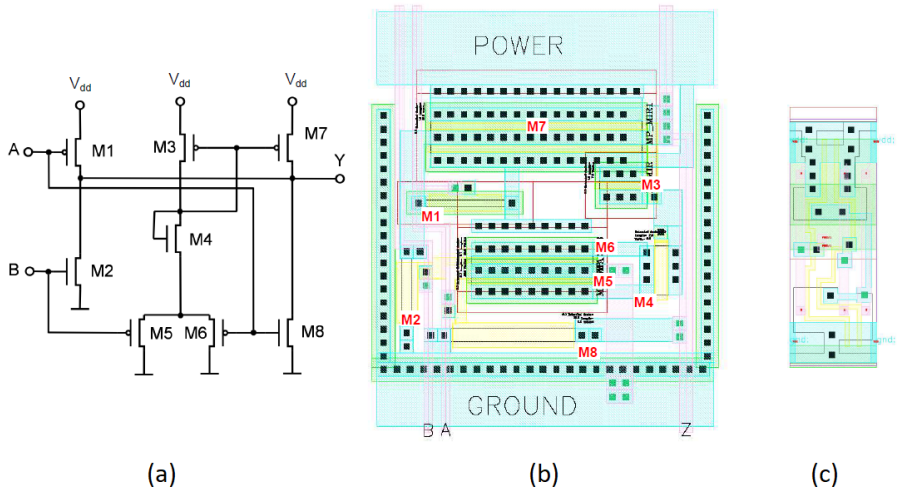

Figure 2.2: NAND/NOR gate controlled by supply voltage level [45]: (a) schematic, (b) realisation in AMIS 0.7 μm technology in comparison to (c) conventional NAND gate (4 transistors) in the same technology [44].

2.3.2 Gates controlled by chip temperature

Sensitivity of silicon semiconductor technology to the temperature of the silicon chip can also be successfully used in the design of polymorphic gates. In the conventional CMOS circuits, this sensitivity is intentionally suppressed so that the circuit performs the same function in the widest possible temperature range. However, if the circuit is designed so that the operating points of some transistors move with a change of the temperature, the circuit function may change.

The same principle is basically used also in the gates controlled by the supply voltage level, where the change of operating points occurs by changing the supply voltage. For this reason, the polymorphic circuits controlled by supply voltage level are also sensitive to the temperature and vice versa [44]. This dependence was shown on the polymorphic gate NAND/NOR from Figure 2.2 [47, 48]. If the gate was supplied by 3.3 V, at which the gate normally executes the NOR function, and the chip temperature was intentionally increased, function of the gate changed to NOT at 127 °C and then to NAND at 137 °C. When the supply voltage is higher, these temperature thresholds decrease (see Figure 2.3). There is also a certain hysteresis obvious between increasing and decreasing the temperature at a constant supply voltage in Figure 2.3.

The polymorphic gates primarily published as temperature-sensitive are listed in Table 2.2. In general, properties of those gates are rather worse. AND/OR gates published in [64] are composed of a small number of transistors with relatively small channels dimensions. However, the one with 6 transistors is a pass-logic gate with a delay up to 5 ms. The other one with 8 transistors has output levels incompatible with CMOS voltage levels: While the gate is supplied by 3.3 V, logic zero is represented by a voltage of up to 0.9 V and logic one by a voltage of down to 1.8 V at the output for certain inputs. NAND/NOR gate published in [62] is composed of 12 transistors, i.e. much more than it is needed for a separate (parallel) implementation of NAND and NOR functions. Furthermore, publication [62] provides no simulation results so it is difficult to determine other properties of the gate. NOR/NOT gate published in [70] is based on more transistors opened at the same

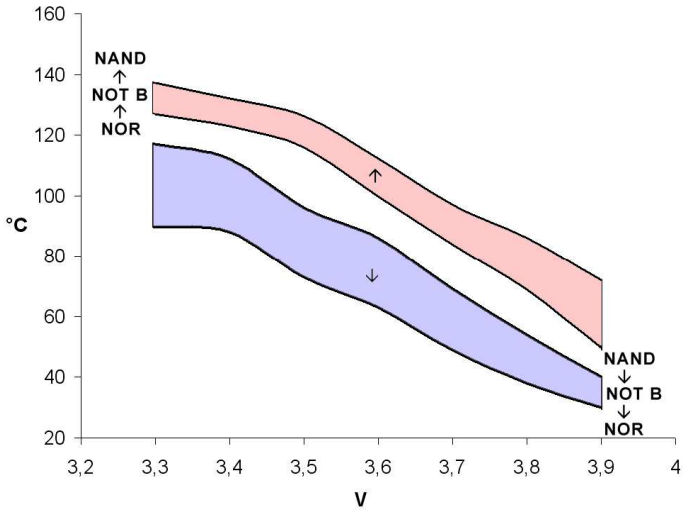

Figure 2.3: Dependence of NAND/NOR gate from Figure 2.2 on the chip temperature and supply voltage [48].

time for some inputs. It can be predicted with a certainty that all four gates will have higher power consumption in some states (for some inputs). The remaining gates listed in Table 2.2 (AND/BUF, NAND/NOT and OR/AND) are only mentioned in [70] without any schematics. Thus, it is not possible to determine any of their parameters.

Table 2.2: A survey of polymorphic gates controlled by chip temperate.

Functions	Control value	Transistors count	Ref.
AND/BUF	25/125 °C	7	[70]
AND/OR	27/125 °C	6	[64]
AND/OR	5/90 °C	8	[64]
NAND/NOR	80/120 °C	12	[62]
NAND/NOT	25/125 °C	6	[70]
NOR/NOT	25/125 °C	6	[70]
OR/AND	25/125 °C	6	[70]

In general, the advantage of temperature-controlled polymorphic gates can be their small size and no required global signal for function change across the chip. On the other hand, the behaviour of gates controlled by a continuous physical quantity is defined only in specified intervals of this quantity. For the same input, the output of these gates may oscillate between these intervals [44]. The biggest disadvantage of temperature-controlled gates is thus a high inertia – heating and cooling of the chip is usually very slow. In addition to that, heating of the chip may not occur evenly (temperature can be different in various parts of the chip).

2.3.3 Gates controlled by dedicated control signal

Stoica's team proposed also a possibility to control the function of polymorphic gates by a dedicated control signal; more precisely by a voltage at this control wire [64]. In contrast

to the control approaches introduced above (supply voltage level and chip temperature), an additional global signal across the whole chip is required, which could make the chip more expensive.

In case of the gates implementing just two functions, the behaviour of such gates is defined only for two voltage intervals at the dedicated wire – i.e. this dedicated wire transmits a binary information similarly to any other logic signal. Thus, such gates can be understood as conventional digital circuits having one more input signal and can also be designed by conventional synthesis methods at the gate (or transistor) level. Although inclusion of such gates to the field of polymorphic electronics may be controversial, authors of polymorphic electronics consider them also as polymorphic [64]. A requirement of three (or more) functions built into a single gate leads again to an analogue design where some transistors usually work in a linear mode.

First gates, designed as configurable by a special signal, were created before the introduction of the idea of polymorphic electronics. Between 1996 and 1997, Mark W. McDermott and John E. Turner patented XNOR/XOR [26] a NAND/NOR [27] gates. The specific function was chosen through a dedicated control wire by a voltage close to zero volts or close to the power supply voltage. A specific object of the invention was to maximise the flexibility in the design of spare gate arrays, such as for use in making fixes to integrated circuits through spare gates only.

The summary of published gates controlled by a dedicated signal is shown in Table 2.3. Parameters of many of them were thoroughly investigated in [44]. They vary a lot. There is a lot of gates in which one of the input signals can be switched through transistors directly to the output, i.e. they are pass-logic: AND/OR, AND/OR/XOR, NAND/WIRE/AND and further all gates published in [66].

Table 2.3: A survey of polymorphic gates controlled by dedicated control wire.

Functions	**Control value**	**Transistors count**	**Ref.**
AND/OR	0/3.3 V	6	[64]
AND/OR/XOR	3.3/1.5/0 V	10	[64]
NAND/AND	3.3/0 V	? (6 or 8)	[66]
NAND/NOR	0/5 V	10	[27]
NAND/NOR	0/5 V	10	[74]
NAND/NOR	5/0 V	8	[44]
NAND/NOR	5/0 V	10	[44]
NAND/NOR/XNOR/AND	0/0.9/1.1/1.8 V	11	[75]
NAND/XOR	5/0 V	9	[42]
NAND/WIRE/AND	0/1/-1.8 V	9	[76]
NOR/AND	3.3/0 V	? (6 or 8)	[66]
OR/NAND	3.3/0 V	8	[66]
OR/NOR	3.3/0 V	8	[66]
XNOR/XOR	5/0 V	16	[26]

The most interesting gate is definitely the NAND/NOR/XNOR/AND gate which implements four different functions in a single circuit just by 11 transistors [75]. It was designed

as an analogue circuit, similarly to AND/OR/XOR and NAND/WIRE/AND gates. It can be assumed that they will all have higher power consumption.

Four polymorphic gates were published in [66]. According to the publication, proposed gates do not follow the conventional CMOS design, so their output levels are sometimes 0.5 V for logic zero and 2.5 V for logic one whereas the gates were supplied by 3.3 V. Unfortunately, image quality of schematics and graphs with simulation results is low, so the results are not reproducible. Moreover, NAND/AND and NOR/AND gates are once drawn with 6 transistors, once with 8 transistors, although just one circuit was designed for each polymorphic function.

The rest of gates (NAND/NORs, NAND/XOR, XNOR/XOR) have a high input resistance, low output resistance, and input and output levels usually in the range of CMOS circuits. Their power consumption is also most probably comparable with similar CMOS circuits (it was not simulated for many gates or the results were not published).

Gajda mentioned also WIRE/OR/XOR/AND2b/NAND/AND1b polymorphic gate in his PhD thesis [17]. However, this gate was not found in the provided reference.

2.3.4 Gates controlled by supply voltage polarity

Technologies based on MOSFET and FinFET transistors are undoubtedly dominant in the today's electronics. However, they are slowly approaching the physical limitations (channel size, heat dissipation from the chip, etc.) [22, 59]. Thus, it began to search for transistors that could completely replace conventional silicon transistors in the future, or at least to find a convenient alternative. The exploitation of beyond silicon devices like carbon nanotubes (CNT) [24], graphene [39] and silicon nanowires (SiNW) [9] based transistors, as well as organic single crystal [14] or heterostructures [15], is considered by some researchers as a potential answer.

Ambipolar transistors

It has been shown in various literature sources that many post-silicon devices developed in recent years exhibit so-called ambipolar behaviour. The principle behind the ambipolar behaviour of such a transistor is that the transistor operates like N-type conventional MOS transistor under certain conditions and like P-type conventional MOS transistor under other conditions.

Ambipolar transistors have several variants. In this thesis, double-independent-gate ambipolar FETs are primarily investigated and utilised. Examples of such transistors are shown in Figure 2.4 and Figure 2.5. While the *control gate* (marked as G or CG) works in the same way as in case of the standard unipolar FETs, the *polarity gate* (PG) controls the device conduction mode (polarity; i.e. whether the transistor works as P- or N-type). Such transistors have been reported with use of emerging technologies such as carbon nanotubes [24], graphene [20] and silicon nanowires [21, 25]. Another variant of ambipolar transistors has only one gate (three terminals in total) [3, 8]. In the future, ambipolar FETs with three [16] or even more gates [2] can also be useful.

Described behaviour of ambipolar transistors seems to be very advantageous for complementary (CMOS like) structures. Moreover, the fabrication of such circuits may be simplified – just one type of the transistor is used everywhere.

In order to reduce the number of transistors in conventional (monofunctional) circuits, a lot of gates and more complex circuits based on double-gate ambipolar transistors were designed [1, 5]. All of them were designed as conventional digital circuits with PG controlled

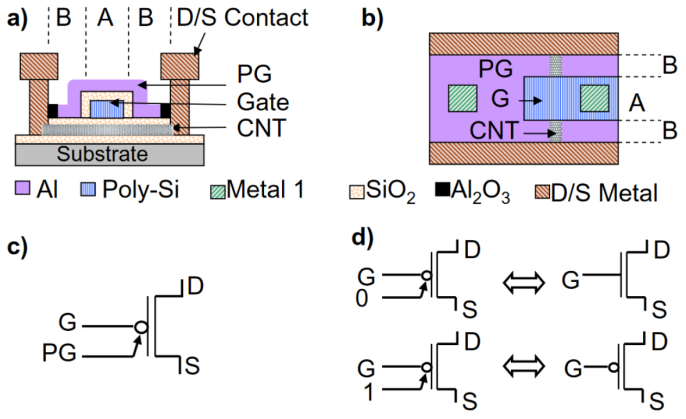

Figure 2.4: (a) Double-gate ambipolar CNT transistor, (b) layout, (c) schematic symbol and (d) a way to control its polarity in digital circuits [4].

by logic levels. The author of this thesis created a classification of double-gate transistors according to the PG terminal control which was further used in all his publications:

- **Type 1:** Ambipolar transistor acts as N-type in case of logic 1 at PG terminal and as P-type in case of logic 0 at PG terminal – e.g. CNT transistors utilised in [5] (see Figure 2.4).
- **Type 2:** Ambipolar transistor acts as P-type in case of logic 1 at PG terminal and as N-type in case of logic 0 at PG terminal – e.g. SiNW transistors utilised in [1] (see Figure 2.5).

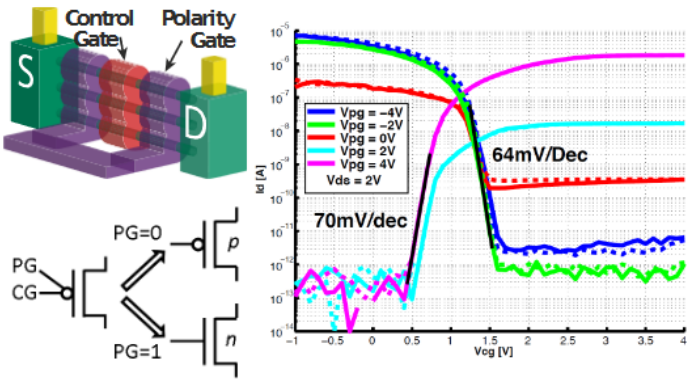

Figure 2.5: Structure of ambipolar double-gate SiNW FET, volt-ampere characteristics [25] and a way to control its polarity in digital circuits [1].

Gates controlled by supply voltage polarity

Because the polarity of ambipolar transistors is not specifically defined at an early stage by the fabrication process, but it could be changed also during the operation, it was shown that ambipolar transistors can be used with advantages also in polymorphic circuits. The idea of changing the transistor polarity by changing the logical value at PG terminal led

to an idea of a new control approach for polymorphic circuits: Function of the circuit is given by the polarity of power supply rails. If such circuit is supplied for instance by five volts above ground using one supply rail and the second supply rail is grounded, the second circuit function is available when the first supply rail is grounded and the second one is supplied by five volts – i.e. when the potentials of supply rails are swapped. Based on this principle, the polymorphic circuits controlled by the polarity of supply voltage have just *two functions*.

As it is shown in paper [73], which introduced several possibilities for usage of ambipolar transistors (and which calls this type of electronics as *ambipolar electronics*), structure of such bi-functional circuits can be similar to the CMOS circuits – one part of the circuit is used for delivering of a logic one to the output (in the conventional circuits usually based on P-MOS transistors) and the other (complementary) one for delivering of a logic zero to the output (see Figure 2.6a). In a suitably designed circuit, role of these two circuit parts may mutually change by changing the supply voltage polarity.

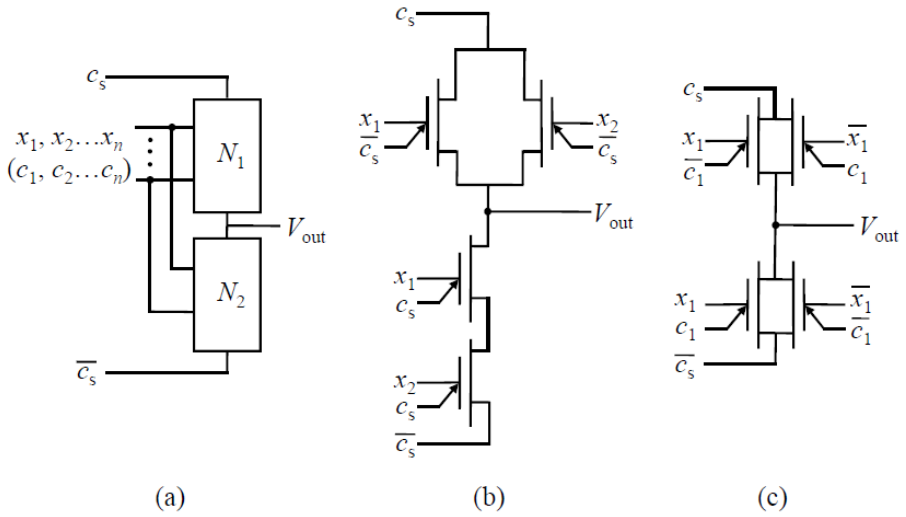

Figure 2.6: (a) Structure of gates controlled by power supply polarity, (b) NAND/NOR gate and (c) XOR/XNOR gate [73].

Most of the papers introducing some new ambipolar transistor show its behaviour on an inverter, e.g. [8, 25]. The inverter consists of two transistors connected similarly to the conventional MOSFET inverter. Such inverter based on ambipolar transistors can be labelled as NOT/NOT polymorphic gate because it produces an inverted input value to the output independently of the supply voltage polarity.

Yang and Mohanram [73] show another two polymorphic gates created from double-gate ambipolar transistors – NAND/NOR and XOR/XNOR gates. The first one is based on a structure similar to the conventional implementation of NAND and NOR functions in CMOS technology (see Figure 2.6b). It utilises four transistors only. When the supply rail c_s has higher (positive) potential than $\overline{c_s}$, the gate behaves as NAND. Otherwise ($\overline{c_s}$ has higher potential than c_s), the gate performs NOR function. XOR/XNOR gate (Figure 2.6c) is also assembled from four transistors. However, it requires also inverted inputs. Thus, two additional inverters would be needed for its realisation and the number of ambipolar transistors would increase to eight.

All three gates (inverter, NAND/NOR and XOR/XNOR) prove to be very promising in terms of properties and criteria listed at the beginning of Chapter 2.3. High input impedance is provided by connecting of all signal inputs to the gates of transistors. Transistors operate in the saturation mode, which minimises the gate consumption. The gate output is switched from the power rails by transistors with the correct polarity. That ensures low output impedance and output voltages close to the power supply voltage. The number of transistors being used in the gates is also low. Besides inverter, which is constructed (as well as a conventional solution) from two transistors, significantly lower number of transistors were used in comparison to a separate (parallel) implementation of both functions in a conventional CMOS solution. Implementation of a potential multiplexer would further significantly increase the number of transistors in conventional solutions.

These promising parameters led the author of this thesis to the further research. As a result, a high number of polymorphic gates controlled by the polarity of power supply voltage were later designed [37, 35, 36, 38]. Different implementations of AND/OR and XOR/XNOR functions were proposed in [37] for both Type 1 and Type 2 ambipolar transistors. But what is perhaps more important than new implementations of AND/OR and XOR/XNOR functions is a fact that the used evolutionary-based circuit design method proposed by the author of this thesis earlier [34] was not able to design 32 from 36 polymorphic functions (AND/XOR, AND/XNOR, etc.).

As it is shown later in Chapter 3.2, electronics based on ambipolar transistors and supplied by two rails, which can change their potentials, is really *not functionally (Boolean-) complete*. In other words, several logic functions cannot be implemented by this type of electronics. When one or two power rails with a stable potential (v_{DD}, v_{SS}) are added to the power rails determining the circuit function, circuits can implement any logic function. Design of such circuits is shown [36]. Furthermore, it was shown that similar approach can be used also for polymorphic circuits based on MOSFET transistors [35]. Polymorphic gates designed in this way assume transistors with conventional dimensions and working in the saturation mode. That provides much better properties (power consumption, propagation delay, size, etc.) compared to the gates controlled by supply voltage level or chip temperature (see Chapters 2.3.1 and 2.3.1).

38117 gates controlled by the polarity of dedicated supply rails were published by the author of this thesis in PoLibSi library [38], which is available at `www.fit.vutbr.cz/~inevoral/polibsi`. The library contains eight sets of efficient bi-functional two-input polymorphic gates, whose function is selected by polarity of dedicated power rails. Particular gate sets differ in the transistor type (conventional MOSFET, double-gate ambipolar transistors), feature which the gate sets were optimised to (transistor count, propagation delay, power consumption) and input impedance constraint (see Table 2.4). Each gate implementation includes a schematic, an HSPICE description and simulation results (see Figure 4.1). The propagation delay and power consumption is provided for all MOSFET based gates. Furthermore, each gate set is complete – it provides at least one (usually even more) efficient implementation of any pair of two-input Boolean functions. That can be useful for efficient synthesis of complex polymorphic circuits.

In order to make the enumeration of polymorphic circuits based on ambipolar transistors (mono-gate ambipolar transistors in this case) complete, it is also worth to mention a work of Radek Tesař. He designed two-input NAND/NAND and NOR/NOR gates resistant to the change of supply polarity [69], further identity/negation gate and a polymorphic multiplexer [68]. The last-mentioned gate propagates the first multiplexer input to its output in the first polymorphic mode and the other input in the other mode. However,

Table 2.4: List of gate sets in the PoLibSi library.

Gate set name	Transistor type	Input impedance	Opt. criteria	No. of gates in the set
MOS_SIZE_HI	MOSFET	high	size	507
MOS_DELAY_HI	MOSFET	high	delay	257
MOS_POWER_HI	MOSFET	high	power	239
MOS_OPT_HI	MOSFET	high	delay, power	253
AMBI_N1_HI	ambipolar, type 1	high	size	11577
AMBI_N1_NO	ambipolar, type 1	–	size	4791
AMBI_P2_HI	ambipolar, type 2	high	size	11279
AMBI_P2_NO	ambipolar, type 2	–	size	9214

these gates differ from the original concept as they use also rectifier diodes besides the ambipolar transistors.

2.3.5 Non-conventional multifunctional gates

In the recent years, several other gates based on unconventional structures have shown to be polymorphic or at least multifunctional. This section shows three such gates.

Figure 2.7 shows a graphene-based multifunctional device whose output F is given by the relation $AC + A'B$ for $U = 1$ and $A'C + AB$ for $U = 0$ [67]. The basic function of the element is thus a multiplexer controlled by the A or U signal. If a specific constant voltage is applied to electrodes A and/or B, the gate can realise up to 8 functions derived from the mentioned formulas. However, from the viewpoint of polymorphic electronics, it is a gate with two functions. These two functions are then given by the specific connection of the gate in the circuit.

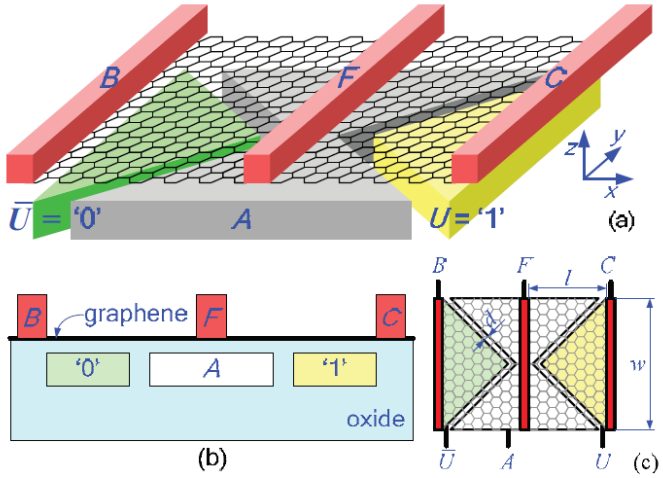

Figure 2.7: Graphene gate: (a) 3D visualisation, (b) side cut, (c) to view [67].

In 2017, Parveen's team introduced hybrid spin-CMOS logic gates using magnetic domain wall motion devices with five [41] and six terminals [40]. Their function is given by a multi-bit key (key in Figure 2.8 composes of K1, K2 and K3 signals). By applying one of the four keys, the gate can be used to implement AND, OR, identity or XOR function. Because the gate contains also a negation of the output, functions NAND, NOR, NOT and XNOR are then also automatically available. If a suitable key signal is used as a signal describing the state of the environment, the gate could also be called as a polymorphic gate with two functions.

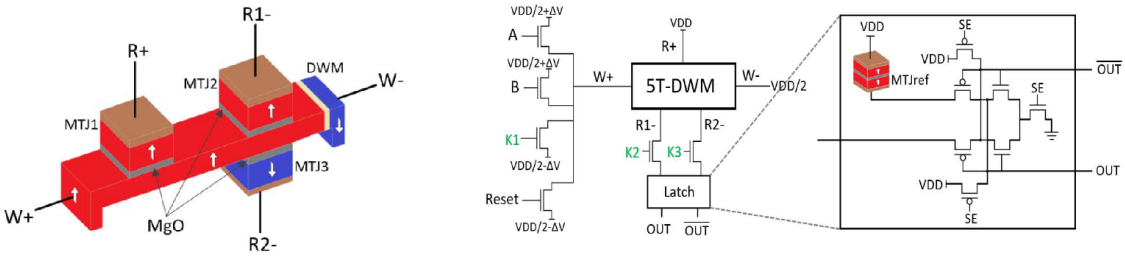

Figure 2.8: 5-terminal magnetic domain wall motion device structure (left), proposed gate (right) [41].

All three devices are multifunctional and provide implementations of different logic functions. While the graphene one could be used as a gate controlled by a dedicated control signal, the others require a complicated sequential control (reset, compute, and sense states) which is not typical for polymorphic gates. Moreover, the hybrid spin-CMOS logic gates need a high number of transistors (13 in [41] and 17 in [40]) in addition to the main domain wall motion device. That would probably not allow their deployment in the polymorphic electronics.

Chapter 3

Research summary

This chapter summarises the research presented in the thesis. After a brief overview of the research process; the motivations, contributions and abstracts for each included paper are presented. Then, other achieved results related to this thesis are summarised, which are parts of two submitted but not yet published papers. Finally, remaining papers of the author that are not included in this thesis are listed together with research projects the author participated in.

3.1 Overview

The goal of the research conducted in this doctoral thesis is to deeply investigate an approach to the gate-level polymorphism where the circuit function is selected by the polarity of supply voltage. As the basic building blocks, conventional MOSFET and emerging double-gate ambipolar transistors were chosen.

Only a few polymorphic gates controlled by the supply voltage polarity have been published earlier by other authors. Such gates were designed by an ad-hoc approach. In order to systematically design new polymorphic gates, an evolutionary-based design method was created and published in Paper I. To our best knowledge, it is the first design approach for design of circuits controlled by the supply voltage polarity and also the first approach for design of circuits based on the double-gate ambipolar transistors ever.

A subsequent research focused on the gates based on double-gate ambipolar transistors resulted in several innovative gates published in [37] and especially in the finding, that polymorphic electronics controlled by the supply voltage polarity is functionally complete only if at least one constant logic value (i.e. v_{SS} or v_{DD}) is available in the circuit. Chapter 3.2 describes the problem more in detail. In the rest of the research, it was assumed that these logic values currently exist in the circuit (polymorphic electronics is, for example, combined with conventional electronics in the chip) or it is possible to create them from the power supply rails in the particular chip manufacturing technology.

Design approach published in Paper I was later improved for a fast and reliable design for specific transistor types: Paper II is devoted to the design of polymorphic gates based on MOSFET transistors and Paper III to the design of gates based on double-gate ambipolar transistors. In both papers, complete sets of size-efficient polymorphic two-input gates are presented (five sets in total). Note that the author of this thesis is the first who came up with the idea to combine such type of gate-level polymorphism with conventional MOSFET transistors.

In order to provide the complete sets of second generation polymorphic gates to the research community, an online polymorphic gate library called PoLibSi was created (Paper IV) and released online to www.fit.vutbr.cz/~inevoral/polibsi. Each gate in the library includes a schematic, an HSPICE description and simulation results (see Figure 4.1). Moreover, propagation delay and power consumption are provided for all MOSFET-based gates. Besides the size-oriented gate sets, delay-oriented, power-oriented and delay&power-oriented MOSFET gate sets were later created and attached to the library. A paper dedicated to the power consumption of the second generation of polymorphic gates is currently submitted to a conference by the author of this thesis. It was proven that properties of the designed gates are really better compared to the first generation of polymorphic gates (see Chapter 3.4). Moreover, it was shown that such polymorphic gates could be competitive to the conventional CMOS solutions in terms of the size, delay and also power consumption.

Paper V brings a case study with an intention to show on an example (adder/subtractor) that complete sets of efficient bi-functional gates may allow an efficient implementation of components at a higher level of abstraction. In several classes of applications, which typically involve RT level oriented design approach, these components can circumvent various issues related to synthesis of multifunctional circuits at the gate level.

Chapter 3.4 shows more complex polymorphic circuits. In order to show the advantage of the proposed gate sets, bi-functional image filters were chosen as target applications. A few tens of complex size-efficient RTL components were designed and subsequently utilised for implementations of three bi-functional image filters. A part of the designed RTL components was published already in Paper IV. It was shown that designed filters are significantly smaller compared to the implementations based on the first generation of polymorphic gates. Moreover, proposed implementations are significantly smaller than conventional solutions with conventional mono-functional gates.

3.2 Problem of a constant in the environment with changing power supply polarity

In the conventional CMOS electronics, any Boolean function can be implemented only by using NAND gates or only by using NOR gates. These gates can also be utilised for implementation of unary or nullary (constants) Boolean functions. Note that the constants (logic zero and logic one) are present in the circuits by supply rails anyway.

Similarly, at least one permanent logic value (a constant) is required in the polymorphic circuits controlled by the supply voltage polarity. In 2017, author of this thesis showed that an evolutionary method for design of such polymorphic circuits was able to design only four out of 36 different two-input gates, which supposed to be based on double-gate ambipolar transistors and had no access to any permanent logic value or any other constant potential [37]. Out of all 256 possible two-input functions, only 16 were successfully designed (identity and various combinations of NOT/NOT, NAND/NOR and XOR/XNOR functions). The usage of an evolutionary algorithm cannot prove that the remaining functions cannot be designed, of course, but a proof, showing that some of the gates cannot be designed, follows:

Theorem 1 *Polymorphic electronics based on double-gate ambipolar transistors and controlled by the supply voltage polarity is NOT functionally (Boolean-) complete if there is no constant logic value in the circuit.*

Proof *Suppose that polymorphic electronics based on double-gate ambipolar transistors and controlled by the supply voltage polarity is computationally complete. Thus, for any two Boolean functions, there is a polymorphic circuit that realises them. Thus, there is also a circuit producing a permanent logic one output regardless of the supply voltage polarity (such polymorphic function can be denoted as 1/1). Let's create such a circuit.*

The logic one must be independent of any signal inputs of the circuit, because all signal input can be zero at the same time. Thus, the logic one must be switched to the output from the supply rails. In order to ensure strong (undegraded) output level, the logic one must be switched by one or more transistors with P polarity.

Let's consider the first polymorphic function of the circuit, when there is a potential corresponding to logic one at supply rail pwr0 and a potential corresponding to logic zero at supply rail pwr1. The logic one must be switched from pwr0 through one (or more) opened ambipolar transistor, currently configured to work as p-MOS. Its gate must be connected to pwr1 – to logic zero in order to ensure that the transistor will be opened (see Figure 3.1 left). The connection of PG terminal to a specific power rail (ensuring the P polarity) depends on the type of ambipolar transistor (see Chapter 2.3.4).

After swapping of supply rail potentials (i.e. changing the supply voltage polarity), a logic zero is at pwr0. Thus, at least one of the transistors mentioned above must necessarily be closed so that the logic zero from pwr0 is not propagated to the output. Since logic one is now at the gate terminal of the transistor, its polarity must remain same (p-MOS). That requires to maintain the same logic level at PG terminal as it was there before swapping of supply rail potentials (see Figure 3.1 right).

So, a constant potential is required to create a constant logic level. However, there is no constant potential in the circuit. Thus, the circuit with a permanent logic one at the output cannot be created. Thus, polymorphic electronics mentioned above is NOT functionally complete. □

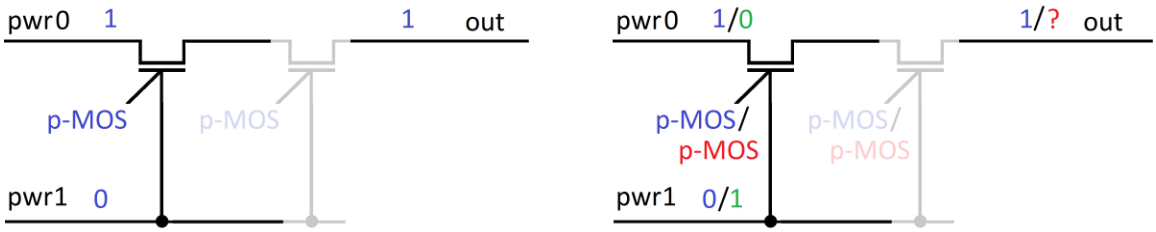

Figure 3.1: Wiring of ambipolar transistor(s) during an attempt to create a circuit generating constant logic one: Before (left) and after (right) change of supply voltage polarity.

Theorem 2 *Polymorphic electronics based on double-gate ambipolar transistors and controlled by the supply voltage polarity is computationally complete if at least one permanent logic value is available in the circuit.*

Proof *If just one permanent logic value is available in the circuit, the other one can be created by an inverter (NOT/NOT gate). Any polymorphic gate can be then implemented e.g. by conventional CMOS circuits realising both circuit functions, whose output is selected by a multiplexer according to one of the power supply rails. Such circuit is supplied by permanent logic one and permanent logic zero. As transistors, double-gate ambipolar transistors are used, whose PG terminal is connected either to permanent logic one or a permanent logic*

zero, depending on whether the particular transistor should behave as n-MOS or p-MOS transistor in the circuit. □

Note that the universal implementation of a polymorphic gate utilised in the proof of Theorem 2 is working for a given pair of functions, but it is most probably not the most efficient implementation of such a function.

A similar problem with constant logic values can be found also in the polymorphic circuits controlled by supply voltage polarity and based on MOSFET transistors. The substrates of n-MOS transistors are usually connected to the negative pole of the power supply and the substrates of p-MOS transistors to the positive one [72].

For the design of polymorphic gates controlled by of the supply voltage polarity, it is supposed in this thesis that the permanent logic values currently exist in the circuit (polymorphic electronics is, for example, combined with conventional electronics in the chip) or it is possible to create these permanent levels from the power supply rails in the particular chip manufacturing technology (in the MOSFET-based polymorphic electronics e.g. by PN-based rectifiers in a silicon chip).

3.3 Papers included in the thesis

This section presents details on the motivation and contributions for each paper together with the paper abstract.

3.3.1 Paper I

NEVORAL Jan, RŮŽIČKA Richard and MRÁZEK Vojtěch. **Evolutionary Design of Polymorphic Gates Using Ambipolar Transistors**. In: *2016 IEEE Symposium Series on Computational Intelligence*. Athens: Institute of Electrical and Electronics Engineers, 2016, pp. 1-8. ISBN 978-1-5090-4240-1.

Author participation: 50 %
Conference ranking: B5 (Qualis[1])

Motivation and contributions

Before 2016, no method for systematic design of gates based on ambipolar transistors nor any method for systematic design of polymorphic gates controlled by polarity of supply voltage rails was published. In this paper, we presented an evolutionary based method for design of polymorphic circuits at the transistor level. It is capable of designing both polymorphic gates controlled by the polarity of supply voltage rails and bi-functional polymorphic gates controlled by dedicated control signal. Besides double-gate ambipolar transistors, designed gates can be also based on N-MOS and P-MOS transistors.

Speed of the evolutionary based circuit design methods is mostly dependent on the speed of circuit evaluation. The proposed method is inspired by a design method published earlier by Mrázek et al. [30], because it was shown that a discrete simulator with a switch-level transistor model extended by a threshold drop degradation effect proposed originally by Mrázek is able to achieve a fast circuit simulation with a reasonable accuracy. Instead of single-output and two-input CGP nodes, we utilised single-output and three-input CGP

[1] http://www.conferenceranks.com/

nodes which can represent ambipolar transistors, N-MOS transistors, P-MOS transistors or junctions. The evaluation of candidate circuits is performed by a discrete even-driven simulator. Six different discrete values are supported: *strong* as well as *degraded* zeros and ones, a high-impedance state and an undefined (forbidden) state. The implemented simulator generates outputs of candidate circuits for all possible input vectors and checks, whether the output values are identical with the specification, and no short-circuit connections nor any values oscillations (caused by cyclic connections) occurred during the simulation.

Two models of transistors are proposed in this paper. The first one (called *six-state*) is based on the behaviour of conventional MOSFET transistors. In the circuits designed with use of this model, degraded values at gate (and polarity gate) terminals usually have a similar impact on the transistor behaviour as non-degraded (strong) values (see Paper I, Section 4B). In this PhD thesis, the six-state model is later used for design of gates based on MOSFET transistors. The other model (called *four-state*) ensures that only non-degraded values will be present at gate (and polarity gate) terminals of utilised transistors. Because of a lack of freely available exact models of double-gate ambipolar transistors, is not possible to determine their degraded levels and also their behaviour with certainty when degraded values are present at their gates. Therefore, the *four-state* model was used for design of gates based on double-gate ambipolar transistors in the following papers.

It was demonstrated that the proposed method is able to produce valid solutions. Moreover, AND/OR and XOR/XNOR gates designed by this method provides transistor savings (i.e. size or area savings) compared to the existing polymorphic gates based on ambipolar transistors. The method proposed in this paper was further modified and utilised for design of polymorphic gate sets in attached Paper II, Paper III and Paper IV.

The proposed design method is not strictly related just to MOSFET or double-gate ambipolar transistors. If the currently implemented transistor models would correspond to behaviour of any other modern transistors (FinFET, FDSOI, etc.) or similar discrete models could be created for another types of transistors (e.g. mono-gate ambipolar transistors), the proposed design method can be easily extended by their support.

Finally, the paper introduces a new class of polymorphic gates discovered thanks to the newly proposed design method – polymorphic gates controlled by the polarity of supply voltage rails which are based purely on the conventional MOS transistors (previously published gates controlled by the same way were based on ambipolar transistors).

In this paper, a new approach suitable for the evolutionary design of smaller polymorphic circuits based on ambipolar transistors was introduced. The novelty lies in a new circuit representation and new simulation models. The approach can be utilised for design or optimisation of polymorphic circuits controlled by the polarity of supply voltage or circuits controlled by the dedicated control wire.

Abstract

The objective of the paper is to introduce a new approach to the evolutionary design of polymorphic digital circuits conducted directly at transistor level. A discrete event-driven simulator was utilised to achieve reasonable trade-off between performance and precision. The proposed approach was evaluated on a set of polymorphic logic circuits controlled by switching the power rails. It was demonstrated that the proposed method is able to produce valid solutions. A lot of polymorphic gates based on ambipolar transistors were designed, which provide transistor savings compared to existing circuits. A new class of polymorphic gates was discovered thanks to the proposed system – gates based on conventional

MOS transistors whose functions are changed by switching the power rails. They seem to have the best parameters among currently known polymorphic gates based on conventional transistors.

3.3.2 Paper II

NEVORAL Jan, RŮŽIČKA Richard and ŠIMEK Václav. **CMOS Gates with Second Function**. In: *2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. Hong Kong: IEEE Computer Society, 2018, pp. 82-87. ISBN 978-1-5386-7099-6.

Author participation: 60 %

Conference ranking: B1 (Qualis)

Motivation and contributions

Paper I introduced a new class of polymorphic gates discovered thanks to the proposed evolutionary method – polymorphic gates controlled by the polarity of supply voltage rails which are based purely on the conventional MOS transistors. Until then, all gates controlled by the polarity of supply voltage rails were created from ambipolar transistors. In this paper, design of just such gates based on MOS transistors is investigated.

For design of new polymorphic gates, design method published in Paper I was improved in the context of this contribution. It was shown that not all the circuits produced from the method described in Paper I behave as expected (see Paper II, Figure 3). Detailed analysis of evolved circuits exposed an issue in the transistor model used in the discrete simulation, which may occur under certain conditions. In order to prevent this issue, a new design constraint (ensuring that the high-impedance discrete level will never be present at any transistor gate terminal for any circuit input) was added to the circuit requirements.

Another shortcoming of the design method proposed in Paper I turned out to be a low success rate (see Paper II, Figure 4). This issue was solved by proposing an optimisation approach based on the same design method. Furthermore, success rate was improved by reduction of the chromosome size (and thus reduction of state space) by removing one input from CGP nodes.

With such modified design approach, a set of size-efficient two-input polymorphic gates with high input impedance and controlled by dedicated power rails was created. The set is complete – it provides efficient implementation of any pair of two-input Boolean functions. Note that it is the first complete set of polymorphic gates ever published (regardless of the control phenomenon). The gate set was later released as a part of the PoLibSi library (see Paper IV) with schematics and simulation results under name *MOS_SIZE_HI*.

The gates in the set were designed to be as small as possible (i.e. to contain as few transistors as possible). Each gate published in the set is composed of less transistors than it is required for a multiplexer and a separate implementation of individual Boolean functions. Moreover, most of the gates are also composed of same or even much smaller number of transistors than it is required for a separate (parallel) implementation of the individual Boolean functions (i.e. without multiplexer).

Gates in the set show the best parameters of all the previously published polymorphic gates: They were designed as non-pass-logic, i.e. with a high input impedance and low output impedance. All transistors work in the saturation mode. Besides the low number of transistors with conventional dimensions, the gates have also a short time of signal propagation and low power consumption compared to the first generation of polymorphic

gates. Results in this paper show that polymorphic electronics should be the concept which improves area-efficiency (price) of implementation of circuits with a second function not only at the academical level, but also in practice.

In this paper, an improved approach to the design of MOSFET-based polymorphic gates controlled by polarity of dedicated power rails was shown. Furthermore, a complete set of such two-input gates with good properties was designed and validated by HSPICE simulations. These gates bring significant advantages for space-efficient synthesis of polymorphic circuits in terms of the overall size as it is shown later.

Abstract

In this paper, a new approach to design of multifunctional digital circuits is presented. It is based on adoption of polymorphic electronics paradigm which permits digital circuits to exhibit more than one function while preserving the same structure. In that case only components of the circuit (gates) have to be multifunctional. Individual gates have typically built-in sensitivity to the occurrence of some phenomena invoking the function change (e.g. power supply level etc.), which means that no dedicated net is required for that purpose. One of the key advantages of such circuits is the efficiency in terms of size. In this paper, MOS transistors are exploited in an unconventional manner where the circuit function selection depends just on the condition of power supply voltage rails, which is otherwise typical for polymorphic circuits utilising ambipolar transistors. Furthermore, a first complete set of successfully simulated two-input polymorphic gates was obtained. These gates show the best parameters of all the previously published polymorphic gates – high input impedance and low output impedance, short time of signal propagation, low power consumption and low transistor count being used. Wide range of proposed polymorphic gates (function combinations) may help to obtain more efficient results during synthesis.

3.3.3 Paper III

NEVORAL Jan, RŮŽIČKA Richard and ŠIMEK Václav. **From Ambipolarity to Multifunctionality: Novel Library of Polymorphic Gates Using Double-Gate FETs**. In: *2018 21st Euromicro Conference on Digital System Design (DSD)*. Prague: Institute of Electrical and Electronics Engineers, 2018, pp. 657-664. ISBN 978-1-5386-7376-8.

Author participation: 60 %

Conference ranking: B1 (Qualis)

Motivation and contributions

As it was shown in Chapter 2.3.4, only few polymorphic gates based on ambipolar transistors were published before 2018. These gates were supplied by only two wires whose potentials were swapped when a change of the gate function was required. As it was shown in Chapter 3.2, such concept cannot create functionally complete systems. In this paper, design of gates based on double-gate ambipolar transistors with two additional power supply rails (conventional v_{SS} and v_{DD}) is investigated.

For design of new polymorphic gates, design method published in Paper I was improved in the context of this contribution. Only two types of CGP nodes are used: double-gate ambipolar transistors and junctions. Similarly to Paper II, a new design constraint was added to the circuit requirements, which ensures that the high-impedance discrete level

will never be present at any transistor gate or PG terminal for any circuit input. Because of the lack of freely available exact models of double-gate ambipolar transistors, four-state model introduced in Paper I was utilised. That ensures only strong zero or strong one discrete level to be present at any transistor gate and PG terminal for any circuit input. In order to improve the success rate of the design approach, an optimisation approach based on the same design method was proposed.

With such modified design approach, four complete sets of size-efficient two-input polymorphic gates controlled by dedicated power rails were created. Two gate sets are based on Type 1 double-gate ambipolar transistors, another two on Type 2 transistors. For each type of transistors, one set contains gates with a high input impedance and low output impedance; the other set had no impedance requirements during its design – i.e. most of the contained gates are pass-logic. Pass-logic gates are usually smaller. That can be useful in some parts of complex circuits, where pass-logic gates are also acceptable. All four sets are complete – each provides efficient implementation of any pair of two-input Boolean functions. Designed gate sets were later released as a part of the PoLibSi library (see Paper IV) under names *AMBI_N1_HI*, *AMBI_N1_NO*, *AMBI_P2_HI* and *AMBI_P2_NO*.

All gates in the sets were designed to be as small as possible (i.e. to contain as few transistors as possible). Each gate published in the sets is composed of equal or less transistors than it is required for a multiplexer and a separate (parallel) implementation of individual Boolean functions. Moreover, most of the gates are also composed of equal or even less transistors than it is required for a separate implementation of individual Boolean functions (i.e. without multiplexer). A significant difference between sizes of Type 1 and Type 2 gates can be observed – gates with a high input impedance based on Type 1 transistors are composed of approximately 1.5 more transistors in average compared to Type 2 gates.

Gates in the sets with a high input impedance (AMBI_N1_HI and AMBI_P2_HI) show the best parameters of all the previously published polymorphic gates: High input impedance, low output impedance and low number of transistors with conventional dimensions. Furthermore, short time of signal propagation and low power consumption is also expected, compared to the polymorphic gates controlled by an analogue quantity. Thus, properties of the gates should correspond to the ideal ones defines in Chapter 2.3.

In this paper, an improved approach to the design of polymorphic gates based on double-gate ambipolar transistors and controlled by polarity of dedicated power rails was shown. Furthermore, four complete sets of such two-input gates with good properties were designed and validated by HSPICE simulations. These gates bring significant advantages for space-efficient synthesis of polymorphic circuits in terms of the overall size as it is shown later.

Abstract

Ambipolarity, a unique feature typically found in some beyond silicon devices, e.g. CNT or organic FETs, is still treated today just as something rather peculiar. But in reality, it does not hinder such devices from utilisation when it comes to the implementation of logic. From other point of view, this feature could be perceived as an opportunity to implement the logic in more refined and efficient way. The practical impact of ambipolarity results in devices which becomes more versatile than conventional FET element. In this paper, a set of multifunctional logic gates based on ambipolar FETs is presented. The multifunctionality of these gates means that each gate could exhibit one of two defined functions in a given moment. The selection of their function depends on circumstances under which the circuit is operated. The proposed set of gates could be employed in multifunctional circuits using

techniques and procedures established for polymorphic electronics. This field of study, yet proposed nearly 20 years ago, now offers synthesis methods and application approaches to obtain an efficient implementation of more than one function in one logic circuit.

3.3.4 Paper IV

NEVORAL Jan, ŠIMEK Václav and RŮŽIČKA Richard. **PoLibSi: Path Towards Intrinsically Reconfigurable Components**. In: *2019 22nd Euromicro Conference on Digital System Design (DSD)*, Kallithea, Chalkidiki: Institute of Electrical and Electronics Engineers, 2019, pp. 328-334, ISBN 978-1-7281-2861-0.

Author participation: 70 %
Conference ranking: B1 (Qualis)

Motivation and contributions

The main intention of Paper II and Paper III was to show how to design size-efficient polymorphic gates based on MOSFET and double-gate ambipolar transistors. It was also shown that it is possible to design such gates with a relatively small number of transistors. The main goal of this paper is to introduce a library, which contains specific implementations of such gates. The library is called PoLibSi and it is freely available for the research community at www.fit.vutbr.cz/~inevoral/polibsi.

The PoLibSi library is composed of eight sets of gates controlled by the polarity of dedicated power rails. Four of them are based on double-gate ambipolar transistors, another four on MOSFET transistors (see Table 2.4). Besides the size-oriented MOSFET gate set, delay-, power- and delay&power-oriented MOSFET gate sets are also part of the library.

During development of the PoLibSi library, more than ten thousand of fully operational variants of MOSFET-based gates were obtained for each particular polymorphic function. Of course, it was not an exception to observe different level of mutual similarity between some of them. However, a plenty of implementations were still completely unique and did not share any structural similarity. That particular fact has allowed to create also delay-oriented, power-oriented and delay&power-oriented MOSFET gate sets. Although only size-oriented and delay-oriented sets were finished at the time of writing Paper IV, the library currently contains all eight sets. A paper dedicated to power consumption of polymorphic gates was submitted to a different conference by the author of this thesis later (see Chapter 3.4).

Each gate set is complete – it provides efficient implementation of any pair of two-input Boolean functions. Furthermore, each polymorphic function (a pair of Boolean functions) in the gate sets usually has more unique transistor-level implementations contained in the PoLibSi, not just a single one.

The PoLibSi library is composed of 38117 polymorphic gates in total. Each of them was simulated in order to validate its function: MOSFET-based gates by 45nm transistor models; gates based on ambipolar transistors using a behavioural model of such transistors (see Paper IV, Figure 3). The author of this thesis later proved that the MOSFET-based gates are functional also with 32nm and 65nm transistor nodes (see Chapter 3.4).

Each gate in the library includes a schematic, an HSPICE description and simulation results. Moreover, propagation delay and power consumption are provided for all MOSFET-based gates. It turned out that the size-optimised MOSFET gates usually have little bit higher power consumption and longer propagation delay (compared to the conventional

CMOS logic gates, but still much better compared to the first generation of polymorphic gates). Th Power consumption and the delay of those gates with few more transistors (e.g. gates from the delay&power-oriented gate set) is significantly lower. Such polymorphic gates could be then competitive to the conventional CMOS solutions in terms of the size, the delay and also the power consumption! Unfortunately, a lack of freely available accurate SPICE-based models of double-gate ambipolar transistors has not allowed to investigate the propagation delay and power consumption for gates based on double-gate ambipolar transistors.

A size-efficiency of the proposed size-oriented gate sets is demonstrated by three RTL components in this paper. Their implementation is significantly smaller compared to the previous implementation from Sekanina et al. [54], who used a combination of conventional mono-functional gates and a polymorphic NAND/NOR gate – so far typical approach for polymorphic circuits.

In this paper, a large library of polymorphic gates with promising parameters is presented. It is the first freely available library with polymorphic gates ever. Each gate implementation includes a schematic, an HSPICE description and simulation results. Moreover, propagation delay and power consumption are provided for all MOSFET-based gates. Besides the size-oriented gate sets, delay-, power- and delay&power-oriented sets dedicated to the MOSFET transistors are also part of the library. It is supposed that the proposed library may significantly improve complex polymorphic circuits in terms of the resulting size, the delay and/or the power consumption. Compared to a few dozen gates of the first generation, author of this thesis also showed that the problem with a lack of polymorphic gates offering good properties is well solvable.

Abstract

One of the main research directions of polymorphic electronics is focused on various issues connected with the design of basic polymorphic components – polymorphic gates. Without a sufficient amount of polymorphic gates offering good properties, conventional electronics will be most likely the preferred way to polymorphic electronics in application scenarios targeting multifunctional behaviour or reconfiguration. The main objective of this paper is to propose a library called PoLibSi which contains eight sets of efficient bi-functional two-input polymorphic gates, whose function is selected by mutual polarity of dedicated power rails. The gate sets differ in the transistor type (conventional MOSFET, emerging double-gate ambipolar transistors), feature the gate sets were optimised to (transistor count, delay, power consumption) and input impedance constraint. The individual gates were designed by means of using an evolutionary based approach and further validated by HSPICE simulations. Each gate implementation includes a schematic, an HSPICE description and simulation results. Moreover, propagation delay and power consumption are provided for all MOSFET based gates. Furthermore, each gate set is complete – it provides efficient implementation of any pair of two-input Boolean functions. Besides providing polymorphic gates with better properties to the research society, the aim of the proposed library is to improve the synthesis of polymorphic circuits in terms of the resulting size, as it is also shown in the paper. Finally, the PoLibSi library is available at: www.fit.vutbr.cz/~inevoral/polibsi.

3.3.5 Paper V

NEVORAL Jan and RŮŽIČKA Richard. **Efficient Implementation of Bi-functional RTL Components – Case Study**. In: *2018 New Generation of CAS (NGCAS)*. Valletta: IEEE Circuits and Systems Society, 2018, pp. 25-28. ISBN 978-1-5386-7680-6.

Author participation: 75 %

Motivation and contributions

As it has been already stated in Chapter 2.2, logic synthesis of polymorphic digital circuits is very challenging. Most of the existing circuits were created using evolutionary algorithms.

In this paper, a case study is presented showing that it is possible to effectively implement bi-functional RTL components when a complete set of efficient bi-functional gates is available. In applications involving design at the RT level (e.g. signal processing), multifunctional RTL components could circumvent issues related to synthesis of multifunctional circuits at the gate level. While the synthesis at the gate level is difficult, at the RT level a skilled designer would be still able to design far more complex circuits only by himself.

A demonstration of this assumption is given by a bi-functional adder/subtractor circuit. At the gate level, one-bit full adder/subtractor circuit was created and optimised. It was subsequently utilised for design of multi-bit adder/subtractor. Three-bit adder/subtractor was then implemented by the size-efficient MOSFET-based gate set from Paper II and successfully simulated at the transistor level. Besides adder/subtractor, an increment/decrement RTL component is also presented. More complex RTL components were designed later by the author of this thesis. Their summary can be found in Chapter 3.4.

This paper demonstrates on an example that complete sets of efficient polymorphic gates can contribute to efficient implementations of RTL components. Such components could then move the synthesis of polymorphic circuits one level up – to the RT level. Furthermore, new circuits (new in the field of polymorphic electronics) are presented: increment/decrement, adder/subtractor.

Abstract

The emergence of highly optimised implementations of many bi-functional gates allows an efficient implementation of components at a higher level of abstraction. In several classes of applications, which typically involve RT-level oriented design approach, these components can circumvent various issues related to synthesis of multifunctional circuits at the gate level. While the synthesis at the gate level is difficult, at RT level a skilled designer is still able to design far more complex circuits by himself. If a set of efficient bi-functional RTL components is available, their utilisation is expected to improve efficiency of the resulting circuit. In this paper, validity of this assumption is demonstrated through a design of bi-functional adder/subtractor circuit. At the gate level, one-bit full adder/ subtractor circuit was created and optimised. This circuit was subsequently utilised for design of multi-bit adder/subtractor which was successfully simulated at the transistor level with MOSFET implementation of bi-functional logic gates. Besides adder/subtractor, an increment/decrement RTL component is also presented.

3.3.6 Author's contributions to selected papers

The papers presented in this PhD thesis arose mainly as a part of research of the Unconventional Digital Circuits Research Group at Faculty of Information Technology, Brno University of Technology. The evolution approach presented in the first paper was inspired by an idea published earlier by Vojtěch Mrázek (also Faculty of Information Technology, BUT) who provided a lot of valuable advice and also participated in preparation of the first paper. Although all co-authors contribute to the selected papers, author of this thesis has the main share in all of them, especially in terms of the presented results. The following list summarise author's contribution to the selected papers:

1. **Paper I** – Novel circuit representation, discrete models of ambipolar transistors, implementation of the evolutionary algorithm and experimental evaluation.
2. **Paper II** – Approach to the design of gates based on MOSFET transistors, development of size-efficient gate set, validation of functionality of the gates.
3. **Paper III** – Approach to the design of gates based on double-gate ambipolar transistors, development of size-efficient gate sets, validation of functionality of the gates.
4. **Paper IV** – Development of whole PoLibSi library which primarily included: Development of the gate sets, validation of functionality of the gates, analysis of propagation delay and power consumption, creation of HSPICE descriptions, schematics and library front-end.
5. **Paper V** – Development of presented gate-level circuits and their validation, proof of the concept by a case-study.

3.4 Following results

Author of this thesis continued with the research related to the second generation of polymorphic gates also after submission of the presented papers. This section briefly summarises the results of two more submitted but in the time of writing this thesis not yet published papers.

3.4.1 Power consumption of proposed gates

In order to get a better insight to properties of the gates from the PoLibSi library, power consumption of the proposed gates was investigated by the author of this thesis. Average power consumption was calculated with use of the HSPICE simulator and added into the library for each MOSFET-based gate set. Furthermore, a huge amount of function implementations produced by the evolutionary based design approach allowed to create two novel power-oriented MOSFET-based gate sets and to attach them to the PoLibSi library:

- **MOS_POWER_HI** – contains gates with the lowest power consumption for different number of transistors being used.
- **MOS_OPT_HI** – contains gates with the lowest multiple of delay and power consumption for different number of transistors being used.

All MOSFET-based gate sets in the PoLibSi library were validated with 45nm BSIM4 V1.0 models from [31] during their design. Besides the experiments carried out with 45nm transistor model, further analysis with 32nm and 65nm BSIM4 V1.0 models from [31] was also done. In this case, the main goal was primarily to validate the fact whether the same gates exhibit stable operation also with different transistor technology nodes. Moreover, the attention was also given to the fact if the properties of the most power efficient gate would be independent of the actual transistor model.

Concerning the actual simulation runs, recommended supply voltages [80] together with sizes of transistors directly proportional to the selected technology were chosen. The measurement results for NOR/XNOR gates can be found in Table 3.1. It has been successfully confirmed that the gates are functional also when using 32nm and 65nm technologies. Moreover, the best gates (best in terms of the propagation delay and/or the power consumption) simulated using 45nm models mostly turned out to be dominating also with the other types of transistor models previously mentioned.

Table 3.1: Propagation delay and power consumption of NAND/NOR gates from the PoLibSi library in 32nm, 45nm and 65nm transistor technology nodes.

Function			**65nm, 1.1V**		**45nm, 1.0V**		**32nm, 0.9V**	
(Gate set)	**ID**	**Trans.**	**Delay [ps]**	**Pwr [nW]**	**Delay [ps]**	**Pwr [nW]**	**Delay [ps]**	**Pwr [nW]**
NOR/XNOR (MOS_SIZE_HI)	b1026	7	68	2203	93	1199	107	694
	b1030	7	93	3410	132	1746	150	1029
	b1060	7	93	3354	131	1727	152	1012
	b1499	7	67	2158	91	1174	105	682
NOR/XNOR (MOS_DELAY_HI)	b1499	7	67	2158	91	1174	105	682
	b371	9	55	2246	60	1030	74	658
	c906	10	51	2853	52	1485	59	823
	k412	11	27	835	26	434	27	245
NOR/XNOR (MOS_POWER_HI)	b1499	7	67	2158	91	1174	105	682
	a296	8	90	2001	130	1081	176	598
	b371	9	55	2246	60	1030	74	658
	a552	10	58	898	72	440	111	259
	j658	11	43	719	43	368	44	202
NOR/XNOR (MOS_OPT_HI)	b1499	7	67	2158	91	1174	105	682
	b371	9	55	2246	60	1030	74	658
	g100	10	58	910	65	446	85	262
	k412	11	27	835	26	434	27	245

At this point, the following consideration is naturally arising. How good do the MOSFET based polymorphic gates released in the PoLibSi library prove to be in a direct comparison to circuits implemented by means of using conventional approaches? Are the novel polymorphic gates competitive in terms of the number of transistors, the power consumption and the propagation delay? In general, positive answer can be obviously concluded for gates from the *MOS_OPT_HI* gate set, which is optimised to all those criteria.

As an illustrative example, NOR/XNOR gate was chosen – specifically its implementation with identifier k412 (11 transistors, 26 ps, 434 nW, see Table 3.1). HSPICE simulations of the conventional NOR and XNOR gates with the same transistor models clearly showed interesting evidence that separate (parallel) implementations of NOR and XNOR functions

achieved higher transistor count (12 vs. 11) and demands more power in total (475 nW vs. 434 nW) compared to #k412 NOR/XNOR gate, while the propagation delay is similar ($\approx$ 27 ps). Moreover, the advantage of polymorphic NOR/XNOR gate can be recognised in the already implemented switch between these NOR and XNOR functions, which comes as a natural built-in feature of such circuit components. An implementation of such a switch by means of utilising dedicated piece of additional circuitry would render the conventional circuit to score much worse in all the compared properties.

Another example could be given by means of analysing $0/b$ gate (ID: i1033, 5 tr., 19 ps, 180 nW). Its output assumes a permanent logic 0 in the first mode and an identity of the input in the other mode. For a separate implementation of these functions, no transistor is needed. However, when you consider that the gate is multifunctional and, moreover, it has a high input impedance, then the gate is definitely competitive to the conventional solutions. It should be also emphasised that just a pass-transistor implementation of a single multiplexer requires 6 transistors, power consumption of 233 nW and brings 16 ps delay. Similarly, other gates from the from the MOS_OPT_HI gate set can be identified as comparable or even better.

It was shown that the second generation of MOSFET-based polymorphic gates has much better parameters compared to the first generation. Furthermore, in general, the size-optimized MOSFET gates from the PoLibSi library usually tend to exhibit higher power consumption and longer propagation delay (among the gates of the second generation). By using a few more transistors in the gates, their power consumption and their delay can be improved towards significantly lower values as power&delay-oriented gate set shows. Such polymorphic gates then become competitive to the existing conventional solutions. Thus, polymorphic electronics could be now a reasonable alternative for a designer when a circuit with a second (alternative) function is needed.

3.4.2 Applications of proposed gates

In order to show the advantage of the proposed gate sets, bi-functional image filters were chosen as target applications. To implement these filters as polymorphic circuits, more than twenty size-efficient 8-bit polymorphic RTL components were designed. As target technologies, all previously discussed transistor types were chosen: Ambipolar transistors of Type 1 and Type 2 as well as MOSFET transistors. More precisely, size-efficient gate sets with a high input impedance out of the PoLibSi library were utilised: MOS_SIZE_HI, AMBI_N1_HI, AMBI_P2_HI. Chosen bi-functional RTL components were designed for each transistor type separately.

Table 3.2 shows the resulting number of gates and transistors of the designed RTL components. Implementations of some of them were previously published also by Sekanina et al. [54], who implemented them with a combination of conventional (mono-functional) gates and polymorphic NAND/NOR gate, so far typical approach to implementation of polymorphic circuits. Sekanina designed the components with respect to *relative implementation cost* (relative area). In order to approximately compare the relative cost of Sekanina's components with the newly designed components, whose size is determined in number of transistors, a ratio of 1:4 (4 transistors match one area unit) was considered. That keeps 1 area unit cost of NAND and NOR gates, which are implemented same or similar in all compared technologies.

Calculated relative area and area saving compared to Sekanina's components is listed in Table 3.2 for each RTL component. Relative area of designed RTL components is up

Table 3.2: Implementation cost of RTL components published in [54] and implementation cost of RTL components designed with use of the gate sets from the PoLibSi library. Columns with approximate area savings are denoted „Save“.

RTL	[54]		**MOS_SIZE_HI**				**AMBI_N1_HI**				**AMBI_P2_HI**			
component	**Gates**	**Area**	**Trans.**	**Gates**	**Area**	**Save [%]**	**Trans.**	**Gates**	**Area**	**Save [%]**	**Trans.**	**Gates**	**Area**	**Save [%]**
_or/add			170	34	42.5		208	34	52.0		191	34	47.8	
_or/adds	78	93.8	211	45	52.8	43.8	255	45	63.8	32.0	230	45	57.5	38.7
adds/id			239	50	59.8		286	52	71.5		232	48	58.0	
and			48	8	12.0		48	8	12.0		32	8	8.0	
id/add	69	88.1	182	37	45.5	48.4	216	37	54.0	38.7	182	36	45.5	48.4
id/min	50	68.3	203	51	50.8	25.7	234	51	58.5	14.3	204	51	51.0	25.3
max/add	114	139.2	344	79	86.0	38.2	404	85	101.0	27.4	348	79	87.0	37.5
max/adds			366	83	91.5		442	93	110.5		390	92	97.5	
max/div2	83	98.9	246	58	61.5	37.8	288	59	72.0	27.2	244	58	61.0	38.3
max			204	52	51.0		232	52	58.0		202	51	50.5	
mean/max	118	135.9	330	73	82.5	39.3	368	68	92.0	32.3	308	68	77.0	43.3
min/max	74	86.3	224	52	56.0	35.1	230	53	57.5	33.4	202	51	50.5	41.5
min/mean	117	144.9	346	80	86.5	40.3	407	86	101.8	29.8	360	82	90.0	37.9
min			202	51	50.5		228	53	57.0		202	51	50.5	
min/or			220	51	55.0		232	53	58.0		202	51	50.5	
nand/and	18	26.1	56	8	14.0	46.4	64	8	16.0	38.7	64	8	16.0	38.7
nand/min	77	100.0	218	51	54.5	45.5	267	52	66.8	33.3	227	51	56.8	43.3
or/max	64	90.3	216	50	54.0	40.2	230	52	57.5	36.3	200	50	50.0	44.6
xnor/mean	78	97.8	199	40	49.8	49.1	247	43	61.8	36.9	214	44	53.5	45.3
xor/inv	18	25.5	56	8	14.0	45.1	72	8	18.0	29.4	64	8	16.0	37.3
xor/mean	64	83.0	202	40	50.5	39.2	248	43	62.0	25.3	208	41	52.0	37.3
Average	73.0	91.3	213.4	47.7	53.4	41.0	247.9	49.3	62.0	31.1	214.6	48.0	53.6	39.8

to 49% lower (41% in average) in case of MOSFET transistors, up to 39% lower (31% in average) in case of type 1 ambipolar transistors and up to 48% lower (40% in average) in case of type 2 ambipolar transistors. Although the mentioned ratio is approximate only, it is obvious that the implementation cost of newly designed components is significantly lower. That confirms a hypothesis that a design based on complete sets (complete in terms of the gate functionality) of efficient polymorphic gates of the second generation is more efficient than a design based on a combination of conventional mono-functional gates and a single bi-functional gate (NAND/NOR).

Designed polymorphic RTL components were subsequently used for implementation of three bi-functional image filters. These filters were proposed in [54] for image filtering of various types of noise (shot noise and Gaussian noise elimination), edge detection, dilatation and erosion. The filters are considered as digital circuits with nine 8-bit inputs (3x3-pixel kernel) and one 8-bit output, which process grayscale (8-bits/pixel) images. Their filtering abilities are comparable to the conventional solutions while the implementation cost is significantly lower [54].

Table 3.3 compares implementation costs (relative area) of the filters when different sets of RTL components are utilised. Column „CoABC [54]“ shows cost of filters whose RTL components were implemented with conventional mono-functional gates and later optimised by ABC [6]. Mode of such RTL components, and thus also mode of the filters, is selected by a dedicated input wire (i.e. additional circuit input).

Table 3.3: Implementation cost of image filters created by different RTL components. Ratio of the cost of the newly proposed implementations against column „Proposed in [54]“ (implementations with combination of NAND/NOR gates and conventional gates) is expressed in brackets.

Image filter	**CoABC [54]**	**Proposed in [54]**	**MOSFET**	**Amb. Type 1**	**Amb. Type 2**
Dilatatation/Erosion	569	659	441 (67%)	461 (70%)	404 (61%)
Edges/Shots	1089	1156	743 (64%)	834 (72%)	724 (63%)
Gauss/Shots	1639	1735	1114 (64%)	1290 (74%)	1118 (64%)

The following column in Table 3.3 (column „Proposed in [54]“) represents filters based on the RTL components already mentioned in Table 3.2 – i.e. RTL components created with a combination of conventional (mono-functional) gates and polymorphic NAND/NOR gates and optimised by CGP. Implementation cost of such filters is higher than the conventional one. According to the authors of these filters, it is caused by a high implementation cost of polymorphic multiplexers (6.67 area units) [54].

The second generation of polymorphic circuits brings efficient implementation of the polymorphic multiplexer. Its relative cost is 1.5 in case of MOSFET gate set and 2.0 in case of double-gate ambipolar transistors [32]. However, the low cost of newly designed RTL components is primarily given by a high amount of efficient gates, not only by efficient implementation of the multiplexer!

Last three columns of Table 3.3 show the relative costs of filters created out of the newly designed RTL components – components with the same functions but implemented by polymorphic gates from the PoLibSi library. Implementation costs of those filters are lower compared to the filters where only NAND/NOR gates and conventional gates are con-

sidered (implementation cost ratio is stated in Table 3.3 in brackets). Moreover, proposed implementations are also more size-efficient than filters designed by conventional gates and conventional design approaches (CoABC column). Note that the image filtering capabilities remain exactly the same.

3.5 List of other publications

2017

- ŠIMEK Václav, NEVORAL Jan, CRHA Adam and RŮŽIČKA Richard. **Towards Design Flow for Space-Efficient Implementation of Polymorphic Circuits Based on Ambipolar Components.**. In: *ElectroScope*. Plzeň: University of West Bohemia in Pilsen, 2017, vol. 11, no. 1, pp. 1-10. ISSN 1802-4564.

  Author participation: 20 %

- NEVORAL Jan, ŠIMEK Václav and RŮŽIČKA Richard. **Compact Library of Efficient Polymorphic Gates based on Ambipolar Transistors**. In: *2017 12th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*. Palma de Mallorca: IEEE Circuits and Systems Society, 2017, pp. 155-160. ISBN 978-1-5090-6376-5.

  Author participation: 65 %

2016

- NEVORAL Jan. **Polymorfní obvody na bázi ambipolárních tranzistorů**. In: *Počítačové architektury a diagnostika PAD 2016*. Bořetice: Faculty of Information Technology BUT, 2016, pp. 45-48. ISBN 978-80-214-5376-0.

  Author participation: 100 %

3.6 Research projects and grants

- FIT-S-17-3994 – *Advanced parallel and embedded computer systems, Brno University of Technology.* Team member.
- LD14055 – *Unconventional Design Techniques for Intrinsic Reconfiguration of Digital Circuits: From Materials to Implementation, Ministry of Education, Youth and Sports Czech Republic.* Team member.
- FIT-S-14-2297 – *Architecture of parallel and embedded computer systems, Brno University of Technology.* Team member.

Chapter 4

Conclusions

This chapter summarises the results presented in this thesis and gives conclusions and possible directions for future work.

One of the main issues behind the adoption of polymorphic electronics is related to the lack of suitable polymorphic components – polymorphic gates. Although there have been published more than twenty polymorphic gates controlled by the supply voltage level, the chip temperature or the dedicated control signal, parameters of most of them are far from the ideal ones; no matter whether the power consumption, speed (propagation delay) or area occupied in the chip is taken into account.

The main goal of the research conducted in this thesis was to deeply investigate an approach to the gate-level polymorphism where the circuit function depends on the polarity of supply voltage. It was assumed that a discrete control quantity of such gates can simplify their design and significantly improve their properties compared to the previously published gates (gates of the first generation).

4.1 Contributions

Only a few polymorphic gates controlled by the supply voltage polarity have been published earlier by other authors. Such gates were designed by an ad-hoc approach. In order to systematically design new polymorphic gates at the transistor level, an evolutionary-based design approach was proposed and further improved for design purposes of circuits based on conventional MOSFET and emerging double-gate ambipolar transistors. Fast and sufficiently accurate evaluation of the candidate solutions was reached by discrete simulation with a switch-level transistor model extended by a threshold drop degradation effect. The novelty of the proposed design approach lies primarily in a new circuit representation and new simulation models of transistors. It was shown that the proposed method is successfully capable of designing size-efficient polymorphic gates and smaller polymorphic circuits controlled by the supply voltage polarity. To our best knowledge, it is the first approach for design of circuits controlled by the supply voltage polarity ever and also the first approach for design of circuits based on double-gate ambipolar transistors ever.

It was shown that polymorphic electronics controlled by the supply voltage polarity is not functionally complete when no constant logic value is available in the circuit. In the rest of the research, it was assumed that logic constants (logic zero and logic one) currently exist in the circuit (polymorphic electronics is, for example, combined with conventional

electronics in the chip) or it is possible to create them from the power supply rails in the particular chip manufacturing technology.

Using the evolutionary method, five complete sets of size-efficient bi-functional two-input polymorphic gates controlled by the polarity of dedicated supply voltage were designed. One set is based on MOSFET transistors, the others on double-gate ambipolar transistors. These sets were exposed to the research community in a freely available online library called PoLibSi. Each gate published in the sets is composed of less transistors than it is required for a multiplexer and a separate implementation of individual Boolean functions. That confirmed the hypothesis formulated in Chapter 1.3 of this thesis. Moreover, most of the gates are also composed of same or even much smaller number transistors than it is required for a separate implementation of the individual Boolean functions (without multiplexer).

All gates were validated by HSPICE simulator for 32, 45 and 65nm technology nodes. Furthermore, the delay and the power consumption of all MOSFET gates from the PoLibSi library were determined and attached to the library together with delay-, power- and delay&power-oriented MOSFET-based gate sets. It was shown that the parameters of the MOSFET-based gates are significantly better compared to the first generation of polymorphic gates. Moreover, gates from the delay&power-oriented MOSFET-based gate set proved to be competitive to the conventional solutions in terms of the size, propagation delay and also the power consumption. Accurate properties of the gates based on double-gate ambipolar transistors were unfortunately not investigated because of a current lack of freely available accurate SPICE-compatible transistor models.

All gate sets in the PoLibSi library are complete, i.e. each provides efficient implementation of any pair of two-input Boolean functions. It is supposed that the proposed library may significantly improve complex polymorphic circuits in terms of the resulting size, delay and/or the power consumption. Compared to a few dozen gates of the first generation, author of this thesis showed that the problem with a lack of polymorphic gates with good properties is well solvable (PoLibSi contains even 38117 gates).

Furthermore, it was demonstrated that complete sets of efficient polymorphic gates can contribute to size-efficient implementations of more complex polymorphic circuits. Case study with bi-functional RTL components and applications with two functions were presented. Newly designed RTL components were 14.3 – 49.1% (37.1% in average) smaller compared to the state-of-the-art implementations based on the first generation of polymorphic gates. Bi-functional image filters based on the newly designed gate sets were 30 – 39% smaller than implementations based on the first generation of polymorphic gates and also 19 – 34% smaller than implementations designed by conventional gates and conventional design approaches. In general, it was shown that it is possible to circumvent issues related to the gate-level synthesis of multifunctional circuits in applications involving design at the RT level by moving the synthesis one level up – from the gate level to the RT level. Furthermore, new efficient bi-functional circuits (new in the field of polymorphic electronics) were designed: increment/decrement, adder/subtractor.

Results in this thesis show that polymorphic electronics should be the concept which improves area-efficiency (price) of implementation of circuits with a second function not only at the academical level, but also in practice.

4.2 Developed library available online

As a part of the research, author of this thesis developed the *PoLibSi* library, which is available online at www.fit.vutbr.cz/~inevoral/polibsi. It is the first freely available library

with polymorphic gates ever. PoLibSi contains 38117 bi-functional gates with promising parameters, whose function is selected by the polarity of dedicated power rails. Individual gates are classified into the gate sets. The gate sets differ in the transistor type (MOSFET, double-gate ambipolar transistors), feature which the gate sets were optimised to (transistor count, delay, power consumption) and input impedance constraint. Each gate implementation comprises a schematic, an HSPICE description and simulation results. Moreover, the propagation delay and power consumption are provided for all MOSFET based gates. Figure 4.1 shows an example of gate details in the PoLibSi library. Furthermore, each gate set is complete – it provides at least one (usually even more) efficient implementation of any pair of two-input Boolean functions. The PoLibSi library can be later utilised for design and synthesis of complex bi-functional circuits by other researchers.

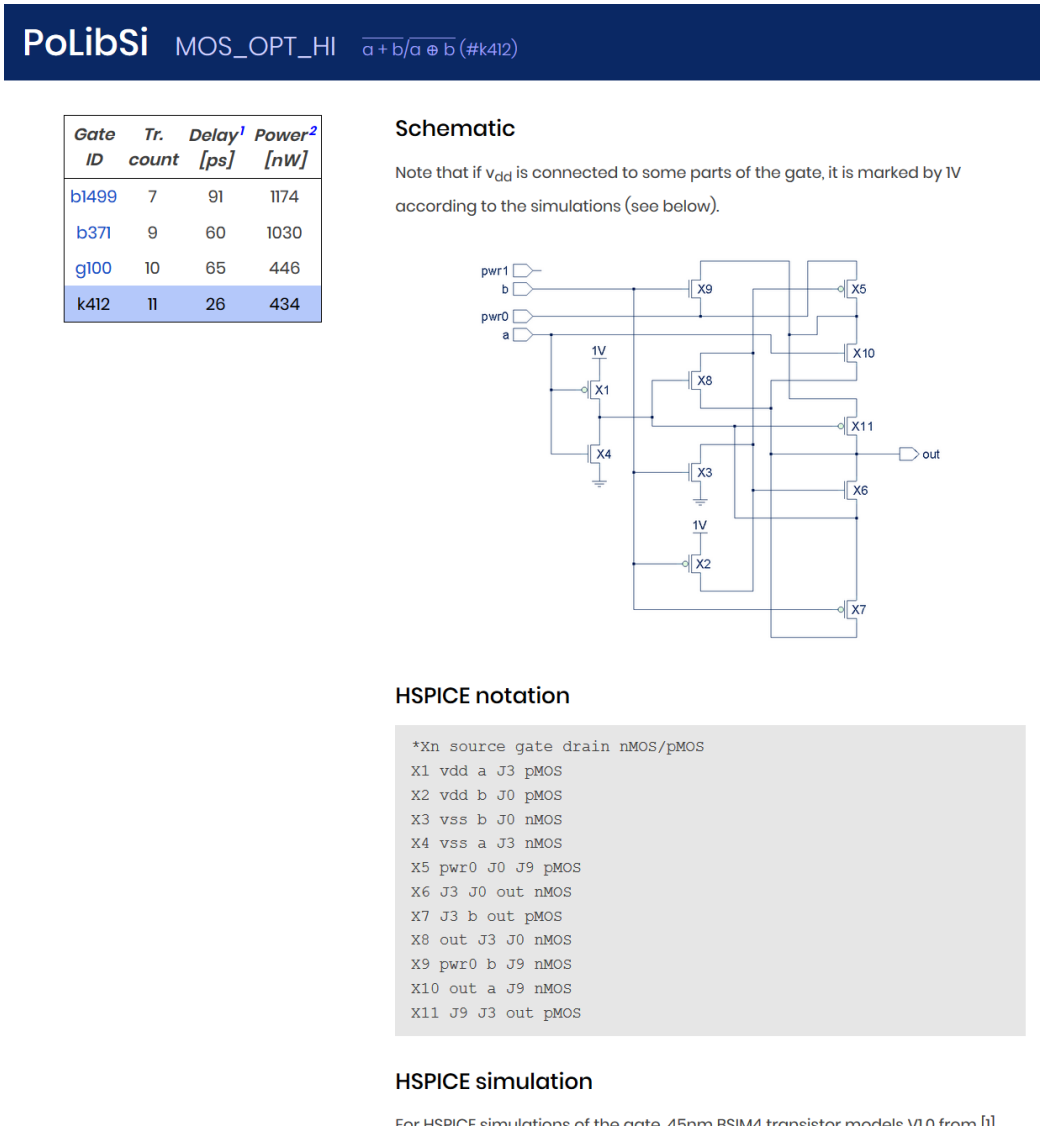

Figure 4.1: Screenshot of the PoLibSi library with details about NOR/XNOR gate with identifier k412 from the MOS_OPT_HI gate set.

4.3 Future work

Besides the five attached papers, which form the core of the dissertation, power consumption of MOSFET-based gates from PoLibSi was already investigated together with different technology nodes (32nm, 45nm and 65nm) of MOSFET transistors. Furthermore, complex RTL components and several applications were designed and compared to both implementations with conventional gates only and implementations with polymorphic gates of the first generation. The results, summarised in Chapter 3.4 of this thesis, are currently submitted as one conference paper and one journal paper.

There are still some different ways how to further develop the research results:

- As soon as accurate models of double-gate ambipolar transistor will be freely available, the propagation delay and power consumption of designed gates can be determined in order to select the best implementation(s) of each polymorphic function.
- The PoLibSi library can be further extended by new gate sets based on other modern on emerging transistor types, e.g. FD-SOI, FinFETs or mono-gate (three-terminal) ambipolar transistors.
- The most promising method for synthesis of polymorphic circuits optimises the circuits in so-called PAIG data structure [13]. The method cannot perform technology mapping. It would be useful to develop a method which efficiently maps such circuits to two-input polymorphic gates with any functions, i.e. to the gates from the PoLibSi library. Such method may also take into account optimisation criteria as size, delay or power consumption.
- The PoLibSi library can be further extended by selected three- or more-input gates (e.g. AND3/OR3, NAND3/XNOR3, etc.) which may also be useful during the circuit synthesis.
- For further research related to the designed MOSFET-based gates and to the gates controlled by power supply polarity, a subset of PoLibSi gates can be designed at the layout level and employed in some integrated circuit similar to REPOMO32 [52] to definitely prove the concept on silicon.

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Appendix A

Curriculum Vitae

Education

Ph.D. of Computer Science and Engineering 2015 – present
Faculty of Information Technology, Brno University of Technology
Supervisor: doc. Ing. Richard Růžička, Ph.D., MBA

Master of Computer and Embedded Systems 2013 – 2015
Faculty of Information Technology, Brno University of Technology
Control Panel with Touchscreen
Supervisor: Ing. Petr Musil

Bachelor of Information Technology 2010 – 2013
Faculty of Information Technology, Brno University of Technology
Design and Realization of Device-Prototype for Multi-Channel Monitoring of Measured Quantities via USB
Supervisor: Ing. Josef Strnadel, Ph.D.

Secondary school 2002 – 2010
Gymnázium Jihlava

Conferences, Institutions

2019

Euromicro DSD (Kallithea, Chalkidiki, GR)

2018

ISVLSI (Hongkong, HK), Euromicro DSD (Prague, CZ), NGCAS (Valletta, MT)

2017

DTIS (Palma de Mallorca, ES)

2016

SSCI (Athens, GR), PAD (Bořetice, CZ)

2015

TEI of Crete, Nanomaterials & Advanced Electronics Group (Heraklion, GR)

Projects

- FIT-S-17-3994 — *Advanced parallel and embedded computer systems, Brno University of Technology.* Team member.
- LD14055 — *Unconventional Design Techniques for Intrinsic Reconfiguration of Digital Circuits: From Materials to Implementation, Ministry of Education, Youth and Sports Czech Republic.* Team member.
- FIT-S-14-2297 — *Architecture of parallel and embedded computer systems, Brno University of Technology.* Team member.

Teaching

- Electronics for Information Technology — *labs*
- Microprocessors and Embedded Systems — *labs, projects*
- Design of External Adapters and Embedded Systems — *lectures*
- Supervised master student
  - Marek Miklíček: Technical Condition Monitoring of Radar Systems Components
- Reviews of bachelor and master thesis

Work Experience

Programmer, junior analyst 2013 – 2015
Stormware, s.r.o., Jihlava, Czech Republic
SW engineer 2016 – present
NXP Semiconductors Czech Republic, s.r.o., Brno, Czech Republic