BRNO UNIVERSITY OF TECHNOLOGY

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF RADIO ELECTRONICS

ÚSTAV RADIOELEKTRONIKY

AN EMC ROBUST PRECISE VOLTAGE REFERENCE FOR AUTOMOTIVE APPLICATIONS

EMC ROBUSTNÍ PŘESNÁ NAPĚŤOVÁ REFERENCE PRO AUTOMOBILOVÉ APLIKACE

DOCTORAL THESIS PROPOSAL
TEZE DIZERTAČNÍ PRÁCE

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BRNO 2023

Keywords

Bandgap voltage reference, Brokaw bandgap voltage reference, electromagnetic compatibility, electromagnetic interference, electromagnetic susceptibility, element-by-element extraction, passive network synthesis, transmission line, voltage reference.

Klíčová slova

Brokawova napěťová reference typu bandgap, elektromagnetická citlivost, elektromagnetická interference, elektromagnetická kompatibilita, extrakce prvek-po-prvku, napěťová reference typu bandgap, napěťová reference, přenosové vedení, syntéza pasivního obvodu.

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Contents

1 INTRODUCTION AND SETTING GOALS

With the increasing advent of high-speed and radio frequency (RF) mix-signal devices, maintaining signal integrity and electromagnetic interference (EMI) susceptibility have become one of the major issues facing modern integrated circuit design. It must be noted that the automotive industry sets high requirements for electronics, especially for used semiconductors, concerning a very wide temperature operating range, ESD pulses, transient overvoltage pulses on supply and signal lines, supply voltage variations, requirements for very low electromagnetic emissions (EME), high immunity to EMI and low power consumption [1]. Harsh EMC disturbances can easily couple from the environment to the ICs through cabling harnesses or printed circuit board (PCB) tracks [2].

An EMC robust integrated circuit design together with a low power design sets a new challenge. One of the EMC robust design guidelines suggests to keep node impedances low and increase current biasing to improve the EMI immunity of the circuit [2]. This is directly opposite to a low-power design, where all currents are minimized. The low-power EMC robust design requires new circuit principles and circuit topologies, and the complete design is dictated by these requirements.

A commonly utilized reference for ICs is a bandgap voltage reference. It is a temperature-independent voltage reference circuit, which produces ideally a fixed (constant) voltage regardless of power supply variations, temperature changes, and circuit loading.

The main topic of the dissertation thesis is to define a methodology for a design of low power and EMC robust voltage references. The proposed EMC robust bandgap design recommendations verified by designs, simulations, and measurements of test chips are presented.

1.1. Thesis Objectives

The doctoral dissertation is focused on a study of bandgap voltage reference EMI susceptibility, especially in the automotive environment. The main aim of this dissertation is to define a methodology to improve the EMC robustness of low-power bandgap voltage references. Proposed methodology recommendations are verified by design, simulations, and measurements of bandgap references fabricated on test chips in various technologies

To be able to study the EMC robustness of the voltage references, the first step is to understand how the IC EMI susceptibility is measured and how the measurement setup can be modeled in the IC impedance environment. A new method for impedance circuit modeling was formulated and implemented. It was utilized for a low power supply network with an EMC power supply filter (a bias-tee) which is used for the power supply EMI susceptibility measurement of the IC.

A detailed study of an existing low-power integrated bandgap voltage reference, which was designed for a harsh automotive environment with a wide temperature range from -40 °C to 160 °C and a demanding immunity to EMI, is performed and results are presented in the dissertation thesis. The possibilities of the power supply EMI susceptibility reduction of the voltage references are also discussed.

Based on this study, a new EMI simulation method was developed. The method involves creating a circuit model of the external coupling path and implementing new requirements for an improved voltage reference that can operate in an extended temperature range from -50 °C to 200 °C. Studies of different topologies for reference functional blocks were conducted, and results are presented in the dissertation thesis. From the achieved results, the best topology was selected and improved. A new methodology for EMC robust low-power voltage reference designs was proposed and verified by manufacturing a test chip with the proposed EMC robust voltage reference.

In summary, the most important objectives of the dissertation thesis are:

a) Create a circuit model of the external impedance environment of the voltage reference with respect to EMI susceptibility analysis, measurements, and simulations.

b) Systematically analyze EMI susceptibilities of existing and commonly used integrated voltage references, which are divided into functional blocks, and analyze these blocks. Compare these results and draw conclusions.

c) Based on the outcome of the analysis, select the best topologies, and try to further improve them with respect to EMI susceptibility. Perform a detailed theoretical study. Propose a design methodology for EMC robust low power bandgap voltage references.

d) Verify the proposed methodology by designing and manufacturing a test chip with a new EMC robust voltage reference and perform a detailed evaluation of the performance. Compare the expected and achieved results.

2 EMI SUSCEPTIBILITY MEASURING CONCEPT AT THE IC LEVEL

The first step of the thesis is to understand how the IC EMI susceptibility is measured and how the measurement setup can be modeled in the IC impedance environment for analytical methods of circuit design.

2.1. Direct Power Injection Measurement Method

The RF Direct Power Injection (DPI) method to the dedicated IC pin described in IEC 62132-4 [3] is used for the EMI susceptibility measurement at the IC level. The typical DPI measurement setup with a directional coupler, which is used for an RF power measurement on a line, is shown in Fig. 1.

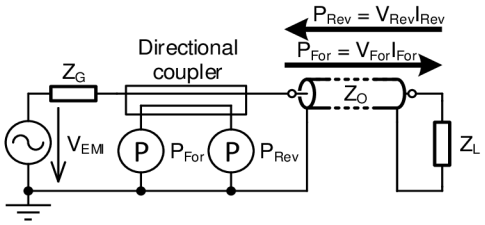


Fig. 1: RF power on the line and its transfer in the typical DPI setup [4].

The RF generator with amplifier is represented by the V_{EMI} sinusoidal voltage source with output (internal) impedance Z_G and the injected IC pin with the coupling capacitor is represented by load impedance Z_L. It must be noted that the value of the coupling capacitor has to be selected with respect to the functionality of the applied IC pin (e.g., according to the maximum capacitive load of the pin). The directional coupler should be matched to the characteristic impedance Z_O and it is always placed between the source and the coaxial line. The source side of the line is matched to its source and therefore the measured forward power P_{For} is equal to the source nominal power P_N [4].

The average value of the alternating power is typically measured by power sensors on R_{RF} resistors, which is equal to characteristic impedance Z_O due to impedance matching (minimum reflection is obtained). The average value of e.g., forward wave power can be calculated according to the following equations

$$P_{For} = \frac{1}{2} I_{ForPeak}^2 R_{RF}, \tag{1}$$

$$P_{For} = \frac{1}{2} \frac{V_{ForPeak}^2}{R_{RF}}. \tag{2}$$

A general RF coaxial cable or an RF coaxial transmission line has a 50 Ω characteristic impedance. It must be noted that the output of the used coaxial line can be connected to the impedance whose value is unknown [5]. For this reason, there can be three general cases of transmission line loading as shown in Fig. 2.

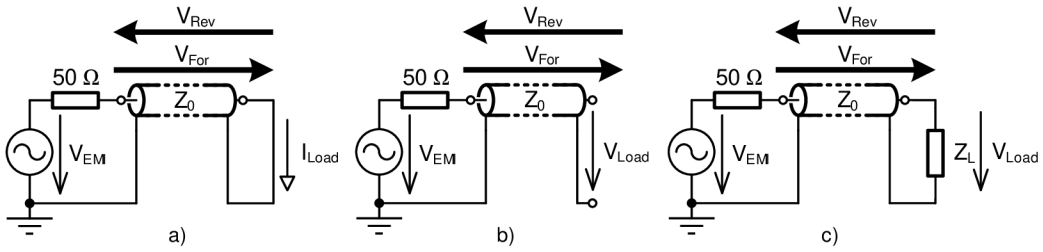


Fig. 2: Three possible states of the RF power injection: a) short, b) open, and c) general load at the end of the transmission line (DPI coupling point).

In the case of short-circuited end of the transmission line, the maximum I_{Load} current flows through the line which can be expressed by equation (19) for $Z_{\mathrm{L}} = 0\ \Omega$ (impedance of ideal electrical short) if the loss-less transmission line is considered.

$$I_{Load} = V_{EMI}\frac{1}{50 + Z_L}. \tag{3}$$

On the other hand, the maximum V_{Load} voltage appears at the line end in the case of the open-circuited end of the transmission line. This voltage can be expressed from the equation for a general loaded loss-less transmission line (20) where Z_{L} is infinity (impedance of ideal open circuit). For this situation, the maximum V_{Load} voltage is equal to V_{EMI}.

$$V_{Load} = V_{EMI}\frac{Z_L}{50 + Z_L} = V_{EMI}\frac{1}{\frac{50}{Z_L} + 1}. \tag{4}$$

Because the low-power IC has low power current consumption and its decoupling capacitors are not often effective at very high frequencies, the high impedance state at the power supply line end can be considered. Therefore, the worst case for the EMI simulation is the DPI to high impedance load. The basic power supply EMI susceptibility simulation is performed with DC and AC (EMI) voltage sources connected in series to form one voltage source, that supplies the analyzed IC.

2.2. Impact of the DPI Measurement Setup

The EMI susceptibility of the real IC is often given by an IC environment. The IC environment is considered such as electric impedances of bond wires, lead frame, and PCB tracks with electrical components at the inputs and outputs. An equivalent circuit model of the RF DPI coupling path to the IC pin is a vital task for the IC EMI susceptibility simulation.

2.2.1. Synthesis of Passive Circuit Network Model

The passive circuit network model synthesis form required circuit function is a classical well-known subject in the electrical circuit theory which was researched in a "golden era" from the 1930s to 1970s, for example [6] and [7]. Nowadays modeling of passive network elements according to high-frequency S-parameters is developed for example in [8] – [10]. The disadvantage of these methods is a very long execution time with many different measurements. The following text describes an extended passive network synthesis method, which requires only a simple two-terminal impedance frequency characteristic measurement.

The passive network model synthesis is an estimation of all passive circuit elements of the circuit model which is valid for the required circuit function in a specified range (e.g., frequency range) and conditions (simplifications). The following described synthesis method based on the element-by-element extraction algorithm [11] is modified and extended to calculate serial and shunt resistors as lossy elements of a passive (linear) circuit network.

The first step of passive network model synthesis from the measured impedance frequency characteristic is obtaining the impedance frequency function [12]. The Laplace representation of impedance can be described by a rational function. The polynomial roots of the rational impedance function determine the impedance frequency characteristic shape. The general impedance rational function according to [11] and [13] with a scaling constant K is given by the following equation

$$Z(\boldsymbol{s}) = \frac{N(\boldsymbol{s})}{D(\boldsymbol{s})} = \frac{\sum_{k=0}^{n} a_k \boldsymbol{s}^k}{\sum_{l=0}^{m} b_l \boldsymbol{s}^l} = K \frac{\prod_{k=1}^{n} (\boldsymbol{s} - \boldsymbol{s}_{z,k})}{\prod_{l=1}^{m} (\boldsymbol{s} - \boldsymbol{s}_{p,l})}, \tag{5}$$

where $N(\boldsymbol{s})$ is the numerator polynomial, $D(\boldsymbol{s})$ is the denominator polynomial, a_k is the k-th numerator polynomial coefficient, b_l is the l-th denominator polynomial coefficient, $\boldsymbol{s}_{z,k}$ is the k-th position of impedance zero, $\boldsymbol{s}_{p,l}$ is the l-th position of impedance pole in the complex $\mathbf{s}$-plane and $\boldsymbol{s}$ is the Laplace variable.

The extended passive network model synthesis method aims to add frequency bandwidths of impedance resonances to obtain lossy elements (resistors and conductors) of the passive circuit model for cases with quality factors lower than infinity. For this situation, a biquad impedance function with complex conjugate pairs of zeros and poles is according to [14]

$$Z(\boldsymbol{s}) = \frac{\boldsymbol{s}^2 + \frac{\omega_\mathrm{z}}{Q_\mathrm{z}}\boldsymbol{s} + \omega_\mathrm{z}^2}{\boldsymbol{s}^2 + \frac{\omega_\mathrm{p}}{Q_\mathrm{p}}\boldsymbol{s} + \omega_\mathrm{p}^2}, \tag{6}$$

where ω_z is the angular serial resonance frequency, Q_z is the zero-quality factor, ω_p is the angular parallel resonance frequency and Q_p is the pole quality factor of the biquad impedance function. By comparing this function with the general quality factor equation according to [15]

$$Q = \frac{\omega_0}{B}, \tag{7}$$

where Q is the bandpass (or resonance) quality factor, ω_0 is the center (or resonance) frequency and B is the bandpass (or resonance) frequency bandwidth, the following impedance function with frequency bandwidths of each resonance and one pole at the beginning of $\boldsymbol{s}$-plane is obtained

$$Z(\boldsymbol{s}) = K\frac{\prod_{k=1}^{\frac{n}{2}}\left(\boldsymbol{s}^2 + B_{2\mathrm{z},k}\boldsymbol{s} + \omega_{2\mathrm{z},k}^2\right)}{\boldsymbol{s}\prod_{l=2}^{\frac{m-1}{2}}\left(\boldsymbol{s}^2 + B_{2\mathrm{p},l}\boldsymbol{s} + \omega_{2\mathrm{p},l}^2\right)}, \tag{8}$$

where $B_{2\mathrm{z},k}$ is the k-th angular frequency bandwidth of serial resonance, and $B_{2\mathrm{p},l}$ is the l-th angular frequency bandwidth of parallel resonance. For passive circuit model synthesis, it is necessary to calculate all polynomial coefficients of the impedance rational function (5) after substituting resonance frequencies and their bandwidths with numeric values into the impedance function (8). The scaling constant K includes an impedance norm coefficient that is described by the following equation

$$k_\mathrm{Z} = \frac{Z_\mathrm{norm}(\boldsymbol{s})}{Z(\boldsymbol{s})}, \tag{9}$$

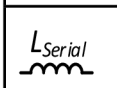
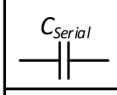
$$K = \frac{1}{k_\mathrm{Z}}, \tag{10}$$

where k_Z is the impedance norm, Z_norm is the normalized impedance and Z is the original impedance [16].

A numerator polynomial degree n of impedance function (5) may be different from a denominator polynomial degree m by no more than one. If this condition is violated, then the circuit model cannot include passive circuit elements only (resistors, conductors, inductors, and capacitors) [11]. The values of angular frequencies can be normalized to the lowest resonance frequency for reducing large numbers in calculations. A software multiplication of polynomials can be done using a simple polynomial multiplication algorithm mentioned for example in [17].

After obtaining all coefficients of the rational impedance function (5) and fulfillment of the passive circuit elements condition, the next step is a passive network model elements extraction. The extraction algorithm is extended to serial and shunt resistors (lossy elements) calculation. The polynomial division is used for the impedance elements calculation which brings six considered solutions from all possible solutions summarized in Tab. 1.

Tab. 1: Simple circuit element extraction conditions and calculations (the first step of extraction for this case, for the next step, there is residual polynomial after polynomials division) [5].

Element	$Z_x(s)$ or $Y_x(s)$	Conditions of $Z(s)$ function	Element value
	$Z_x(\boldsymbol{s}) = R_{\text{Serial}}$	$n = m, D[m] > 0$ and the previous element is $Z(s)$ type	$R_{\text{Serial}} = \dfrac{N[n]}{D[m]}$
	$Y_x(\boldsymbol{s}) = G_{\text{Shunt}}$	$n = m, N[n] > 0$ and the previous element is $Y(s)$ type	$G_{\text{Shunt}} = \dfrac{D[m]}{N[n]}$
	$Z_x(\boldsymbol{s}) = \boldsymbol{s}L_{\text{Serial}}$	$n > m$ and $D[m] > 0$	$L_{\text{Serial}} = \dfrac{N[n]}{D[m]}$
	$Z_x(\boldsymbol{s}) = \dfrac{1}{\boldsymbol{s}C_{\text{Serial}}}$	$N[0] > 0$ and $D[0] = 0$	$C_{\text{Serial}} = \dfrac{D[1]}{N[0]}$
	$Y_x(\boldsymbol{s}) = \dfrac{1}{\boldsymbol{s}L_{\text{Shunt}}}$	$N[0] = 0$ and $D[0] > 0$	$L_{\text{Shunt}} = \dfrac{N[1]}{D[0]}$
	$Y_x(\boldsymbol{s}) = \boldsymbol{s}C_{\text{Shunt}}$	$n < m$ and $N[n] > 0$	$C_{\text{Shunt}} = \dfrac{D[m]}{N[n]}$
$Z(\boldsymbol{s}) = \dfrac{N(\boldsymbol{s})}{D(\boldsymbol{s})} = \dfrac{N[0] + N[1]\boldsymbol{s} + N[2]\boldsymbol{s}^2 + \cdots + N[n]\boldsymbol{s}^n}{D[0] + D[1]\boldsymbol{s} + D[2]\boldsymbol{s}^2 + \cdots + D[m]\boldsymbol{s}^m}$			

The following equations (11) – (13) show an example of impedance rational function polynomial divisions (without resonance bandwidths for clarity), where $Res_x(\boldsymbol{s})$ is the residual polynomial.

$$Z(\boldsymbol{s}) = \frac{N(\boldsymbol{s})}{D(\boldsymbol{s})} = Z_1(\boldsymbol{s}) + \frac{Res_1(\boldsymbol{s})}{D(\boldsymbol{s})}, \tag{11}$$

$$\frac{D(\boldsymbol{s})}{Res_1(\boldsymbol{s})} = Y_1(\boldsymbol{s}) + \frac{Res_2(\boldsymbol{s})}{Res_1(\boldsymbol{s})}, \tag{12}$$

$$\frac{Res_1(\boldsymbol{s})}{Res_2(\boldsymbol{s})} = Z_2(\boldsymbol{s}) + \frac{Res_3(\boldsymbol{s})}{Res_2(\boldsymbol{s})}. \tag{13}$$

The condition for performing the next polynomial division is the positive real residual function after the current division. If the residual function Res_x is negative, then the impedance rational function cannot be assembled from the passive circuit elements in the Cauer passive network model form. On the other hand, negative resistors in the mathematical circuit model can be considered because this model can be used for computer simulation only.

If the mentioned polynomials division steps are applied, then the division results can be written into the following continuous fraction expansion

$$Z(\boldsymbol{s}) = Z_1(\boldsymbol{s}) + \frac{1}{Y_1(\boldsymbol{s}) + \frac{1}{Z_2(\boldsymbol{s}) + \cdots}}. \tag{14}$$

This ladder equation according to [18] has passive network realizations called first and second Cauer canonical forms which are shown in Fig. 3.

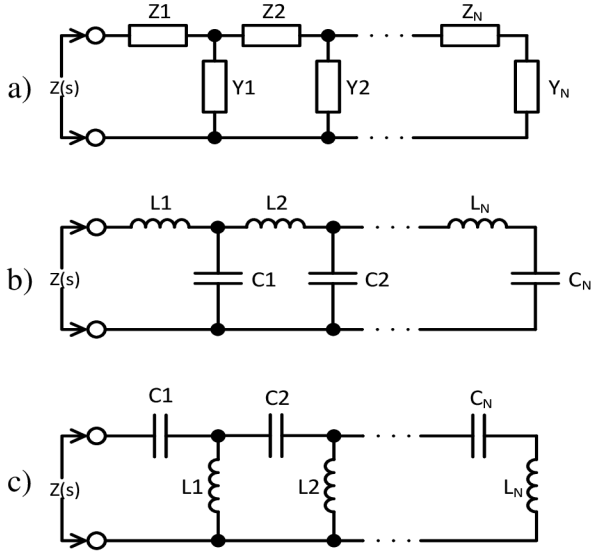


Fig. 3: a) The general Cauer passive network impedance model, b) the first Cauer, and c) the second Cauer canonical form [5].

From a practical point of view, it must be noted that all measured impedance function elements are unknown except the one element that is always presented in the measurement setup. This element is an RF input coupling capacitor that creates the one impedance pole at the beginning of the $\boldsymbol{s}$-plane. The first serial capacitor C_C of the synthesized passive network is the coupling capacitor, and its capacity value is used as the reference value for the calculation of other circuit model elements [5]. This coupling capacitor capacity can be measured by an electronic impedance meter like an LCR meter with four terminal-pair definitions [19]. Fig. 4 shows a realization example of measured impedance function with lossy elements.

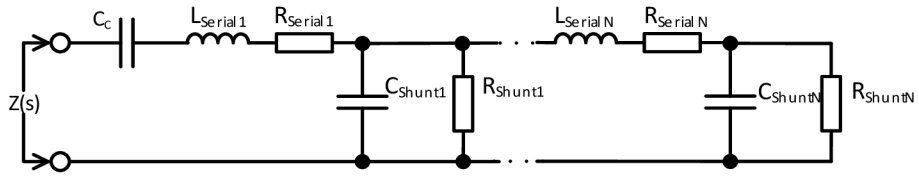


Fig. 4: A passive circuit network model example of the proposed element-by-element extraction method.

2.2.2. Bias-Tee High-Frequency Circuit Model

The bias-tee is a three-port EMC filter that combines the DC and AC (high frequency) signal path into one path with the DC and AC part of the signal. The target of this device is to isolate the coupling path or tested pin from the low impedance of the DC power supply. Otherwise, the bias-tee can be used for AC signal part minimalization for DC signal measurement as a protection of a voltmeter. The bias-tee is often used in EMC susceptibility setup which is used for the DPI method measurement at the IC level according to IEC 62132-4 [3]. The real example of the bias-tee, its photo, its schematic diagram, and its high-frequency impedance measurement setup diagram are shown in Fig. 5.

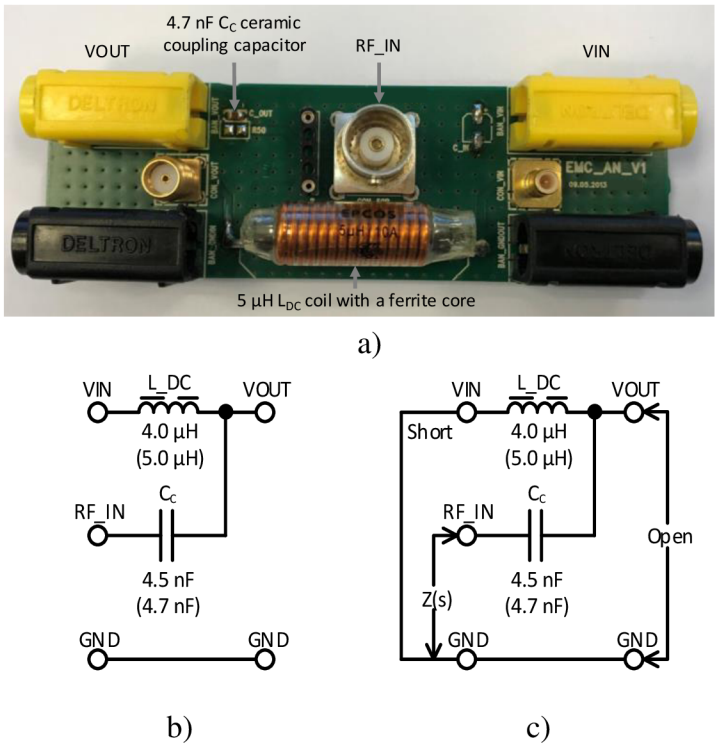


Fig. 5: The bias-tee a) photo, b) its schematic diagram, and c) its impedance measurement setup schematic diagram [5].

The 4.7 nF coupling capacitor was selected according to the RF DPI immunity test method, which is used for the EMS test at the IC level [3]. The synthesized passive circuit model from these parameters is shown in Fig. 6.

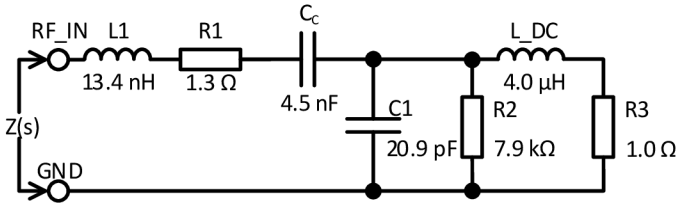


Fig. 6: The synthesized passive circuit model of the bias-tee [5].

The impedance characteristics vs. frequency as the impedance measurement and AC simulation results of the bias-tee real circuit and its synthesized circuit model from the SPICE circuit simulator are shown in Fig. 7 and Fig. 8.

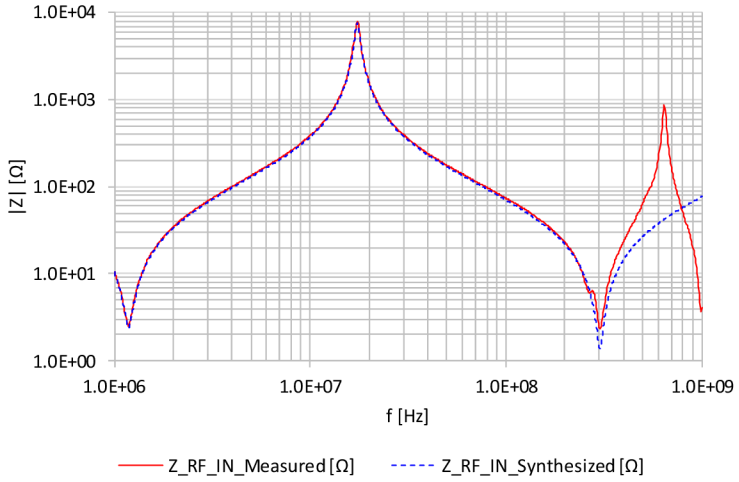


Fig. 7: The impedance magnitude characteristics of the measured bias-tee and its synthesized circuit model [5].

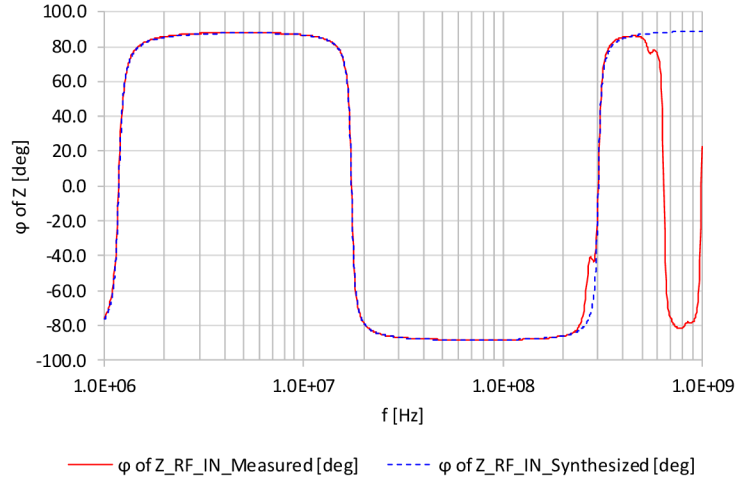


Fig. 8: The impedance phase characteristics of the measured bias-tee and its synthesized circuit model [5].

The bias-tee circuit model is built of frequency-independent elements and the simulated results show a very good correlation with measured results in the frequency range from 1 to 200 MHz. The synthesized circuit model is a simplified finite lumped approximation for distributed parameter circuit systems. Therefore, the correlation at last considered resonance frequency is poor.

An impedance network synthesizer software was used for the passive network circuit model calculation. The software uses all methods corresponding with the element-by-element extraction method which was described in the thesis. A graphical user interface of the software is shown in Fig. 9.

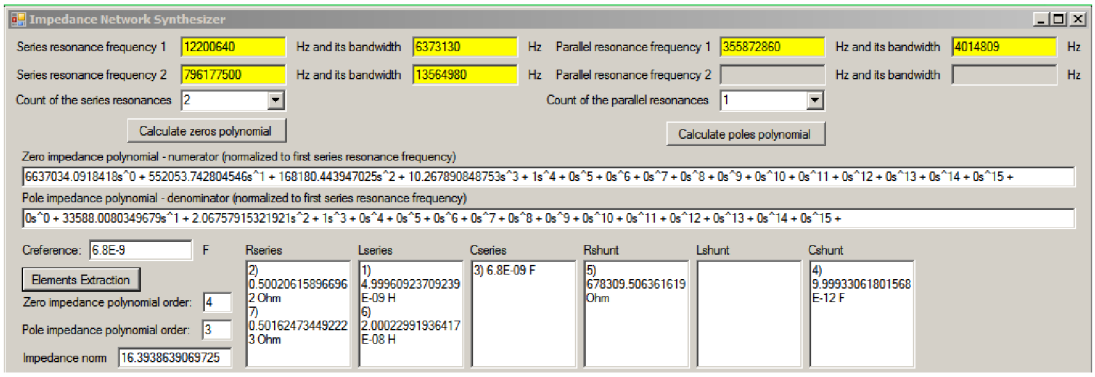


Fig. 9: The passive network impedance synthesizer software using the proposed element-by-element extraction method (results are rounded to appropriate decimal places) [5].

The described passive network model synthesis method and the achieved results were published in the "A Passive Network Synthesis from Two-Terminal Measured Impedance Characteristic" paper [5]. The practical results of the EMI susceptibility simulation with the synthesized passive circuit model of the bias-tee, which supplies the first investigated voltage reference, compared with an EMI DPI susceptibility measurement are shown in Fig. 10.

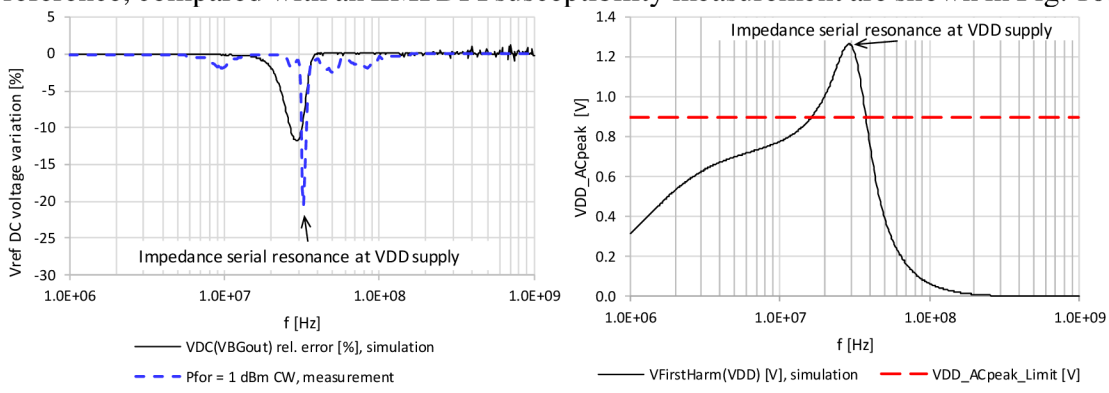


Fig. 10: The a) V_{Ref} DC voltage variation and b) AC voltage at VDD supply of the bandgap DPI setup model simulation with $V_{EMIpeak}$ = 0.710 V (1 dBm P_{For}) [20].

The EMI susceptibility simulation results show that the internal VDD AC signal is higher than the allowable limit, which is 0.9 V in peaks. The highest peak is caused by a VDD impedance serial resonance seen from the RF source with a high RF current which also flows through the IC's small capacitances. The measurement and simulation results confirm this hypothesis and for further EMI susceptibility improvement, it must be VDD serial resonances taken into account. The mentioned voltage reference and results were published in the "An Automotive Low-Power EMC Robust Brokaw Bandgap Voltage Reference" paper [20].

3 PROPOSED VOLTAGE REFERENCE

Detailed study of the low power and EMC improved Brokaw bandgap voltage reference and systematic EMI susceptibility analyses of voltage reference blocks are presented in the thesis. Chapter 3.1 discusses the theoretical possibilities of power supply EMI susceptibility reduction and chapter 3.2 shows the comparative analysis of different basic bandgap cores. Based on the outcome of these analyses, chapter 3.3 presents the new proposed EMC robust voltage reference with the proposed new EMC robust design methodology.

3.1. Possibilities of the Power Supply EMI Susceptibility Reduction

From all the achieved results in the thesis about power supply EMI susceptibility of the low power Brokaw bandgap voltage reference in this work, it is evident, that the main issue is the resonances on the power supply line. These resonances can create a higher voltage supply ripple than the EMI generator can produce when it drives a high impedance load in the ideal case. Therefore, it is important to pay more attention to this phenomenon and consider here some compensation for this effect by, e.g., using the discussed following techniques:

a) Using a fast rectifier at the supply line for the bandgap reference.

b) Using a passive VDD supply net resonance damping circuit.

c) Using an active VDD supply net resonance damping circuit.

d) Using a fast VDD supply switch controlled by the internal VDD supply voltage value, which cannot be very low or very high.

e) Using an EMC robust voltage pre-regulator for the bandgap supply.

The presented techniques for EMC robust design are listed from the simplest to more complex and more expensive. The following text discusses the pros and cons of each mentioned technique.

Ad a) Pro is a high-frequency EMI translation to an ideal DC value of the voltage supply in case of appropriate supply filtration. Cons are reverse voltage stress when rectified voltage increases up to a given limit value by high EMI peaks and the finite speed of the rectifier due to its reverse recovery time. The unwanted capacity between input and output reduces the upper limit of the frequency range as well.

Ad b) Pro is resonance voltage peak damping, ideally in a wide frequency range. Con is higher power dissipation of a damping element, e.g., resistor, which causes resonance energy loss. This unpredictable loss causes a temperature increase in the element, which may lead to the element's destruction.

Ad c) Pros are resonance voltage peak damping, ideally in a wide frequency range, and lower power dissipation of the damping element. Cons are the finite speed of active damping and increased complexity. The active damping realization is very difficult at higher frequencies.

Ad d) Pros are voltage supply values in the required range and ideally zero power dissipation of the switch. Cons are the finite speed of the switch control, unwanted capacity between input and output of high voltage switch, and increased complexity.

Ad e) Pros are increased overall PSRR and regulated bandgap voltage supply in the required range with a higher dynamic range of a higher external supply domain. Cons are controlled startup procedure (first egg or chicken issue), higher requirements for higher external supply voltage (e.g., undervoltage/overvoltage transients with internal supply discharging/charging effects), and increased complexity.

From the mentioned resonance compensation techniques, the voltage pre-regulator for the bandgap supply is practically the most used. This voltage regulator has mostly a built-in unprecise voltage reference due to supplying the precise voltage reference during the startup phase. When the precise reference voltage is up to a given value (e.g., 80% of nominal value), then the voltage regulator is switched to this precise reference voltage in order to parametric regulation of the output voltage. The description of the EMC robust voltage pre-regulator is not intended in this work. The voltage reference only will be examined and improved for EMI susceptibility in case of low PSRR of the integrated voltage pre-regulator, which is externally supplied from the pin. The voltage regulator will be bypassed by a direct connection to the internal voltage reference supply during measurements.

For further work, an effort is taken to find new techniques and principles for EMI susceptibility improvement of the new voltage reference. Before finding new techniques for susceptibility reduction, systematic studies of commonly used voltage reference core and OTA topologies are conducted in the thesis. From the achieved results, a suitable basic topology of the voltage reference is selected for further improvements and investigations.

3.2. Study of Different Integrated Basic Bandgap Cores

Systematically analysis of existing and commonly used bandgap core topologies of voltage references was published in the "An EMC Susceptibility Study of Integrated Basic Bandgap Voltage Reference Cores" paper [22]. The paper includes temperature drift, sensitivity to OPA amplifier input offset, line regulation, and EMC susceptibility comparisons for Kuijk, Brokaw, and Tsividis concepts with a reduced count of BJTs.

Many articles focus on the temperature dependence of voltage references usually within a limited temperature range from -50 °C to 125 °C [23]-[28]. With this temperature range, the reachable temperature coefficients (TCs) are tens of ppm/°C and even 2 ppm/°C with some more advanced techniques. However, higher current consumption and higher supply voltage requirements are the costs of these very low-temperature variations [29]. In the automotive industry, the maximum junction temperature can go up to 200 °C during operation. Voltage references designed to handle such high temperatures often use advanced curvature correction techniques based on measurement of temperature characteristics and trimming [29], [30].

The automotive voltage references in sub-micron technologies are also limited by supply voltage, where the reference has to be parametric, e.g., from 2 V, to support fluctuating supplies [29]. The current consumption from this onboard power supply can be around 10 µA for a complete system on chip, including voltage reference, regulators, wakeup blocks, etc. [29].

From the above-mentioned requirements, the following criteria for the analysis of the basic bandgap cores are considered: temperature drift over a wide temperature range from -50 °C to 200 °C, line regulation for supply voltage from 2 V to 4 V, and low EMI susceptibility over wide high frequency (HF) range from 100 kHz to 1 GHz. The current consumption of the bandgap shall be less than 5 µA. It is worth noting that MOS transistors in a subthreshold region can be used instead of BJTs, but they are usually not used in automotive bandgap designs due to their weakness in noise immunity [29]. To compare bandgap core topologies and not BJT properties, only NPN bandgap cores will be used further [22].

3.2.1. Investigated Bandgap Cores

There are several well-known basic topologies of bandgap voltage reference cores. The first chosen one is the Kuijk, the second one is the Brokaw, and the third one is the Tsividis bandgap core [31]. The investigation proposes nine simple cores from the three chosen basic bandgap core topologies with two methods of collector leakage current compensation. The compensation BJT Q3 with a floating emitter [20] and a shorted base-emitter (BE) junction connected to an emitter of Q2 [21] as two different versions for the leakage compensation were chosen. With the floating emitter, the impact of the collector substrate junction leakage is mainly expected. With the shorted BE junction connected to the emitter of Q2, a leakage current of closed bipolar to the circuit in emitters of BJTs is added. Fig. 11 shows the proposed bandgap cores.

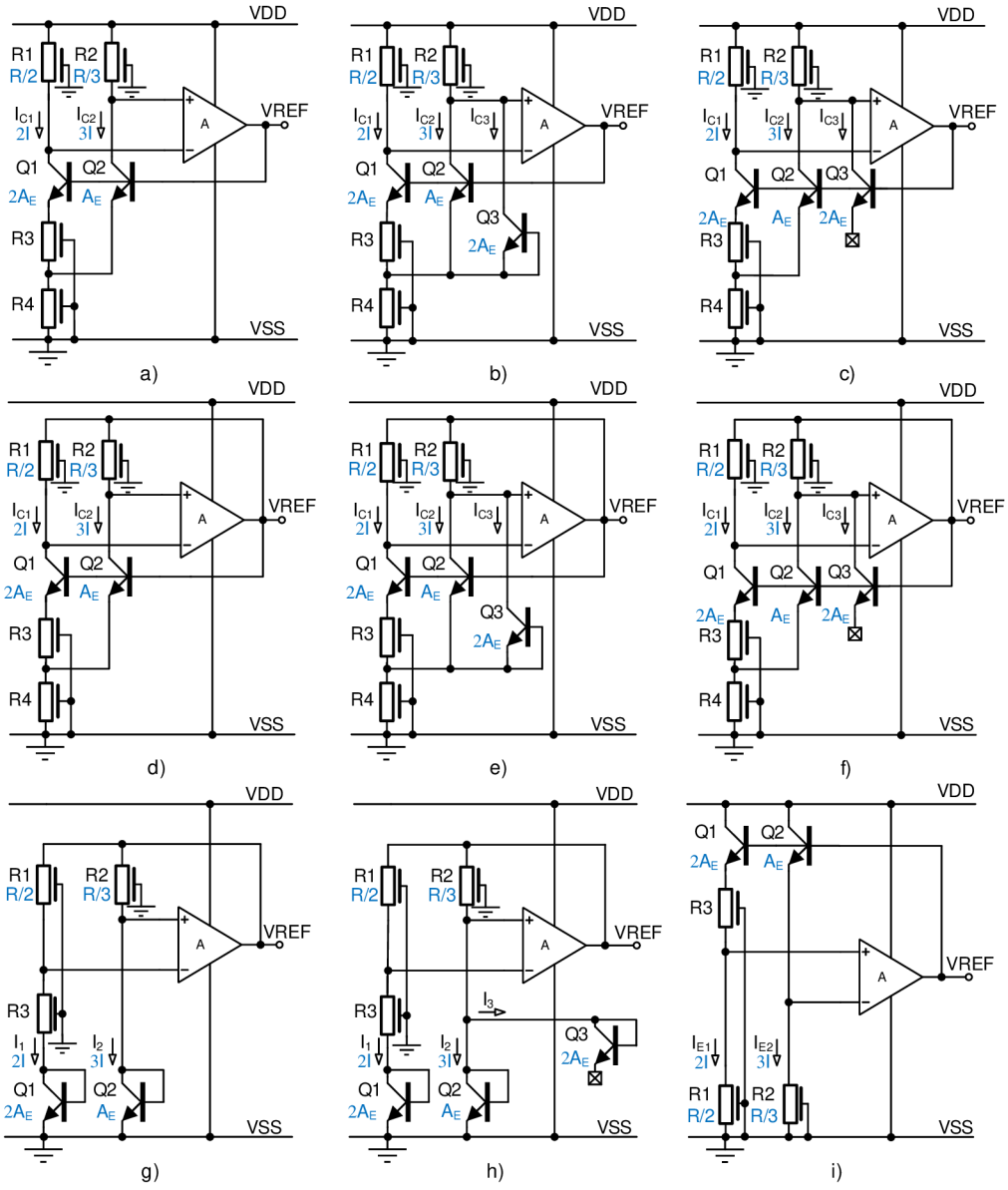


Fig. 11: The proposed bandgap cores for investigations [22].

The chosen bandgap cores are:

a) Brokaw bandgap 2:1,

b) Brokaw bandgap 2:1 with the collector leakage current compensation where the compensation BJT has shorted BE junction,

c) Brokaw bandgap 2:1 with the collector leakage current compensation where the compensation BJT has a floating emitter,

d) Self-supplied Brokaw bandgap 2:1,

e) Self-supplied Brokaw bandgap 2:1 with the collector leakage current compensation where the compensation BJT has shorted BE junction,

f) Self-supplied Brokaw bandgap 2:1 with the collector leakage current compensation where the compensation BJT has a floating emitter,

g) Kuijk bandgap 2:1,

h) Kuijk bandgap 2:1 with the collector leakage current compensation where the compensation BJT has a floating emitter, and

i) Tsividis bandgap 2:1.

The well-known Brokaw 8:1 bandgap core as a reference is also included. All proposed bandgap cores are designed to have the same operating point, such as bias currents of the cores and the same ratio of currents and BJTs. The current consumption of each bandgap core is around 1.3 µA. The one collector current compensation is chosen only for the Kuijk bandgap core due to the connection of the BJTs like diodes. Only BJT's intrinsic reverse polarized diodes between collectors and VSS ground keep collector leakage currents in the same ratio as the ratio of working currents I_1:I_2 (Fig. 11 h)). In general, the Tsividis core does not need leakage current compensation in collectors because it uses the emitter currents. Therefore, this core without compensation transistors (Fig. 11 i)) is first analyzed [22].

3.2.2. EMI Susceptibility

The EMI susceptibility simulation was performed as transient envelope analysis with fifteen harmonics by Cadence Spectre RF simulator. The simulation results are post-processed after the circuit settles for the VREF DC and the first harmonic for each selected bandgap core. The Brokaw cores with both leakage current compensations and the Tsividis bandgap cores were compared [22]. The EMI susceptibility results as relative VREF DC voltage shifts are shown in Fig. 12.

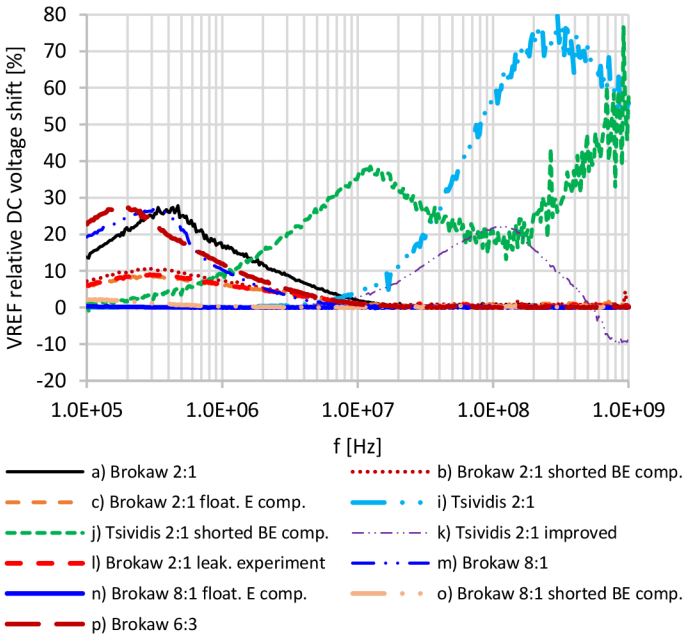


Fig. 12: Relative VREF DC voltage shifts of the selected bandgap cores induced by the 1 V peak sinusoidal HF EMI on the VDD supply with 3 V DC [22].

The Brokaw 2:1 and 8:1 cores without leakage current compensation have medium EMI susceptibility due to unbalanced time constants defined by the collector resistors and BJT collector to VSS capacitances. When the floating emitter leakage current compensation (marked as the “float. E comp.”) is used, the collector RC time constants are balanced for Brokaw cores. The leakage current compensation with shorted BE (marked as the “shorted BE comp.”) also shows influence by the CB junction capacitance. While this version is good for low-temperature drift, the EMI susceptibility shows slightly unbalanced collector time constants resulting in a slightly higher voltage shift. Both leakage compensations show a low rectification effect, which causes reference voltage shifts due to collector capacitances balancing at the OPA inputs. An effect of different collector resistors for Brokaw 2:1 with balanced BJT capacitors (Fig. 12 c)) can be seen in a frequency range from 100 kHz to 10 MHz. This is caused by the resistor’s parasitic capacitance between its poly layer and the well below, which is connected to VSS. When the collector resistors are the same, they have the same parasitic capacitance. These resistors with balanced BJT capacitors cause a very low reference voltage shift, as can be seen for Brokaw 8:1 core with floating emitter leakage compensation (Brokaw 8:1 float. E comp. in Fig. 12 n)) [22].

The Tsividis 2:1 cores have high EMI susceptibility caused by the CB junction capacities. These capacities are effective at a higher frequency than 1 MHz. These capacities, together with the BJT capacities and emitter resistances, create unbalanced RC networks, which result in pass band rectification of the HF interference on the VDD supply. The Tsividis 2:1 improved core by approximately balanced RC networks shows lower EMI susceptibility (Fig. 12 k)) as was expected. A power supply rejection ratio (PSRR) of selected bandgap cores within EMC susceptibility analyses was investigated as well. The reference voltage PSRR of each selected core is calculated from the first harmonic voltage amplitudes using the following equation

$$VREF\_PSRR = 10\,log\left(\frac{\Delta V_{VDD}^2}{\Delta V_{ref}^2}\right) = 20\,log\left(\frac{\Delta V_{VDD}}{\Delta V_{ref}}\right), \tag{15}$$

where ΔV_{VDD} is a change in the VDD supply, and ΔV_{ref} is a change in the reference voltage. The changes as first harmonic voltage amplitudes were considered [22]. The VREF PSRRs of selected bandgap cores are shown in Fig. 13.

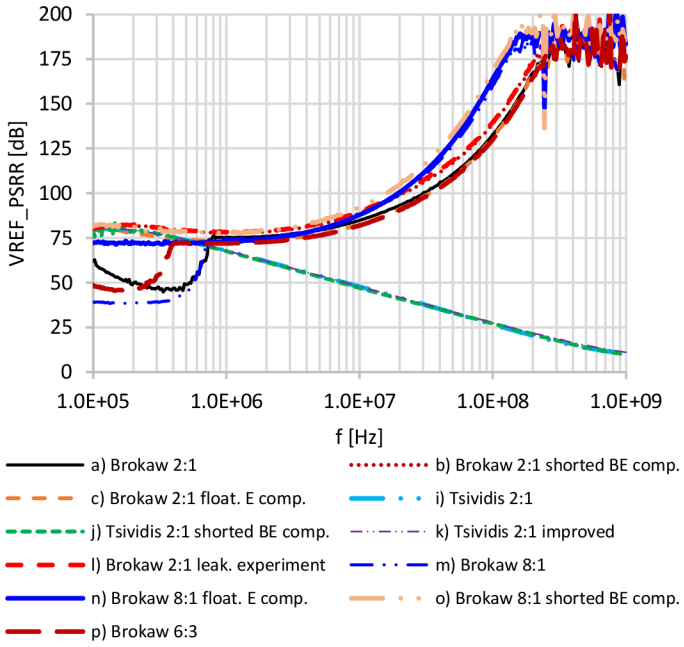


Fig. 13: The PSRR of the selected bandgap cores induced by the 1 V peak sinusoidal HF EMI [22].

The VREF PSRRs of the selected bandgap cores reflect behaviors of relative VREF DC voltage shifts from Fig. 12. The unbalanced collector RC time constants of the Brokaw cores without leakage current compensation cause a small OPA input differential voltage that is amplified by the OPA. This amplified AC voltage is added to the voltage reference resulting in lower PSRR. It must be noted that the OPA model has a 1 MHz unity gain bandwidth. The leakage current compensation balances the collector RC time constants and results in higher PSRR in a frequency range from 100 kHz to 1 MHz. The Tsividis cores have low PSRR at higher frequencies above 1 MHz due to VDD coupling to the output through CB junction capacities [22].

Study results of proposed bandgap cores include temperature coefficients calculated from temperature drifts, relative sensitivities to OPA offset, relative line regulations in VDD range from 2 V to 4 V, output voltage noise, mismatch, and relative voltage DC shifts with PSRRs within EMI susceptibility analyzes. It must be noted that the self-supplied Brokaw and Kuijk cores were supplied from the ideal OPA model, which is not dependent on VDD supply like a real OPA. For this reason, the line regulation and EMI susceptibility with PSRR results are not included in this table because the results are dependent on the parameters of the used OPA. These results are in the following summary table Tab. 2.

Tab. 2. Comparison of proposed bandgap cores [22].

Proposed bandgap cores	Parameters							
	No. of BJTs [-]	TC [ppm/°C]	Sensitivity to OPA offset [%/mV]	Line regulation [%]	Voltage noise at 1 Hz [μV/√Hz]	mismatch 6 sigma [mV]	DC shift induced by HF EMI on VDD max. [%]	PSRR min. [dB]
a) Brokaw 2:1	3	18.3	0.07	0.06	4.2	28.5	27.8	44.8
b) Brokaw 2:1, shorted BE comp.	5	10.9	0.07	0.06	4.2	28.5	10.6	77.7
c) Brokaw 2:1, floating E comp.	5	10.7	0.07	0.06	4.2	28.5	8.7	73.2
d) Self-supplied Brokaw 2:1	3	46.5	1.19	NA*	5.4	31.6	NA*	NA*
e) Self-sup. Brokaw 2:1, short. BE comp.	5	66.0	1.19	NA*	5.4	31.6	NA*	NA*
f) Self-sup. Brokaw 2:1, float. E comp.	5	43.2	1.19	NA*	5.4	31.6	NA*	NA*
g) Kuijk 2:1	3	71.8	1.81	NA*	5.6	27.1	NA*	NA*
h) Kuijk 2:1, float. E compensation	5	23.1	1.81	NA*	5.6	27.1	NA*	NA*
i) Tsividis 2:1	3	11.5	1.82	0.05	5.4	28.5	79.9	10.3
j) Tsividis 2:1, shorted BE comp.	5	11.1	1.82	0.05	5.4	28.5	76.8	9.8
k) Tsividis 2:1 with improvements	5	11.5	1.82	0.05	5.4	28.5	22.3	11.1
l) Brokaw 2:1 leakage experiment	5	15.1	0.07	0.06	4.2	28.5	9.0	78.3
m) Brokaw 8:1	9	57.5	0.05	0.06	3.3	15.7	26.7	38.3
n) Brokaw 8:1, float. E compensation	16	12.1	0.05	0.06	3.3	15.7	0.4	71.4
o) Brokaw 8:1, shorted BE comp.	16	17.4	0.05	0.06	3.3	15.7	2.2	77.5
p) Brokaw 6:3	9	39.1	0.08	0.06	3.1	18.2	27.3	45.4

Note that the NA* means not available due to using the ideal OPA model.

3.3. EMI Susceptibility Improved Voltage Reference

This chapter presents the new proposed EMC robust voltage reference with the new EMC robust design methodology based on the outcome of previous analyses.

3.3.1. Selection of the Bandgap Reference Core

On top of the bandgap core EMI susceptibility comparison results in chapter 3.2, the Brokaw 2:1 with floating E leakage compensation was chosen with a 3:2 collector current ratio. This bandgap core has a low-temperature coefficient of about 10.7 ppm/°C in the temperature range from -50 °C to 200 °C with well-basic EMC robustness. The chosen bandgap reference core is shown in the following Fig. 14.

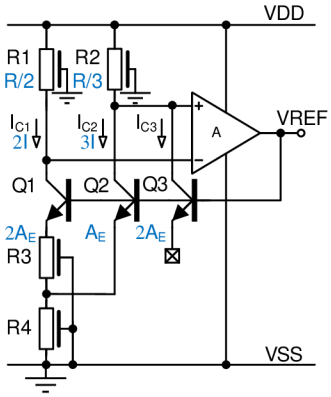


Fig. 14: The chosen bandgap reference core.

3.3.2. OTA Improvements

The OTA, which is a part of the bandgap, highly impacts the EMI susceptibility of the complete voltage reference [33]. In general, the common mode EMI plays an important role there. This type of EMI can be suppressed when the amplifier has a symmetrical input stage with a fully symmetrical load in case of the symmetrical rectification effects [32]. For this reason, a folded cascode OTA was chosen.

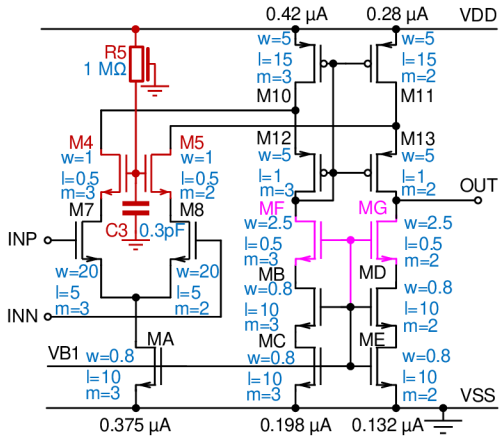


Fig. 15: The proposed one-stage folded cascode OTA.

Fig. 15 shows a circuit diagram of the improved one-stage folded cascode OTA with PMOS and NMOS pseudo-cascode current mirror structures described in [28]. The proposed folded cascode OTA denotes a wide input common mode range (ICMR) from 0.5 to 2.9 V within linearity error below 1 mV, an open loop gain of 85 dB, a unity gain bandwidth of 95.5 kHz with a phase margin of 84° and current consumption of the amplifier is only 0.7 μA. From these parameters, it is evident that the amplifier is designed to tolerate high common mode input voltage, which can be created by EMI in the bandgap core. The wide ICMR is achieved by the M7 and M8 input differential pair with a weak inversion operating point due to high transconductance with low bias current, as was stated in [20] and [32].

Because the bandgap core has asymmetrical collector impedances within the 3:2 collector current ratio, the comparison between a 1:1 fully symmetrical and a novel 3:2 asymmetrical OTA will be investigated. The introduced 3:2 ratio respects the impedance ratio of the bandgap core at the amplifier differential input. The basic folded cascode OTA topology presented in [20] was used as an initial topology. The topology will be improved so the following configurations will be analyzed, refer to Fig. 15:

a) The basic version with simple bias (MB – ME only) and the 1:1 ratio (the same m-factors),

b) The basic version with simple bias and the 3:2 ratio,

c) Bias pseudo-cascodes (MB – MG) within the 3:2 ratio, and

d) Bias pseudo-cascodes with additional input NMOS cascode (M4 and M5) within the 3:2 ratio.

The small signal open loop gains across the different folded cascode OTA configurations are shown in the following Tab. 17.

Tab. 3. Open loop gains of proposed OTA configurations.

OTA configuration	A_{OL} [dB]	UGBW [kHz]	PM [°]
a) Simple bias, 1:1	73.3	117.3	80.8
b) Simple bias, 3:2	71.5	95.5	84.6
c) Bias pseudo-cascodes, 3:2	84.9	95.5	84.4
d) Input cascode added, 3:2	85.0	95.5	84.3

The gain between the fully symmetrical and asymmetrical topologies differs by about 1.8 dB. This is the expected change due to transconductance changes caused by the different bias currents. The configuration with bias pseudo-cascodes brings its benefit, besides the OTA gain increase, in a wider VDD supply voltage room. Finally, the additional input NMOS cascode (M4 and M5 in Fig. 15), whose advantage is in decreasing unwanted coupling capacitances between differential outputs and inputs (described in the next chapter), does not change the gain as expected. The M4 and M5 NMOS cascode ensures operating point invariance of the M7 and M8 differential pair as the M12 and M13 PMOS cascode in previous configurations.

3.3.3. Bandgap Reference Improvements

Fig. 16 shows the circuit schematic of the proposed voltage reference. The circuit consists of the bandgap core (*R*1–*R*4, *C*1, *C*2, and Q1–Q3), a BJT anti-saturation circuit (M1–M3, M6, and M9), a part of bias circuits (MF–MH), and the asymmetrical OTA (*R*5, *C*3, *C*4, M4, M5, M7, M8, M10–M14 and MA–ME). A startup circuit was omitted for simplification.

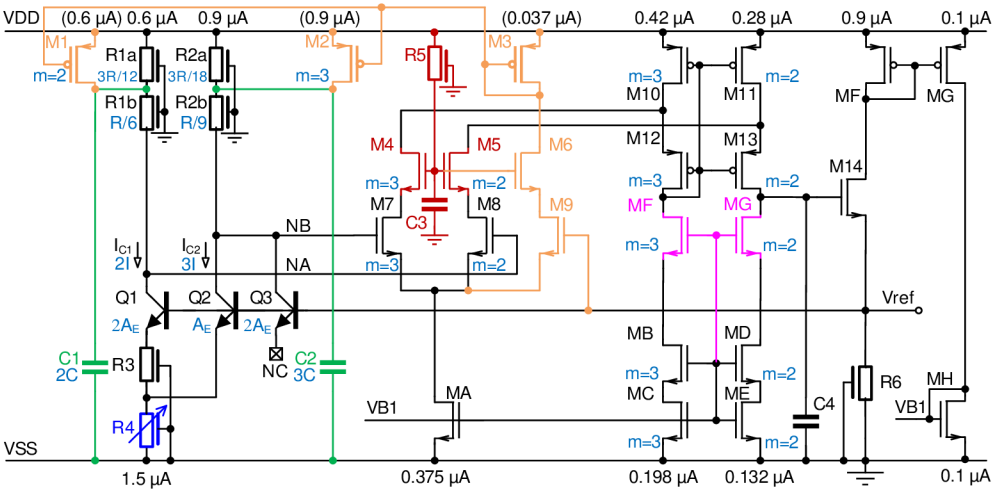


Fig. 16: Simplified circuit schematic of the new proposed bandgap.

The improvements of the voltage reference are discussed as follows. As shown in Fig. 16, *C*1 and *C*2 are used as additional filtration capacitors to minimize the coupling of the VDD supply EMI to the bandgap core. It is more effective to split the collector resistors into two parts and create a second-order filter than just connecting additional capacitors to the collectors. To lower the conversion of the common mode disturbances to differential OTA input signal, it is crucial to match well time constants between the two collector branches. *R*1a, *R*1b, *R*2a and *R*2b resistors together with *C*1, *C*2, C_{CQ1}, C_{CQ23}, C_{GM7} and C_{GM8} capacitors form two second order low-pass filters with time constants τ_{1a}, τ_{2a} and τ_{1b}, τ_{2b}. These time constants can be roughly estimated from node impedances by considering the validity that $C1 > (C_{CQ1} + C_{GM8})$ and $C2 > (C_{CQ23} + C_{GM7})$ as follows:

$$\tau_{1a} \approx R1a \cdot C1 = \frac{3}{12} \cdot R \cdot 2 \cdot C = \frac{1}{2} \cdot R \cdot C, \tag{16}$$

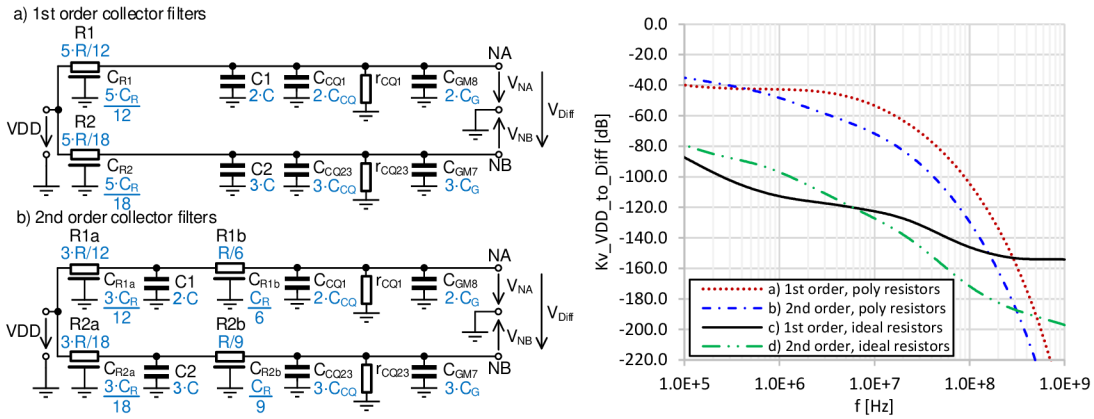
$$\tau_{2a} \approx R2a \cdot C2 = \frac{3}{18} \cdot R \cdot 3 \cdot C = \frac{1}{2} \cdot R \cdot C, \tag{17}$$

$$\tau_{1b} \approx R1b \cdot \left(C_{CQ1} + C_{GM8}\right) = \frac{1}{3} \cdot R \cdot \left(C_{CQ} + C_G\right), \text{and} \tag{18}$$

$$\tau_{2b} \approx R2b \cdot \left(C_{CQ23} + C_{GM7}\right) = \frac{1}{3} \cdot R \cdot \left(C_{CQ} + C_G\right). \tag{19}$$

Where C is a design unity capacity, C_{CQ} is an intrinsic unity capacity of the Q1 – Q3 BJT collectors and C_G is an intrinsic unity capacity of the M7 and M8 NMOS transistor gates. The design unity capacity was chosen in the order of a picofarad. To be able to well match the time constants the new asymmetrical OTA mentioned above was proposed. In [20] impact of the mismatch of these capacitances was neglected compared to the values of filtering capacitors. In the case of splitting sensing resistors and placing filtering capacitors between the split resistors, this matching is more important.

R1a – R2b are polysilicon resistors that are placed above a P-well diffusion. The diffusion is connected to the VSS ground, and therefore, the resistors have intrinsic capacitance to the ground. A simplified simulation circuit schematic with two types of collector filters was introduced in order to determine how resistor intrinsic capacitances C_{Rx} influence the matching of time constants and demonstrate the effectiveness of VDD decoupling by second-order filters. The schematic and achieved AC simulation results are shown in Fig. 17.



a) b)

Fig. 17: The a) simplified circuit schematic of collector filters and b) their common mode to differential voltage conversion.

The second-order filters with polysilicon resistors have a lower common mode to differential voltage conversion than the first-order filters in the frequency range from 1 MHz to 1 GHz, and the difference is around 20 dB. Note that this range is mostly used for EMI susceptibility tests. As a reference, filters with ideal resistors (without C_{Rx}) show low common mode to differential conversions impacted only by different BJT resistances r_{CQ1} and r_{CQ23}. It is evident from simulation results that the common mode conversion is negatively impacted by resistor intrinsic capacitances, which are opposite to the required capacity ratio. Within the same occupied area, the second-order filter gives higher common mode rejection.

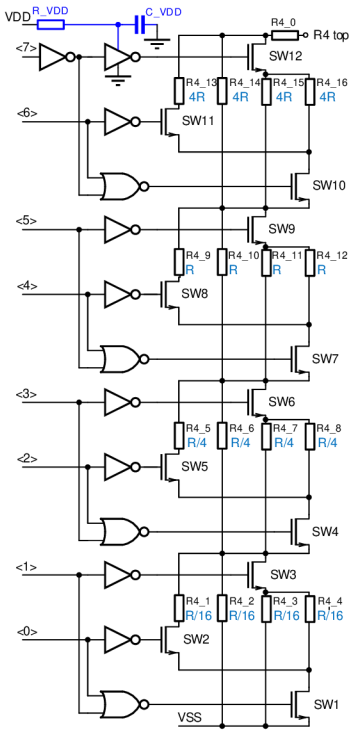


Fig. 18: A resistor *R*4 trimming circuit with filtered VDD supply.

The minimum supply voltage of the bandgap is 3.1 V, and the circuit was designed to work with only a 2.1 V supply to ensure good EMI robustness. By doing this, the circuit has the benefit of approximately 1 V margin for disturbances on VDD.

Voltage drop on *R*1 and *R*2 resistors was set to 0.9 V. For larger EMI levels, the bandgap core BJTs are pushed to unwanted saturation, which strongly influences the reference voltage. Therefore, a simple BJT anti-saturation circuit (M1–M3, M6, and M9 in Fig. 16) was added to maintain bandgap core BJTs in the linear region. This circuit consists of a detection transistor M9, which is cascoded by M6, and a forcing current mirror M1–M3. When BJTs collector to base voltage decreases close to 0 V, transistor M9 starts to conduct and delivers current to the forcing current mirror M1–M3. This current mirror decreases voltage drop on *R*1a and *R*1b and pulls up BJTs collectors as well.

The proposed bandgap employs digitally variable resistor *R*4 (Fig. 18) to trim the reference voltage due to process variations. An 8-bit trimming allows approx. 1 mV/LSB trimming step. Switched resistors are grouped into two-bit sections, and using special topology decreases requirements for switch resistances yielding a smaller layout area. A one-temperature trimming at 150 °C was used.

Because resistor *R*4 is in the emitter circuit of the bandgap core, there is a high sensitivity to disturbances coming from supply through digital gates and intrinsic capacities of trimming NMOS switches. Therefore, the trimming logic was supplied, which has almost zero static current consumption, by a first-order low-pass RC filter. In this design, the cutoff frequency of the filter is approximately 5 MHz.

3.3.4. EMI Susceptibility of the Bandgap Reference

To verify the proposed EMI susceptibility improvements, EMI simulations were performed with the following configurations of the overall bandgap, refer to Fig. 16:

a) Without EMI susceptibility improvements,

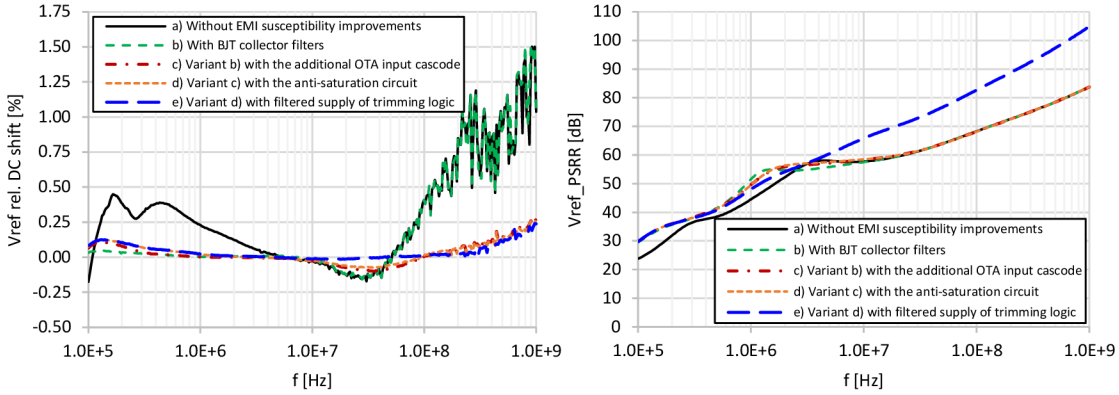
b) With BJT collector filters (*C*1 and *C*2 added),

c) Variant b) with the additional cascode of the differential input pair (*R*5, *C*3, M4, and M5 added),

d) Variant c) with the anti-saturation circuit (M1–M3, M6 and M9 added), and

e) Variant d) with the filtered supply of trimming logic.

The transient envelope analyses by the Cadence Spectre RF simulator for each bandgap configuration were performed. The 1 V amplitude EMC signal was superimposed on the supply voltage. Achieved results are shown in Fig. 19 a) and b).

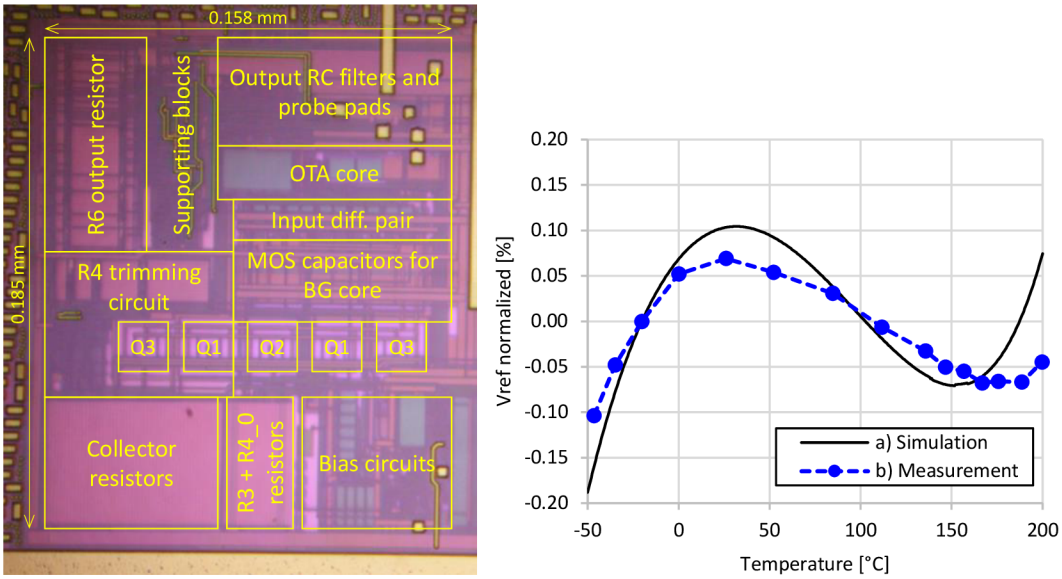


a) b)

Fig. 19: The a) relative DC voltage shifts and b) PSRRs of the new bandgap for 1 V peak EMI at VDD supply from transient simulation.

From these results, the added second-order collector filters show their essence in the lower frequency range from 100 kHz to 10 MHz. Further, the proposed additional cascode of the differential input pair reduces supply EMI susceptibility in the higher frequency range from approximately 50 MHz to 1 GHz. On the other hand, the susceptibility at the lower frequency range is slightly decreased, and the relative reference voltage shift is up to 0.1 %. The BJT anti-saturation circuit slightly decreases the susceptibility in the frequency range of around 50 MHz. This contributor is the smallest of all improvements at a given disturbance level, and it helps with higher disturbances. Finally, the filtering of the logic supply of *R*4 trimming shows a reduced susceptibility in the middle-frequency range from 10 MHz to 100 MHz. The simulation results prove that all presented EMI improvements help to decrease the susceptibility of the proposed bandgap.

The proposed bandgap voltage reference was realized in the onsemi 180 nm smart power BCD process as a part of a System on Chip (SoC). A die micro-photo of the realized voltage reference with the active silicon area of about 0.03 mm^2 and temperature dependency of measured and simulated reference voltages after trimming are shown in Fig. 20.



a) b)

Fig. 20: The a) die micro-photo and b) temperature characteristics after trimming.

For both simulation and measurement, the trimming code was firstly determined at a temperature of 150 °C by finding a target voltage of 1.215 V. Subsequently, the temperature sweep was performed, and the resulting output voltage was measured. The measured temperature coefficient of V_{ref} is about 7 ppm/°C. The simulation and measurement results are roughly correlating.

The susceptibility of the proposed bandgap was validated by the DPI method according to IEC 62132-4:2006 [3] in the frequency range from 100 kHz to 1 GHz. According to this method, a sinusoidal interfering signal with a known frequency and an average power was injected via an AC coupling capacitor to the VDD supply of the SoC since the output reference voltage was monitored by a DC voltmeter. The DPI test setup is shown in Fig. 21.

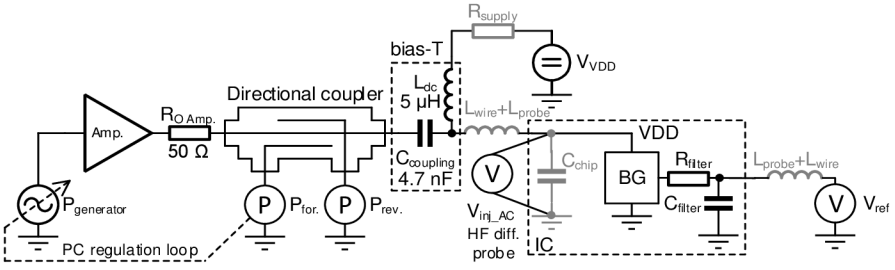
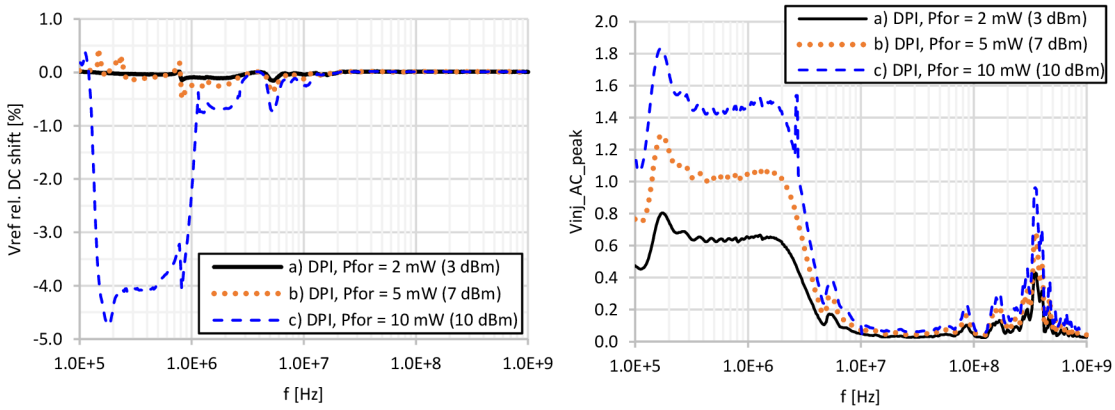


Fig. 21: The simplified circuit diagram of the DPI test setup.

This test setup does not have any external decoupling capacitor on the VDD supply to cover the worst case. For this case, there is native chip capacity C_{chip} with a value of about 10 nF as the VDD supply decoupling. The DC voltage supply source is isolated from AC by a choke L_{DC} which forms with the AC coupling capacitor $C_{coupling}$ a "bias-T" circuit. The parameters of this circuit were published in [5]. The DPI measurement results are shown in Fig. 22.



a) b)

Fig. 22: The DPI measurement results: a) V_{ref} relative DC shift and b) VDD AC voltage in the chip.

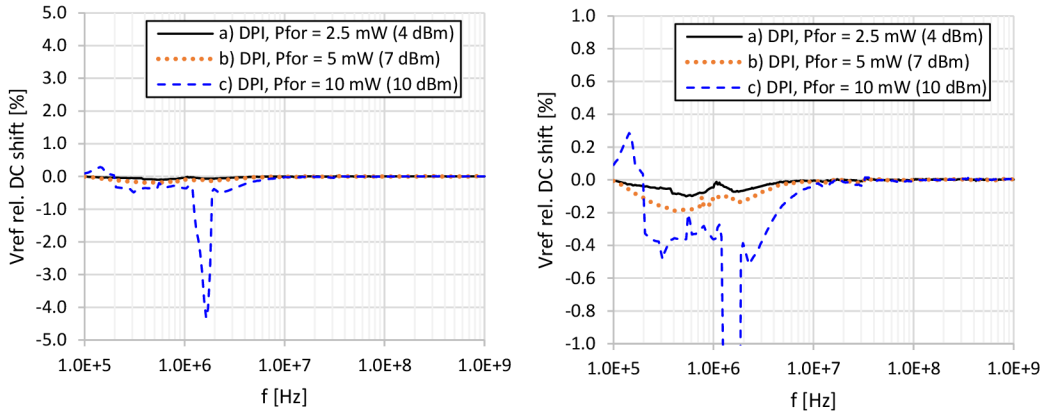
In the frequency range from 100 kHz to 1 GHz, the measured DC shifts are below 0.5 % for 5 mW (7 dBm) forward power. For the 10 mW (10 dBm), the maximum DC shift is lower than 5 % without damage of the bandgap. The high AC amplitudes of supply resonances create the peaks of DC shift. These resonances are caused by the "bias-T" circuit with coaxial wire and micro-probe inductances and the C_{chip} capacity. The internal resistor of the VDD voltage supply, R_{supply} in Fig. 21, partially dampens the resonances.

The DPI method involves a regulation loop of the average forward power using a personal computer (PC) with measurement software. The power meter measures the forward power through a directional coupler in this loop. The regulation loop behaves like negative feedback, which means that the amplifier output resistance, $R_{O\,Amp.}$ in Fig. 21, does not play a dominant role within the resonance damping. Therefore, more than one dominant resonance is seen in Fig. 22 b).

To measure the VDD voltage, a HF differential probe with 3 GHz bandwidth (Rohde & Schwarz RT-ZD30) was connected to a digital storage oscilloscope with 2 GHz bandwidth and 10 GSa/s sampling rate (Rohde & Schwarz RTO 1024). This voltage, marked as V_{inj_AC} in Fig. 21, was measured between microprobes connected to the internal VDD and GND of the IC.

The AC voltage in Fig. 22 b) shows the transmission of the "bias-T" filter and the attenuation caused by C_{chip} capacity, including resonances from parasitic circuit elements. The first dominant resonance is caused by the AC coupling capacitor and the inductance of the "bias-T" with the DC power supply. The other resonances are the results of the above-mentioned circuit interactions. An interesting dominant resonance occurs at 350 MHz. It is caused by inductances of coaxial wire and micro-probe with the input capacitance of the differential probe, which is less than 1 pF.

Fig. 23. shows the measurement results of the standard DPI to an external VDD pin of the test chip. This pin was added only for measurements and not used for normal functions.



a) Overview b) Detail

Fig. 23: The measurement results for DPI to external VDD pin via socket.

The internal supply is typically not connected to the external pin. However, the DPI measurements show a lower relative DC shift than previous tests. This effect is because the test chip was placed in a socket that has an inductance and capacitance in its wiring, and the external pin that attenuates the AC signal. Due to the different impedances in the DPI path, two effects are observed when comparing Fig. 23 a) to Fig. 22 a). Firstly, there is a higher AC attenuation (lower DC shift). Secondly, the dominant resonance has moved to a higher frequency according to the DC shift peaks.

In general, measured results show significantly lower supply EMI susceptibility of the proposed bandgap than other similar published bandgaps. The comparison of the bandgaps is in Tab. 4.

Tab. 4. Comparison of published Brokaw bandgaps with power supply EMI susceptibility measurements.

Reference	**[34]**	**[35]**	**[20]**	**This work, new BG**
Technology	0.7 µm	0.32 µm	0.35 µm	0.18 µm
Active area	0.160 mm^2	N/A	0.040 mm^2	0.029 mm^2
Supply voltage	3.0 V	3.3 V	3.0 V	3.1 V
Output voltage	1.170 V	1.247 V	1.205 V	1.215 V
Temperature range	-40 to 125 °C	-50 to 180 °C	-40 to 160 °C	-50 to 200 °C
Temperature coefficient	50 ppm/°C	3 ppm/°C	100 ppm/°C	7 ppm/°C
Current consumption	46 µA	50 µA	3.5 µA	3.2 µA
Power consumption	138 µW	165 µW	10.5 µW	9.9 µW
EMI DPI level	-13 dBm	-5 dBm	-3 dBm	7 dBm
V_{ref} rel. DC shift with DPI	max. 12.0 %	max. 7.8 %	max. 7.0 %	max. 0.5 %

Note that the output stage of the proposed bandgap is not designed for driving an external pin due to on-chip use only. Therefore, the output is connected to an output RC first-order low-pass filter (R_{filter} and C_{filter} in Fig. 21) with a cutoff frequency of 0.6 MHz. Then the filtered reference voltage is distributed around the overall chip, where each reference voltage input of IC blocks has an input RC low-pass filter. Since a very low EMI at the internal bandgap reference output is expected, the output EMI susceptibility of the proposed voltage reference was not analyzed.

3.3.5. Summary of Recommendations for Good EMC Design

This chapter summarizes recommendations for IC design with low EMI susceptibility. The simulation and measurement results from previous chapters demonstrate the validity of the EMC robust design methodology which consists of the following general recommendations. These can be summarized into four points:

a) Using a fully symmetrical and differential topology everywhere where it is possible for high CMRR and PSRR.

b) Keep all possible circuit nodes in a low impedance state at high frequencies.

c) Make symmetrical filtering of all differential signals and keep the same time constants.

d) Count with hidden structures of the IC.

Six more points based on the summarizing of this work can be added to these basic methodological recommendations, and these are:

e) Count with hidden impedance resonances, especially impedance serial resonances, which can create very high voltage ripple at an internal IC capacity.

f) Reduce AC coupling from supply to sensitive inputs or nodes by cascoding and/or filtrations.

g) Use perfect time constant matching for differential signals, e.g., OPA input capacities with respect to bandgap core outputs.

h) Consider sufficient voltage room for EMI disturbances and design the circuit to operate at a significantly lower supply voltage than the nominal one.

i) Consider supply filtration of logic circuits, which control switches in highly sensitive analog circuits.

j) Post-layout simulation of a complete block, e.g., the voltage reference for checking unwanted coupling effects.

The following steps are recommended to ensure that analog design is robust against EMI. Firstly, the relationship between the IC and its EMI environment needs to be understood. It is crucial to identify the location of interference, the affected IC pins, and the impact of the PCB on coupling. From the PCB perspective, conductive paths with external parts act as an antenna, which can receive EMI from the radio environment or local current loops. From the IC perspective, an internal impedance, such as distributed spread capacitances and resistances from other nodes, determines the unwanted signal propagation and its effect. The IC pin capacitance affects the propagation from the PCB to the IC.

The second step is to analyze the EMC properties of each system part. For the IC block, it can help to investigate factors such as voltage dc shift, PSRR, and CMRR. During this investigation, it is crucial to identify the most susceptible block of the entire circuit or system. High impedance and sensitive nodes can be found, which need to be improved by decreasing high-frequency impedance and increasing voltage or current static stability. After circuit modifications, the EMC properties should be rechecked to establish the impact of the changes.

For the PCB, a vital step is estimating an external impedance circuit model for the dedicated IC pin. The IC block connected to the pin with the model can be investigated for voltage dc shift, PSRR, and CMRR. Experiments such as moving unwanted resonances away by detuning from the frequency range of interest by changes of PCB and external parts can be considered. Finally, experimental simulations and measurements of the entire circuit are needed to verify the validity of all changes.

4 CONCLUSIONS

The EMC is a crucial performance measure for any electronic device, particularly in the automotive where high standards are required for new applications. Standardized compliance tests for EMC of the entire car are performed, but these tests are often too late for IC development. Identifying and solving EMC issues at an early stage reduces development costs and time to market. Therefore, it is vital to verify the EMC performance during the development of a new IC to ensure EMC robust circuit design and avoid the complexities that come with later detection of EMC issues.

This dissertation work focuses on techniques for designing more robust bandgap voltage references through EMC-resistant analog IC design. This work presents several recommendations for improving the EMI robustness of the voltage references. The EMI susceptibility simulations and measurements of two test chips were used to validate the effectiveness of these recommendations.

The first existing voltage reference, manufactured in 0.35 µm BCD process, has a current consumption of 3.5 µA and operates in a wide temperature range from -40 °C to 160 °C. It can withstand -3 dBm EMI DPI power coupled to the supply pin, and the maximum output DC voltage variation is 7 %.

The second proposed reference is manufactured in 0.18 µm BCD process and has a current consumption of 3.2 µA. It operates in a temperature range from -50 °C to 200 °C and can withstand 7 dBm DPI power to the internal supply line with a relative DC shift only below 0.5 %.

It is evident that the proposed new voltage reference has a lower current consumption, wide temperature range, and higher EMC robustness in comparison to the previous references discussed in Tab. 4. Additionally, the new EMC robust reference is capable of withstanding 10 dBm DPI RF power at the low voltage supply line without any damage and with a DC voltage deviation of up to 5 %. The validity of all recommendations and design methodology has been proven, and all dissertation aims have been successfully achieved.

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Abstract

A crucial component of modern integrated circuits is the voltage reference that acts like the heart for analog blocks providing stable voltage. This doctoral thesis explores advanced methods to reduce electromagnetic interference (EMI) susceptibility of low-power voltage references for an automotive environment with a wide temperature range. The EMI susceptibility is an unwanted phenomenon that can cause electronic system malfunctions. Electromagnetic disturbances can easily couple to the circuit via a cable harness and a printed circuit board. This thesis provides a literature overview, research suggestions, and results that focus on hidden effects in the voltage reference core, such as the impact of parasitic capacitance from bipolar transistors' collectors to the substrate and the effects of a used operational amplifier. Recommendations for improving voltage reference EMI robustness are presented and implemented. To prove the validity of the suggested improvements, test chips with proposed voltage references using various technologies were fabricated and measured.

Abstrakt

Klíčovou součástí moderních integrovaných obvodů je napěťová reference, která funguje jako srdce analogových bloků poskytující stabilní napětí. Tato disertační práce zkoumá pokročilé metody pro snížení citlivosti nízko příkonových referencí na elektromagnetické interference (EMI) pro automobilová prostředí s širokým teplotním rozsahem. Citlivost na EMI je nežádoucí jev, který může způsobit poruchy elektronického systému. Elektromagnetické rušení se může snadno vázat do obvodu prostřednictvím kabelového svazku a desky s plošnými spoji. Práce poskytuje přehled literatury, návrhy výzkumu a výsledky, které se zaměřují na skryté efekty v napěťovém referenčním jádru, jako je vliv parazitní kapacity z kolektorů bipolárních tranzistorů do substrátu integrovaného obvodu a efekty použitého operačního zesilovače. Jsou uvedena a implementována doporučení pro zlepšení EMI odolnosti napěťové reference. Aby se prokázala platnost navrhovaných vylepšení, byly vyrobeny a změřeny testovací čipy s navrženými napěťovými referencemi v různých technologiích.