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Faculty of Electrical Engineering
and Communication

BACHELOR'S THESIS

Brno, 2022 Gregor Karetka

BRNO UNIVERSITY OF TECHNOLOGY

VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ

FACULTY OF ELECTRICAL ENGINEERING AND COMMUNICATION

FAKULTA ELEKTROTECHNIKY
A KOMUNIKAČNÍCH TECHNOLOGIÍ

DEPARTMENT OF RADIO ELECTRONICS

ÚSTAV RADIOELEKTRONIKY

SDR BASED SHORTWAVE RECEIVER

KRÁTKOVLNNÝ PŘIJÍMAČ NA BÁZI SDR

BACHELOR'S THESIS
BAKALÁŘSKÁ PRÁCE

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VYSOKÉ UČENÍ TECHNICKÉ V BRNĚ
FAKULTA ELEKTROTECHNIKY A KOMUNIKAČNÍCH TECHNOLOGIÍ

Bakalářská práce

bakalářský studijní program **Elektronika a komunikační technologie**

Ústav radioelektroniky

Student: Gregor Karetka ***ID:*** 221053

Ročník: 3 ***Akademický rok:*** 2021/22

NÁZEV TÉMATU:

Krátkovlnný přijímač na bázi SDR

POKYNY PRO VYPRACOVÁNÍ:

Prostudujte aktuální druhy provozu používané na krátkých vlnách a jejich modulace. Zaměřte se hlavně na Digital Radio Mondiale – DRM. Zhodnoťte struktury softwarově definovaných přijímačů a nejvhodnější architekturu navrhněte pro platformu RedPitaya. Navrhněte a simulujte obvodové schéma. Výsledky simulací zhodnoťte. Pro přijímač zvolte vhodnou realizaci antény pro příjem na krátkých vlnách.
Pro navržený a simulovaný obvod navrhněte desku s plošnými spoji a tu realizujte. Změřte parametry realizovaného front-endu, porovnejte se simulacemi a případné rozdíly diskutujte a popište možné příčiny těchto rozdílů. Pro zvolenou modulaci navrhněte jednoduchý demodulátor, který implementujete do platformy RedPitaya a ověřte správnou funkci.

DOPORUČENÁ LITERATURA:

[1] XU, Yuanzhe, Dapeng TONG a Beiqiao JIANG. Hardware design of short wave radio based on Software Radio. In: 2018 IEEE 3rd Advanced Information Technology, Electronic and Automation Control Conference (IAEAC) [online]. IEEE, s. 2133-2136. DOI: 10.1109/IAEAC.2018.8577747. Dostupné z: https://ieeexplore.ieee.org/document/8577747/

[2] WILLCOX, Donald E., Joonwan KIM, Chris LOEWEN a John WINEMAN. Implementation of Digital Radio Mondiale receiver-part I. In: 2010 42nd Southeastern Symposium on System Theory (SSST 2010) [online]. IEEE, 2010, s. 56-59 . DOI: 10.1109/SSST.2010.5442862. Dostupné z: http://ieeexplore.ieee.org/document/5442862/

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Vedoucí práce: Ing. Miroslav Waldecker

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ABSTRACT

This thesis proposes shortwave radio receiver integrated as part of SDR. The objective is to design, simulate and implement RF front-end. Whole device is going to be stack-able on top of Red Pitaya which is capable of receiving DRM broadcast. Final design choice was to implement dual-conversion mixing as it presents advantages such as good image rejection, selectivity and being able to receive signals ranging from short waves up to very high frequencies. Thesis includes system design (schematics of individual blocks) and its simulations which were used to determine theoretical parameters (gain, sensitivity, SNR etc.). Important parameters were measured on assembled PCB. QPSK demodulator was implemented with Red Pitaya system using matlab [1].

KEYWORDS

Shortwave receiver, Digital Radio Mondiale, Analog front-end, Software defined radio, Red Pitaya

ABSTRAKT

Práca sa zaoberá krátkovlnným prijímačom založeným na báze SDR (softvérovo definované rádio). Cieľom je navrhnúť a simulovať analógový predstupeň krátkovlnného prijímača pripojeného do Red Pitaya, ktorý dokáže prijímať vysielanie služby DRM. Návrh využíva mixovanie s duálnou konverziou. Návrh obsahuje systémovú schému a schému navrhovaného zariadenia a realizáciu DPS, ktoré bolo simulované na systémovej úrovni pro určenie dôležitých parametrov (zisk, prenos, citlivosť, SNR, atď.). Následne bola realizovaná doska plošného spoja, ktorá bola osadená, a na ktorej boli vykonané merania. S pomocou Red Pitaya bol implementovaný QPSK demodulátor v matlabe [1].

KĽÚČOVÉ SLOVÁ

Krátkovlnný prijímač, Digital Radio Mondiale, Analogový predstupeň, Softvérovo definované rádio, Red Pitaya

ROZŠÍRENÝ ABSTRAKT

Vysielanie na krátkych vlnách vo vyspelom svete v posledných rokoch stráca na popularite. Platiaci používatelia prešli na vyššie frekvencie z dôvodu technických výhod, ktoré ponúkajú. Medzi hlavné výhody patrí použitie zložitejších modulácií, ktoré umožňujú vyššiu kvalitu zvuku a miniaturizácia, ktorá na vyšších kmitočtoch dovoľuje zmenšenie prijímačov, použitie nových výrobných technológií filtrov a zmenšenie antén. Hlavnou výhodou krátkych vĺn je možnosť odrazu od ionosféry, avšak, táto technika si dnes nájde uplatnenie hlavne medzi rádioamatérmi, keďže v dnešnej dobe je jednoduchšie a spoľahlivejšie na prenos na dlhé vzdialenosti využiť satelity. Aby toto spektrum bolo znova naplno využité, vznikli technológie ako DRM (Digital Radio Mondiale), ktoré na krátkych vlnách umožňuje digitálny prenos a s ním spojené výhody (vyššia kvalita zvuku, lepšie zabezpečenie proti chybám atď.). Táto práca sa zaoberá návrhom krátkovlnného prijímača (analógovým stupňom) na báze SDR a následnou implementáciou demodulátora. Ako SDR bola vybraná platforma Red Pitaya, ktorá bola použitá na vzorkovanie, obsluhu a ovládanie integrovaných obvodov na doske (signálové generátory) a následné digitálne spracovanie signálu. Návrh prijímača bol začatý analýzou požiadaviek na DRM prijímač dostupný v špecifikácií. Následne bolo nutné vybrať vhodnú architektúru prijímača, za ktorú bola zvolená architektúra s dvojitým zmiešavaním (dual-conversion), ktorá umožňuje prijímať široké frekvenčné spektrom, poskytuje dobrú selektivitu a dobre potlačuje signály na zrkadlových kmitočtoch. Keďže DRM sa dá prevádzkovať od stoviek kHz do stoviek MHz, vstup bol rozdelený na krátkovlnný a vysoko frekvenčný. Toto umožňuje použiť dve antény a medzi pásmami prepínať. Následne bolo zariadenie rozložené do niekoľkých modulov s rovnakou vstupnou a výstupnou impedanciou, 50 Ω pre jednoduchšie prispôsobenie. Medzi základné moduly patria: vstupné filtre, nízkošumové zosilňovače, automatické vyrovnávanie citlivosti, dva zmiešavače (na medzifrekvenciu a I/Q demodulátor), medzifrekvenčné filtre a signálne generátory. Jednotlivé moduly boli simulované na systémovej úrovni a následne boli pospájané do blokovej schémy, ktorá sa následne prekreslila do schémy programu KiCAD, z ktorej sa následne navrhla doska plošného spoju. Následne bola doska realizovaná na štvorvrstvovom substráte. Jednotlivé moduly boli merané a ich charakteristiky boli vynesené do grafov. Následne pozorované rozdiely boli komentované. Najväčší rozdiel bol v prenosovej charakteristike eliptického filtru použitého v medzifrekvenčnej časti. Táto odchýlka vznikla zanedbaním akosti kondenzátorov. Ostatné bloky vykazovali očakávané charakteristiky, ktoré boli v tolerancií so simuláciami. Následne bol implementovaný QPSK demodulátor v Matlabe.

KARETKA, Gregor. *SDR based Shortwave Receiver*. Brno: Brno University of Technology, Faculty of Electrical Engineering and Communication, Department of Radio Electronics, 2022, 68 p. Bachelor's Thesis. Advised by Ing. Miroslav Waldecker

Author's Declaration

Author:	Gregor Karetka
Author's ID:	221053
Paper type:	Bachelor's Thesis
Academic year:	2021/22
Topic:	SDR based Shortwave Receiver

I declare that I have written this paper independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the paper and listed in the comprehensive bibliography at the end of the paper.

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Introduction

In recent times commercial shortwave radio broadcasts popularity is on decline in developed countries. Listeners and broadcasters moved to higher frequencies because of advantages such as higher efficiency, more efficient modulations, miniaturization of antennas (possible on higher frequencies) and higher audio quality. With modern equipment (eg. smartphones, pocket radio receiver and car radios) it is now possible to receive broadcast with small antennas, high bitrate and very good audio quality. Skywave propagation, being one of the big advantages of shortwave radio, has been made obsolete by today's satellite technology. In developing countries, the situation is a bit different. Shortwave broadcast is still popular option today. It permits easy coverage of wide area and by using simple modulation technique like AM it can be received using simple cost effective equipment. Popularity of shortwave radios has been increasing in recent years due to rise of digital radios, using modern techniques/modulations like DRM (Digital Radio Mondiale). Digital radios use different digital modulations with new audio/speech compression/error correction algorithms and therefore deliver better audio quality and perform better in noisy environment. Advantages of digital systems are: increased number of channels, reduced radiated power, increased audio quality, increased noise protection. Shortwave radio for civilian sector is also applicable in emergency situation, during power outage, natural disasters and other scenarios during which other forms of communication may fail and for entertainment as digital radio. DRM present emergency warning system. Other users of shortwave bands include: military (over-the-horizon radars, communication etc.), HAM (amateur radio) operators, maritime long range communication (when not using satellites), air traffic long range communication (when not using satellites) and time signal and radio clock stations. Scope of this thesis is to design and implement RF front-end for SDR that would enable reception of DRM and DRM+ on all frequencies specified in documentation (bands: LF, MF, HF, VHF) in addition it must meet all requirements for DRM receiver with accordance to specifications. Device is designed as module that would sit on top of Red Pitaya (STEM^{lab} 125-14) development board. Red Pitaya contains SoC: FPGA + ARM that can be used to perform fast signal processing and Linux environment which can be used to control peripherals of the system (eg. PLLs, AGC/VGA, etc.). In order to be able to play received audio, board presents audio codec that is controllable by either FPGA or ARM [1].

1 Shortwave radio transmission

Frequency spectrum of shortwave radio is not firmly defined but generally it includes frequency bands: MF (medium frequency band) and of HF (high frequency band). Nowadays, its primary users are HAMs (amateur radio operators).

1.1 Types of modulation

Types of modulation used on shortwaves has been changing over course of the years. Types of modulation used on shortwaves nowadays range from simplest analog modulations like CW (constant wave) up to complex digital modulations like QAM (Quadrature amplitude modulation).

Constant wave (CW)

Constant wave (CW) modulation is one of the first and most simplest modulation ever used. Working principle of this modulation is based on "on off keying" of transmitted carrier frequency. Nowadays, this modulation is mainly used by HAMs.

Amplitude modulation (AM)

Amplitude modulation (AM) is still used today not only by HAMs and enthusiast all around the world but also by civilian maritime and air traffic control. Working principle of this modulation is based on modulating amplitude of carrier frequency by input signal (audio, speach, etc.) [4].

Single sideband (SSB)

Single sideband (SSB) is a form of amplitude modulation. Advantage of this modulation over amplitude modulation is less power consumption and narrower bandwidth. This is achieved by transmitting only one side of the band (upper sideband (USB), lower sideband (LSB)), which decreases bandwidth needed, and not transmitting carrier, which decreases power consumption. By removing carrier frequency we lose ability of demodulating the signal using simple detector circuit therefore radio receivers for SSB are more often more expensive [4].

Digital modulations

Digital modulations are gaining on popularity since they usually provide increase in data transmission at equal bandwidth compared to analog modulations. Focus

of this thesis is on DRM (and DRM+) which uses 64-QAM, 16-QAM and 4-QAM modulation based on error coding scheme [4], [11].

1.2 Digital Radio Mondiale (DRM)

Overview

Digital Radio Mondiale (DRM) is modern radio broadcasting protocol. Its main purpose is to replace traditional analog radio by using modern digital modulations and digital frequency multiplexing thus increasing number of channels and decreasing power required.

System specifications for DRM and DRM+ can be found in [12]. Digital Radio Mondiale uses orthogonal frequency division multiplexing (OFDM). This technique is based on multiple users sharing the same frequency slot. Each slot is orthogonal to neighboring slots thus they overlap with each other but since they are orthogonal to each other they do not interfere with each other thus more users can use the same bandwidth than when using regular FDM. One device can use multiple slots and sends its serial data over these slots in parallel in order to further increase bandwidth [2].

Modulations used by DRM are always digital MQAM modulations, where M parameter depends on selected error coding scheme and can be 4, 16 and 64.

Quadrature amplitude modulation (QAM) is combination of two digital modulations, PSK, which is responsible for phase keying and ASK which is responsible for amplitude keying. By combining these two modulations bandwidth can be increased since $\log_2 M$ bits can be coded as single symbol [12].

1.2.1 Receiver requirements

Frequency Bands

According to [11] the DRM receiver shall support at least one of the categories of Tab 1.1. It is recommended to support all frequency bands. The DRM receiver shall allow reception of DRM transmissions in frequency steps as defined in 1.1.

Additional steps may be provided for analogue reception, DRM receivers should be backward compatible with old analog modulations (AM). Result of this thesis, RF front-end, should be able to receive all frequencies specified in Tab 1.1. Resulting design is going to be software defined radio (SDR). This gives possibility of sampling wide frequency range and after that using digital down-conversion block and digital filters to further select desired radio channel or multiple channels. This gives a possibility of receiving multiple channels at once without change in RF front-end.

Tab. 1.1: DRM receiver frequency bands [11] Table 2 (2019, p.14)

Receiver category	Frequency range	Lowest center frequency
LF	148.5 to 283.5 kHz	153 kHz
MF	526.5 to 1 606.5 kHz	531 kHz
	525 to 1 715 kHz	530 kHz
HF 1	2.3 to 6.2 MHz	2.305 MHz
HF 2	6.2 to 27 MHz	6.205 MHz
Band I	47 to 68 MHz	47.05 MHz
Band II	76 to 108 MHz	76.05 MHz
Band III	174 to 240 MHz	174.05 MHz

Signal to Noise ratio (SNR)

According to [10] minimal SNR to achieve BER of 10^{-4} varies between different modes of robustness and even between different bands. Since scope of this thesis is receiver for whole DRM and DRM+ band, worst case scenario is selected. In Tab 1.2 are example values of SNR worst case reception. Cell in Tab 1.2 with red contains highest SNR. Since SNR values needed for good reception are at peak on Ch. mode 5 and robustness mode D at VF, this value dictates SNR we aim for. This value should be guaranteed at the input of digital demodulator for it to work properly [1].

Tab. 1.2: S/N (dB) to achieve BER of 1 x 10–4 for DRM robustness mode D with spectrum occupancy type 3 dependent with different protection levels and code rates [10] Table A1.7 (2008, p.72)

Modulation scheme	Protection level No.	Average code rate	Channel Model No. 3	4	5	6
16-QAM	0	0.5	18.5	16.9	15.3	16.0
	1	0.62	21.2	19.9	18.3	19.2
64-QAM	0	0.5	24.2	22.2	20.8	22.1
	1	0.6	26.3	24.5	22.9	25.2
	2	0.71	29.2	27.6	27.2	29.3
	3	0.78	32.1	31.7	35.5	32.5

Different channels represent different channel conditions (type of propagation, time of a day, etc.) . Fig 1.1 is the list of tested channels and their description. Source of these conditions is [10].

Fig. 1.1: Description of different channel conditions [10]

1. Model 1. propagation by ground wave during daytime on LF and MF frequencies
2. Model 2. wave propagation during night taking into consideration reflected sky wave on MF frequencies
3. Model 3, 4, 5, 6 represent channels with strong frequency selective behavior mainly suitable for HF.
4. Model 5. channels with fast-fading present
5. Model 6. channels affected by long path delay and Doppler spreads

2 System overview

In order to design an adequate RF front-end for the given task, it is necessary to perform system analysis. Every system is composed out of blocks performing different tasks that are chained together to convert incoming signals according to given rules (bands, bandwidth, SNR, sensitivity, etc.).

2.1 Red Pitaya (STEM^{lab} 125-14)

At the heart of the system, there is Red Pitaya (STEM^{lab} 125-14). This development board was selected because it contains Xilinx SoC (ARM MCU with FPGA) and high speed ADC with good resolution [14], [15].

I/O

Red Pitaya development board contains two connectors. One of them is dedicated to ARM special purpose drivers (SPI, I2C, UART, etc.), the other is dedicated to GPIOs. This way, devices using peripherals like SPI, I2C and UART can be controlled by ARM C code running in Linux environment instead of being synthesized onto FPGA, since it is necessary for signal processing [14], [15].

Powering RF front-end

Red Pitaya provides few power rails at two pin header connectors. These rails can provide up to 500 mA for rails +5V and +3V3. There is also -3V3 rail which only supports 50 mA. This has to be taken into consideration when selecting components and designing whole system, since it is not a lot [14], [15].

2.1.1 Analog-to-digital and digital-to-analog conversion

Analog-to-digital

Used ADC is LTC2145-14. Selected development board also contains 50 MHz low pass filter and amplifier. This filter serves as anti-aliasing filter to ensure Nyquist–Shannon sampling theorems condition is not violated.

LTC2154-14 is two channel, 14-bit, 125MSPS ADC with select-able input voltage range of 1 Vp-p or 2 Vp-p. It performs with 73.1 dB SNR and can be utilized for under-sampling because of low jitter. This high SNR is ideal for communication applications. Communication between FPGA and ADC is done using CMOS, DDR CMOS or LVDS standard [16].

Digital-to-analog

Red Pitaya is equipped with 2 channel 125MSPS DAC (AD9767). This device is not planned to be used in final application since its sampling rate is not high enough to be used as DDS or as LO of any of the mixing stages [15].

2.2 Radio receiver architecture selection

In today's high demand communication applications where frequencies of tens of GHz are utilized to carry wideband signals, receivers use mixing of RF signal with a fixed or tunable signal called LO to lower signals at frequency called IF, intermediate frequency. This is called heterodyne mixing when mixing once, or superheterodyne mixing, when mixing multiple times. This principle has been used for over a hundred years and is still used today.

Another widely used receiving scheme is direct conversion also called zero-IF conversion and a similar scheme called low-IF [1], [3].

2.2.1 Heterodyne receiver

Down-converting receiver

Heterodyne receiver consist of one or two mixing stages. Input signal called RF is then down-converted to lower frequency called IF, which is easily demodulated and then processed [3].

Dual-conversion receiver

In contrary to down-converting receiver, IF frequency of dual-conversion receiver is greater than that of RF. This scheme is utilized mainly due to filter size and high Q-factor of filters at higher frequencies. It is suitable mainly for wide band applications covering large frequency ranges (eg. hundreds of kHz up to hundreds of MHz). This scheme has been selected for this thesis [3].

2.2.2 Direct conversion

This receiver scheme has been very popular recently since ADCs sampling frequencies have increased significantly and it requires the least hardware. It is mostly used in low-demand applications. There are two types: Zero-IF and Low-IF each having its pros and cons. It may seem that these schemes are easier to implement than heterodyne receiver but it is not always the case [3].

Zero-IF

As the name implies this scheme is used to convert a spectrum of high frequencies directly to a spectrum around DC. This requires the least hardware but it has its drawbacks. The biggest disadvantage of the system is the possibility of LO leakage. Leakage of LO back to RF if not handled properly can produce unwanted radio emission at LO which can lead to the production of EMI and therefore lead to violation of EMC.

Leaked LO and RF carrier can cause LO self-mixing which results in DC at the output of mixer. This DC can be of large amplitudes and can easily saturate the next amplifier causing it to be less sensitive, lose dynamic range or become nonlinear causing whole device to underperform [3].

Low-IF

This receiver scheme addresses zero-IF self-mixing problem by down-converting high RF signals down to few kHz and not directly down to DC but this does not prevent LO leakage. A drawback to this scheme is requirement of ADC with higher sampling frequency making it more expensive [3].

2.2.3 I/Q Demodulation

IQ demodulator is a device that takes RF signal and LO as an input and produces two signals I and Q at the output which are 90° out of phase. Main purpose of IQ demodulator is to demodulate quadrature modulations (eg. BPSK, QPSK, QAM16, QAM64 etc.) since two output signals I and Q represent two modulated signals by transmitter with IQ modulator 2.1. Other properties of this device are used in SDRs. By using one IQ demodulator and two ADCs (preferably one ADC with two inputs so the samples are taken exactly at the same time) the bandwidth of whole system can be doubled as it can be seen in the Fig. 2.2. In this case IQ demodulator works as simple mixer down-converter. Since two signals I and Q are out of phase by 90° and are sampled at the same time each represent one part of the spectrum and the resulting bandwidth doubles because the two spectrums can be combined together. Usually both I and Q signals are low-pass filtered to eliminate higher order mixing products. This has many advantages such as using two ADCs with higher precision (dynamic range) and be able to sample at twice the bandwidth thus resulting in better performance and decrease in total cost of the device [4].

Fig. 2.1: I/Q modulator and demodulator transmitting and receiving QPSK signal

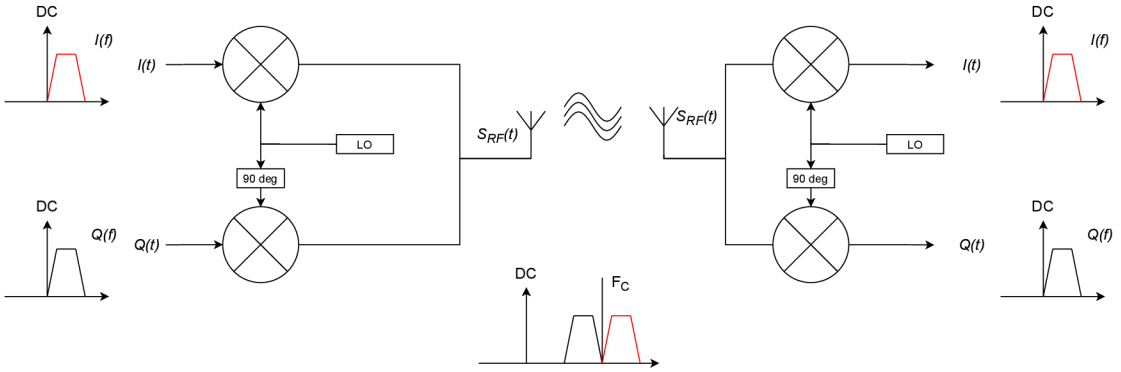
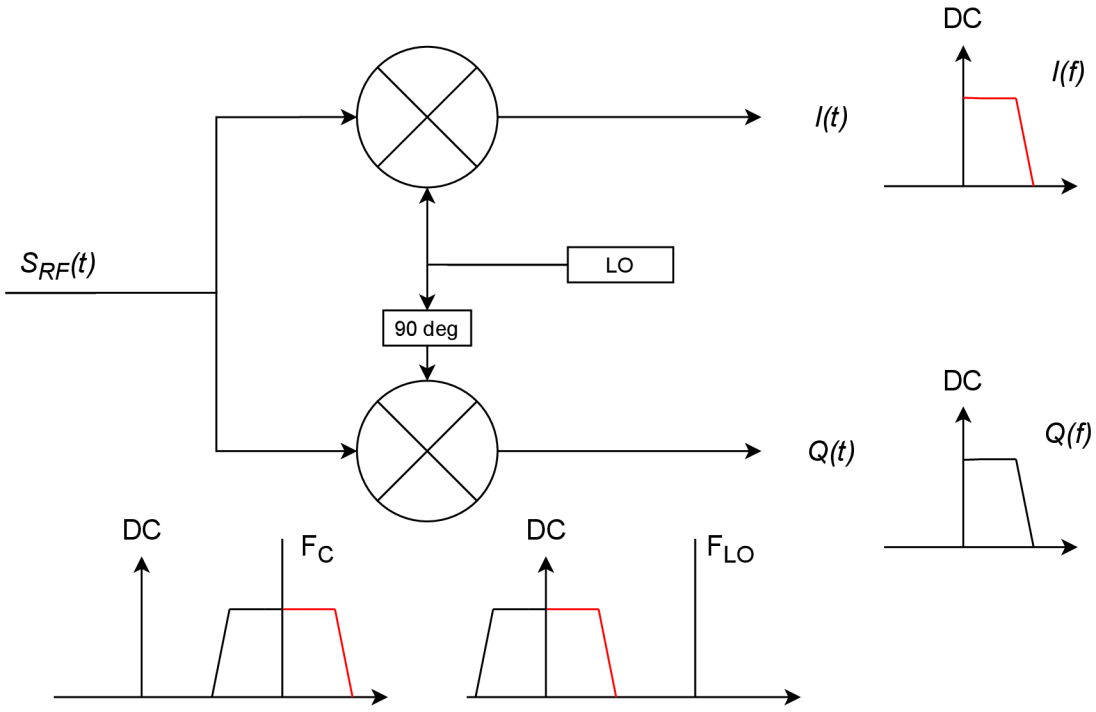


Fig. 2.2: I/Q Demodulator used in SDR to double bandwidth



2.3 Filters

Filters are one of the key component to every RF design used for filtering out unwanted signals. Filters can be realised using simple passive components (resistors, capacitors, inductors) but they can also contain active components (eg. Operational amplifier), the most notable being Sallen-Key active filter topology. In recent years many new principles and physical effects are being used for signal filtering. With the rise of digital era digital filter design, running filters digitally in DSP or FPGA, has grown in popularity. Nonetheless analog filtering is still valid today. In this thesis, multiple filtering stages with wide variety of manufacturing technology are need [4].

2.3.1 Input band pass filter - band selection

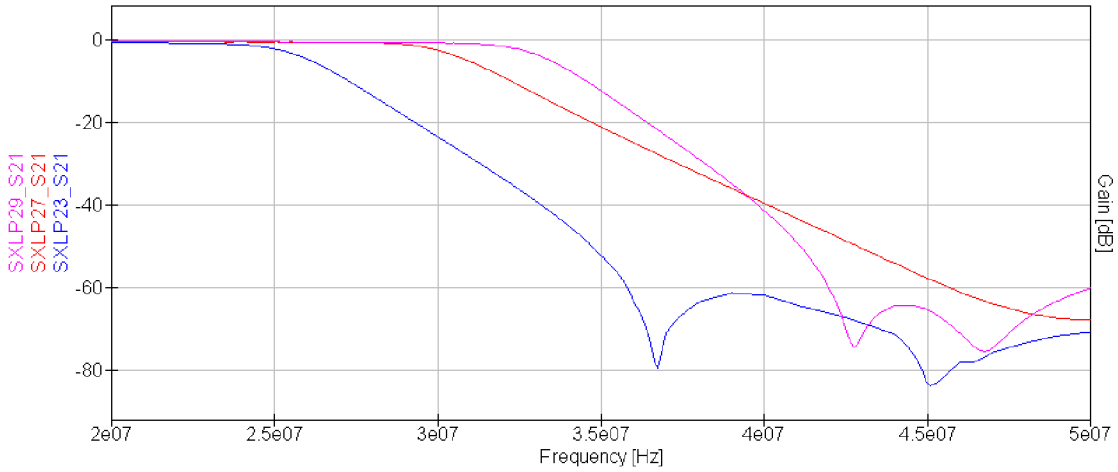
Considering real world antenna its bandwidth is not finite therefore band pass filter is required. The RF front-end presents two antenna ports with SMA connectors. Since input frequency spectrum is too wide for one antenna (from hundreds of kHz up to hundreds of MHz) two antenna system is implemented. Spectrum is divided into two ranges: SW (shortwave) ranging from 100 kHz up to 30 MHz; HF/VHF (very high frequency) ranging from 30 MHz up to 240 MHz, where single port is dedicated for each range.

SW input filter selection

Filter selection for low frequencies is not trivial since today many manufacturer specialize in making mm-wave products therefore combination of high pass filter made out of discrete components and lumped LC low-pass filter is used. As low pass filter, three monolithic LP filters from Mini-circuit are selected: SXLP-23+, SXLP-27+ and SXLP-29+. These filters have common characteristics but different cut-off frequency denoted by last two numbers (in MHz). Manufacturer provides S-parameter files for each of this filters for 3 different temperatures. Comparison between all three filters was done using QUCS simulator. From simulated data 2.3 it can be seen that the most suitable filter for this application is SXLP-27+ since its cut-off frequency is right around 30 MHz. One of the advantages of using filters from same manufacturer and same family of products is that the packages are the same and thus quick swap is very easy [17], [18], [19].

In order to block DC and lower frequencies high pass filter is needed. In order to simplify whole design process, this filter is designed out of discrete components. There are multiple ways of designing RF filters to name few: using tables and

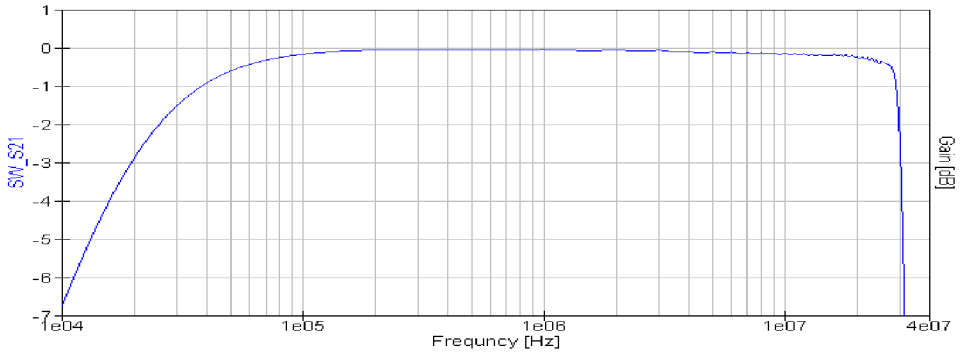
Fig. 2.3: Mini-circuit LP filter selection for SW, comparison by S21 parameter (Gain [dB])



synthesizing filters using transfer function. To ease the process of design, table method is selected. To even further ease the process, filter calculator [20] is used.

It generates schematic and s-parameter file usable in simulation. Since s-parameter file contains values only up to few MHz schematic file is used. Scheme of generated filter is then put in cascade with s-parameter file of SXLP-27+. The final filter with S21 characteristics 2.4 is created. It can be seen that pass-band is around 20kHz up to 30 MHz. Since this application does not require steep filtering at low frequencies, simple blocking capacitor is selected because other passive realizations require high value inductors thus making it impossible due to low self-resonance frequency.

Fig. 2.4: S21 [dB] characteristics of final filter. Combination of 1st order Butterworth high pass filter(simple DC blocking capacitor) with cut-off frequency at 20 kHz and input input and output of 50 Ω with SXLP-27+



HF/VHF input filter selection

Precise selection of specific bands may not be so trivial. Most of the time, this can not be solved by simply using pre-built filters thus filter cascade may be needed. Discrete components tend to have self-resonance in HF/VHF region, this has to be taken into consideration. In order to minimize this problem, monolithic components and discrete components with high resonance frequencies are preferred.

Once again, as for shortwave port, three monolithic filters are selected for comparison: LFCN-190+, SCLF-190+, SXLP-190+. 2.5 As final filter, SXLP-190+ is selected because it presents similar results compared to SCLP-190+ at lower price. Also SXLP series of filters presents multiple options in the same package with different cut-off frequencies so further change of components is trivial as swapping component for component.

Once again high pass filter made out of discrete components is synthesized [20] and put in cascade with SXLP-190+. The final characteristics is shown in 2.6 representing ideal components. In real world it is necessary to take into account real components characteristics. Two parallel ideal inductors in high pass filter were replaced two real inductors from Coilcraft: 0805CS-221 (VHF_real_0) and 0603HP-R22 (VHF_real_1). It can be clearly seen that real components do perform in different manner compared to ideal counterparts. The results of the simulation can be seen in 2.7 [21], [22], [23], [24], [25].

Fig. 2.5: Mini-circuit LP filter selection for HF/VHF, comparison by S21 parameter (Gain [dB])

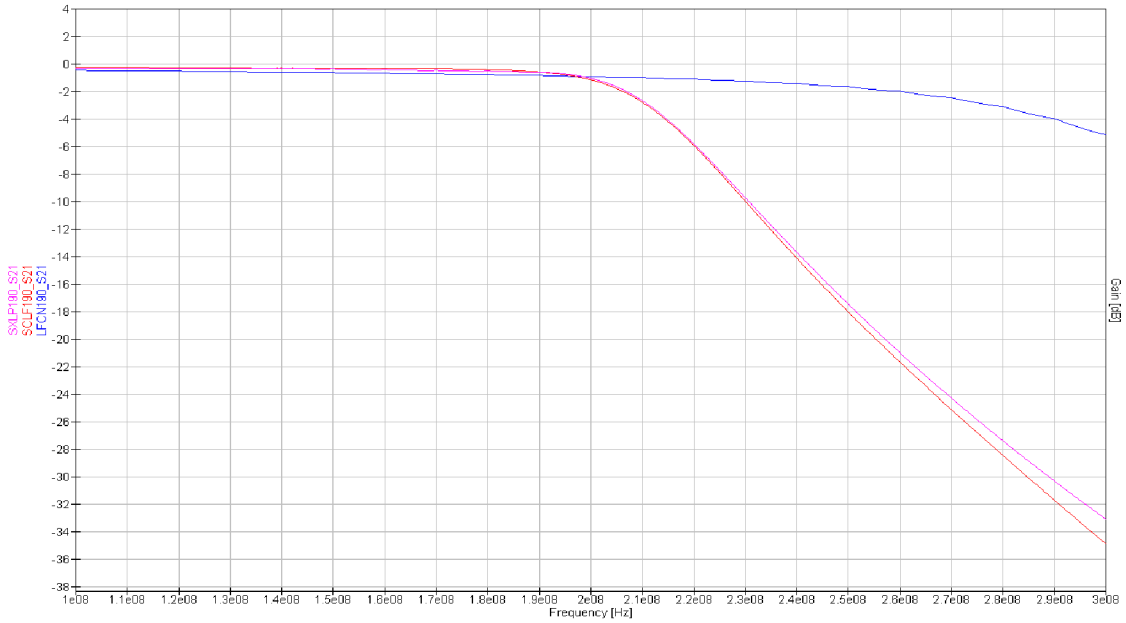
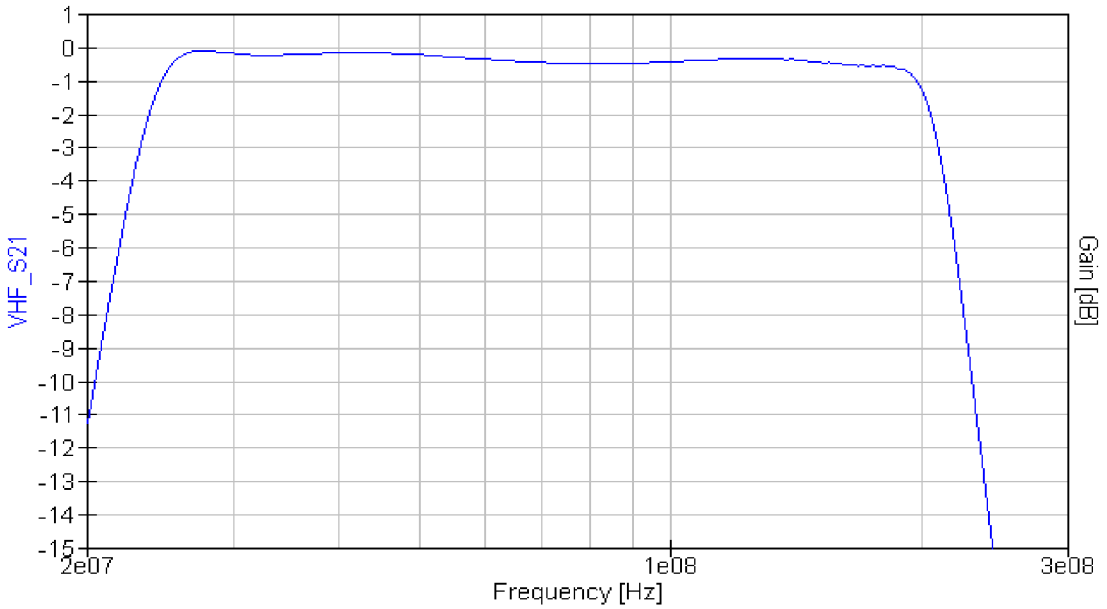


Fig. 2.6: S21 [dB] characteristics of ideal final filter. Combination of 5th order Chebyshev high pass filter with cut-off frequency at 25 MHz and input input and output of 50 Ω (**with ideal components**) with SXLP-190+



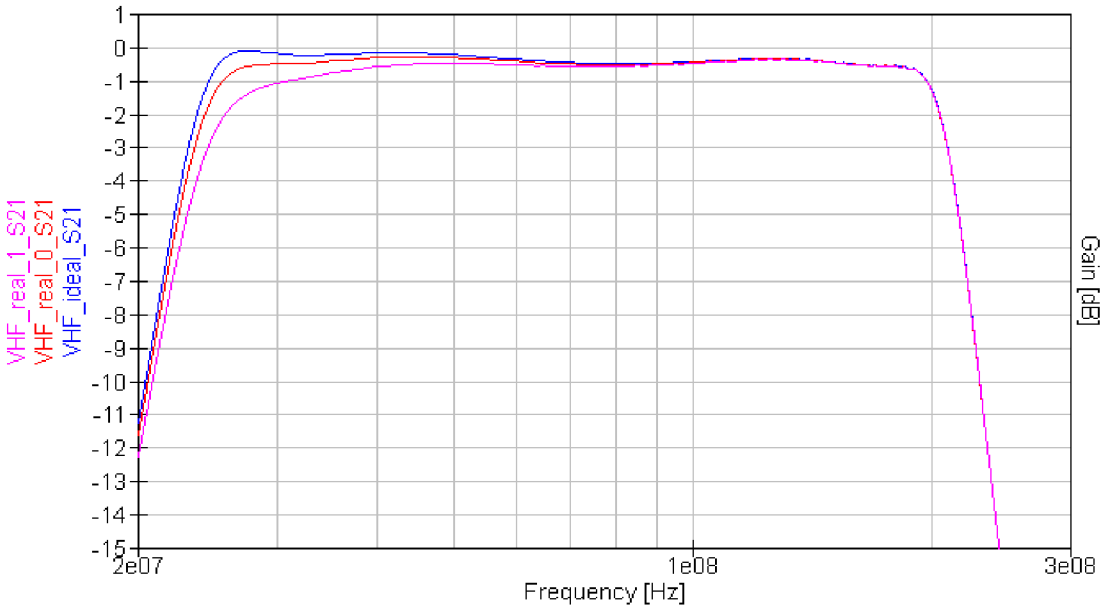
2.3.2 IF filters

To ensure aliasing does not happen and later stages are not saturated with unwanted signals, high Q band pass filter must be implemented at certain frequency span to select only desired bandwidth (in this case 100 MHz). In order to perform better in terms of noise, two filter configuration is selected. In this case, two different filters, one with full 100 MHz (or close to 100MHz) bandwidth and one with narrow bandwidth are put in parallel and IF signal of first mixer is passed through one of them at a time. With this configuration it can be selected to receive narrow band or wide band signals.

High Q maximal bandwidth filter

In this application wide band filter is used in order to maximize band coverage of whole device. Since two ADCs with 125MHz sampling rate are used, maximal bandwidth is set to 100 MHz. For this application three integrated filters are selected: BPF-C495+, CBP-670F+ and RBP-440+. After close evaluation none of them is suitable since the passband is too wide, too narrow or the device is too expensive. In this case 6th order elliptic bandpass filter out of discrete components is selected as ideal candidate for this role. As mentioned previously when designing filters, [20]

Fig. 2.7: S21 [dB] characteristics of ideal final filter. Combination of 5th order Chebyshev high pass filter with cut-off frequency at 25 MHz and input and output matched to 50 Ω (**with real components**) with SXLP-190+



is used to ease workflow. After this, finalized schematic is exported into LTSpice where S-parameter simulation is performed. Since inductors used in this design are of low value, self resonance occurs at high frequencies compared to selected pass band. Inductors selected have Q factor of 30 @ 100 MHz and tolerance of 5%. These parameters are incorporated in Monte Carlo simulation done in LTSPice with these results 2.8. By examining the result it can be seen that Q factor and component tolerances can play important role in selection of components and system design [26], [27], [28].

High Q narrow-band filter

In order to minimize noise generated by temperature and to improve selectivity it is necessary to reduce bandwidth. This can be deduced from simple equation

$$P_{Noise}\ [\mathrm{W}] = kT_sB \tag{2.1}$$

$$P_{Noise}\ [\mathrm{dBm}] = -174\ \mathrm{dBm} + 10\log(B) \tag{2.2}$$

where k is Boltzmann constant, T_s is temperature in Kelvin and B is bandwidth in Hertz. Therefore decreasing bandwidth, thermal noise decreases.

In similar manner to wideband, narrow-band filter is selected. When selecting this filter it is necessary to look for filters with similar center frequency to wide band filter. This helps in later steps when calculating frequency step for LO frequency synthesizers. The best and most suitable for this application is narrow band SAW or dielectric filter thus SF2136E is selected with 5MHz bandwidth. According to equations above, this decreases P_{Noise} from -95 dBm to -107 dBm thus decreasing noise floor by 12 dB 2.9 [13].

Fig. 2.9: S21 characteristics of SF2136E [13] SF2136E Frequency Response Plots (RFMI, 2021, p.2)

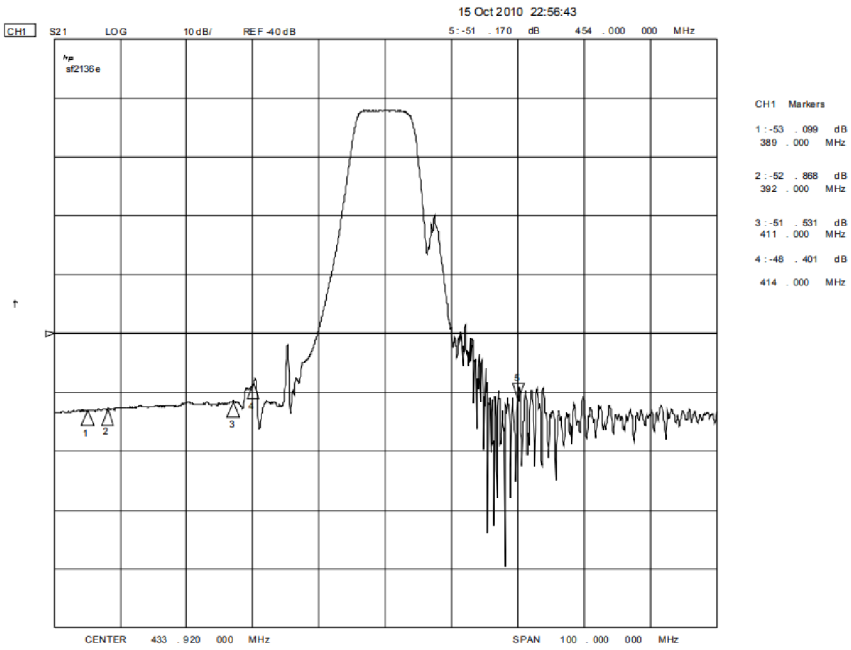
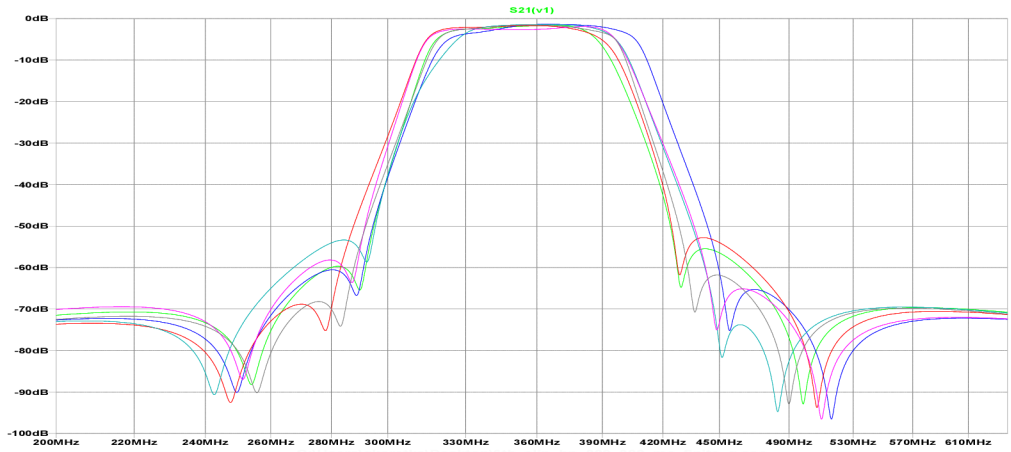


Fig. 2.8: Monte Carlo simulation of selected filter using 5% component tolerances and Q-factor of 30 @ 100MHz for coils



2.3.3 Anti aliasing filters

Two anti aliasing filters are implemented in Red Pitaya analog front-end. These two filters with cut-off frequency 50 MHz serve as anti-aliasing filters and suppress additional higher order harmonics.

2.3.4 Further digital filtering

In the heart of the system is fast FPGA which can be used as digital signal processor. Digital filters can be implemented for better selectivity and to reduce noise or signals of high amplitude that could corrupt demodulation [8].

2.3.5 Switching between different bands and filters

In order to switch RF signals, it is necessary to use proper RF switches with controlled impedance since basic relays and switches do not present constant impedance across wide frequency range.

For this task, HSWA2-30DR+ SPDT switch is selected for switching between different bands and as filter switch. Its working range is from DC (lowest frequency determined by AC coupling capacitor) up to 3GHz so it does not interfere with signals, the only problem is that it presents insertion loss of around 0.6 dB [29].

2.4 Amplifiers

In RF circuits amplifiers convert DC biasing power into AC power therefore increase input signal strength. This is needed in order to receive signals of low amplitude which decreases mainly due to distance between transmitter and receiver. Amplifiers can be optimized for several objectives: low noise, high gain or high output power. In this thesis few amplifier stages are needed. First, it is necessary to amplify incoming signal without adding too much noise and then it must be adjusted to not exceed point of 1dB compression. For the first task low noise amplifier is used and for the second task variable gain amplifier is used [3].

2.4.1 LNA - low noise amplifier

In order to minimize noise for both input ports two low noise amplifiers are integrated into the design one for SW and one for HF/VHF reception. This way noise factor for HF/VHF band can be improved.

In order to maximize SNR Friis relation (2.3) can be used to determine the best component order in the final chain

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + ... \tag{2.3}$$

where F is the final noise factor, F_n are individual noise factors of block in chain and G_n are individual gains of block in the chain, n determines index of the block in the chain. All variables are dimensionless. The chain can be represented by block with given F and G as shown in Fig. 2.10 [2].

Point of 1dB compression

Real world amplifier produce linear output power (relative to input power) only in a certain range therefore the gain is almost constant in this range. Point of 1dB compression is defined as point where real output power is 1dB under ideal linear characteristics and it defines maximum input power the amplifier can be fed to still work in linear range. It can be clearly seen in the Fig. 2.11 that by increasing P_{1dB} dynamic range and output power can be increased [5].

Output 3rd Order Intercept Point

All non-linear components can produce intermodulation products. Second order intermodulation products can be easily filtered out since they lay further away from desired frequencies. Third order intermodulation products are basically 3rd harmonics of input signal frequencies and mix of 2nd order intermodulation products and input signals therefore if the two signals of frequencies f_1 and f_2 mix with $2f_2$ and $2f_1$ four new signals appear in the final spectrum. Since $2f_2 + f_1$ and $2f_1 + f_2$ are further away they can be ignored since band pass filter can be utilized to eliminate them but two signals produced at $2f_2 - f_1$ and $2f_1 - f_2$ can not be filtered easily due to their presence near our desired signal.

The main concern with 3rd order intermodulation products is that for every dB of input power their output increases by 3 dB. Output 3rd order intercept point is the point where ideal gain of the amplifier intersects with gain of 3rd order intermodulation products. In the plot it can be represented similarly to Fig. 2.12, [3].

Therefore higher OIP3 is preferred.

Fig. 2.10: Example of an RF chain consisting of 4 block

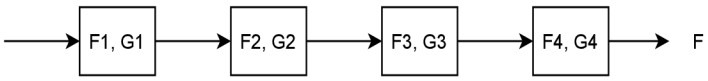


Fig. 2.11: Point of 1dB compression

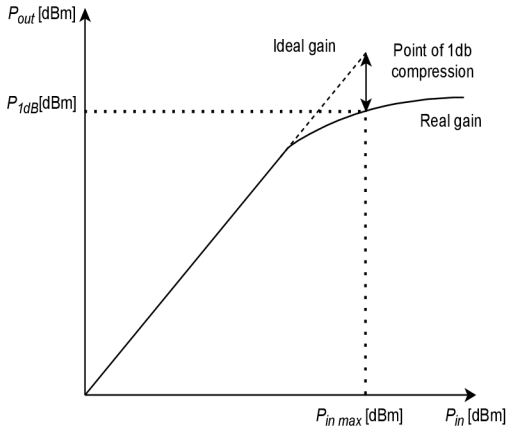
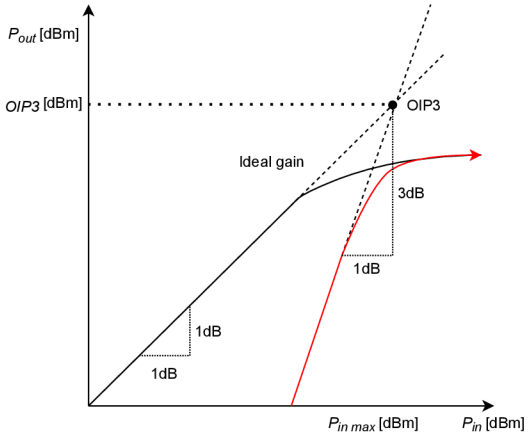


Fig. 2.12: Point of 3rd order intercept



Shortwave LNA selection

Since modern day RF equipment works primarily in mm-wave range it is not trivial to find dedicated shortwave LNA integrated into single package. Luckily Mini-circuits produces fair amount of LNA that work all the way down to DC. 2.2. In order to find suitable LNA, few things have to be taken into consideration: gain, noise factor, 1dB compression, IP3, supply voltage and current (power consumption).

Since power received by the antenna is fairly low, high gain of the amplifier is crucial but it is not the most important parameter. The most important parameter of LNA is noise factor (NF) which represents amount of noise added by the amplifier. It is defined as a difference between SNR_i (in dB) and SNR_o (in dB). In Tab 2.2 it is expressed in dB therefore for further calculation it must be converted into dimensionless variable. Since SW presents a low of unwanted noise from consumer electronics it is good to have high dynamic range. In this case it is mainly defined by P1dB since all other parameters are pretty much the same for all the amplifiers. High P1dB is necessary for good operation in SW range. Another important parameter, expressed by OIP3 in the table, is linearity. Greater difference between OIP3 and P1dB means better linearity. Since Red Pitaya can deliver only certain amount of current this has to be taken into consideration.

As a compromise between all the parameters PSA-39+ is selected as SW amplifier. It presents good gain, exceptional noise factor, good P1dB and good linearity. Lastly this amplifier draws about an average current from power source compared to other amplifiers and therefore it is suitable for this application [30].

Tab. 2.2: Listing of Mini-circuits amplifiers working down to DC up to few GHz

Model No.	Gain(dB)	NF(dB)	P1dB(dBm)	OIP3 (dBm)	V_{cc}(V)	I_{cc}(mA)
PSA-39+	23.0	2.2	10.7	23.3	5.0	32
LEE2-6+	18.9	2.3	2.8	17.6	3.6	16
MAR-6SM+	20.2	2.3	3.7	18.1	3.5	16
RAM-6A+	19.7	2.3	3.2	17.3	3.5	16
GALI-39+	19.7	2.4	9.0	22.9	3.5	35
GALI-S66+	18.2	2.4	3.3	19.1	3.5	16
LEE-39+	20.8	2.4	10.4	23.4	3.5	35
RAM-8A+	28.0	2.6	12.6	24.4	3.7	36
GALI-52+	17.8	2.7	15.5	32.0	4.4	50
GALI-74+	21.8	2.7	18.3	38.0	4.8	80
PSA-8A+	31.0	3.0	12.8	25.8	5.0	36

HF/VHF LNA selection

Selecting HF/VHF LNA is much easier than SW amplifier since this band is still highly used today. Few suitable amplifier are listed in Tab. 2.4. Once again the same steps as for selecting SW LNA are taken to select appropriate amplifier. As a compromise between all the parameters PHA-13LN+ is selected. It can work in two modes of operation: 5V and 3V nonetheless 5V mode is primarily selected even with its higher current draw due to significant parameter degradation in 3V mode. The detail comparison of difference between parameters can be views in Tab. 2.6, [31].

LNA position in RF chain

In order to determine the best order of two blocks it is necessary to calculate total noise factor by using Friis formula for noise. To determine noise factor of a filter it can be treated as attenuator whose noise factor F can be calculated (2.4)

$$F = 1 + (L - 1)\frac{T}{T_0} \tag{2.4}$$

where T is the temperature at which the noise factor is being evaluated in Kelvin, T_0 is 290 K and L is insertion loss. By examining Fig. 2.4 it can be seen that L in true pass band (100 kHz - 28 MHz) is around 0.1 dB (1.023 [-]) therefore by utilizing (2.4) and (2.3) at 25°C (298.15 K) with parameters of SW filter and amplifier as

Tab. 2.4: Listing of Mini-circuits amplifiers working down to 1 MHz up to few GHz

Model No.	Gain(dB)	NF(dB)	P1dB(dBm)	OIP3 (dBm)	V_{cc}(V)	I_{cc}(mA)
TSS-13LN+	22.8	1.1	24.5	39.2	5/3	142/72
TSS-13HLN+	23.0	1.4	28.4	42.9	8	234
PHA-13LN+	22.4	1.0	24.5	39.0	5.0/3.0	138/71
PHA-13HLN+	22.7	1.1	28.7	43.0	8	234
LHA-13LN+	22.4	1.1	23.3	38.3	5/3	143/73
LHA-13HLN+	22.7	1.2	28.0	43.3	8	239

dimensionless variables

$$F_{filt} = 1 + (1.023 - 1)\frac{298.15}{290} = 1.024\ [-]$$
$$F_{amp-filt} = F_{amp} + \frac{F_{filt} - 1}{G_{amp}} = 1.66 + \frac{1.024 - 1}{199.53} = 1.66\ [-]$$
$$F_{filt-amp} = F_{filt} + \frac{F_{amp} - 1}{G_{filt}} = 1.023 + \frac{1.66 - 1}{0.9775} = 1.70\ [-]$$

the noise factor for RF chain consisting of amplifier and filter is therefore better in terms of noise than that of filter and amplifier.

The same calculation can be done to determine order of block for HF/VHF stage. This time Fig. 2.7 and 2.6 is used to feed equations therefore L in pass (25MHz - 200MHz) band ranging between 3dB (1.995) and 0.5 dB (1.1220). Worst case scenario values are used

$$F_{filt} = 1 + (1.995 - 1)\frac{298.15}{290} = 2.023\ [-]$$
$$F_{amp-filt} = F_{amp} + \frac{F_{filt} - 1}{G_{amp}} = 1.259 + \frac{1.995 - 1}{199.53} = 1.26\ [-]$$
$$F_{filt-amp} = F_{filt} + \frac{F_{amp} - 1}{G_{filt}} = 1.995 + \frac{1.259 - 1}{1.995} = 2.12\ [-]$$

but still the noise factor for RF chain consisting of amplifier and filter is better in terms of noise than that of filter and amplifier.

2.4.2 AGC - Automatic gain control

In order to maintain constant level of input power at RF port of first mixing stage AGC needs to be implemented. This way it also helps to increase dynamic range of the system. Usually AGC is implemented in IF section of receiver but since mixer used in first stage requires relatively high input power in order to work properly AGC is implemented in RF portion of the receiver otherwise the mixer would limit the dynamic range.

Tab. 2.6: Comparison of parameters with highest deviation between different modes of operation for LNA by Mini-Circuits: PHA-13LN+ [31]

Parameter	F (MHz)	V_{cc}=5	V_{cc}=3V	ΔParam	Units
Output P1dB compression	1	21.3	15.1	6.2	dBm
	20	23.0	16.9	6.1	
	250	24.4	19.5	4.9	
Output IP3	1	37.0	30.6	6.4	dBm
	20	40.2	33.3	6.9	
	250	40.2	33.4	6.8	

AGC can be implemented digitally where DSP processes the input signal and adjusts the gain of AGC. The other possibility is to implement analog level detector that adjusts the gain of AGC. In this thesis AD8368 is used since it is VGA with integrated analog AGC detector but can also be overrode by driving one of the gain pins. In order to simplify the design analog AGC detector is preferred but it can be overrode in case it would be a bottleneck to the final application [2], [32].

2.5 Mixing

Mixing is essential part of almost every radio receiver. As mentioned in 2.2.1 heterodyne receiver uses mixers to shift spectrum of desired band up or down in order to simplify reception. As previously mentioned in 2.2.1 double conversion receiver scheme is selected for RF front end of this thesis.

2.5.1 Double conversion receiver

Double conversions biggest advantage is in distance between upconverted spectrum and image spectrum thus increasing image rejection. It also enables simple filtering as at higher IF filters can be easily integrated into one single package. Modern filtering technologies like ceramic resonators, SAW filters and distributed-element filter are huge benefit of double conversion scheme. Another benefit of higher frequencies is that smaller component values, thus smaller components, can be used in building filters from discrete components even though it is not very practical in GHz range. Another big advantage is possibility of multiple filters with different bandwidth but same or similar center frequency this property is exploited in this thesis as well [3].

First mixing stage - upconverter

First mixing stage consists of LT5560 double balanced mixer. Since it is used in the first stage of double conversion receiver it is used as upconverting mixer. In combination with filters mentioned in 2.3.2 any spectrum can be selected in order to be process it in later stages. This is shown in Fig. 2.13. Filters remove unwanted signals and leave us with only single 100 MHz band for further processing [33].

Mixers usually have two inputs (RF and LO) and one output (IF). Local oscillator is signal with which mixer "mixes" RF input signal in order to produce IF. The resulting frequency of IF is defined as

$$F_{IF} = m \cdot F_{RF} + n \cdot F_{LO} \tag{2.5}$$

where m and n are integers therefore can be of negative sign [4], [6].

Mixers can be of different types. The most common type and the type that is used in this thesis is called double balanced mixer. Its main advantages include: good linearity, suppression of unwanted products of LO and RF and better isolation between ports. Biggest disadvantage of such mixer is that it requires at least one balun at RF and possibly second at IF. Also due to more complex internal structure than unbalanced mixer it requires more power at LO [6].

Second mixing stage - I/Q demodulator

In order to bring upconverted signal down to baseband and maintain whole bandwidth of 100 MHz it is necessary to mix input signal with two signals with phase difference of 90° thus I/Q demodulator is selected for this task.

Fig. 2.13: Example of upconverting and filtering using BP filter

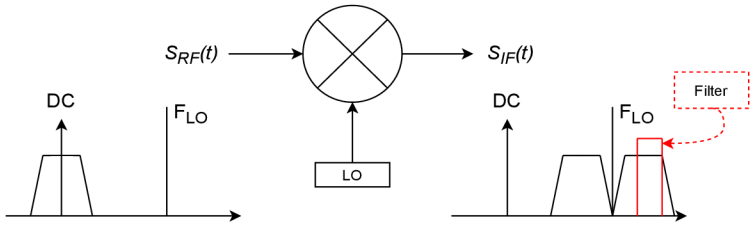
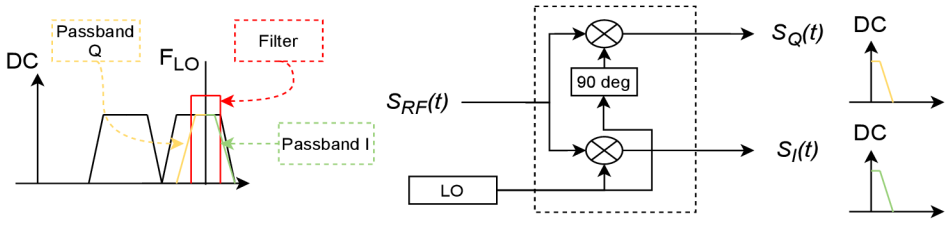


Fig. 2.14: Example of downconversion of upconverted signal with band pass filter



Since outputs of I/Q demodulator are directly connected to inputs of Red Pitaya it is essential for I/Q demodulator to be able to provide power up to 10 dBm at 50 Ω to ensure whole range of ADC is used. In addition LNA (TSY-13LNB+) is placed before I/Q demodulator in order to increase power at the mixer input. Since powering solely from Red Pitaya is preferred it is necessary to look at I/Q demodulators that consume little power but still maintain capability of driving ADC in the full range. These devices usually consume a lot of power due to presence of two amplifiers at the output otherwise low point of 1dB compression is achieved. Devices that fit these parameters from Analog Devices are listed and out of them the best fit for this thesis is ADL5387 since it possess P1dB of 17.4 dBm at desired frequency range so it can be connected directly to input of ADC without any additional amplification and the current consumption is also decent. The only downside of this I/Q demodulator is that it uses frequency divider at LO input by 2 thus LO input frequencies needs to be 2x center frequency of selected filters (thus $355 \cdot 2$ MHz and $433 \cdot 2$ MHz) but selected frequency synthesizer in 2.5.2 is able to deliver both. Working principle is shown at Fig. 2.14.

Digital downconversion

In order to receive data from signal of 100 MHz bandwidth at I/Q output it is necessary to perform digital downconversion. This process digitally moves spectrum of signal to lower band. It can be also combined with demodulation. Since the bandwidth is 100 MHz it can cover whole SW or FM spectrum thus by increasing instances of DDC (digital donwconverters) more channels can be decoded (theoretically all channels) [7].

2.5.2 Local oscillator generator

Local oscillator generator is device that is designed to produce LO signal for mixer. LO drive level is usually specified in mixer specifications. For LT5560 the LO drive level is specified to be between -10 dBm and 0 dBm. With higher drive level noise floor decreases, gain increases and around -2 dBm to 0 dBm it stabilizes. In order to properly drive this circuit frequency synthesizer is selected [33].

Frequency Synthesizer

As LO generator for LT5560 and ADL5387 ADF4351 programmable synthesizer is selected. Since the output of ADF4351 can drive LO with drive level of -4 dBm to 5 dBm of drive level and therefore satisfy LT5560 and ADL5387. It can produce

frequencies in range of 35 MHz up to 4400 MHz. It incorporates fractional-N PLL which gives possibility to adjust LO frequencies with very fine tuning.

I/Q demodulator, ADL5387, requires only two frequency selection since it demodulates signals that are present inside passband of IF bandpass filter. The desired LO frequency according to Fig. 2.14 is in the center of bandpass filter. Since two filters are used with center frequency of 355 MHz and 433.92 MHz these two frequencies need to be tunable. To determine register values following equations found in [34] can be used. First equation is use used to determine f_{PFD} since it affect loop filter design and does not affect frequency step

$$f_{PFD} = REF_{IN}\frac{1+D}{R(1+T)} \tag{2.6}$$

where f_{PFD} is frequency at the PFD (Phase-frequency detector) output, REF_{IN} is reference frequency (in this case 25 MHz), D is REF_{IN} doubler bit (left 0), R is reference division factor (left at default 1) and T is the reference divide-by-2 (left at 0). After inputting default values and values derived from other components the resulting f_{PFD} is 25 MHz. After that it can be later used in calculating other register values

$$RF_{OUT} = N\frac{f_{PFD}}{RF_{Divider}} \tag{2.7}$$

$$N = INT + \frac{FRAC}{MOD} \tag{2.8}$$

In order to simplify these calculations expression in (2.7) containing INT, $FRAC$ and MOD is replaced with N. The value of N is then calculated and separated into its components (INT, $FRAC$ and MOD). Therefor to calculate N for given RF_{OUT}, in this case 433.92 MHz, it is best to start with selecting $RF_{Divider}$ since it can be of few discrete values (1, 2, 4, ..., 64) and then proceeding with N. In this case $RF_{Divider}$ is set to 8

$$N = RF_{Divider}\frac{RF_{OUT}}{f_{PFD}} = 8\frac{433.92MHz}{25MHz} = 138.8544[-] \tag{2.9}$$

Looking at the result the whole part of N is equal to INT so $INT = 138$ leaving us with 0.8544 for the decimal part that is composed out of two numbers $FRAC$ and MOD which can be rewritten as following

$$0.8544 = \frac{FRAC}{MOD} = \frac{8544}{10000} = \frac{534}{625} \tag{2.10}$$

therefore $FRAC = 534$ and $MOD = 625$. Both numbers satisfy size of their registers. If this was not the case $RF_{Divider}$ can be increased/decreased but sometimes some values are not achievable. For faster calculation Analog Devices provides register calculator for their frequency synthesizers with simple interface [34], [35].

Lock Loop Filter

In order to design decent filter with good properties Analog Devices provides software [36] and [37] for easier setup. Here it is possible to select from variety of filter types each having its pros and cons in terms of filtering, lock speed and complexity. This program is able to generate whole schematic with all necessary components. Filter for down converting mixer LO was selected to provide lowest jitter. For up converting mixer fast locking speed is key factor for filter selection. Also filter at port MUXOUT (pin that can be used to monitor locking) is present [34].

2.6 Antenna selection

Since focus of this thesis is on wideband receiver with accordance to DRM specifications input is separated into SW port (100 kHz - 30 MHz) and HF/VHF port since it is not easy to build antenna for frequencies in range of multiple decades (eg. 100 kHz up to 240 MHz).

2.6.1 SW antenna

For SW antenna WiNRADiO AX-81SM Active LF-HF Antenna is selected since it operates in range of 20 kHz up to 30 MHz as this is one of few valid options. Since this is an active antenna it requires biasing. According to [38] it requires current of 80 mA at 12 V. As mentioned [38] it can be powered by WiNRADiO SF-41 Low-noise Linear Power Supply together with the WiNRADiO WR-BT-650 Power Injector.

2.6.2 HF/VHF antenna

For HF/VHF there are multiple options from different manufacturers. Antenna AD-39/3512 from Trival Antene is selected since it presents consistent gain across whole spectrum. It is passive antenna thus it does not require any powering.

2.6.3 LNA input protection

In order to prevent LNA saturation with signals out of desired band low pass filter LFCG-400+ is used at the input of each of the two ports. In order to protect against fast transients TPD1E0B04 is implemented right at antenna input. It is TVS (transient voltage suppressor) from Texas Instruments with relatively low capacitance with regards to frequencies of concern [39] therefore it does not interfere with signals.

This simple circuitry should handle most of unwanted interference and transient voltage spikes or other ESD bursts up to level 4.

2.7 Audio Codec

In order to be able to listen to demodulated audio output audio codec is required. Since Red Pitaya does not present dedicated I2S bus for communication with audio systems it must be programmed into FPGA later. This is also opens possibility of further digital filtering of audio in FPGA thus not overloading CPU.

For this task SSM2604CPZ from analog devices is selected as it presents stereo audio output, requires low power input and is relatively inexpensive [43].

2.8 Connecting Red Pitaya to Analog front-end

In order to control analog front-end from application running on Red Pitaya some pins of E2 and E1 connector of RP are used. For controlling devices via SPI and I2C interface ARM processor is used since it already presents I2C and SPI hardware blocks therefore I2C and SPI packets can be send using simple C code. On the other hand I2S interface must be implemented on FPGA side since this allows audio stream to be demodulated and sent directly to audio codec. This can be viewed in final schematic Fig. A.3.

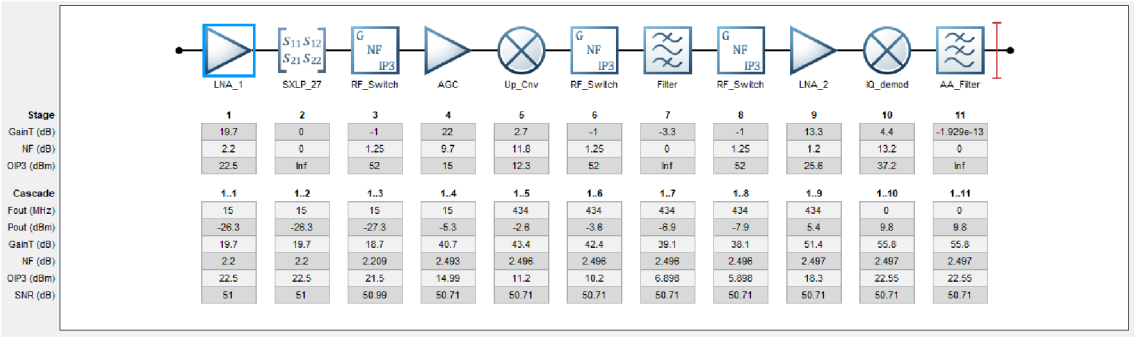
2.9 System parameters

In order to be able to compare the final device and industry standard devices few parameters need to be determined. In this thesis theoretical parameters of this device are presented and compared with few selected devices.

2.9.1 System Gain and SNR

The system is composed out of two paths the SW (shortwave) and HF/VHF (High frequency/Very High Frequency) path. The receiver can listen only to one path at a time therefore this parameter is calculated for both paths in Fig. 2.15. In order to determine parameters for both signal paths (SW and HF/VHF it is necessary to perform system simulation. Both simulations are calculated for input signal of -46 dBm and respective frequency bands. Bandwidth of these signals is limited by input filter. For SW band it is 100 kHz to 30 MHz. In order to simplify calculations, bandwidth is set to $BW = 30$ MHz. Bandwidth of HF/VHF path is ranging from 30 MHz up to 200 MHz therefore, bandwidth is set to $BW = 170$ MHz.

Fig. 2.15: Example of cascade gain/noise simulation of whole device for SW [1]



Stage	1	2	3	4	5	6	7	8	9	10	11
GainT (dB)	19.7	0	-1	22	2.7	-1	-3.3	-1	13.3	4.4	-1.929e-13
NF (dB)	2.2	0	1.25	9.7	11.8	1.25	0	1.25	1.2	13.2	0
OIP3 (dBm)	22.5	Inf	52	15	12.3	52	Inf	52	25.8	37.2	Inf

Cascade	1..1	1..2	1..3	1..4	1..5	1..6	1..7	1..8	1..9	1..10	1..11
Fout (MHz)	15	15	15	15	434	434	434	434	434	0	0
Pout (dBm)	-26.3	-26.3	-27.3	-5.3	-2.8	-3.8	-8.9	-7.9	5.4	9.8	9.8
GainT (dB)	19.7	19.7	18.7	40.7	43.4	42.4	39.1	38.1	51.4	55.8	55.8
NF (dB)	2.2	2.2	2.209	2.493	2.496	2.496	2.496	2.496	2.497	2.497	2.497
OIP3 (dBm)	22.5	22.5	21.5	14.99	11.2	10.2	6.898	5.898	18.3	22.55	22.55
SNR (dB)	51	51	50.99	50.71	50.71	50.71	50.71	50.71	50.71	50.71	50.71

In this scenario whole dynamic range of ADC is used (10 dBm/2 V_{p-p} at 50 Ω) at the output of AA filter). This simulation provides also information about minimal sensitivity of individual signal paths. SW signal path sensitivity is determined to -96 dBm (11 dBuV) and sensitivity of -87 dBm (20 dBuV) is determined for HF/VHF path. By increasing input power also SNR increases. If higher sensitivity is required, additional amplifier or narrow band filter is required.

If there is strong signal present on the input bandstop filter can be utilized. This simulation provides information about gain of the whole system. Gain can be set in range of 22 dB to 56 dB which corresponds with AGC gain range of -12 dB to 22 dB. Output of AGS is set to fixed output power of -5 dBm [1].

2.9.2 Power Consumption

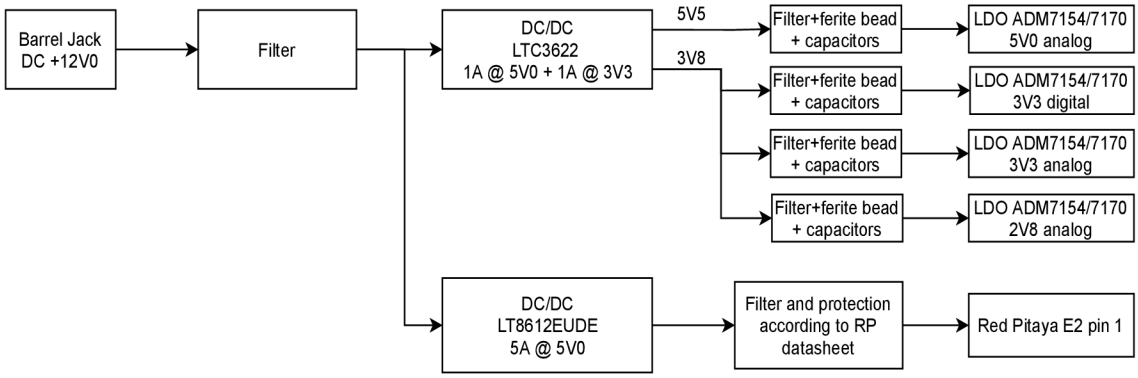
Since this device is supposed to be power directly from Red Pitaya low power consumption is crucial. All components were selected with power consumption kept in mind but according to [40] it can deliver only 500 mA on 5V0 rail and +3V3 rail combined (2.5 W max). This requirement was not met 2.7 so external power supply is used to delivered +12 V DC via barrel jack and it is fed to DC/DC converter. This device in order to work properly has also to power Red Pitaya. Whole powering scheme is displayed in 2.16.

This kind of powering scheme was selected in order to remove common powering plane between digital systems (PLL and AGC digital peripherals etc.) and sensitive analog RF circuitry (LNA at the input, mixers etc.) since noise generated by these devices can be easily picked up by sensitive components and amplified thus making the radio unusable. Also Red Pitaya, since it is mainly a digital system, is power directly from single DC/DC power supply in order to further limit EMI generated by fast FPGA/ADC switching.

In order to further minimize interference from switching of DC/DC power supply LTC3622 is selected. This device presents multiple modes of switching: Burst, Pulse skipping and can also be synchronized to external clock source. The last option can be exploited to move switching spectrum so that it would not interfere with currently selected spectrum.

To further suppress switching noise generated by DC/DC converters filters consisting of capacitors and ferrite bead is implemented between DC/DC and LDO according to [41]. LDOs with high PSRR and low noise are selected. In this case two different parts with similar properties are selected due to chip crisis.

Fig. 2.16: Whole powering scheme of RF front-end



Tab. 2.7: Power consumption of individual devices by power rail and sum

Device ID	Rail 5V0 [mA]	Rail 3V3 [mA]	Power [mW]
LNA1 (SW)	162		810
LNA2 (HF/VHF)	32		160
RF Switch 1		0.02	0.066
AGC	60		300
PLL 1		110	363
Upconverter	13		65
Switch 2		0.02	0.066
Switch 3		0.02	0.066
LNA 3 (IF)		7.7	25.41
PLL 2		110	363
I/Q Demodulator	180		900
SUM	447	227.76	2986.6

3 Implementation

After theoretical design of schematics, system parameter calculations whole device must be implemented. Since schematics are drawn in KiCAD this tool is selected even for PCB design. Whole system is designed as stack-able board for Red Pitaya platform.

3.1 PCB design

In order for any RF system to work properly, the most important thing is to keep impedance matching, EMC/EMS and power supply layout in mind.

3.1.1 Impedance matching

In order to deliver maximum power across the system, impedance of all block in cascade must be matched. Also, Friss' equations for NF cascade works only for matched system so any mismatch presents slight deviation in this parameters and could result to worse performance than expected [3]. Impedance miss match can also cause standing waves that could damage power components if not handled properly. Matching also includes transmission lines connecting individual blocks and connectors. In order to simplify design all blocks were selected in such way that they are either internally matched to 50 Ω or are easily matched for broadband operation. In order to match transmission line to the same impedance as all the other blocks present, various parameters must be taken into consideration. Board was made in Gatema using pool service with predefined stackup, that can be seen in 3.1.

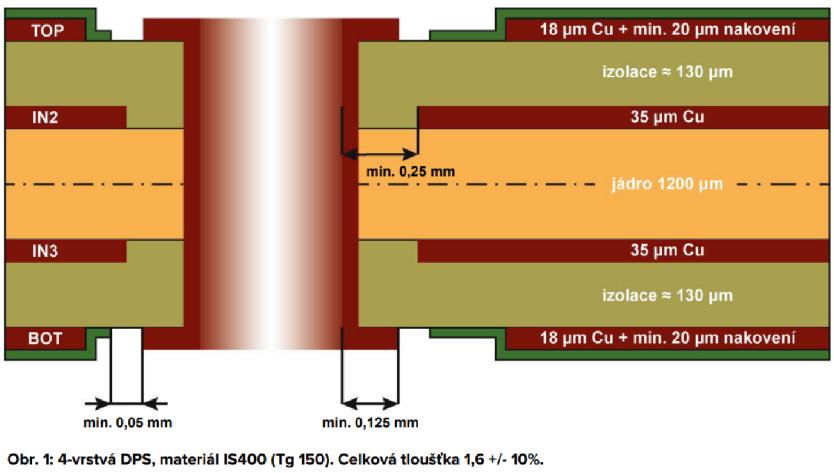


Fig. 3.1: Standard Gatema stackup for 4-layer PCB [44]

This option is relatively cheap and still provides very high quality PCBs. It was decided to use 4-layer PCB in order to reduce width of RF 50 Ω tracks and to simplify design. This way one whole layer (second layer) is used as reference ground for RF signals and second internal layer is used for powering. Stackup is based on IS400 which is lead free, mid tg epoxy laminate and prepreg provided by Isola. The most important parameters for transmission line design are Dk (Permittivity), Df (Loss Tangent) and substrate height (in this case prepreg between layer 1 and layer 2). These parameters influence final impedance of the transmission line. According to data sheet for given material Dk stays in range of 4.2 - 4.1 in 100 MHz to 1 GHz frequency span. Thickness of material between RF signaling layer and ground reference plane is around 130 μm, worst case dissipation factor is 0.02 for 1 GHz. In order to simplify design process, KiCAD includes transmission line calculator that can be utilized for such calculations. After inputting these parameters into the software it can be used to analyze or synthesize resulting with of the track [45].

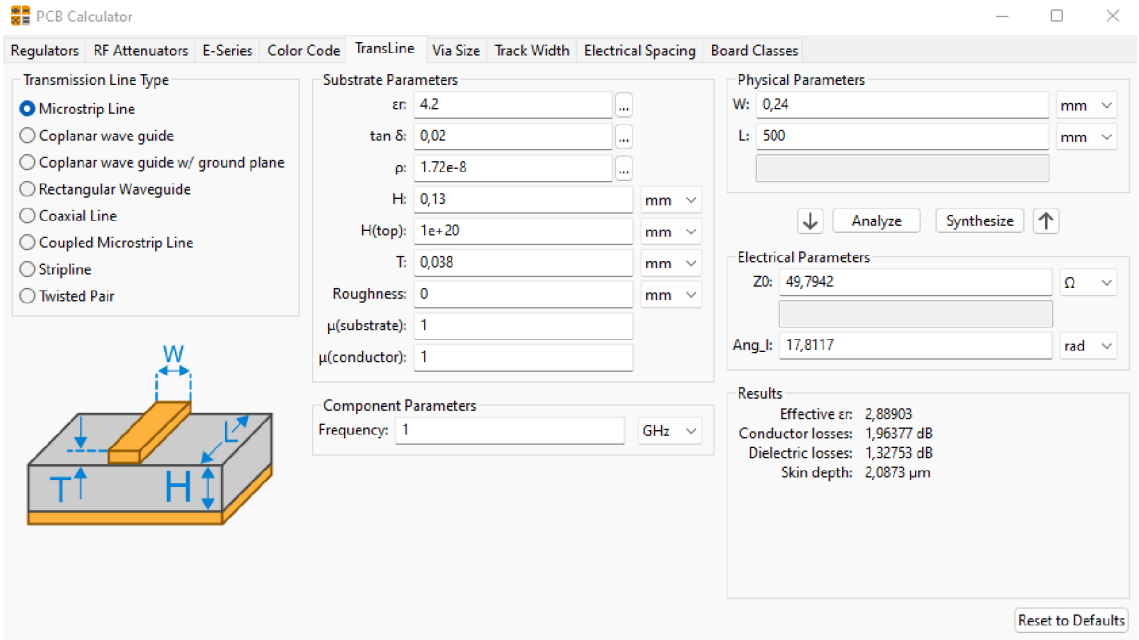


Fig. 3.2: KiCAD transmission line calculation for microstrip line (track + reference GND plane) and parameters provided by Isola datasheet

Resulting impedance varies between 50.30 Ω for $\varepsilon_r = 4.1$ and 49.80 Ω for $\varepsilon_r = 4.2$. Then by calculating reflection coefficients it can be obtained that,

$$\Gamma = \frac{Z_1 - Z_0}{Z_1 + Z_0} = \frac{50.3 - 50}{50.3 + 50} = 0.002991\ [-] \tag{3.1}$$

resulting in negligible impedance missmatch (good impedance matching) [3].

3.1.2 EMC/EMS - cross-talk, noise isolation

In order to minimize problems with noise generated by DC/DC switching power supplies, these blocks are put in designated area on the PCB, away from sensitive RF components and isolated with via stitching. For further isolation, small aluminum shield can be put on top of this region.

In order to minimize cross-talk between digital communication interfaces (SPI, I2C, GPIOs) and sensitive RF part, these signals are routed primarily on the bottom layer and connected to components by vias.

To improve EMC, RF tracks have via fencing around them. This way with proper impedance matching the unwanted radiation is minimized.

3.1.3 Powering

The most important part of power design is to maintain low impedance interconnections. In order to filter out input power signals, simple LC filter is placed right at the beginning of whole block.

3.2 Problems in PCB

3.2.1 SMA designator labels reversed

After closer inspection of the PCB it has been noticed that silkscreen specifying which port is for SW and which is for HF/VHF is incorrect. Since both monolithic filters for SW and HF/VHF present the same package this caused confusion during assembly resulting in need for them to be re-soldered. 3.3

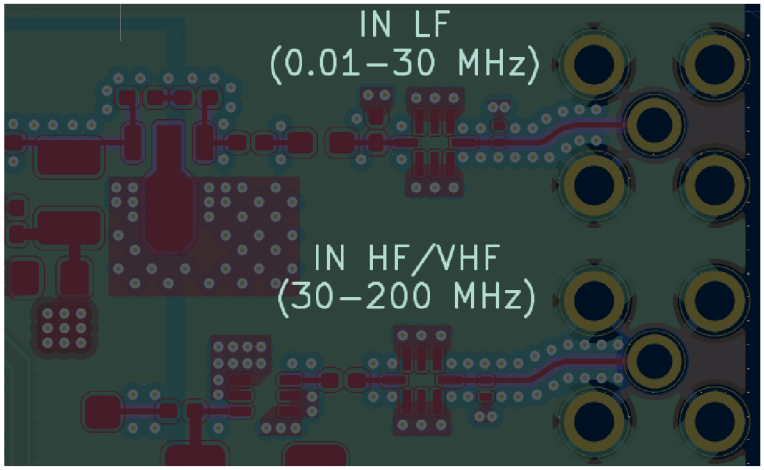


Fig. 3.3: Labels assigned to wrong SMA connector

3.2.2 Input low pass filters

Since buying two filters would result in unreasonably high shipping costs both filters were replaced with filters built on FR4 substrate using discrete components. Filter for SW band was designed with similar cutoff frequency as the commercial monolithic filter. After discussion cutoff frequency of low pass filter used to limit input signal in HF/VHF path was increased from 200 MHz to 240 MHz in order to fully comply with DRM receiver frequency band requirements 1.1. Both filters are hand made and matched to 50 Ω impedance.

3.2.3 Red Pitaya GPIOs

In order to control LO signal generators SPI interface is needed since both ICs present SPI-like interface (MOSI, SCLK and CE). In order to control both, separate CE pins are mandatory. GPIO driver of Red Pitaya is connected in such way that only 16 pins are controllable by ARM GPIO (through Linux environment). Other pins are controllable via other peripheral drivers (I2C, SPI etc.) and are not accessible directly as GPIO. During design this was not known resulting in not being able to control SPIs separately.

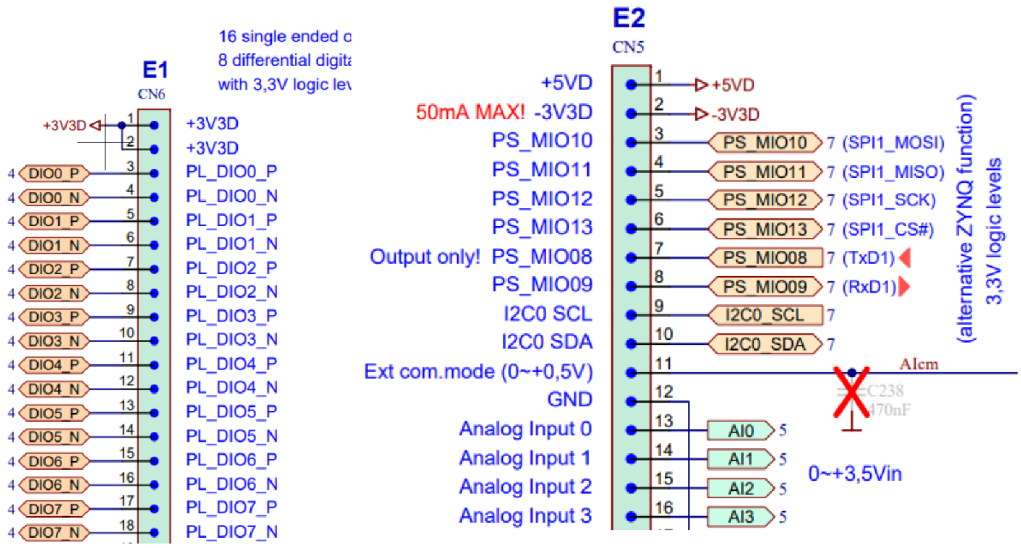


Fig. 3.4: Red Pitaya connectors E1 and E2 [15]

As it can be seen on 3.2.3 Red Pitaya presents two connectors. Pins on E1 are accessible through Linux interface as GPIO. Pins PS_MIO8 and PS_MIO13 are connected to CSs of ICs but they can not be controlled by GPIO controller so in order to select which device is being written to, tracks going out of these pins must

be cut and individual CSs must be connected to spare pins on E1. For this purpose pins 16 and 17 (DIO6_N and DIO7_P) were selected.

3.2.4 Wrong orientation of single to differential transformer

IF mixer was not working. It was found out that transformer that turns single ended output of AGC into differential so it can be used to drive differential inputs of LT5560 was placed inversely. The simple fix was to turn it 180 degrees and solder small wire under it and solder it to resistor connected to ground.

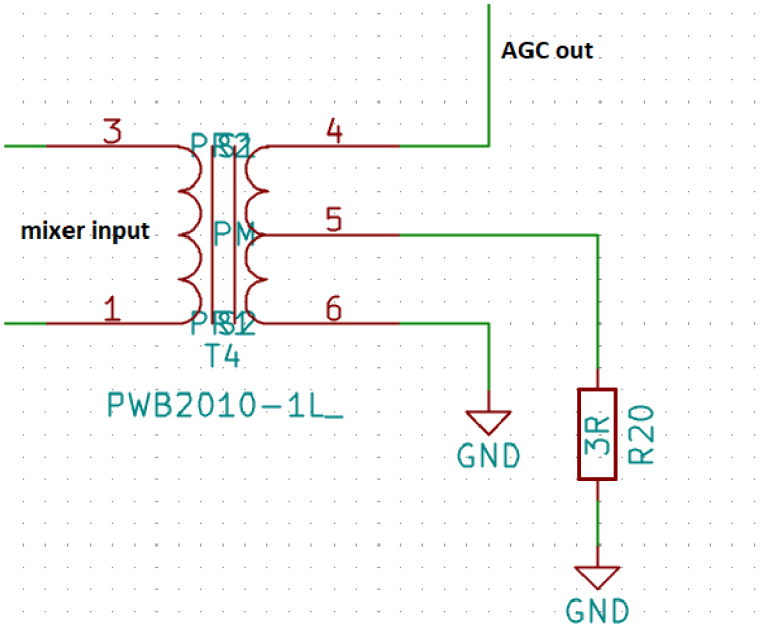


Fig. 3.5: Wrong orientation of transformer

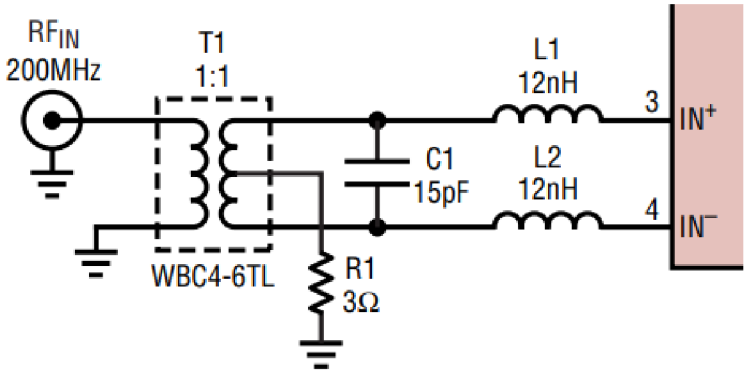


Fig. 3.6: Correct orientation of transformer to turn single ended input into differential [33]

3.3 Measured Parameters

3.3.1 Inputs

Both inputs (SW and HF/VHF) were measured using vector network analyzer in order to gain overview of the performance of the LNAs and filters. Since output power of VNA was at 0 dBm, saturating LNAs, 30 dB attenuator was inserted into the path resulting in all values being decresed by 30 dB. S-parameters (S21 and S11) of SW path show 3.7 that it is well matched (presenting -40 dB S11 maximum) while gain remains in whole range at around 20 dB. SW measurement was performed from 300 kHz up to 500 MHz.

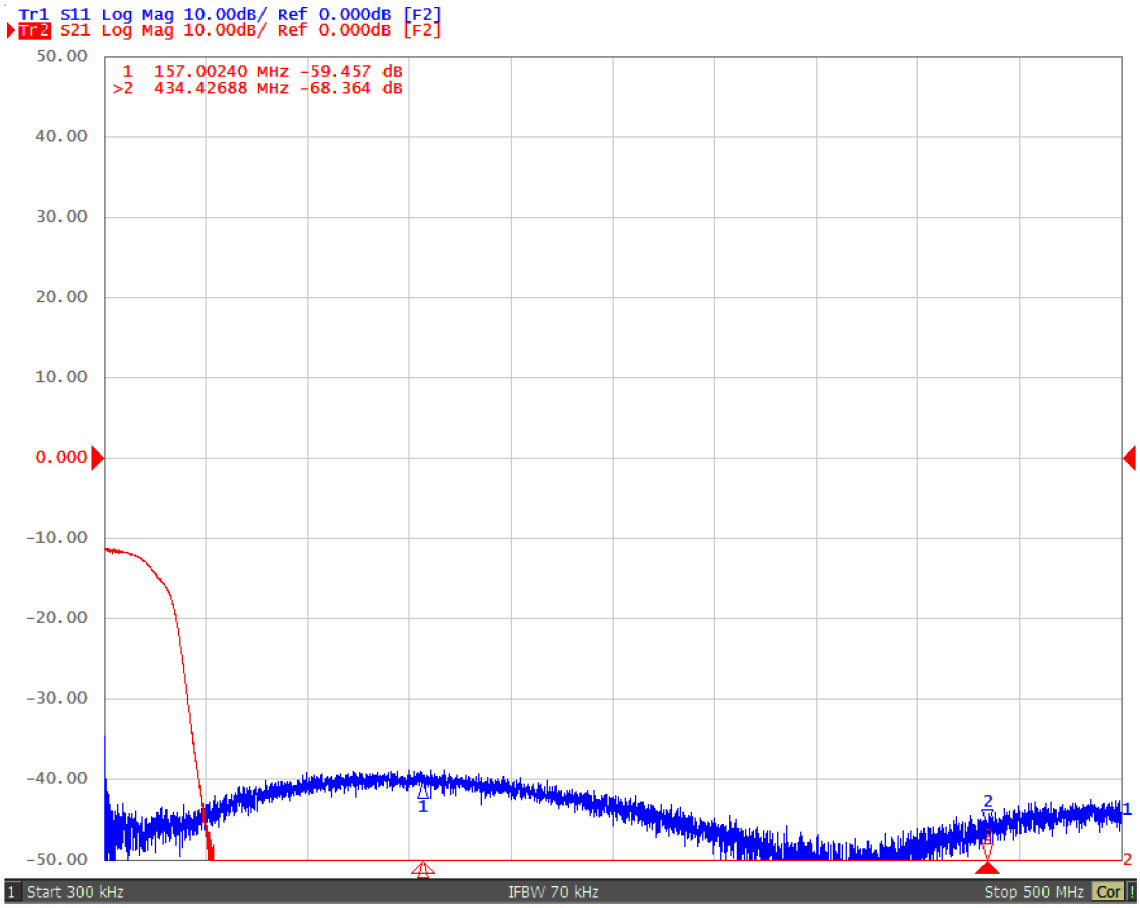


Fig. 3.7: S11 and S21 parameters of SW signal path (LNA + filter)

Measurement of HF/VHF signal path was done in similar manner to SW path, it was performed from 300 kHz up to 500 MHz with similar setup (with 30 dB attenuation). It can be seen 3.8 that the circuit is well matched and that the gain is relatively flat in whole pass band (presenting deviation of around 3 dB). Both spectrum interleave with each other.

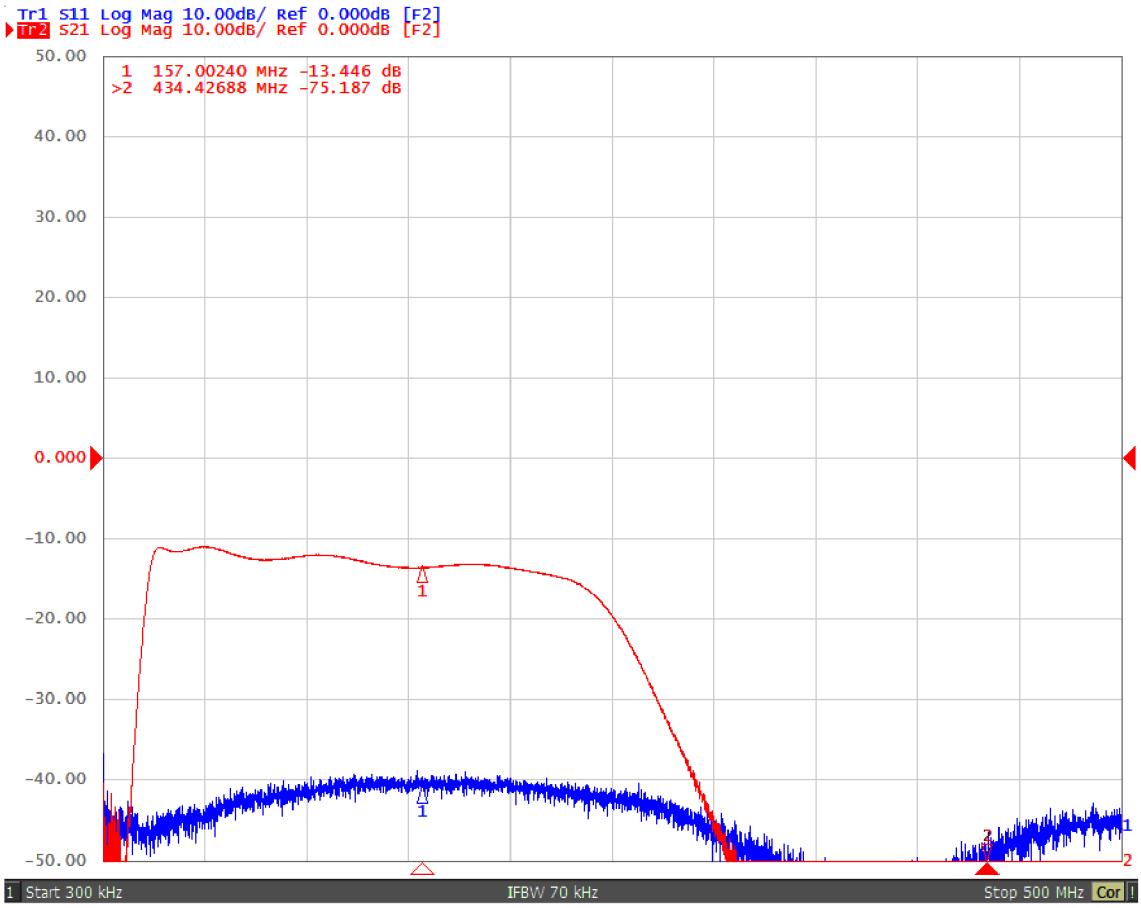


Fig. 3.8: S11 and S21 parameters of HF/VHF signal path (LNA + filter)

3.3.2 AGC

AGC is used to set constant power level in order to maintain dynamic range and to use whole range of ADC. Output of AGC is set by two resistor divider to 126 mV RMS about − 4.98 dBm. It can be seen that it stabilizes output for wide range of input power (ranging from −40 dBm up to −10 dBm). AGC also presents two capacitors which are used to set cut-off frequency of AGC. This is crucial in order to prevent AGC following amplitude modulations with slow symbol rate resulting in degradation of signal. By looking at 3.9 it can be seen that AGC works steadily in range from 250 kHz up to 30 MHz. Both characteristics 3.9 3.10 present also average value calculated from every frequency. The dip in characteristics in SW band for 100 kHz could be solved by using bigger capacitor on DECL and HPFL pins thus lowering AGC gain loop frequency.

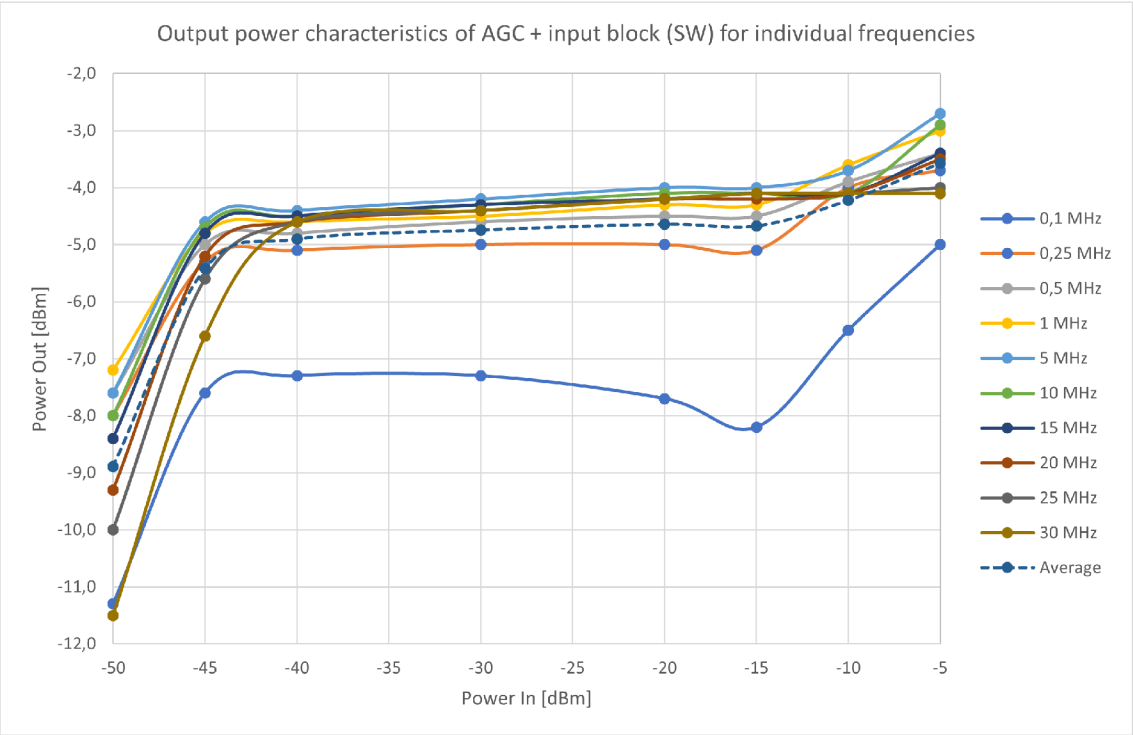


Fig. 3.9: AGC input to output characteristics for SW frequencies

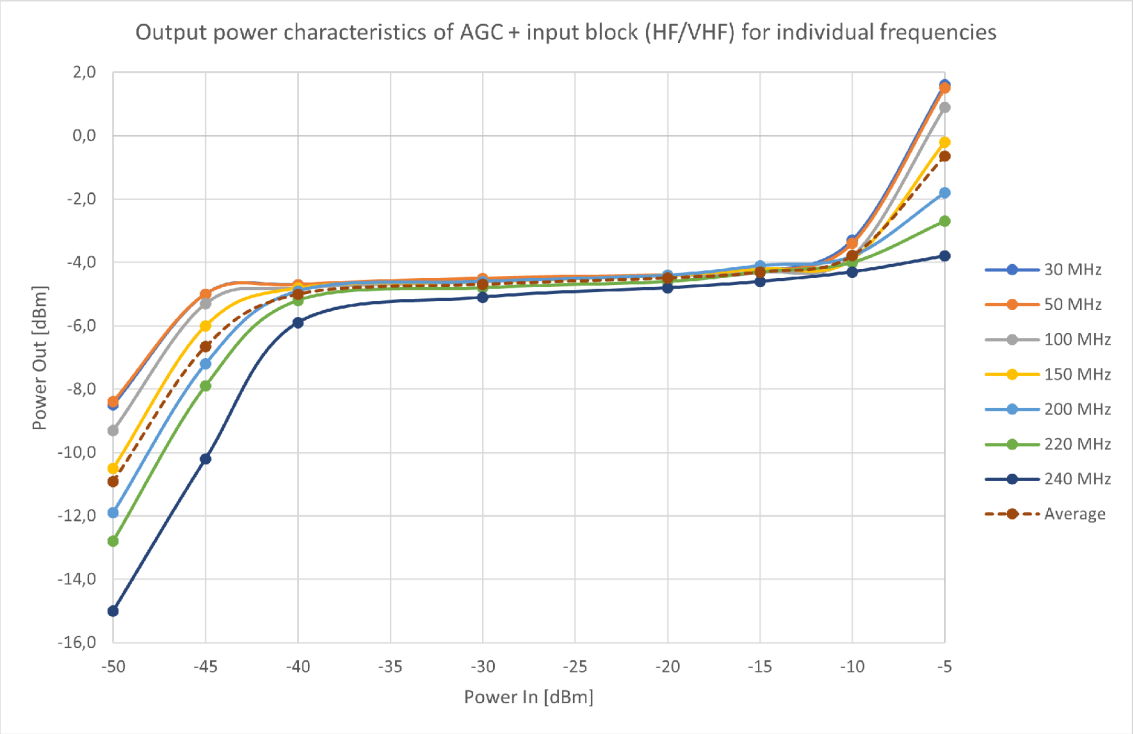


Fig. 3.10: AGC input to output characteristics for HF/VHF frequencies

3.3.3 IF filters

IF stage presents two filters, first is 5 MHz SAW filter and second is 70 MHz elliptic filter made out of discrete components. S-parameters (S11 and S21) of both filters have been measured with following amplifier stage. First image 3.11 (wide view) it can be seen that filter is narrow (bandwidth of around 8 MHz). By examining zoomed image 3.12, pass band of this filter can be estimated to be between in range of 429.2 MHz and 437.2 with gain of around 12 to 15 dB.

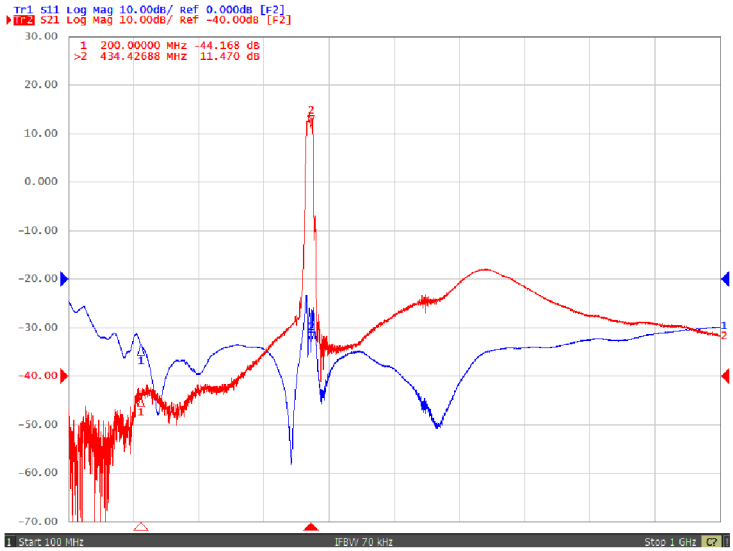


Fig. 3.11: S11 and S21 parameters of 5 MHz IF filter (filter + amplifier) from 100 MHz up to 1 GHz

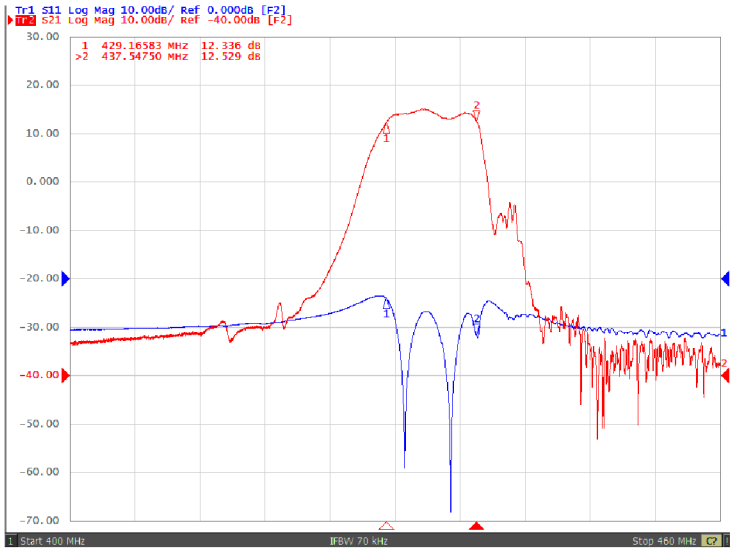


Fig. 3.12: S11 and S21 parameters of 5 MHz IF filter (filter + amplifier) from 400 MHz up to 460 MHz

Second IF filter is built out of discrete components (RF inductors and capacitors) because there was not any monolithic filter with desired parameters for reasonable price. In simulations inductors with Q factor of 30 @ 100 MHz were taken into consideration and capacitors were assumed to be ideal. By comparing SAW filter and this filters S21 parameter (3.13, 3.14) it can be seen that this filter presents attenuation greater by 10 dB. After evaluation of simulations and by adding resistance to each capacitor, results of the simulation are closer to those of the measurement. Nonetheless this filter can be used for sampling strong wideband signals where its high attenuation does not present a drawback.

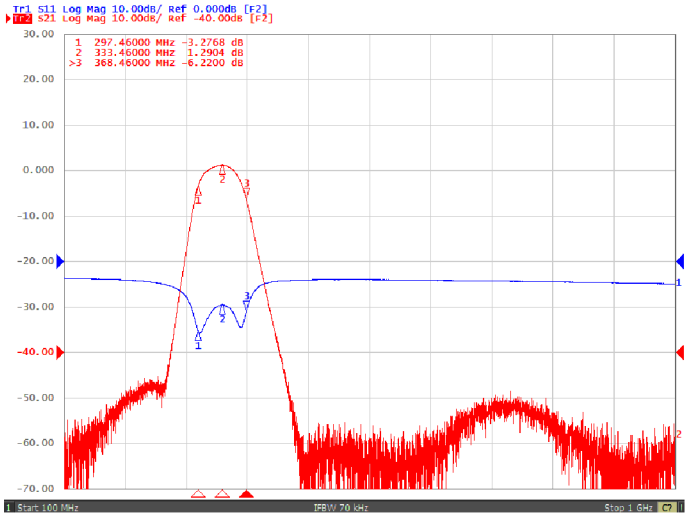


Fig. 3.13: S11 and S21 parameters of 70 MHz IF filter (filter + amplifier) from 100 MHz up to 1 GHz

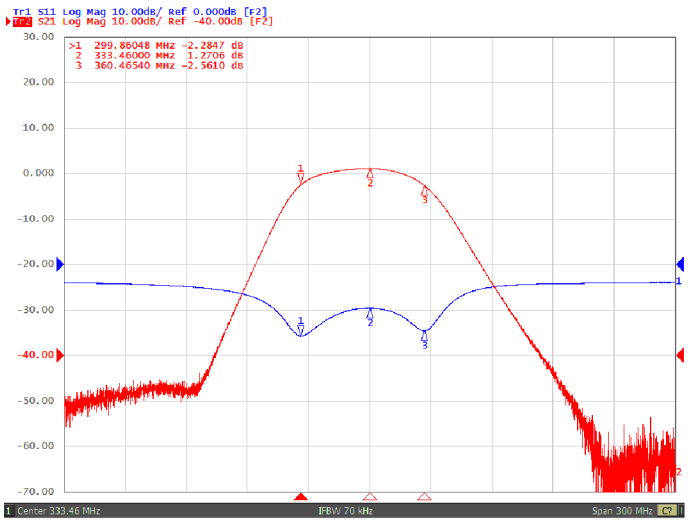


Fig. 3.14: S11 and S21 parameters of 70 MHz IF filter (filter + amplifier) with center 333.46 MHz and span of 300 MHz

3.3.4 Output of I/Q demodulator

Output of this RF front-end consists of two signals, I and Q. These signals are provided by IQ demodulator. Whole path was tested with variety of frequencies, modulations, symbol rates and input power. Both paths, SW and HF/VHF were tested in specified frequency ranges. Test in SW band can be seen in 3.15 and 3.16. It can be clearly seen that even at input power as low as −25 dBm output voltage is still decent (at around 200 mV_{p-p}).

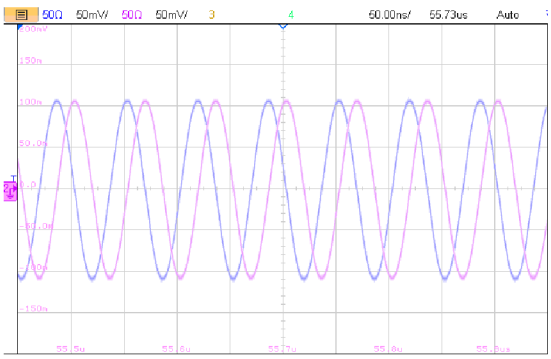


Fig. 3.15: I and Q signals of 15 MHz input signal with −25 dBm power and no modulation

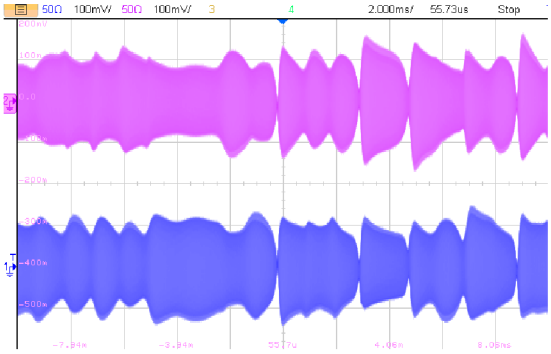


Fig. 3.16: I and Q signals of 2 MHz input signal with −25 dBm power QPSK modulation with 10 ksym/s

Test of HF/VHF band can be seen in 3.17 3.18. Output is still at around 200 mV_{p-p}. Signals on the output would be easily demodulated because they present good SNR.

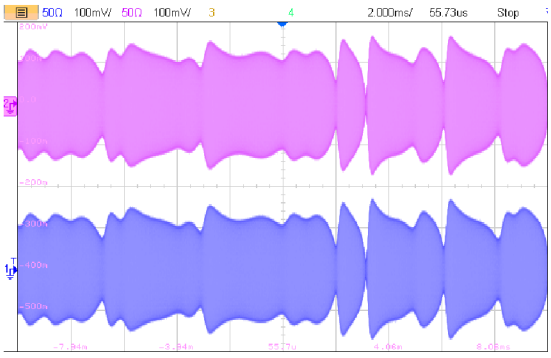


Fig. 3.17: I and Q signals of 50 MHz input signal with −25 dBm power 16QAM modulation with 1 ksym/s

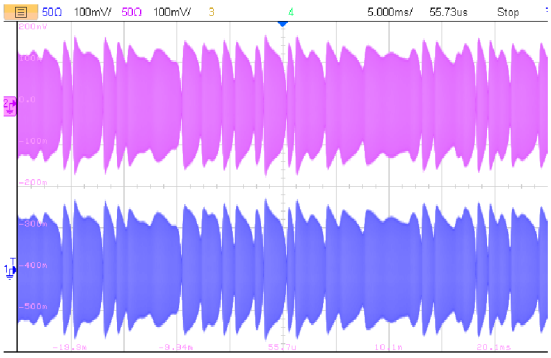


Fig. 3.18: I and Q signals of 150 MHz input signal with −25 dBm power 16QAM modulation with 1 ksym/s

3.4 Software

3.4.1 Controlling GPIOs

In order to control different subsystems (switching between different IF filters, selecting different bands etc.) Red Pitaya GPIO driver is used. This driver enables applications to access 16 GPIOs on connector E1. By including `rp.h` Red Pitaya HW API can be accessed. working with this library is straight forward. It allows to set direction (input, output) and state (high, low) for each individual GPIO. In order to simplify changing bands and filters for user, simple library is implemented. It implements functions for these task. Function for selecting bands, (`select_band(enum band_t band)` takes single argument, and updates GPIO. In similar manner, function `select_filter(enum if_filter_t filter)` can be used to select between `IF_FILTER_5MHZ` and `IF_FILTER_70MHZ`.

3.4.2 Controlling ADF4351 via SPI

Similarly for controlling SPI there is an SPI driver. It can be directly written to by Linux command `write`. In order to send 32-bit register values to ADF4351, `write_u32_order_spi` is implemented. Argument of this function is CS (chip select pin), data and SPI file handler. In order to calculate values for each register, ADF4351 interface is implemented. This interface defined in `adf4351_spi_driver.c` consists of three structures: `ADF4351_register_t` containing register values as plain 32-bit integers, `ADF4351_t` containing frequency dependent variables (INT, FRAC, MOD etc.) and `ADF4351_settings_t` containing all settings for ADF4351 PLL. First step in order to control output frequency of ADF4351 is to calculate necessary parameters. For this purpose there is a function `Pll_ADF4351_set_frequency` taking output frequency as parameter and pointer to ADF4351_t in order to save settings for future processing. Following this step, it is necessary to load default setting by calling `Pll_ADF4351_load_default_settings`. finally in order to store these values in 32-bit integers for SPI transmission it is necessary to call `Pll_ADF4351_fill_registers` providing it with all necessary structures. After that, register values can be viewed by calling `Pll_ADF4351_display_registers_hex`

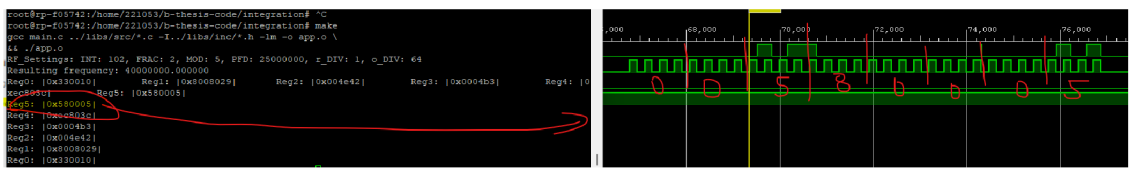


Fig. 3.19: View of SPI write to register 5 of value 0x580005 using ILA in FPGA

in order to verify registers with values from software from Analog Devices. In order to update registers in ADF4351, registers must be written in descending order (starting with reg5 to reg0) by calling `write_u32_order_spi` and providing individual registers. SPI must be released after transaction by calling `release_spi`.

3.4.3 QPSK demodulator

In order to receive and demodulate QPSK signal, it is necessary to use QPSK demodulator. Simple QPSK demodulator without frequency and phase correction may look like this 3.20. This demodulator is able to correctly demodulate only QPSK signals that are perfectly aligned with phase and frequency of f_c.

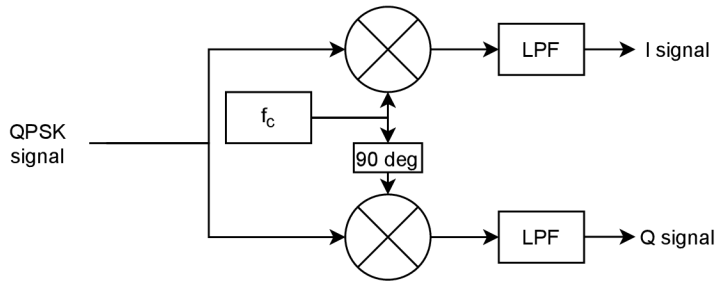


Fig. 3.20: Simple QPSK demodulator

In real world applications frequency and phase of transmitter and receiver are not the same due to different varying of temperature, distance and even tolerances of components. In addition to initial miss alignment it is common for these parameters to drift during operation. In order to synchronize and correctly demodulate QPSK signal in real world applications, to correct frequency and phase, blocks like Costas loop can be utilized [4], [9].

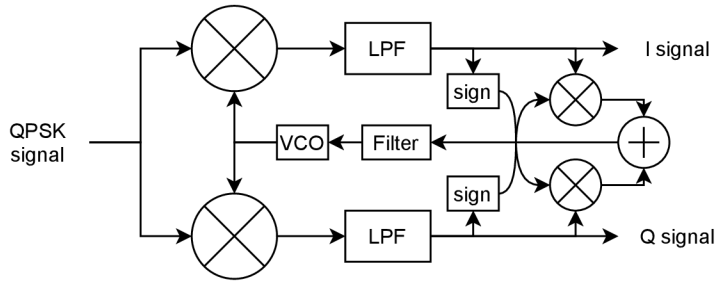


Fig. 3.21: QPSK demodulator with Costas loop

QPSK demodulator was implemented in matlab for easy demonstration and simplicity of implementation. Signal from Red Pitaya was loaded and then demodulated. After frequency and phase synchronization it is necessary to take samples of

input signal while symbol is stabilized. For this purpose mean square error method is used for finding smallest value of EVM (error vector magnitude) and synchronizing to symbols. Output of Costas loop and resulting IQ diagram after MSE symbol synchronization 3.22 3.23.

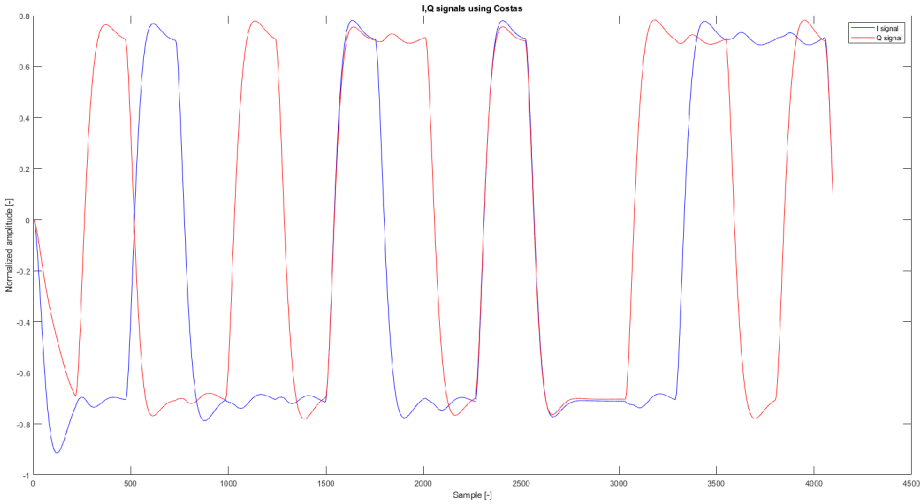


Fig. 3.22: Output of QPSK demodulator with Costas loop

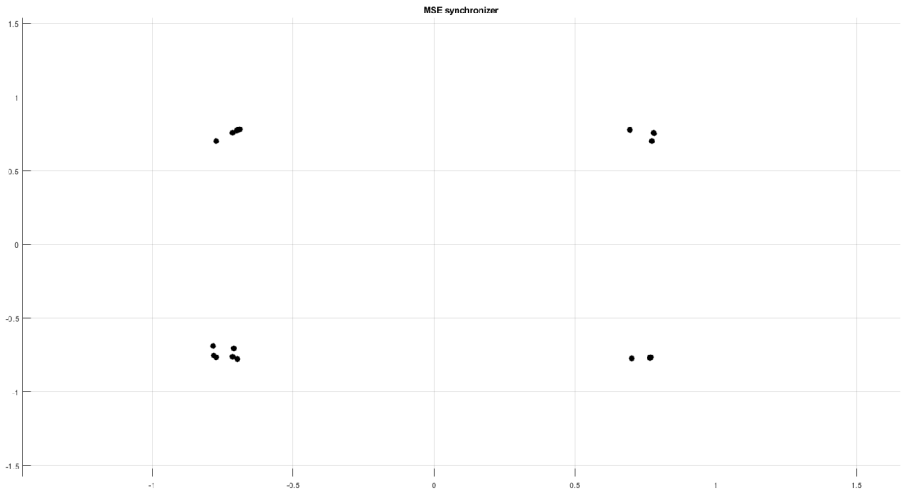


Fig. 3.23: IQ diagram of QPSK demodulated signal using Costas loop and MSE for symbol synchronization

3.5 Final PCB

Fig 3.24 is top view of the final PCB. All fixes are present on the board and is fully functional. In 3.25 it can be seen that PCB is mounted on top of Red Pitaya.

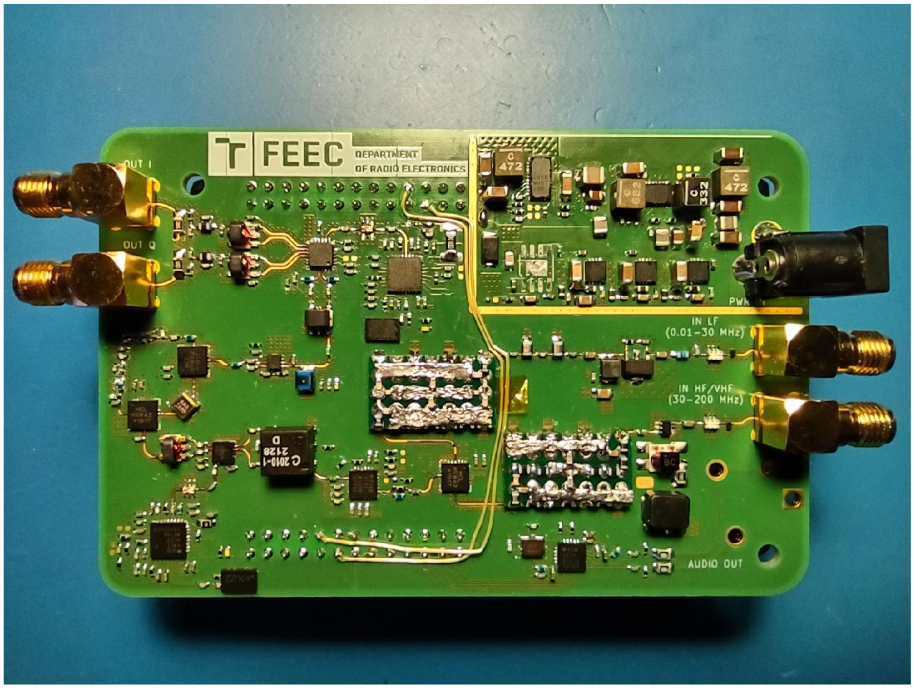


Fig. 3.24: Image of final PCB

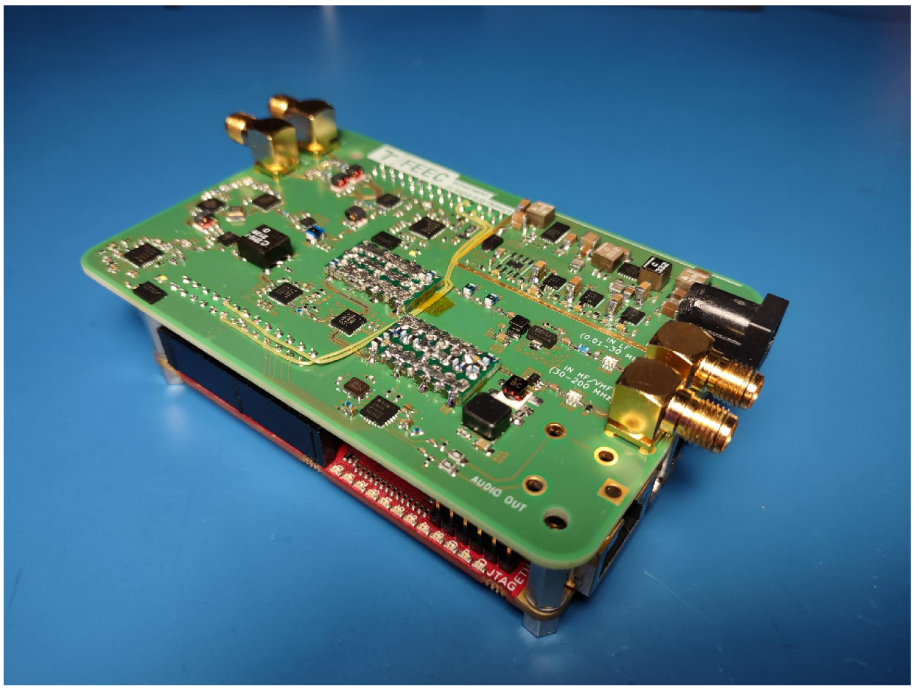


Fig. 3.25: Image of final PCB stacked on Red Pitaya

Conclusion

The main objective of the thesis is analog front end for Red Pitaya. These two devices together work as SW and HF/VHF receiver thus being compliant with DRM receiver specifications. Initially DRM requirements (frequency bands, SNR, minimal sensitivity, etc.) have been taken into consideration and used as reference for determining receiver architecture and component parameters. The most versatile and effective receiver architecture has been determined to be dual-conversion receiver since it allows usage of filters with high Q (SAW or crystal filters) and presents good image rejection. Also LO leakage is minimized due to presence of multiple components with low S12 in signal path between antenna and mixers. This architecture with I/Q demodulator increases bandwidth to 100 MHz. Input signal is filtered to prevent LNA saturation and to minimize noise. Analog front-end also presents two filters in IF stage. First filter is high order wide band bandpass filter built out of discrete components with bandwidth of around 70 MHz. Second filter is high order narrow band SAW filter used to further limit noise. In order to select only desired channels digital filtering must be implemented inside FPGA. In order to amplify weak signals LNA is used in cascade with AGC to set constant power level. Selected amplifiers are highly linear presenting high IP3 and P1dB. Linearity is necessary to demoudulate modulations with envelope (AM etc.). Two mixing stages are used. First mixing stage upconverts signals to IF stage. Second stage is used to downconvert signals to baseband to be sampled by ADC. As LO frequency synthesizer fraction-N PLL synthesizers are used. Two antennas were selected each for different frequency range in order to maximize gain. Input is protected with LP filter and TVS. In order to listen to demodulated signals audio codes is placed on board unfortunately due to lack of time it is not implemented in software. Whole device is powered by external power supply since Red Pitaya is not able to deliver enough power. After design stage, PCB has been designed and manufactured. After assembly process functionality has been verified. Problems found were addressed and solved by HW modifications or software modifications. Parameters of final board were similar to parameters provided by simulations except for wideband IF filter. Capacitors used in this filters were during simulation thought to be ideal which turned out to cause non negligible attenuation. In the end QPSK demodulator was implemented in matlab which provides good interface that can be used to debug.

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Symbols and abbreviations

DRM	Digital Radio Mondiale
DSP	Digital Signal Processing
ADC	Analog to Digital Converter
FPGA	Field Programable Gate Array
SoC	System On Chip
MCU	Microcontroller Unit
ARM	Advanced RISC Machines
VGA	Variable Gain Control
SW	Short wave
HF/VHF	High Frequency/Very High Frequency
CW	Constant wave
QAM	Quadrature amplitude modulation
AM	Amplitude modulation
SSB	Single sideband
USB	Upper sideband
LSB	Lower sideband
PSK	Phase Shift Keying
ASK	Amplitude Shift Keying
FDM	Frequency-division multiplexing
OFDM	Orthogonal frequency division multiplexing
SNR	Signal to Noise Ration
BER	Bit error rate
PSRR	Power Supply Rejection Ration
SAW	Surface acoustic wave

List of appendices

A Schematics

Fig. A.1: RF front-end

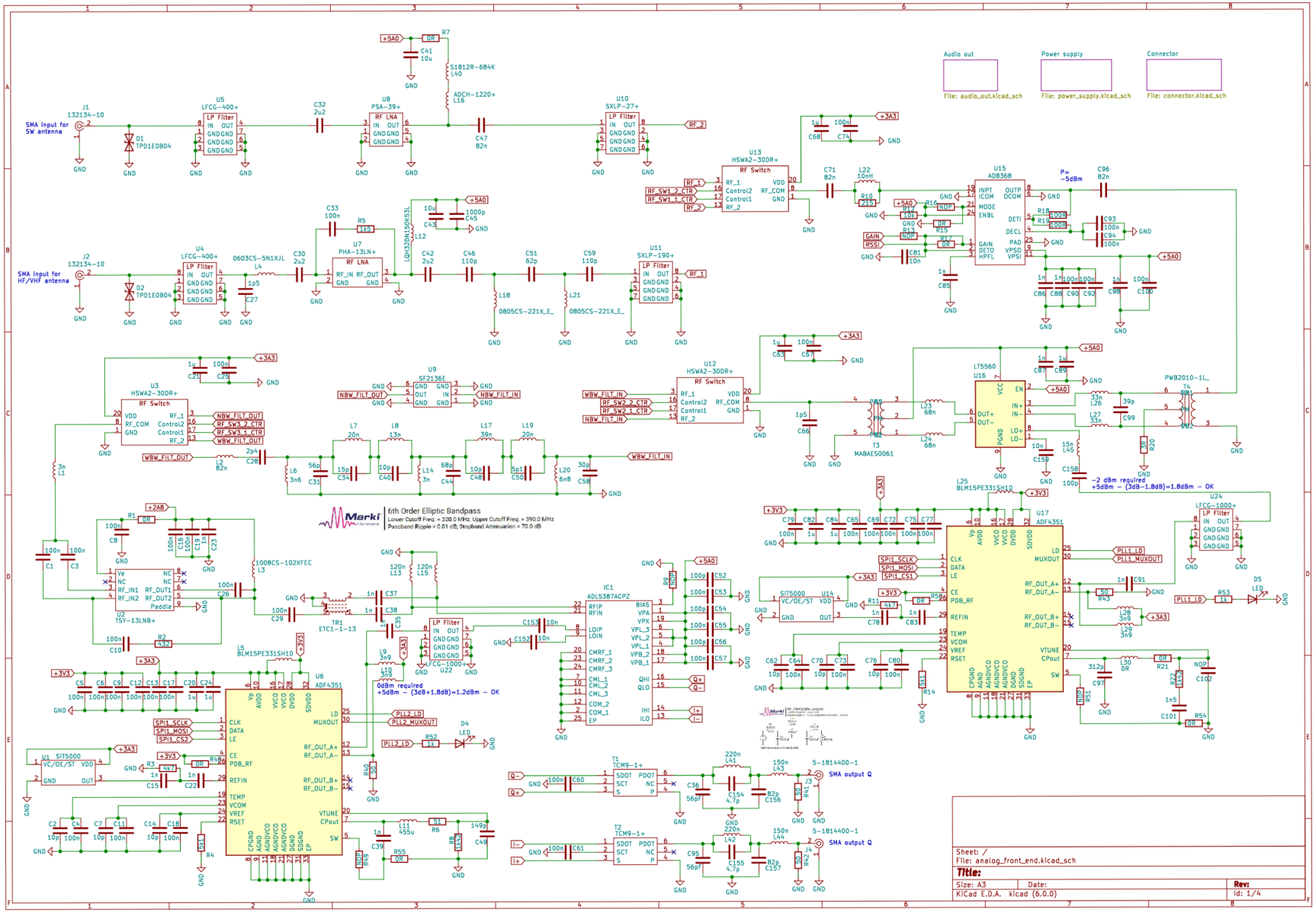

Fig. A.2: Powering scheme

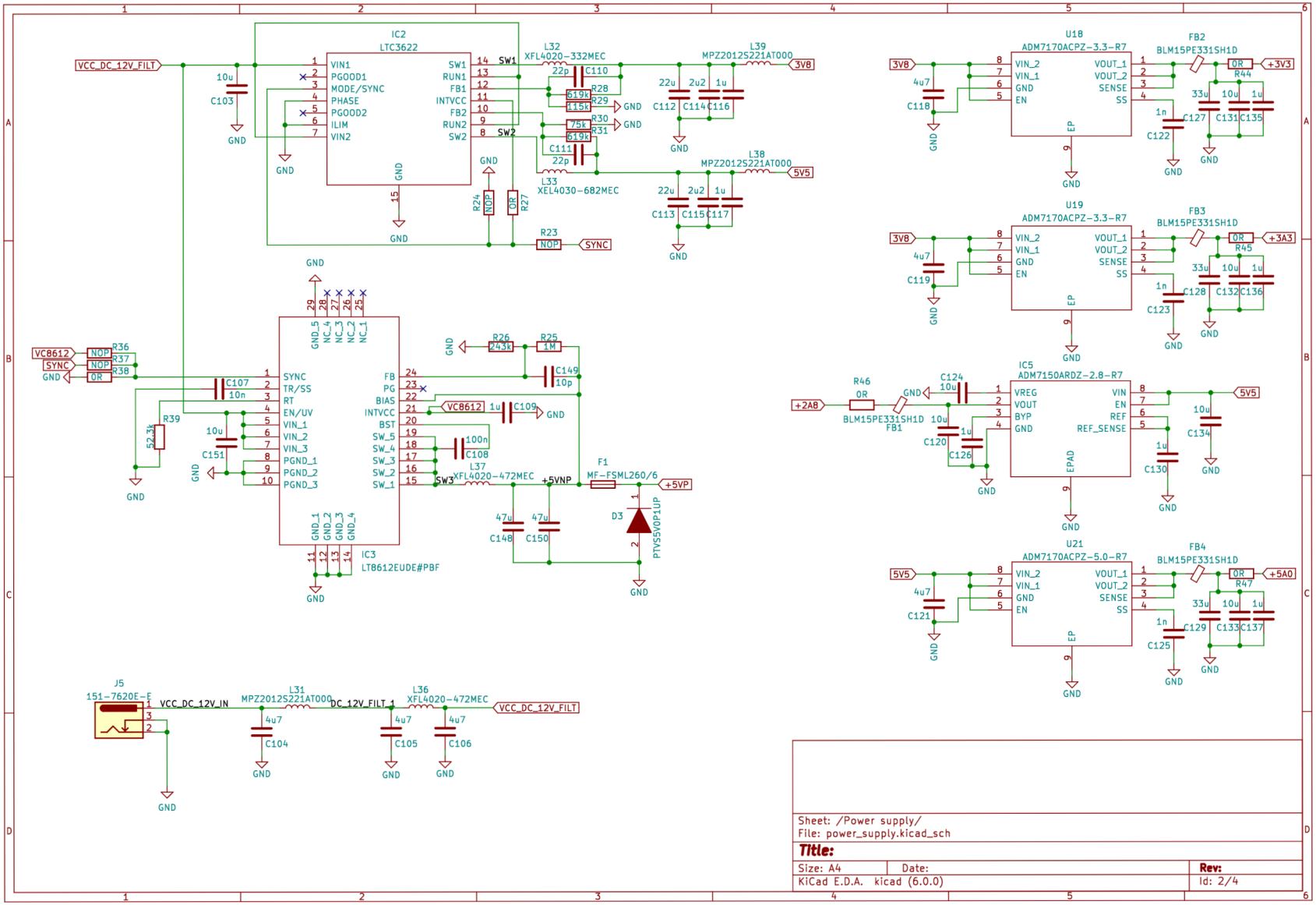

Fig. A.3: Red Pitaya connection scheme

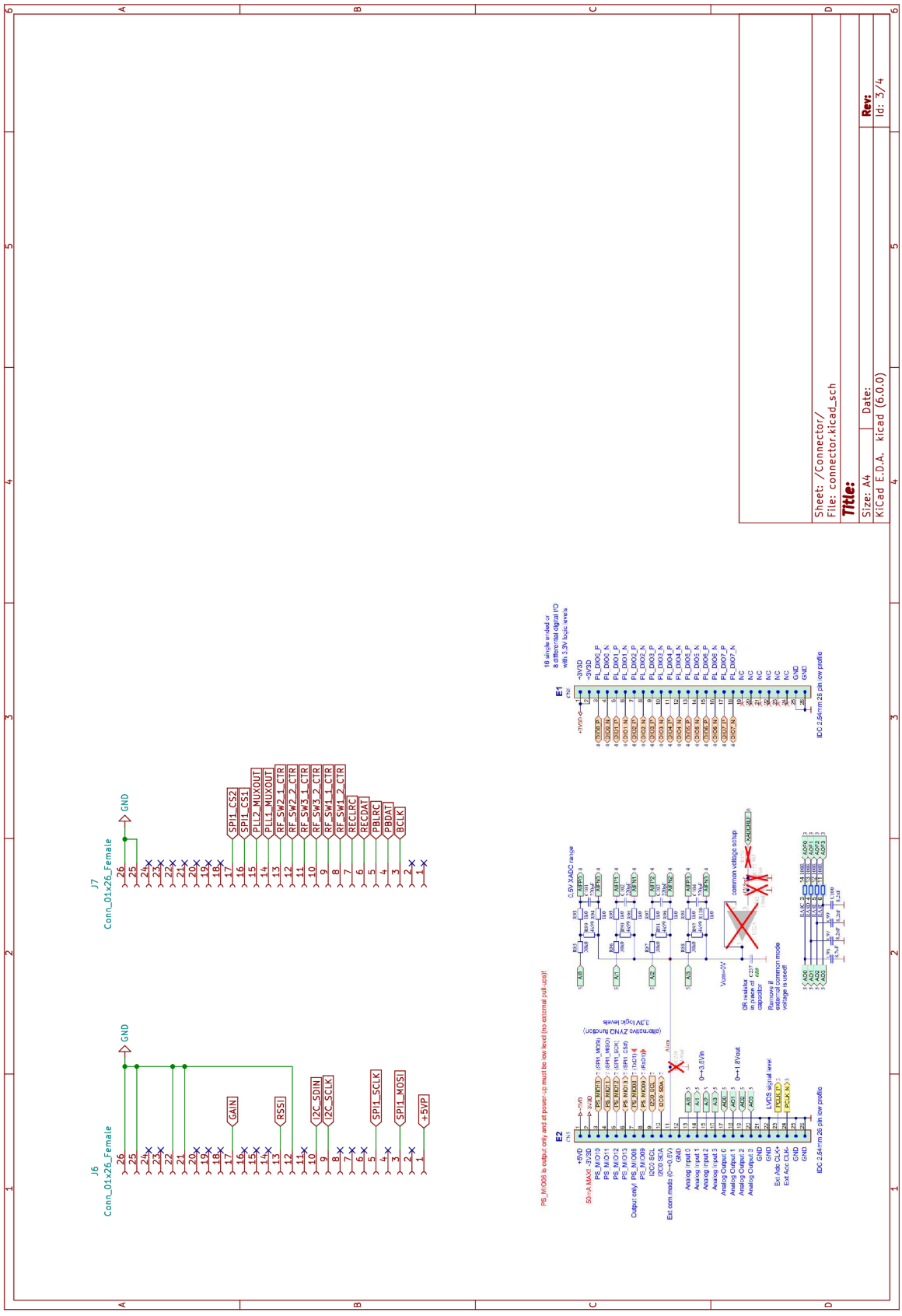

Fig. A.4: Audio coded scheme

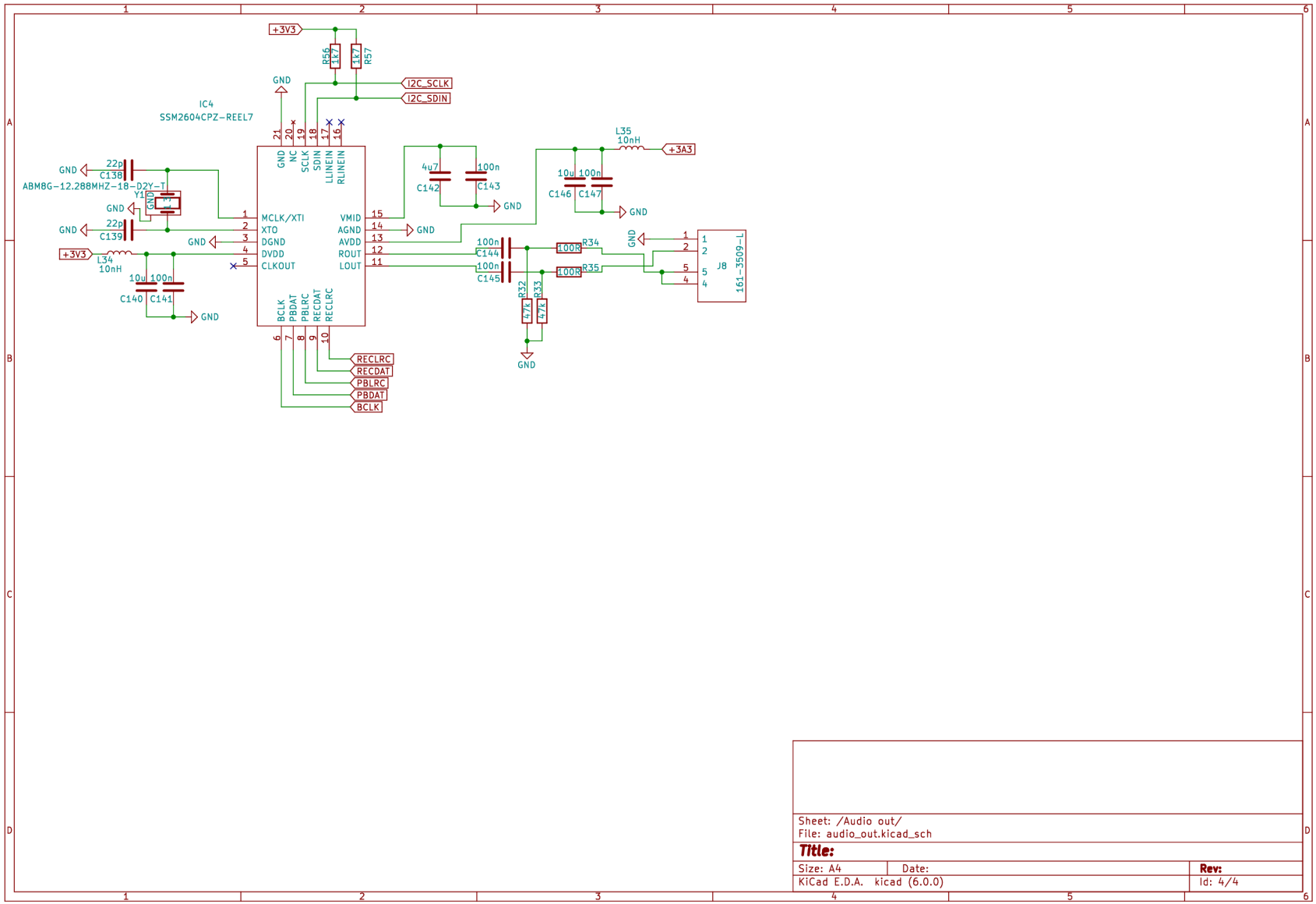

Fig. A.5: System diagram