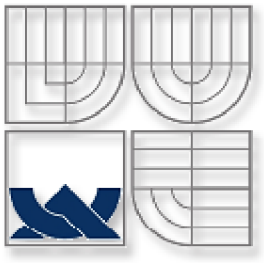

BRNO UNIVERSITY OF TECHNOLOGY

Faculty of Electrical Engineering and Communication

LOW VOLTAGE CURRENT-CONVEYORS DESIGN TECHNIQUES

DISSERTATION THESIS

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ABSTRACT

This thesis work discusses the low-voltage current-mode CCII analog circuits and their various aspects. The need of high speed, high performance, low power circuits because of the advent of the portable electronic and mobile communication systems and difficulties faced in achieving that in today, this need for high performance LV circuits give encourages the analog designers to look for new circuit architectures, and new LV techniques.

Self cascode and bulk-driven techniques can help to produce efficient LV circuits with reduced power supply restrictions are explained, some of the basic building blocks such as current mirrors, differential pairs structures capable to operate in LV are explored and discussed. The basic device level techniques also play important role in the design of smarter and efficient circuits; some of those techniques have also been discussed here.

Designing CCII using low voltage techniques is the core part in this thesis, their advantages are discussed here and a comparison with the conventional mode circuits has been presented, The principle and the implementation of the most common CCII-based operational amplifier circuits has been described.

KEYWORDS

Low Voltage Current Conveyor, Bulk-Driven Mosfet, Self Cascode Mosfet, Bulk-Driven Current Conveyor, self cascode current conveyor, Current Conveyor Based Filters.

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List of Abbreviations

CC	Current Conveyor
CCI	First Generation Current Conveyor
CCII	Second Generation Current Conveyor
CCIII	Third Generation Current Conveyor
CCCII	Current Controlled Current Conveyor
DOCC	Dual Output Current Conveyor
CGCCII	Current Gain Controlled Conveyor
DVCCII	Differential Voltage Current Conveyors
FDCCII	Fully Differential Current Conveyors
N	Network
Na	Adjoint Network
LP	Low-Pass
HP	High-Pass
BP	Band-Pass
OTA	Operational Transconductance Amplifier

List of symbols

BW	Bandwidth [Hz]
C	Capacitance [F]
C_{BD}	Bulk-drain capacitance [F]
C_{BS}	Bulk-source capacitance [F]
C_{GB}	Gate-bulk capacitance [F]
C_{GD}	Gate-drain capacitance [F]
C_{GS}	Gate-source capacitance [F]
C_{OX}	Thin oxide capacitance per unit area [$F.m^{-2}$]
C_{GB0}	Gate-bulk capacitance [$F.m^{-1}$]
C_{GD0}	Gate-drain overlap capacitance [$F.m^{-1}$]
C_{GS0}	Gate-source overlap capacitance [$F.m^{-1}$]
C_L	Load capacitor [F]
CMR	Common mode range [V]
$CMRR$	Common mode rejection ratio [dB]
f	Frequency [Hz]
f_T	Unity gain frequency [Hz]
GBW	Gain-bandwidth product[Hz]
g_m	Gate transconductance [S]
g_{mb}	Bulk transconductance [S]
γ	Bulk threshold parameter [$V^{1/2}$]
I	Current [A]
I_B	Bulk current [A]
I_D	Drain current [A]
Ix	X node current (input current), [A]
Iz	Z node current (output current) [A]
k	Boltzmann's constant [$J.K^{-1}$]
K	Transconductance parameter [$A.V^{-2}$]
L	Channel length [m]
L_D	Lateral diffusion [m]
λ	Channel length modulation coefficient [V^{-1}]
R	Resistance [Ω]
rx	X node impedance[Ω]

rz	Z node impedance[Ω]
ry	Y node impedance[Ω]
ro	Output resistance [Ω]
V_{DD}	Positive supply voltage [V]
V_{BS}	Bulk-source voltage [V]
V_{DS}	Drain-source voltage [V]
V_{dsat}	Saturation voltage [V]
V_{GS}	Gate-source voltage [V]
V_T	Threshold voltage [V]
V_{T0}	Threshold voltage at V_{BS}=0 [V]
V_{SS}	Negative supply voltage [V]
vy	Y node voltage (input voltage) [V]
vx	X node voltage [V]
W	Channel width [m]

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Contents

1 Introduction

Since the beginning of electronics, the need of new active devices has always been very important. It has driven to the birth of transistors which have been used, then, in amplifiers, impedance converters, filters, etc... In particular, the voltage operational amplifier has rapidly become the main analog block and has dominated the market since the advent of the first analog integrated circuits. Nowadays, the situations changing because there is a new impulse towards these called current mode circuits, which are able to overcome the limitation of a constant gain- bandwidth product and trade-off between speed and bandwidth, so that performance is improved in terms of low-voltage characteristics and of slew-rate and bandwidth.

1.1 Voltage mode to current mode

One procedure for finding alternative, preferably simpler, circuit realizations is to use current signals rather than voltage signals for signal processing. MOS-transistors in particular are more suitable for processing currents rather than a voltage because the output signal is current both in common-source and common-gate amplifier configurations and common-drain amplifier configuration is almost useless at low supply voltages because of the bulk-effect present in typical CMOS-processes.

Moreover, MOS current-mirrors are more accurate and less sensitive to process variation than bipolar current-mirrors because with the latter the base currents limit the accuracy. Therefore, at the very least, MOS-transistor circuits should be simplified by using current signals in preference to voltage signals. For this reason, integrated current-mode system realizations are closer to the transistor level than the conventional voltage-mode realizations and therefore simpler circuits and systems should result. When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits.

Current-mode circuits cannot avoid nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit techniques. Current-mode interconnection circuits in particular show promising performance.

1.2 Adjoint principle

As a wide range of voltage-mode analog circuits already exist, a straight forward method of converting these voltage-mode circuits to current-mode circuits would be very useful. In such a method a circuit using voltage amplifiers and passive components is converted into one that contains current amplifiers and passive components. An ideal voltage amplifier has infinite input impedance and zero output impedance, while an ideal current amplifier has zero input impedance and infinite output impedance.

Consequently, direct replacement of a voltage amplifier with a current amplifier will lead to different circuit behavior.

A voltage-mode circuit can be converted into a current-mode circuit by constructing an inter-reciprocal network by using the adjoint principle [4]. According to this principle, a network N is replaced with an adjoint network Na, the voltage excitation is interchanged to a current response, and the voltage response is interchanged to a current excitation, as demonstrated in Figure 1-1. Thus, the resulting transfer functions of these two networks N and Na are identical:

$$H_v(S) = \frac{v_{out}}{v_{in}} = \frac{i_{out}}{i_{in}} = H_i(S) \qquad 1.1$$

The networks N and Na are thus said to be inter-reciprocal to one another. When the networks N and Na are identical, for example in the case of passive networks, the networks are said to be reciprocal. Since all passive networks are reciprocal, all passive circuit elements have themselves as their adjoint elements i.e., passive elements are inter-reciprocal. In order to maintain identical transfer functions for both the original network N and the adjoint network Na the impedance levels in the corresponding nodes of both networks should be identical. Therefore, the signal flow is reversed in the adjoint network and a voltage source is converted to a current sensing element as they both behave as short circuits. Similarly, a voltage sensing element is converted to a current source.

A list of circuit elements and their adjoint elements are presented in the Table 1-1. In addition, controlled sources can be converted with the same principles: the signal flow is reversed and the impedance level is kept the same. In this way, a voltage amplifier is converted to a current amplifier and a current amplifier is converted to a voltage amplifier, respectively. However, since transresistance and transconductance amplifiers are inter-reciprocal, networks containing only transresistance or transconductance amplifiers and passive elements differ only in signal direction and type.

The adjoint principle can also be applied to transistor level circuits. In this case, a bipolar transistor in a common-emitter amplifier configuration is inter-reciprocal to itself and the common-collector amplifier configuration has the common-base configuration as its adjoint. Converting a voltage-mode bipolar transistor circuit to a current-mode MOS-transistor circuit could be beneficial as it minimizes the use of source-follower stages which have poor low-voltage performance due to the bulk effect Bipolar transistor circuits are conventionally constructed of common-emitter and common-collector amplifier stages and the resulting MOSFET transistor adjoint circuit is constructed of common-source and common-gate amplifier stages

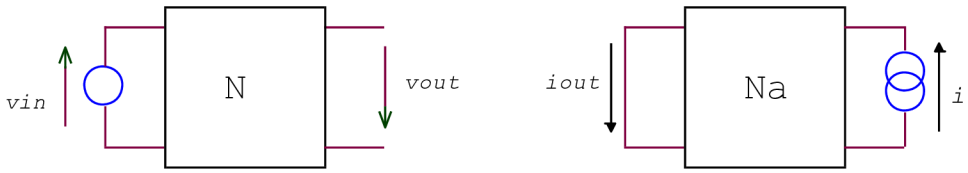

Figure 1-1 inter-reciprocal networks N and Na

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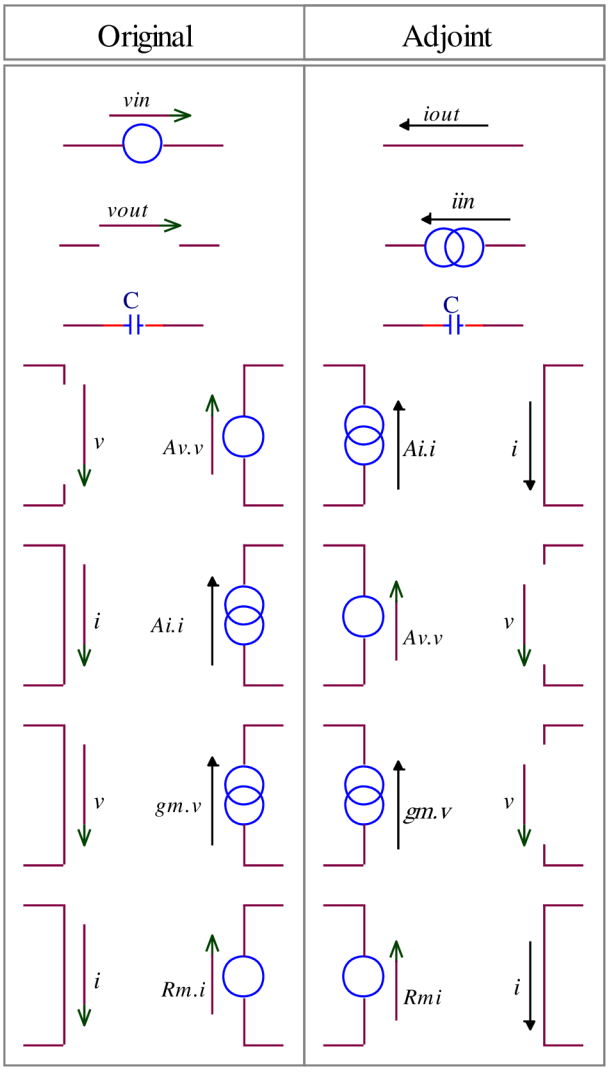


Table 1-1 Some circuit elements with their corresponding adjoint elements.

1.3 Current conveyors

Analog VLSI can address almost all real world problems and finds exciting new information processing applications in variety of areas such as integrated sensors, image processing, speech recognition, hand writing recognition etc. All conventional analog circuits viz., op amps, voltage to frequency converters, voltage comparators etc. are voltage mode circuits, which suffer from low bandwidths arising due to the stray and circuit capacitances and are not suitable in high frequency applications.

The need for low-voltage low-power circuits is immense in portable electronic equipments like laptop computers, pace makers, cell phones etc. voltage mode circuits are rarely used in low-voltage circuits as the minimum bias voltages depend on the threshold voltages of the MOSFETs. However, in current mode circuits, the currents decide the circuit operation and enable the design of the systems that can operate over wide dynamic range. The low end of the circuit operating range is limited by the leakage currents and noise floor level while the high end is decided by degradation of the trans-conductance per unit current available above the threshold voltage[1].

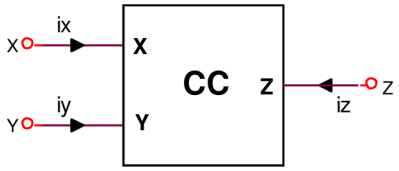


Figure 1-2 Current conveyor symbol.

These circuits can give large bandwidths and are suitable for low-voltage applications. Current feedback amplifiers, Operational floating Conveyors, Current Conveyors (CCs) etc. are the popular current mode circuit's structures and most widely used structure among them is the CCII structure [2]. In this work we present some of the emerging applications of the CCs and the classification schemes.

A CC is a three or more port (X, Y, and Z) network. The commonly used block representation of a CC is shown in Figure 1-2, whose input-output relationship is given by

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & A & 0 \\ B & R_X & 0 \\ 0 & C & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad 1.2$$

where A, B, C assume a value either 1, 0 or −1 and RX is the intrinsic resistance offered by the port X to the input currents. For an ideal CC VX = VY and the input resistance (RX) at port X is zero (equation 1-2).

But in practical CCs, RX is a nonzero positive value. So the equivalent symbol of a CC should include RX in its representation and the popular CC symbol is shown in Figure 1-1 [3]. The equivalent circuits are used to analyze the complex circuits. One can understand the circuit operation better when the complex structures are simplified using equivalent circuits. For an analog circuit designer precise equivalent models of devices are essential for getting the near exact circuit performance and the one such model is given in reference [4].

1.4 Dissertation Outline

Chapter 2 provides a background review of the history, fundamental functions, and performance of Current Conveyors, The chapter giving an overview of the classification of Current Conveyors: 1st generation, 2nd generation and 3rd generation, them characteristics. The sort of CCs was according to X, Y, Z ports and to quiescent current too.

Chapter 3 goes through the design flow of CCII topology explaining strategy of CCII design, some circuit solutions for the implementation of CCII in CMOS technology to reach LV LP CCIIs investigated and simulated. A variety of CMOS operational amplifier can be converted into a CCII- using general method studied with examples.

Chapter 4 introduces low voltage technique, started with basic level technique to reduce power consumption and in the same time keeping or improving the circuit performance. Next, two new technologies in low voltage CMOS design studied to design CCII, Self-cascode and Bulk-driven.

Then novel CCII based Self cascode or Bulk-Driven design, designed and implemented, the behavior of the circuits was analyzed and simulated; comparison results with conventional circuits are tabulated then two filter circuits designed to prove the validity of low voltage CCII in analog functions.

2 Background

2.1 Current Conveyors

The concept of the current-conveyor was first presented in 1968 [1] and further developed to a second-generation current-conveyor in 1970 [2]. The current-conveyor is intended as a general building block as with the operational amplifier. Because of the operational amplifier concept has been current since the late 1940's, it is difficult to get any other similar concept widely accepted. However, operational amplifiers do not perform well in applications where a current output signal is needed and consequently there is an application field for current-conveyor circuits. Since current-conveyors operate without any global feedback, a different high frequency behavior compared to operational amplifier circuits results.

2.1.1 Classification of Current Conveyors

There are several schemes for classification of CCs. Most common techniques among them are based on the characteristics of its ports X, Y and Z. CCs have also been classified similar to power amplifiers based on the quiescent current flow.

2.1.1.1 Port Y based classification

Port Y is used as input for voltage signals and it should not load the input voltage source by drawing current. But in some applications, it is desirable to draw currents from the input voltage source.

When port Y draws a current equal to the current injected at port X, A = 1 according to equation 1.2, this configuration is termed as First generation current conveyor.

When port Y draws zero current (A = 0), it is Second generation current conveyor.

Similarly, when this current equals to the current injected at port X but of opposite polarity, the configuration is known as Third generation current conveyor for which A = −1 [3]-[7].

- **First Generation Current Conveyors – CCI**

Current-conveyors are three-port networks with terminals X, Y and Z as represented in Figure 2-1. The network of the first generation current-conveyor CCI has been formulated in a matrix form as follows [1]:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad 2.1$$

The first generation current conveyor CCI forces both the currents and the voltages in ports X and Y to be equal and a replica of the currents is mirrored (or conveyed) to the output port Z.

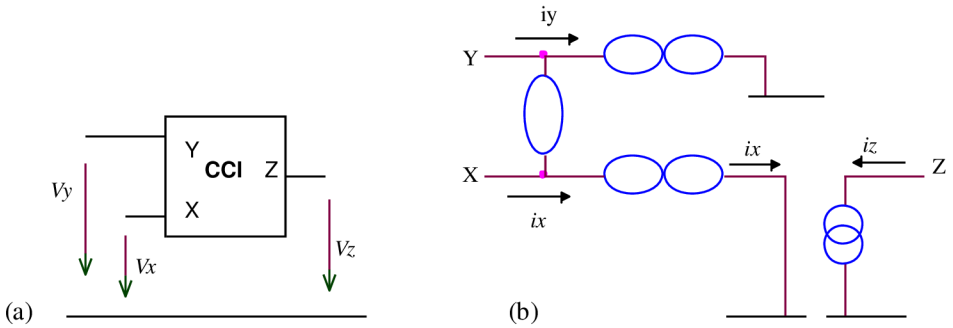


Figure 2-1: a) The first generation current-conveyor symbol and its signal definitions. **b)** Nullator-norator CCI complete scheme.

- **Second Generation Current Conveyor – CCII**

For many applications a high impedance input terminal is preferable and to increase the versatility of the current conveyor, which no current flows in terminal Y. For these reasons, the second generation current-conveyor was developed. It has one high and one low impedance input rather than the two low impedance inputs of the CCI [2].

This building block has since proven be more useful than CCI. CCII can be described by following matrix:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad 2.2$$

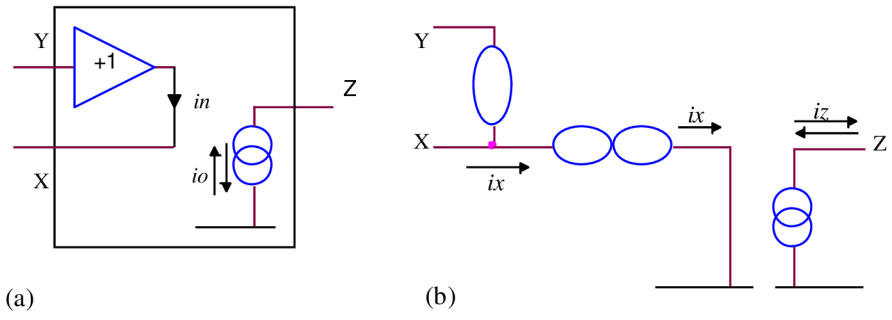


Figure 2-2: **a)** The principle of the second generation current conveyor: CCII+,iz=ix. CCII-,-iz=ix. **b)** Nullator-norator CCII complete scheme.

The current flowing into (CCII+) or out of (CCII-) the Z node is proportional to the current flowing into the X node.

The second-generation current-conveyor is a principle of voltage-follower with a voltage input Y node and a voltage output X node, and a current-follower (or current-inverter) with a current input X and a current output Z connected together Figure 2-2.

CCII has proven to be by far the more useful of the current conveyor family types. Wide range of applications was published. It's very suitable building block for design of the active-RC filters or number of special admittance converters. In the last decade the numbers of high-speed and wide-range op amps are based on current conveyor structure. And also for low voltage applications CCII is starting to be very powerful building block.

- **Third Generation Current Conveyor – CCIII**

Yet another current-conveyor was proposed in 1995 [3]. The network of this third generation current-conveyor CCIII is formulated in a matrix form as follows. This type is similar to CCI, there is opposite current transfer between X and Y terminal. Matrix described this CC type is following:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad 2.3$$

The input current flows into the Y-terminal and out from the X-terminal, one might think that a differential current input could be realized with this amplifier. However, the CCIII has high input impedance with common-mode current signals, i.e. identical currents are fed both to Y- and X-terminals. Therefore common-mode currents can push the input terminals out from the proper operation range. This current-conveyor can be used as an active current probe.

2.1.1.2 Port X based classification

For voltage signals, port Y serves as input port and now the port X serves as output port. The output voltage at port X can either have same polarity as that of the input voltage (V_Y) , in this case current conveyor is called as non-inverting CC. or that of opposite polarity , are termed as inverting CCs [8].

The inverting second generation current conveyor 'positive' (ICCII+), has the following port relation between terminal voltages and currents:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad 2.4$$

2.1.1.3 Port Z based classification

Port Z is the current output port and usually, the magnitude of the output current at port Z equals to the magnitude of the current injected into port X. In some cases, however, this amplitude may be scaled version (generally up scaled) of the input current and also the direction of the current may be same or opposite to that of the current in port X. CC with positive current output is termed as CC+ and with negative output currents as CC− [10].

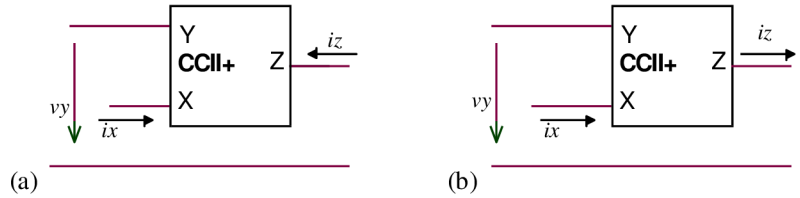


Figure 2-3 Positive and negative CCII basic blocks.

A CC can have two or more output ports, which can independently sink or source currents. Such a CC is known as multi port CC. A multi port CC with both types of output ports (positive as well as negative), is known as composite port CCII.

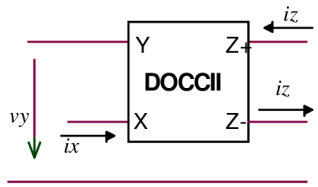


Figure 2-4 Dual output CCII basic block.

2.1.1.4 Quiescent current based classification

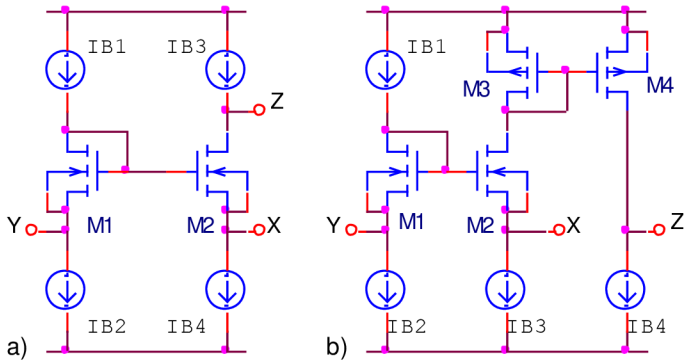


Figure 2-5 Class A CCIIs **a)** CCII- **b)** CCII+.

Similar to the classification of power amplifiers, CCs have been classified as Class A shown in Figure 2-5, Class B which rarely use due to strongly nonlinear characteristic and Class AB mode CCs shown in Figure 2-6. In a class A CC, a quiescent current flows throughout the circuit operation. The bandwidth of this CC is high. Contrary to this, in class B CC, current flows through the circuit only when the input signal is present. Such a circuit consumes negligible power in standby mode, but its bandwidth is much smaller compared to class A CCs. Class AB CCs have emerged as the best alternative, where a small amount of quiescent current flows throughout the circuit operations. Class AB CCs have higher bandwidth than that of a class B CCs and the power consumption is much less than a class A CC [11]-[14].

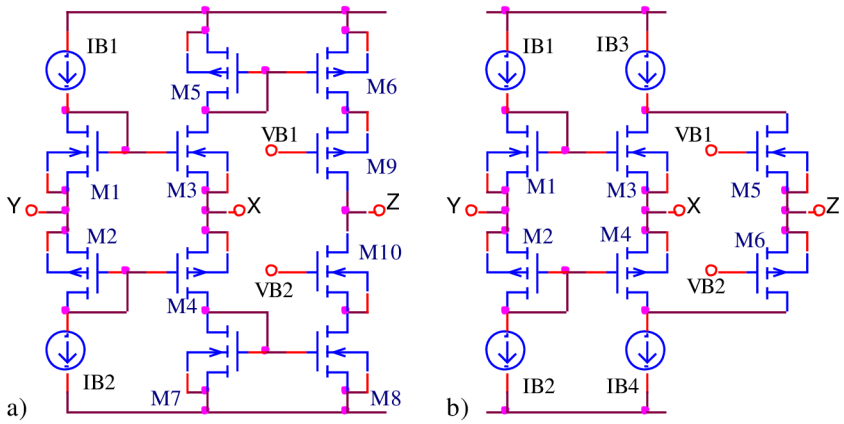


Figure 2-6 Class AB CCIIs: **a)** CCII+ and **b)** CCII-

2.1.1.5 Other CC configurations

Other CC configurations are electronically controlled current conveyors (ECCII),

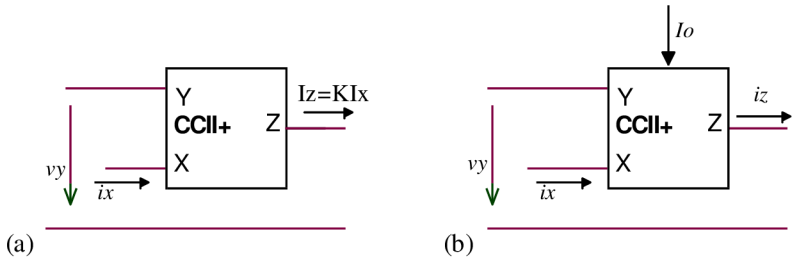


Figure 2-7 a) CGCCII basic block, **b)** CCCII basic block.

If Iz is designed K times higher with respect to Ix, the new block so implemented is named Current Gain Controlled Conveyor (CGCCII) and is shown in Figure 2-7a.

The designer can adjust the value of the x node parasitic impedance, the current Io may control the biasing of the output stage, so modifying the parasitic resistance rx, in Current Controlled Current Conveyor, or (CCCII) Figure 2-7b.

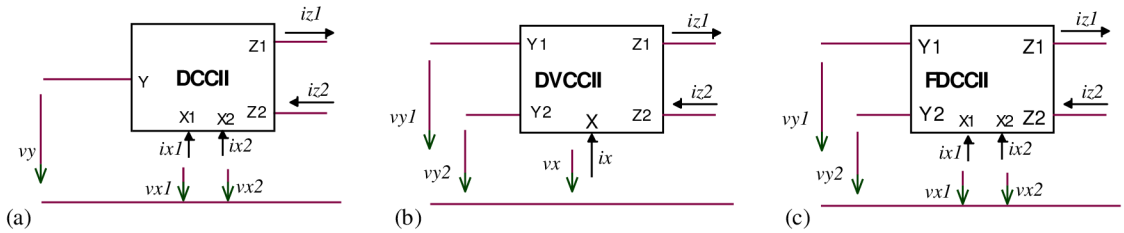


Figure 2-8: a) DCCII. **b)** DVCCII. **c)** FDCCII. basic blocks.

.

Deferential approach, leads to several circuit solutions such as shown in Figure 2-8 [9], the differential current conveyor is a powerful current mode building block with properties that make it ideal for designing all MOS analog circuits which can be integrated on a single chip. Differential current conveyors (DCCII) Figure 2-8a, differential voltage current conveyors (DVCCII) Figure 2-8b, fully differential current conveyors (FDCCII) Figure 2-8c [11]-[14]. There are some other variations structure [15].

2.1.2 CCII Applications

Because of the separate voltage and current inputs both voltage and current amplifiers can easily be realized with the second-generation current conveyors and the gain can be set by resistor ratios as in operational amplifier circuits. Signal processing in current-conveyor circuits is based on voltage-to-current and current-to-voltage conversions and on signal buffering by voltage and current buffers. Because there is typically no feedback in current-conveyor circuits, wide bandwidth operation without any slewing at large signal amplitudes is achieved. The conventional applications of CCs include amplifiers, oscillators, filters, wave shaping circuits, analog computers etc. [11], [15]. Low-voltage and low-power architectures of CCs are particularly suitable in the design of voltage and power starved systems.

2.1.2.1 Current Output Amplifier

The CCII can easily be used to configure the current output amplifiers, as shown in Figure 9.

Current amplifier can be performed through the use of a CCII Figure 2-9a, the input current is converted into an input voltage, applied to Y node. The X node voltage obtained in this way forces, into R2, a current which flows from high impedance Z node.

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} \qquad 2.5$$

V-I converter Figure 2-9b is an important circuit block in current code amplifier design.

$$I_z = g V_y \qquad 2.6$$

Current integrator is presented in Figure 2-9c.

$$I_{out} = \frac{I_{in}}{sCR} \qquad 2.7$$

Current differentiator is obtained, as pictured in Figure 2-9d

$$I_{out} = sCRI_{in} \qquad 2.8$$

Current Buffer or Current Follower, shown in Figure 2-9e The X node has a low input impedance and conveys the input current through to the high output impedance Z node. Hence the current gain is unity, negative for a CCII+ and positive for a CCII-.

current adder as depicted in Figure 2-9f is implemented simply connecting more than a current source to the low impedance input node X according to the fact in the CCII+, Iz=Ix.

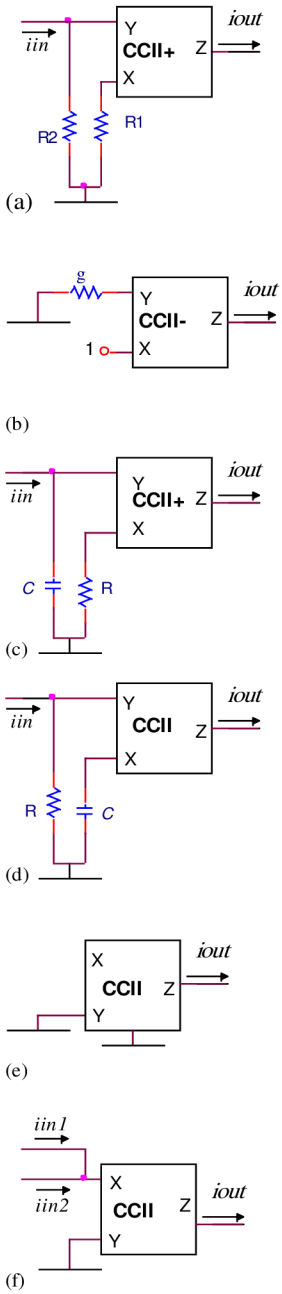


Figure 2-9 CCII-based current output amplifiers.

2.1.2.2 Voltage Amplifiers

Voltage amplification can be obtained by adding a voltage buffer to the VCCS of Figure 2.9b.

The voltage amplifier shown in Figure 2.10a is implemented through the use of two CCII blocks. The second CCII performs the buffering operation, so it can be avoided either when R2 resistance considered the load or with less value than load resistance.

$$V_{out} = \frac{R_2}{R_1} V_{in} \qquad 2.9$$

Voltage integrator is depicted in Figure 2.10b The second current conveyor ensures again the voltage buffer operation at the output.

$$V_{out} = \frac{1}{sCR} V_{in} \qquad 2.10$$

Voltage differentiator, also the passive elements can be swept to reach the design Figure2.10c.

$$V_{out} = sRCV_{in} \qquad 2.11$$

Voltage adder, as depicted in Figure 2.10d, input voltage are converted into currents through R1 and R2 resistors. The first CCII performs the current adder action seen before. Then, the output current is converted again into a voltage through the use of R resistor. In order to obtain low output impedance level, a second CCII has been used as a voltage buffer.

Instrumentation amplifier, by converting the output current back to a single-ended voltage, this differential transadmittance cell can be extended to produce a high performance instrumentation amplifier [17], [18], as shown in Figure 2.10e.

$$V_{out} = \frac{R_2}{R_1} V_{in} \qquad 2.12$$

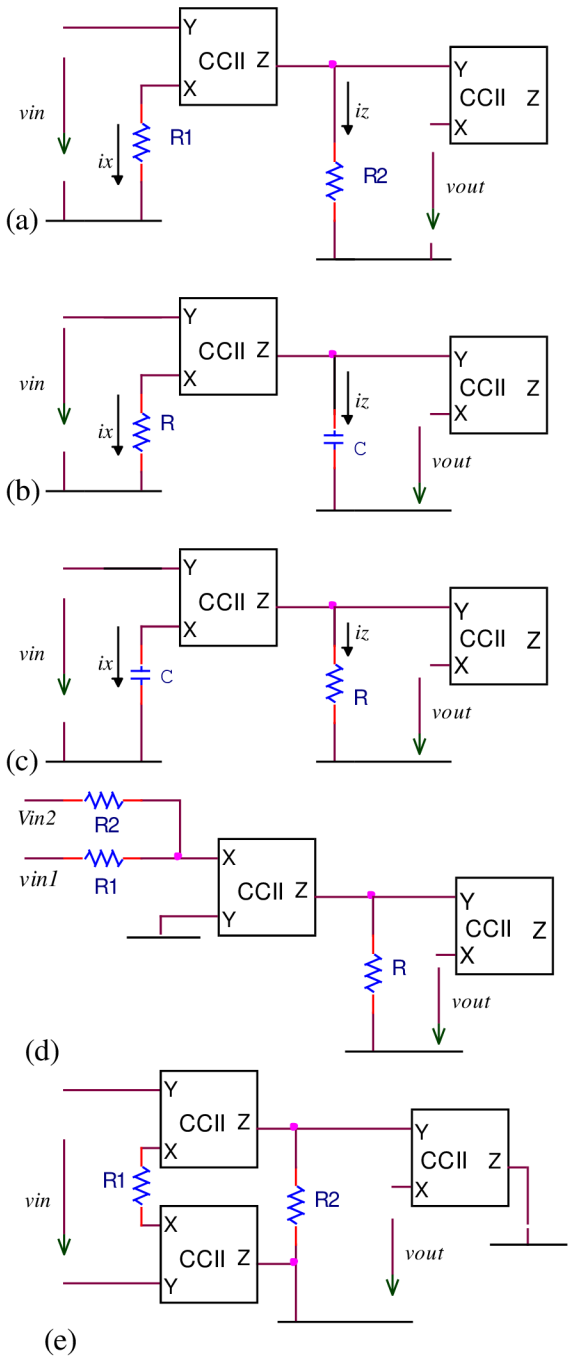


Figure 2-10 CCII-based voltage amplifiers.

2.1.2.3 Impedance Simulators.

Negative impedance converter, a simple circuit using a positive CCII has been reported Figure 2.11a, the current injected at X node will flow into Z impedance, so imposing a negative voltage at Y node. This value is also present at X node, where the equivalent impedance is equal to –Z, current controlled negative resistance.

$$Zin = \frac{V_X}{I_X} = -\frac{V_Y}{I_Z} = \frac{V_Z}{I_Z} = -Z \qquad 2.13$$

If a resistor R is connected between X and ground the input impedance of the port Y which is equal to -Z is a voltage controlled negative resistance Figure2.11b.

$$Zin = \frac{V_X}{I_X} = -\frac{V_Y}{I_Z} = \frac{V_Z}{I_Z} = -Z \qquad 2.14$$

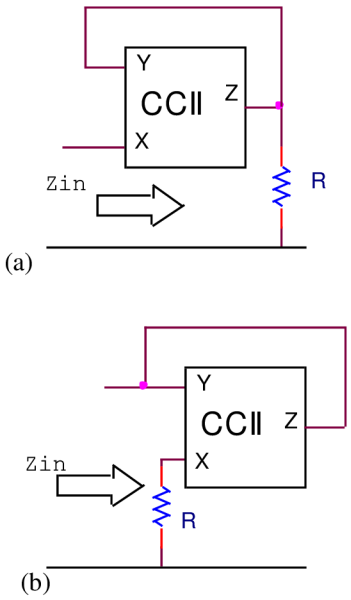


Figure 2-11 CCII-based impedance converter.

It is useful in some applications like oscillators.

Capacitance multiplier invented to substitute large capacitance, since large capacitance it needs large silicon areas in integrated applications, so using either external capacitance or designing circuits able to simulate the behavior of such passive components.

Capacitance multiplication can be performed by implementing high capacitance values from smaller ones. From Figure 2.12, if current flowing from Z node is K times greater than that flowing from X node, the impedance at X node is K times higher than that seen from Y node, as clarified by the following formulas:

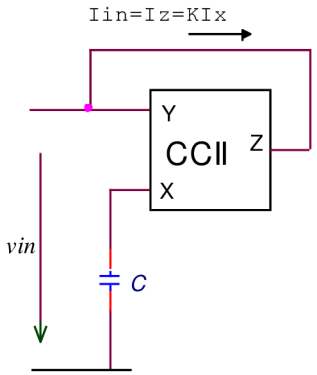


Figure 2-12 CGCCII-based capacitance multiplier.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{V_Y}{I_{in}} = \frac{V_Y}{I_Z} = \frac{V_Y}{KI_X} = \frac{V_Y}{K\frac{V_X}{Z_C}} = \frac{V_Y}{K\frac{V_Y}{Z_C}} = \frac{Z_C}{K}$$

$$Z_{in} = \frac{1}{sCK} \qquad 2.15$$

.

2.1.2.4 Oscillators and Filters

Current conveyor (CCII) has attracted the attention of researchers in the field of active filters and oscillators due to its distinct advantages over operational amplifier. This is attributed to their larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry and low power dissipation.

CCII- based Wien oscillator

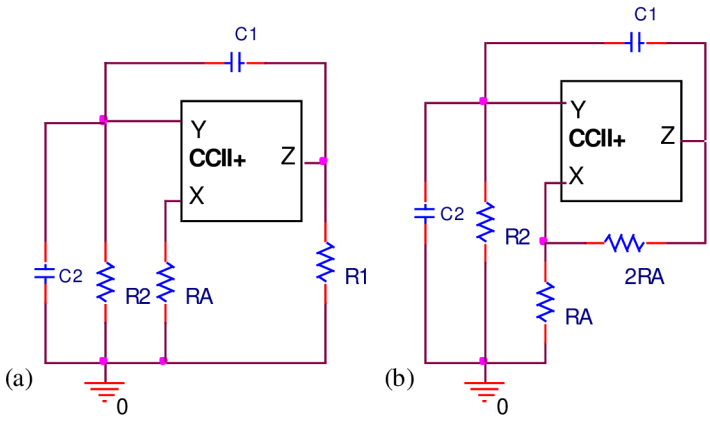


Figure 2-13 CCII-based Wien oscillators.

This one example from various circuits in literature [42], oscillation frequency and condition are the same, provided that the following relationships are verified:
Figure 2-13a:

$$R_A = \frac{R_1}{K} \qquad 2.16$$

Figure 2-13b:

$$R_A = \frac{R_1}{K - 1} \qquad 2.17$$

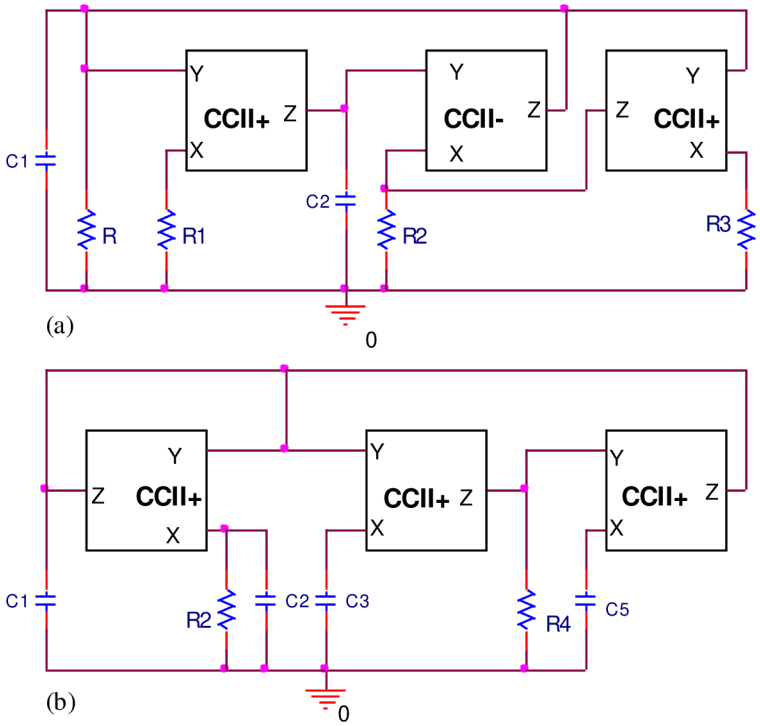


Figure 2-14CCII-based oscillators using passive components grounded.

All passive components grounded oscillator is depicted in Figure 2-14a.

Oscillation frequency

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}; R_1=R_2 \qquad 2.18$$

Resistors R or R3 utilized to control the oscillation without affecting the frequency of oscillation, since R1 or R2 controlling the oscillation frequency independently from the oscillation condition.

Other CCII oscillator shown in Figure 2-14b, using only positive CCII,

Oscillation frequency

$$\omega_0 = \frac{1}{\sqrt{C_3 R_4 R_2 C_5}}; C_1=C_2 \qquad 2.19$$

Dual output CCII based oscillator

Another possible oscillator can be implemented starting from dual output CCIIs and only grounded resistance and capacitance [45].

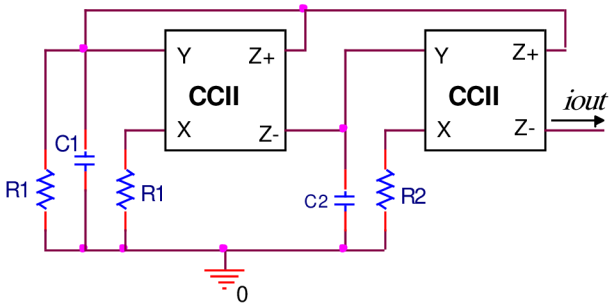


Figure 2-15 Dual output CCII-based oscillators.

In this case only two CCII blocks are needed Figure 2-15.The design equation for this oscillator is the following:

Oscillation frequency

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}; R_1=R \qquad 2.20$$

Operational amplifier based filter topologies can be converted to current conveyor based circuits by applying the adjoint principle, described in Section (1.2). An example of this is the Sallen-Key SAB (=single operational amplifier biquad) filter in Figure 2-16, which is converted to a CCII- based current-mode filter. However, in the voltage-mode circuit, the operational amplifier operates as a voltage follower and, as a result; its adjoint circuit element is a current follower. For this reason a second generation current-conveyor can by used as a replacement for the operational amplifier in a limited number of applications.

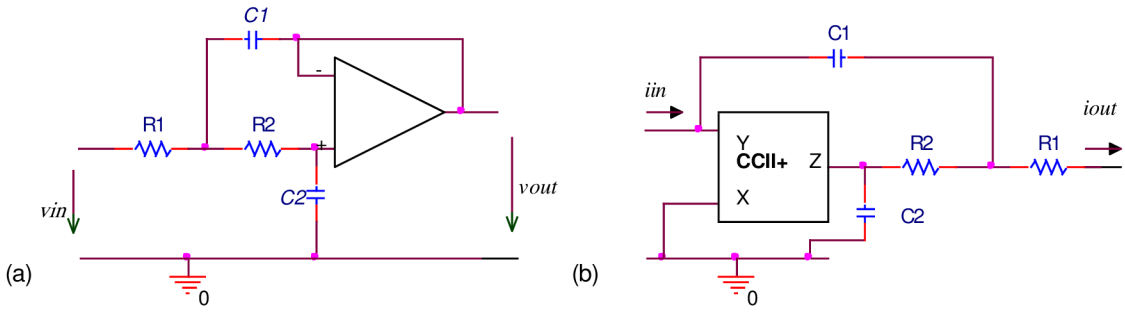


Figure 2-16 Sallen-key low pass filter implementations. (a) Voltage-mode filter using an op amp. (b) Current-mode filter using a current-conveyor CCII.

2.2 CCII Design and Characteristics

CCII-based topologies presented in the literature have been studied on how is possible to improve performance, reduce supply voltage and which effects this reduction has on CCII performance. This chapter goes through the design flow of CCII topology, some circuit solutions also presented, and then two circuit techniques used to construct novel topologies of CCII.

2.2.1 Current Mirror based CCII

Traditional nMOS current mirror shown in Figure 2-17 [16] can be seen as a CCII.

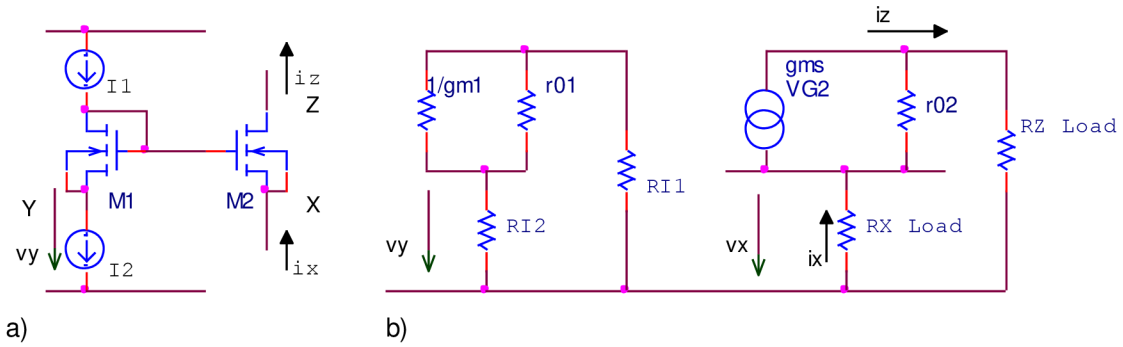


Figure 2-17 a nMOS current mirror. **b** small signal equivalent circuit.

Considering the circuit depicted in Figure 2-17, the voltage at gate of M2 VG2 determined as a function of the voltage at Y node VY:

$$v_{G2} = \frac{R_{I1}}{R_{I1} + \frac{r_{01}}{1 + g_{m1} r_{01}}} v_Y \cong v_Y \qquad 2.21$$

Concerning equation 2.5, the voltage at X node VX can be expressed as a function of the voltage at M2 gate and VG2=VY:

$$A_v = \frac{v_X}{v_Y} = \frac{g_{m2} r_{02} R_X}{1 + g_{m2} r_{02} R_X} \cong 1 \qquad 2.22$$

IX and IZ currents are equal, as cleared from the small signal equivalent circuit Figure 2-17 which is equal to one in this circuit:

$$A_i = \frac{i_Z}{i_X} = 1 \qquad 2.23$$

Impedance at Y node is given by:

$$r_Y = R_{I2} // \left(\frac{1}{g_{m1}} + R_{I1} \right) \qquad 2.24$$

X node impedance is affected by the load connected to Z node, while the impedance seen at Z terminal is related to the load connected to X node. X and Z impedances as following:

$$r_x \cong \frac{r_{02} + R_z}{1 + g_{m2} r_{02}} \cong \frac{1}{g_{m2}} \qquad 2.25$$

If $r_{02} >> R_Z$

$$r_z \cong r_{02} + (1 + g_m r_{02}) R_x \qquad 2.26$$

In Figure 2-18a negative CCII has been implemented. If a positive current conveyor is needed, it is possible to add a current mirror, as pictured in Figure 2-18b in this topology, IX and IZ flow in the same direction with respect to the CCII, so performing the CCII+ operation.

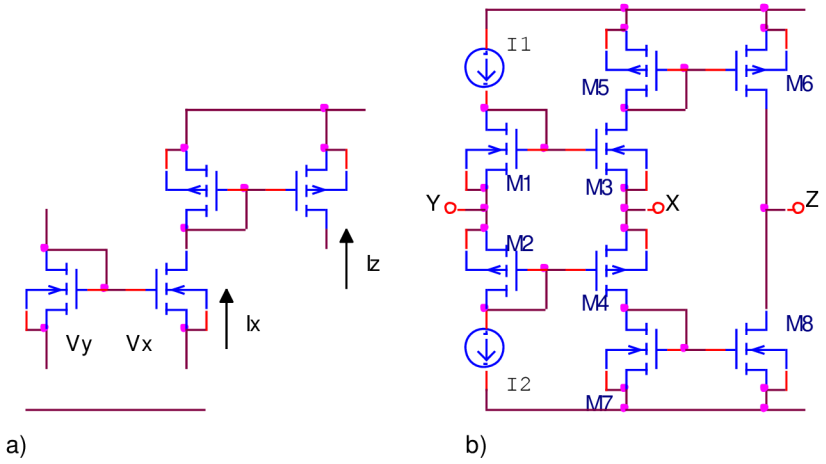


Figure 2-18 a) Current mirror used for positive CCII implementation.

b) Class AB CCII based on current mirrors.

The topology presented in Figure 2-18a can be doubled to obtain a class AB current conveyor, shown in Figure 2-18b. in this circuit, obviously, I1 and I2 have to be equal [15][17]. The input voltage VY is transferred to the output voltage VX of the follower

precisely by considering the product gm.ro much greater than 1, the voltage characteristic is very close to the ideal one:

$$A_v = \frac{v_y}{v_x} = 1 + \frac{1}{(g_{m3} + g_{m4})(r_{o3} r_{o4})} \cong 1 \qquad 2.27$$

The current mirrors (M5-M6) and (M7-M8) are transferring the current from the X terminals of the current conveyors to their Z terminals.

In this case, the quiescent current in all the branches is set by aspect ratios as expressed:

If $g_{m5}=g_{m7}$ and $g_{m6}=g_{m8}$

$$A_i = \frac{i_z}{i_x} \cong \frac{g_{m3} g_{m6} g_{m7} + g_{m4} g_{m5} g_{m8}}{g_{m5} g_{m6} (g_{m3} + g_{m4})} = 1$$

or

$$A_i = \frac{i_z}{i_x} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_5} = \frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_7} \qquad 2.28$$

If current gain will be set to 1, the circuit will operate as current follower.

The input resistance is:

$$r_x \cong \frac{1}{g_{m3} + g_{m4}} \qquad 2.29$$

The impedance seen at Z node is typically high and given by:

$$r_z \cong \frac{r_{o7} r_{o8}}{r_{o7} + r_{o8}} \qquad 2.30$$

AB current mirror current conveyor shown in Figure 2-18b was modified as shown in

Figure 2-19, this was simulated and the values were summarized in Table 2-1. The main advantage of this circuit, the CCII has a wide bandwidth obtained with relatively low biasing currents. Its drawback is represented by the limited dynamic range because of:

$$V_{\min} = V_{THP} + V_{THN} + 2V_{DSAT} \qquad 2.31$$

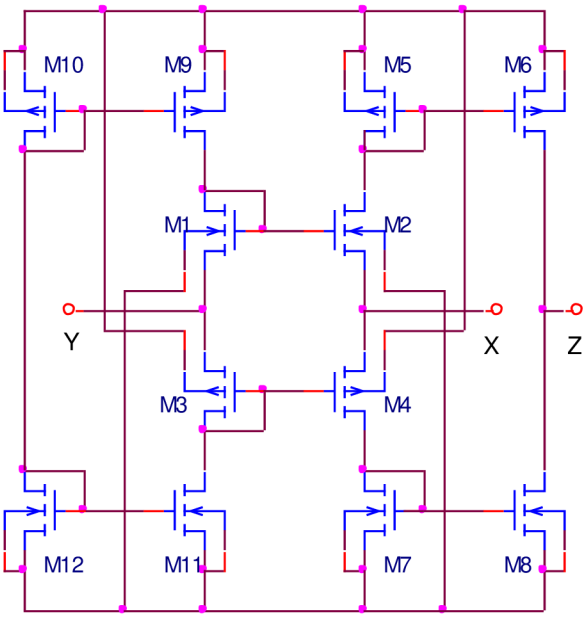


Figure 2-19 CCII based CM characteristics

Data	Value
Voltage Supply	± 2.5 V
Power Consumption	95µW
3dB Bandwidth	200MHz
Dynamic Range	-180mV, +180mV
Node X Parasitic Impedance	2.5 KΩ
Node Z Parasitic Impedance	850kΩ

Table 2-1 CCII based CM characteristics

The following simulation presented in Figure 2-20 affirming last results.

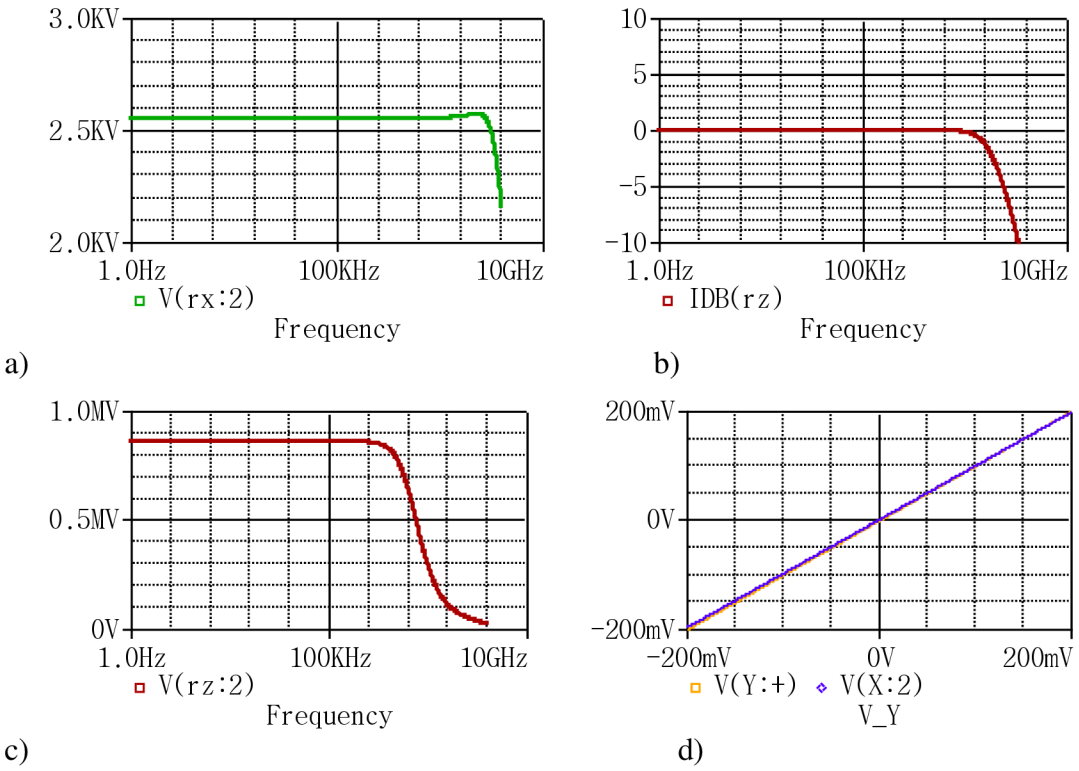


Figure 2-20: CCII-based CM simulation. **a)** input resistance rx. **b)** current transfer ratio iz/ix. **c)** output resistance rz. **d)** Y node X node voltages.

2.2.2 Differential pair based CCII

In literature, a large number of current conveyors utilizing a differential pair which realizes through a feedback connection the input voltage buffer [20].

The first design step in these circuits concerns the differential pair Figure 2-21

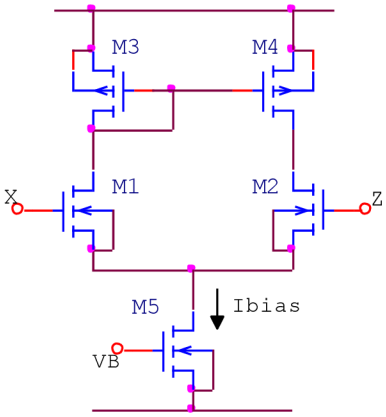


Figure 2-21 Differential pair.

For LV LP applications, a special attention to the supply values of current sources, it is fundamental to guarantee signal dynamic and a constant bias current independent from supply voltage.

The choice of biasing current is one of the important keys to power consumption, differential pair transistor sizes, and X node parasitic impedance, after implement the current source have to set M1-M4 sizes,

Class A CCII based on differential pair solution has been proposed in order to lower the supply voltage Figure 2-22a.

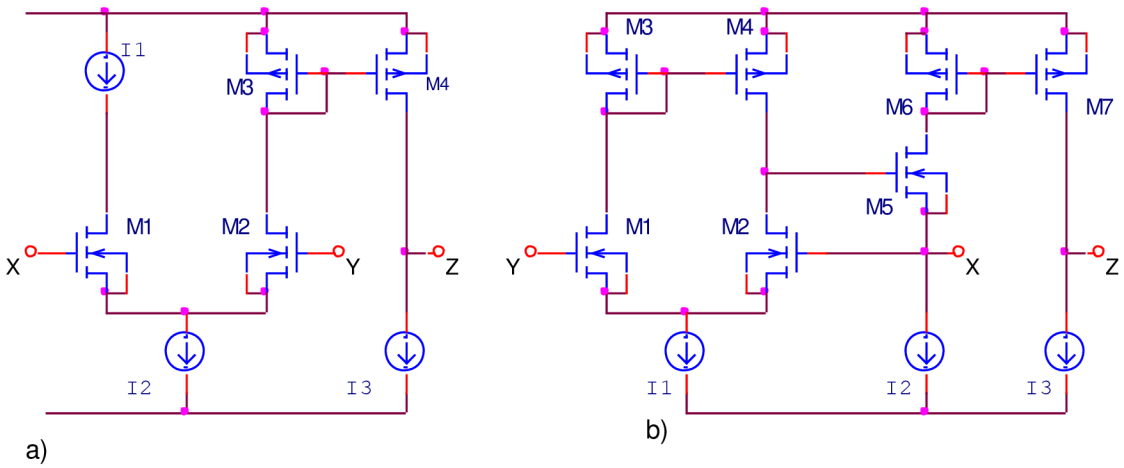


Figure 2-22 a) Class A CCII based on a diff. pair. **b)** Improved CCII based on a differ. Pair.

To improve performance, a feed back connection at X node provides the low impedance Figure 2-22b, since the input voltage buffer is related to gm1 and gm2 values which have to be equal. In this circuit, the feed back connection at X node can be performed by a nMOS transistor, current mirror M6, M7 is used to sense the current flowing from X node and to mirror it to the high impedance Z node.

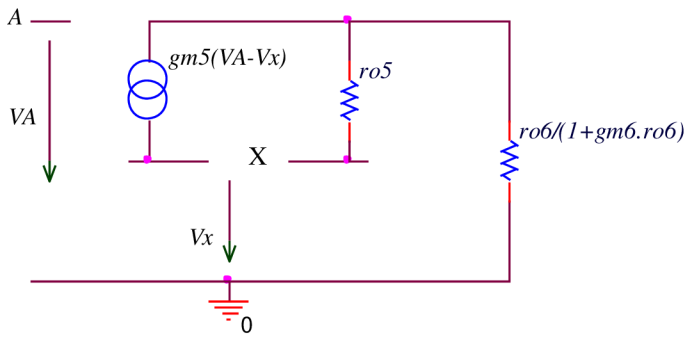


Figure 2-23 small analysis equivalent circuit

From the analysis of the circuit in Figure 2-22b, Figure 2-23 and by assuming M1-M4 have the same value, the Y node and X node voltage parameters it's very close to the ideal unitary value:

$$Av \cong \frac{g_{m1}}{g_{m2}} \qquad 2.32$$

By neglecting the equivalent resistance of the biasing currents I2 and I3, current inverter parameters have the expression:

$$Ai \cong \frac{g_{m7}}{g_{m8}} \qquad 2.33$$

Impedance at X node has been evaluated grounding Y node,

ro1=ro2=ro3=ro

$$r_x \cong \frac{1}{g_{m5}(1+\frac{r_0}{2}g_{m2})} \cong \frac{2}{g_{m5}r_0 g_{m2}} \qquad 2.34$$

$$r_z = \frac{r_{07}R_{IBIAS3}}{r_{07}+R_{IBIAS3}} \qquad 2.35$$

The differential pair permits to have high Y node impedance that is independent from the biasing current resistance.

$$r_y = \gamma WLC_{OX} \qquad 2.36$$

To reduce input impedance at X node, another circuit has been proposed in Figure 2-24a by connecting X node directly to M5 transistor drain to implement feed back, this circuit shows improved characteristics at lower supply voltages[21][23]. But the stronger limitation of this solution is class A operation, since the output stage designed

only from one kind of MOS transistors, the dynamic range is very limited, for this reason class AB has been implemented.

X node impedance of Figure 2-24:

$$r_x \cong \frac{1}{\frac{1}{r_{O5}} + g_{m2}\frac{r_0}{2}g_{m5}}$$

$$\cong \frac{2}{g_{m2}r_0 g_{m5}}, r_o = r_{o1} // r_{o3} \qquad 2.37$$

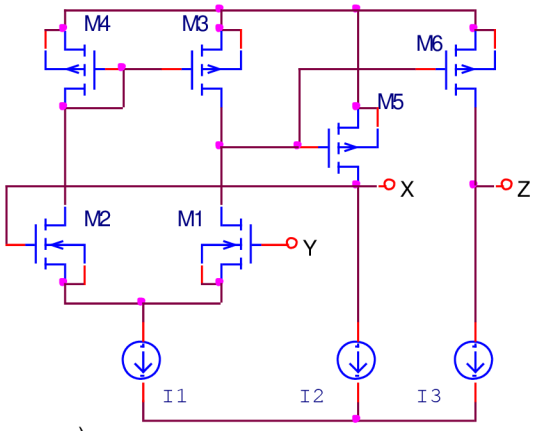
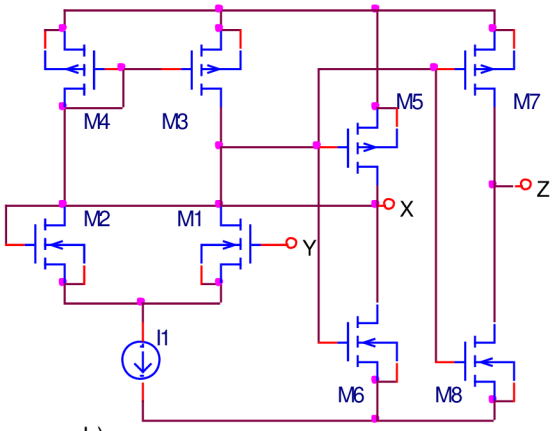


Figure 2-24 a) CCII based on diff. pair



b) Class AB CCII based on diff. pair

The circuit introduced in Figure 2-24a can be easily modified to obtain class AB current conveyor shown in Figure 2-24b, simply replacing the biasing sources with inverter output stages. Electrical parameters expressed as:

$$r_z \cong \frac{r_{O7}r_{O8}}{r_{O7}+r_{O8}} \qquad 2.38$$

$$A_i \cong \frac{g_{m8}+g_{m7}}{g_{m6}+g_{m5}} \qquad 2.39$$

$$r_x \cong \frac{2}{g_{m2}r_O\left(g_{m5}+g_{m6}\right)} \qquad 2.40$$

The simulation of the circuit shown in Figure 2-24b represents the total supply voltage reduced to 1.2 V.

In this case the minimum voltage supply is

$$V_{\min} = V_{THN} + 2V_{DSAT} \qquad 2.41$$

2.2.3 Current Conveyor based on Operational Amplifier Design

Standard operational amplifier is used to implement the unity gain buffer between the Y and X inputs Figure 2-25. The X input current i_x, is sensed by simply duplicating the buffer's output transistors MN and MP using transistors M1 and M2, and extracting the X current from them as i_z. Since transistors M1 and M2 have the same size and gate-source voltage as the output stage transistors MN and MP, the current i_z should be a copy of the current flowing through MN and MP which is i_x. Since no additional transistors need to be inserted between the operational amplifier and the supply rails, the approach will not increase the minimum operating voltage over that of the operational amplifier core. In addition, the voltage follower is based on an operational amplifier and so will maintain all the benefits (and disadvantages) of such a circuit (a good voltage follower at the cost of lower bandwidth) [1], [2], [24], [24], [1].

Variety of CMOS operational amplifier can be converted into a CCII- using this general method. Since the unity gain buffer is implemented as a two stage amplifier, for almost all practical implementations, a compensation capacitor will be required to ensure stability. The addition of the compensation capacitor potentially disrupts the current transfer from i_x to i_z. At high frequencies and beyond the unity gain bandwidth of the buffer, some of the i_x current will be lost to compensation capacitor C_c as well as to parasitic node capacitances. Our contribution is study the frequency characteristics of an operational amplifier derived CCII-. It will be shown that the current conveyor formed in this way inherits the characteristics of the core operational amplifier. Thus the results can be used to predict the frequencies at which the magnitude of the input impedance at port X begins to increase and the magnitude that the current transfer ratio begins to deviate significantly from unity [27].

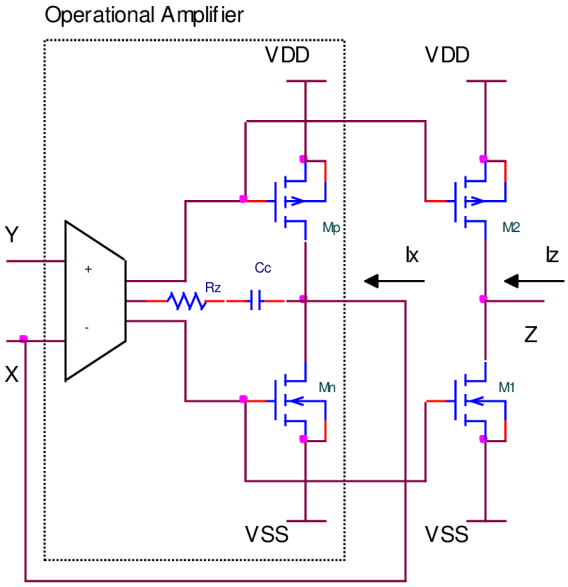


Figure 2-25 CCII based on an operational amplifier

2.2.3.1 Simulations of CCII Topologies

To verify the results a Miller two stages compensated operational amplifier along with a selection of designs of operational amplifiers from the literatures were used to make the buffer required in the transformation process to the CCII- [1][2]. Simulations were

carried out with orcade 9.2 using 0.7 µm CMOS process model from AMIS were all the operational amplifiers designed to work with a ±2V supply.

Figure 2-26 shows the simulated of the Miller compensated two stage operational amplifier based current conveyor in terms of the current transfer ratio iz/ix and the input resistance of the X terminal rx. The current transfer ratio stays at 0dB indicating the value of | iz/ix | to be unity until approximately the unity gain bandwidth is reached as presented in Figure 2-27. This reveals that the circuit exhibits a good degree of accuracy in its current following capability as is expected of a current conveyor. Also the simulated input resistance rx as expected good response until the unity gain bandwidth is reached which reveals the effect of Rx on current transfer ratio.

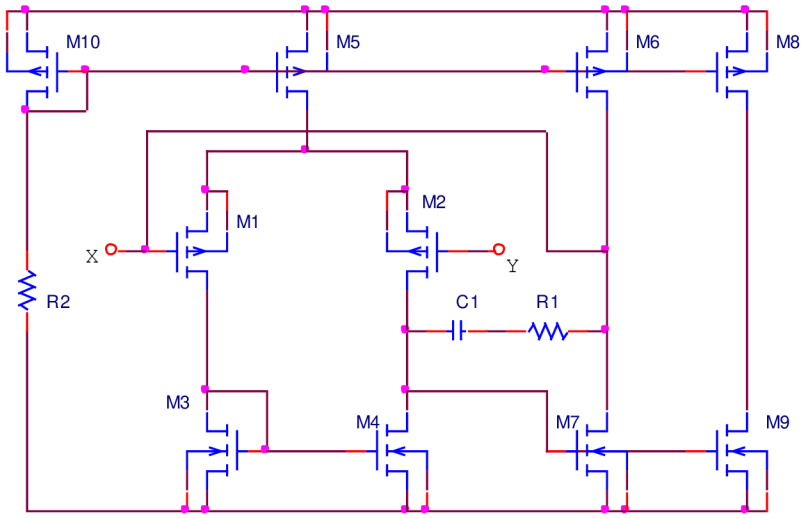


Figure 2-26 CCII- based on the Miller compenstaed operational amplifier.

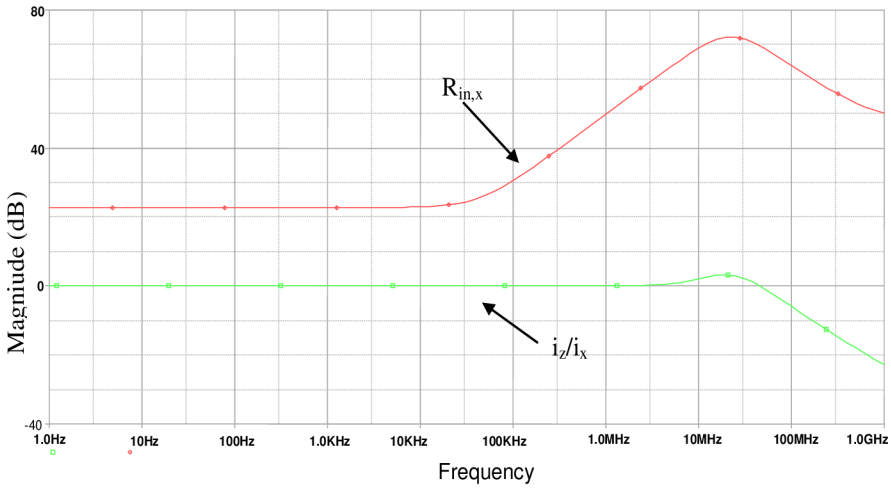


Figure 2-27 simulation of iz/ix and rin,x, in dB is normalized to 1 ohm.

Several other types of operational amplifiers, the push-pull operational amplifier, the cascode output operational amplifier and the Class AB operational amplifier were used to implement the required buffer for the CCII- and were used to verify the general validity of the conclusions concerning small signal analysis. The class AB operational

amplifier does not use a differential pair at the input and has a relatively low open-loop gain, which results in rx being big. The cascade example used has relatively low first stage gain with the majority of the gain obtained from the output stage, a high significant rx comparable to the class AB operational amplifier design.

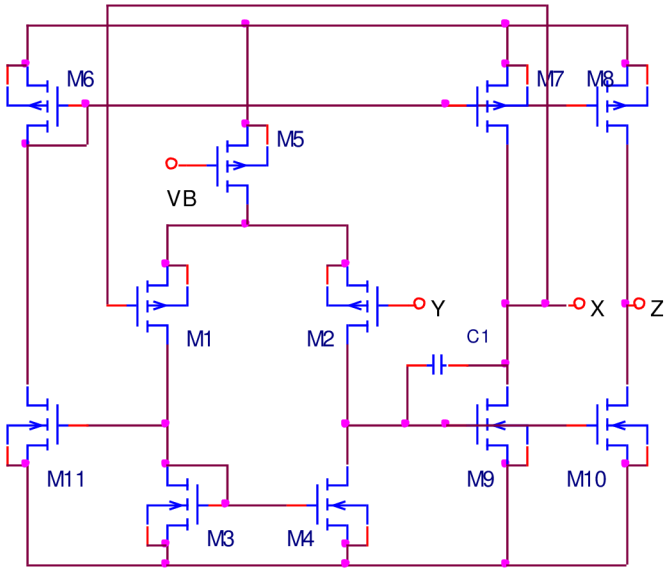


Figure 2-28 push pull op amp.

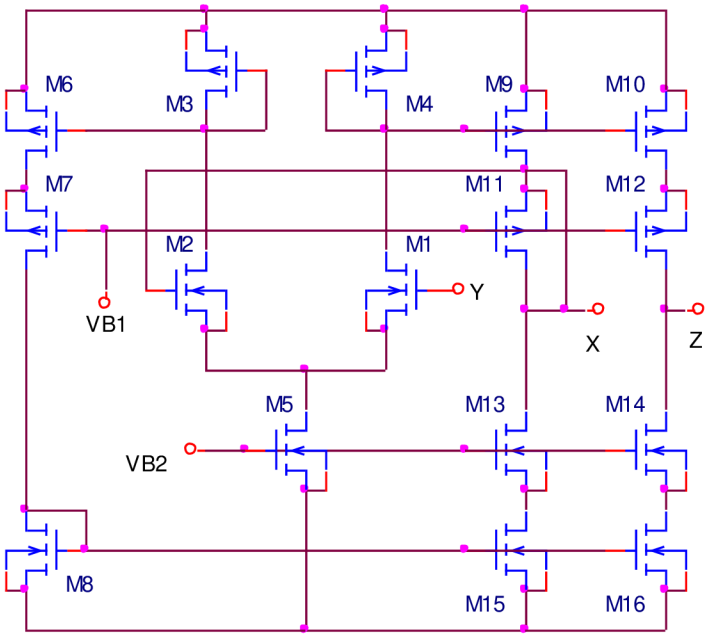


Figure 2-29 cascode output op amp.

The circuit schematics are shown in Figure 2-28, Figure 2-29, Figure 2-30 and the simulated results shown in Figure 2-31 for the current transfer ratio approving that the method works well with the other types of operational amplifiers since the current transfer ratio obtained is of unity value until around the unity gain bandwidth. Figure 2-32 showing the X terminal's input resistance obtained from the current conveyor made from these three types of operational amplifier, r_x of class AB and cascode output type

having a relatively higher rx but nevertheless still low in comparison with the impedance of the Y terminal.

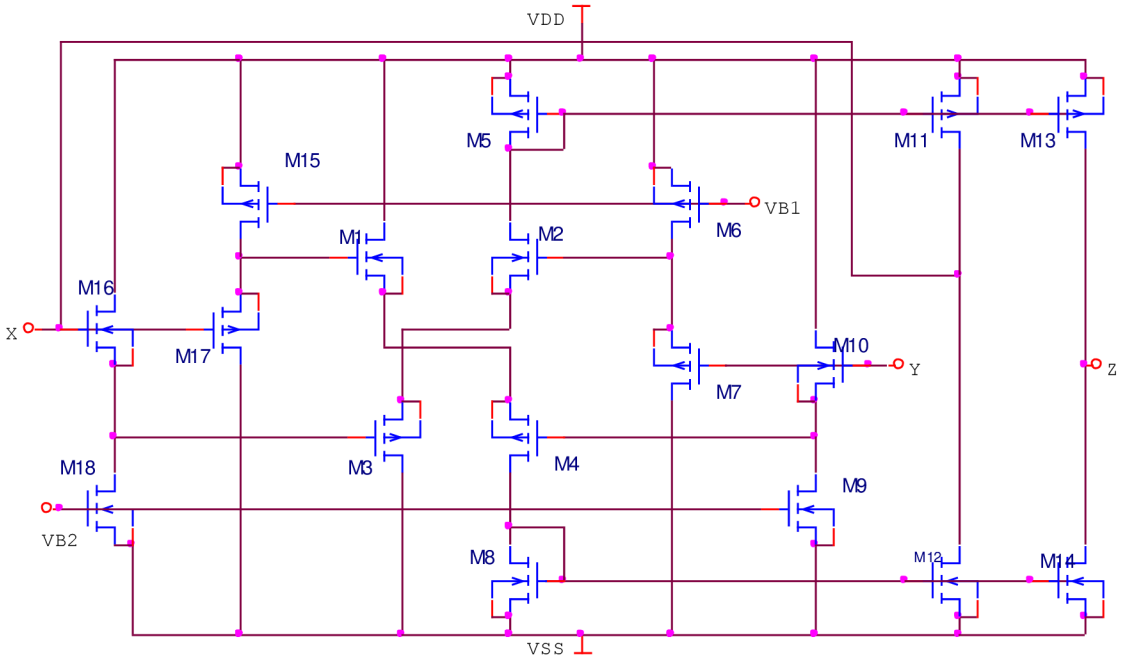


Figure 2-30 class AB op amp.

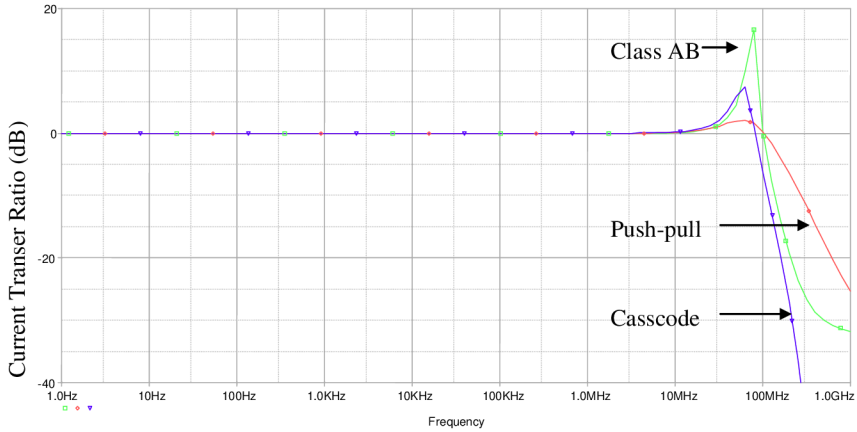


Figure 2-31 Transfer function for class AB, output cascode, push-pull.

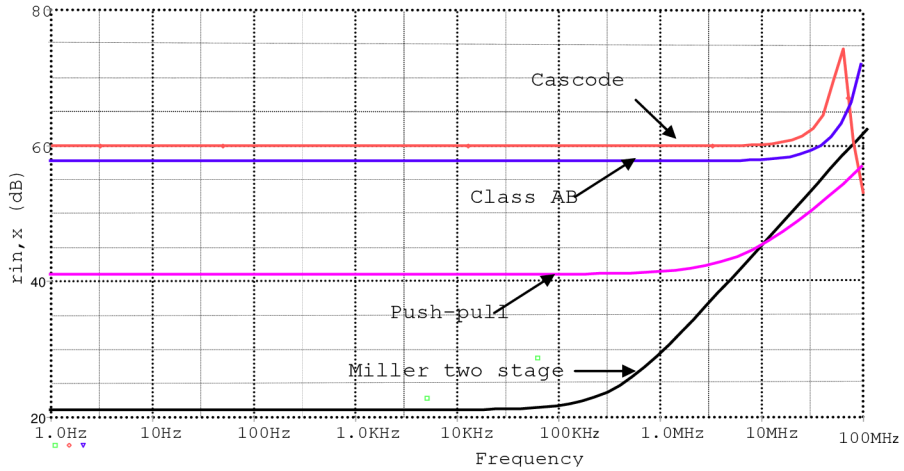


Figure 2-32 The X terminal input resistance for the Miller Compensated two-stage, Class AB, Push-pull and cascode output. Note rx in dB is normalized to 1 ohm.

Let us see the following circuit Figure 2-33 [33][42]which is able to operate at only 1V total supply voltage, the lower supply voltage has performed through the improvement of a different biasing circuit for X and Z output stages, the output stages in this circuit not dependent on supply voltage.

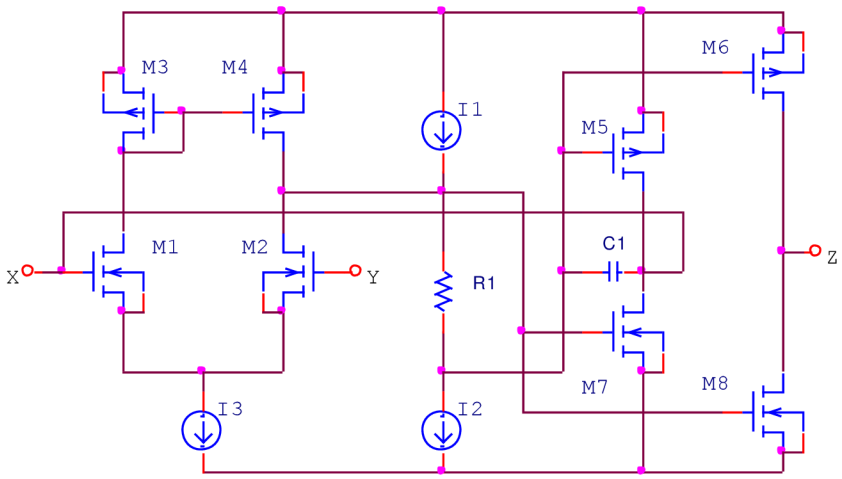
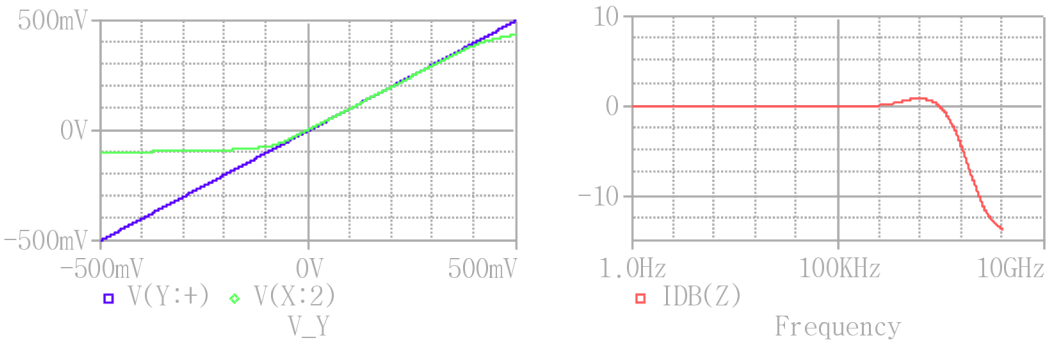


Figure 2-33 Class AB CCII with improved biasing.

There is a limitation for dynamic range at negative voltages, because X node voltage level cannot follow Y node as shown in Figure 2-34, since this CCII is based on a n-type differential pair, the dynamic range is more extended towards the positive voltages (-80mv to 350mv).



a) Vy and Vx voltages. **b)** Current transfer ratio iz/ix in dB.

Figure 2-34 Class AB CCII with improved biasing simulations.

It's possible to find similar results considering the solution based on the complementary p-type differential pair Figure 2-35, more over , the designer must take into account the fact that each supply voltage used cannot have lower than one threshold voltage PMOS transistor (the PMOS transistors have a threshold voltage about 0.8V in AMIS 0.7 um CMOS technology).

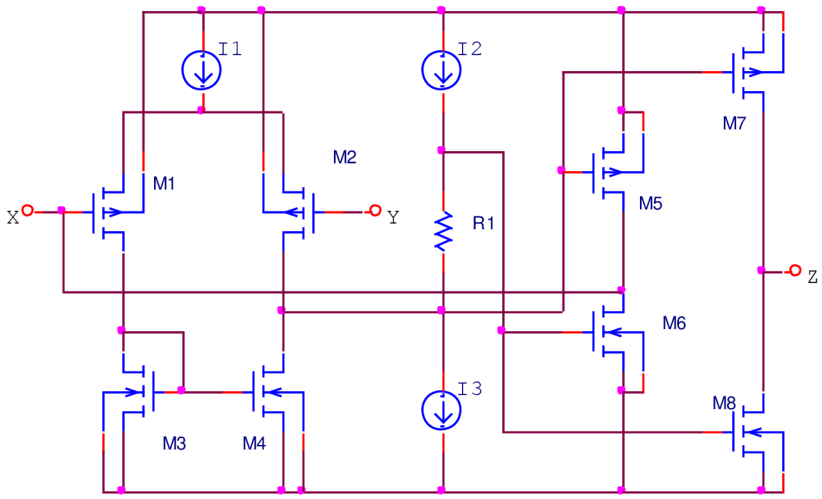
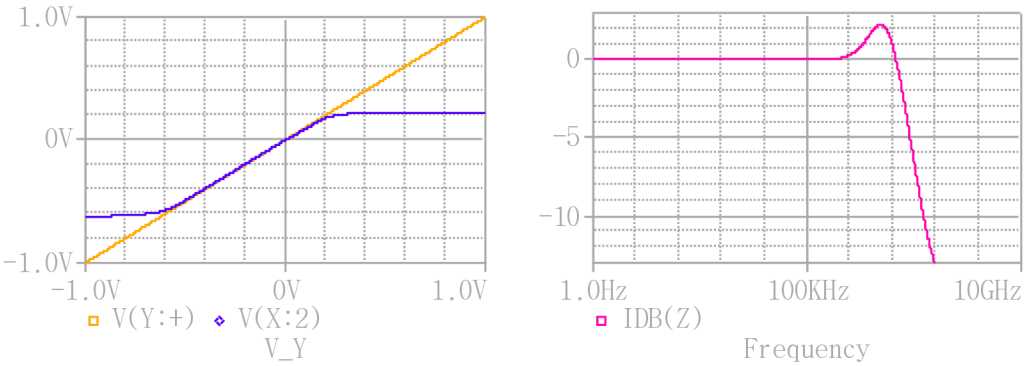


Figure 2-35 Class AB CCII based on p-type differential pair.



a) Voltage follower between Xnode and Ynode.

b) Current transfer between xnode and z node.

Figure 2-36 Class AB CCII based on p-type differential pair.

The two last topologies can be merged together to design a rail to rail CCII, as seen in Figure 2-37 [33], the basic concept is to use both differential pairs, the n-type based and p-type based, connecting the two single ended outputs to the gates of output stages.

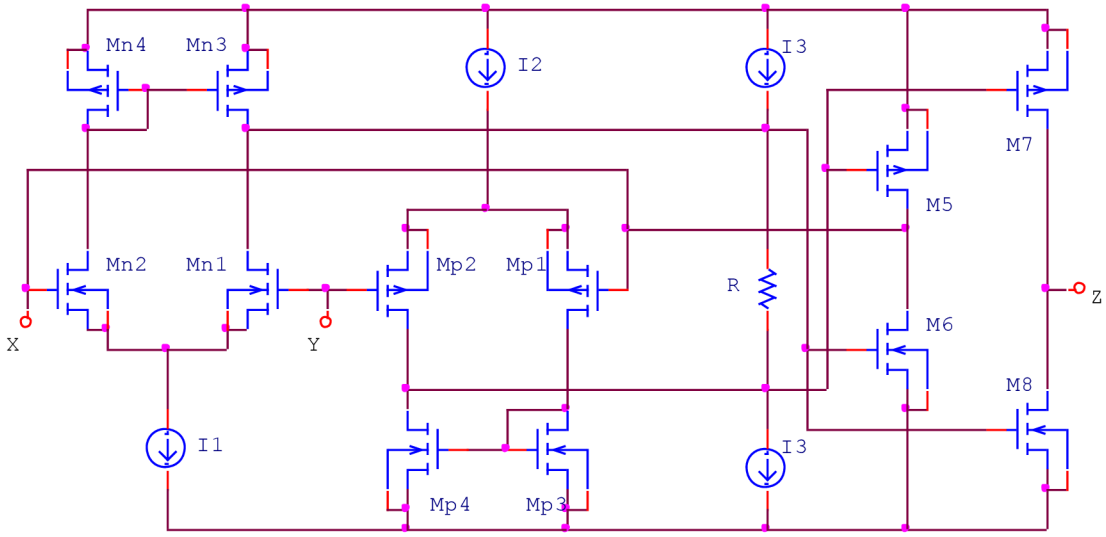
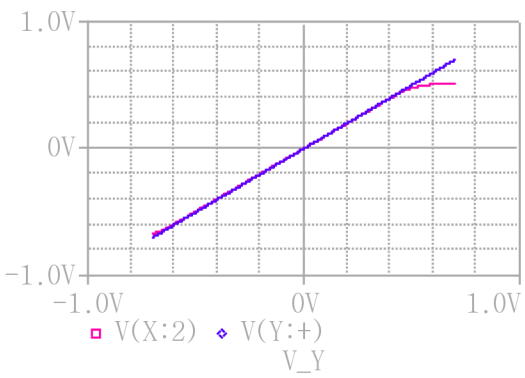
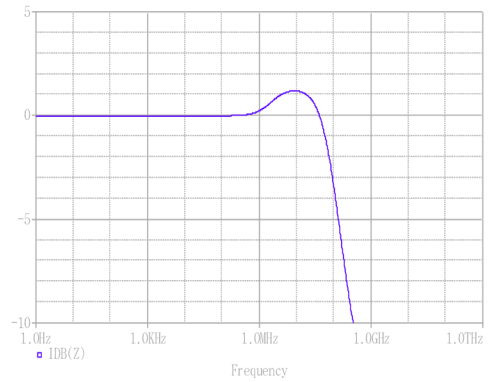


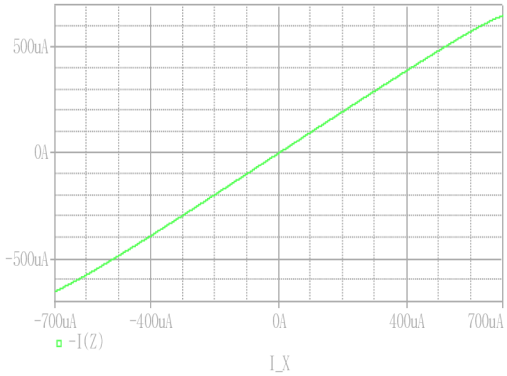
Figure 2-37 LV rail to rail OTA based CCII.



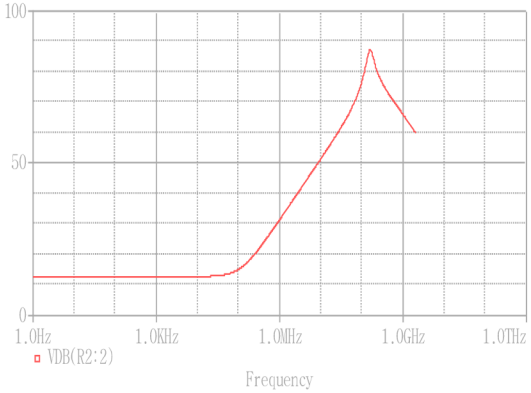
a) Vy and Vx voltages.



b) Current transfer ratio.



c) Current linearity in output node.



d) x node parasitic impedance.

Figure 2-38 LV rail to rail OTA based CCII simulation.

By placing the two complementary pairs in parallel, it has been possible to design a rail to rail OTA based CCII, which shows good performance at LV supplies. The voltage follower extended to both positive and negative directions (-600mV, 550mV) with 80MHz current transfer ratio, low input resistance 12Ω, and excellent current linearity between x and z nodes, simulation results shown in Figure 2-38.

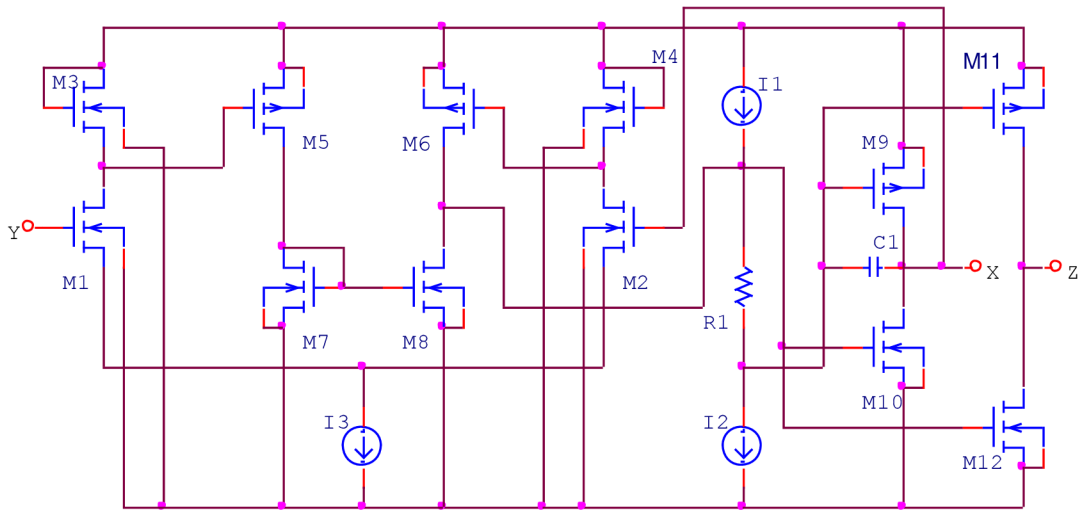


Figure 2-39 LV OTA based CCII.

Another Second generation current conveyors[42] are implemented starting from an OTA topology, using gained output stages (class AB inverter) and applying a proper feedback, as shown in the schematic in Figure 2-39 which is able to operate at value ±

1V supply voltage level. For this CCII, A_v and A_i parameters are given by the following expressions.

$$A_v = \frac{V_X}{V_Y} \cong \frac{g_{m1}}{g_{m2}} \cong 1 \qquad 2.42$$

$$A_i = \frac{I_Z}{I_X} \cong \frac{gm11 + gm12}{gm9 + gm10} \cong 1 \qquad 2.43$$

The parasitic impedance levels at X and Z nodes are

$$r_x \cong \frac{2}{g_{m2}(g_{m9} + g_{m10})} \qquad 2.44$$

$$r_z = \frac{r_{O11} r_{O12}}{r_{O11} + r_{O12}} \qquad 2.45$$

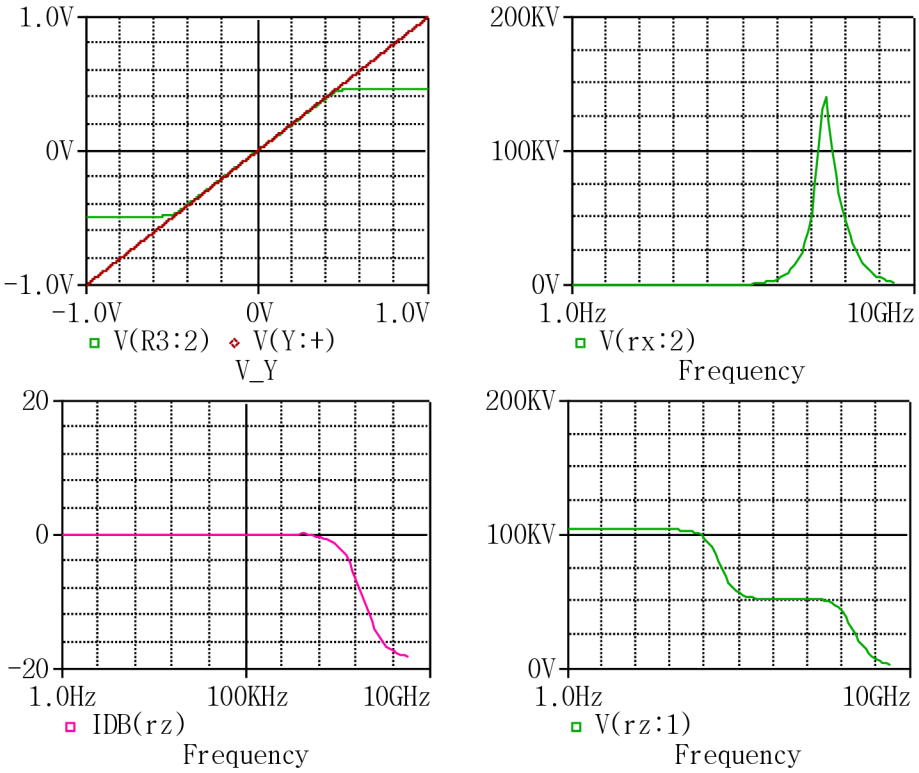


Figure 2-40 LV OTA based CCII simulations.

This circuit is solution for low voltage supply, it showing acceptable characteristic, dynamic range is -380V to 210V Figure 2-40.

3 Aims of the work

The goal of this thesis is to explore the implementation of second generation current conveyors using CMOS processes. To contain the scope of the present work, we will focus on challenge of power consumption related to the design of the CCII.

The design of low voltage CCII is a challenging task, not only to meet stringent performance requirements, but to do so efficiently. Often the circuit requirements push the devices, transistors in particular, near their performance limits. At the same time, cost, and the economy of time-to-market require the design process to be highly efficient.

This work focuses on developing analog circuit techniques that are compatible with future CMOS technologies with out ignoring the basic device level techniques which also play important role in the design of smarter and efficient circuits.

The first is the new technique, which does not require high compliance voltages at output nodes, it provides high output impedance to give high output gain and so it is useful in low-voltage design, called self-cascode. The second is removes the threshold voltage requirements and the device can be operated at low supply voltages, called bulk-driven technique.

These techniques are used to design and construct CCII, their performance characteristics are discussed here and a comparison with the conventional techniques has been presented.

Finally, we want to remark that, for LV applications, the current-mode approach can be a valid alternative to traditional circuits to obtain high performance architectures, because the designer is concerned with current levels for circuit operation instead of node voltages. In this manner, as well known, the gain-bandwidth product limitation, typical of operational amplifiers, is overcome.

4 Work Progress

4.1 Low Voltage Techniques

The reduction of the total supply voltage in CMOS integrated circuits has forced analog designer to find solutions able to operate in a wide supply range in order to obtain an acceptable signal to noise ratio.

There are three possible approaches to achieving high performance analog circuits in CMOS technology at low power supply voltages. One is to multiply the lower voltage dc to larger values. Another is to modify existing CMOS technologies to accommodate low-voltage analog circuits. A third is to develop new circuit techniques that achieve this objective with existing technology.[28], [38].

This work illustrates the application of the third approach, the advantages are that it is efficient and can be used without the need for costly process development.

4.1.1 Low biasing current design

Normally the CCII-based Current Mirror topologies have to set to the minimum operating supply voltage related to the drain-source (saturation) voltage required by the biasing transistors, which has to be minimized to reduce the supply voltage.

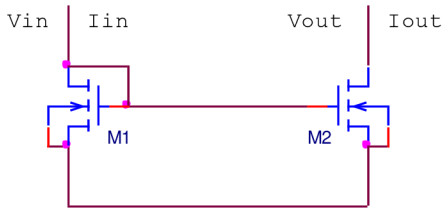


Figure 4-1 nMOS current mirror

The basic current mirror shown in Figure 4-1 is the same if transistor works either in saturated or sub threshold region; the output current is approximately related to input current according to the transistor W/L ratios.

Due to MOS output characteristics, only when the output voltage is greater than the saturation voltage, this transistor behaves like a current generator.

Its transconductance (gm1) decides the input impedance (Rin) of the CM. For this structure Vin is given as

$$V_{in} \cong V_{TN} + \sqrt{\frac{2I_{in}}{\beta_i}} \qquad 4.1$$

$$V_{out} = V_{DS}(sat), R_{out} = r_{o2}.$$

To obtain higher impedance it's possible to utilize a cascade structure, as shown in Figure 4-2 [39].

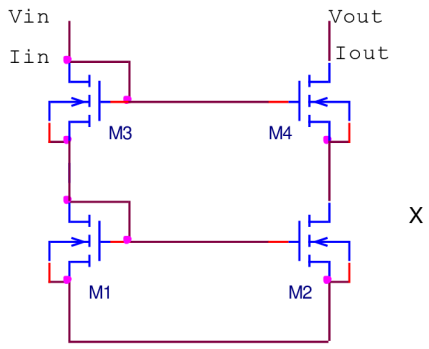


Figure 4-2 nMOS cascaded current mirror.

$$V_{in} \approx 2V_{TN} + 2\sqrt{\frac{2I_{in}}{\beta_i}} \qquad 4.2$$

$$Vout\ \min = 2VDS\,(sat), Rout = gm4ro4ro2$$

The solution reported in Figure 4-2 allows to improve only the output impedance level, but the minimum operating voltage, given by $2V_{TH}$.

An enhanced current mirror capable of operating with lower supply voltage or performing higher swings is reported in Figure 4-3 [39][41].

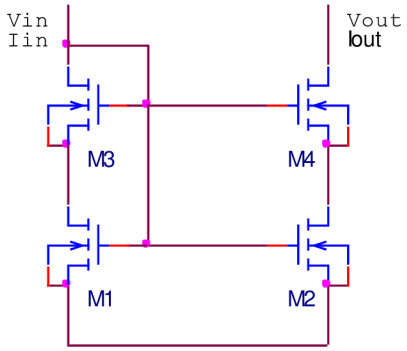


Figure 4-3 Low voltage cascaded current mirror.

$$V_{in}\ \min = V_{TH}$$
$$V_{out}\ \min = 2V_{DS}\,(sat) \qquad 4.3$$
$$R_{out} = g_{m4} r_{o4} r_{o2}$$

Unfortunately, all these solutions proposed for current generators depend on the supply voltage value.

$$I_{in} = \frac{V_{DD} - V_{GS}}{R} \qquad 4.4$$

This means if VDD reduced all the biasing currents reduces too. In all the portable system applications, where the supply voltage is a single-cell battery, it is possible to use a different for biasing current, which is independent from the supply voltage and is only related to the MOS threshold voltage (which is a typical value for each technology). It's possible to use a different topology for biasing current, which is independent from the supply voltage and is, related to the MOS threshold voltage, as shown in circuit of Figure 4-4 [40], [42].

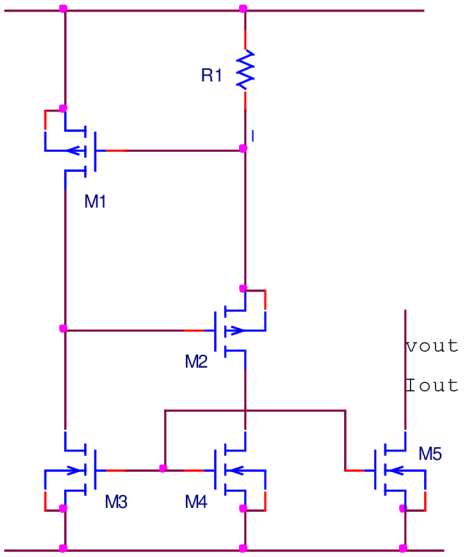


Figure 4-4 Low voltage current source (independent from supply voltage)

From the analysis of the circuit presented in Figure 4-4, the biasing voltage given as:

$$V_{GS1} = RI = V_{TH,P} + \sqrt{\frac{2I}{K_p \left(\frac{W}{L}\right)_1}} \qquad 4.5$$

If M1 aspect ratio is very high, the previous expression can be simplified as follows:

$$V_{GS1} = RI \cong V_{TH,P}$$

$$I \cong \frac{V_{TH,P}}{R} \qquad 4.6$$

$$I_{OUT} \cong \frac{V_{TH,P}}{R} \frac{\left(W/L\right)_5}{\left(W/L\right)_4} = \frac{V_{TH,P}}{R}$$

Using this circuit for unitary gain current mirrors, suitable for LV application (the minimum operating supply voltage is 2Vth + V_{DSAT}); the biasing current is independent from the supply voltage and, consequently insensitive to any supply discharge.

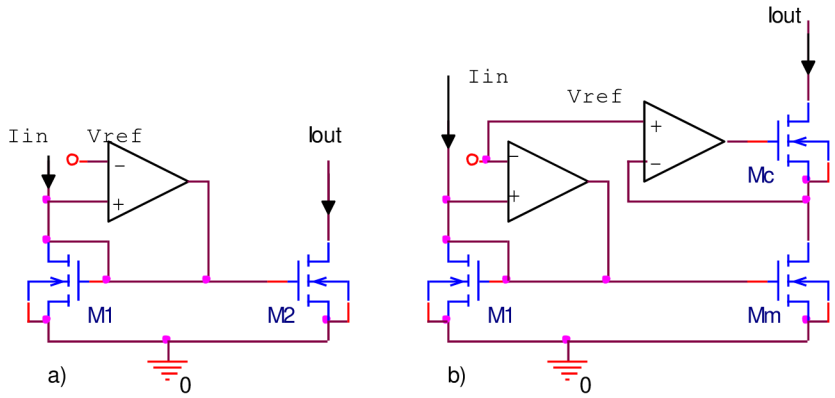


Figure 4-5 a) active input current mirror. **b)** active input regulted cascode current mirror.

There are a number of transistor level implementations of cascode and regulated cascode structures, active input Figure 4-5 [43] could considerably lower the input impedance, and has a well controlled input bias voltage, it can be used in some high precision applications. Care must be taken to ensure the stability of the feedback loop [43], [44] in the active-input and/or regulated cascode structures.

All the above circuits have input voltage equal or higher than V_T, which make them not suitable circuits for low voltage solution.

Could be concluded to summarize desirable characteristics of LV current mirrors are:

i) low AC equivalent input resistance rin, and small DC voltage drop at the input node. ii) high output impedance, thus the output current is independent on the output voltage, whether in DC or AC; iii) low output compliance voltage, such that maximum voltage swing at the output node is allowed; iv) good frequency response for high frequency applications; v) a linear current transfer ratio B [45]-[49].

From above discussion reducing power supply voltage is a straightforward method to achieve low power consumption but there is the fundamental limitation to lower voltage analog circuits using existing design techniques as shown in equation 4.7. This equation states that the power supply must be at least equal to the sum of the magnitudes of the p-type and n-type threshold voltages [73].

$$V_{DD} - V_{SS} > V_{TN} + V_{TP} \qquad 4.7$$

4.1.2 Self-cascode technique

As the device sizes are diminishing fast, the output impedance of the MOSFET is also reducing due to the channel length modulation and these short channel MOSFETs cannot provide high gain structures. To have high output impedance and thereby high gains, cascoding is done.

The regular cascode structures are evaded as their use increases the gain of the structure, but decreases the output signal swing. Self-cascode is the technique which does not require high voltages at output nodes. It provides high output impedance to give high output gain and so it is useful in low-voltage design.

4.1.2.1 Self Cascode (Composite) Transistor

A self-cascode is a 2-transistor structure [14] Figure 4-6, which can be treated as a single composite transistor (Figure 4-6). The composite structure has much larger effective channel length and the effective output conductance is much low. For optimal operation transistor M2 working in saturation region, the lower transistor M1 working in linear region and so equivalent to a resistor, whose value is input dependent, for most advantageous operation the W/L ratio of M2 should be larger than that of M1 W1/L1=mW2/L2, i.e. m>1 [14], [55],[58].

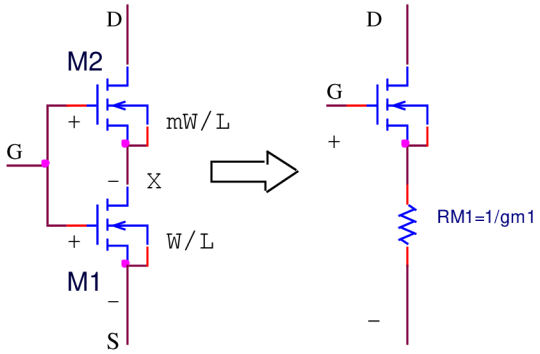


Figure 4-6 simple-Cascode composite NMOS transistor and equivalent simple transistor.

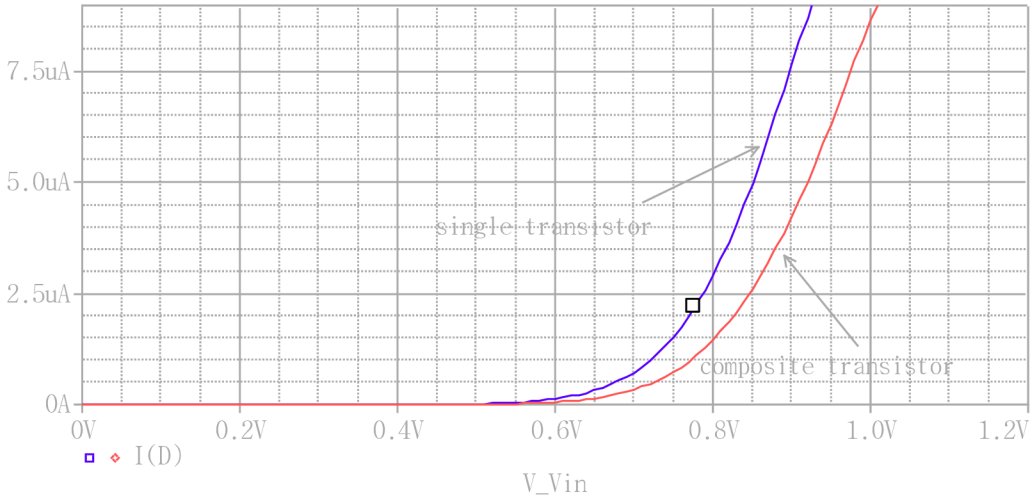


Figure 4-7 input characteristics for composite and single transistor.

For the composite transistor to function properly, both M2 and M1 should conduct, thus, the following conditions should be satisfied:

$$\begin{aligned} V_G - V_X - V_T &> 0 \\ V_G - V_S - V_T &> 0 \end{aligned} \qquad 4.8$$

We can rewrite equation 4.8 as:

$$V_X - V_S < V_G - V_S - V_T = V_{DS}(sat) \qquad 4.9$$

From equation 4.9 we know that transistor M1 must be in linear region. Depending on the drain voltage, while transistor M2 operates in saturation region or linear region. Hence voltage between source and drain of M1 is small. There is no appreciable difference between the V_{DS} (sat) of composite and simple transistors as shown in Figure 4-7.

$$V_{DS}(sat) = V_{DS2}sat + V_{DS1}$$

or 4.10

$$V_{DS}(sat) = V_{DS2}sat + I_{D2}R_1$$

$$R_1 = \frac{1}{(\mu C_{OX}(V_{in} - V_{TN})\frac{W}{L})}. \quad 4.11$$

For the composite transistor to be in saturation region M2 have to be in saturation and M1in linear region. For these transistors, the currents ID1 and ID2 are given as:

$$I_{D1} = \beta_1\left(V_{GS} - V_{TN} - (\frac{V_X}{2})\right)V_X \ (ohmic - region) \quad 4.12$$

$$ID2 = (\beta_2 / 2)(V_{GS} - V_X - V_{TN})^2 (saturation - region), \quad 4.13$$

$$I_{D2} = \left[\left(\beta_2\beta_1\right)\Big/ 2\left(\beta_2 + \beta_1\right)\right]\left[V_{GS} - V_{TN}\right]^2.$$

Because β is proportional to W/L, we can have the equivalent W/L:

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{W}{L}\right)_2\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2 + \left(\frac{W}{L}\right)_1} \quad 4.14$$

If lengths of M2 and M1 are equal, and M2 is m times wider than M1, the equivalent W/L ratio is:

$$\left(\frac{W}{L}\right)_{eq} = \frac{m}{m+1}\left(\frac{W}{L}\right)_1 = \frac{1}{m+1}\left(\frac{W}{L}\right)_2 \quad 4.15$$

Small-Signal Equivalent Circuit (Composite Transistor).

Composite transistor, which has a much larger effective channel length (thus lower output conductance), the effective transconductance gm for the composite transistor is approximated as[50]-[55].

$$g_m(effective) = (g_{m2}/m) = g_{m1} \qquad 4.16$$

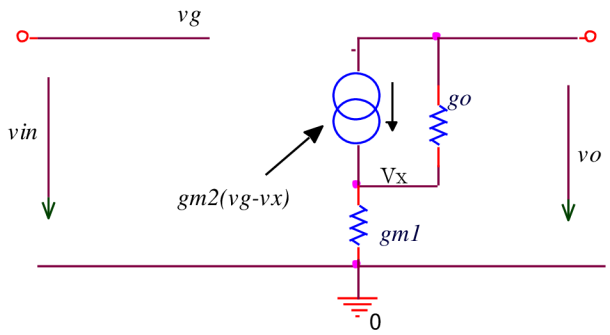


Figure 4-8 small signal equivalent circuit of the composite trnsistor.

Using Figure 4-8 voltage gain and current gain are given as:

$$Av = -g_{m1}g_{m2} \qquad 4.17$$

$$\beta = g_{m2} + g_o + g_{m1} + g_{m1}g_o \cong g_{m2} \qquad 4.18$$

The equivalent output impedance of the composite transistor as depicted in Figure 4-9 is:

$$r_o = g_{m2}r_2r_1 - r_2 - r_1 \approx (g_{m2}r_1 - 1)r_2$$

$$= (m.g_{m1}r_1 - 1)r_2 = (m-1).r_2 ... (m \gg 1) \qquad 4.19$$

It is obvious from equation 4.19 output resistance of composite transistor is bigger than of conventional.

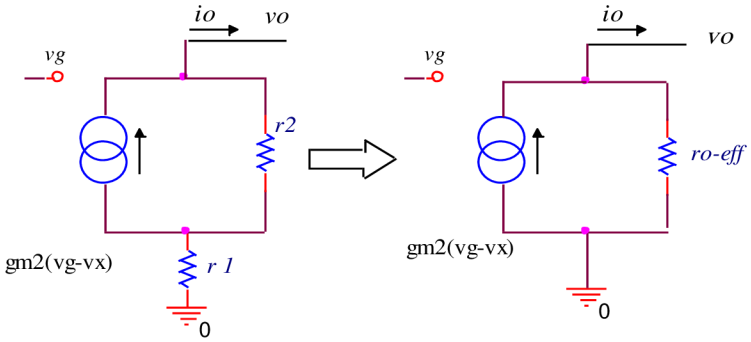


Figure 4-9 the equivalent output impedance of the composite transistor.

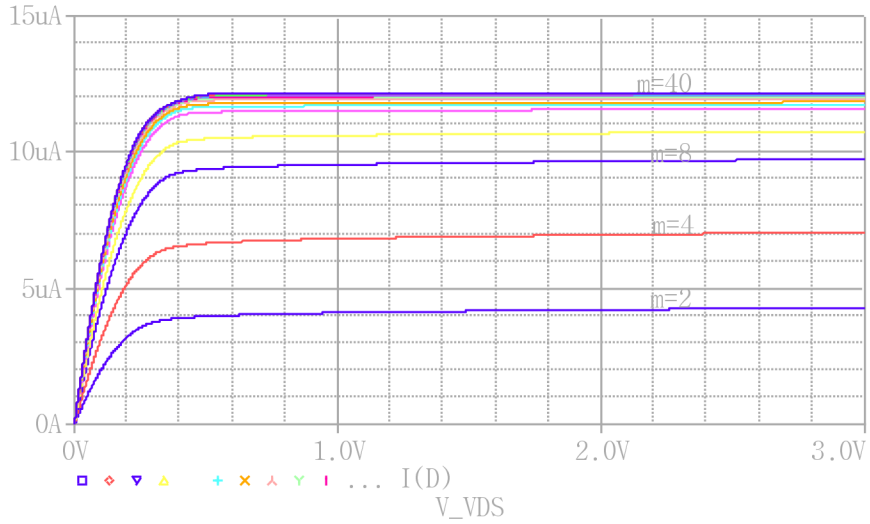


Figure 4-10 " m" varying effect on the ouput characteristic.

The composite transistor comparing to simple transistor has bigger transconductance, bigger out put impedance, there is no discernable voltage supply requirement difference in both the composite and simple transistors. Thus, self-cascode structure can be used in low voltage applications [56]-[62].

Two decisive advantages of composite transistors design are significant area savings and simple modeling.

4.1.2.2 Self cascode current mirrors

Current-mode structures performances depend strongly on performance of employed current mirrors, Usually, high current transfer accuracy, high output impedance, low input voltage (VIN) and low minimum output voltage are expected from a current mirror;

The simple current mirror Figure 4-11a is usually far from achieving high accuracy and high output impedance, mainly due to channel length modulation effect. Both accuracy and output impedance of a conventional double-cascode current mirror Figure 4-11b [47], [48] are much higher with respect to a simple current mirror, however, input and output voltage swings are restricted. [55],[58],[63]-[65].

To improve output swings, a simple self-cascode current mirror has been reported [64], which utilizes the self-cascode structure [55] shown in Figure 4-11c.

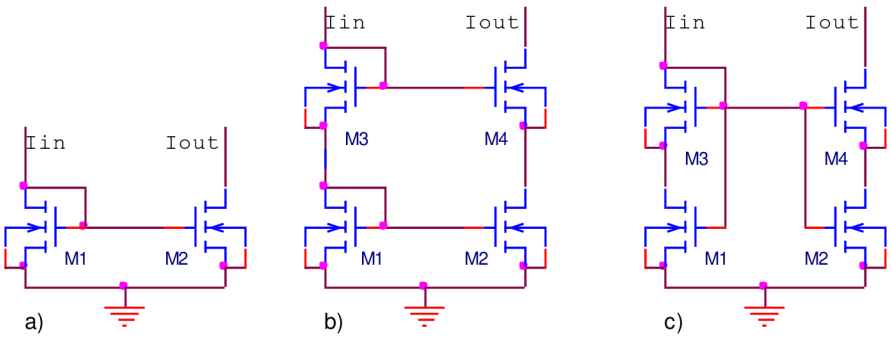


Figure 4-11 (a) simple current mirror. **(b)** cascode current mirror. **(c)** self cascode current mirror.

The small signal input resistance and output resistance of Figure 4-11c can be found as:

$$r_{in} = \frac{1}{g_m(effective)} \qquad 4.20$$

g_m effective bigger than gm of equivalent conventional transistor, then input resistance rin of composite transistor is smaller.

$$r_{out} = (g_{m4} r_3 - 1) r_4 \qquad 4.21$$

It is obvious from equation 4.21 output resistance of composite transistor is bigger than of conventional.

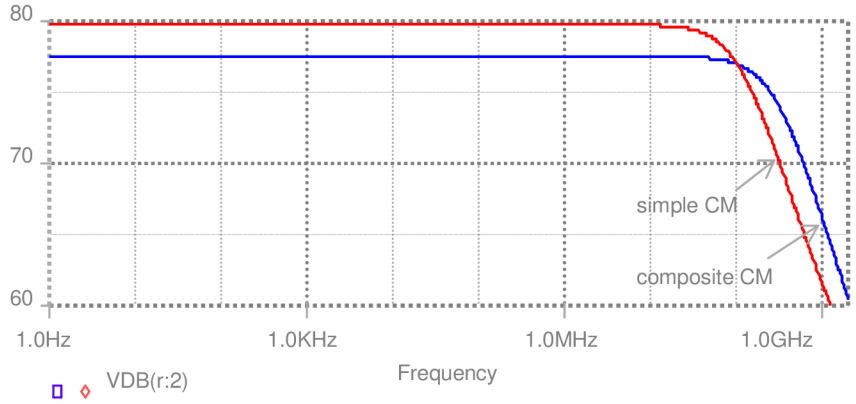


Figure 4-12 input impedance for composite and conventional CM.

From last Figure 4-12 , that parasitic input impedance of self cascode current mirror smaller than simple current mirror impedance.

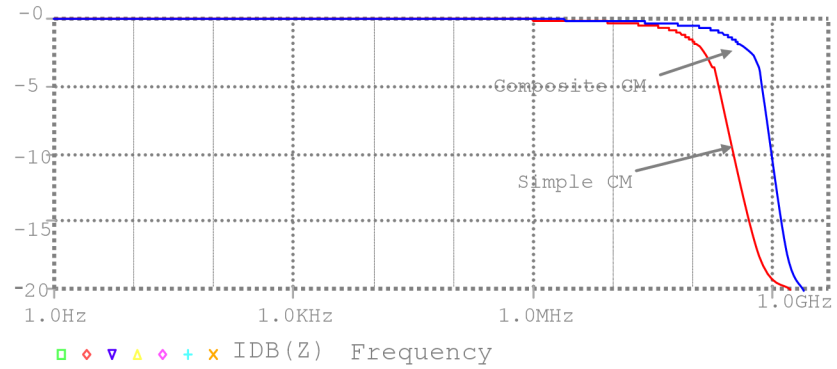


Figure 4-13 current mirror AC simulation.

This composite transistor has a transconductance-to-output conductance ratio as high as that of a long-channel transistor but a shorter “physical channel length”. Figure 4-13, Figure 4-14, Figure 4-15 presenting better characteristics performance for self cascode current mirror.

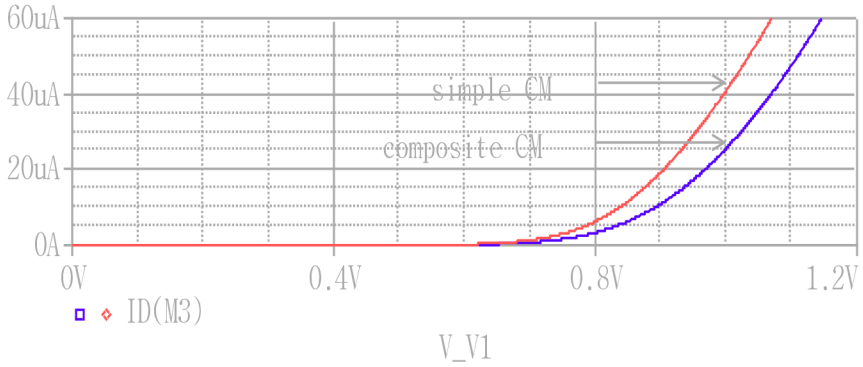


Figure 4-14 input voltage vs input current characteristics

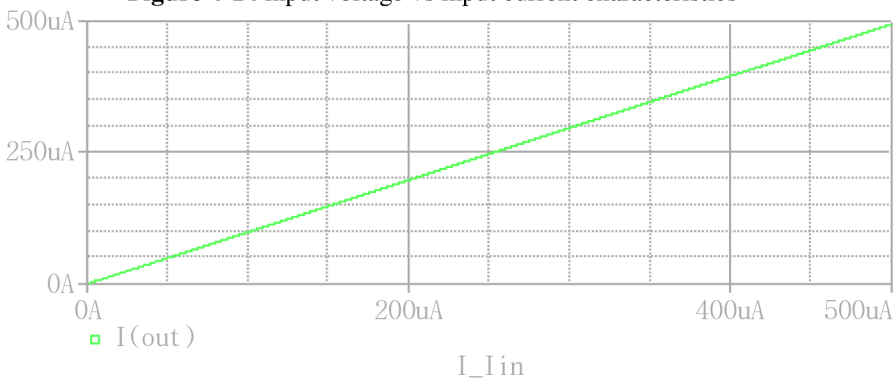


Figure 4-15 DC simulation for Iin and Iout self cascode CM current follower of CM.

4.1.2.3 Self Cascode Differential Pair

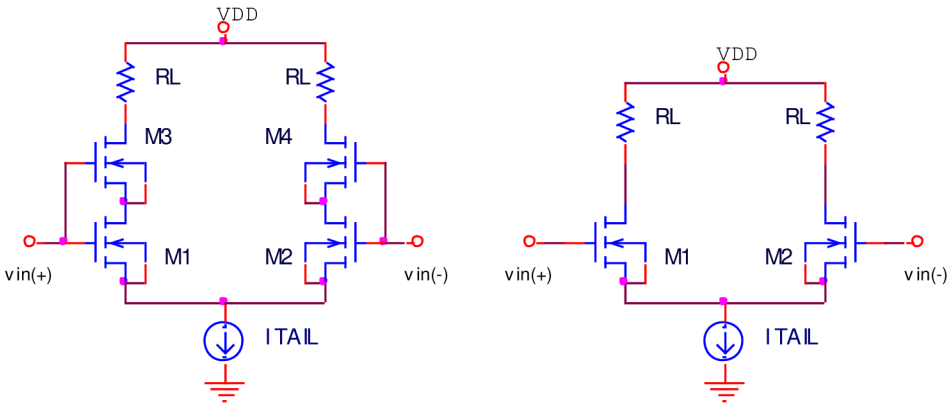


Figure 4-16 self cascode differential pair and conventional differential pair.

Composite transistor can replace single transistors in a differential pair; self-cascode differential pair configuration shown in Figure 4-16 provides high gain with larger voltage headroom than the conventional cascode structures. The lower transistors operate in non-saturation region. For (W/L) 3 >> (W/L) 1 and (W/L) 4 >> (W/L) 2, the circuit behaves like two transistors operating in saturation region but with out severe channel length modulation effects[66]-[68].

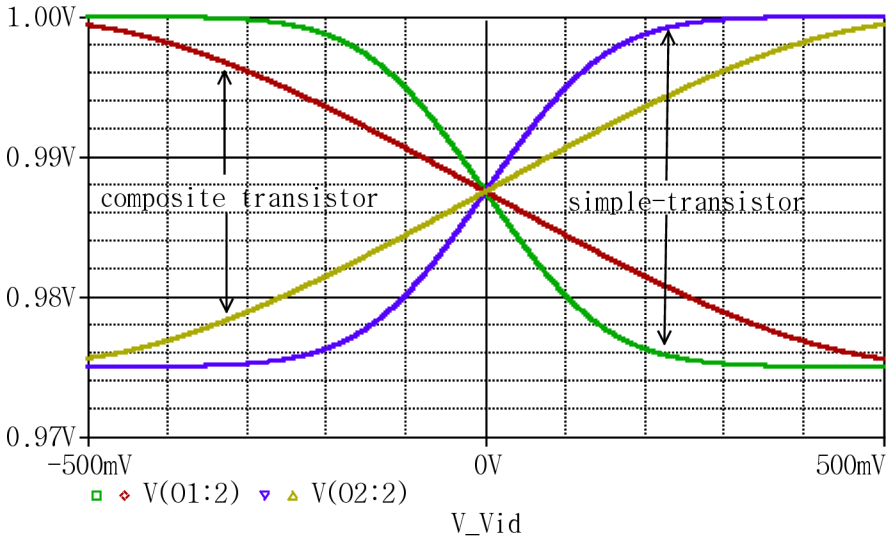


Figure 4-17 Input voltage vs output voltage.

4.1.3 Bulk-Driven Technique

Among the many possibilities for implementing the third approach**,** the bulk-driven technique one of the best approaches for low voltage CMOS circuits offers the potential for avoiding the limit of Equation (4.7).

4.1.3.1 Bulk-Driven MOSFETs

The real solution to the threshold voltage problem comes from an intimate knowledge of the technology is general principle called "bulk driven" MOSFET method. In this method, the gate-to-source voltage is set to a value sufficient to form an inversion layer, and an input signal is applied to the bulk terminal [69].

The operation of the bulk-driven MOSFET is much like a JFET Figure 4-19, the inversion layer forming the conduction channel beneath the gate structure in Figure 4-18[70], its enough to connect the gate terminal to a fixed voltage of sufficient magnitude to form a channel. The thickness of the depletion layer beneath the source, inversion layer, and drain of the MOSFET is determined by the bulk potential. By varying the bulk-source voltage, this depletion layer thickness changes, and the inversion layer through which the drain current is flowing is modulated. The channel current can be modulated with very small dc values of the bulk-source potential resulting in a device that is extremely useful for low voltage applications.

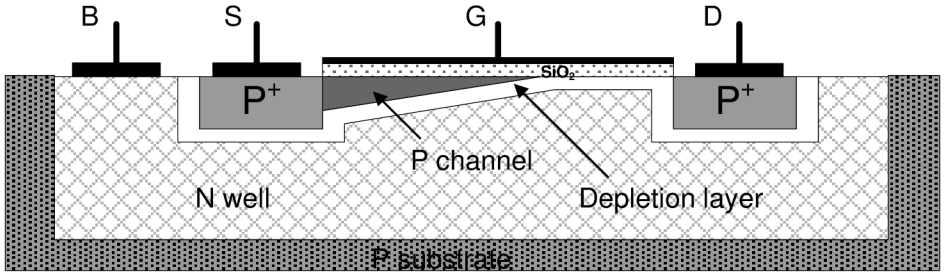


Figure 4-18 Cross section of p-channel MOSFET in N-well CMOS technology.

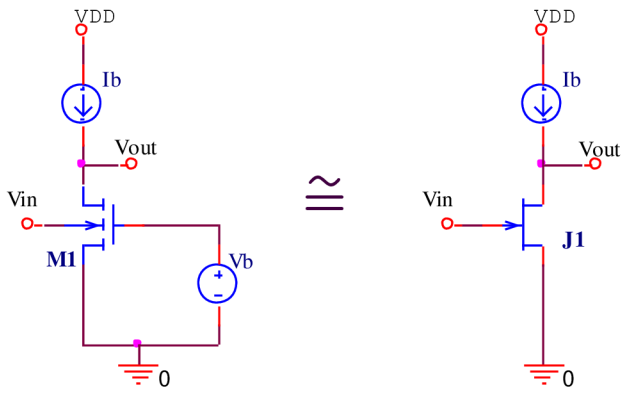


Figure 4-19 Similarity between Bulk-driven NMOS transistor and junction field effect transistor.

Simply if we apply signal to the bulk, instead of to the gate, and keep VGS constant, then we have a bulk-driven MOS transistor [70]-[73].

Small Signal Bulk-Driven MOS Transistors

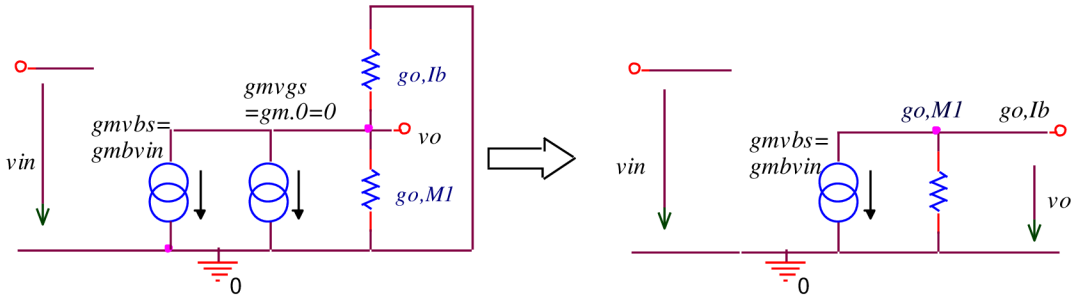


Figure 4-20 Small signal equivalent circuits.

To apply signal at the bulk, we must have a separate well for the bulk to isolate it from the substrate of the chip. According to analysis of Figure 4-20 the values can be written as:

$$Av = \frac{v_{out}}{v_{in}} = \frac{g_{mb}}{g_{o,Ib} + g_{o,M1}} \qquad 4.22$$

$$G_m eff = g_{mb} \qquad 4.23$$

$$g_o = g_{o,Ib} + g_{o,M1} \qquad 4.24$$

First-order theory [70] gives the dependence of the drain current, i_D, as:

$$i_D = \frac{K'W}{L}\left(v_{GS} - V_T - \frac{n}{2}v_{DS}\right)v_{DS}, \qquad 4.25$$

$v_{DS} \leq v_{DS}(sat)$

$$i_D = \frac{K'W}{2nL}\left(v_{GS} - V_T\right)^2\left(1 + \lambda v_{DS}\right) \qquad 4.26$$

$v_{DS} \geq v_{DS}(sat)$

$$v_{DS}\left(sat\right) = \frac{v_{GS} - V_T}{n} \qquad 4.27$$

$$n = 1 + \frac{C_{BC}}{C_{ox}} + \frac{qNFS}{C_{ox}} = 1 + \frac{\gamma}{2\sqrt{\phi j - V_{BS}}} \qquad 4.28$$

The parameters in equation 4.28 are identical with standard SPICE parameters for MOSFETs. However, in bulk-source operation, the gate-source voltage becomes a constant and we re-express equations 4.25 and 4.26 as:

$v_{DS} \leq v_{DS}(sat)$

$$i_D = \frac{K'W}{L}\left(V_{GS} - V_{T0} - \gamma\sqrt{2\phi_F - v_{BS}} + \gamma\sqrt{2\phi_F} - \frac{n}{2}v_{DS}\right)v_{DS}, \qquad 4.29$$

$v_{DS} \geq v_{DS}(sat)$

$$i_D = \frac{K'W}{L}\left(V_{GS} - V_{T0} - \gamma\sqrt{2\phi_F - v_{BS}} + \gamma\sqrt{2\phi_F}\right)^2\left(1 + \lambda v_{DS}\right), \qquad 4.30$$

Respectively, the small signal transconductance in saturation is given by:

$$g_{mbs} = \frac{di_D}{dv_{BS}} = \left(\frac{di_D}{dv_{GS}}\right)\left(\frac{dv_{GS}}{dv_{BS}}\right) = -\left(\frac{di_D}{dv_{GS}}\right)\left(\frac{dv_t}{dv_{BS}}\right) = \frac{\gamma g_{ms}}{2\sqrt{2\phi_F - V_{BS}}} \qquad 4.31$$

If $V_{BS} \geq 2\Phi_F - 0.25\gamma^2$ then the channel JFET transconductance exceeds the MOSFET transconductance [73].

The bulk-driven structure is more suitable for low voltage operation as shown in Figure 4-21, but big attention to prevent potentials to turn on the parasitic BJT transistors which may result in latch-up problem [73], [74].

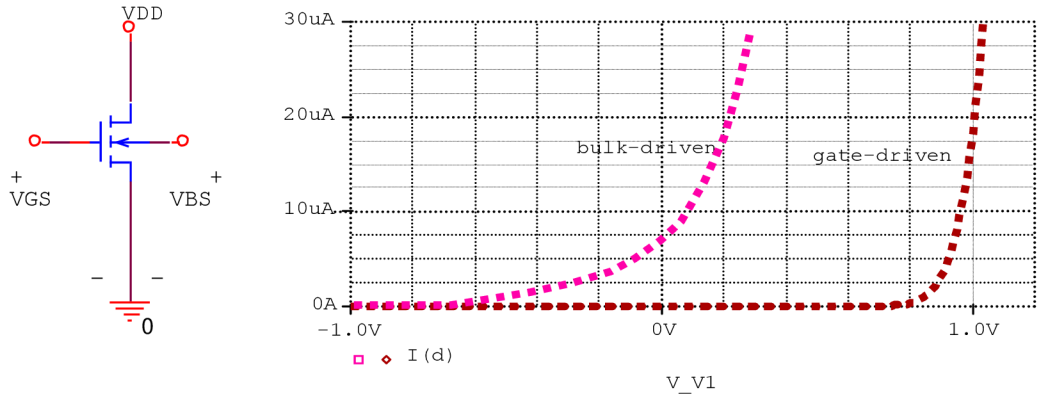


Figure 4-21 ID vs Vbs or Vgs of bulk driven conventional gate driven MOS transistor.

4.1.3.2 CMOS Current mirror Bulk-Driven

One of the problems with MOSFETS or BJT current mirrors is that a significant voltage must be dropped across the input device. The voltage drop across this connection is greater than V_T for the strong inversion-inversion saturation operation, If the bulk-driven MOSFET is operating with the bulk-source junction slightly forward biased, this voltage drop is minimized.

Low voltage current mirror is shown in Figure 4-22b [73]. Instead of the gate drain diode connection used in the standard simple current mirror Figure 4-22a; this current mirror has a bulk drain connection. And, the bulks of M1 andM2 are tied together rather than the gates. The gates of M1 and M2 for the N-type version go to the most positive voltage available, VDD. This n-type current mirror can be implemented in CMOS p-well technology [73]-[77].

The small signal input resistance and output resistance of Figure 4-22b can be found as

$$r_{in} = \frac{1}{g_{mbs}} = \frac{2\sqrt{2\phi_F - V_{BS}}}{g_{ms}{}^{\gamma}} \qquad 4.32$$

$$r_{out} = \frac{1}{\lambda I_{DS}(sat)} \qquad 4.33$$

Where I_{DS} (sat) is proportional to V_{GS2}-V_t these values are in the same range as gate-driven mirrors.

The results show that the input voltage drop for the bulk-driven mirrors can be much less as presented in Figure 4-23. For example, at 30µA input current, the value of VDS1 for the gate-driven mirror was 0.9V and for the bulk-driven mirror it was 0.25V. From Figure 4-24 the same values of output current can get it with less VDS. The input-output current linearity of the gate-driven mirrors is absent in the bulk-driven mirrors because the input transistor is operating in saturation Figure 4-25. The small signal output resistances are approximately the same.

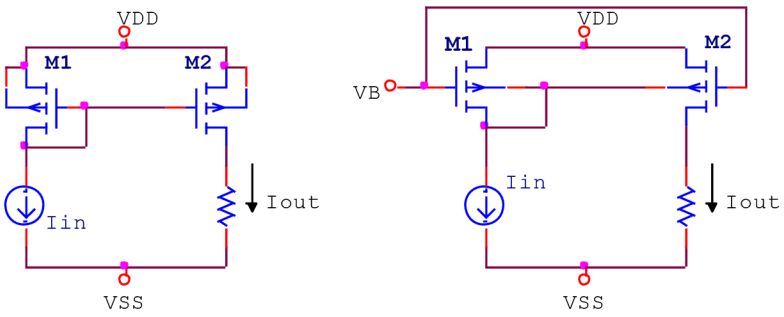


Figure 4-22 Simple current mirror: **a)** Gate-driven, **b)** Bulk-driven.

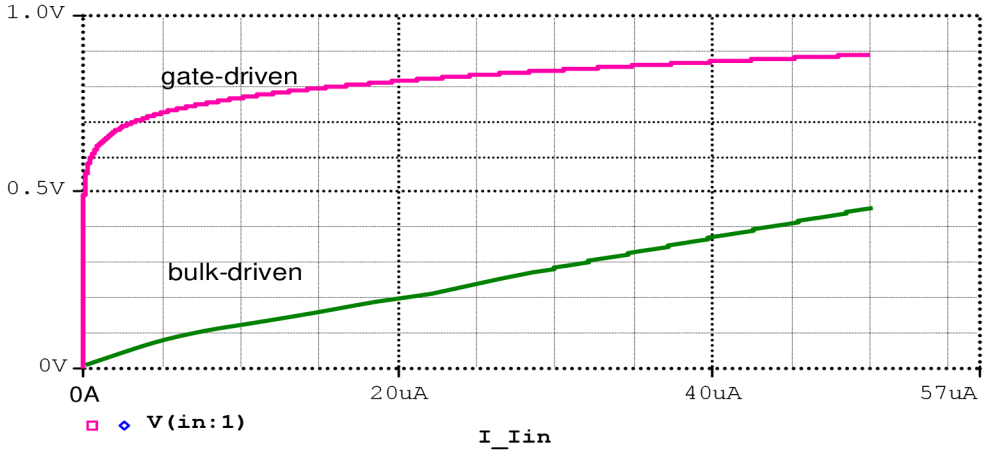


Figure 4-23 Input voltage vs. input current characteristics.

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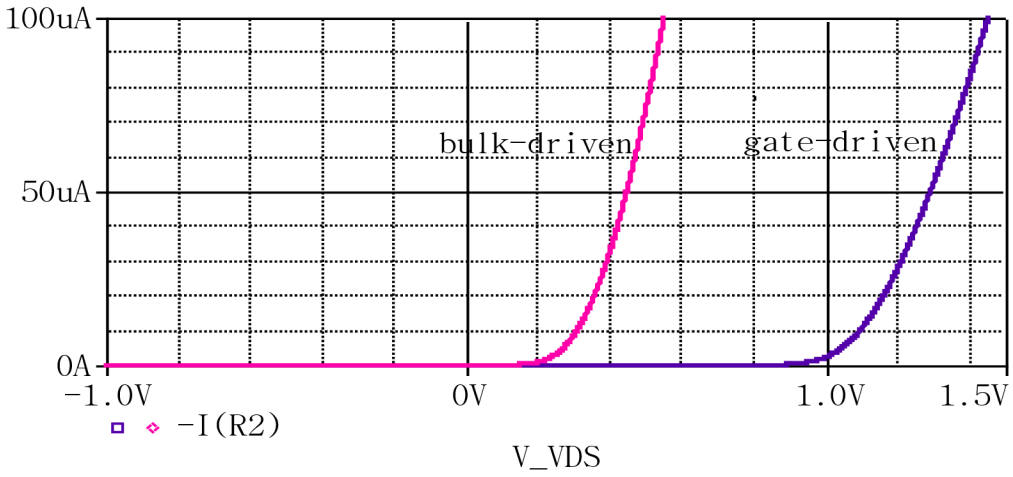


Figure 4-24 voltage vs output current characteristics.

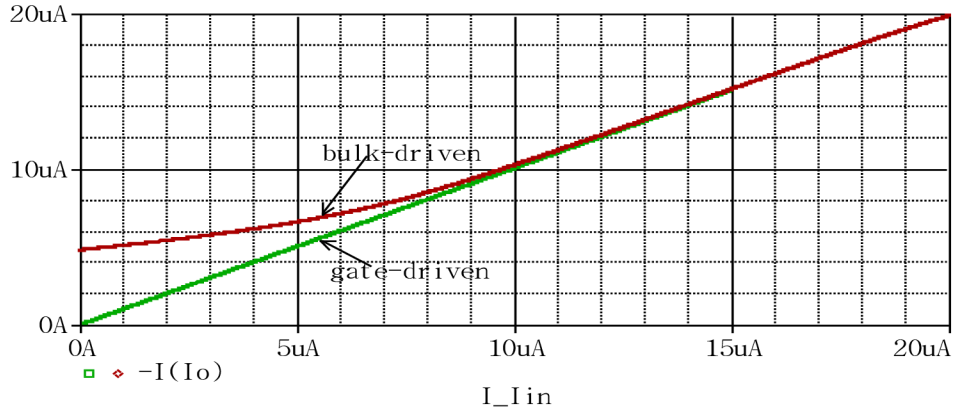


Figure 4-25 Input output transfer characteristics.

4.1.3.3 CMOS Deferential stage Bulk Driven

One of the best approaches for low voltage CMOS circuits is the bulk-driven differential pair is to form the channel in the input transistors by connecting their gate terminals to an appropriate bias voltage, and apply the input signal to the bulk terminal of these devices Figure 4-26 [75]. The use of the bulk as the input terminal of the circuit allows a large signal swing with cutting off the transistor. However, the body transconductance gmbs is smaller than the gate transconductance gm because of smaller control capacitance of the depletion layer, larger parasitic capacitance to the substrate and therefore the unit gain bandwidth is smaller considering the same current and higher input referred noise, this is the main draw back of the bulk driven approach. Nevertheless, the slew rate does not change, as long as the capacitance does not change significantly [75]-[80], and the two bandwidths are related as

$$f_T, bulk-driven \approx \frac{\eta}{3.8} f_T, gate-driven \qquad 4.34$$

Where η is the ratio of g_{mb} to g_m and typically has a value in the range of 0.2 to o.4.

It can be consider that the gain of a bulk driven amplifier can actually exceeds that of a standard gate driven differential stage [75] as given by

$$g_{mb} = \frac{di_D}{dv_{BS}} = \frac{\gamma \times g_m}{2\sqrt{2\phi_F - V_{BS}}} \qquad 4.35$$

When

$$V_{Bs} \geq 2\phi_F - 0.25\gamma^2$$

Figure 4-27 Drain currents versus differential input voltage, showing convincible characteristics for bulk driven deferential pair.

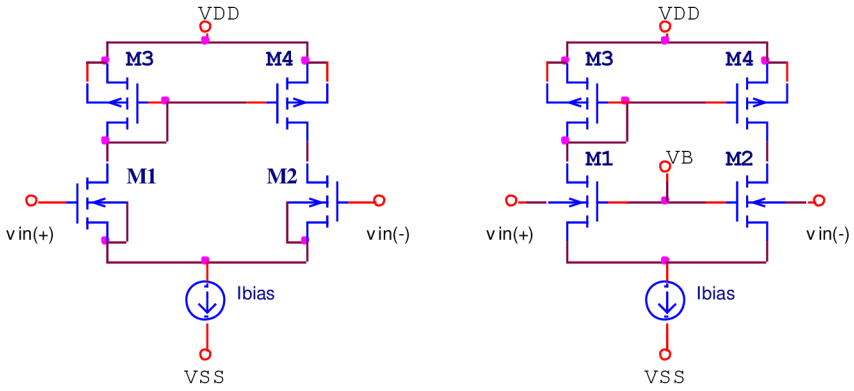


Figure 4-26 Conventional differential pair and bulk driven differential pair.

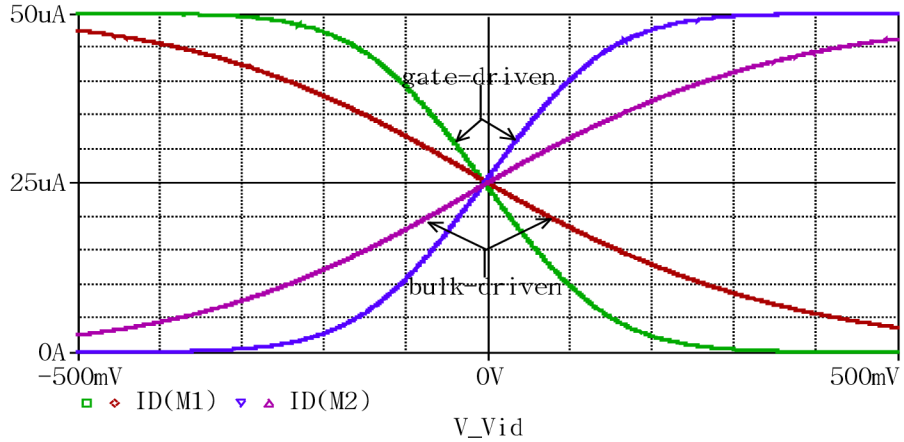


Figure 4-27 Drain currents vs differential input voltage, bulk driven compared with conventional differential pair.

4.2 Low Voltage Second Generation Current Conveyors

Novel topologies of second generation current conveyors (CCIIs) working at low supply voltage with reduced power consumption (in the μW range) are presented.

4.2.1 Self cascode CCII

4.2.1.1 Current Conveyor based Current Mirror

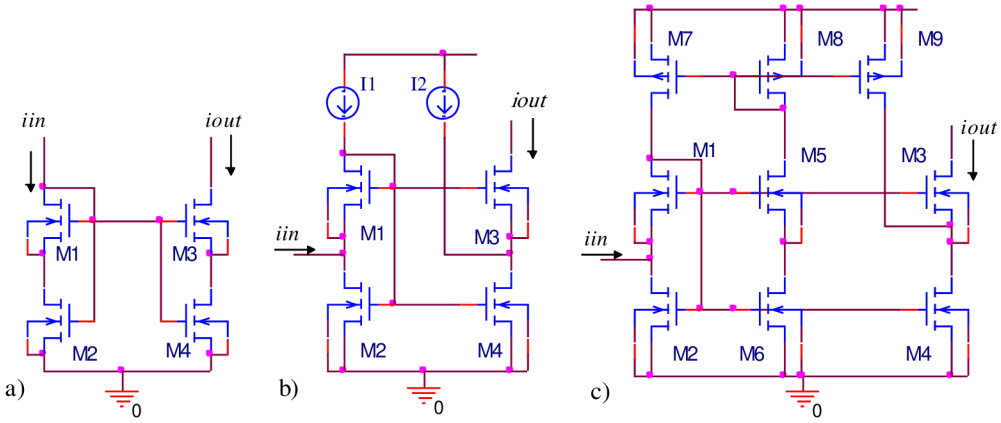


Figure 4-28 low voltage cascaded current mirror a) self cascode. b) low voltage input. c) high output impedance.

Self cascode current mirror has introduced in [55] as shown in Figure 4-28a with advantage of high output impedance comparing to the simple one, to reduce input voltage of self cascode current mirrors, low voltage current mirror has been introduced[58] as shown in Figure 4-28b, the input node is source of M1, instead of its gate. Thus, Vin is no more VT-limited. This is an appreciable feature in low-voltage analog design, since Vin, can be very close to 0V. An implementation of the circuit principle is shown in Figure 4-28c [58], where careful design to eliminate current error and achieve Iout=Iin, this current mirror will show output impedance comparable with that of a conventional double cascode current mirror with low voltage input. the aspect ratios have to set as $(W/L)_2= (W/L)_4= m(W/L)_6$, $(W/L)_3= (m-1)(W/L)_5 =(m-1)(W/L)_1$ and $(W/L)_7= W/L)_8=(W/L)_9$.

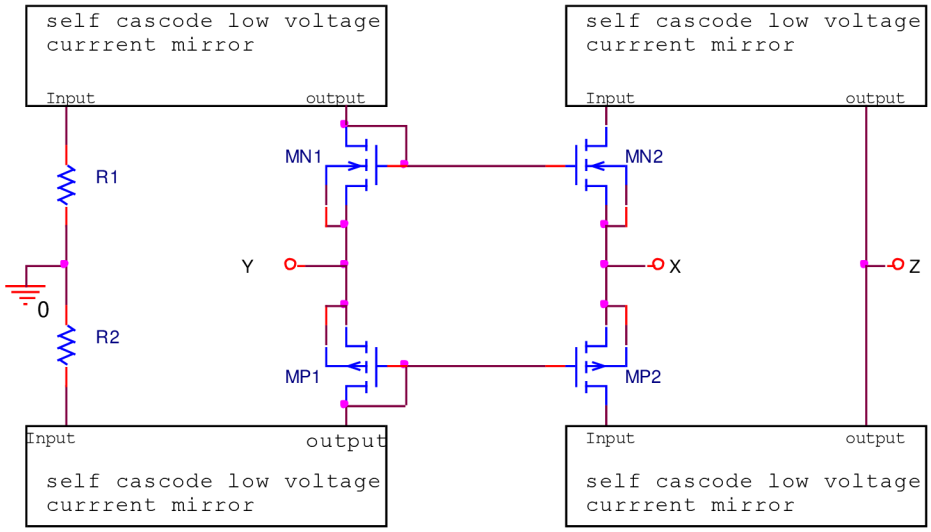


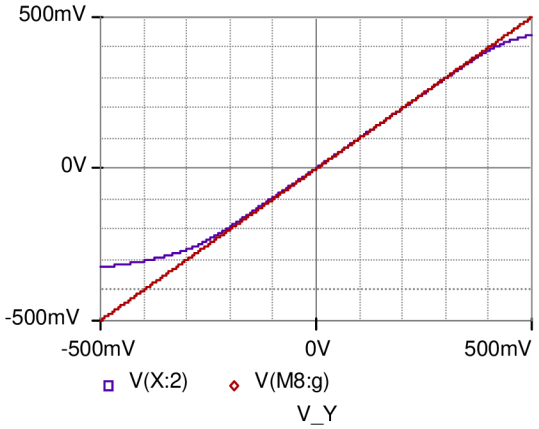
Figure 4-29 CCII based low voltage self cascode current mirror.

Application, NMOS and PMOS versions of low voltage self cascode current mirrors of Figure 4-28c employed to construct novel CM CCII based self cascode current mirrors shown in Figure 4-29 [83].

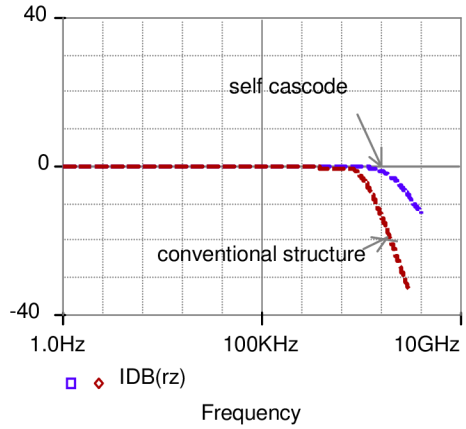
The advantage of self cascode here is that using the advantage of output resistance of composite transistor to get higher output resistance to improve current linearity between x and z nodes and hence minimizing the portion of ix which is lost on output transistors.

Figure 4-30 depicts simulations; the main performance characteristics are summarized in

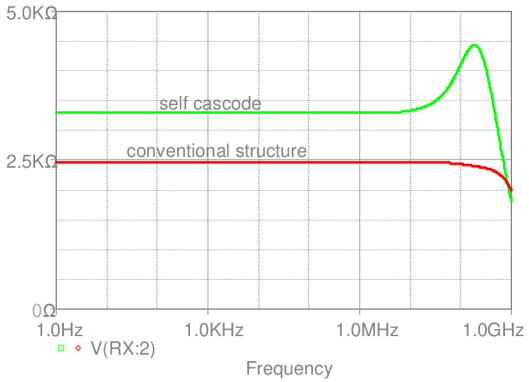
Table **4-1** which reports a comparison with conventional CCII based current mirrors.



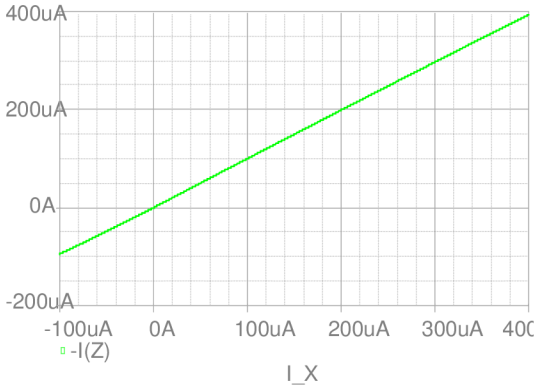
a) Xnode voltage and Ynode.



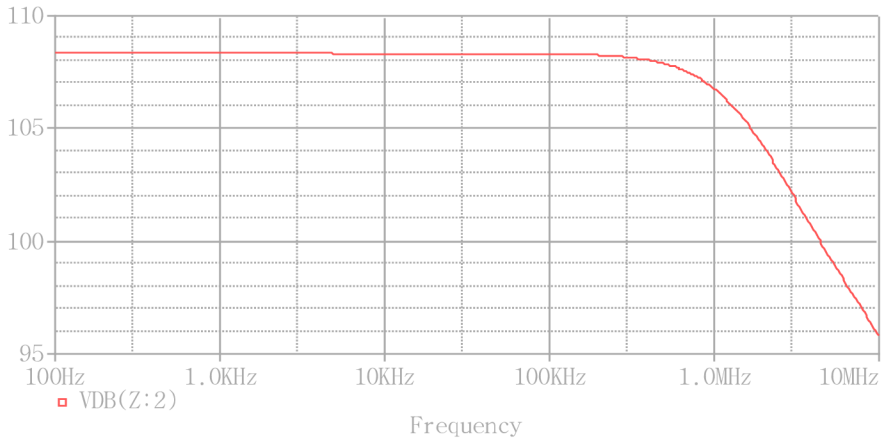
b) Current transfer ratio iz/ix.



c) input impedance rin,x.



d) Ix and Iz linearity.



e) Output resistance Z normalized in dB.

Figure 4-30 CCII based low voltage self cascode current mirror characteristics simulation.

Characteristics	Composite Transistor CCII	Conventional CCII Based CM
Voltage Supply	±1.5 V	± 1.5 V
Power Consumption	70µW	95 µW
3dB Bandwidth	320 MHz	200 MHz
Dynamic Range	-110 mV, +300 mV	-180 mV, +180 mV
Node X Parasitic Resistance	3.3 KΩ	2.5kΩ
Node Z Parasitic Resistance	2 MΩ	850 KΩ

Table 4-1 CCII based low voltage self cascode CM characteristics.

4.2.1.2 Self Cascode CCII based Op Amps

Self Cascode CCII based-Miller Op Amp

The proposed structure diagram of CCII self cascode miller op-amp is shown in Figure 4-31, composite transistors can replace single transistors in a differential pair as was explained 4.1.2.3 Table 4-2 and the differential input signal is applied to composite transistors. The gates of transistors M1a, M2a are connected together, the gates of transistors M1b, M2b are connected too to implement self cascode structure which is has features are demanded by CCII, with the same value approximately of voltage supply that have used in conventional CCII miller op-amp Figure 2-26. In this circuit, current mirror M6-M7 is used to sense the current flowing from node X and to mirror it to the high impedance Z node.

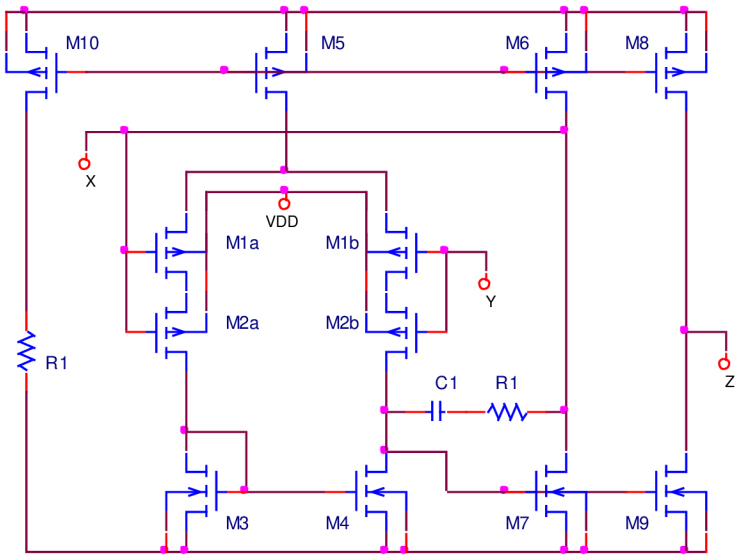


Figure 4-31 self cascode CCII based miller compensated op amp.

Characteristics	Composite Transistor CCII	Conventional CCII
Voltage Supply	± 2 V	±1.5 V
Power Consumption	80µW	70µW
3dB Bandwidth	15 MHz	13 MHz
Dynamic Range	-1.5V, +20 mV	-750mV, +20 mV
Node X Parasitic Resistance	200Ω	110 Ω
Node Z Parasitic Resistance	300 KΩ	300KΩ

Table 4-2 Self cascode CCII based miller compensated op amp characteristics.

Simulation presented in Figure 4-32 to Figure 4-34 affirms foregoing results in Table 4-2, the main advantage affirmed by simulation is that dynamic range extended to appreciable obvious value.

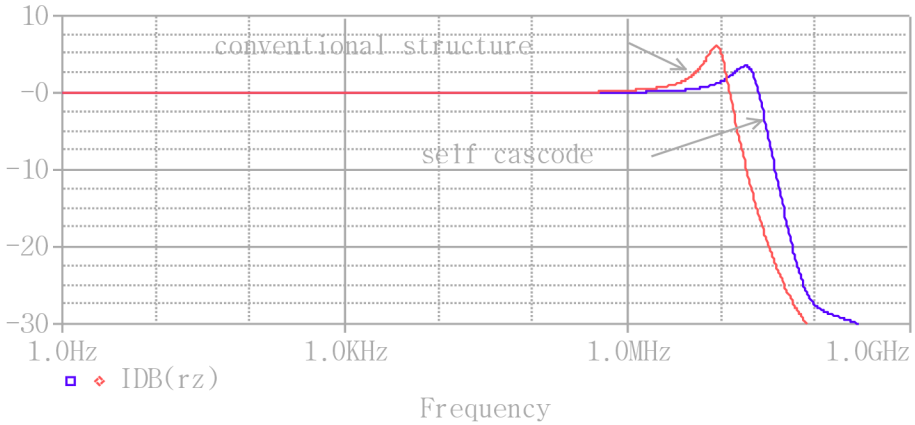


Figure 4-32 Current transfer for conventional and self cascode.

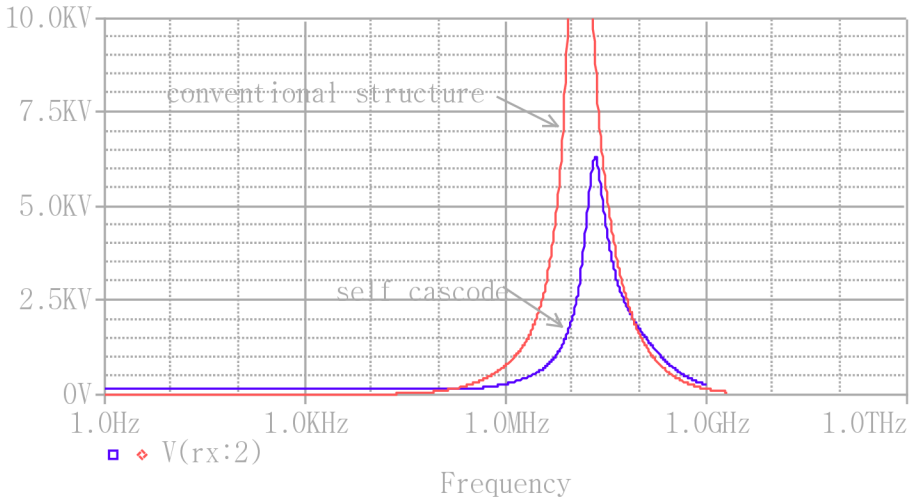


Figure 4-33 x node impedance for conventional and self cascode.

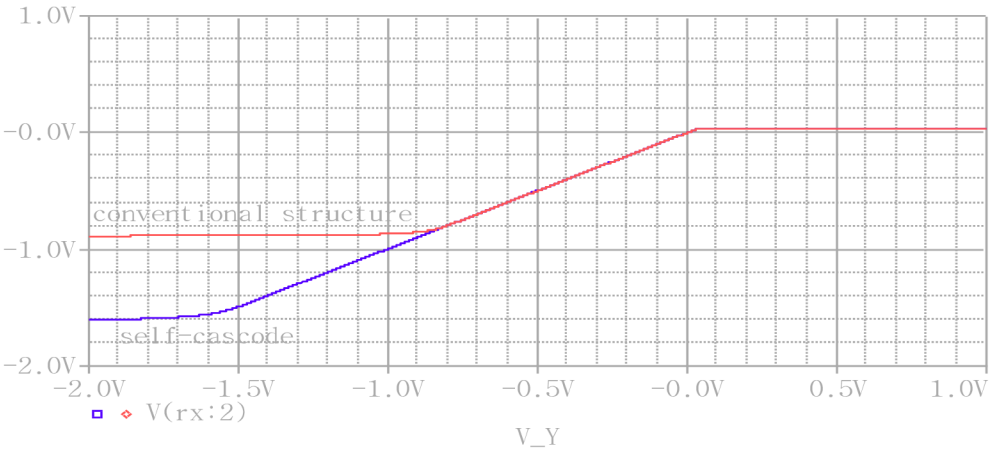


Figure 4-34 X node and Y node voltages.

Characteristics formulas of the previous circuit are:

$$\frac{iz}{ix} = \frac{g_{m8} + g_{m9}}{g_{m6} + g_{m7}} \qquad 4.36$$

$$rx = \frac{2}{g_{m1a} r_o (g_{m6} + g_{m7})} \qquad 4.37$$

$$rz = \frac{r_{o8} r_{o9}}{r_{o8} + r_{o9}} \qquad 4.38$$

CCII based-OTA

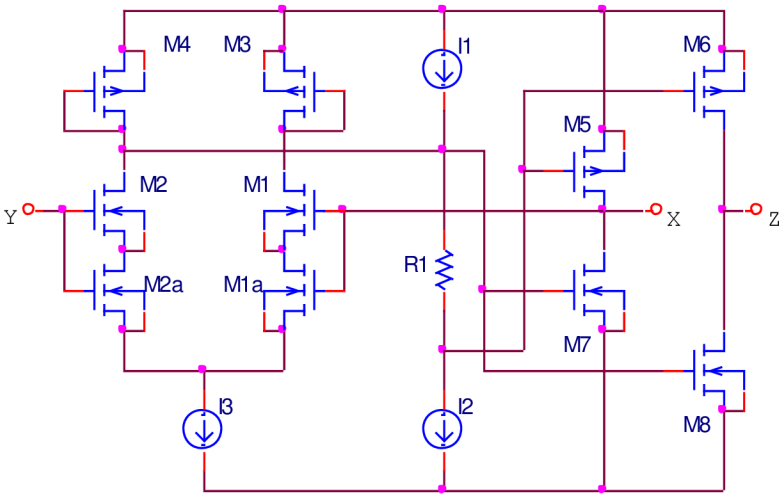


Figure 4-35 CCII Self cascode OTA.

The circuit presented in Figure 4-35 proposed as self cascode CCII OTA, from simulation results, this CCII gives bigger bandwidth comparing to the conventional circuit of Figure 2-33, was introduced in section 2.2.3.1 [83].

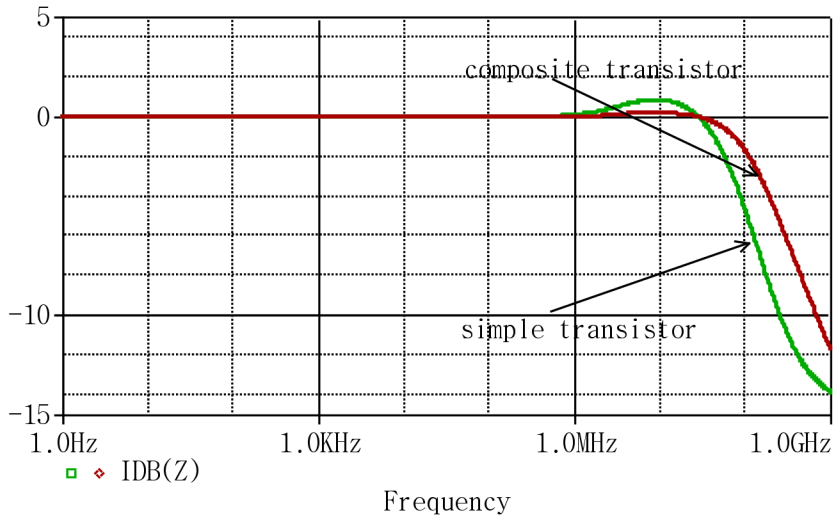


Figure 4-36 current transfer iz/ix.

Current transfer in dB plotted in figure 4.36 showing 155 MHz for composite and 73 MHz for conventional circuit.

CCII based-Push pull Op Amp.

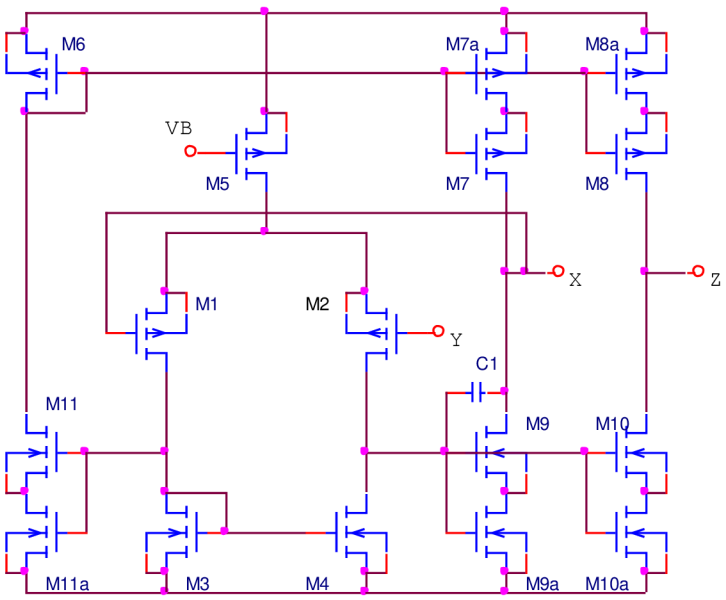


Figure 4-37 Self cascode output push pull Op. Amp

This current topology was introduced and simulated in section (2.2.3.1) as conventional structure OTA with push pull output stage CCII, in this section its modified in order to obtain novel structure, CCII-based self cascode push pull operational amplifier, this can be done replacing the conventional MOS transistors of output stage with composite transistors as shown in Figure 4-37.

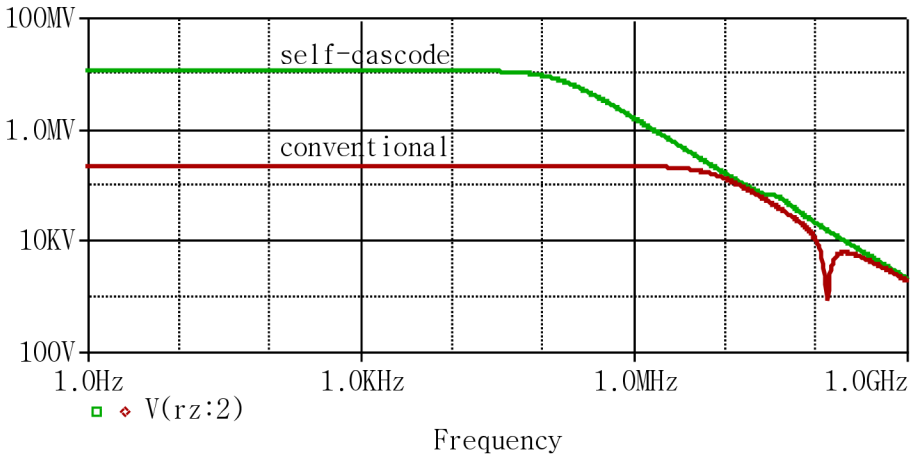


Figure 4-38 z node parasitic impedance for conventional and self cascode.

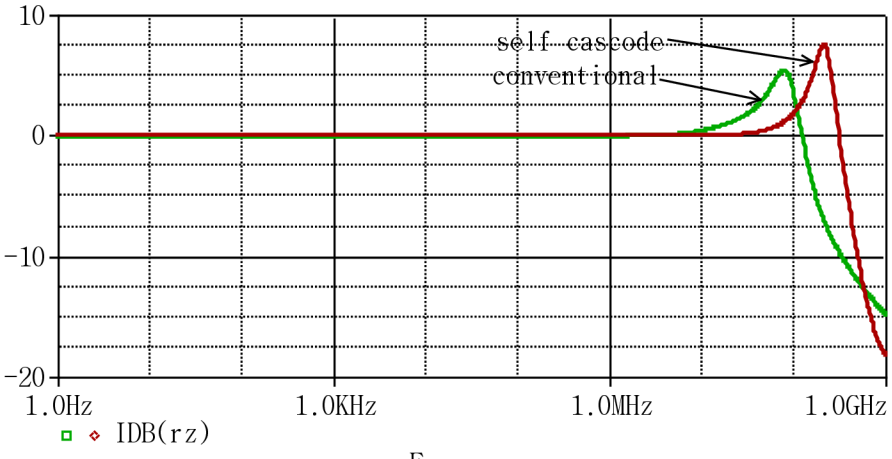


Figure 4-39 Current transfer iz/ix.

The most advantage realized from this structure, the output impedance rz Figure 4-38 is ensured to be high because output impedance of composite transistor is bigger than conventional MOS transistor structure (200k for conventional 15M for self cascode), and consequently better current transfer between x node and z node according to Figure 4-39, Figure 4-40.

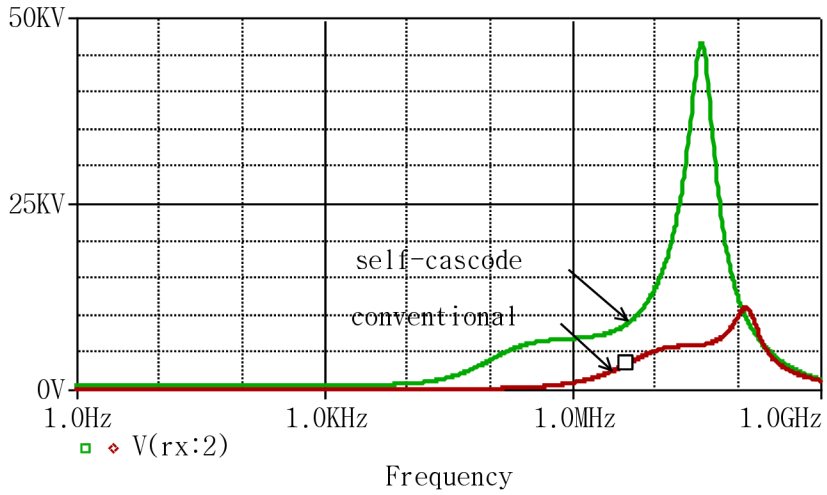


Figure 4-40 x node parasitic impedance.

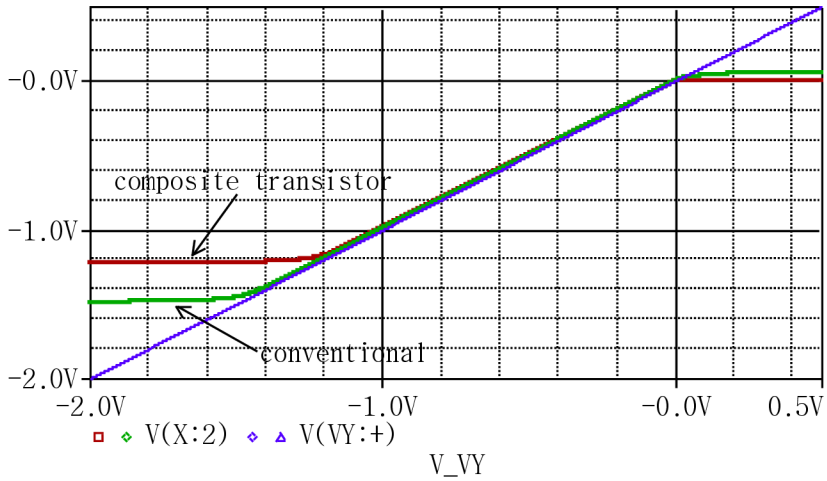


Figure 4-41 Voltage follower between Y node and X node.

As mentioned in section (2.2.3.1) that the conventional circuit has appropriate x impedance, from Figure 4-40 bigger rx for self cascode, but the appreciable draw back is not clear on the CCII characteristic except for voltage follower between y node and x node, the dynamic range for conventional is (-1.5, 0) reduced in self structure to (-1.22, 0) as presented in Figure 4-41.

Main electrical parameters of the CCII of Figure 4-37 can be written as:

$$\frac{iz}{ix} = \frac{g_{m8a} + g_{m10a}}{g_{m7a} + g_{m9a}} \qquad 4.39$$

$$rx = \frac{2}{g_{m1} r_o (g_{m7a} + g_{m9a})} \qquad 4.40$$

$$rz = \frac{r_{o8a} r_{o10a}}{r_{o8a} + r_{o10a}} \qquad 4.41$$

It can conclude it is possible to design an op amp based CCII in self cascode structure to improve the performance; with approximately the same voltage supply level of conventional op amps based CCII.

4.2.2 Bulk Driven CCII

4.2.2.1 CCII based Bulk Driven CM

Novel low-voltage CCII based on bulk-driven current mirror have been constructed.

Figure 4-42 presents positive current conveyors based on a single stage complementary source follower where the gate-source voltage VGS of two n-channel (M1-M3) and two p-channel (M2-M4) devices are supposed to match, the input voltage VY is transferred to the output voltage VX of the follower precisely. The current mirrors (M5-M6) and (M7-M8) are transferring the current from the X terminals of the current conveyors to their Z terminals[55].

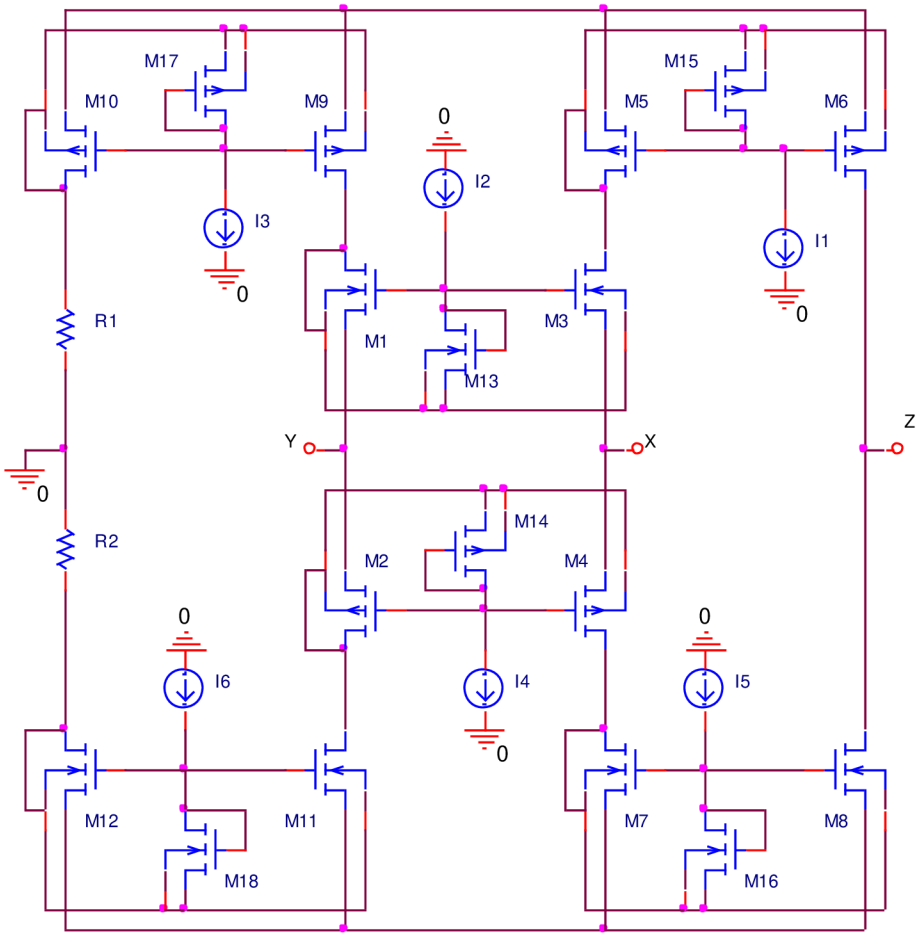


Figure 4-42 CCII based LV bulk-driven CM.

$$\frac{iz}{ix} = \frac{g_{mb3}g_{m7}g_{m6} + g_{mb4}g_{m5}g_{m8}}{g_{m5}g_{m7}(g_{mb3} + g_{mb4})} \qquad 4.42$$

X terminal resistance of this current conveyor is

$$r_x \approx \frac{1}{g_{mb3} + g_{mb4}} \qquad 4.43$$

Z terminal resistance is

$$r_z \approx \frac{r_{o6}r_{o8}}{r_{o6} + r_{o8}} \qquad 4.44$$

While the Y terminal resistance of the current conveyor based on a single stage complementary source follower is dependent on the output conductance of the bias current source M9, M11

$$r_y \approx \left(\frac{r_{o1}}{1 + g_{m1}r_{o1}} + r_{o9}\right) // \left(\frac{r_{o2}}{1 + g_{m2}r_{o2}} + r_{o11}\right) \cong r_{o9} // r_{o11} \qquad 4.45$$

$$r_y \approx \frac{r_{o9}r_{o11}}{r_{o9} + r_{o11}} \qquad 4.46$$

Table 4-3 shows the comparative results of LV LP Bulk-driven versus Gate-driven current conveyor (CCII) based on current mirroring.

Characteristics	LV Bulk-driven CCII	LV Gate-driven CCII
Voltage Supply	± 0.6 V	± 1.5 V
Power Consumption	9 µW	95 µW
3dB Bandwidth	250 MHz	200 MHz
Dynamic Range	-300 mV, +300 mV	-180 mV, +180 mV
Node X Parasitic Resistance	15 KΩ	2.5KΩ
Node Z Parasitic Resistance	2 MΩ	850 KΩ

Table 4-3 charactristics of CCII based LV bulk-driven current mirror.

The provided simulations shown in Figure 4-43 to Figure 4-47 affirm the foregoing performance characteristics.

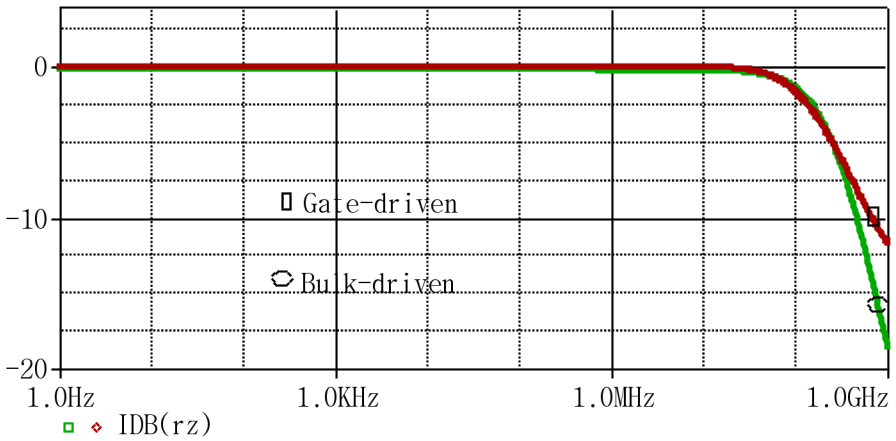


Figure 4-43 Current transfer function iz/ix.

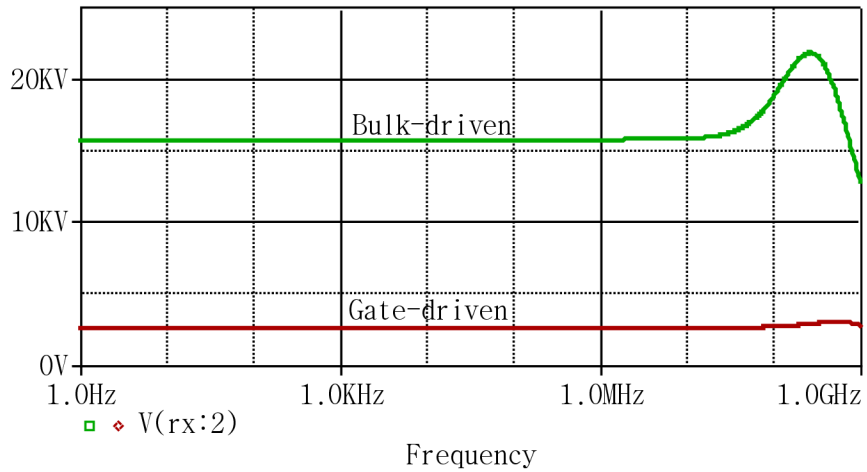


Figure 4-44 x node parasitic impedance.

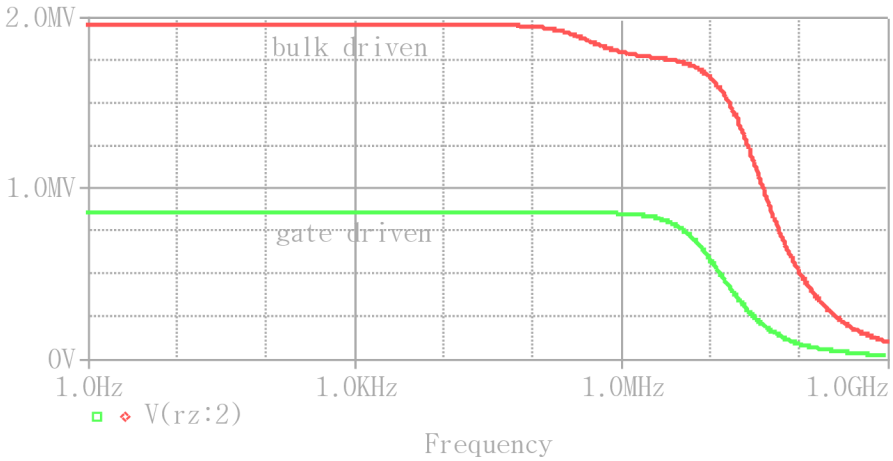


Figure 4-45 z node parasitic impedance.

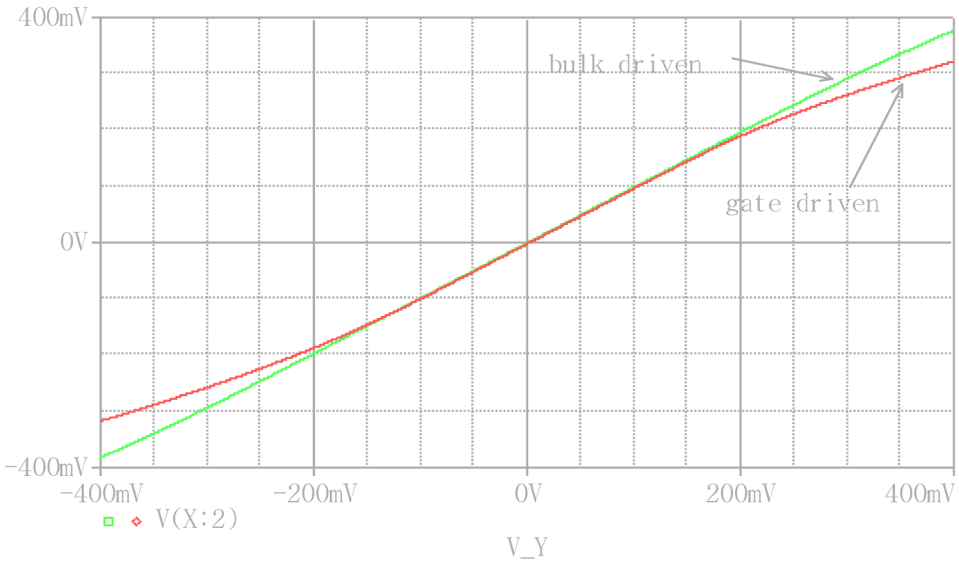


Figure 4-46 voltage follower between X node and Y node.

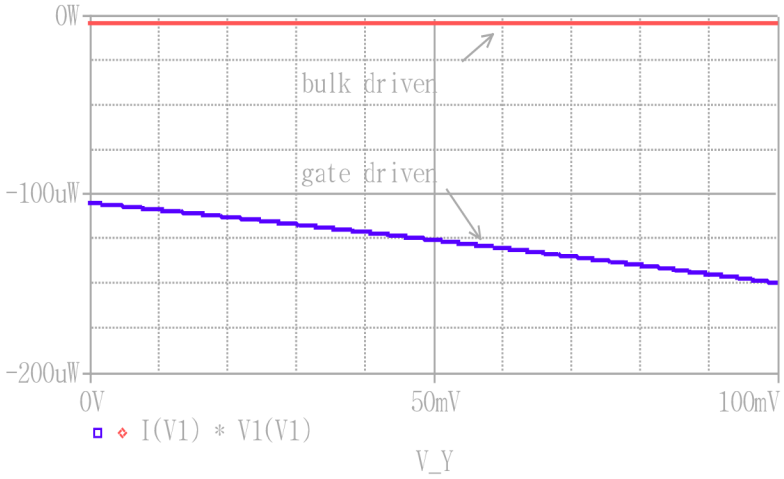


Figure 4-47 power consumption of circuit supply.

The Novel LV LP current conveyor based on bulk-driven current mirror versus gate-driven after simulation approved that is need low voltage supply requirement, has low voltage dissipation, acceptable voltage range and voltage swing for the Y terminal that could not otherwise be achieved at low power supply voltages. But realization of this circuit needed to use an expensive twin-tub technology.

4.2.2.2 Novel LV LP CCII based on bulk-driven miller OTA

Figure 4-48 illustrates the transistor-level implementation of the proposed two stages miller compensated Bulk driven operational amplifier CCII, The input signal is applied to the bulk terminal of the input transistors, MI and M2 while the gate terminals of these devices are connected to ground, the unity gain buffer between Y node and X node is done through the bulks of input transistor transistors.

The minimum supply voltage of a conventional gate driven miller op amp operating in strong inversion is limited by the input stage. This can be expressed as below

$$V_{(\min)} = |V_T| + 3|V_{DSsat}| \qquad 4.47$$

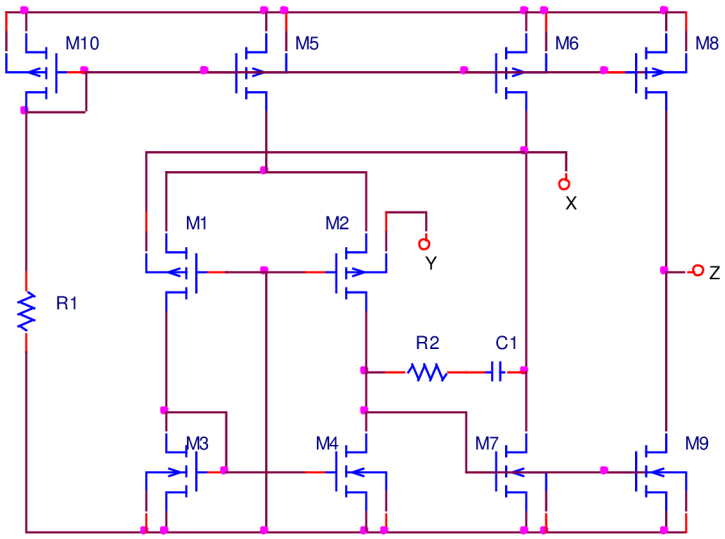


Figure 4-48 CCII based miller compensated bulk-driven op amp.

The operation of the bulk driven MOSFET is of depletion type. The gate-source voltage is set to a value sufficient to turn on the transistor. Input voltage is then applied to the bulk terminal of the transistor to modulate the current flow through the transistor.

By such way of biasing, threshold limit is removed.

The electric parameters as following:

The impedance of the Y terminal is the bulk impedance of MOS transistor which ensuring high input impedance for the voltage follower.

$$r_y = \frac{1}{g_{mb}} = \frac{1}{g_m}\left(\frac{2\sqrt{2\phi_F - V_{BS}}}{\gamma}\right). \qquad 4.48$$

The other terminal resistances of this current conveyor are

$$r_x \approx \frac{2}{g_{mb1} r_o (g_{m6} + g_{m7})} \qquad 4.49$$

$$r_z \approx \frac{r_{o8} r_{o9}}{r_{o8} + r_{oM9}} \qquad 4.50$$

Table 4-4 shows the comparative results of LV LP Bulk-driven versus Gate-driven current conveyor (CCII) based Op. Amp.

Characteristics	LV Bulk-driven CCII	LV Gate-driven CCII
Voltage Supply	± 0.6 V	±1.5 V
Power Consumption	16µW	70µW
3dB Bandwidth	22 MHz	13 MHz
Dynamic Range	-130 mV, +600 mV	-750mV, +20 mV
Node X Parasitic Resistance	2 KΩ	110 Ω
Node Z Parasitic Resistance	300 KΩ	2.3 MΩ

Table 4-4 Table LV bulk-driven versus gate-driven CCII based on miller compensated op amp.

This CCII was designed to operate with a low supply voltage and reduced power dissipation, these requirement are confirmed from previous table and foregoing simulations, the main advantages were verified bigger dynamic range due to the depletion characteristic allows zero, negative, and even small positive values of bias voltage to achieve the desired dc current. This can lead to larger input common mode voltage range, voltage swing that could not otherwise be achieved at low power supply voltages. The simulations in Figure 4-49- Figure 4-54 affirm the foregoing advantages.

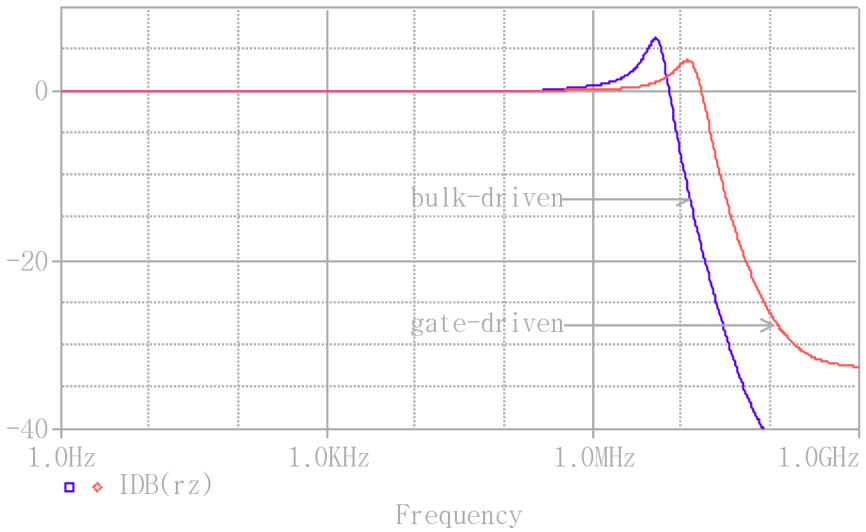


Figure 4-49 Current transfer between x node and z node, iz/ix.

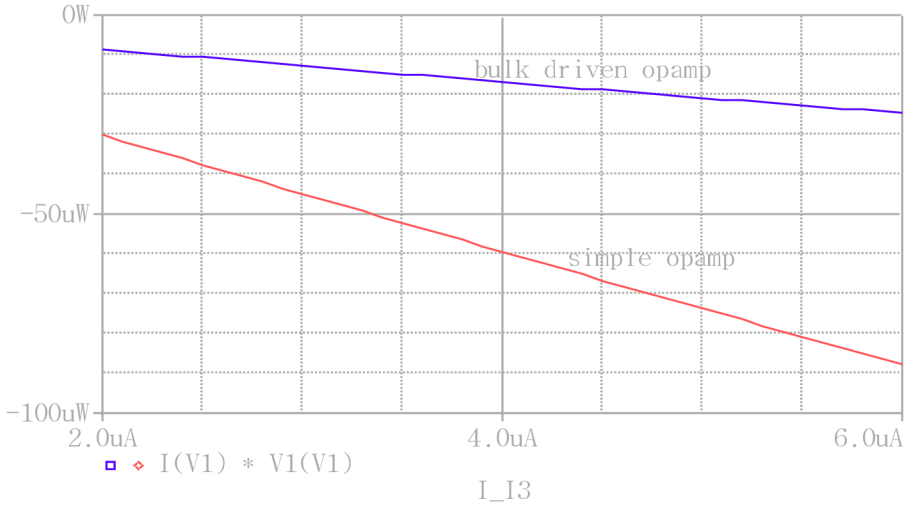


Figure 4-50 power dissipation of current conveyor voltage source.

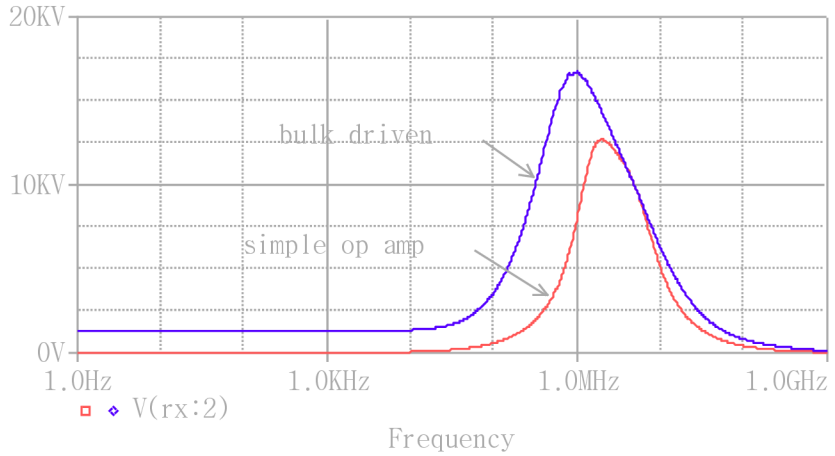


Figure 4-51 Impedance at x node, rx.

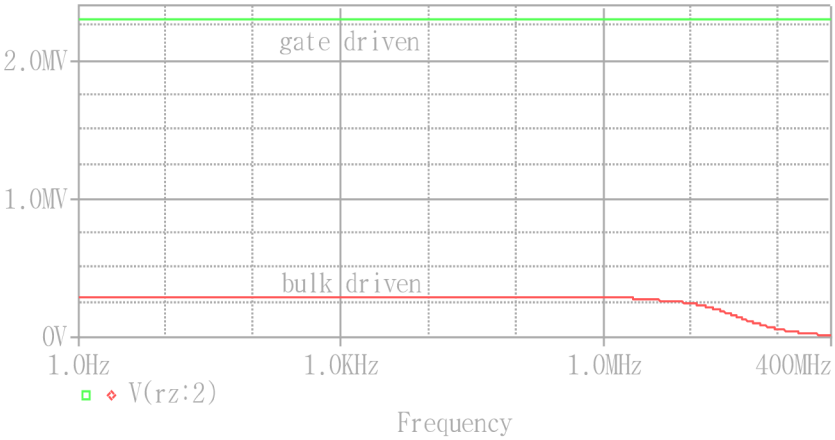


Figure 4-52 Output impedance at z node, rz.

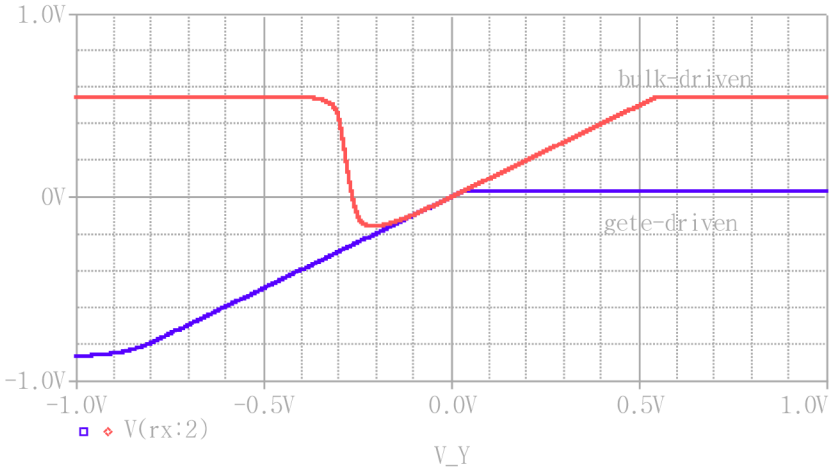


Figure 4-53 Voltage follower between X node and Y node.

4.2.3 Dual Output Current Conveyor

Dual output current conveyor is four terminal devices representing a simple modification of the CCII topology, obtained implementing another output terminal, and named Z−, on CCII architecture. DOCCII basic block is depicted in Figure 4-54, the latter terminal has to show a current flowing in the opposite direction with respect to the conventional output Z+. DOCCII characteristics are summarized in the following matrix.

$$\begin{bmatrix} i_Y \\ v_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ A & 0 & 0 \\ 0 & +B & 0 \\ 0 & -B & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad 4.51$$

Where A and B must be close to 1. For what concerns terminal impedances, as in basic CCII, Y, Z+ and Z− are high impedance nodes, while X terminal shows a low impedance value. The DOCCII basic block is depicted in Figure 4-54.

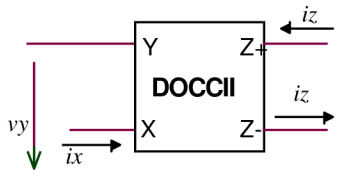


Figure 4-54 DOCCII basic block

4.2.3.1 Dual Output Current Conveyor Implementation

A proposed dual output version of a given CCII is easily obtained simply adding some current mirrors at the output node[4]. In this sense, starting from the circuit shown in Figure 2-39, the corresponding dual output version is presented in Figure 4-55, so obtaining a different current conveyor, having two output terminals (named Z+ and Z-).

One of these terminals (Z+) gives the same current flowing at X node, while the other (Z-) gives it with the opposite sign. In this way an improved second generation current

conveyor, named dual output current conveyor (DOCCII), has been built-up [84]. DOCCII allows an easy implementation of a biquad filter but causes an increase in power consumption.

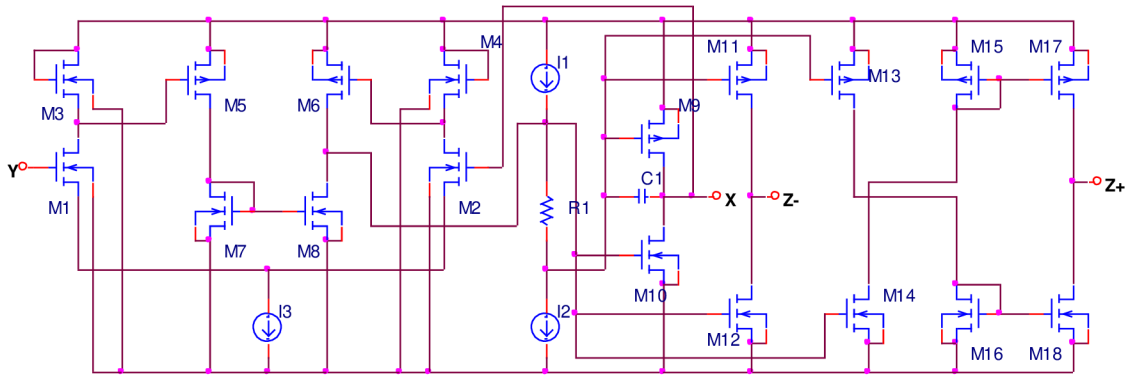


Figure 4-55 LV OTA based DOCCII scheme.

$$r_X \cong \frac{2}{g_{m2}(g_{m9}+g_{m10})} \qquad 4.52$$

$$r_Z = \frac{r_{O11}r_{O12}}{r_{O11}+r_{O12}} \qquad 4.53$$

Table 4-5 DOCCII characteristics

Characteristics	Value
R_x	26 ohm
R_{z+}	280 Kohm
R_{z-}	260 Kohm
Dynamic range	360mV to -500mV
-3dB Bandwidth	35MHz
V_{DD},-V_{SS}	1v

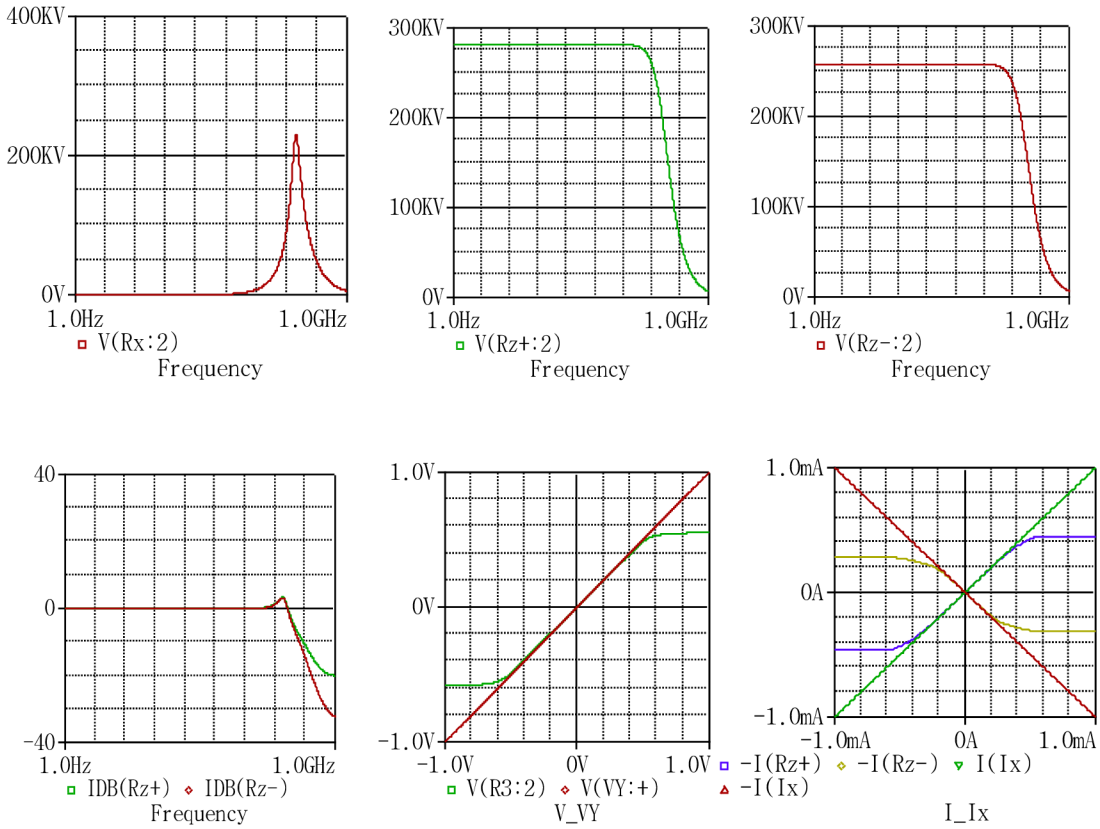


Figure 4-56 DOCCII simulations.

The main simulated results, concerning the DOCCII, have been summarized in

Table 4-5.

The proposed CCII has been designed in a standard CMOS technology (AMIS 0.7µm). It has been characterized from the electric point of view at the input and output nodes once the MOS aspect ratios have been optimized for the total supply voltage of 2 V (±1V). In order to verify the effective behavior of the filter topology, the parasitic impedances of the proposed CCII have been evaluated too.

In Figure 4-56, the simulated results are concerning input impedance at X node, output impedance at Z± node, dynamic range and current transfer ratio giving satisfied values in low voltage supply.

4.2.3.2 DOCCII-based Filters

Current-mode filter with one input and three outputs is presented in Figure 4-57, using three DOCCIIs depicted in Figure 4-55 only two grounded capacitors,. It can

simultaneously realize low-pass, band-pass and high-pass responses. This circuit is derived from the Kenvin-Huelsman-Newcomb (KHN) structure[81], [82]. Filter with one input and three outputs are reported, but the number of active and passive elements is higher with respect to this kind of circuit. The proposed filter presents low passive and active sensitivities and the attractive characteristic of independent control of the current transfer function parameters. Furthermore, the fact that all the passive elements are grounded makes it suitable for integrated realizations, because the resistors can be replaced with OTAs configured as positive resistors.

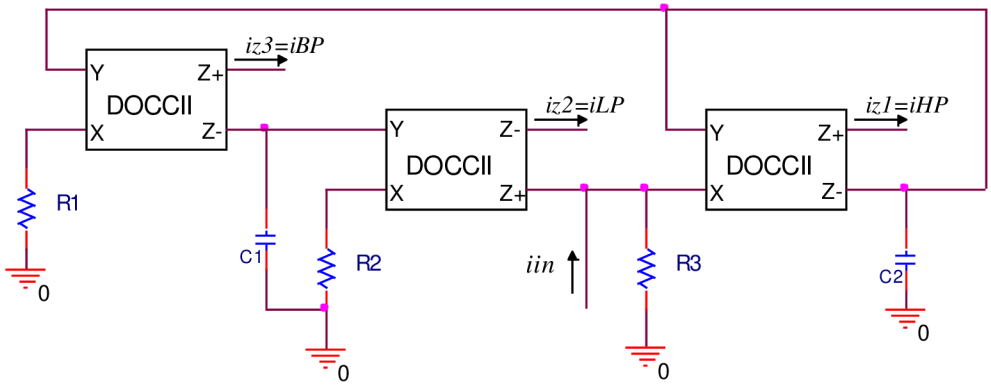


Figure 4-57 CCII-based biquad universal filter.

The circuit has been determined by means of the following considerations. One of the most popular biquad structures for classical op amp-based RC filters is the KHN circuit, in which a summer and two integrators are present. In the circuit in Figure 4-57 the output voltage-input current ratio for the first and third CCII is of integrator kind. The first CCII transforms the output voltage of the third CCII in a current through the resistor R_1. Then the relation between I_{Z1} and I_{Z3} is of integrator kind. On the other hand the second CCII transforms the output voltage of the first CCII in a current through the resistor R2. Then the relation between I_{Z2} and I_{Z1} is of integrator kind. The third CCII performs the adding function, because I_{Z3} is equal to the sum of: a) the input current Iin b) the current I_{Z2} and c) the integration of the current I_{Z3} performed through the feedback of the third CCII and the resistor R3.

Routine analysis allows deriving the following low-pass (I), band-pass (2) and high-pass (3) transfer functions:

$$\frac{i_{LP}}{i_{IN}} = \frac{\frac{1}{R_1R_2C_1C_2}}{S^2 + \frac{S}{R_3C_2} + \frac{1}{R_1R_2C_1C_2}} \qquad 4.54$$

$$\frac{i_{BP}}{i_{IN}} = \frac{\frac{s}{R_1C_2}}{S^2 + \frac{S}{R_3C_2} + \frac{1}{R_1R_2C_1C_2}} \qquad 4.55$$

$$\frac{i_{HP}}{i_{IN}} = \frac{S^2}{S^2 + \frac{S}{R_3C_2} + \frac{1}{R_1R_2C_1C_2}} \qquad 4.56$$

From the previous analysis it is clear that the filter behavior is ensured by three current conveyors. The dual output version is needed only if the three different filter outputs are separately needed. The filter responses can be easily tuned. In fact the parameters ω_0/Q_0 and ω_0 are independently adjustable, through R3 and R1 (or R2), respectively.

4.2.3.3 SIMULATION RESULTS

Figure 4-58 shows the three output currents of the circuit in Figure 4-57. Simulation results are in a good agreement with the theoretical calculations. The behavior has been optimized, for a central frequency of 15 KHz, for the three outputs, but a wide tuning range has been obtained. From the theoretical analysis keeping constant R_1, and R_2 it is possible to control the quality factor Q_0 by modifying R_3 value, as confirmed by simulations results which are quite satisfactory.

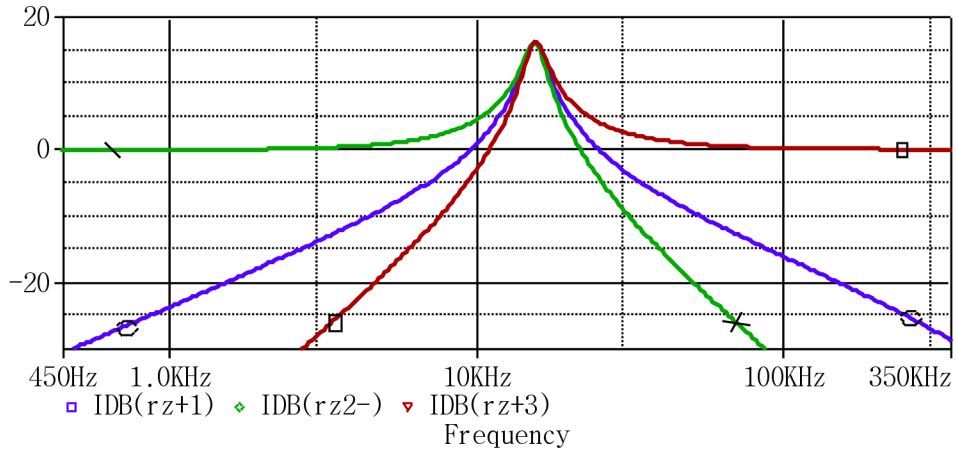
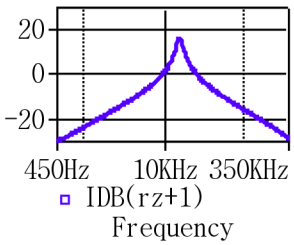
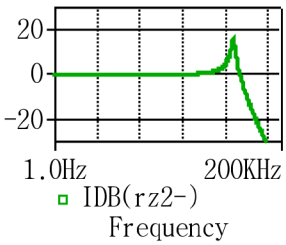
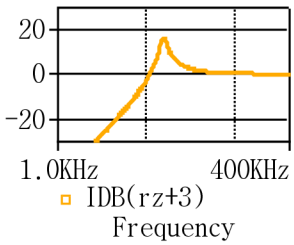


Figure 4-58 DOCCII based-biquad filter response.







4.2.4 Current controlled CCII based-self cascode current mirrors

A proposed implementation of the second-generation current conveyors based self cascode current mirrors with a positive current transfer from X to Z (CCII+) is shown in Figure 4-59. The considered circuit between points Y and X allows the function of voltage follower, by means of M1 to M4. The transistors M9-M12 allow the mixed loop to be dc biased. The output NMOS and PMOS current mirrors duplicate the current flowing through port X at port Z.

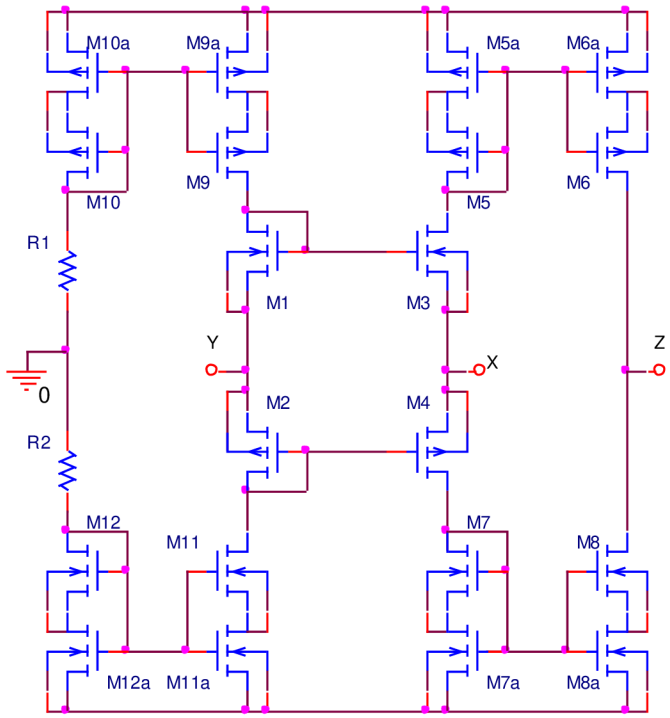


Figure 4-59 LV CCII based self cascode CM.

The rx impedance simulation plotted 2.9 k ohm which means high value resistance as depicted in Figure 4-60 and this is draw back in many applications when x impedance loaded with low load and advantage in some other applications.

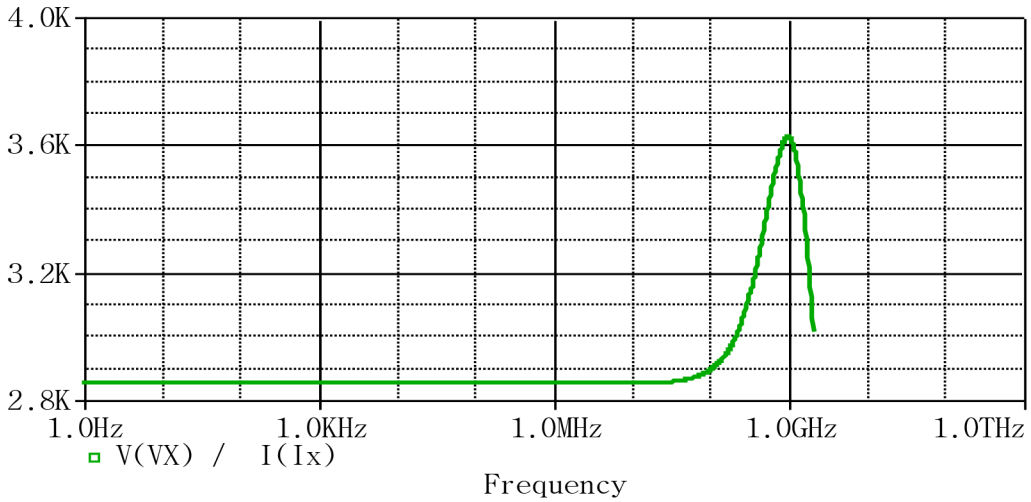


Figure 4-60 rx for self cascode CCII CM.

While x node impedance value is affected by the biasing condition of the transistors that form output stage as expressed in chapter 3. Starting from this consideration the designer can adjust the value of x node impedance by controlling the biasing of output stages.

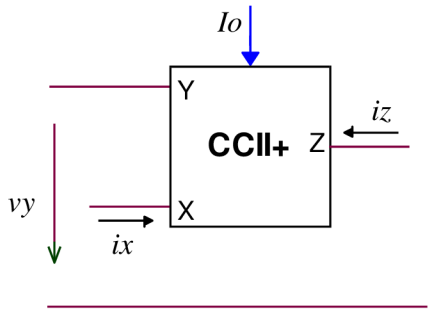


Figure 4-61current controlled basic block.

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & r_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \qquad 4.57$$

Figure 4-62 shows CCCII block, the impedance seen at x node is not more a parasitic element, but becomes a part of the block specifications, as presented in matrix form reported above [23].

In order to control the biasing of the output stage, the circuit presented in Figure 4-59 may be modified as shown in Figure 4-62 to get current controlled current conveyer (CCCII),

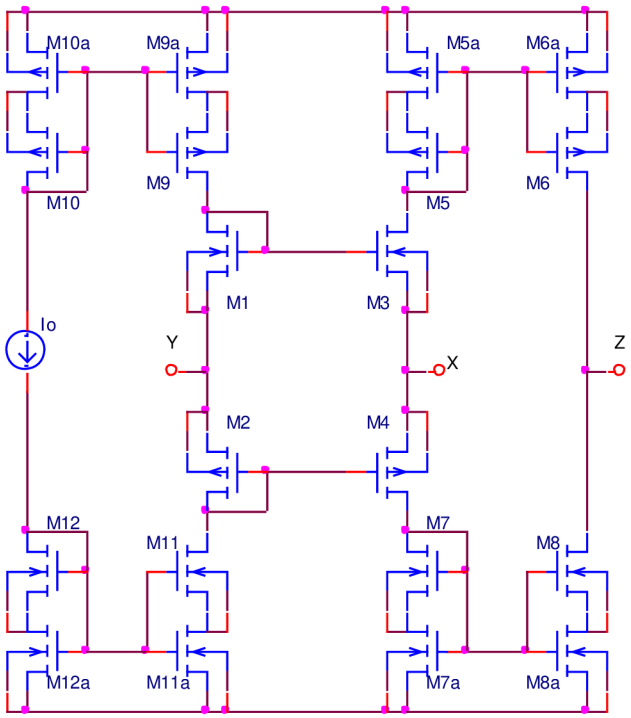


Figure 4-62 modified CCII based self cascode current mirror

The current Io controlling the biasing of the output stage, so modifying the parasitic resistance rx, Simulation results plotted in Figure 4-63 show that this resistance can be controlled between 22.5 kΩ and 1.4 kΩ by varying the current control in the range [1uA-140uA].

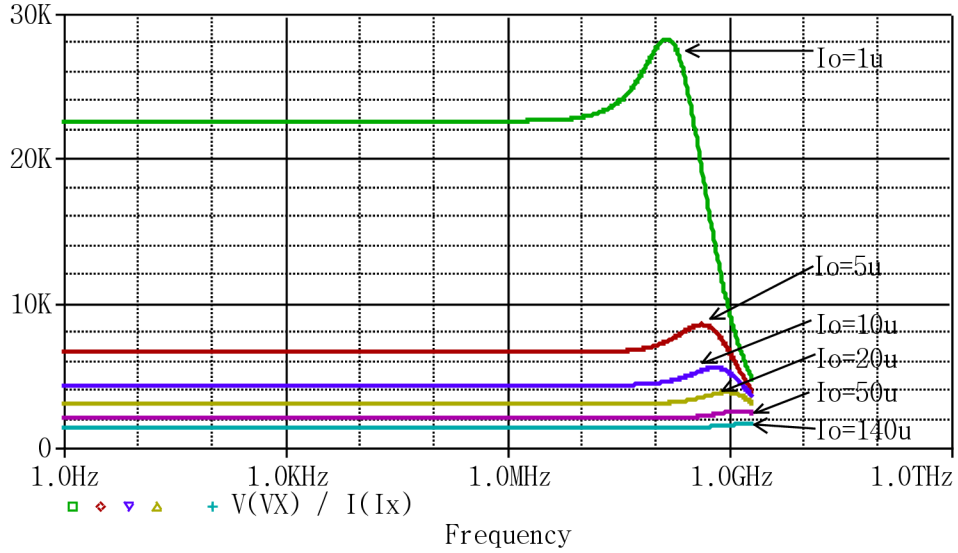


Figure 4-63 Io effect on rx of CCII based self cascode current mirror.

4.2.4.1 Self cascode CCCII band pass filter

This structure is used as a basic building block of a tunable current mode Band-pass filter is depicted in Figure 4-64 [86], [87]. When the CCII1, CCII2 and C1 implement the non ideal inductance, C2 is the shunt capacitor. The controlled negative resistance is used to cancel the effects of the parasitic shunt resistors (rx1 and rx2). Finally the out put current signal is obtained through CCII4.

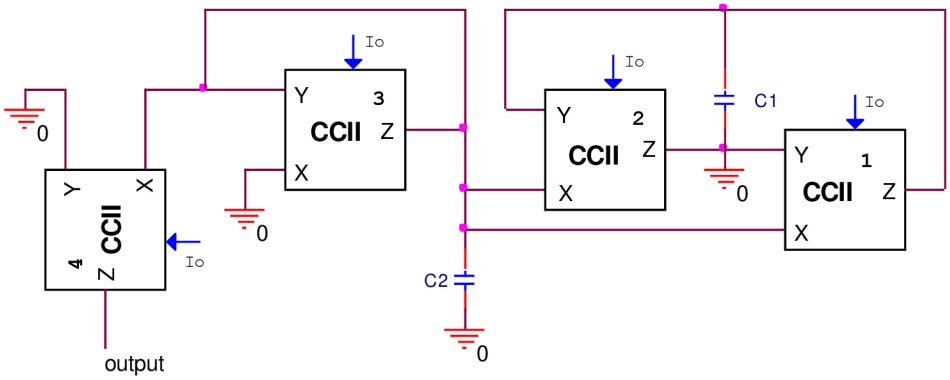


Figure 4-64 Second order filter block

The transfer function of the filter shown in Figure 4-64 is expressed by:

$$H(s)=\frac{i_{out}}{i_{in}}=\frac{S}{r_{X4}C_2S^2+\frac{r_{X4}}{r_g}S+\frac{r_{X4}}{L}} \qquad 4.58$$

$$L=R_{X1}R_{X2}C \qquad 4.59$$

$$\frac{1}{r_g} = \frac{1}{r_{X1}} + \frac{1}{r_{X2}} - \frac{1}{r_{X3}} + \frac{1}{r_{X4}} \qquad 4.60$$

Its resonance frequency and its quality factor are respectively given by the following expressions:

$$\omega_0 = \frac{1}{\sqrt{r_{X1} r_{X2} C_1 C_2}} \qquad 4.61$$

$$Q = \frac{r_g}{\sqrt{r_{X1} r_{X2}}} \sqrt{\frac{C_2}{C_1}} \qquad 4.62$$

4.2.4.2 SIMULATION RESULTS

The Q-factor and the central frequency can be electronically controlled by mean of DC bias current. To validate this result, a Pspice simulation results plotted in Figure 4-65, Figure 4-66 are showing very interesting frequency and Q factor performances, a tunable central frequency in the range of 100 MHz to 120 MHz and a high tunable Q-factor.

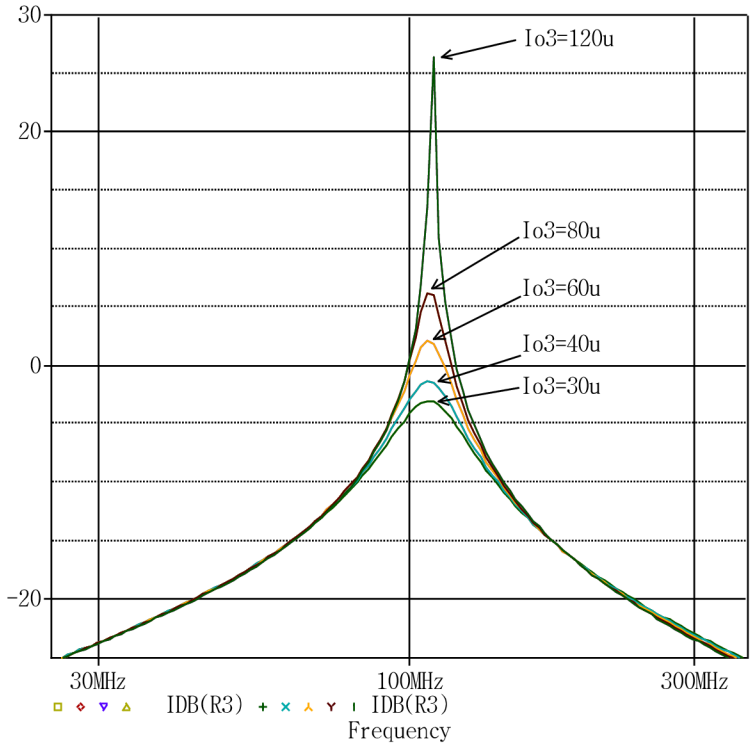


Figure 4-65 tuning of Q factor of band pass filter.

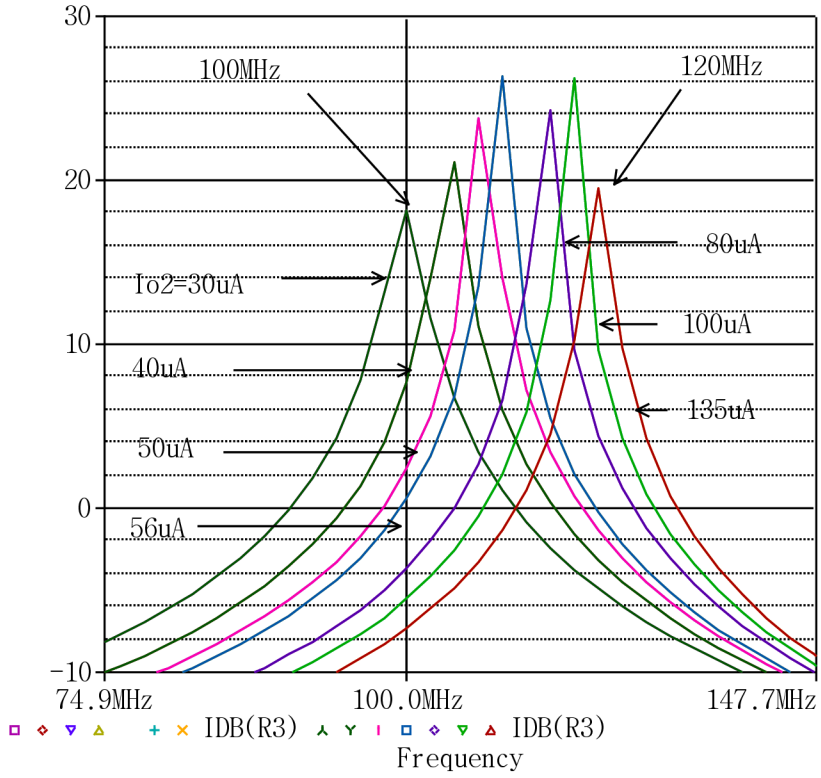


Figure 4-66 resonance frequency tuning of band pass filter.

The central frequency can be adjusted independently of the Q-factor with C1*C2 if the ratio C2/C1 is left constant. And the Q-factor can be tuned from rx3 or rx4 (Io3or Io4) without changing the central frequency. It's desirable to adjust the central frequency after integration but not allowed to change the capacitor's values, the solution comes by varying values of the rx1 and rx2 (Io1 or Io2).

Finally a new architecture of self cascode CCII is presented. The CCII operates at low supply voltage. Simulations using Pspice confirm the good performance of such conveyor. The current mode high Q-factor and high frequency band pass filter is constructed. This architecture is electronically tuned by varying the DC bias current of the conveyor.

5 Conclusion

In the framework of this thesis, it is clear that the main objectives and intentions set out in the beginning of this thesis have been achieved. It is shown that low voltage current conveyor have the potential to satisfy the requirements set out in analog requirements.

The work start by giving CC back ground, in first a brief history of the first, second and third generation current conveyors and the classification of them has explained, then the CCII considered as the main building block in the main active feed back devices and in the implementation of analog functions, as an alternative of operational amplifiers.

The basic device level technique which also play important role in the design of smarter and efficient circuits has presented with some circuit solutions and a design examples for low voltage CCIIs.

This work has mainly focused on circuit design techniques that would permit the implementation of CCII at low power supply voltages in CMOS technology.

The primary limitations of analog circuits at low voltage are a large threshold voltage, large channel length modulation, and poor analog modelling. The last two limitations are caused by short-channel technology. The best solution to the large channel length modulation problem is the composite transistor (self cascode). The threshold voltage limitation is solved by the forward biasing the bulk-source junction (bulk driven).

Advantages of self-cascode are:

Proposed self-cascode technique provides wide input and output swing and high current transfer accuracy within a wide current range. The advantages of self-cascode circuits are numerous, and include the ability to implement a low voltage CCII with good performance characteristics.

It was shown that, a single 5-transistor differential gain stage can be enough for the proposed current mirror to make use of the regulated cascode scheme to enhance the output resistance.

Simulations proved that self cascode current mirrors can be used to build low-voltage high-linearity, high current- efficiency current output stages, these structures are also suitable for low-voltage design of other current-output-based active devices, such as current conveyor based operational amplifiers.

Disadvantage of self-cascode are:

The requirement of the expensive technology to allow for multiple threshold voltage values in Self-cascode MOSFETs.

Advantages of bulk driven:

Removes the threshold voltage requirements and the device can be operated at low supply voltages. Due to depletion characteristics zero, negative, and even small positive values of bias voltage can be applied to get the desired dc currents.

Bulk-driven MOSFETs can work even at 0.9 V (for VT $\approx$ 0.8) and we can use conventional gate to modulate the bulk-driven MOSFETs i.e. the on-off ratio of bulk driven MOSFET modulated by the gate is very large as the gate can totally shutoff the

channel. Moreover experiments simulation show that latch-up problem has not appeared.

The small-signal transconductance, gmb can be larger than the MOSFET's transconductance, gm if VBS $\geq$ .5V. But there will be appreciable current flowing in bulk source junction under these conditions.

The New LV current conveyor based on bulk-driven current mirror have been constructed after simulation approved that is need low voltage supply requirement, have low voltage dissipation, acceptable voltage range and voltage swing for the Y terminal that could not otherwise be achieved at low power supply voltages.

Disadvantages in bulk driven are:

The polarity of the bulk-driven MOSFETs is process related. For P-well process, only N channel bulk-driven MOSFETs are available, and for N-well process, only P-channel MOSFETs are available. Thus, bulk-driven MOSFETs cannot be used in CMOS structures where both N channel and P channel MOSFETs are required.

Bulk-driven MOSFETs are fabricated in differential wells to have isolated bulk terminal and the matching between bulk-driven MOSFETs in differential wells suffers. Thus the analog circuit with tight matching between MOSFETs is difficult to fabricate.

Noise is also a problem for the bulk-driven MOSFET.

This work is believed to be the first instances where CCII-based bulk driven and self cascode cells were presented.

In current mode architecture, the CCII can be considered the basic building block because all the active devices can be made of suitable connection of one or two CCIIs, to perform that, at the end of this thesis two filter topologies using CCII have constructed.

A current-mode biquad filter with one input and three outputs, using unity gain novel dual output current conveyors as low voltage active elements, has been presented. The proposed circuit has the attractive features.

In last part a new architecture of self cascode CCII is used to construct tunable current mode band pass filter, simulations show interest results.

To conclude, we summarize the contributions of the present work to say; new architectures of CCII are presented. The CCIIs designed using model 0.7um process from AMIS to operate at low supply voltage and showing good performance are verified. Simulations using Pspice orcad 9.2 confirm good performance of such conveyor and validity of using it in analog functions.

The future work is involve low voltage low power rail to rail class AB CCII topologies that can be implemented with low voltage design techniques.

6 References

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8 Appendixes

8.1 Appendix A

Spice model files used for Process and electrical parameters CMOS 0.7um from AMI Semiconductor BELGIUM

```
* C07MA & C07MD NMOS PMOS Typical model
*AMI Semiconductor Belgium BVBA
* Release 3.2, Installation date: dd/mm/98
*Revision date: 16-Jul-2002
*Valid range for n channel and p channel models' >= 0.7um, W >= 0.8um.
* Temperature: -55 -> 150 degrees C (study @ 27, 85 and 125 degrees C)
*-------------------------------------------------------------------------------------------------------------
*********************************************************************************
.MODEL NMOS NMOS LEVEL = 7 ;53
+TNOM = 27              TOX = 1.75E-8           XJ = 2.5E-7
+NCH = 1.7E17           NSUB = 4E16             VTH0 = 0.76
+K1 = 0.8219166         K2 = -8.54312E-3        K3 = 11.1089581
+K3B = -1.9786631       W0 = 1E-6               NLX = 3.751355E-8
+DVT0W = 0              DVT1W = 0               DVT2W = -0.032
+DVT0 = 5.2254747       DVT1 = 0.590721         DVT2 = -0.05
+VBM = -5               U0 = 635.6142994        UA = 1.983902E-9
+UB = 1E-21             UC = 4.667652E-11       VSAT = 9.5E4
+A0 = 0.9331753         AGS = 0.1339124         B0 = 0
+B1 = 0                 KETA = -2.746786E-5     A1 = 0
+A2 = 1                 RDSW = 1.573286E3       PRWG = 6.719929E-6
+PRWB = -1E-3           WR = 1                  WINT = 6.065442E-8
+LINT = 2.87042E-8      DWG = -1.268839E-8      DWB = 1.654199E-8
+VOFF = -0.15           NFACTOR = 0.6887273     CIT = 0
+CDSC = -1E-4           CDSCD = 0               CDSCB = 2E-3
+ETA0 = 0.08            ETAB = -0.07            DSUB = 0.56
+PCLM = 1.0175962       PDIBLC1 = 0.032818      PDIBLC2 = 2.506552E-3
+PDIBLCB = -1E-6        DROUT = 0.6067512       PSCBE1 = 3.356583E8
+PSCBE2 = 5E-5          PVAG = 0.0168906        DELTA = 0.01
+ALPHA0 = 5E-7          BETA0 = 26              RSH = 65
+MOBMOD = 1             PRT = 159.2464225       UTE = -1.9522848
+KT1 = -0.4126334       KT1L = 7.244799E-9      KT2 = 2.671323E-3
+UA1 = 8.353648E-11     UB1 = -2.12098E-19      UC1 = -5.6E-11
+AT = 3.3E4             NQSMOD = 0              WL = 0
+WLN = 1                WW = 0                          WWN = 1
+WWL = -5.30182E-20     LL = 0                  LLN = 1
+LW = 0                 LWN = 1                 LWL = 0
+AF = 1                 KF = 3E-28              CAPMOD = 2
+CGDO = 4E-10           CGSO = 4E-10            CGBO = 3.35E-10
+CJ = 5E-4              PB = 0.73               MJ = 0.35
+CJSW = 2.8E-10         PBSW = 0.8              MJSW = 0.21
+JS = 1E-03             XPART = 0               ELM = 5
*
```

```
**********************************************************************
*
.MODEL PMOS PMOS LEVEL = 7 ;53
+TNOM = 27              TOX = 1.75E-8           XJ = 3E-7
+NCH = 1.7E17           NSUB = 4E16             VTH0 = -1.00
+K1 = 0.563991          K2 = 0                  K3 = 16.3317811
+K3B = -2.9202228       W0 = 1.23464E-6         NLX = 9.69545E-8
+DVT0W = 0              DVT1W = 0               DVT2W = -0.032
+DVT0 = 3.5648008       DVT1 = 0.3898843        DVT2 = -0.0284121
+VBM = -10              U0 = 235.7724356        UA = 2.964616E-9
+UB = 1.419129E-18      UC = -7.00385E-11       VSAT = 1.1E5
+A0 = 0.4590784         AGS = 0                 B0 = 0
+B1 = 1.407805E-9       KETA = -0.047           A1 = 0
+A2 = 1                 RDSW = 3E3              PRWG = 2.024978E-3
+RSH = 94               PRWB = 7.428781E-5      WR = 1
+WINT = 10.669321E-8    LINT = 1.9089522E-8     DWG = -1.478082E-8
+DWB = 1.561823E-8      ALPHA0 = 0              BETA0 = 30
+VOFF = -0.1064652      NFACTOR = 0.4324039     CIT = 0
+CDSC = 2.4E-4          CDSCD = 0               CDSCB = 0
+ETA0 = 9.999059E-4     ETAB = -1.999936E-4     DSUB = 0.998946
+PCLM = 2.6025265       PDIBLC1 = 1             PDIBLC2 = 2.853174E-4
+PDIBLCB = 0            DROUT = 0.3837047       PSCBE1 = 4.249266E8
+PSCBE2 = 5E-5                  PVAG = 3.8222424        DELTA = 0.01
+MOBMOD = 1             PRT = 216.4347715       UTE = -1.2989809
+KT1 = -0.4521998       KT1L = -2.091783E-8     KT2 = -0.040013
+UA1 = 3.100822E-9      UB1 = -1E-17            UC1 = -8.35439E-11
+AT = 3.289E4           NQSMOD = 0              WL = 0
+WLN = 1                WW = 0                          WWN = 1
+WWL = -2.33876E-20     LL = 0                  LLN = 1
+LW = 0                 LWN = 1                 LWL = 0
+CAPMOD = 2             CGDO = 1.0E-10                  CGSO = 1.0E-10
+CGBO = 3.35E-10        CJ = 6.0E-4             PB = 0.9
+MJ = 0.51              CJSW = 3.6E-10          MJSW = 0.35
+AF = 1                 KF = 5.0E-30            JS = 1E-3
+XPART = 0              ELM = 5
*
*-------------------------------------------------------------------------------------------------------------------
```

8.2 Appendix B

Data of simulated schematics.
In this section transistor dimensions and component value and parameter and then one net list and output file for biquad filter as example.

Figure 2 19 CCII based CM characteFigure 8-1ristics.
VDD& VSS=±2.5V

Transistor	W(µm)	L(µm)
M1-M2	8	1
M3-M4	24	1
M7-M8	7	3
M11-M12	7	3
M5-M6	30	3
M9-M10	30	3

Figure 2 26 CCII- based on the Miller compensated operational amplifier.
VDD&VSS=±1.5V, R1=100 ohm, C1=1p, R2=70k.

Transistor	W(µm)	L(µm)
M1-M2	15	2
M3-M4	5	2
M5	30	2
M6,M8	100	1
M7,M9,M10	30	1

Figure 2 28 The push pull op amp.
VDD&VSS=±2V, VB=0.9V, C1=1p

Transistor	W(µm)	L(µm)
M1-M2	35	0.7
M3-M4	15	0.7
M5	35	0.7
M6	30	0.7
M7-M8	85	1
M9-M10	75	1
M11	20	0.7

Figure 2 30 The class AB op amp.
VDD&VSS=±2V, VB1=0.9, VB2=-0.9,

Transistor	W(µm)	L(µm)
M1-M2	66.7	1
M3-M4	186.6	1
M5, M11,M13	102.9	1.2
M6, M15	112	0.7
M7, M17	160.2	1
M8 ,M12,M14	34.3	1.2
M9, M18	10	0.7
M10, M16	68.5	1

Figure 2 33 Class AB CCII with improved biasing.
VDD&VSS=±1.2V, I3=10uA, I2 and I1=5uA, R1=1k, C1=2p

Transistor	W(µm)	L(µm)
M1-M2	6	2.5
M3-M4	18	2.5
M5, M6	180	2
M7, M8	60	2

Figure 2 35 Class AB CCII based on p-type differential pair.
VSS&VSS=±1V. I3=10uA, I2 and I1=10uA. R1=1k. C1=2p.

Transistor	W(µm)	L(µm)
M1-M2	5	1.5
M3-M4	5	1.5
M5, M7	100	2
M6, M8	40	1

Figure 2 37 LV rail to rail OTA based CCII.
VDD& VSS=±1V. Ibias1, Ibias2=4uA. I1, I2=2uAFigure 8-2. R1=1k.

Transistor	W(µm)	L(µm)
Mn1-Mn2	5	1.5
Mn3-Mn4	5	1.5
Mp1-Mp2	5	1.5
Mp3-Mp4	5	1.5
M9, M11	200	1
M10 ,M12	70	1

Figure 2 39 LV OTA based CCII.
VDD& VSS=±0.8V. I1, I2, I3=10uA. R1=400 ohm. C1=1p.

Transistor	W(µm)	L(µm)
M1-M8	5	1.5
M9,M11	80	1
M10-M12	23	1

Figure 4 35 CCII Self cascode OTA.
I1, I2=5uA. I3=10uA. R1=1K.C1=2p

Transistor	W(µm)	L(µm)
M1-M2	6	2.5
M1a-M2a	5	0.7
M3-M4	18	2.5
M5-M6	180	2
M7-M8	60	2

Figure 4 37 Self cascode output push pull Op. Amp
VDD&VSS=±2V, VB=1V, C1=1p

Transistor	W(µm)	L(µm)
M1-M2	35	0.7
M3-M4	15	0.7
M5	60	0.7
M7-M8	85	1
M7-M8	15	4
M7a-M8a	15	4
M9-M10	35	1
M9a-M10a	11	4

Figure 4 48 CCII based miller compensated bulk-driven op amp.
VDD& VSS=±0.6V.

Transistor	W(µm)	L(µm)
M1-M2	15	2
M3-M4	5	2
M5	30	2
M6, M8	100	1
M7, M9, M10	30	1

Figure 4.55 LV OTA based DOCCII scheme.
VDD, VSS=±1V. I1,I2,I3=20uA, R1=700Ω

Transistor	W(µm)	L(µm)
M1-M4	5	1.5
M5-M6	5	1.3
M7-M8	5	1.5
M9,M11,M13,M15,M17	80	2
M10,M12,M14,M16,M18	23	2

Figure 4 62 modified CCII based self cascode current mirror
Io= (1u-140u.)

Transistor	W(µm)	L(µm)
M1,M3	8	1
M2-M4	24	1
M5,M6,M9,M10	30	3
M5a,M6a,M9a,M10a	24	3
M7,M7a,M8,M8a	7	3
M11,M11a,M12,M12a	7	3